

ZR6 SYSTEM BLOCK DIAGRAM

BOM MARK
 IV@: INT VGA
 EV@: STUFF FOR EXT VGA
 SP@: STUFF FOR UMA or VGA

REV:C

DDR3 PWR TPS51116 P36	CHARGER ISL6251 P32
THERMAL PROTECTION P40	3/5V SYS PWR ISL6237 P33
DISCHARGER P39	CPU CORE PWR OZ8116LN P35
VGA CORE OZ8118 P37	+1.05V UP6111AQDD P34

CLOCK GENERATOR
 ICS:
 SELGO: SLG8SP512TTR P2

XTAL
 14.318MHz

Penryn 479
 uFCPGA P3, P4

Thermal Sensor
 (G780-1P81U) P3

Fan Driver
 (G991) P25

DDRIII
 SO-DIMM 0
 SO-DIMM 1 P16

NB Cantiga
 (GM45/ PM45/ GL40)
 P5, P6, P7, P8, P9, P10, P11

NVIDIA N10M-GE1
 VRAM DDRII 512MB P17-P23

SWITCH CIRCUIT P24

HDMI switch (PS8101T) P24

CRT P24

LVDS P24

HDMI P24

HDD (SATA) * P25

ODD (SATA) P25

Ext USB Port x 2
 USB 0,1 P26

Int USB Port x 1
 USB 7 P26

Bluetooth
 USB5 P26

CCD
 USB11 P24

SB ICH9M
 P12,P13,P14,P15

PCI-Express

PCI-E-1

Mini Card WLAN P26

Audio CODEC (CX20561) P27

EC (WPC775LDG) P31

Media Cardreader (RTS5159)
 USB2 P30

Atheros Giga-LAN (AR8131) P28

Audio Amplifier G1453L P27

MIC Jack P27

Int. MIC P27

Int. Speaker P27

SPI ROM P31

Touch Pad P25

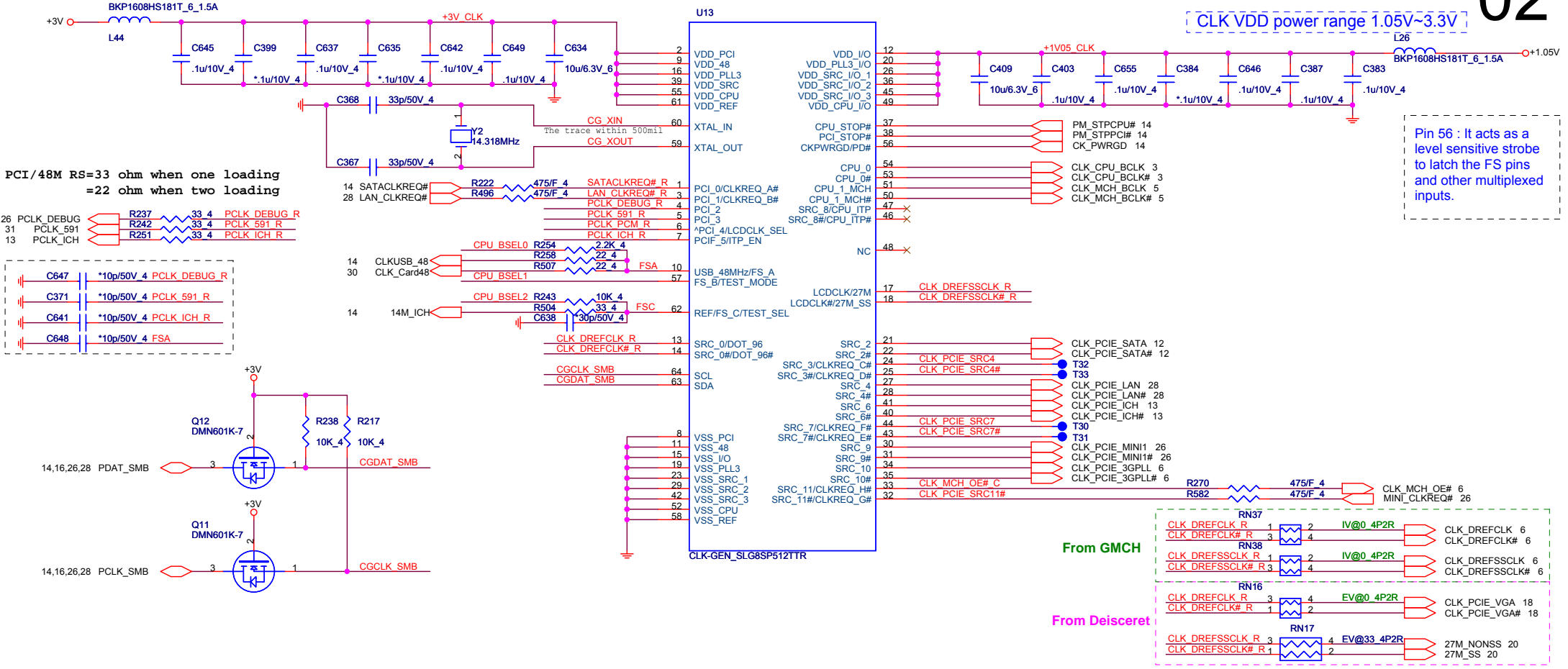
K/B COON. P31

Card Reader Connector P30

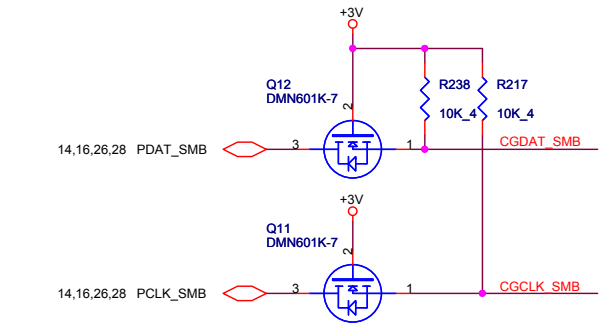
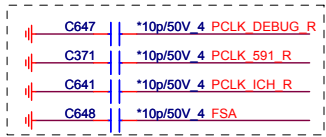
Transformer P29

RJ45 P29

Clock Generator (CLK)



PCI/48M RS=33 ohm when one loading
=22 ohm when two loading

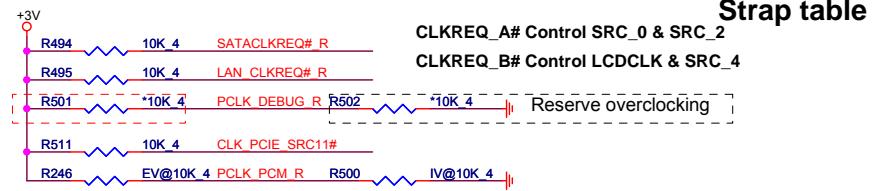
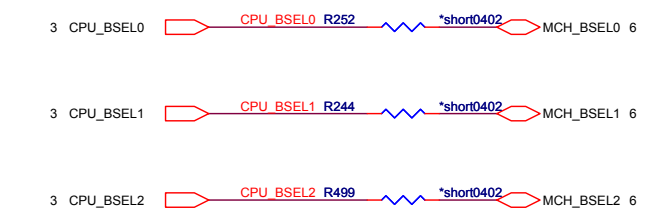


BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

CPU Clock select

Pin 10/57/62 : For Pin CPU frequency selection



Pin 6 : For Pin 13/14 and 17/18 selection
0 = LCDCLK & DOT96 for internal graphic controller support
1 = 27M & 27M_SS & SRC_0 for external graphic controller support

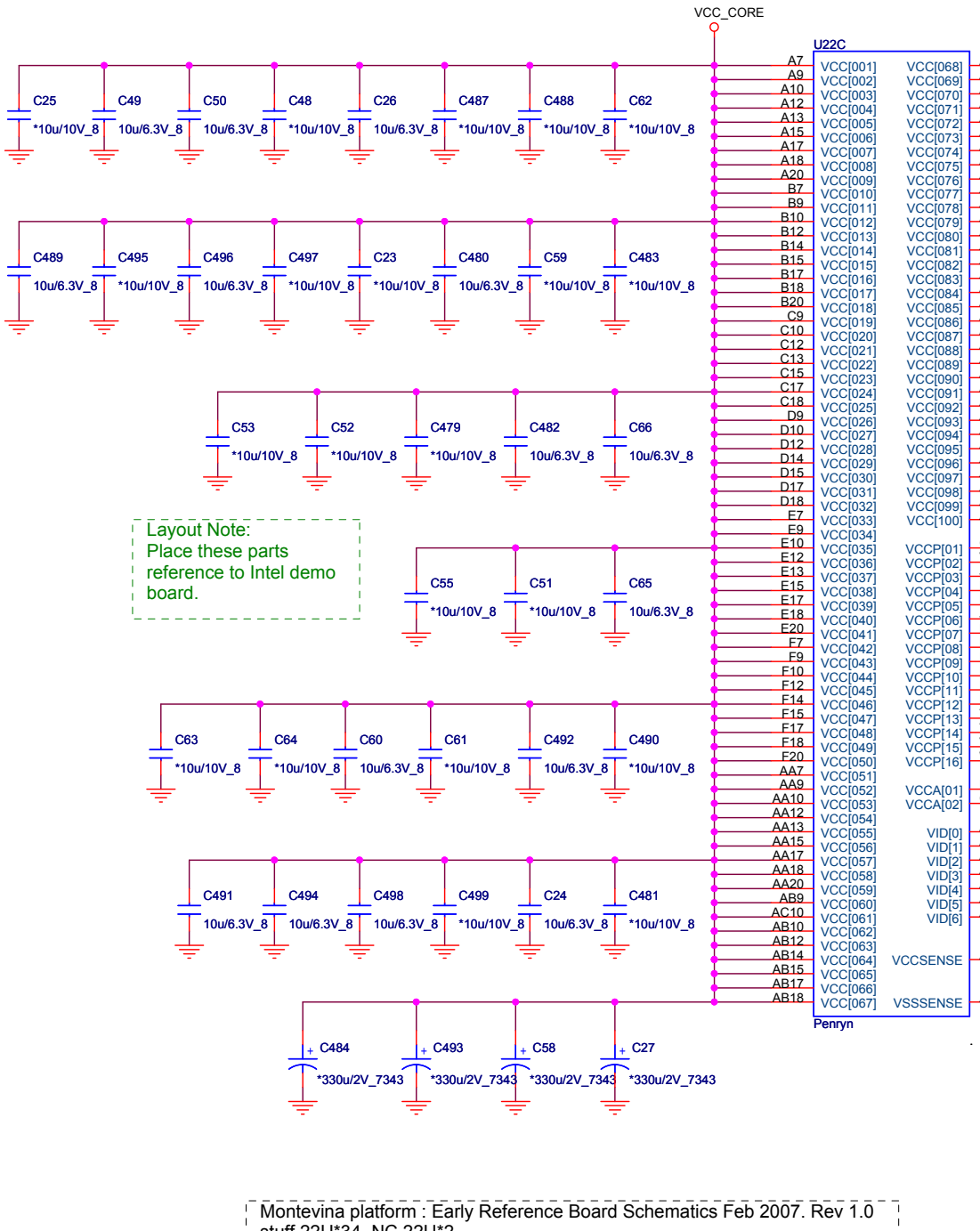
Pin 7 : For Pin 46/47 selection
1 = CPU_ITP
0 = SRC_8

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Size	Document Number	Rev 1A
CLOCK GENERATOR		
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CPU 2/2 (CPU)

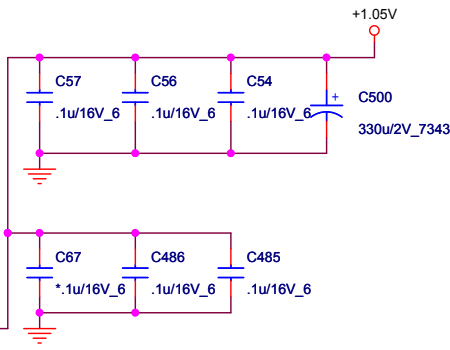
U22D		
A4	VSS[001]	P6
A8	VSS[002]	P21
A11	VSS[003]	P24
A14	VSS[004]	R2
A16	VSS[005]	R5
A19	VSS[006]	R22
A23	VSS[007]	R25
AF2	VSS[008]	T1
B6	VSS[009]	T4
B8	VSS[008]	T23
B11	VSS[010]	T26
B13	VSS[011]	U3
B16	VSS[012]	U6
B19	VSS[013]	U21
B21	VSS[014]	U24
B24	VSS[015]	V2
C5	VSS[016]	V5
C8	VSS[017]	V22
C11	VSS[018]	V25
C14	VSS[019]	V100
C16	VSS[020]	W4
C19	VSS[021]	W23
C2	VSS[022]	W26
C22	VSS[023]	Y3
C25	VSS[024]	Y6
D1	VSS[025]	Y21
D4	VSS[026]	Y24
D8	VSS[027]	AA2
D11	VSS[028]	AA5
D13	VSS[029]	AA8
D16	VSS[030]	AA11
D19	VSS[031]	AA14
D23	VSS[032]	AA16
D26	VSS[033]	AA19
E3	VSS[034]	AA22
E6	VSS[035]	AA25
E8	VSS[036]	AB1
E11	VSS[037]	AB4
E14	VSS[038]	AB8
E16	VSS[039]	AB11
E19	VSS[040]	AB13
E21	VSS[041]	AB16
E24	VSS[042]	AB19
F5	VSS[043]	AB23
F8	VSS[044]	AB26
F11	VSS[045]	AC3
F13	VSS[046]	AC6
F16	VSS[047]	AC8
F19	VSS[048]	AC11
F2	VSS[049]	AC14
F22	VSS[050]	AC16
F25	VSS[051]	AC19
G4	VSS[052]	AC21
G5	VSS[053]	AC24
G1	VSS[054]	AD2
G23	VSS[055]	AD5
H3	VSS[056]	AD8
H6	VSS[057]	AD11
H21	VSS[058]	AD13
H24	VSS[059]	AD16
J2	VSS[060]	AD19
J5	VSS[061]	AD22
J22	VSS[062]	AD25
J25	VSS[063]	AE1
K1	VSS[064]	AE4
K4	VSS[065]	AE8
K23	VSS[066]	AE11
K26	VSS[067]	AE14
L3	VSS[068]	AE16
L6	VSS[069]	AE19
L21	VSS[070]	AE23
L24	VSS[071]	AE26
M2	VSS[072]	A2
M5	VSS[073]	AF6
M22	VSS[074]	AF8
M25	VSS[075]	AF11
N1	VSS[076]	AF13
N4	VSS[077]	AF16
N23	VSS[078]	AF19
N26	VSS[079]	AF21
P3	VSS[080]	A25
	VSS[081]	AF25
	VSS[163]	



VCC:38A (Low power type)
VCC:47A (Standard type)

Layout Note:
Inside CPU center cavity in 2 rows

VCCP : 2.5A(Supply after VCC Stable)
4.5A(Supply before VCC Stable)



Layout Note:
Place these parts
reference to Intel demo
board.

VCC_A:130mA

Layout Note:
Z0=27.4,PU/PD L<1"

Montevina platform : Early Reference Board Schematics Feb 2007. Rev 1.0
stuff 22U*34, NC 22U*2
stuff 330U*2, NC330U*2

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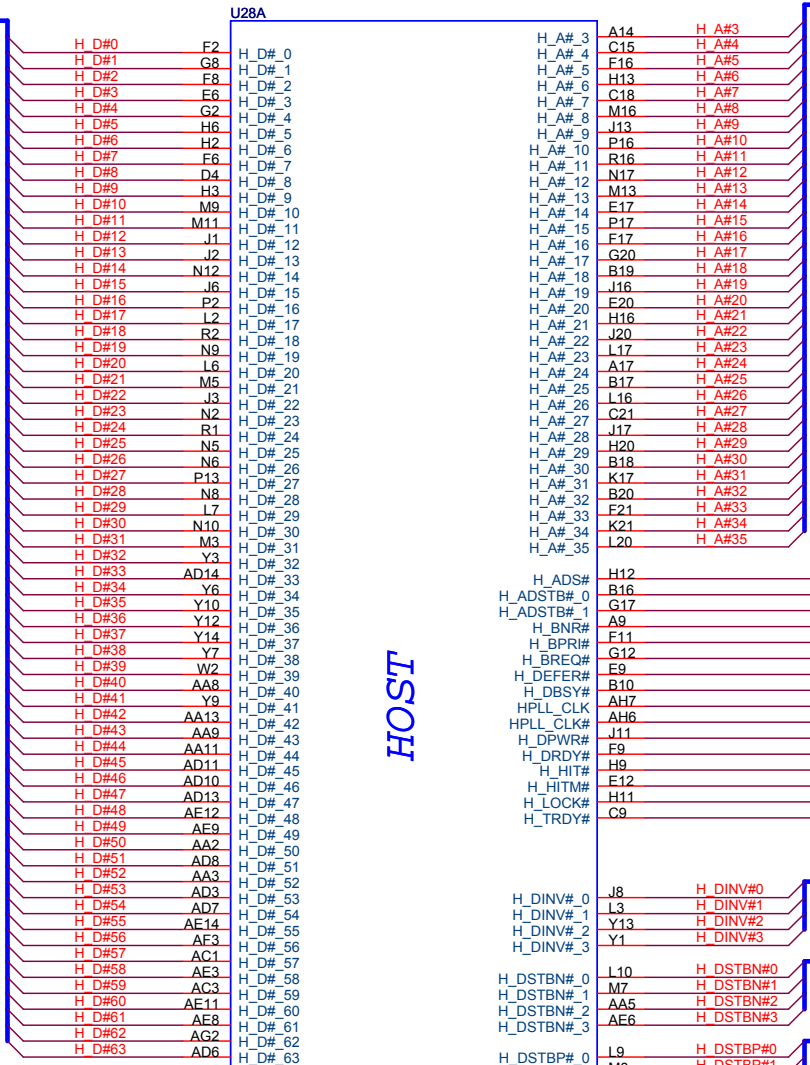
CPU Power

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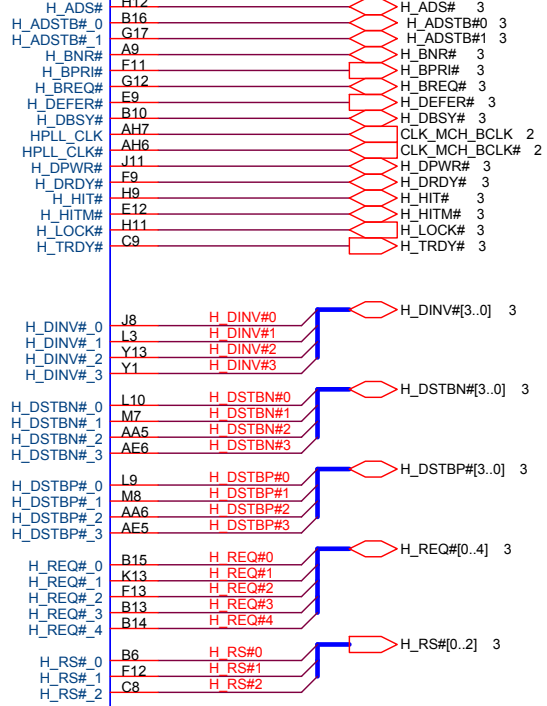
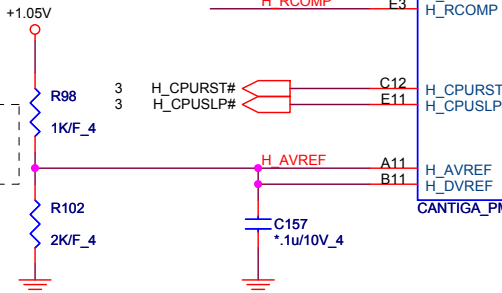
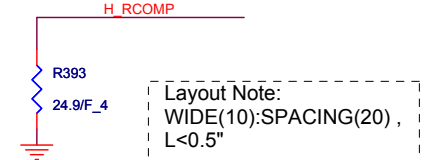
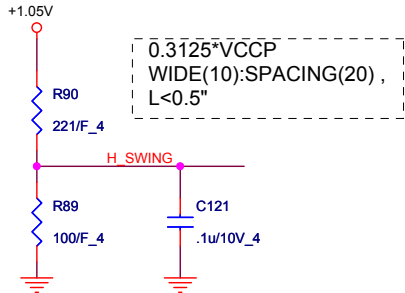
GMCH-CANTIGA(CLG)

	QCI P/N
Intel Cantiga (G)M	AJSLB940T04
Intel Cantiga (P)M	AJSLB970T06
Intel Cantiga (G)L A1	AJSLGGM0T04

3 H_D#0..63



H_A#[3..35] 3



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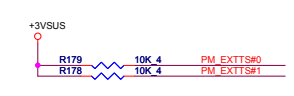
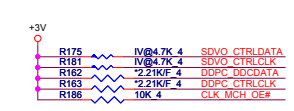
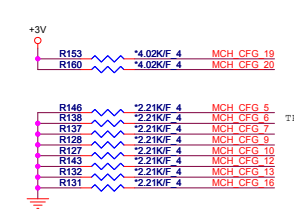
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GMCH HOST		
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Strap table

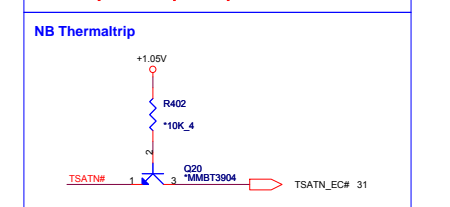
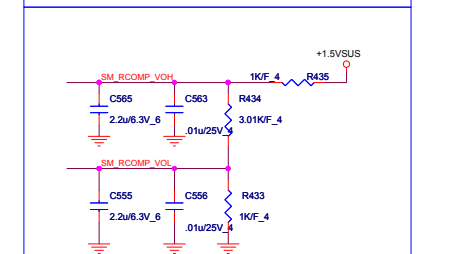
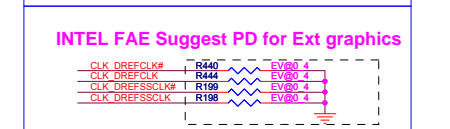
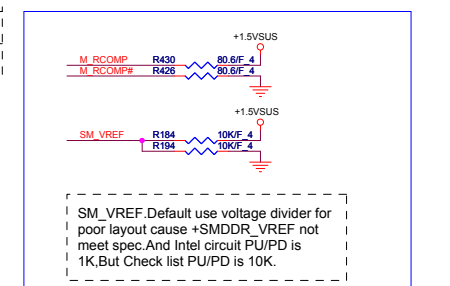
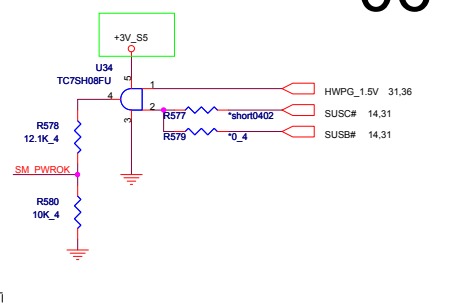
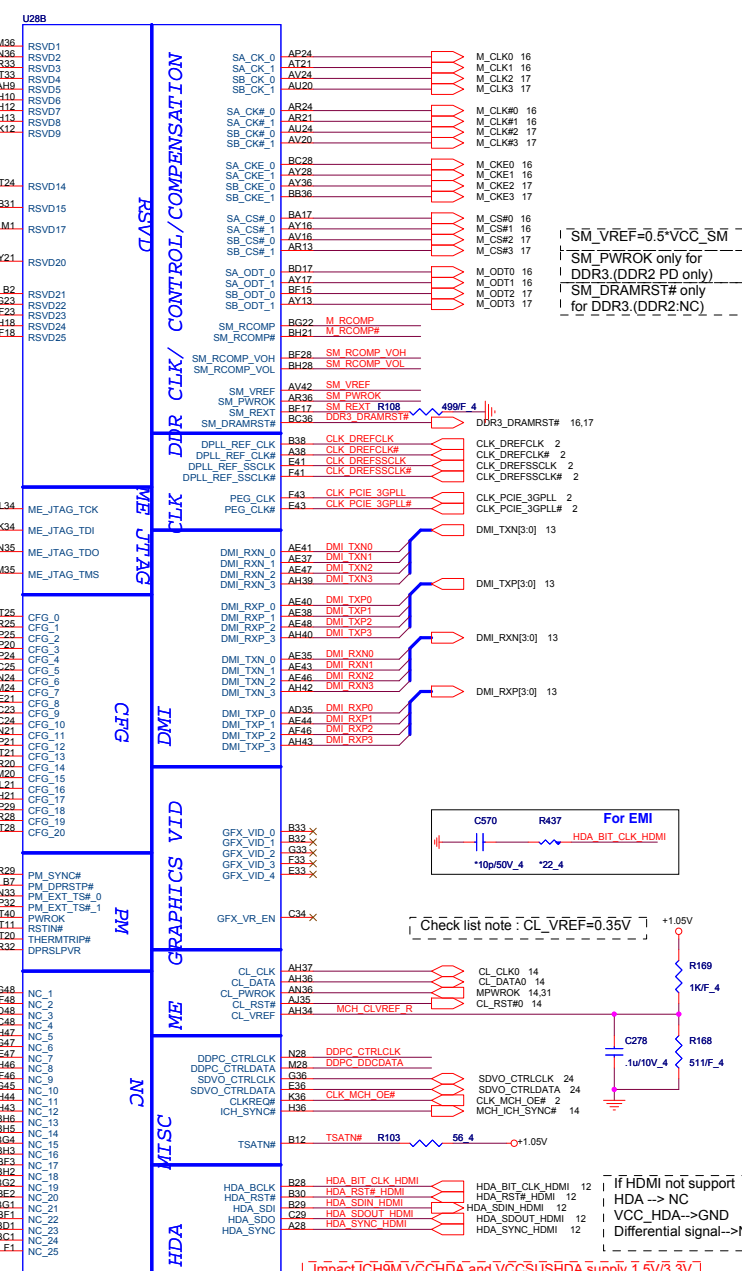
Pin Name	Strap description	Configuration
CFG2[2:0]	FSB Frequency Select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)
CFG8	Reserved	
CFG9	PCIe Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG10	PCIe Loopback enable	0 = Enabled 1 = Disabled (Default)
CFG11	Reserved	
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed
CFG20	Digital Display Port (SDVO/DP/iHDMI)	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIe is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI Device Present(Default) 1 = SDVO/HDMI Device present
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent (Default) 1 = Digital display(HDMI/DP) device present

Strap pin



NB Thermal trip pin
No use Thermal trip NB side can NC, (NB has ODT)

PM DPRSTP#
The Daisy chain topology should be routed from ICH9M to IMVP, then to (GMCH and CPU, in that order).



DDPC_CTRL for HDMI port C
SDVO_CTRL for HDMI port B

<Checklist ver0.8>
If TSATN# is not used, then it must be terminated with a 56-Ω pull-up resistor to VCCP.

<Pin out check issue>
Cantiga EDS 0.7 change Ball B12 to TSATN# from TSATN

Impact ICH9M VCCHDA and VCCSUSHDA supply 1.5V/3.3V

NOTE:
If (G)MCH's HD Audio signals are connected to ICH9M for iHDMI, VCCHDA and VCCSUSHDA on ICH9M should be only on 1.5V. These power pins on ICH9M can be supplied with 3.3V if and only if (G)MCH's HDA is not connected to ICH9M. Consequently, only 1.5V audio/modem codecs can be used on the platform.

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GMCH DMI

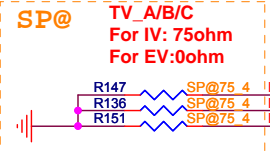
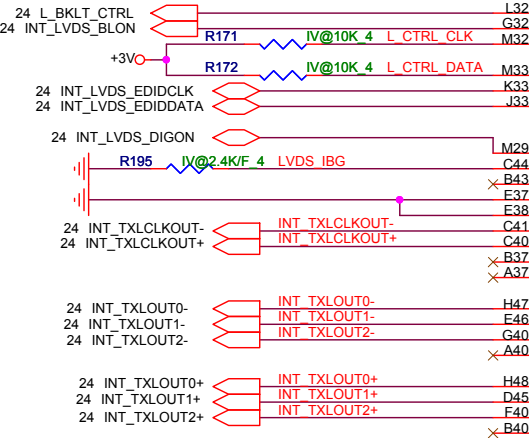
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GMCH-CANTIGA(CLG)

IV&EV Dis/Enable setting

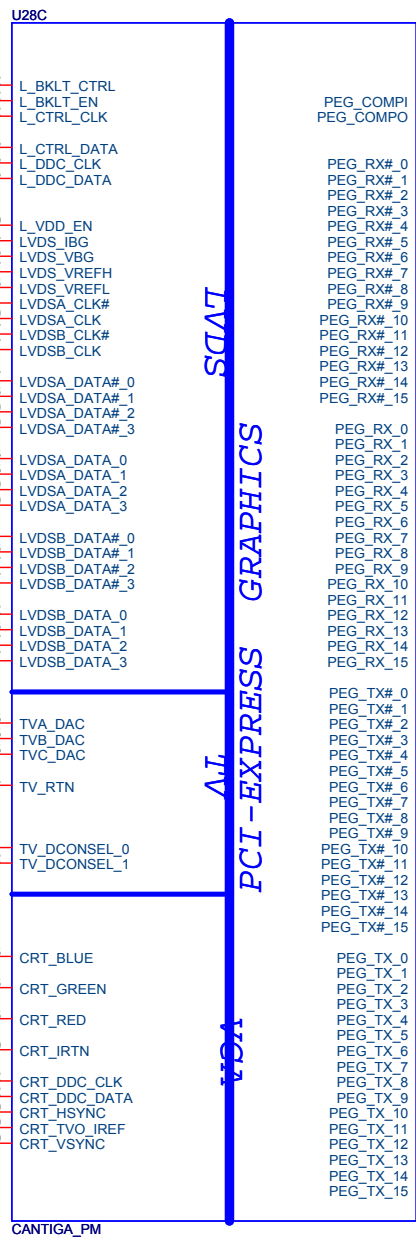
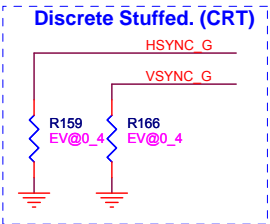
If LVDS no use, all signal can NC

IV@
EV@
SP@

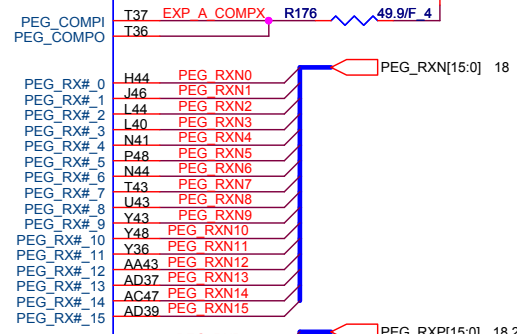


HSYNC/VSYNC serial R place close to NB

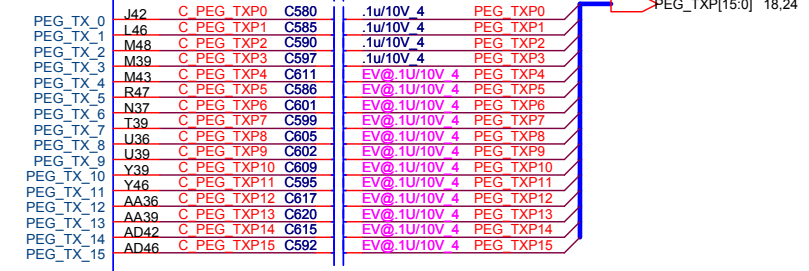
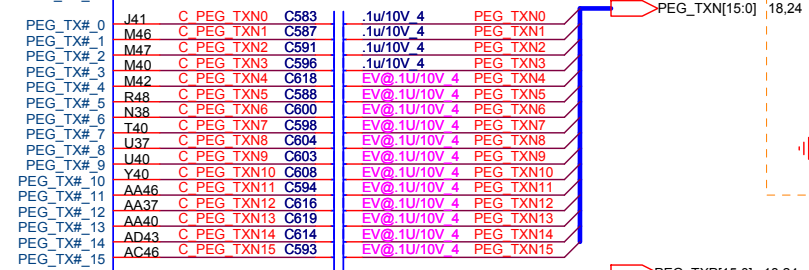
CRTIREF pull down for IV cantiga 1.02k ohm/F



L<0.5", If PCIe not support still connect to +VCC_PEG



Can support reversal routing. If CFG9=1, PCI Express is normal operation. If CFG9=0, then PEG_TXP0 becomes PEG_TXP15, PEG_TXP1 becomes PEG_TXP14, PEG_TXP2 becomes PEG_TXP13, etc. similarly for PEG_RXP[15:0] and PEG_RXN[15:0]



IV&EV Dis/Enable setting
 <5/31>Montevina_Schematics_Checklist_Rev0_8
 a) For TVOUT Disabled, TV_DCONSEL[1:0] Connect to GND. But design guide Rev0.7 show NC. What is correct.
 b) For CRT DAC Disable, CRT_DDC_CLK, CRT_DDC_DATA, CRT_HSYNC, CRT_VSYNC these signals should be connected to GND. But design guide Rev0.7 show NC, Intel suggest follow Design guide.

<check list> For EV@
 CRT R/G/B 0ohm to GND
 CRTIREF 0ohm to GND

<check list> For IV@
 CRT R/G/B 150ohm to GND
 CRTIREF 1Kohm to GND

For topology without the analog switch - if the total motherboard route length is less than 12", the recommended reference resistor value is 1 kΩ ±1%

CRTIREF
 For IV: 1Kohm
 For EV: 0ohm



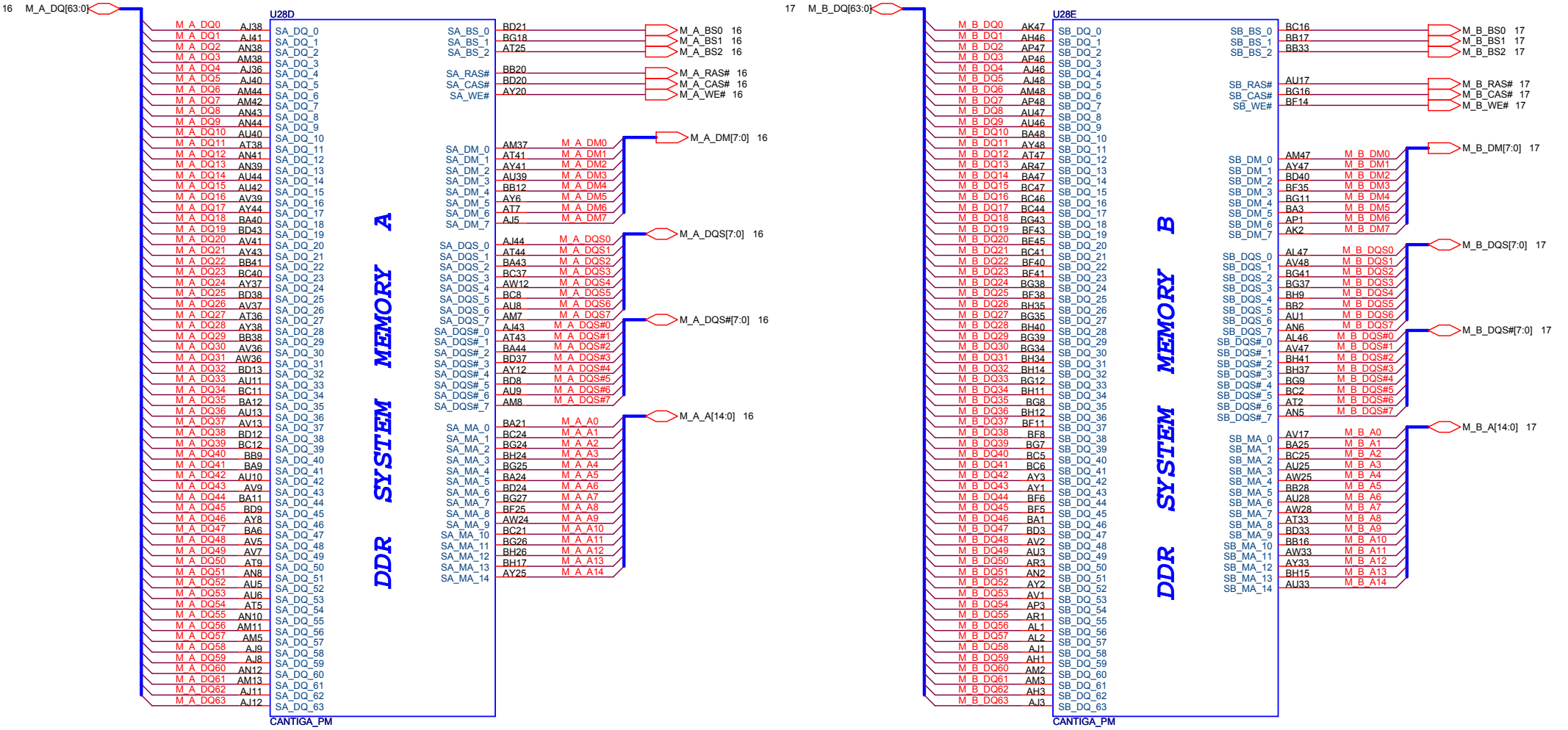
CRT R/G/B
 For IV: 150ohm
 For EV: 0ohm




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 GMCH VGA

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GMCH-CANTIGA(CLG)





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GMCH DDRIII		
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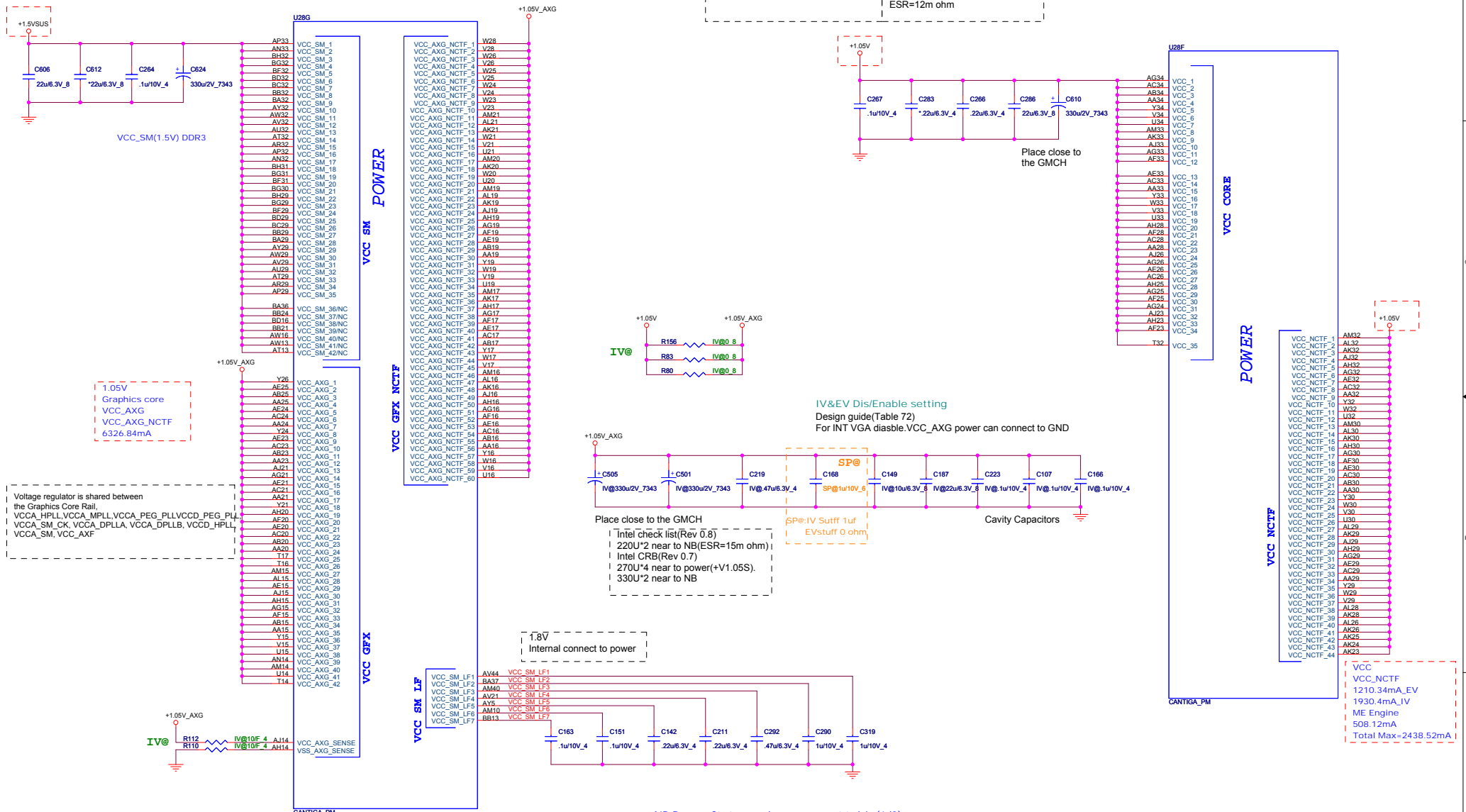
IV@

SP@

Power consumption reference to Intel 644135 Cantiga chipset EDS Volume1. Section 10
 GM TDP 10.5-12W
 GS TDP 7-8W
 PM TDP 7W

Intel check list(Rev 0.8)
 No description for VCC_SM bulk CAP
 Intel CRB(Rev 0.7)
 330U*1 Reserve near to power
 330U*1 near to NB

Intel check list(Rev 0.8)
 270U*1 near to power(+V1.05M).
 270U*2 near to NB
 Intel CRB(Rev 0.7)
 270U*3 near to power(+V1.05M).
 270U*1 near to NB
 ESR=12m ohm



Voltage regulator is shared between the Graphics Core Rail.
 VCCA_HPLL, VCCA_MPLL, VCCA_PEG, PLLVCCD_PEG_PL, VCCA_SM_CK, VCCA_DPLLA, VCCA_DPLLB, VCCD_HPLL, VCCA_SM, VCCA_AXF

1.05V
 Graphics core
 VCC_AXG
 VCC_AXG_NCTF
 6326.84mA

Intel check list(Rev 0.8)
 220U*2 near to NB(ESR=15m ohm)
 Intel CRB(Rev 0.7)
 270U*4 near to power(+V1.05S).
 330U*2 near to NB

IV&EV Dis/Enable setting
 Design guide(Table 72)
 For INT VGA disable.VCC_AXG power can connect to GND

1.8V
 Internal connect to power

VCC_NCTF
 1210.34mA_EV
 1930.4mA_IV
 ME Engine
 508.12mA
 Total Max=2438.52mA

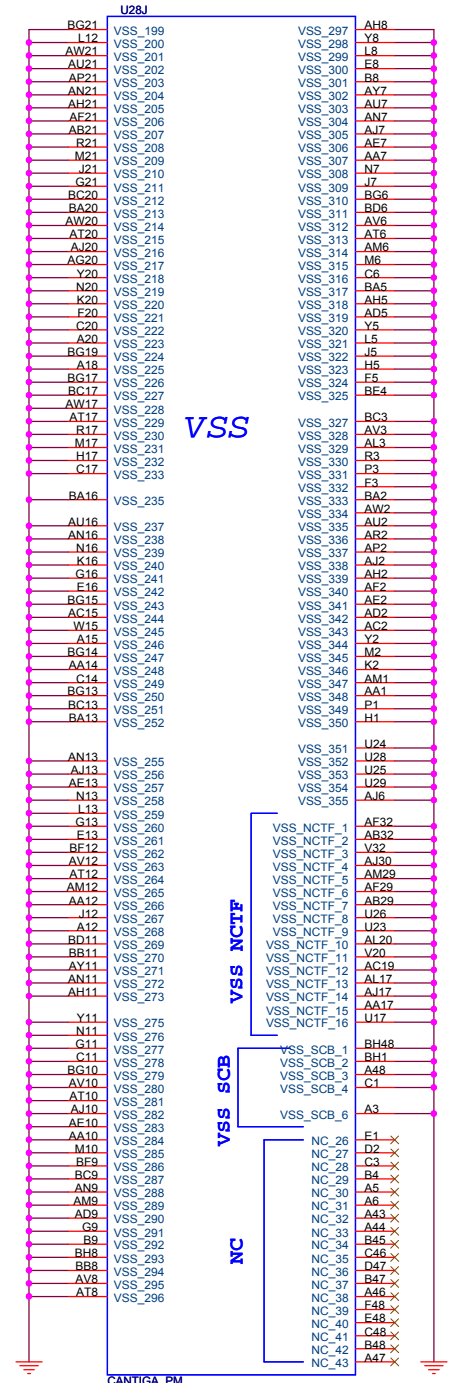
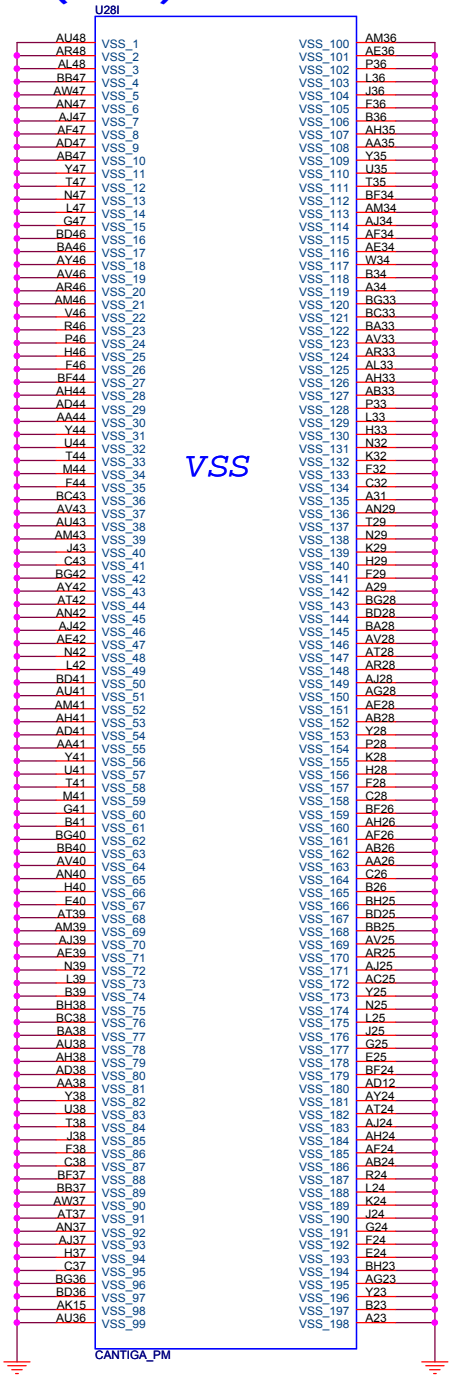
1. Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially
2. VCC_AXG_SENSE PU to +V_GFX_CORE_INT with 10ohm and VSS_AXG_SENSE PD with 10ohm for Intel suggest

NB Power Status and max current table(1/3)

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC(EXT_VGA)	O	X	X	+1.05V	2178mA	
VCC(INT_VGA)	O	X	X	+1.05V	2899mA	
VCC_AXG	O	X	X	+1.05V	8700mA	Graphics Core
VCC_SM(800)	O	O	X	+1.8VSUS	3A	(DDRII-667) 2.6A
VCC_SM(Standby)	O	O	X	+1.8VSUS	1mA	Self Refresh during S3

(See NB EDS Rev.1.0 Section 10.1 for max current)
 (See NB EDS Rev.1.0 Section 12.2 for DC voltage)

GMCH-CANTIGA(CLG)

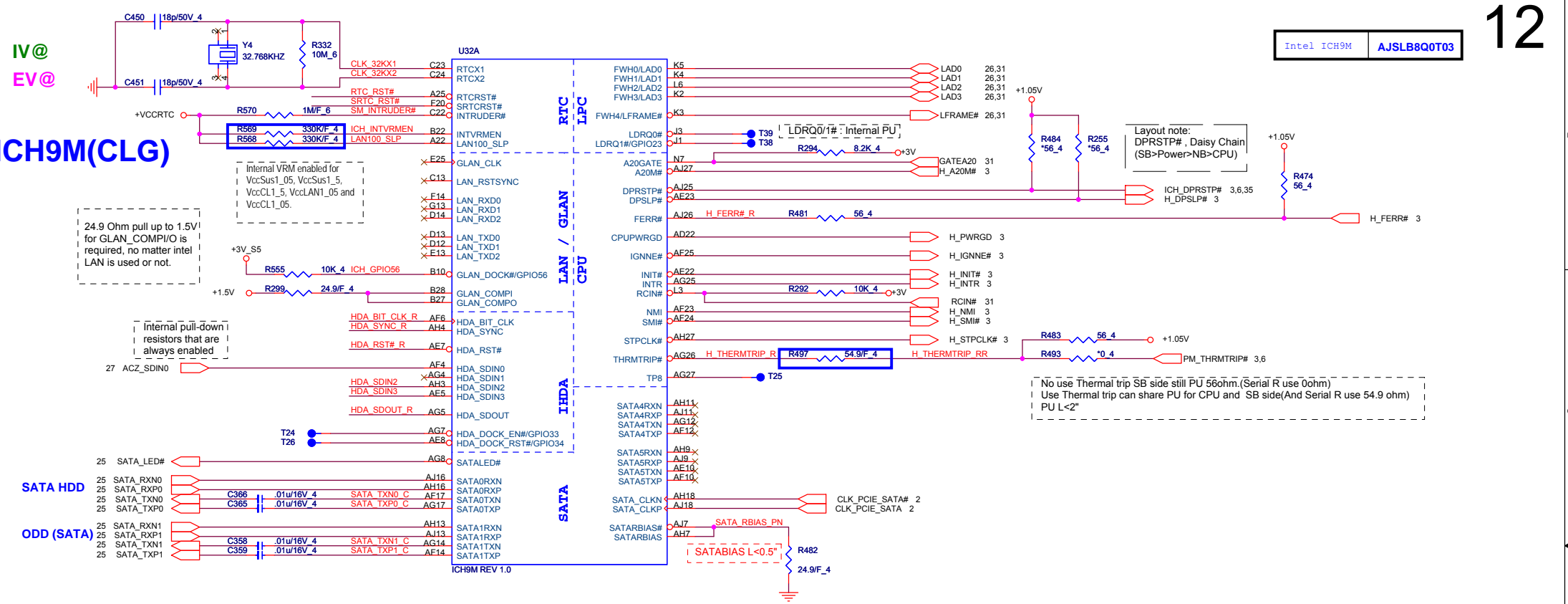


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GMCH VSS

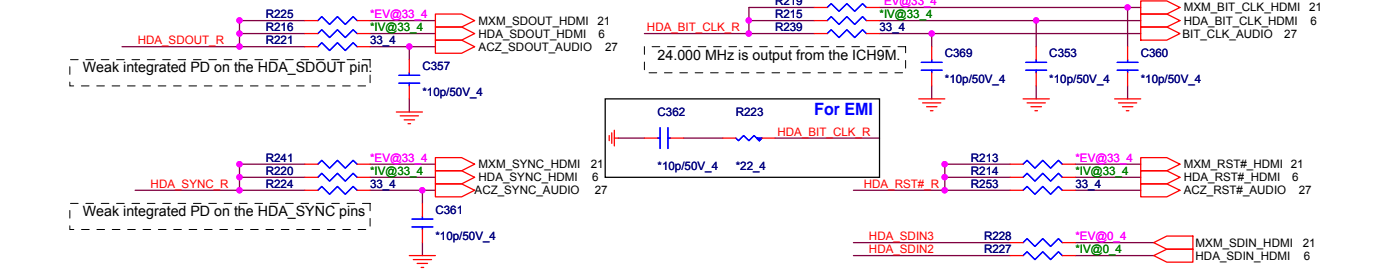
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IV@
EV@

ICH9M(CLG)



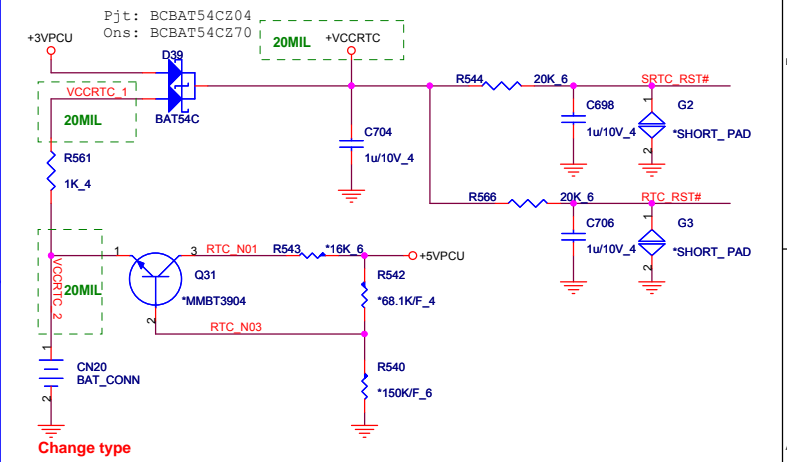
HD Audio



South Bridge Strap Pin (1/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD															
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.															
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU																
TP3	XOR Chain Entrance	PWROK	<table border="1"> <tr> <th>ICH_TP3</th> <th>HDA_SDOUR</th> <th>Description</th> </tr> <tr> <td>0</td> <td>0</td> <td>RSVD</td> </tr> <tr> <td>0</td> <td>1</td> <td>Enter XOR Chain</td> </tr> <tr> <td>1</td> <td>0</td> <td>Normal operation(Default)</td> </tr> <tr> <td>1</td> <td>1</td> <td>Set PCIe port config bit 1</td> </tr> </table>	ICH_TP3	HDA_SDOUR	Description	0	0	RSVD	0	1	Enter XOR Chain	1	0	Normal operation(Default)	1	1	Set PCIe port config bit 1	
ICH_TP3	HDA_SDOUR	Description																	
0	0	RSVD																	
0	1	Enter XOR Chain																	
1	0	Normal operation(Default)																	
1	1	Set PCIe port config bit 1																	
HDA_SDOUR	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK																	

RTC



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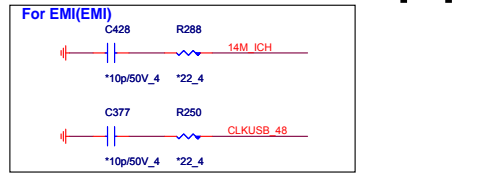
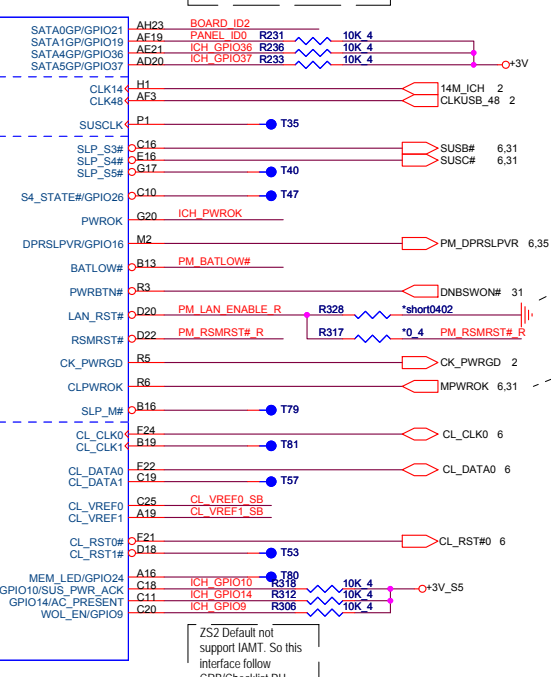
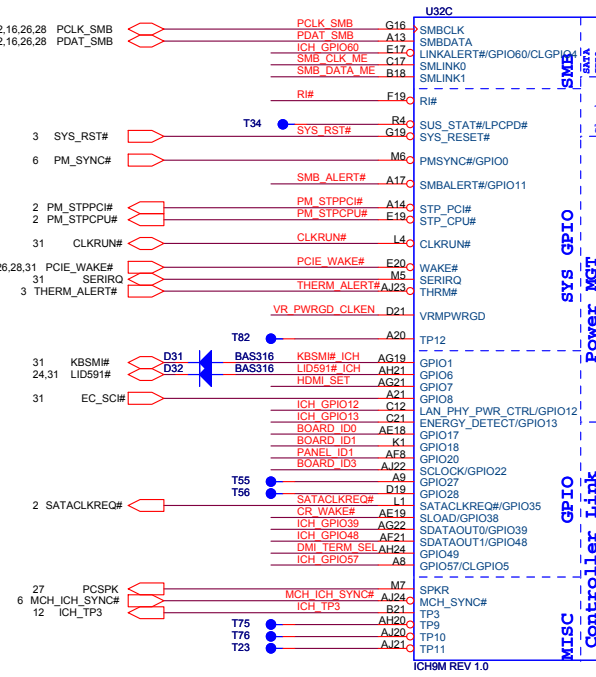
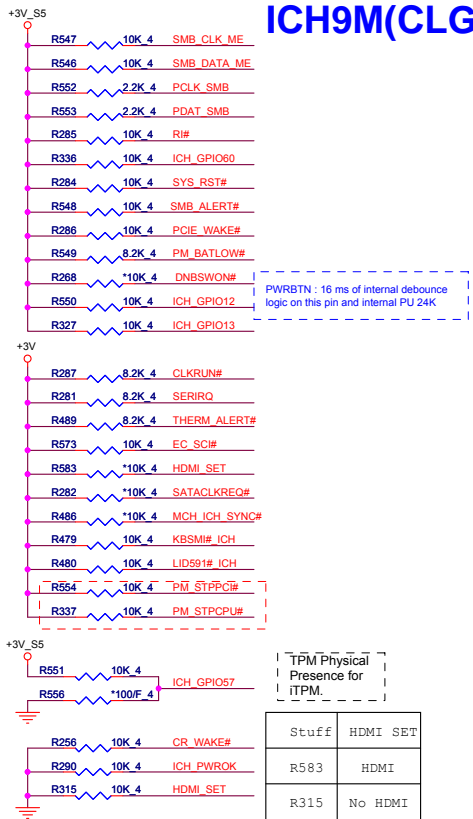
Size Document Number ICH9M HOST Rev 1A

Date: Monday, April 13, 2009 Sheet 12 of 42

ICH9M(CLG)

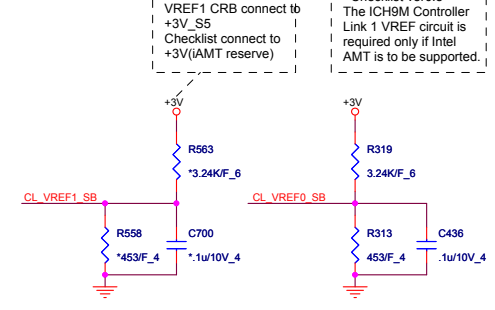
D3A:(1/31) ASSE:when iAMT is not implemented, ICH9M SMBus and SMLink should be connected together to support slave mode. Connect SMLINK0 to SMBCLK and SMLINK1 to SMBDATA (Add R474, R475 for debug use)

SATA[x]IGP pins if unused require 8.2-k to 10-k pull-up to Vcc3.3 or 8.2-k to 10-k pull-down to ground



<Checklist ver0.8>
 If integrated LAN is not used LAN_RST# tie to GND.NC serial R from RSMRST#.
 If Intel LAN is used with Wake On LAN, tie LAN_RST# to RSMRST# and NC 0ohm.
 CL_PWROK must not assert after PWROK asserts for iAMT.
 CL_PWROK to the NB and SB should be connected to existing PWROK inputs on the NB and SB on a platform with no iAMT.

CL VREF

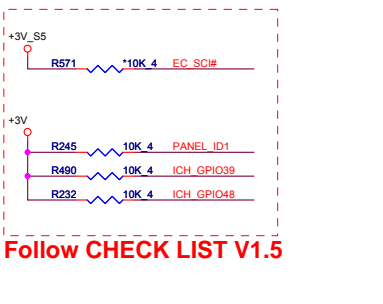


<Checklist ver0.8>
 The ICH9M Controller Link 1 VREF circuit is required only if Intel AMT is to be supported.

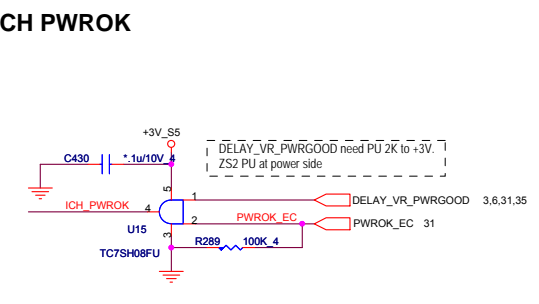
TPM Physical Presence for iTPM.

Stuff	HDMI SET
R583	HDMI
R315	No HDMI

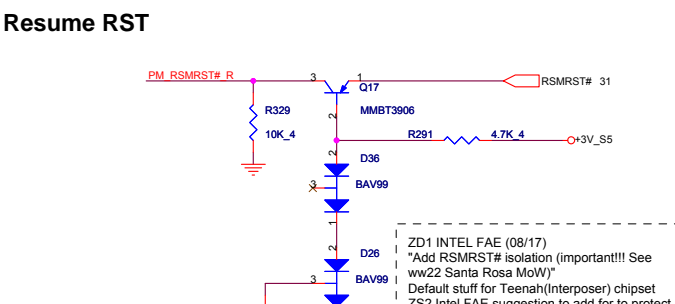
ICH PWROK



Follow CHECK LIST V1.5

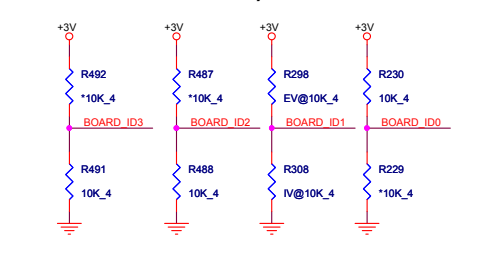


Resume RST



ZD1 INTEL FAE (08/17)
 "Add RSMRST# isolation (important!!! See ww22 Santa Rosa MoW)"
 Default stuff for Teناه(Interposer) chipset
 ZS2 Intel FAE suggestion to add for to protect RTC/CMOS data from corruption when system encounters an abnormal power down sequence

M/B ID ID0=0 -->ZK6, ID0=1 -->ZR6 ID1=0 -->UMA, ID1=1 -->Discrete

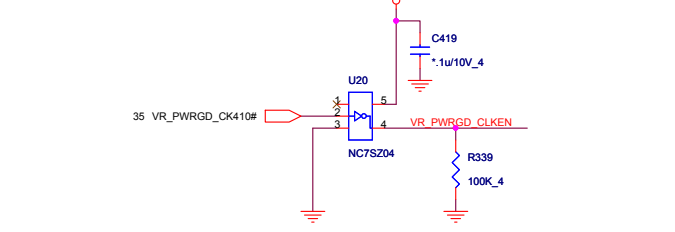


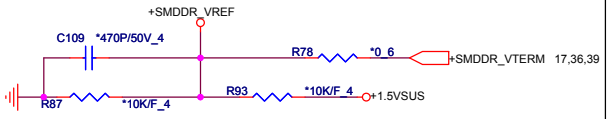
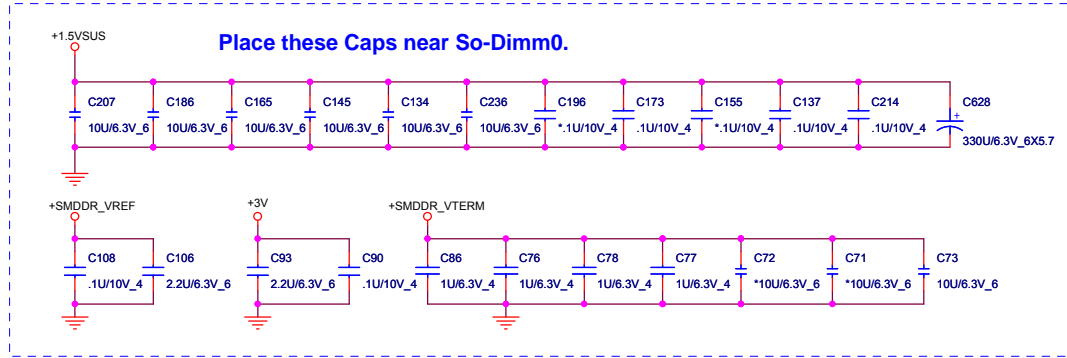
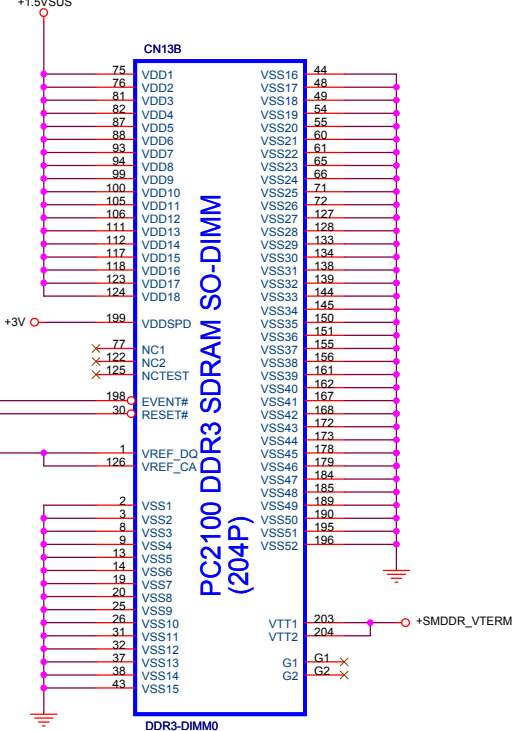
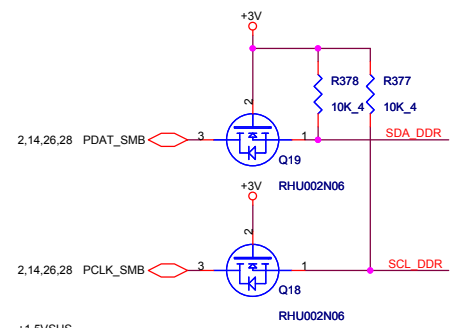
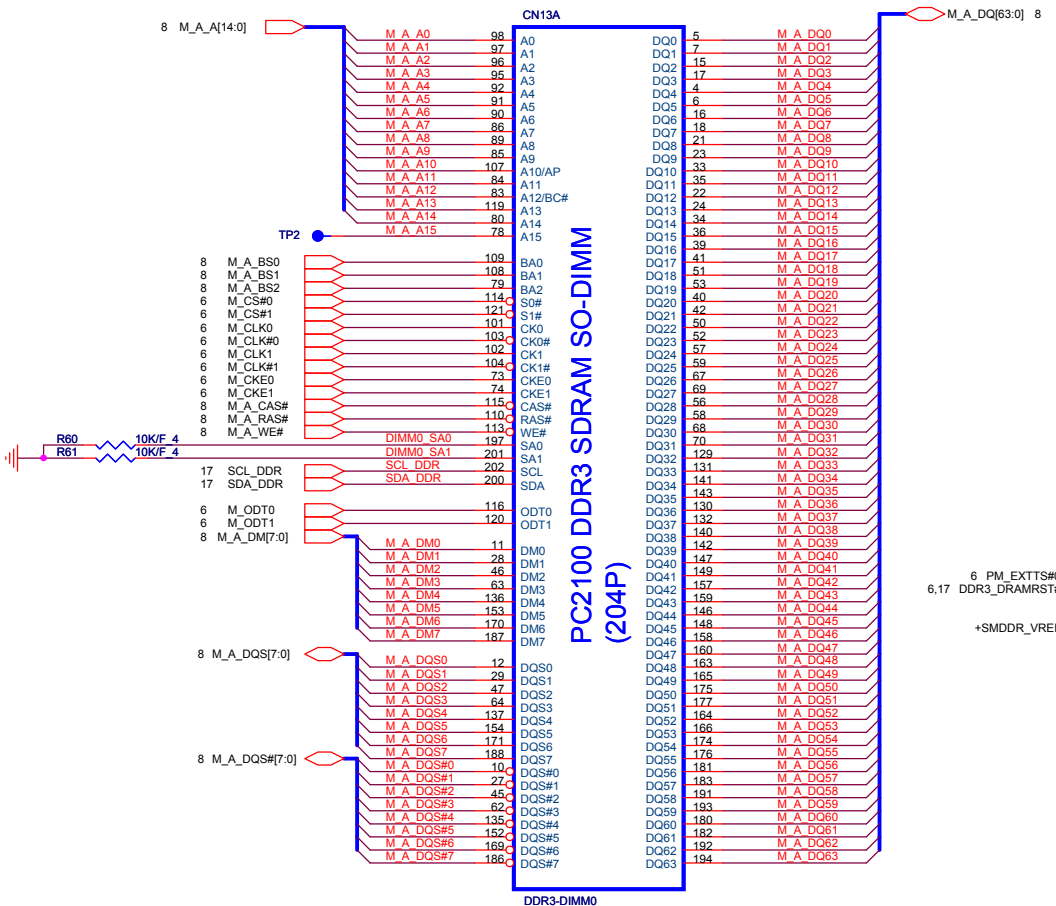
Board ID	ID3	ID2	ID1	ID0
A-SMT, ID1=0 -->UMA, ID1=1 -->Discrete	0	0	0/1	1
	0	0	0/1	1
	0	0	0/1	1
	0	0	0/1	1

South Bridge Strap Pin (3/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode	PCSPK R271 *1K 4 +3V
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL R485 *1K 4

CLK Enable



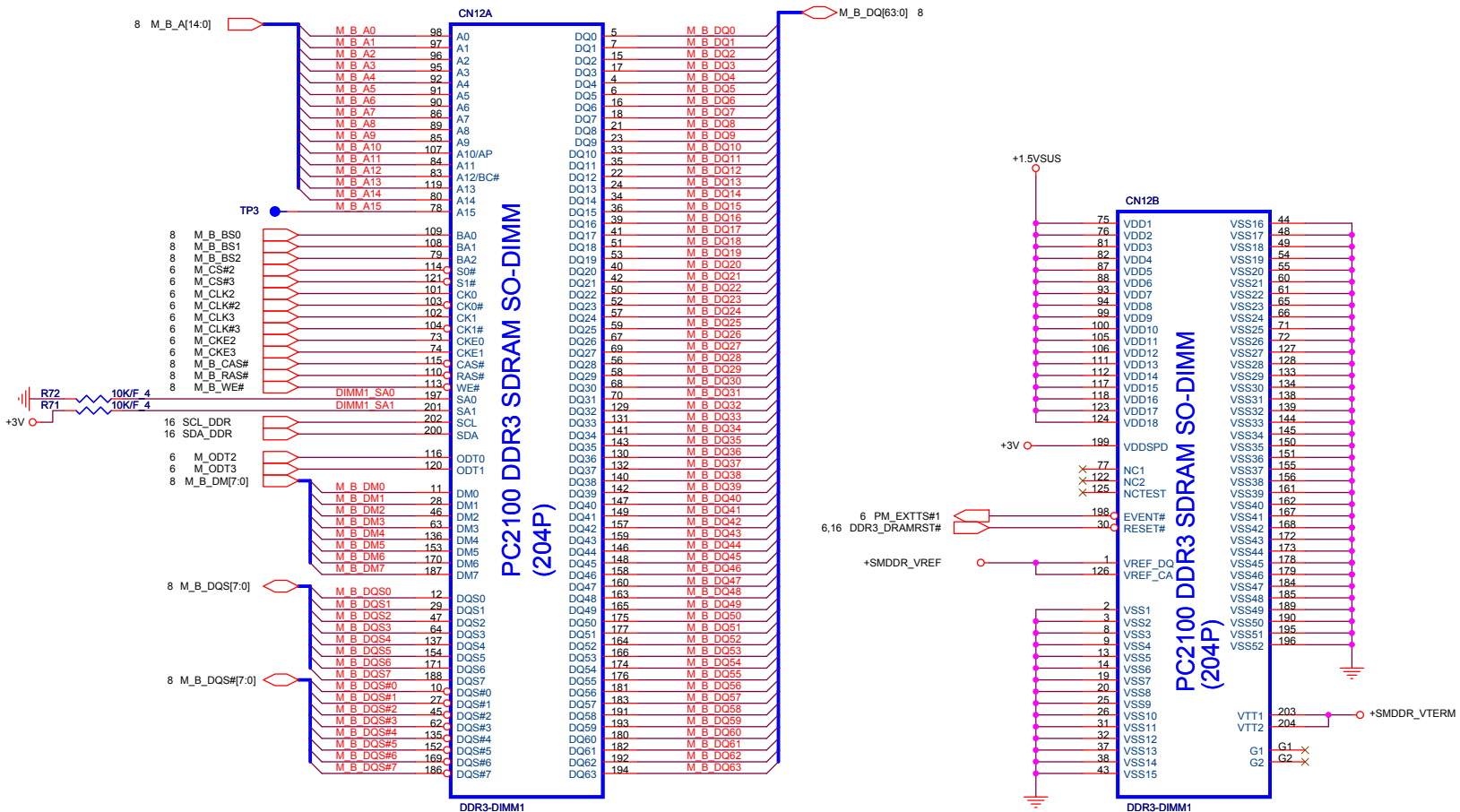


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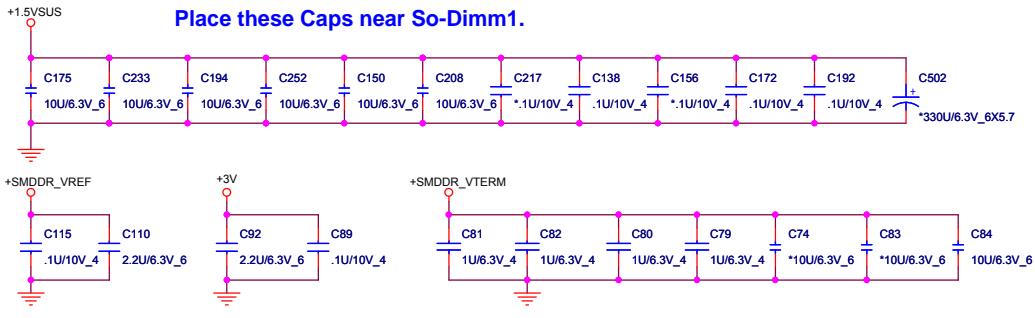
PROJECT : ZR6

Size Document Number **DDR3 DIMM-0(H=5.2)** Rev 1A

Date: Monday, April 13, 2009 Sheet 16 of 42



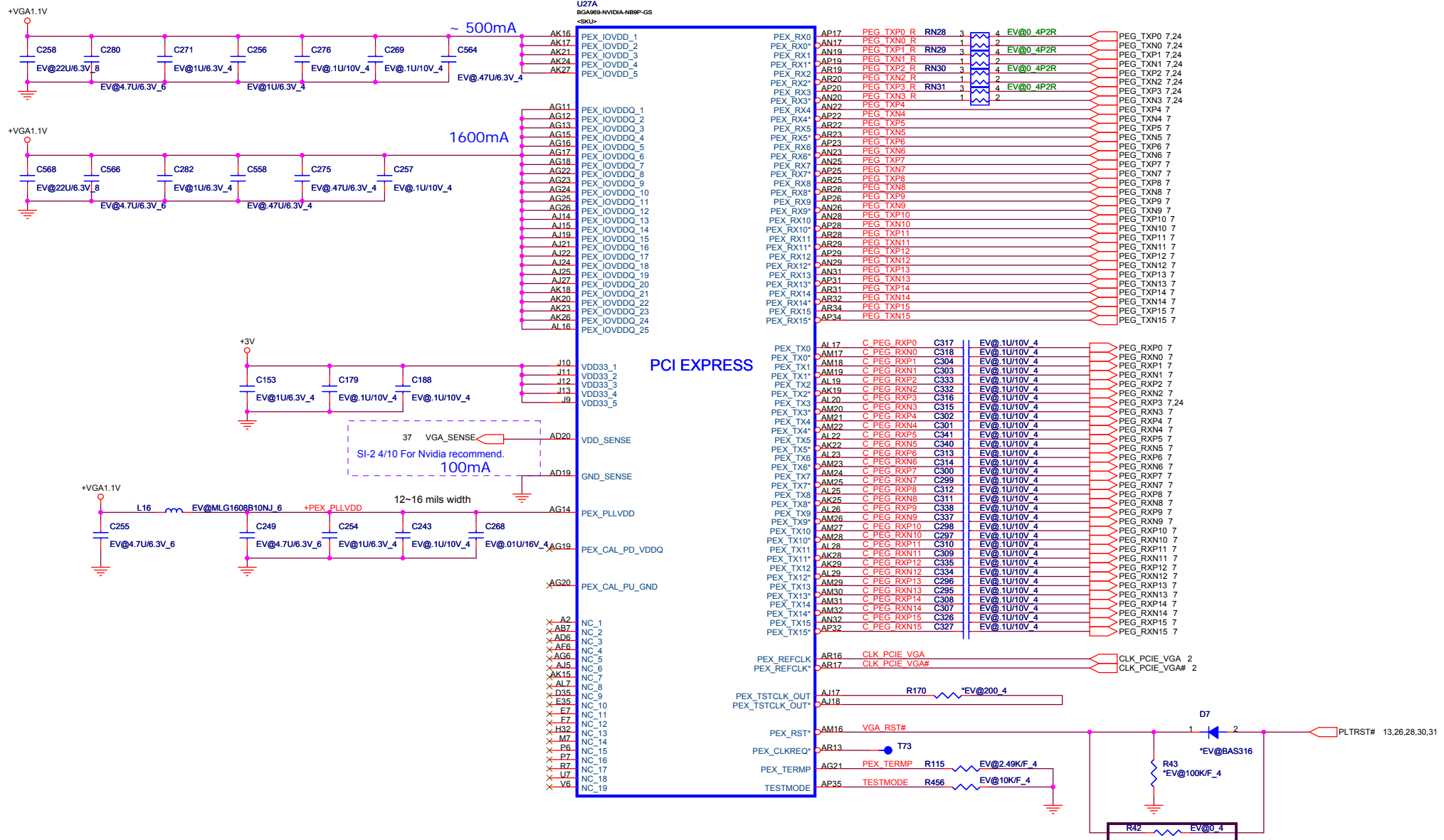
Place these Caps near So-Dimm1.



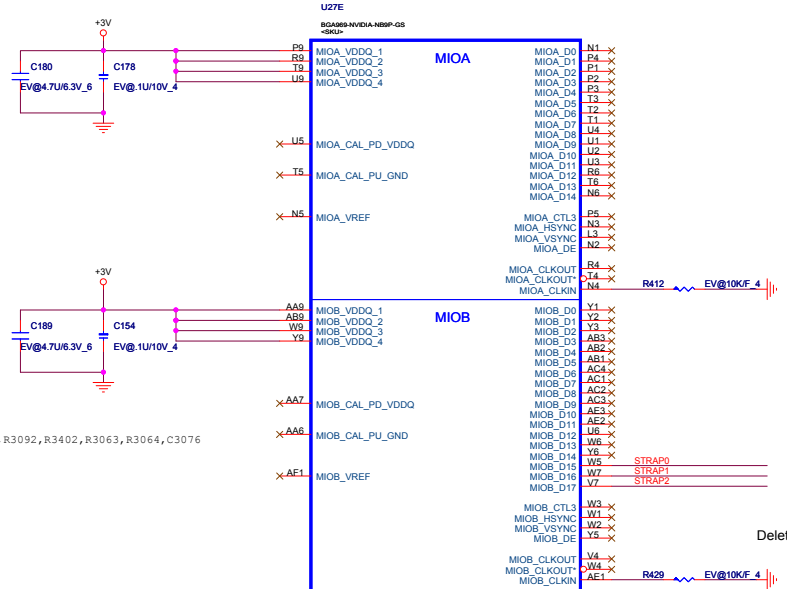
Quanta Computer Inc.
PROJECT : ZR6

Size	Document Number	Rev
	DDR3 DIMM-1(H=9.2)	1A

Date: Monday, April 13, 2009 Sheet 17 of 42

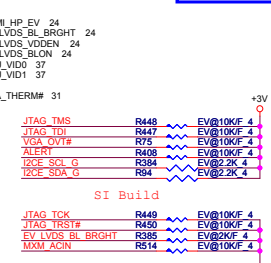
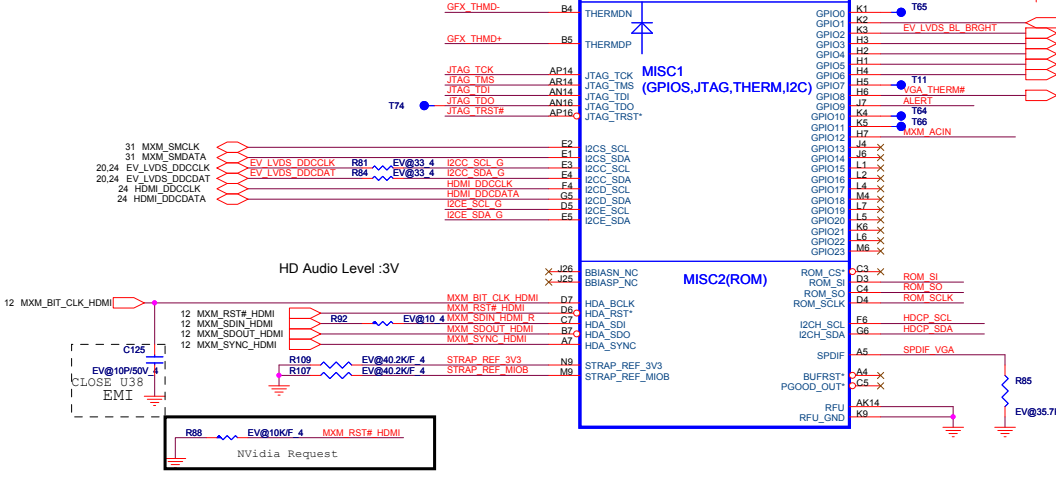


NV10M (VGA)



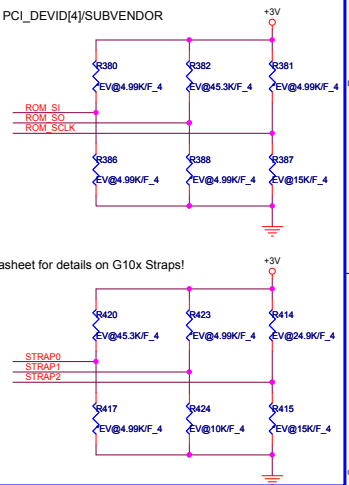
Nvidia Propose Remove C3134, C3681, R3092, R3402, R3063, R3064, C3076

Delete T31



N10P-GE1 (G96) Straps
N10M-GE1 (G98) Straps
GPIO ASSIGNMENTS

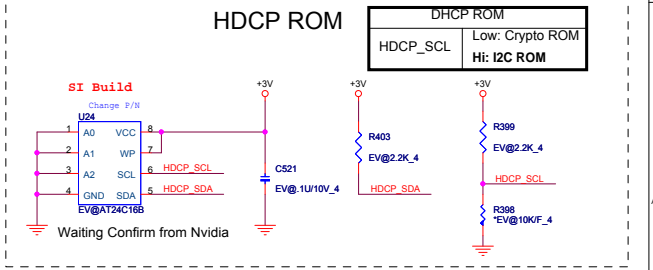
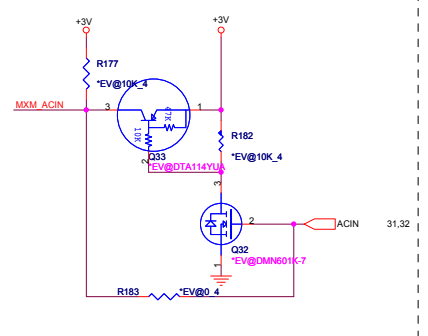
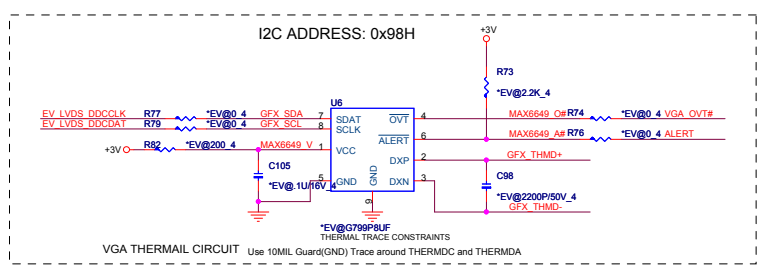
GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOTPLUG
1	IN	N/A	SECONDARY DVI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NV_VDD VID0
6	OUT	N/A	NV_VDD VID1
7	OUT	N/A	FB_VDD VID0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL OR HDMI_CEC
14	OUT	HIGH	PS CONTROL



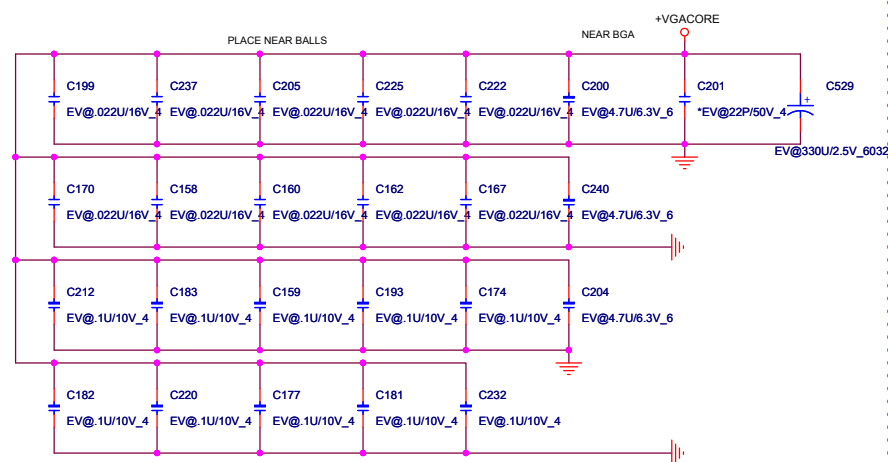
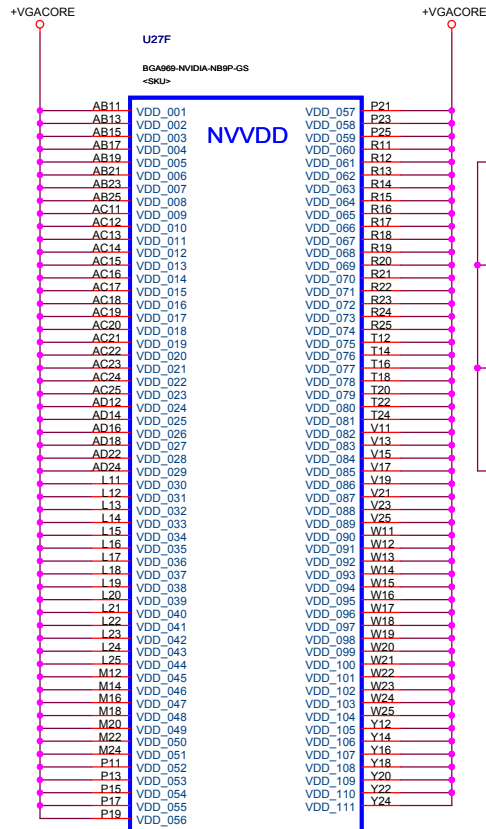
Logical Strap Bit Mapping

PCI_DEVID:	STRAP2	R414	PU-VDD	PD
NB9M-GE	0x06E 8	1000	5K	1000 0000
NB9M-GS	0x06E 9	1001	10K	1001 0001
NB9P-GE2	0x064 8	1000	15K	1010 0010
NB9P-GS	0x064 9	1001	20K	1011 0011
N10P-GE1	0x065 2	0010	25K	1100 0100
N10M-GE1	0x06E C	1100 default	30K	1101 0101
			35K	1110 0110
			45K	1111 0111

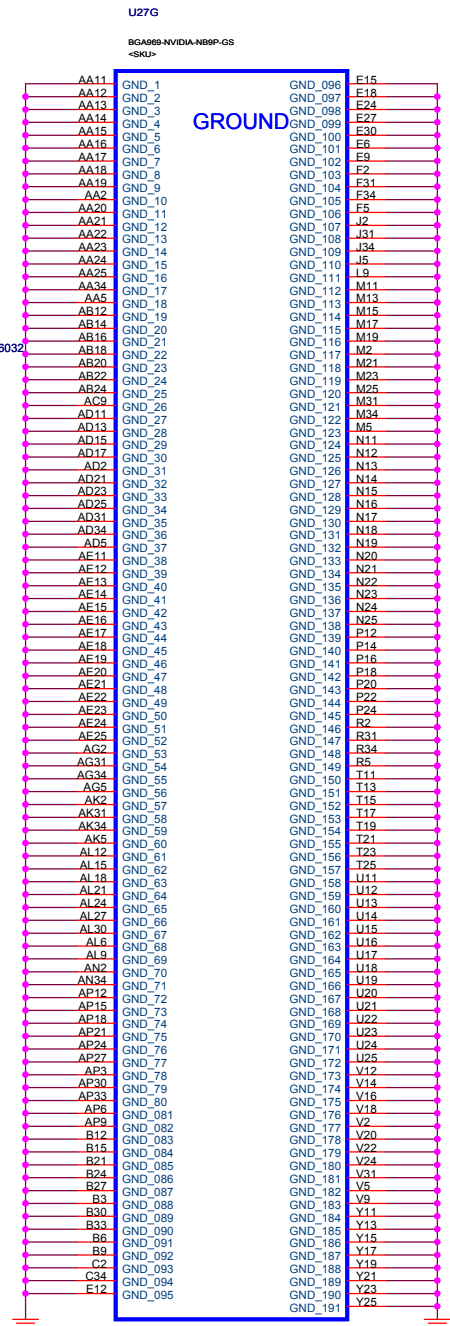
R386	Config	Definitions	Die
CS25102FB02 5K	64Mx16 DDR2	Hynix	E
CS31002FB26 10K	64Mx16 DDR2	Samsung	Q
CS32002FB29 20K	64Mx16 DDR2	Samsung	E

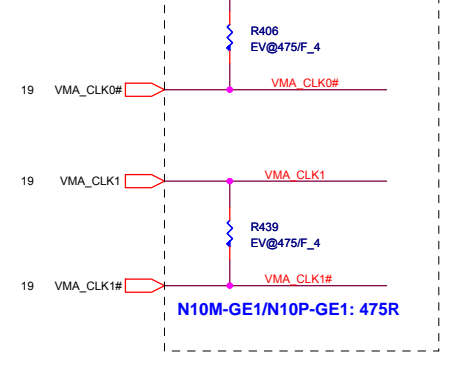
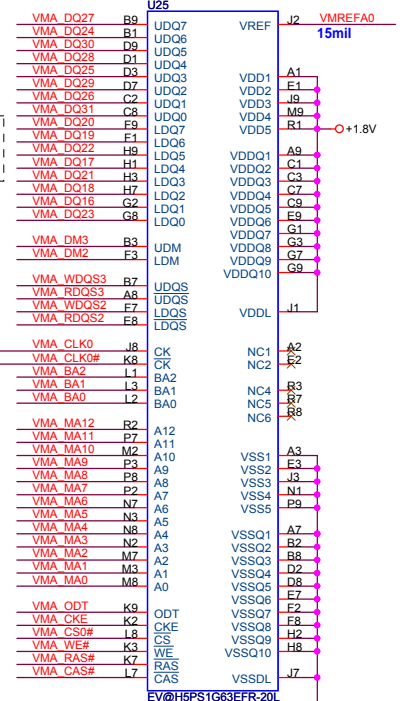
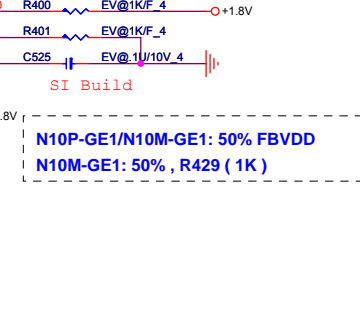
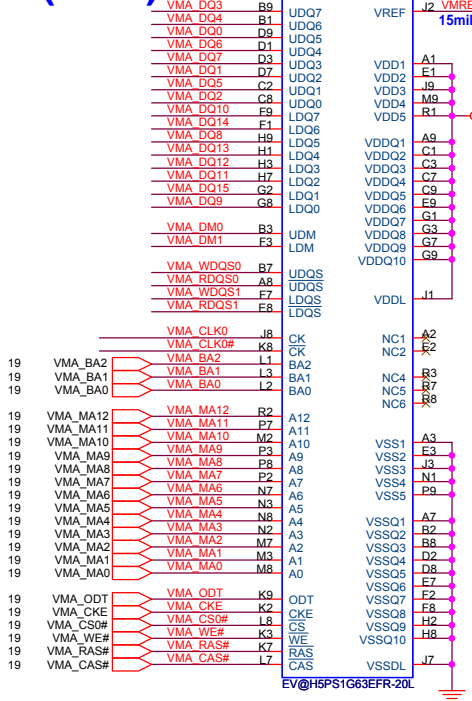


NVVDD Decoupling

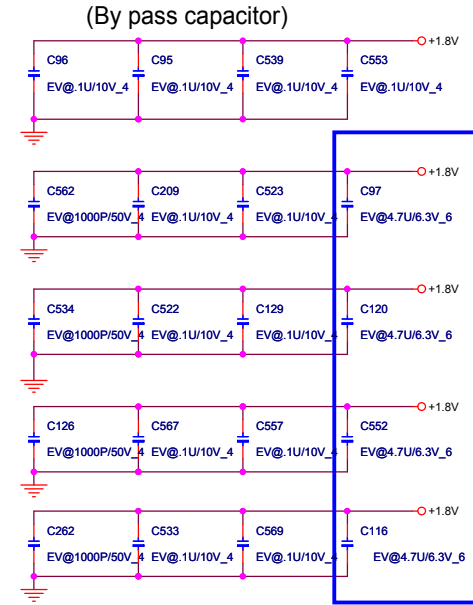
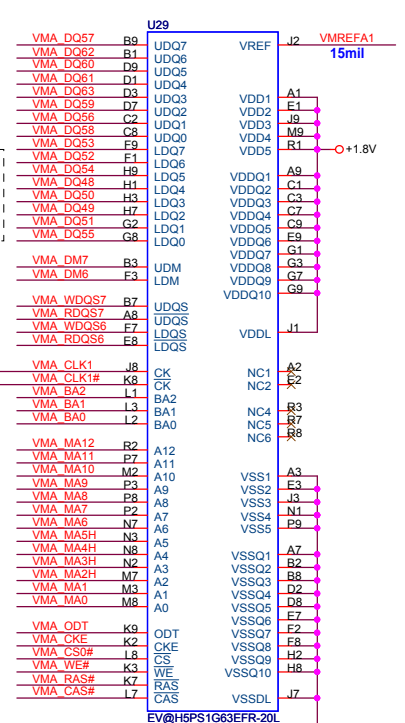
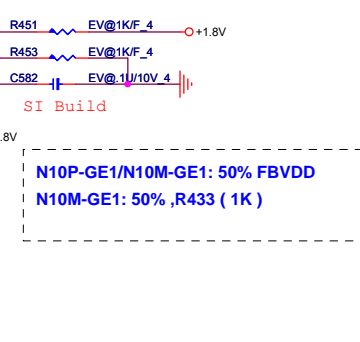
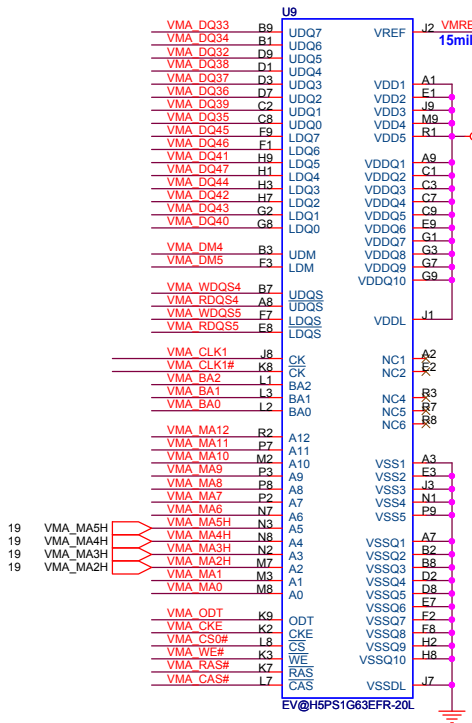


Follow Design Guide DG-03276-001 4.7uF x3 and 0.22x10 uF instead of 0.1uF x10





CS14752FB11 RES CHIP 475 1/16W +-1%(0402)



(By pass capacitor)

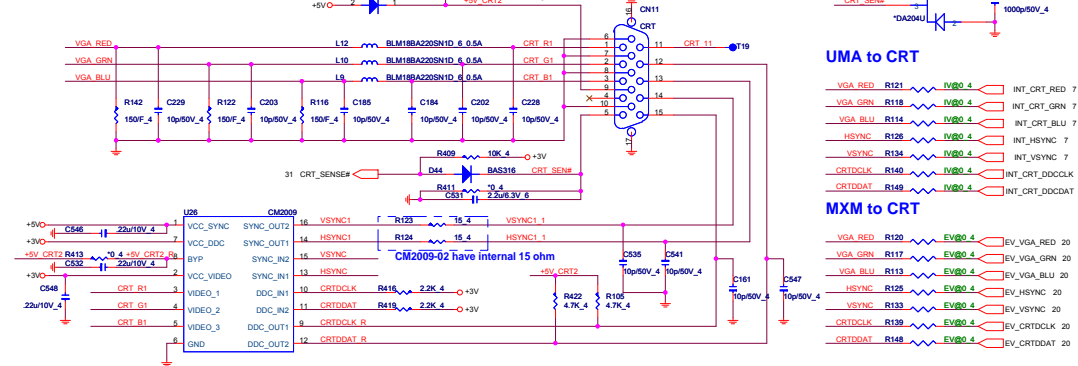
For DB: N10P/N10M : AKD5LG-T510(Samsung,64M*16) AKD5LG-TW02(Hynix,64M*16)

- 19 VMA_DQ[63..0]
- 19 VMA_DM[7..0]
- 19 VMA_WDQS[7..0]
- 19 VMA_RDQS[7..0]

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PROJECT : ZR6

Size: Document Number: **NV10X VRAM-1(GDDR2 BGA84)** Rev: 1A
 Date: Monday, April 13, 2009 Sheet: 23 of 42

CRT(CRT)



LVDS(LDS)

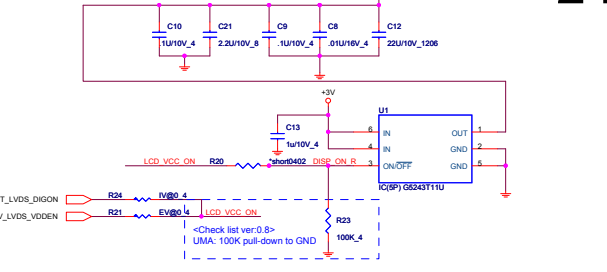


Lid Switch (HSR)

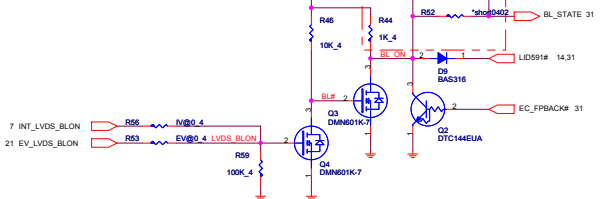


LCD_ON(LDS)

PANEL VCC CONTROL



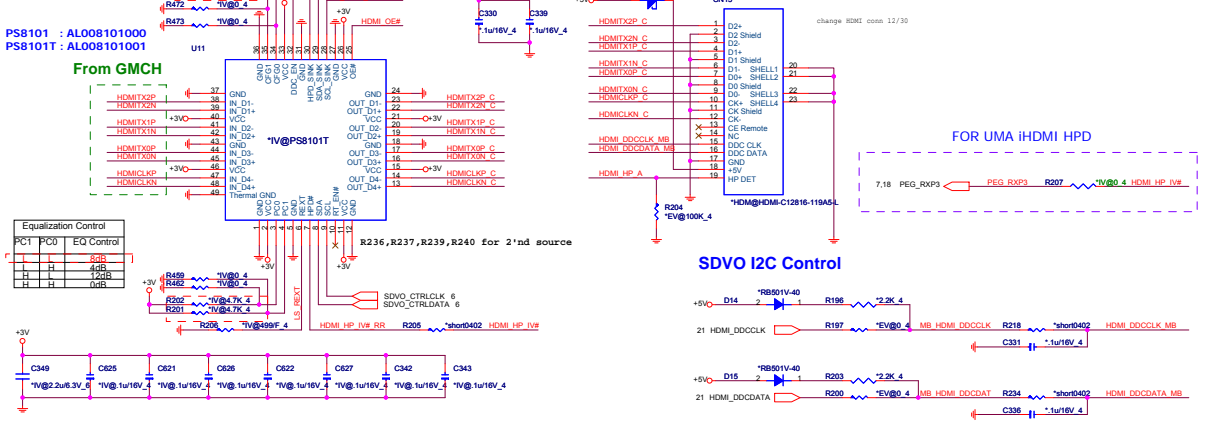
Backlight Control(LDS)



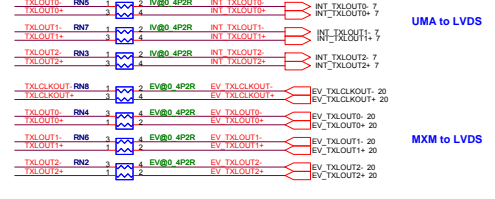
LCD EDID Smbus PU



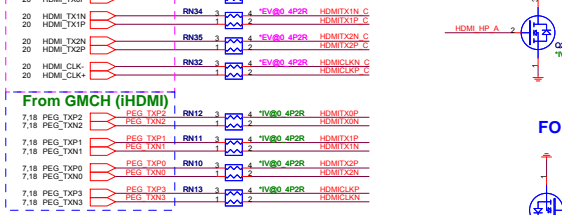
HDMI (HDM)



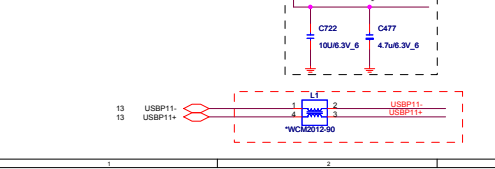
UMA to LVDS



From MXM



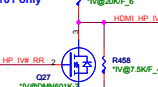
Camera(CCD) Modify



OE# control for power saving



HP-detect for PS8101 only



EV@Hot-plug



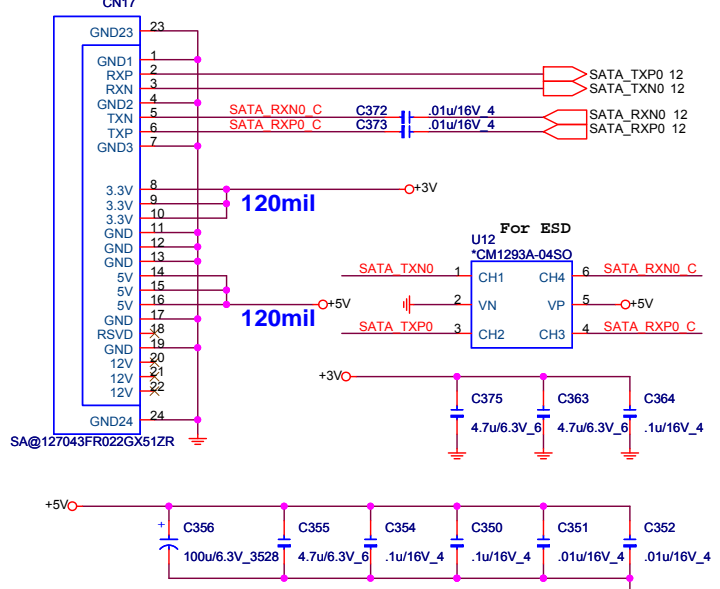
FOR NV HDMI



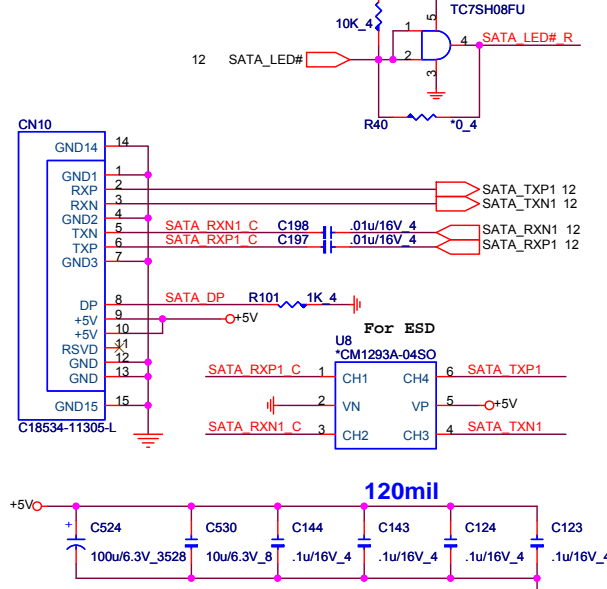
NV suggestion near HDMI connector



SATA HDD(HDD)

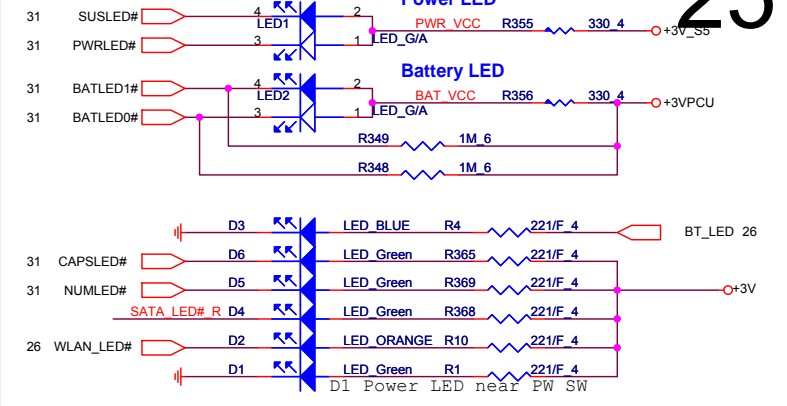


SATA ODD(ODD)

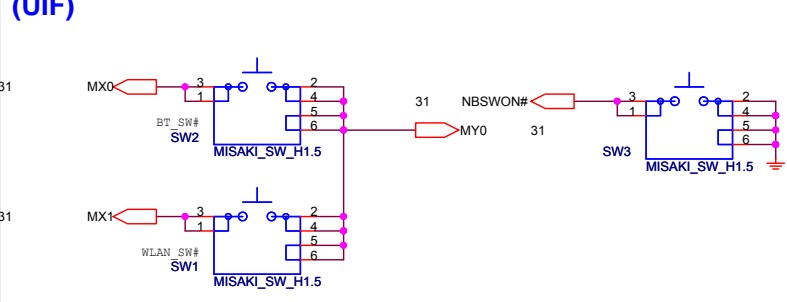


LED(UIF)

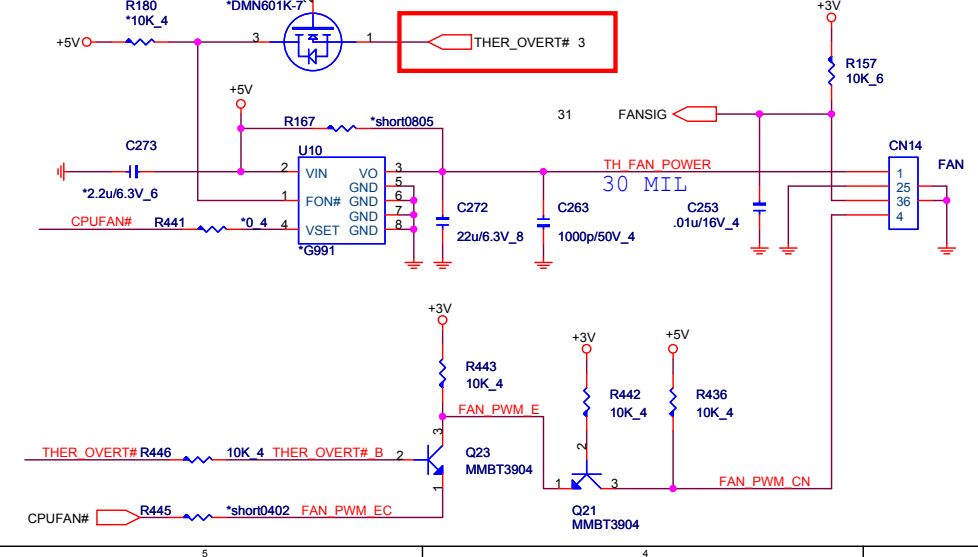
Power / Suspend : Green / Amber



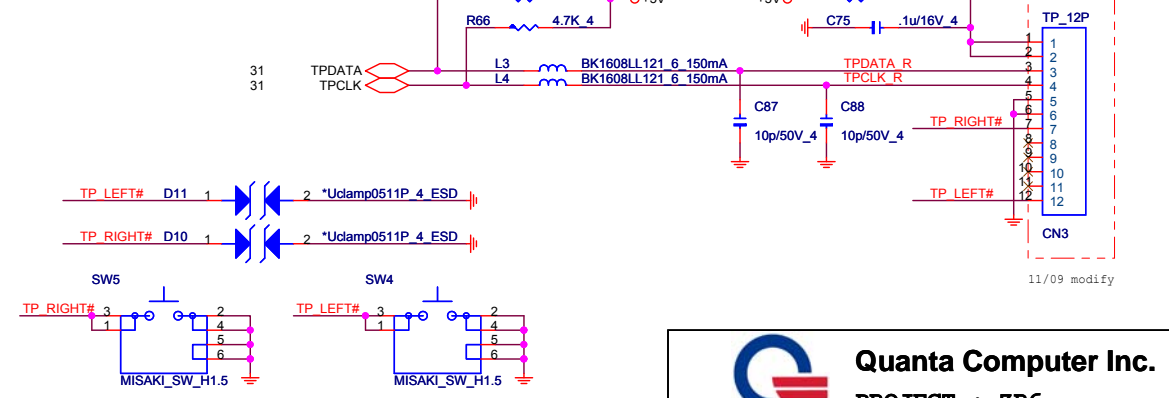
Power Button (UIF)



FAN(THM)



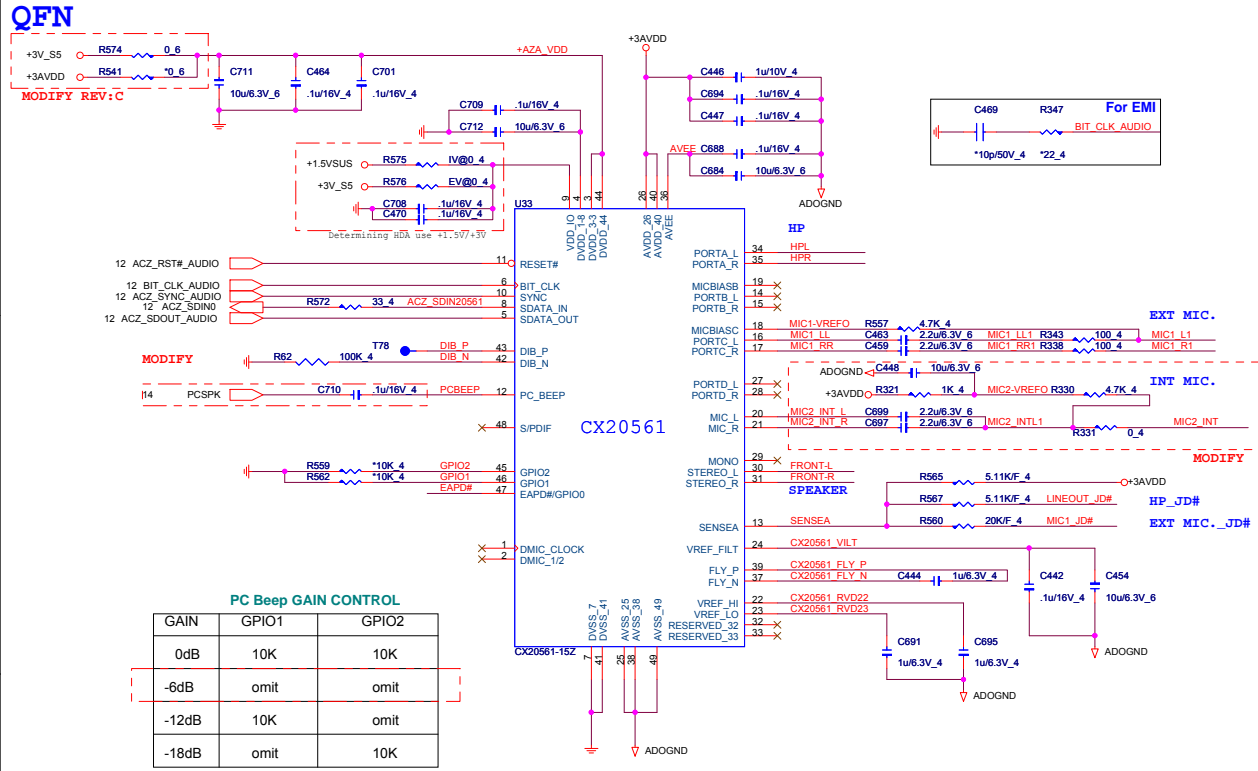
TP CONN



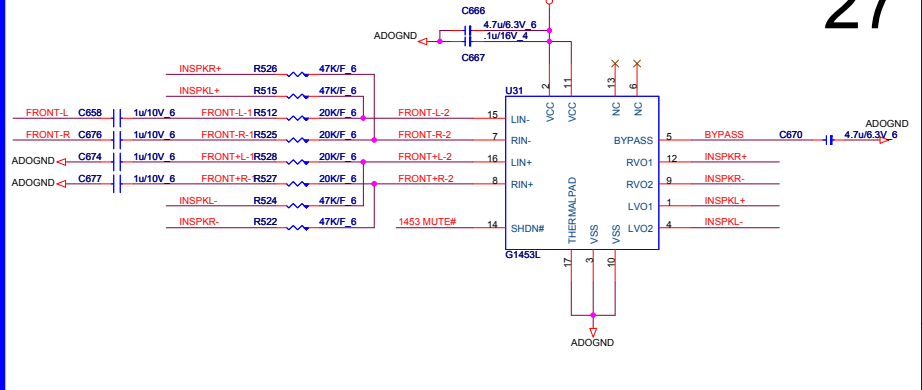
Quanta Computer Inc.
PROJECT : ZR6

Size	Document Number	Rev
	HDD/ODD/LED/SW/TP/FAN/MMB	1A
Date:	Monday, April 13, 2009	Sheet 25 of 42

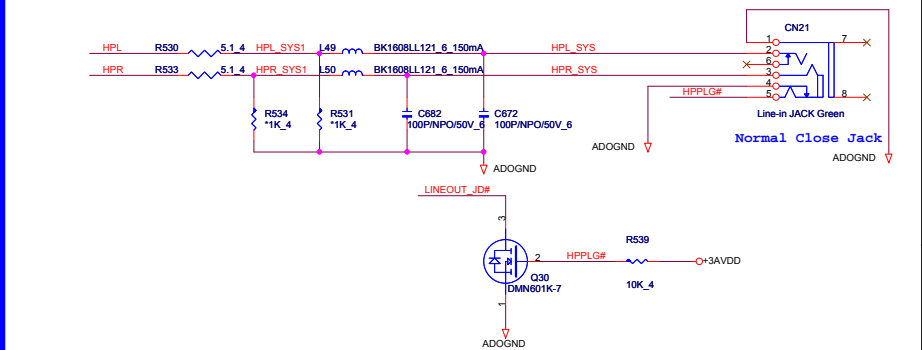
Codec CX20561-15Z (ADO)



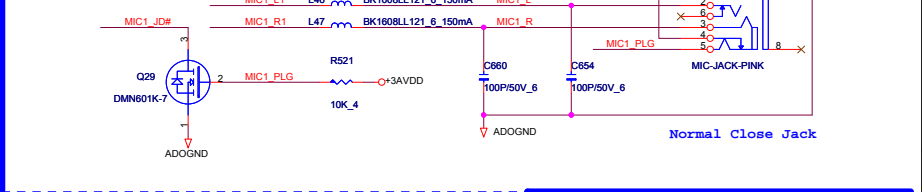
Speaker Amplifier(AMP)



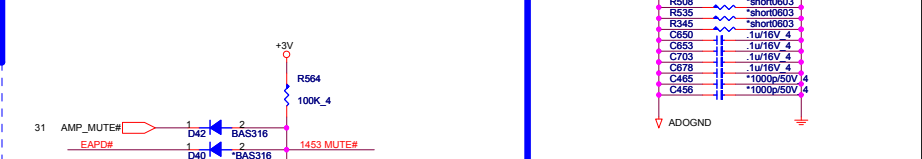
LINE OUT(AMP)



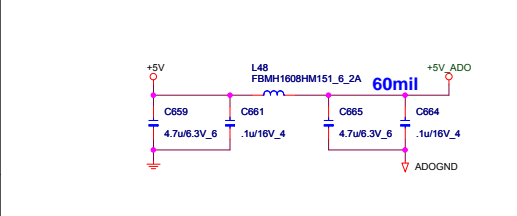
MIC(AMP)



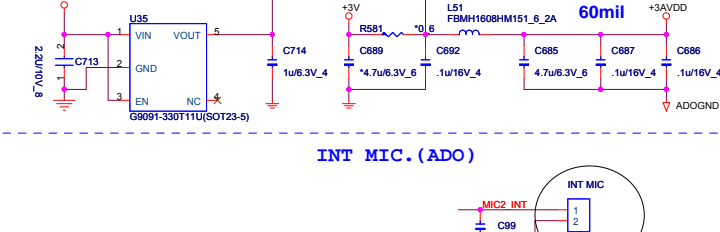
MUTE (AMP)



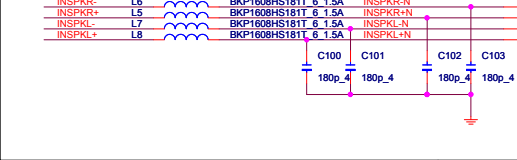
AMP Power(AMP)



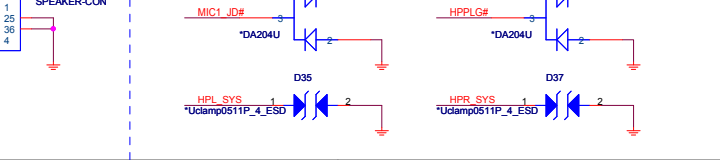
CODER Power(ADO)



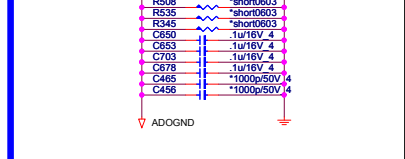
SPEAKER(AMP)



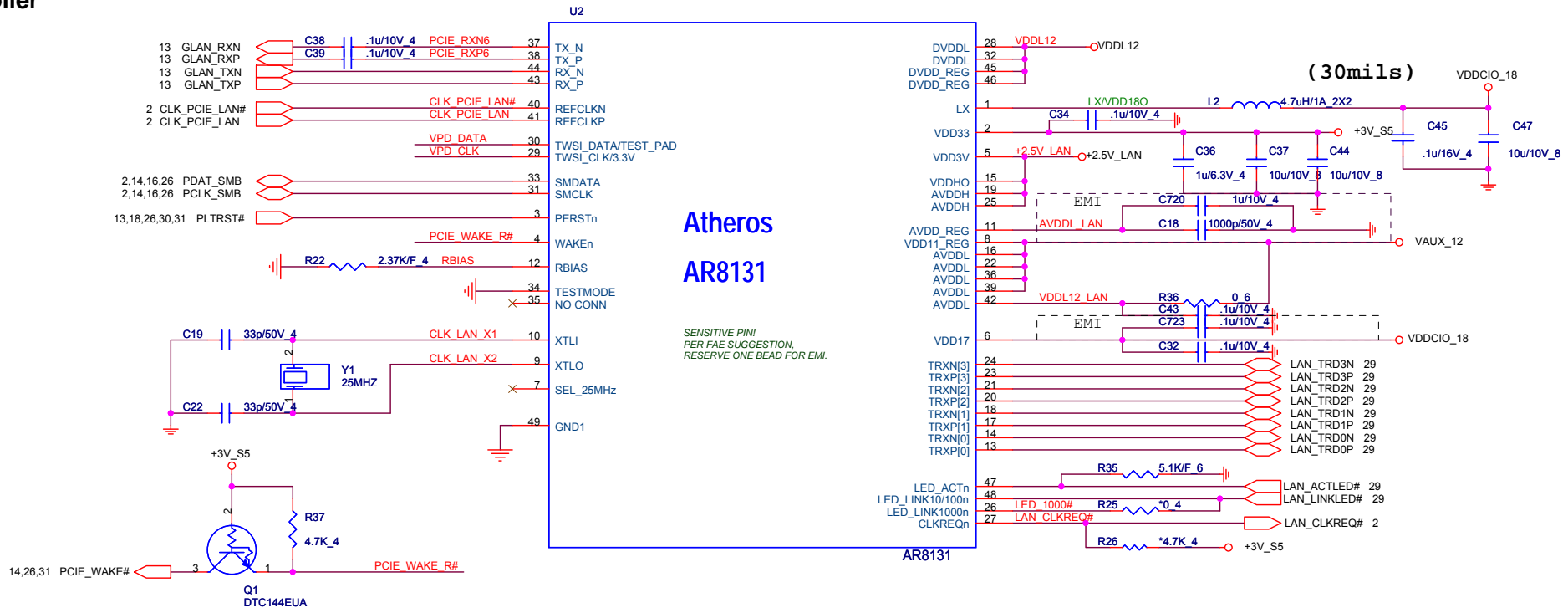
ESD(AMP)



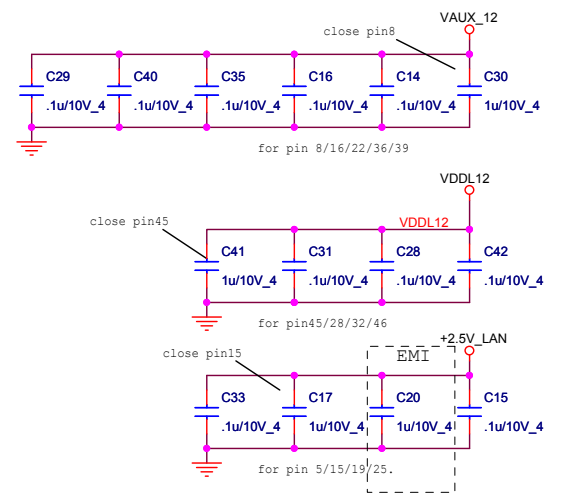
(ADO)



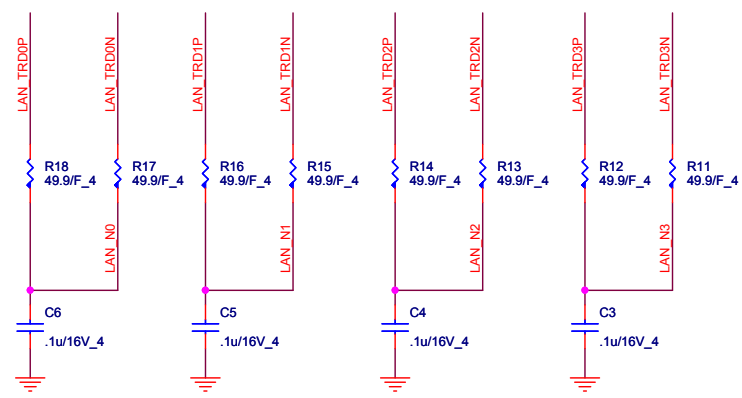
LAN Controller



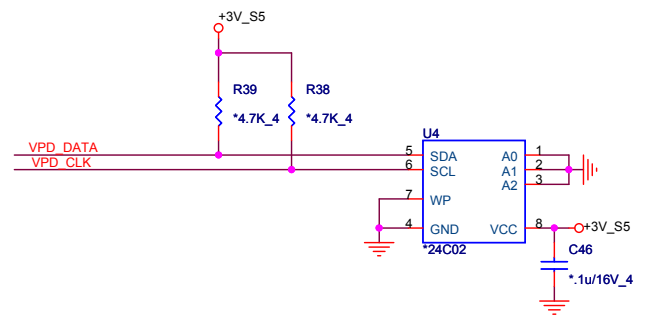
Decoupling CAP



PLACE NEAR IC SIDE



EEPROM

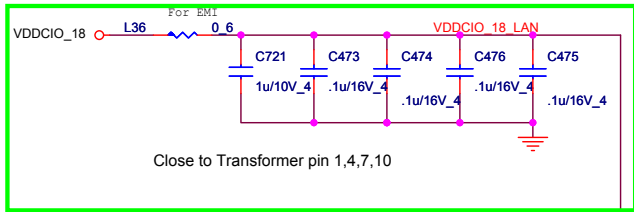


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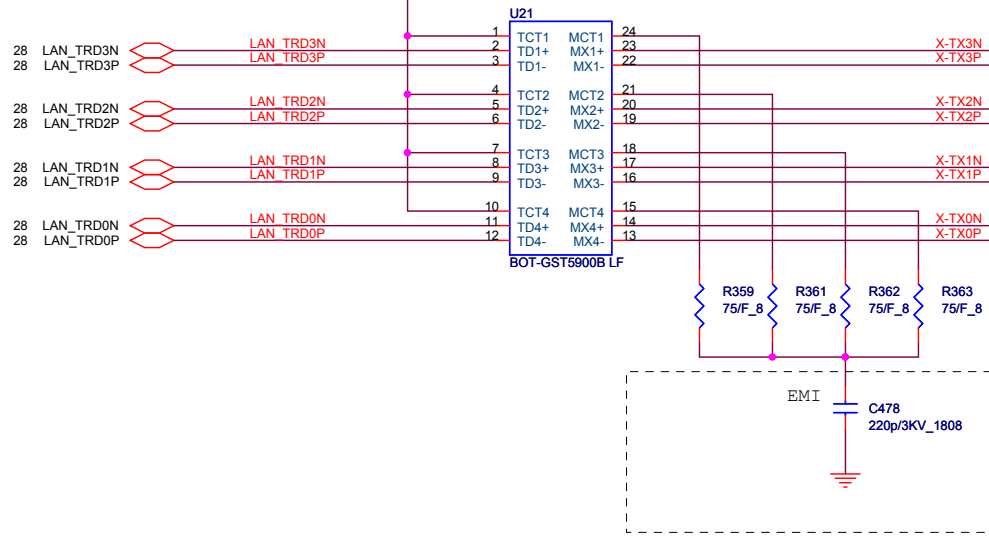
PROJECT : ZR6

Size	Document Number	Rev
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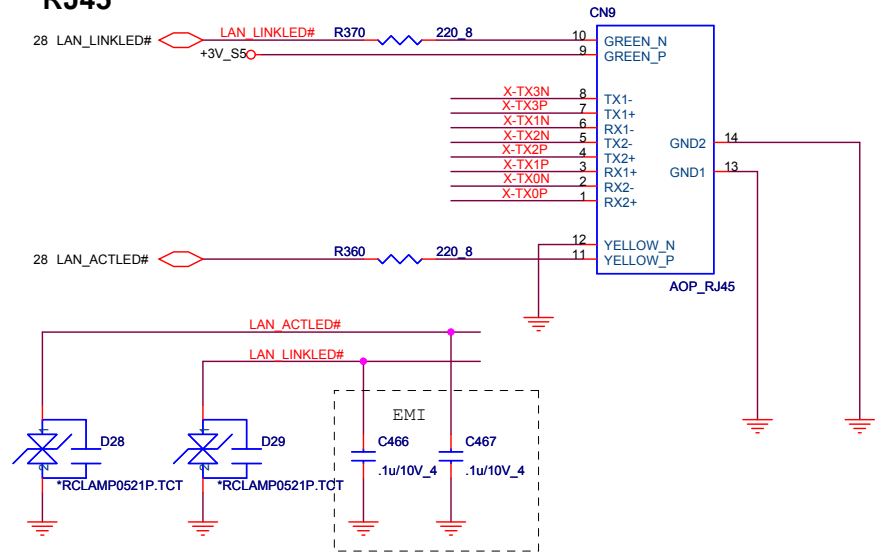
Date: Monday, April 13, 2009 Sheet 28 of 42




TRANSFORMER



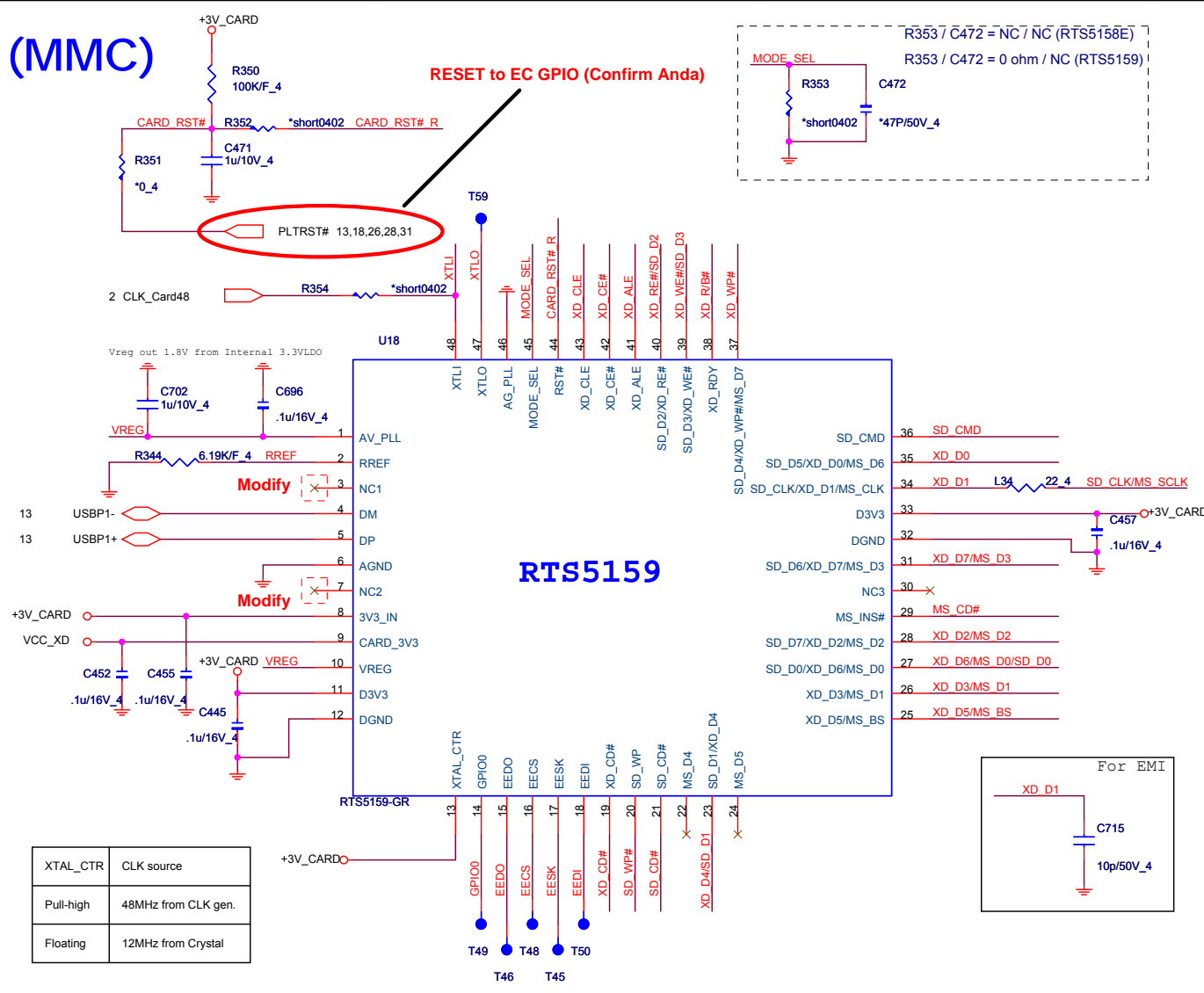
RJ45




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PROJECT : ZR6

Size	Document Number	Rev
	LAN Transformer and RJ45/BT	1A
Date:	Monday, April 13, 2009	Sheet 29 of 42

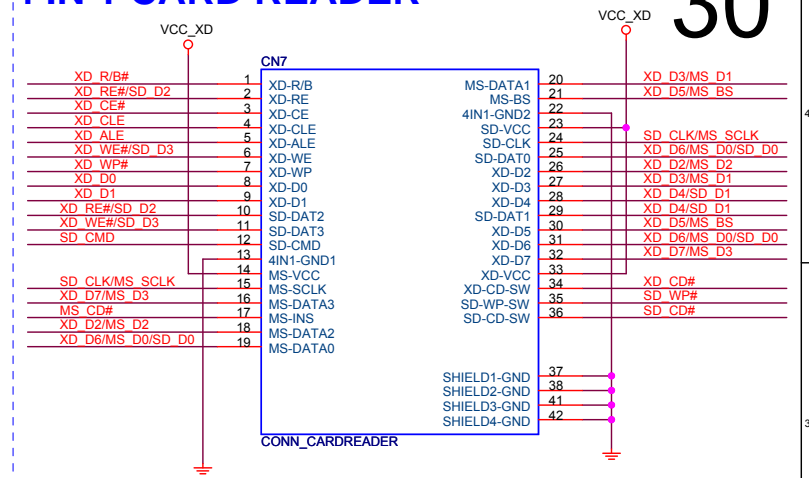
(MMC)



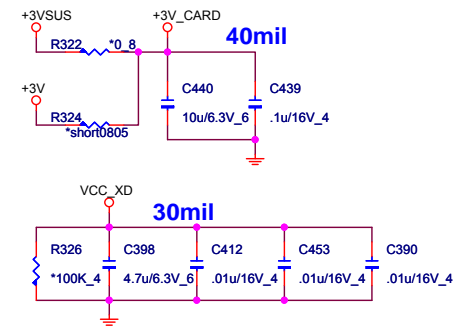
XTAL_CTR	CLK source
Pull-high	48MHz from CLK gen.
Floating	12MHz from Crystal

4 IN 1 CARD READER

30



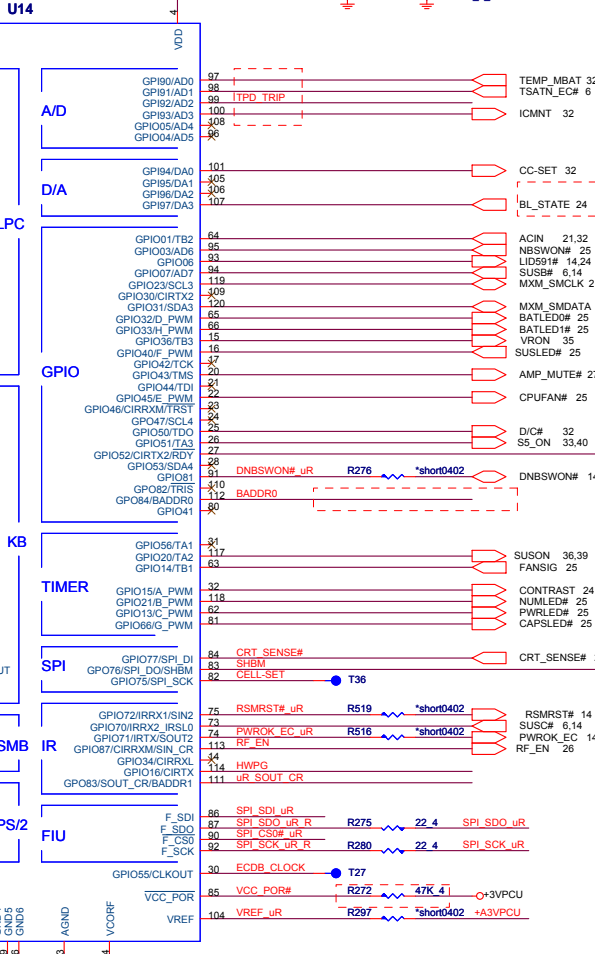
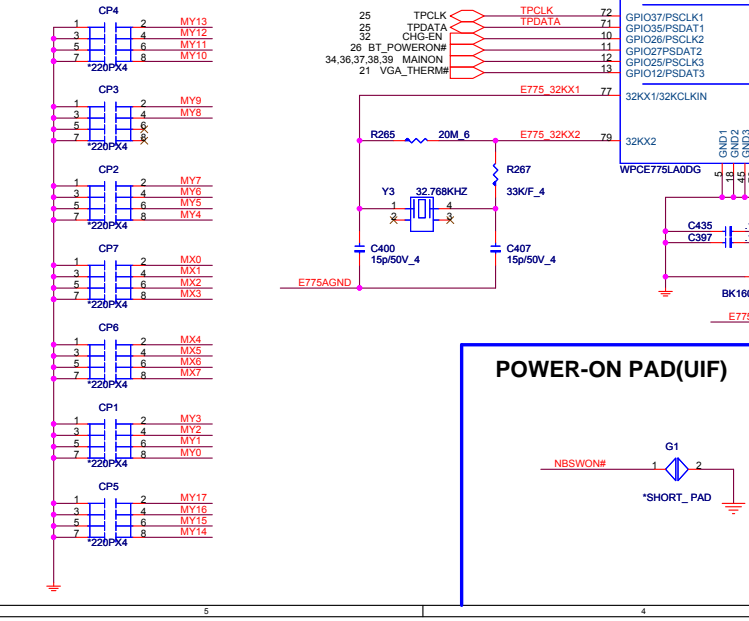
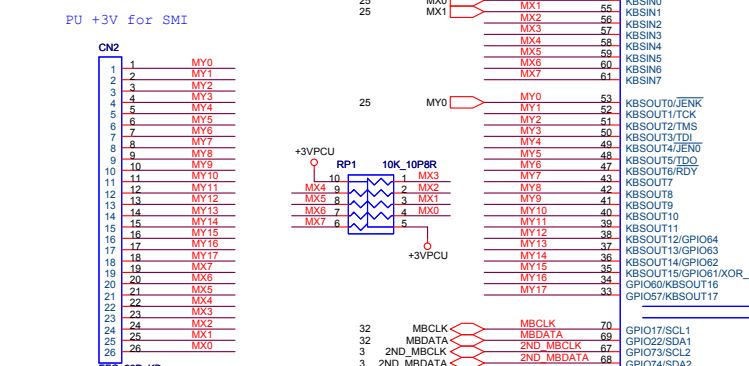
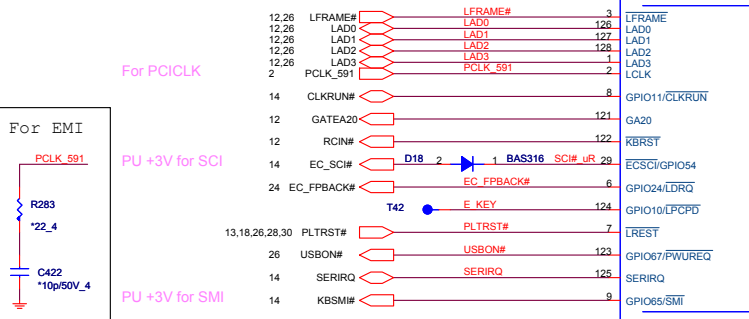
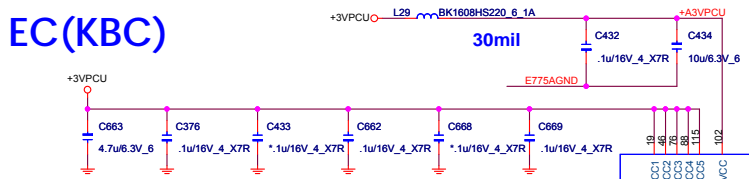
CARDREADER POWER



Quanta Computer Inc.

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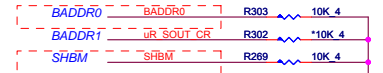
Size	Document Number	Rev
	CARD READER RTS5159	1A
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I/O ADDRESS SETTING

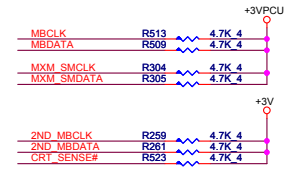
I/O Address	
BADDR1-0	Index Data
0 0	XOR TREE TEST MODE
0 1	CORE DEFINED
1 0	2Eh 2Fh
1 1	164Eh 164Fh

SHBM=0: Enable shared memory with host BIOS

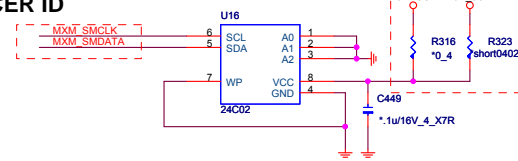


1/13 Confirm by vendor mail :
Disabled ('1') if using FW device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

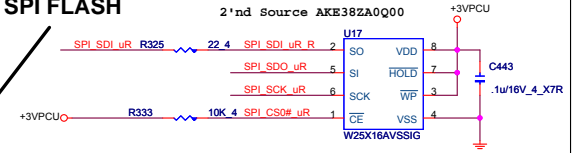
SM BUS PU



ACER ID

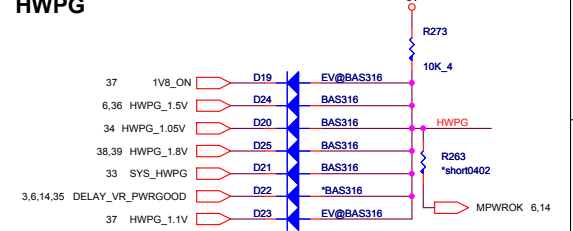


SPI FLASH



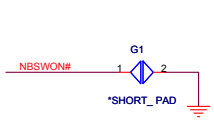
1/13 Confirm by vendor mail :
If the Southbridge enables "Long Wait Abort" by default, the flash device should be 50MHz (or faster)

HWPG

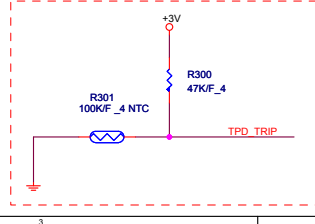


1'st AKE38ZP0N01 : Winbond W25X16AVSSIG
2'nd AKE37FP0Z13 : MXIC MX25L1605AM2C-15G
3'rd AKE38ZA0Q00 : EON EN25F16-100HIP
4'rd AKE38ZN0800 : AMIC A25L016

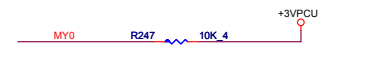
POWER-PAD(UIF)

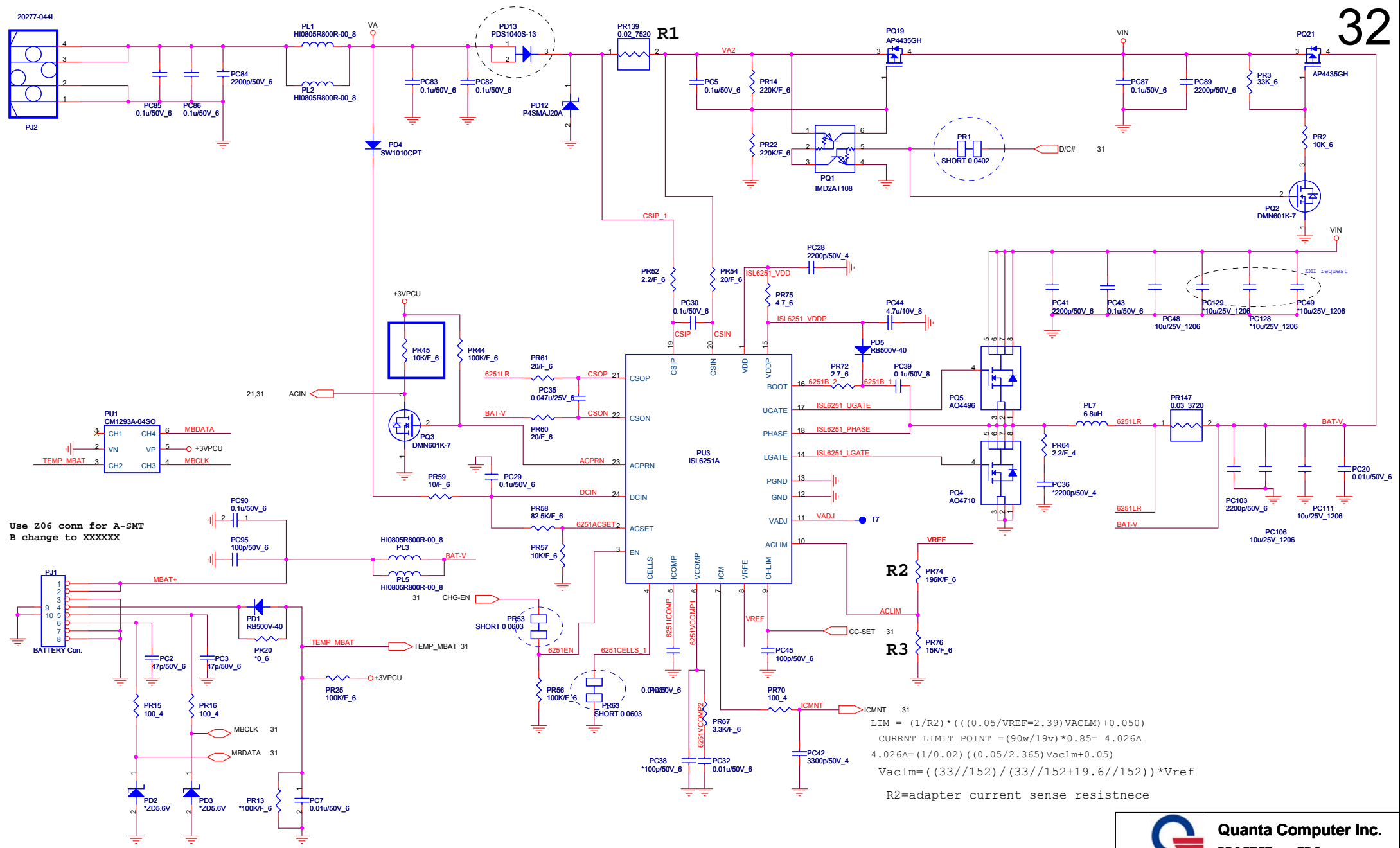


Thermal Sensor(THM)



INTERNAL KEYBOARD STRIP SET





Use Z06 conn for A-SMT
B change to XXXXXX

CELL-SET = Hi ----> Cells = VDD ---->4S
CELL-SET = Low ----> Cells = GND ---->3S

$$LIM = (1/R2) * (((0.05/VREF=2.39) VACLm) + 0.050)$$

$$CURRNT LIMIT POINT = (90w/19v) * 0.85 = 4.026A$$

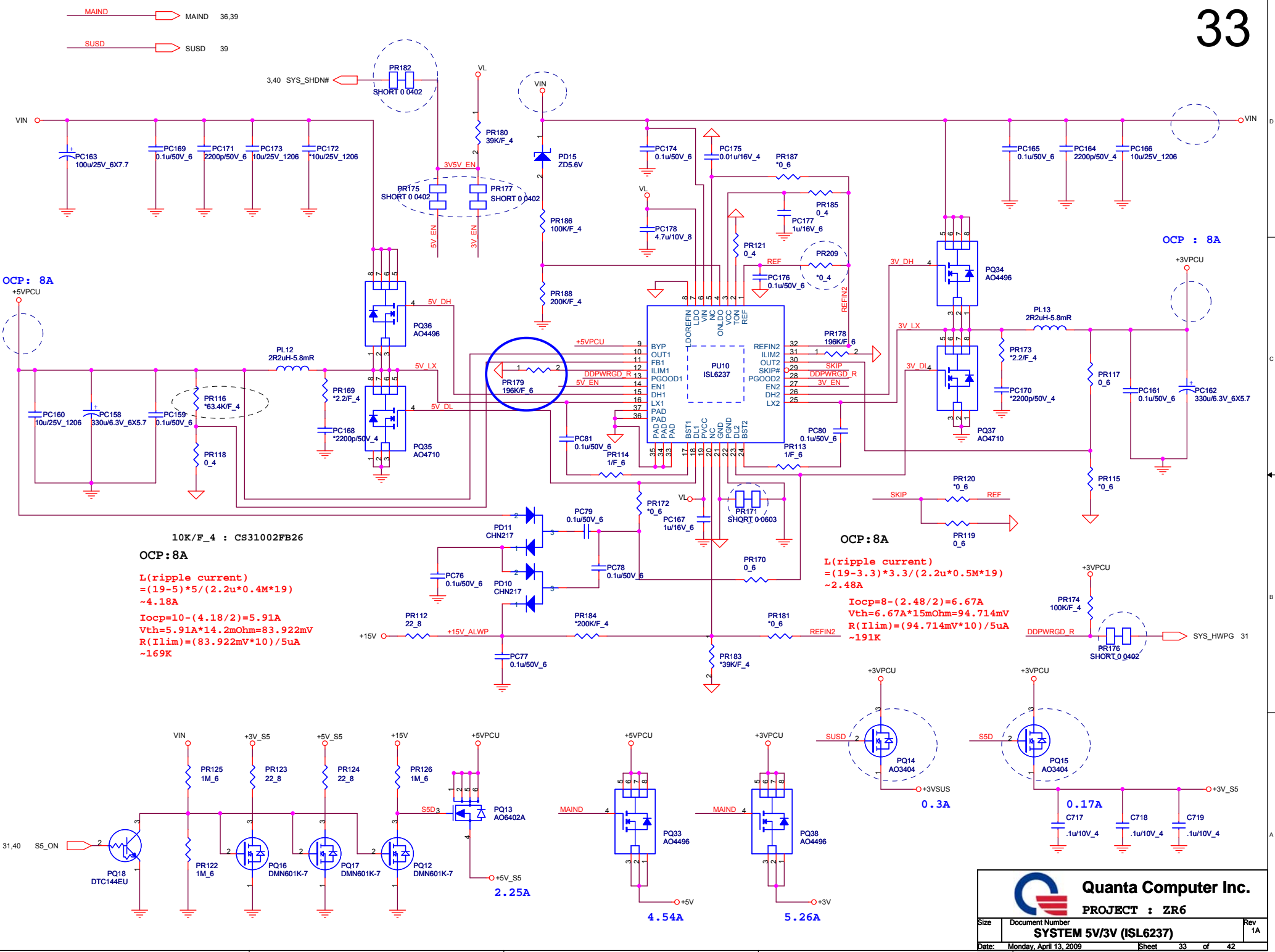
$$4.026A = (1/0.02) * (((0.05/2.365) VACLm) + 0.05)$$

$$VACLm = (((33//152) / ((33//152) + 19.6//152)) * Vref)$$

$$R2 = \text{adapter current sense resistnece}$$

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Size	Document Number	Rev
	Charger (ISL6251A)	1A
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OCP : 8A

OCP : 8A

10K/F_4 : CS31002FB26

OCP : 8A

L(ripple current)
 =(19-5)*5/(2.2u*0.4M*19)
 ~4.18A
 Iocp=10-(4.18/2)=5.91A
 Vth=5.91A*14.2mOhm=83.922mV
 R(Ilim)=(83.922mV*10)/5uA
 ~169K

OCP : 8A

L(ripple current)
 =(19-3.3)*3.3/(2.2u*0.5M*19)
 ~2.48A

Iocp=8-(2.48/2)=6.67A
 Vth=6.67A*15mOhm=94.714mV
 R(Ilim)=(94.714mV*10)/5uA
 ~191K

2.25A

4.54A

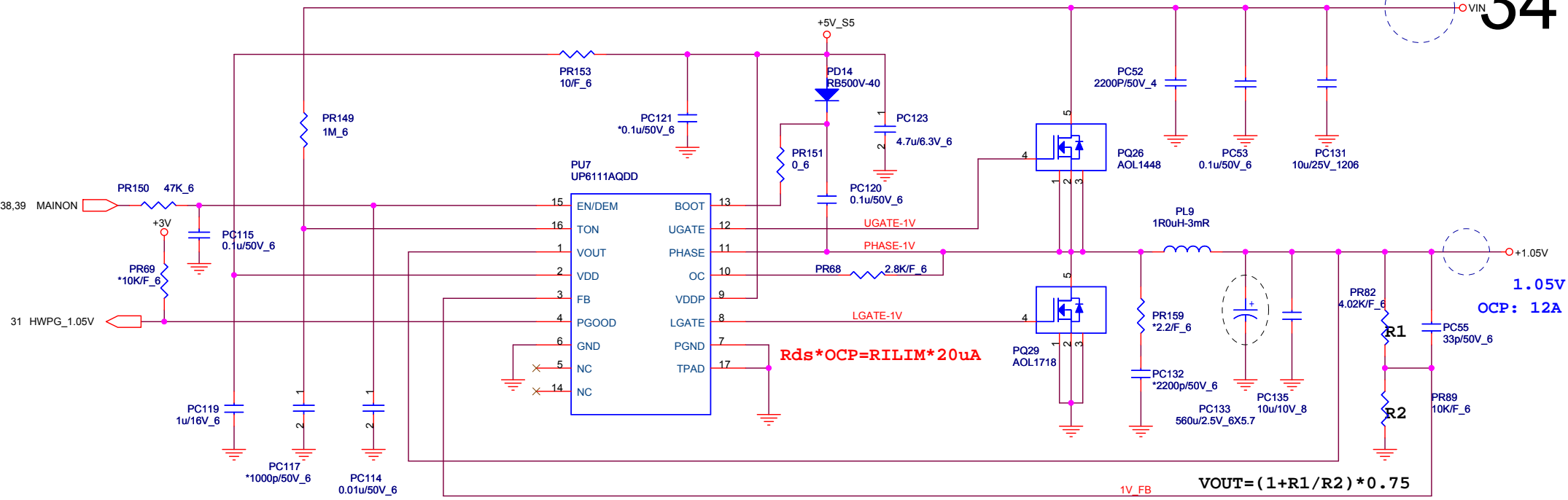
5.26A

0.3A

0.17A

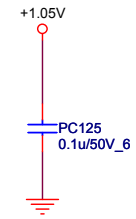
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Date:	Monday, April 13, 2009	Sheet 33 of 42
SYSTEM 5V/3V (ISL6237)		1A



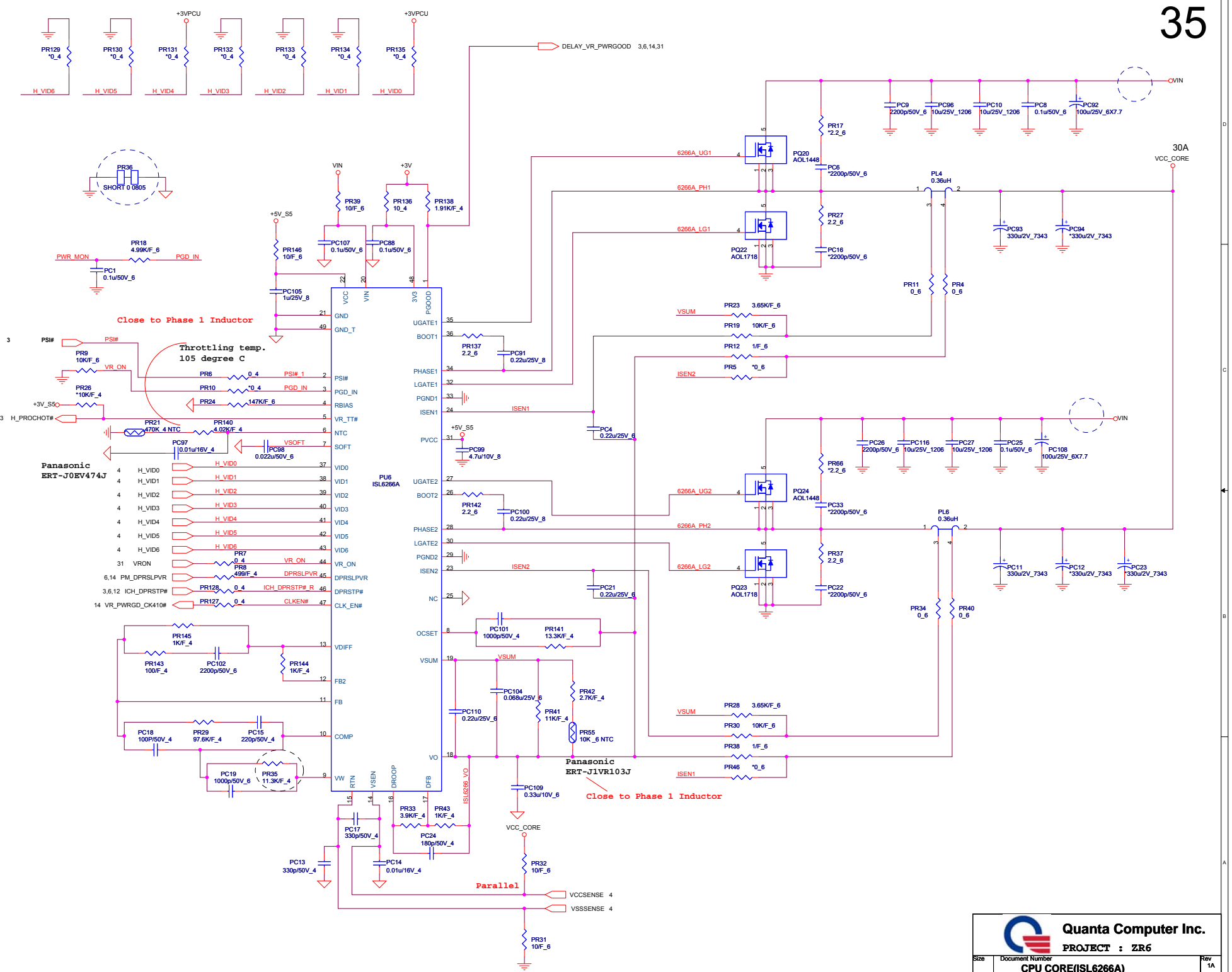
$TON = 3.85p * RTON * Vout / (Vin - 0.5)$
 $Frequency = Vout / (Vin * TON)$
 $TON = 3.85p * 1M * 1 / (Vin - 0.5)$
 $Frequency = 1 / (0.0036767) = 272K$

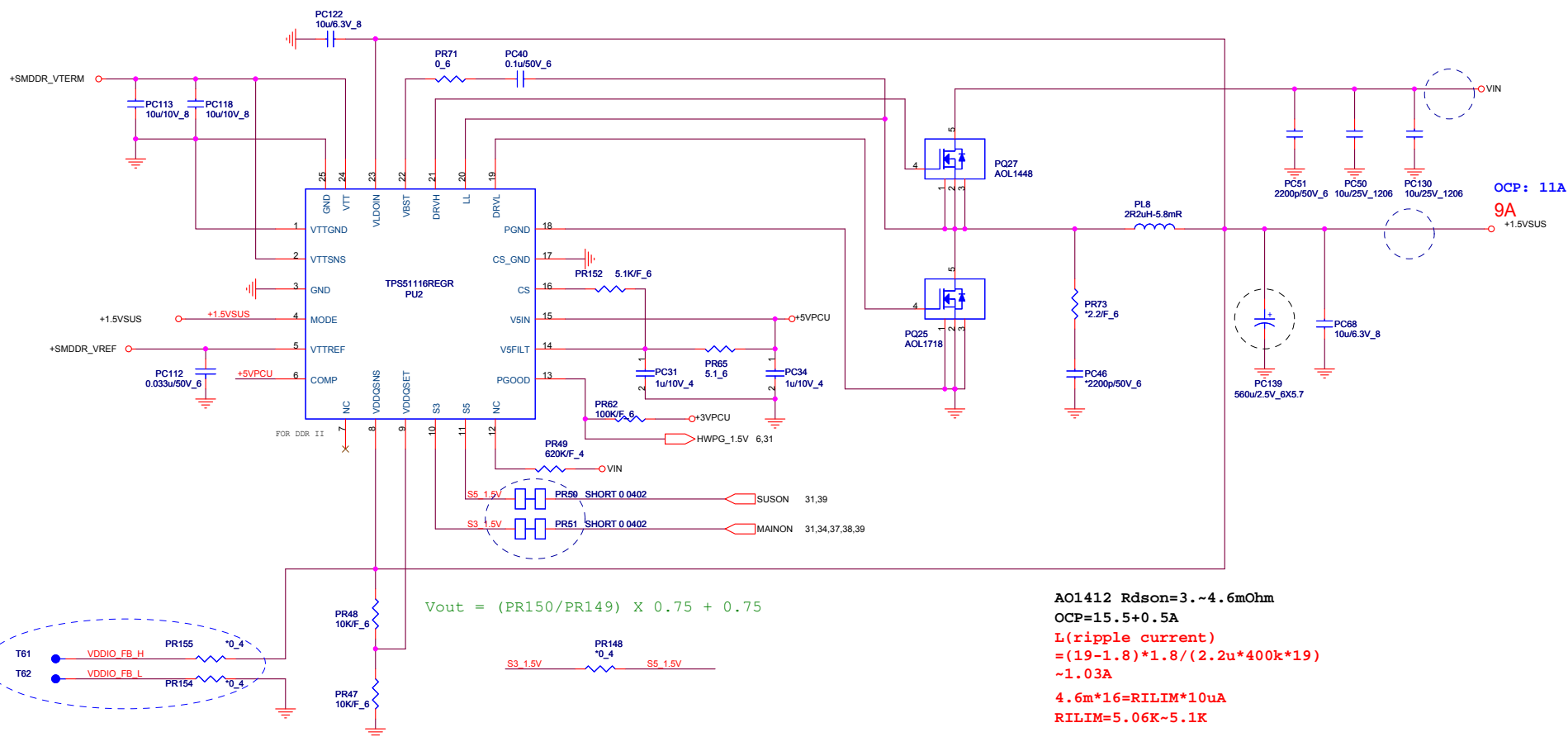
AOL1412 $R_{dson} = 4.6m\Omega$
OCP = 16 - 0.8A
L(ripple current)
 $= (19 - 1.05) * 1.05 / (1u * 272k * 19)$
 $\sim 3.646A$
 $4.6m * 12 = RILIM * 20uA$
RILIM = 2.76K --- 2.8K




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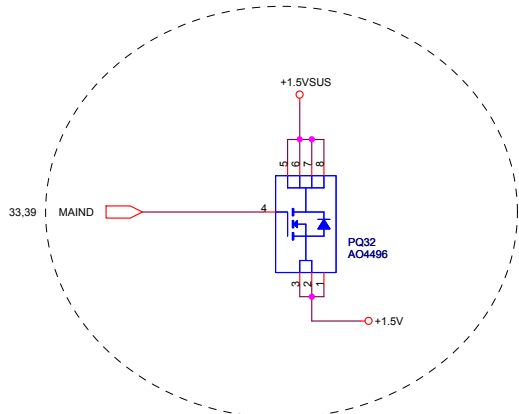
Size	Document Number	Rev
	VCCP 1.05V(UP6111A)	1A
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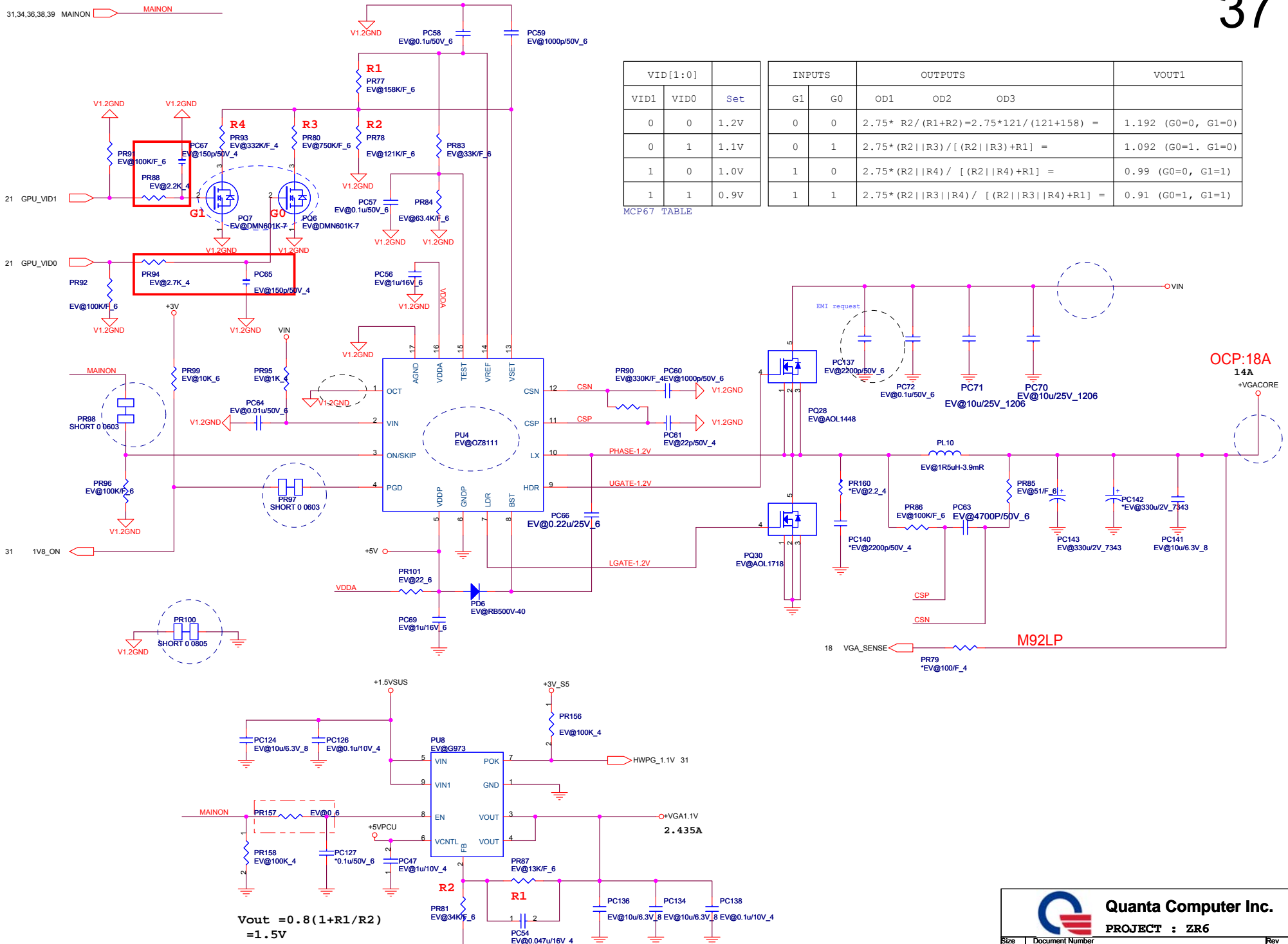


$$V_{out} = (PR150/PR149) \times 0.75 + 0.75$$

AO1412 $R_{dson} = 3. \sim 4.6m\Omega$
 OCP = 15.5 + 0.5A
 $I(\text{ripple current}) = (19 - 1.8) \times 1.8 / (2.2\mu \times 400k \times 19) \sim 1.03A$
 $4.6m \times 16 = RILIM \times 10\mu A$
 $RILIM = 5.06K \sim 5.1K$
 $(10\mu \times PR154) / R_{dson} + \Delta I / 2 = I_{ocp}$



31,34,36,38,39 MAINON



VID[1:0]			INPUTS			OUTPUTS			VOUT1
VID1	VID0	Set	G1	G0	OD1	OD2	OD3		
0	0	1.2V	0	0	2.75 * R2 / (R1+R2) = 2.75 * 121 / (121+158) =			1.192 (G0=0, G1=0)	
0	1	1.1V	0	1	2.75 * (R2 R3) / [(R2 R3) + R1] =			1.092 (G0=1, G1=0)	
1	0	1.0V	1	0	2.75 * (R2 R4) / [(R2 R4) + R1] =			0.99 (G0=0, G1=1)	
1	1	0.9V	1	1	2.75 * (R2 R3 R4) / [(R2 R3 R4) + R1] =			0.91 (G0=1, G1=1)	

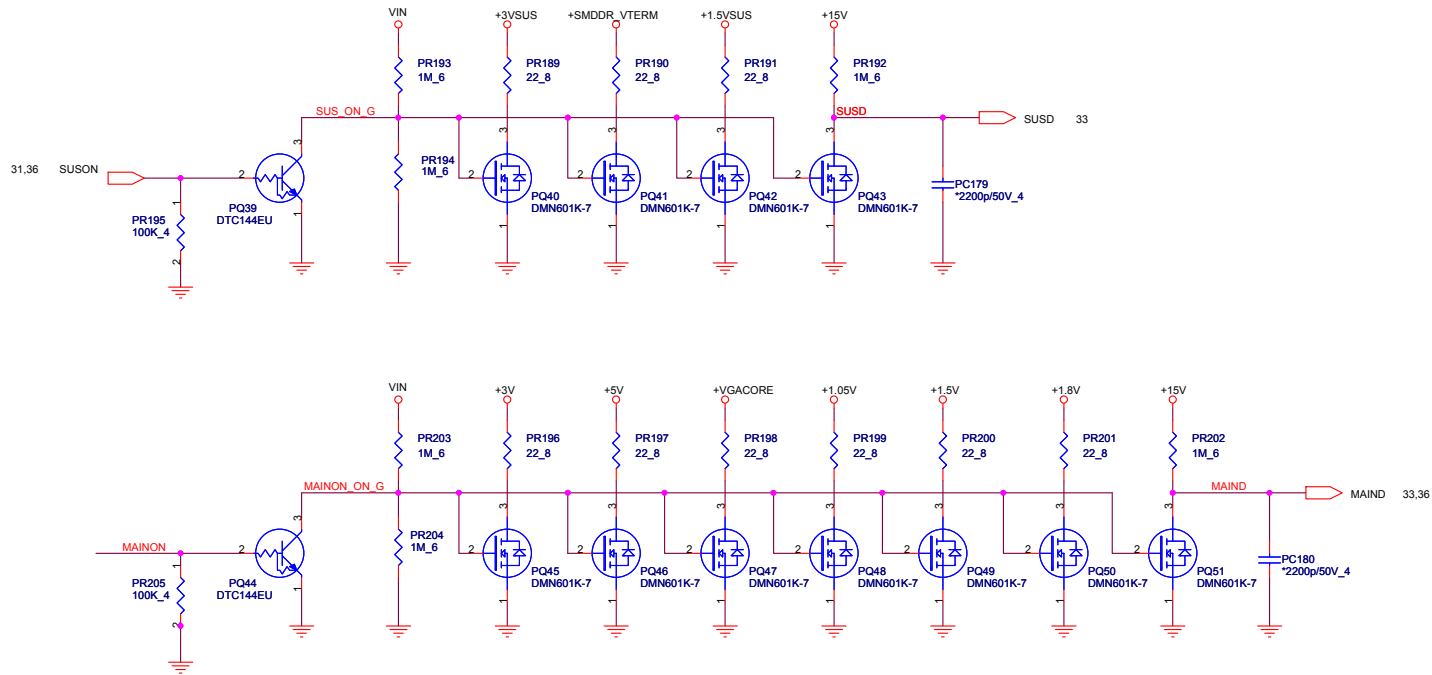
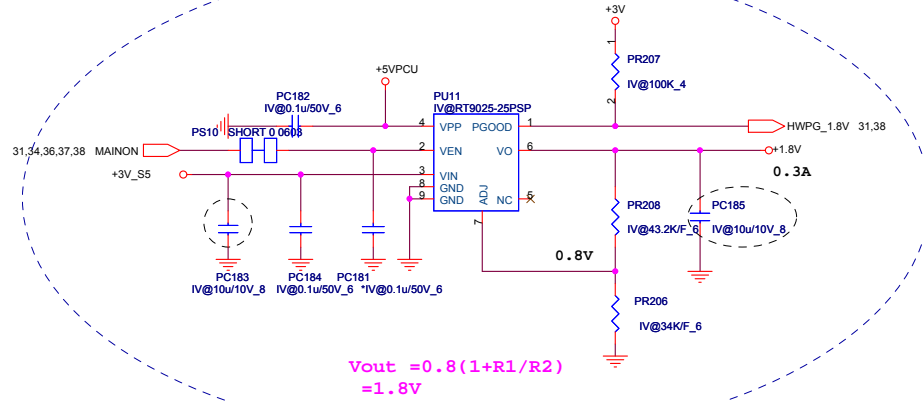
MCP67 TABLE

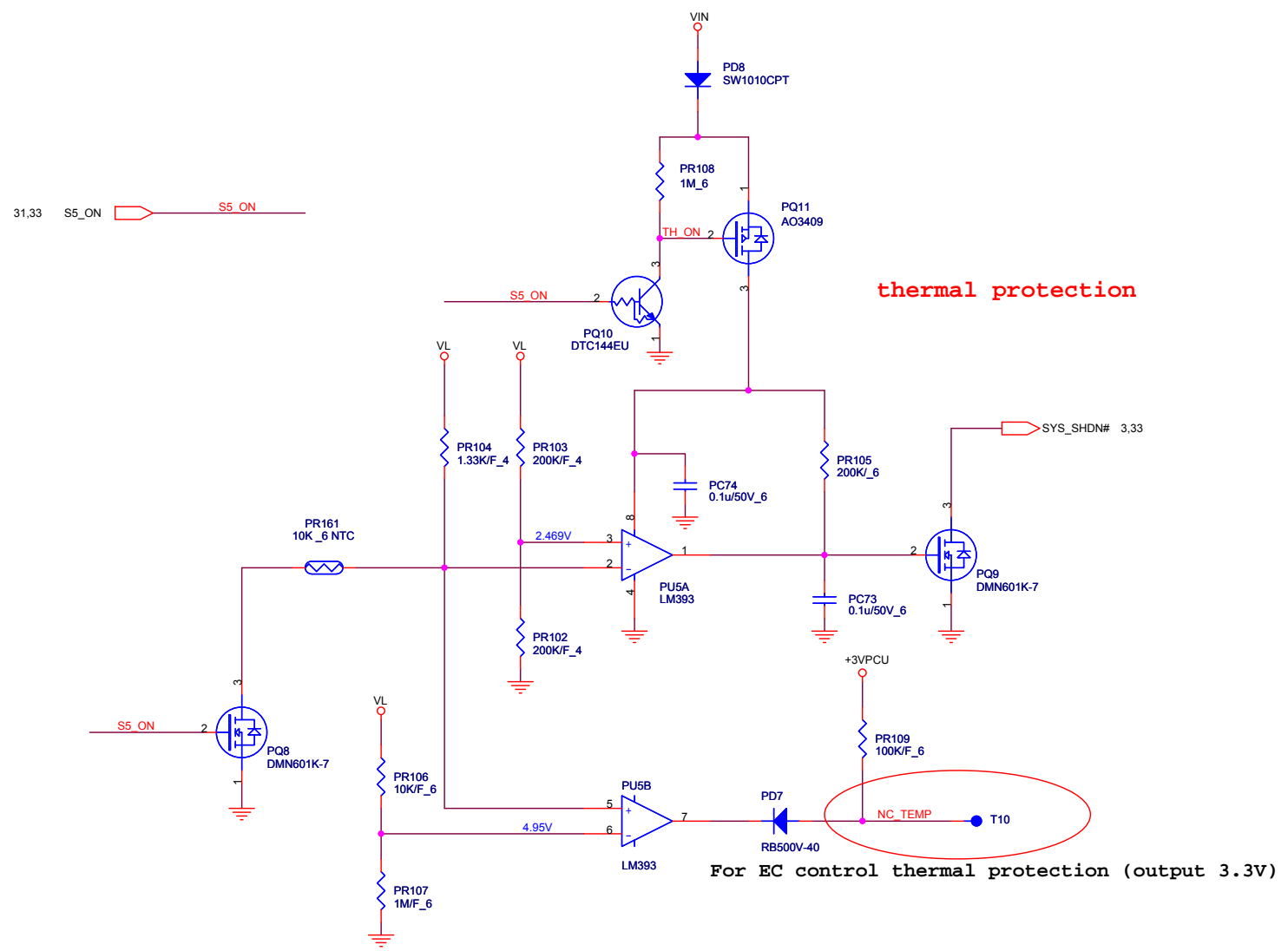
OCP:18A
1.4A
+VGACORE

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	VGA M92LP (OZ8118)	1A
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$$V_{out} = 0.8(1 + R1/R2) = 1.5V$$





thermal protection

For EC control thermal protection (output 3.3V)

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		1A
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Thermal Protection		
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MODEL: REV

CHANGE LIST

PAGE	ZR6 MB	
	FROM	TO
1	1A	
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8	1A	
9	3A	
10	3A	
11	1A	3B
12	1A	
13	1A	
14	3A	
15	2A	
16	1A	
17	3A	3B
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19	3A	
20	1A	
21	3A	
22	1A	
23	3A	
24	3A	
25	2A	
26	3A	
27	2A	
28	3A	
29	3A	3B
30	1A	
31	3A	
32	2A	
33	2A	
34	2A	
35	2A	3B
36	2A	
37	2A	
38	2A	
39	3A	3B
40		

A

First release

B

Page23:Change C209,C522,C567,C533 from CH31003MB14 to CH41002KB93

Page10:change net name +1.8VSUS_TXLVDS-->+1.5VSUS_TXLVDS,+1.8VSUS_VCC_SM_CK-->+1.5VSUS_VCC_SM_CK

Page24:change R174 from 100k to 470K,Del R177 to solve Hall sensor issue

Page25:U12 No stuff and Del R248 to no stuff

Page12:Change R543,R542,Q31 to no stuff,because ZR6 battery can't charging

Page21:VGA ID pin R387 stuff 15k,R382 stuff 45.3K,R414 stuff 25K,R381/R415 no stuff

Page14:MB ID pinR298 Value change to EV@,R308 Valule change to IV@

Page26:change L25 layout and del RN19 and change L23 layout and del RN14

Page24:change L1 layout and del RN1

Page24:Change LCD connector(OT2)

Page33:Mirror the PJ2 connector

Page26:change CN19 footprint to mipci800055fb052g100p1-52p-ldv as ZG5 and Del debug card 0 ohm R518,R517,R514,R511,R510,R315,R310

Page6:Change DD3 power OK circuit as ZK6

Page26:Del R520,R529 and change R538,R536,R532 footprint to short pad

Page24:U11 add pin 49 to thermal pad gnd

Page25:Change CN3 footprint to af7121-a2glt-12p-1-zr6

Page32:Change CN2 footprint to 88502-260N-26P-L-ZR6

Page29:Change U21 footprint to trf-10-1-24p-zr6

Page27:Change U33 footprint to tqfn48-7x7-5-49p-zr6

Page26:Change CN8 footprint to bli123-10r-10p-1-zr6

Page25:Change D1 \ D2 \ D3 footprint to led-ht-110nb5-3p-zr6

Page27:Change CN18 Part Number to DFTJ06FR212 and Change CN21 Part Number to DFTJ06FR211

Page33:Change PJ1 Part Number to DFHD08MR064 for ZR6

Page17:Change C502 to no stuff for cost down

Page26:Change CN8 footprint to bli123-10r-10p-1-zr6& Partumber change to DFFC10FR017

Page2:Del RN15,RN36,RN18,RN22,RN20,RN24,RN23 for cost down &Change R252,R244,R499 to short pad

Page4:Change C58 to No stuff

Page29:change R366,R367,R357,R358 to short pad for cost down

Page27:change R506,R508,R535,R345 to short pad for cost down

Page24:Del R346,R7 for cost down

Page25:Del R218,R407 for cost down

Page26:change C683,C675 to no stuff

Page31:Add C715 for EMI

Page31:Del C466,C467,L35 for cost down

Page24:Add CN1 Pin33,Pin34 to GND ,Add R248,R218 for HDMI and Add L52,L53,L54,L55 for EMI

Page10:change L38 to R037

Page2:Add R511 for Mini_CLKREQ# pull up

Page40:change +3VSUS to +3V_S5,HWPG_1.5V to HWPG_1.8V

Page24:1.Del R248,R218,2.L19,L21 change to R218,R234,3.change D14,D15,R196,R197,R203,R200 vaule to stuff

Page12:Change C450,C451 to 18P

Page28:Change C19,C22 to 33P

Page21:Add MXM ACIN circuit,R177R182,Q33,Q32,R183

Page27:change R574 to no stuff and R541 to stuff

Page24:Add D44 and Del R410

Page28:change R39,R38,U4,C46 to no stuff

Page18-23:change T65,T74,T11,T69,T68,T64,T67,T70,T73,T66,T72,T71 footprint to T3050

Page26:Change C629 to 100uf and C636 to no stuff

Page6:change R175 and R181 to 47K for HDMI vender request

Page24:Change R197,R200 to EV@

MB Assy' P/N: 31ZR6MB0000/10/20/30/40/50/60/70


Project :ZR6 MB

Document No.:

Approved by : Johnny O

Drawing by :Andy Chen

DATE: 2009/03/04



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MODEL: REV

CHANGE LIST

PAGE	MODEL ZR6 MB	
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10	3A	
11	1A	3B
12	1A	
13	1A	
14	3A	
15	2A	
16	1A	
17	3A	3B
18	2A	
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24	3A	
25	2A	
26	3A	
27	2A	
28	3A	
29	3A	3B
30	1A	
31	3A	
32	2A	
33	2A	
34	2A	
35	2A	3B
36	2A	
37	2A	
38	2A	
39	3A	3B
40		

ZR6 MB

B

C

D

E

Page6:change R175 and R181 to 4.7K for HDMI vender request

Page10:change net name +1.5VSUS_TXLVDS--> +1.8V_TXLVDS

Page3:Del Q5,Q6,R62,R63

Page3:change Par Number from AL000780000 to AL000780003 for thermal sensor address change to 9AH

Page21:Del Q10,Q9,R96,R86

Page27:R574 stuff and R541 no stuff

Page31:R300,R301 stuff thermal sensor

Page37:change PC65,PC67 to 150pF

Page28:change U2 PartNumber from AL008131001 to AL008131002(LAN chip)

Page27:change R530,R533 from 10 ohm to 5.1 ohm for headphone

Page27:change CN8 (usb) 12 pin board to board

Page26:Change CN5 footprint to cwy027-b0glz-2p-1,CN16(USB)footprint change to usb-c107h6-10405-1-4p-r-v-nb4

Page30:Change CN7 footprint to 4IN1-R015-212-LM-42P-H-nb4

Page32:PJ1 footprint change to bat-btj-08qn0b-8p-r-v-nb4

Page32:Del R510,change Hole15 Footprint from h-tc315bc433d106p2 to h-tc315bsd106p2

Page04:change C493 to no stuff

Page27:Del T77 and Add R62

Page26:change Hole21 footprint to h-c236d142pt-8

Page24:Change D1 ·D2 ·D3 footprint to led-ht-110nb5-3p

Page24:Change R218,R234 to shortpad

Page26:Change R310 to shortpad

Page10:Change R91,R307,R418,R466,R469 to shortpad

Page29:Add C466,C467 for EMI,Add R358,R357,R366,R367 and change DGND to LAN GND

Page26:Add C716 for EMI

Page30:Change L34 to 0 ohm and C715 to 10P,Change R512,R525,R528,R527 to 20K 1% and Change R526,R515,R524,R522 to 47K 1%

Page25:Change R1,R4,R10,R365,R369,R368 to 221 ohm and Change D1,D2,D3 part number

Page14:Change R282 to no stuff

Page28:Change R26 to no stuff

Page26:Change Hole29 part number to MBZR6005010

Page29:Del net name LAN_LNK_LED_FWR

Page14:Add R583 and R315 at GPIO7 for HDMI option,change R583 to no stuff and R315 to stuff

Page24:change HDMI item to no stuff(remove this function)

Page12:change R225,R216,R241,R220,R219,R215,R213,R214,R228,R227 to no stuff for remove HDMI Audio

Page26:Change Hole 16 footprint as hole1

Page37:change PR97,PR98 to short-pad ,change PU4 OZ8116 change to OZ8111 for cost issue ,Del PC62

Page27:C670 change value from 1U to 4.7U (CH5471M9907)

Page29:change c478 from 1000p to 220p.(CH122GK1I10)

Page28:change C18 from 0.1u to 1000p (CH21006JB10),change C20 from 0.1u to 1u (CH5102K9B06) ,ADD C723 0.1u (CH41002KB93) ,ADD C720 1u (CH5102K9B06)

Page25:change DHP00DA1G03->DHPTME53201

Page24:add C722 (CH6101M9905) to solve ISN issue

Page27:the PC beep will change Gain from -6db to -18 db , so R559 needs stuff 10k on all BOM.


Page34:change PC133 from CC7560JMZ15 to CC7560JMZ02 for cost down

Page36:change PC139 from CC7560JMZ15 to CC7560JMZ02 for cost down

Page38:change PC156 from CC7560JMZ15 to CC7560JMZ02 for cost down

Page33:change PC158,PC162 from CC73301MZB2 to CC73301MZ04 for cost down

Page37:change PQ6,PQ7 from BAM700200F6 to BAM601K0003 for cost down



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