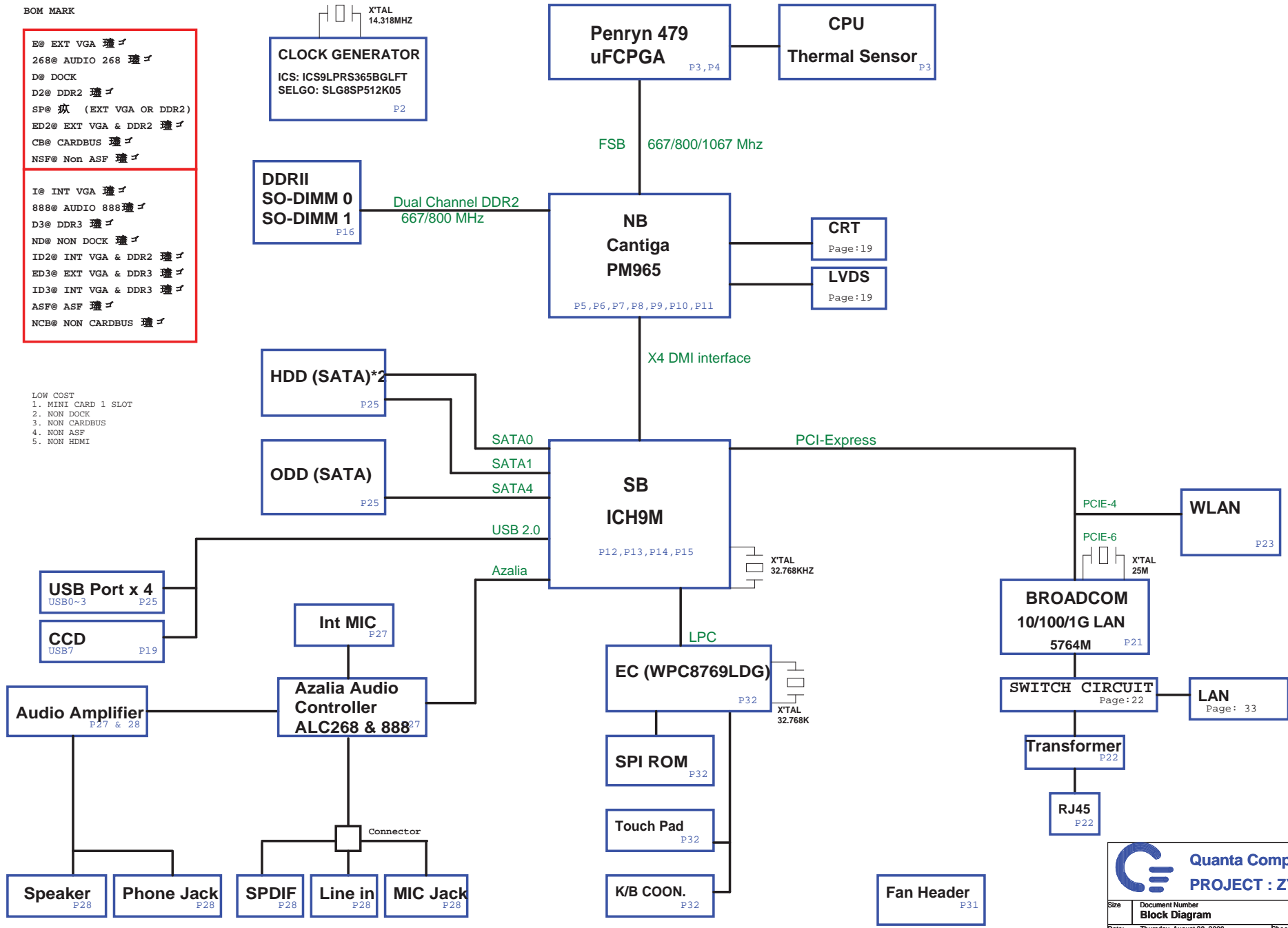


# ZY6D SYSTEM BLOCK DIAGRAM

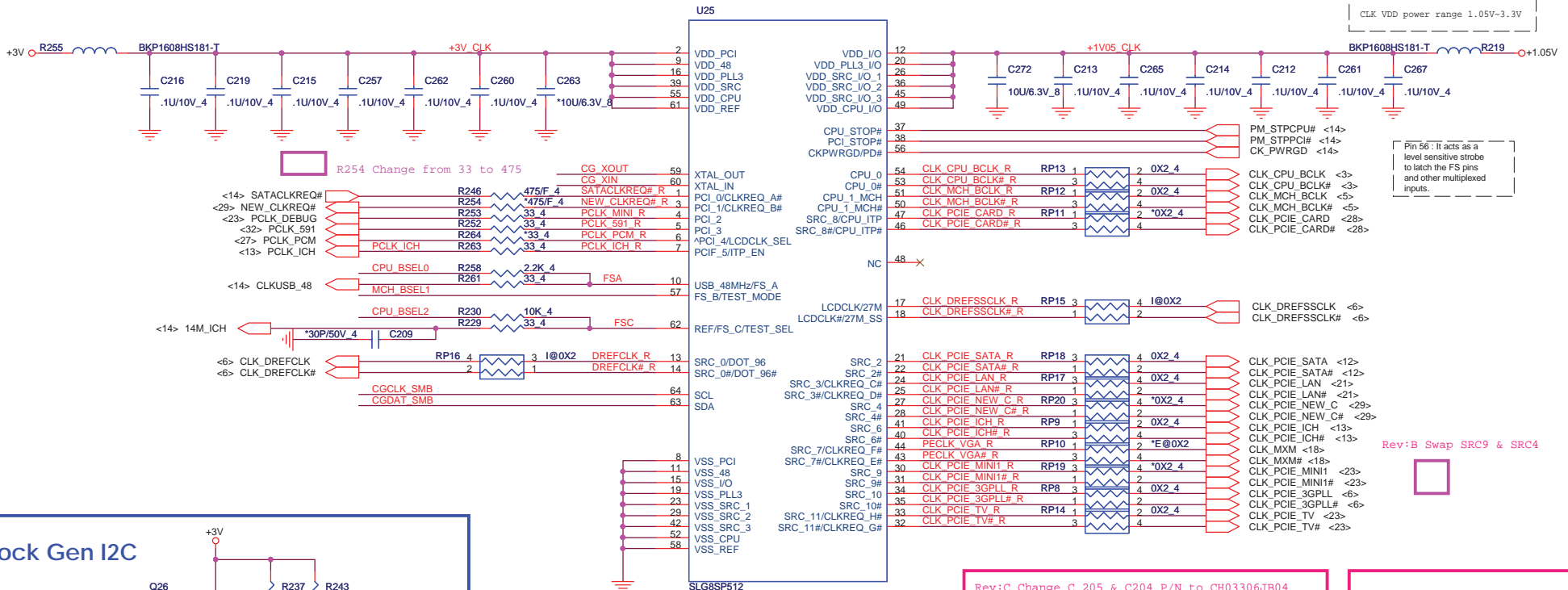
**BOM MARK**

- E@ EXT VGA 璫 ㄣ
  - 268@ AUDIO 268 璫 ㄣ
  - D@ DOCK
  - D2@ DDR2 璫 ㄣ
  - SP@ ㄣ (EXT VGA OR DDR2)
  - ED2@ EXT VGA & DDR2 璫 ㄣ
  - CB@ CARDBUS 璫 ㄣ
  - NSF@ Non ASF 璫 ㄣ
- 
- I@ INT VGA 璫 ㄣ
  - 888@ AUDIO 888璫 ㄣ
  - D3@ DDR3 璫 ㄣ
  - ND@ NON DOCK 璫 ㄣ
  - ID2@ INT VGA & DDR2 璫 ㄣ
  - ED3@ EXT VGA & DDR3 璫 ㄣ
  - ID3@ INT VGA & DDR3 璫 ㄣ
  - ASF@ ASF 璫 ㄣ
  - NCB@ NON CARDBUS 璫 ㄣ

- LOW COST
1. MINI CARD 1 SLOT
  2. NON DOCK
  3. NON CARDBUS
  4. NON ASF
  5. NON HDMI



# Clock Generator

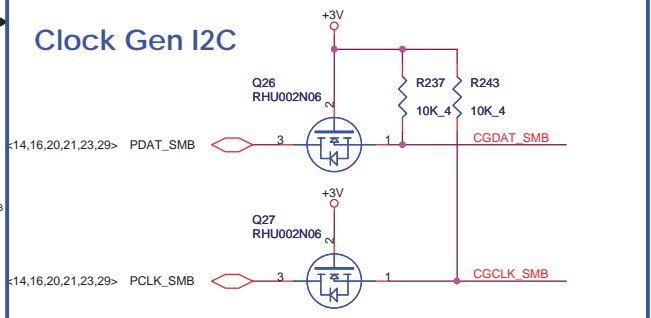


R254 Change from 33 to 475

Pin 56: It acts as a level sensitive strobe to latch the FS pins and other multiplexed inputs.

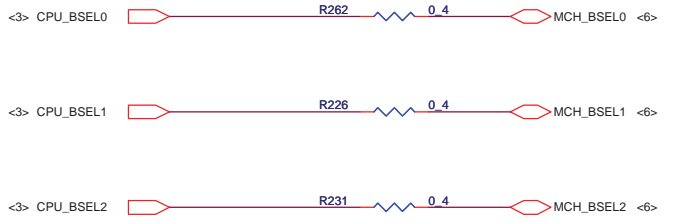
Rev:B Swap SRC9 & SRC4

## Clock Gen I2C



## CPU Clock select

Pin 10/57/62: For Pin CPU frequency selection

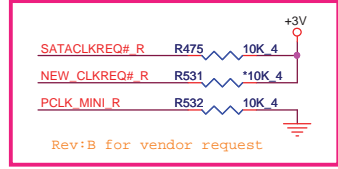
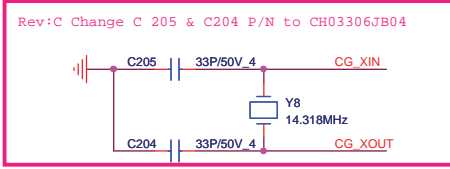


CRB Rev0.7: 110(CBA)

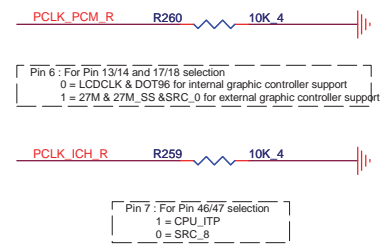
	QCI P/N
SLG8SP512	AL8SP512K05
ICS9LPRS365BGLFT	ALPRS365K13


## BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz



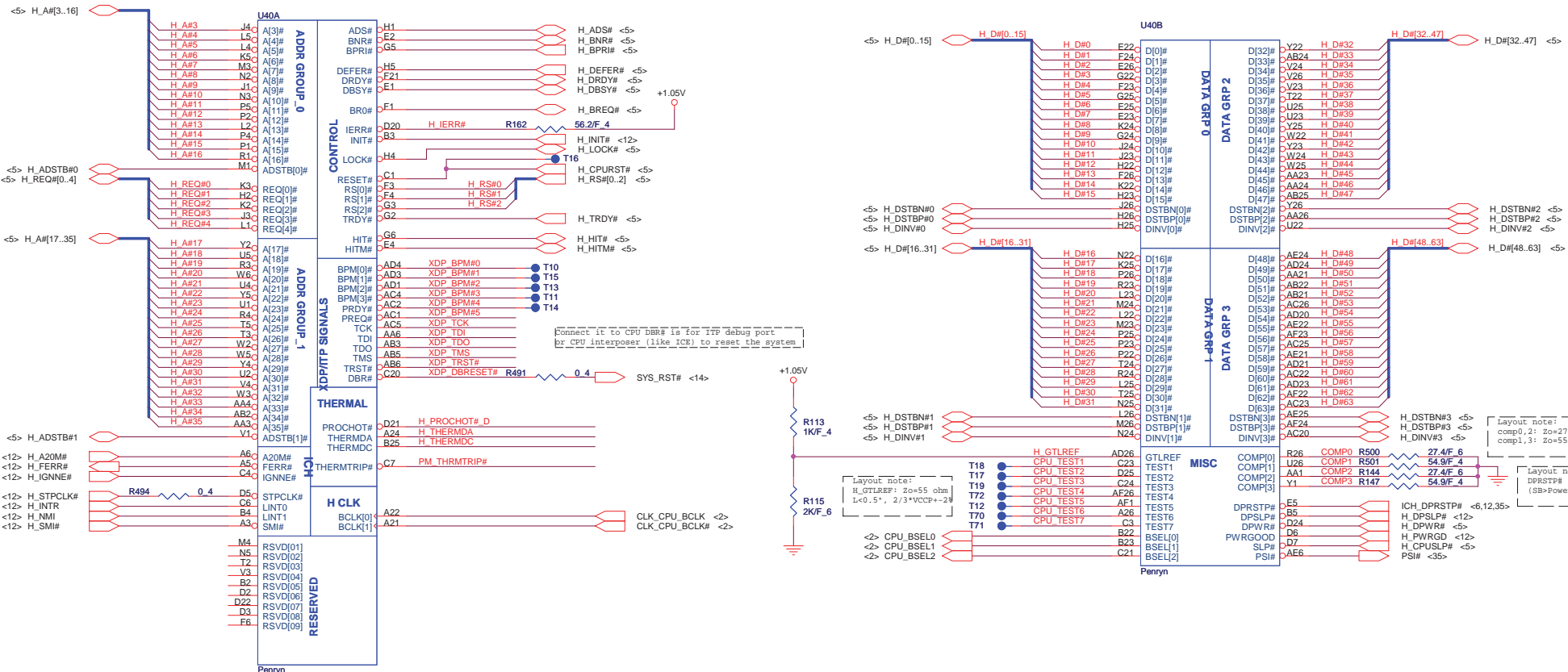
## Strap table



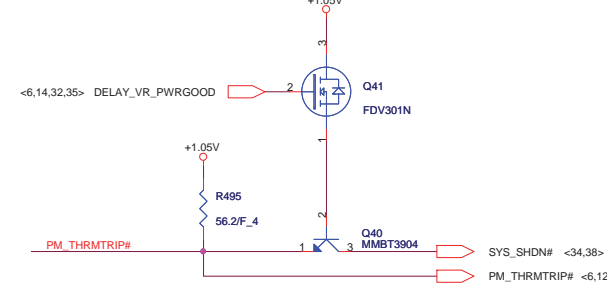


**Quanta Computer Inc.**  
**PROJECT : ZY2 & ZY6**

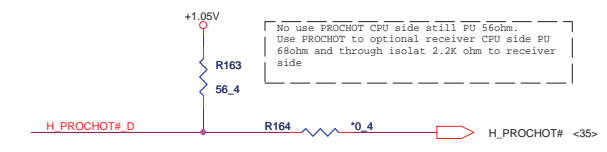
Size	Document Number	Rev
	<b>CLOCK GENERATOR CK505 W/REGULATOR</b>	1A
Date:	Thursday, August 26, 2008	Sheet 2 of 40



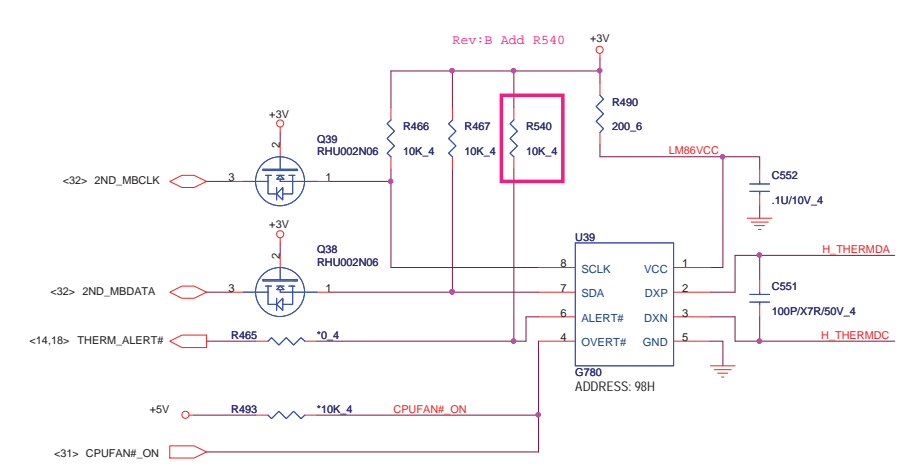
**Thermal Trip**



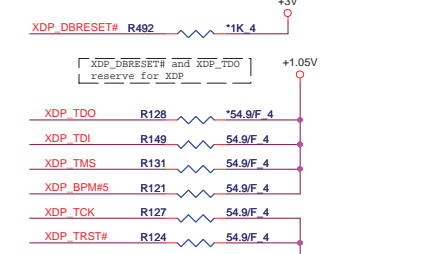
**Processor hot**



**CPU Thermal monitor**

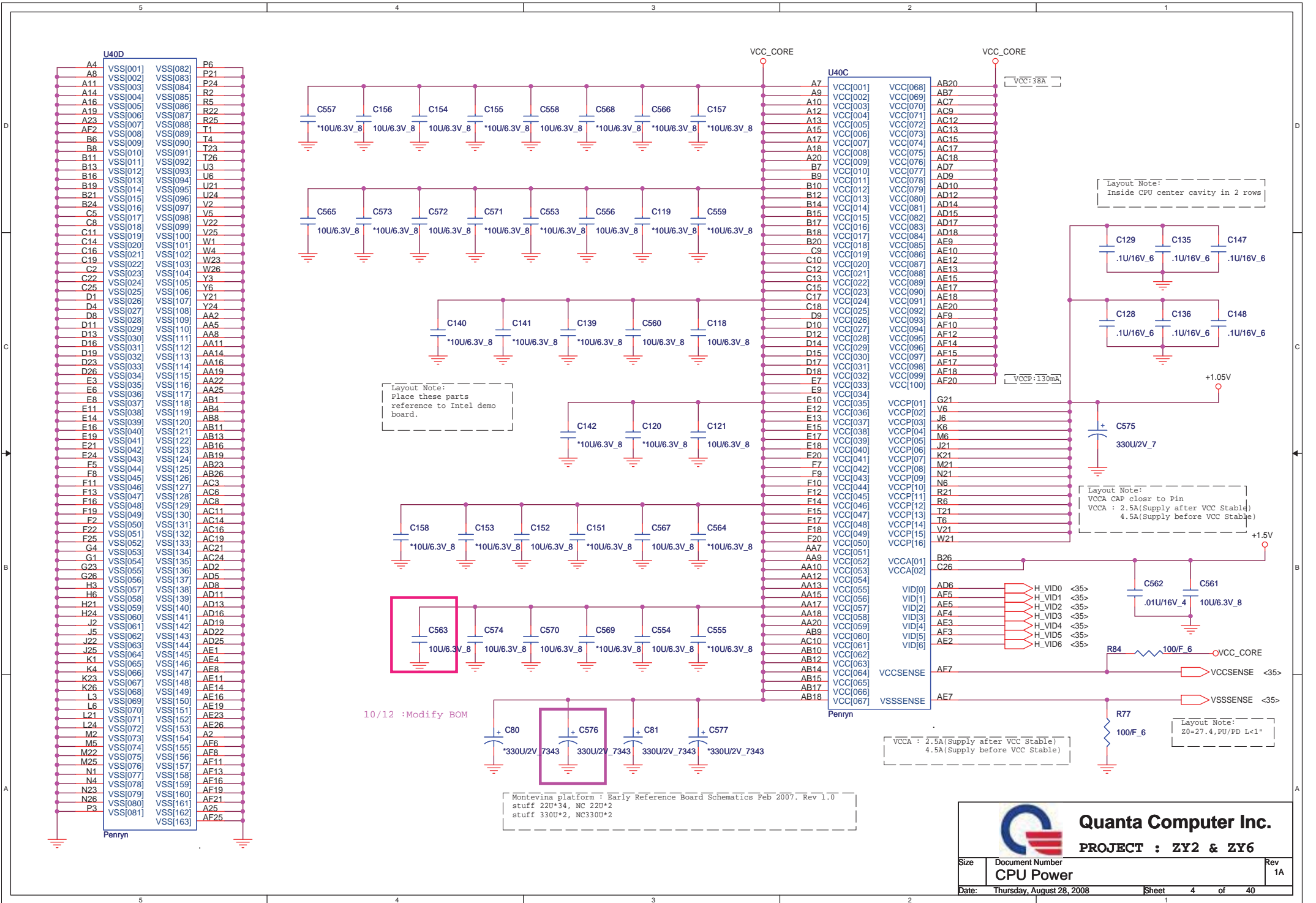


**XDP PU/PD**



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**PROJECT : ZY2 & ZY6**

Size	Document Number	Rev
	CPU Hot Bus	1A
Date:	Thursday, August 28, 2008	Sheet 3 of 40



Layout Note:  
Inside CPU center cavity in 2 rows

Layout Note:  
Place these parts  
reference to Intel demo  
board.


Layout Note:  
VCCA CAP close to Pin  
VCCA : 2.5A(Supply after VCC Stable)  
4.5A(Supply before VCC Stable)

Layout Note:  
20=27.4, PU/PD L<1"

Montevina platform : Early Reference Board Schematics Feb 2007. Rev 1.0  
stuff 22U\*34, NC 22U\*2  
stuff 330U\*2, NC330U\*2

10/12 :Modify BOM

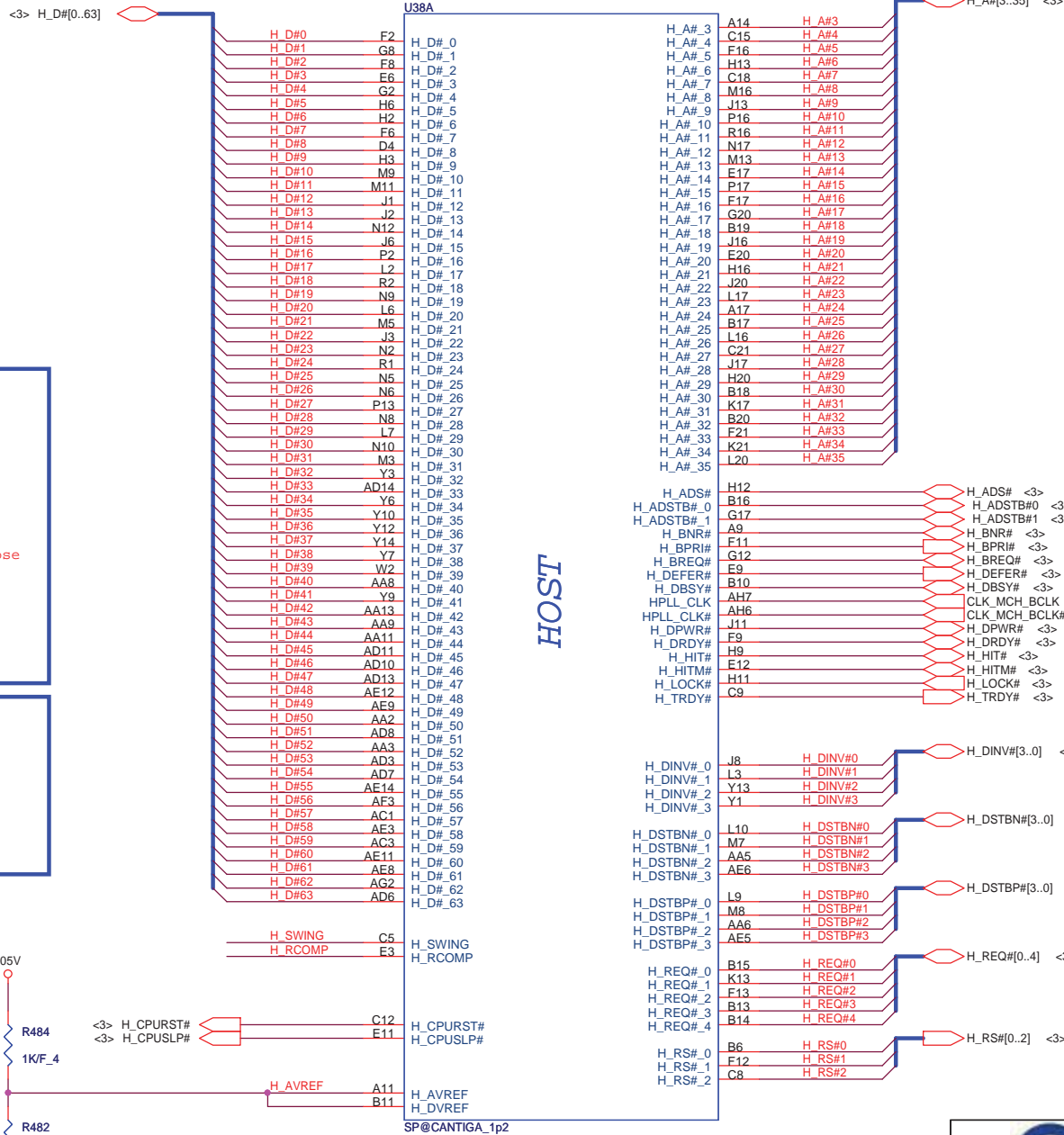
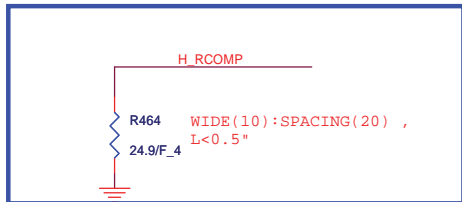
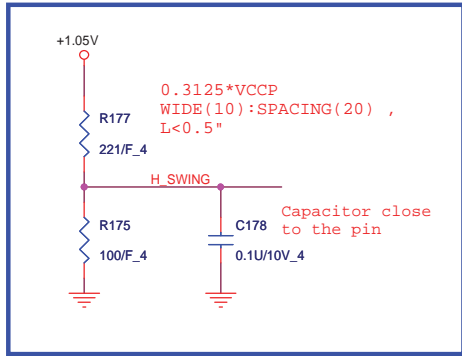
VCCA : 2.5A(Supply after VCC Stable)  
4.5A(Supply before VCC Stable)




**Quanta Computer Inc.**  
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	<b>CPU Power</b>	1A
Date:	Thursday, August 28, 2008	Sheet 4 of 40

	QCI P/N
Intel Cantiga (G)M	AJSLB940T04
Intel Cantiga (P)M	AJSLB970T06



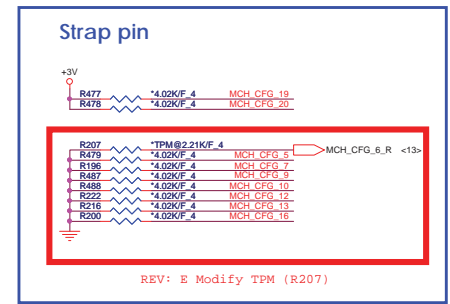
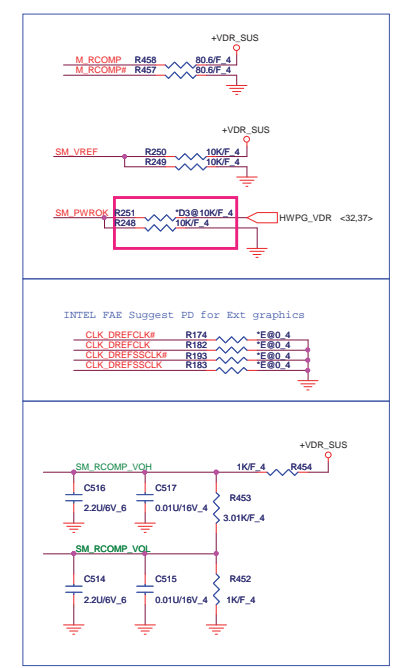
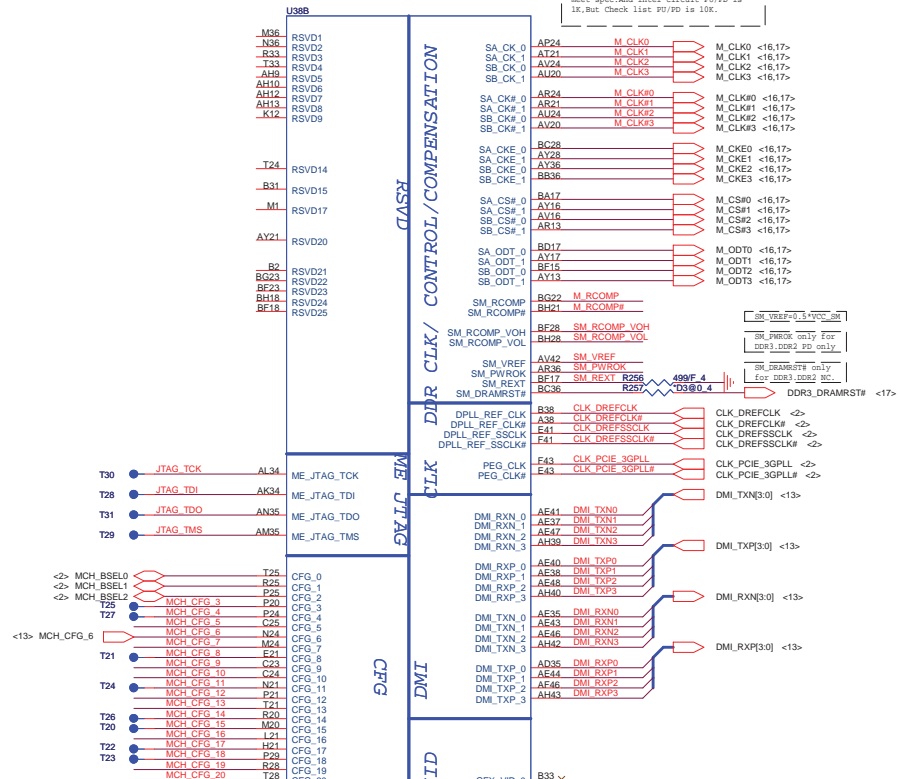
 **Quanta Computer Inc.**  
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	GMCH HOST	1A
Date:	Thursday, August 28, 2008	Sheet 5 of 40

# Strap table

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)
CFG7	MS TLS confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)
CFG8	Reserved	
CFG9	PCIe Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG10	PCIe Loopback enable	0 = Enabled 1 = Disabled (Default)
CFG11	Reserved	
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed
CFG20	Digital Display Port (SDVO/DP/HDMI) Concurrent with PCIe	0 = Only Digital Display port (SDVO/DP/HDMI) or PCIe is operational (Default) 1 = Digital Display port (SDVO/DP/HDMI) and PCIe are operating simultaneously via PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI Device Present(Default) 1 = SDVO/HDMI Device present
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present

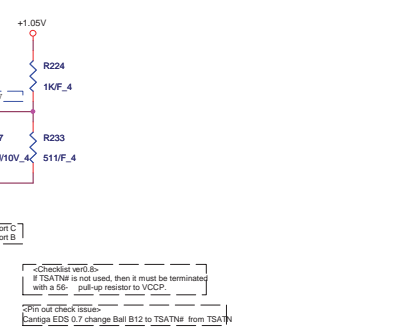
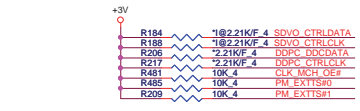
SR\_VREF Default use voltage divider for poor layout cause +SMDCR\_VREF not meet spec. Add Intel circuit PU/PD is 1K, but check list PU/PD is 10K.



REV: E Modify TPM (R207)

MS Thermal trip pin  
No use Thermal trip MS side can NC. (MS has ODT)

TPM\_DPSTP#  
The Daisy chain topology should be routed from IO39M to IWPV, then to (G)IWM and CPU, in that order.

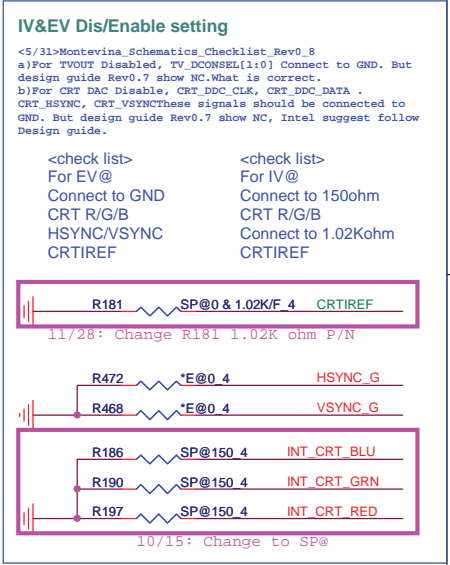
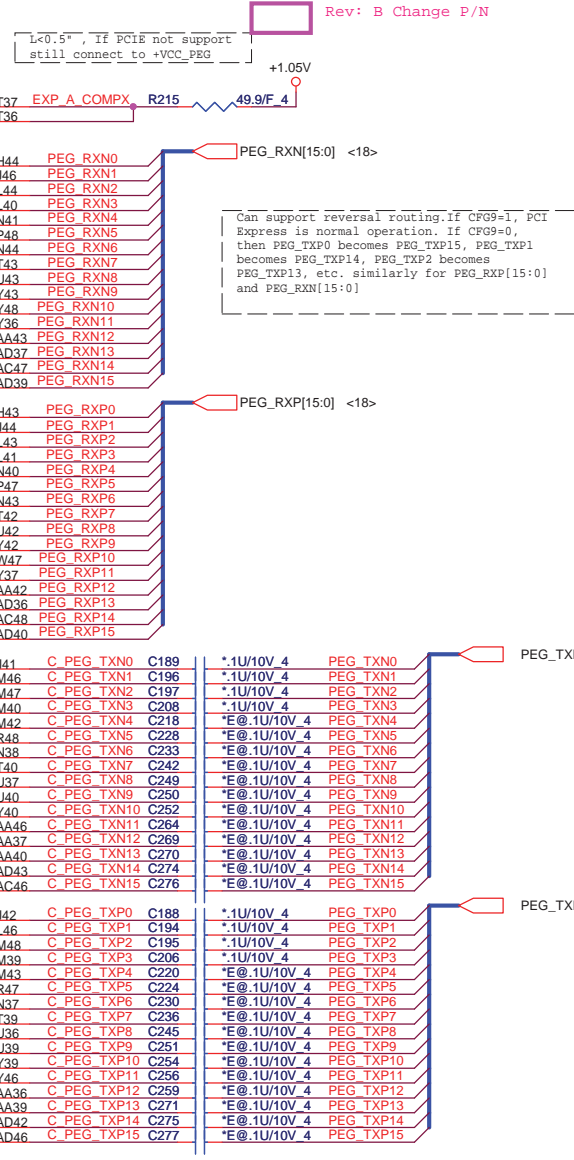
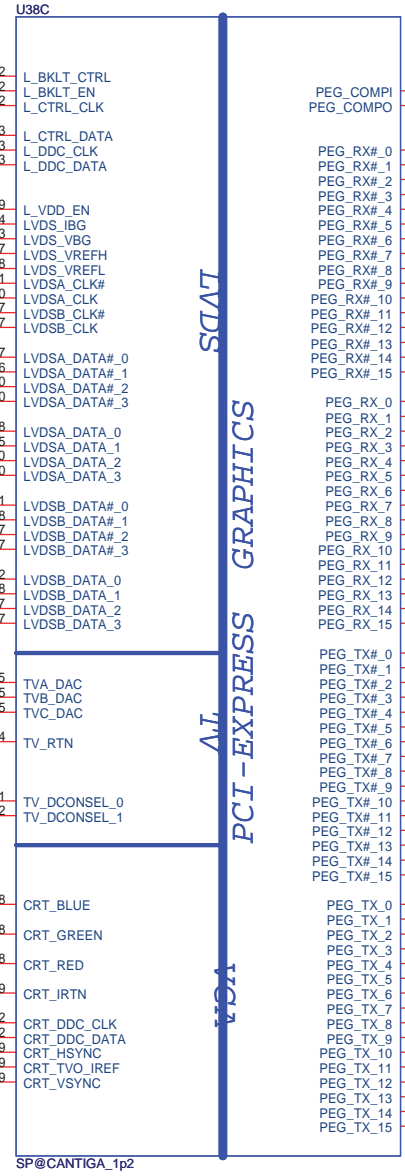
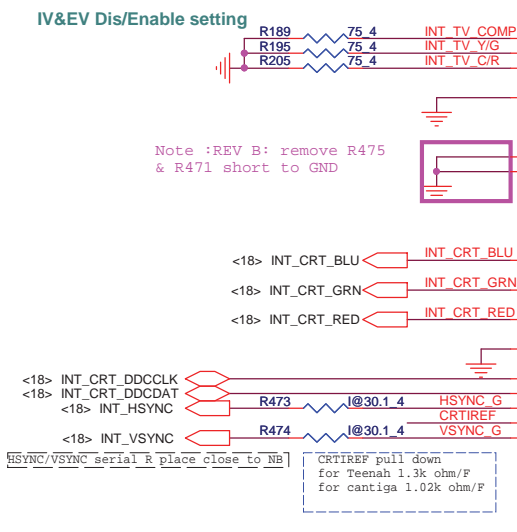
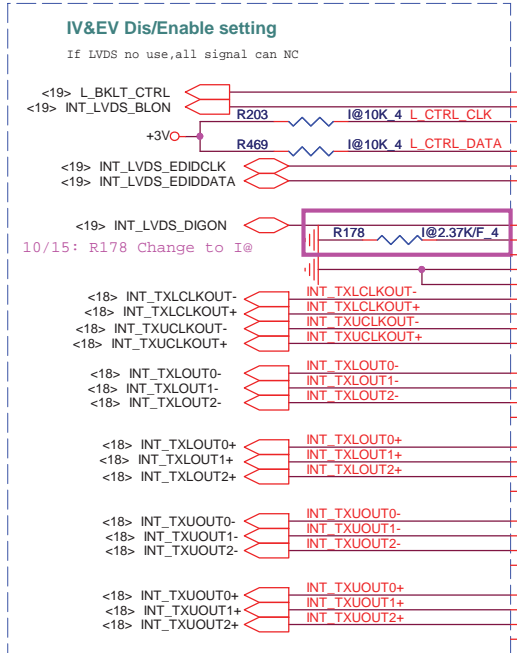



NOTE:  
If (G)IWM's HD Audio signals are connected to IO39M for HDMI, VCCBDA and VCCSIBBDA on IO39M should be only on 1.5V. These power pins on IO39M can be supplied with 3.3V if and only if (G)IWM's HDA is not connected to IO39M. Consequently, only 1.5V audio/modem codecs can be used on the platform.

Checklist ver: a-  
If TSATN# is not used, then it must be terminated with a 50-ohm pull-up resistor to VCCP.  
VCC\_HDA -> GND  
Differential signal -> NC  
\*P/N not check issue\*  
\*Change EOS 0.7 change Ball B12 to TSATN# from TSA1N#

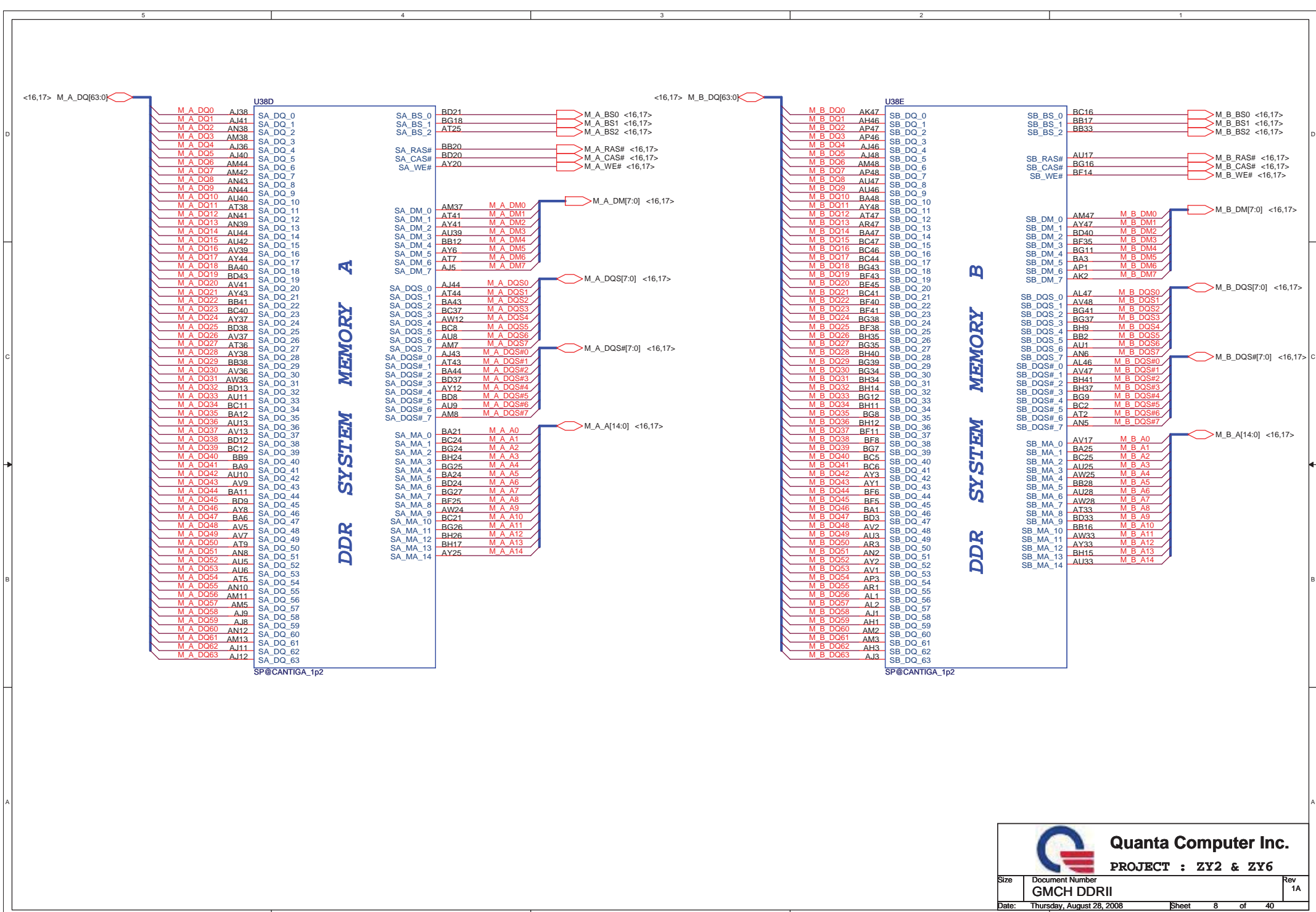
SP@CANYIGA\_1p2

**Quanta Computer Inc.**  
PROJECT : ZY2 & ZY6  
Rev 1A  
Document Number: GMCH\_DMI  
Date: Thursday, August 28, 2008  
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 **Quanta Computer Inc.**  
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	GMCH VGA	1A
Date:	Thursday, August 28, 2008	Sheet 7 of 40



U38D

U38E

DDR SYSTEM MEMORY A

DDR SYSTEM MEMORY B

SP@CANTIGA\_1p2

SP@CANTIGA\_1p2

**Quanta Computer Inc.**  
PROJECT : ZY2 & ZY6

Size	Document Number	Rev	
	GMCH DDRII	1A	
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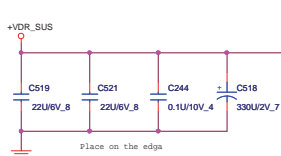
Power consumption reference to Intel  
644135 Cantiga chipset EDS Volume1.  
Section 10

GM TDP 10.5-12W  
GS TDP 7-8W  
PM TDP 7W

Intel check list(Rev 0.8)  
No description for VCC\_SM bulk cap  
330uF Reserve near to power  
330uF1 near to NB

Intel check list(Rev 0.8)  
270uF1 near to power(+V1.05M).  
270uF2 near to NB  
Intel CR8(Rev 0.7)  
270uF3 near to power(+V1.05M).  
270uF1 near to NB  
ESR=12m ohm

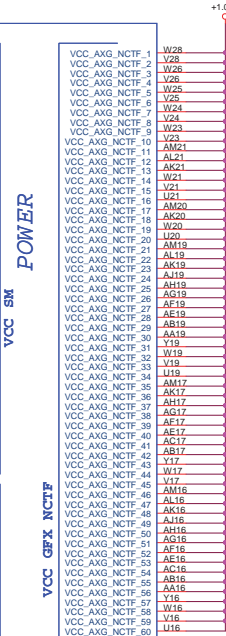
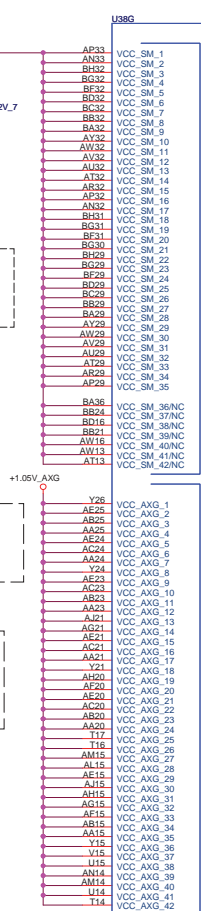
VCC  
VCC\_NCTF  
1210.34mA\_EV  
1930.4mA\_IV  
ME Engine  
508.12mA  
Total Max=2438.52mA



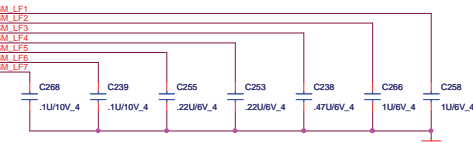
VCC\_SM(1.5V)  
DDR2(800M)  
3000mA\_S0, 1mA\_S3  
DDR2(667M) : 2600mA\_S0  
DDR3(1067M) : 4140mA\_S0

1.05v  
Graphics core  
VCC\_AKG  
VCC\_AKG\_NCTF  
6326.84mA

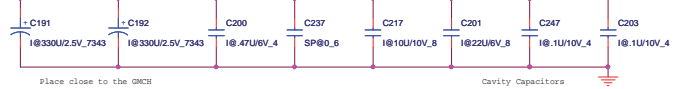
To Edge regulator is shared between the Graphics Core Ball,  
VCCA\_HPL, VCCD\_HPL,  
VCCA\_PRL, VCCD\_PRL,  
VCCA\_HPLB, VCCD\_HPLB,  
VCCA\_SM, VCC\_AXP



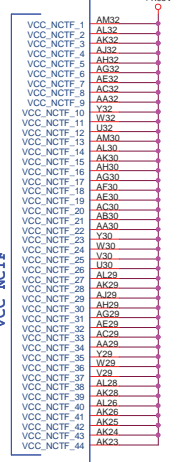
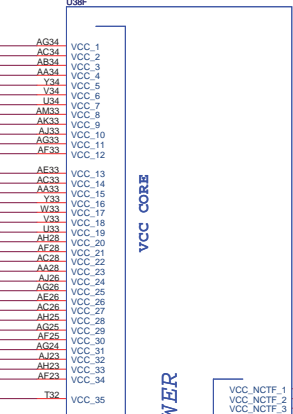
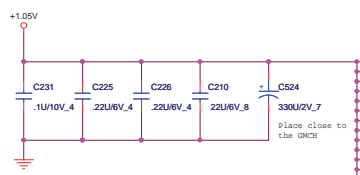
1.8V  
Internal connect to power



IV&EV Dis/Enable setting  
Design guide(Table 72)  
For INT VDD disable, VCC\_AKG power can connect to GND



Intel check list(Rev 0.8)  
270uF2 near to NB(ESR=15m ohm)  
Intel CR8(Rev 0.7)  
270uF4 near to power(+V1.05M).  
270uF2 near to NB



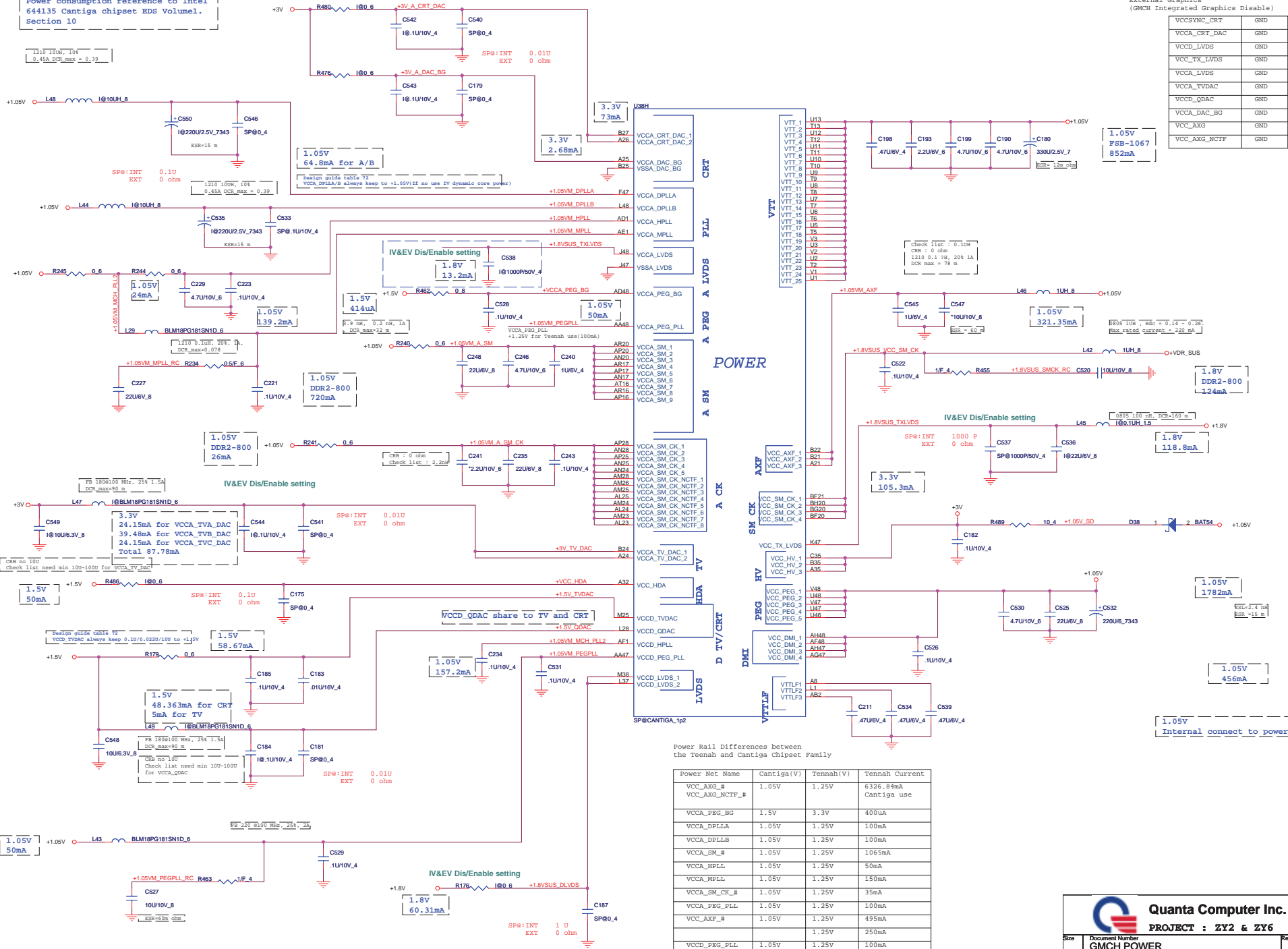
1. Route VCC\_AKG\_SENSE and VBS\_AKG\_SENSE differentially  
2. VCC\_AKG\_SENSE PU to +VDR\_CORE\_INT with 100m  
and VBS\_AKG\_SENSE PU with 100m for Intel suggest

Power consumption reference to Intel 644135 Cantiga chipset EDS Volumel. Section 10

1210 100m, 104  
0.45A DCP\_max = 0.39

External Graphics  
(GMCH Integrated Graphics Disable)

VCCSYNC_CRT	GND
VCCA_CRT_DAC	GND
VCCD_LVDS	GND
VCC_FX_LVDS	GND
VCCA_LVDS	GND
VCCA_TV_DAC	GND
VCCD_QDAC	GND
VCCA_DAC_BG	GND
VCC_AXG	GND
VCC_AXG_NCTF	GND

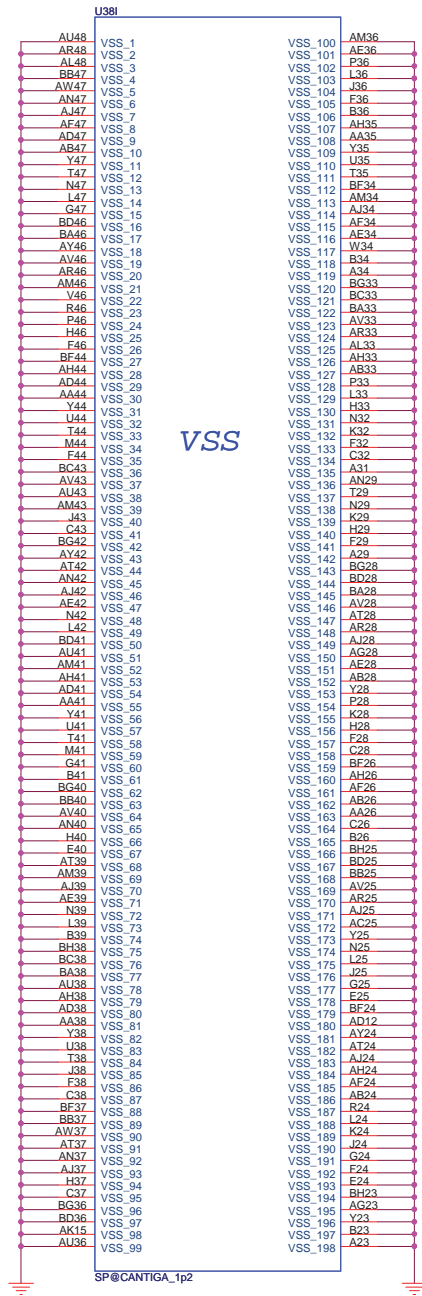


Power Rail Differences between the Tenah and Cantiga Chipset Family

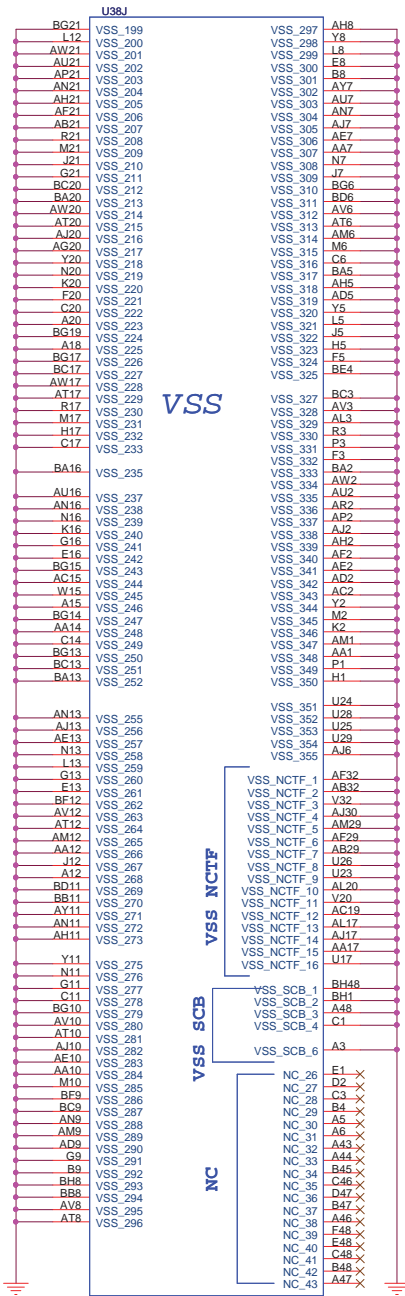
Power Net Name	Cantiga(V)	Tenah(V)	Tenah Current
VCC_AXG_#	1.05V	1.25V	6326.84mA Cantiga use
VCC_AXG_NCTF_#	1.05V	1.25V	
VCCA_PEG_BG	1.5V	3.3V	400uA
VCCA_DPLLA	1.05V	1.25V	100mA
VCCA_DPLLB	1.05V	1.25V	100mA
VCCA_SM_#	1.05V	1.25V	1065mA
VCCA_HPPLL	1.05V	1.25V	50mA
VCCA_MPLL	1.05V	1.25V	150mA
VCCA_SM_CK_#	1.05V	1.25V	35mA
VCCA_PEG_PLL	1.05V	1.25V	100mA
VCC_AXF_#	1.05V	1.25V	495mA
VCC_PEG_LL	1.25V	250mA	
VCCD_PEG_PLL	1.05V	1.25V	100mA

**Quanta Computer Inc.**  
PROJECT : ZY2 & ZY6

Size:  Document Number: **GMCH POWER** Rev: **1A**  
Date: **Thursday, August 28, 2008** Sheet: **10** of **40**



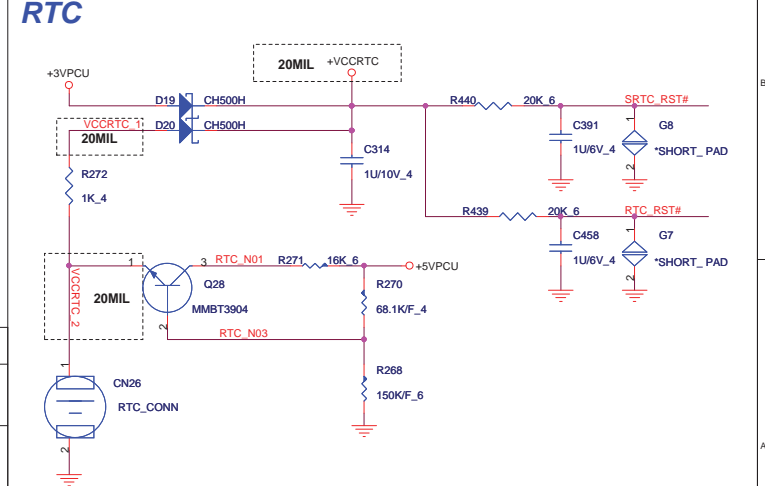
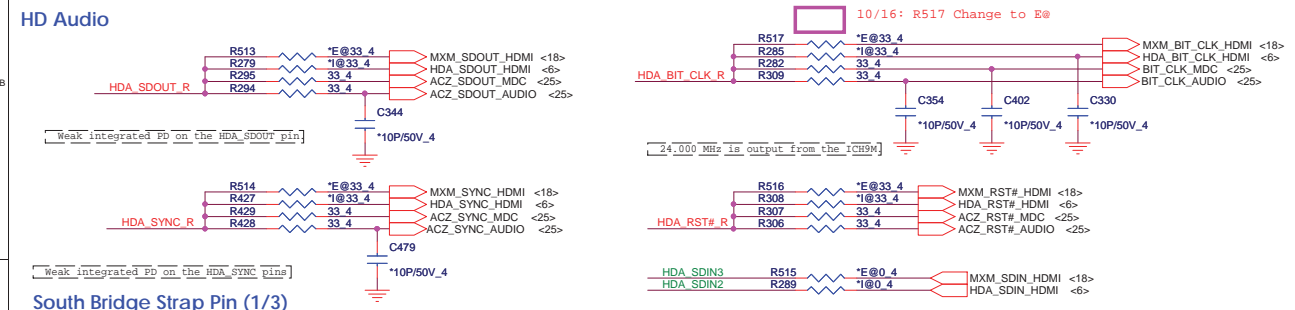
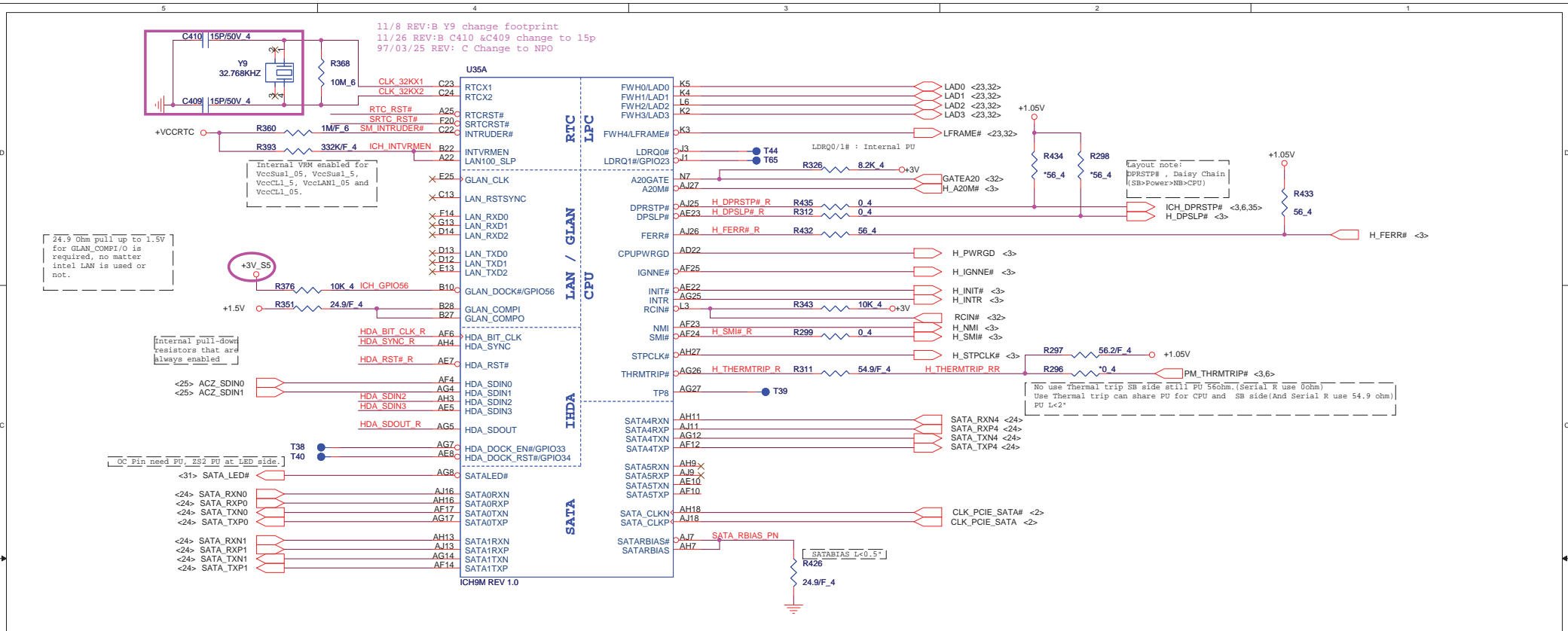
SP@CANTIGA\_1p2



SP@CANTIGA\_1p2

**Quanta Computer Inc.**  
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	<b>GMCH VSS</b>	1A
Date:	Thursday, August 28, 2008	Sheet 11 of 40

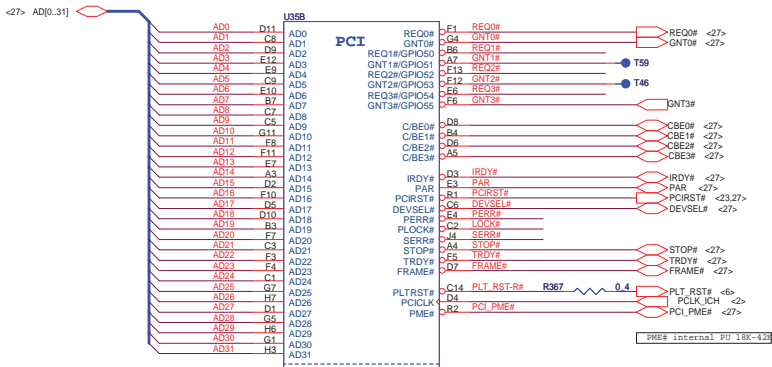


Pin Name	Strap description	Sampled	Configuration	PU/PD	
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.	
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU		
TP3	XOR Chain Entrance	PWROK	ICH_TP3	Description	<14> ICH_TP3 ICH_TP3 R406 1K.4
			0	RSVD	
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1 (Port 1-4)	PWROK	0	Enter XOR Chain	
			1	Normal operation(Default)	
			1	Set PCIE port config bit 1	

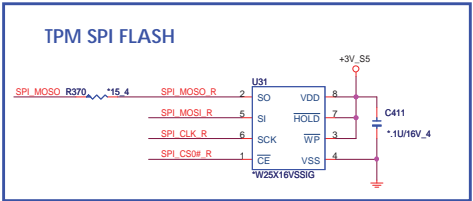
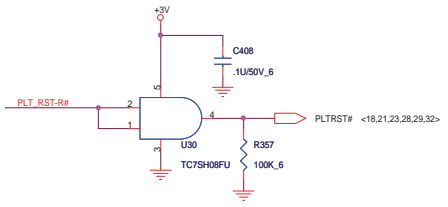
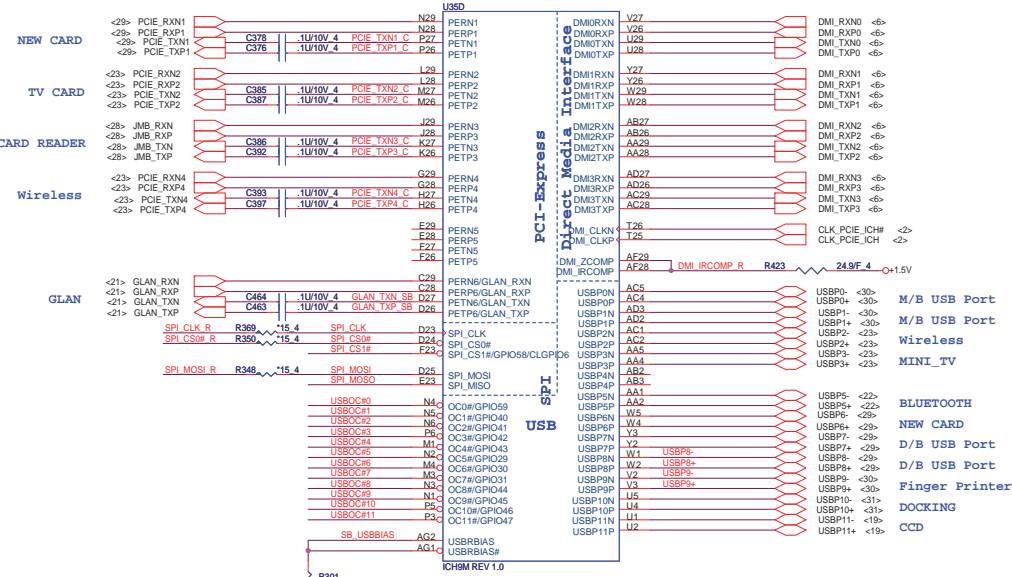
**Quanta Computer Inc.**  
 PROJECT : ZY2 & ZY6

Size: Document Number ICH9M HOST Rev 1A

Date: Thursday, August 28, 2008 Sheet 12 of 40

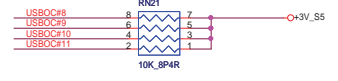
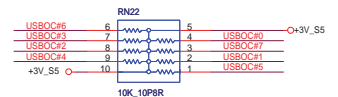
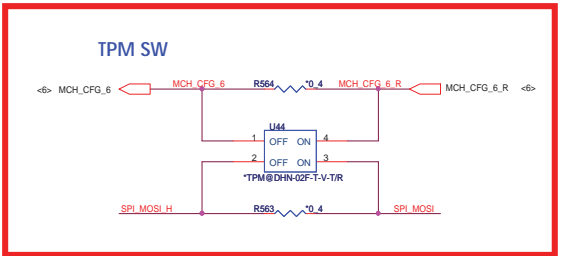


TM & AS	Y
LOW COST	N

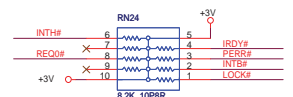
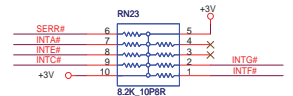
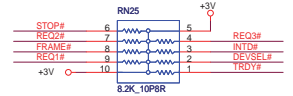


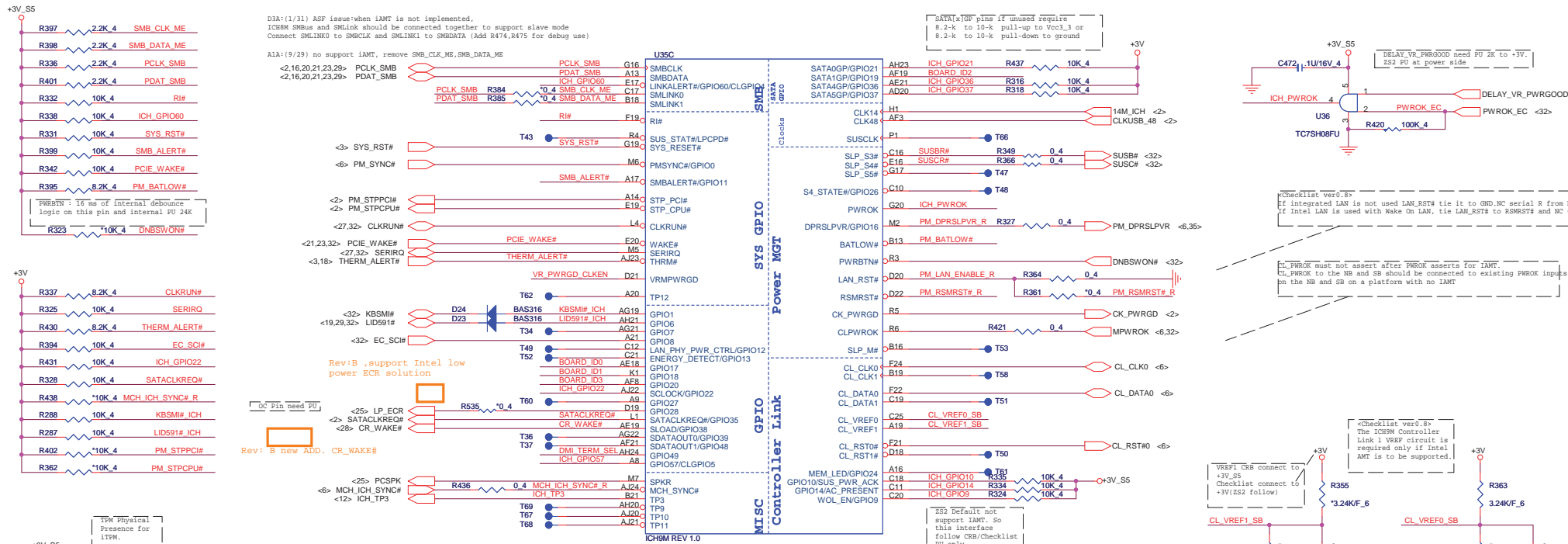
South Bridge Strap Pin (2/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD						
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0							
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default							
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default							
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	GNT3# R347 *1K_4						
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	SPI_MOSI_H R329 *TPM@10K_4 >+3V_S5						
GNT0#	Boot BIOS Selection 0	PWROK	<table border="1"> <tr> <td>PCI_GNT#0</td> <td>SPI_CS#1</td> <td>Boot Location</td> </tr> <tr> <td>0</td> <td>1</td> <td>SPI(Default)</td> </tr> </table>	PCI_GNT#0	SPI_CS#1	Boot Location	0	1	SPI(Default)	GNT0# R344 *1K_4
PCI_GNT#0	SPI_CS#1	Boot Location								
0	1	SPI(Default)								
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK	<table border="1"> <tr> <td>SPI_CS#1</td> <td>0</td> <td>PCI</td> </tr> <tr> <td>1</td> <td>1</td> <td>LPC</td> </tr> </table>	SPI_CS#1	0	PCI	1	1	LPC	SPI_CS1# R340
SPI_CS#1	0	PCI								
1	1	LPC								



PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD20	INTA#	OZ601T





D3A:(1/31) ASP issue:when IAMT is not implemented, ICH9M SMBus and SMLink should be connected together to support slave mode  
Connect SMLINK0 to SMBCLK and SMLINK1 to SMBDATA (Add R474,R475 for debug use)

A1A:(9/29) no support IAMT, remove SMB\_CLK\_ME,SMB\_DATA\_ME

<3> SYS\_RST#  
<6> PM\_SYNC#  
<2> PM\_STPCPU#  
<2> PM\_STPCPU#  
<27,32> CLKRUN#  
<21,23,32> PCIE\_WAKE#  
<27,32> SERIRQ  
<3,18> THERM\_ALERT#

Rev:B ,support Intel low power ECR solution  
OC Fin need PU  
Rev: B new ADD, CR\_WAKE#

<25> PCSPK  
<6> MCH\_ICH\_SYNC#  
<12> ICH\_TP3

<35> VR\_PWRGD\_CK410#

SATAxTOP pins if unused require 8.2k to 10k pull-up to Vcc3.3 or 8.2k to 10k pull-down to ground

DELAY\_VR\_PWRGOOD need PU 2k to +3V. 22k PU at power side

Checklist ver0.8  
If integrated LAN is not used LAN\_RST# tie it to GND.No serial R from RSMRST#  
If Intel LAN is used with Wake On LAN, tie LAN\_RST# to RSMRST# and NC 8pin

CL\_PWR0K must not assert after PWR0K asserts for IAMT.  
CL\_PWR0K to the IB and SB should be connected to existing PWR0K inputs on the IB and SB on a platform with no IAMT

Checklist ver0.8  
The ICH9M Controller Link 1 VREF circuit is required only if Intel IAMT is to be supported.

VREF1 ChB connect to +3V\_S5  
Checklist connect to +3V\_S52 follow

Z52 Default not support IAMT. So this interface follow ChB/Checklist PU only

ChB INTEL FAB (GE,TF)  
\*Add RSMRST# isolation (important!!! See rev22 Santa Rosa MoM)\*  
\*default stuff for Tenah(Interposer) chipset  
Z52 Intel FAB suggestion to add for to protect R2C/0805 data from corruption when system encounters an abnormal power down sequence

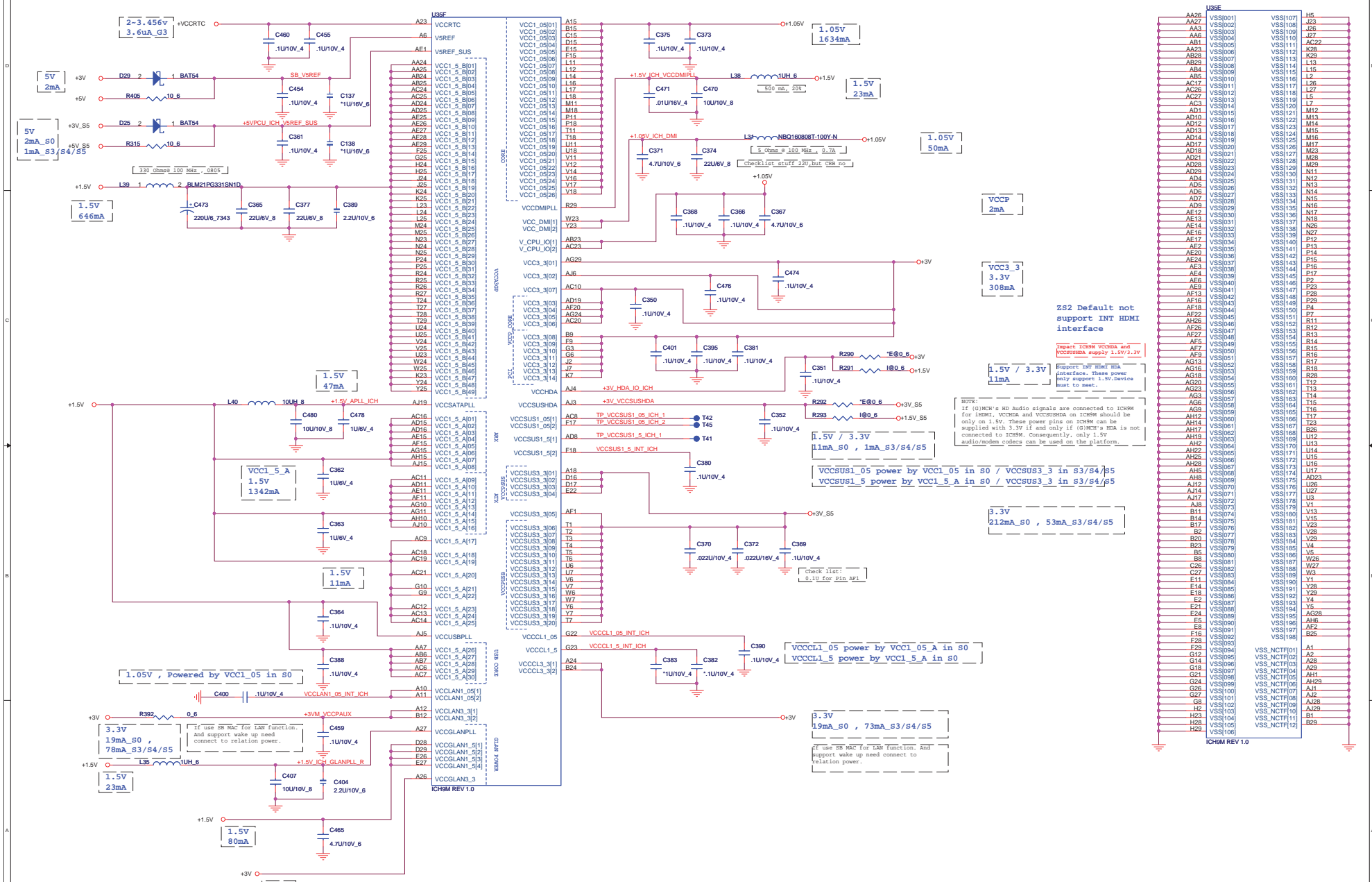
### South Bridge Strap Pin (3/3)

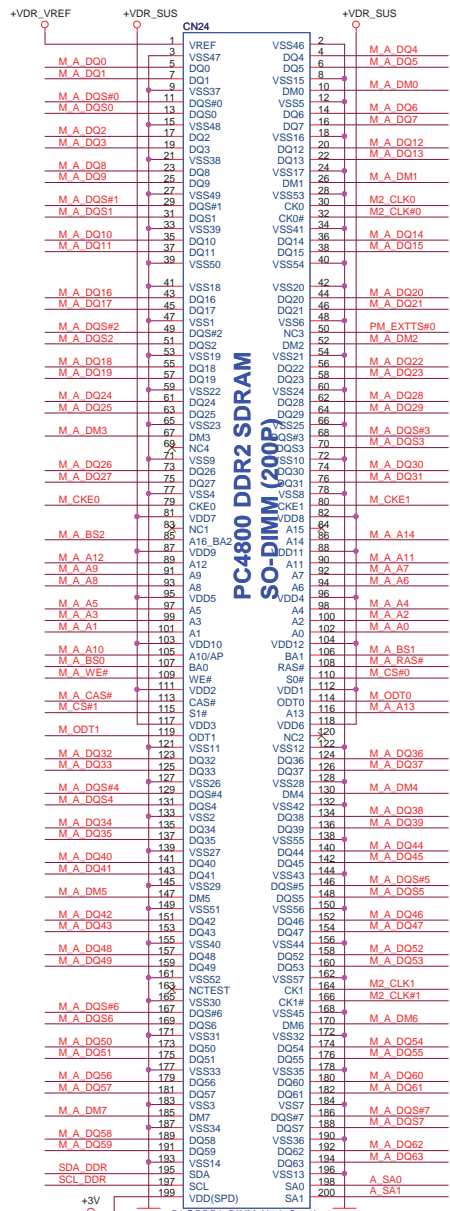
Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode	PCSPK R346 *1K_4 +3V
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL R400 *1K_4

Board ID	ID3	ID2	ID1	ID0
ZY2	0	0	0	0
ZY6	0	0	1	0
ZY2 LOW COST	0	0	0	1
ZY6 LOW COST	0	0	1	1
ZY2 eMachine	0	1	0	0
ZY6 eMachine	0	1	1	0

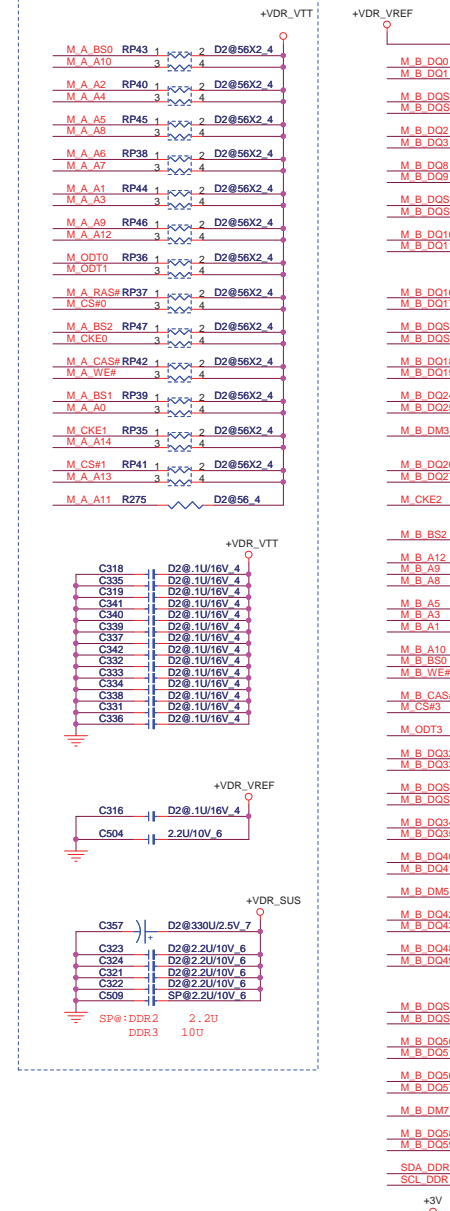
**Quanta Computer Inc.**  
PROJECT : ZY2 & ZY6

Size: Document Number: ICH9M GPIO Rev: 1A  
Date: Thursday, August 28, 2008 Sheet: 14 of 40

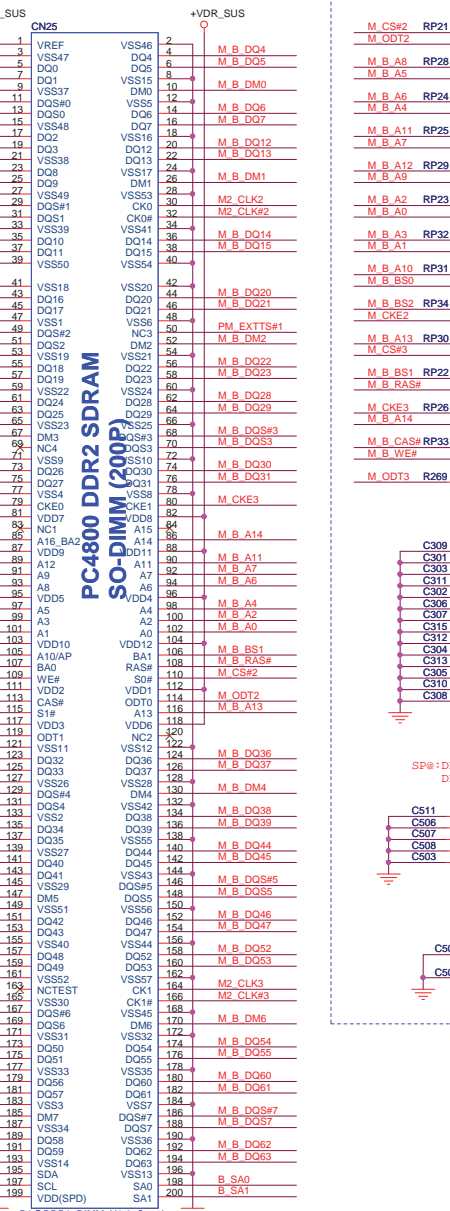




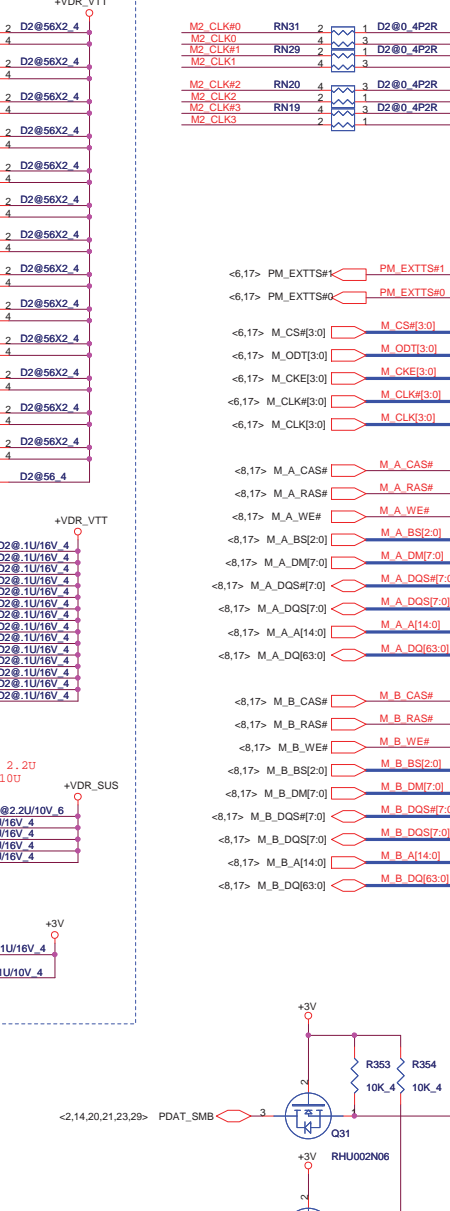
**PC4800 DDR2 SDRAM  
SO-DIMM (200P)**



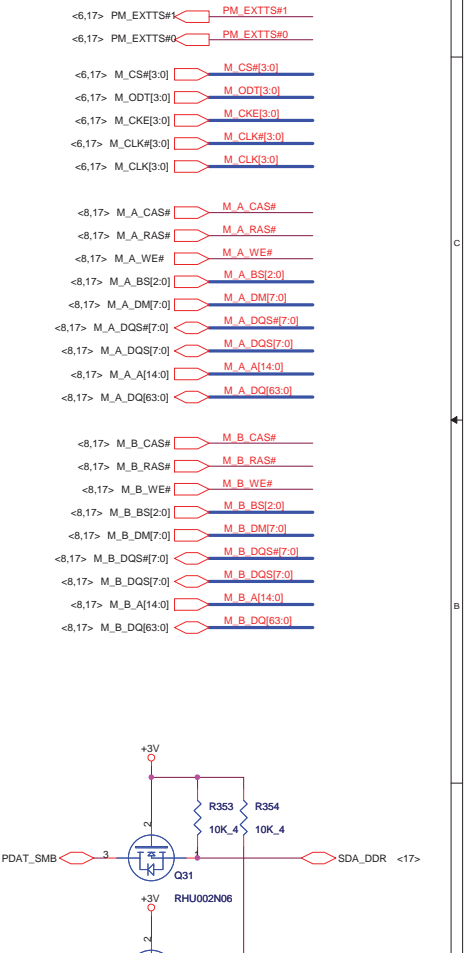
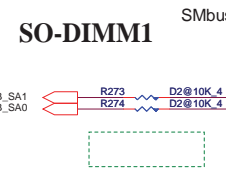
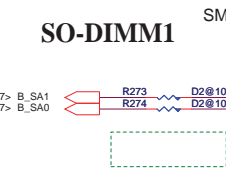
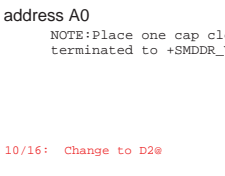
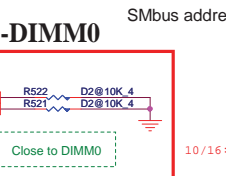
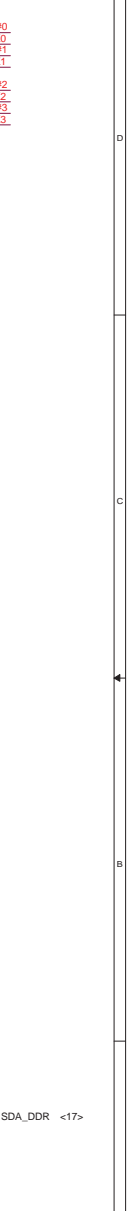
**PC4800 DDR2 SDRAM  
SO-DIMM (200P)**



**PC4800 DDR2 SDRAM  
SO-DIMM (200P)**



**PC4800 DDR2 SDRAM  
SO-DIMM (200P)**

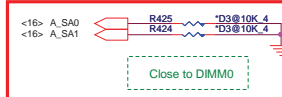
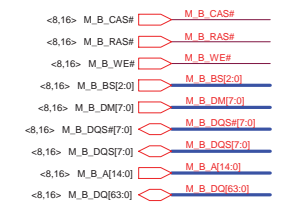
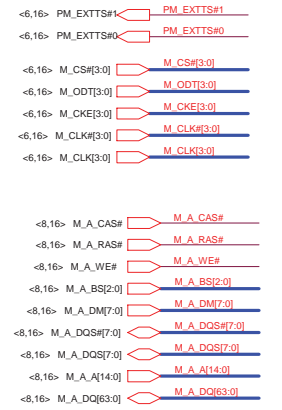
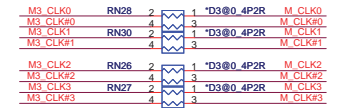


**Quanta Computer Inc.**  
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	DDR11 SO-DIMM	1A
Date: Thursday, August 28, 2008	Sheet 16 of 40	



FOR DDR3

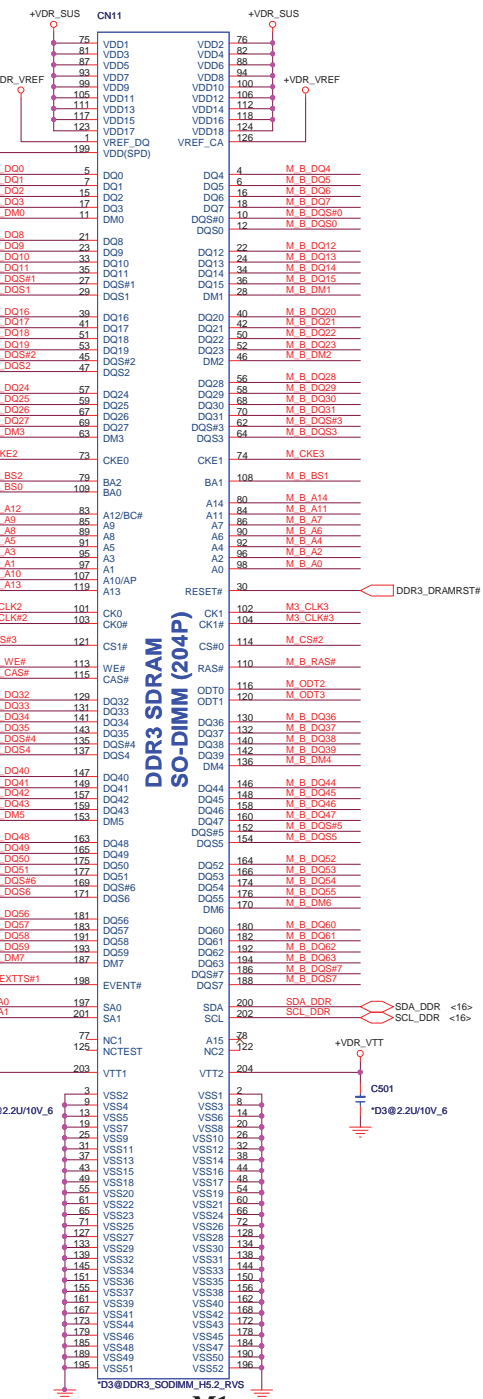
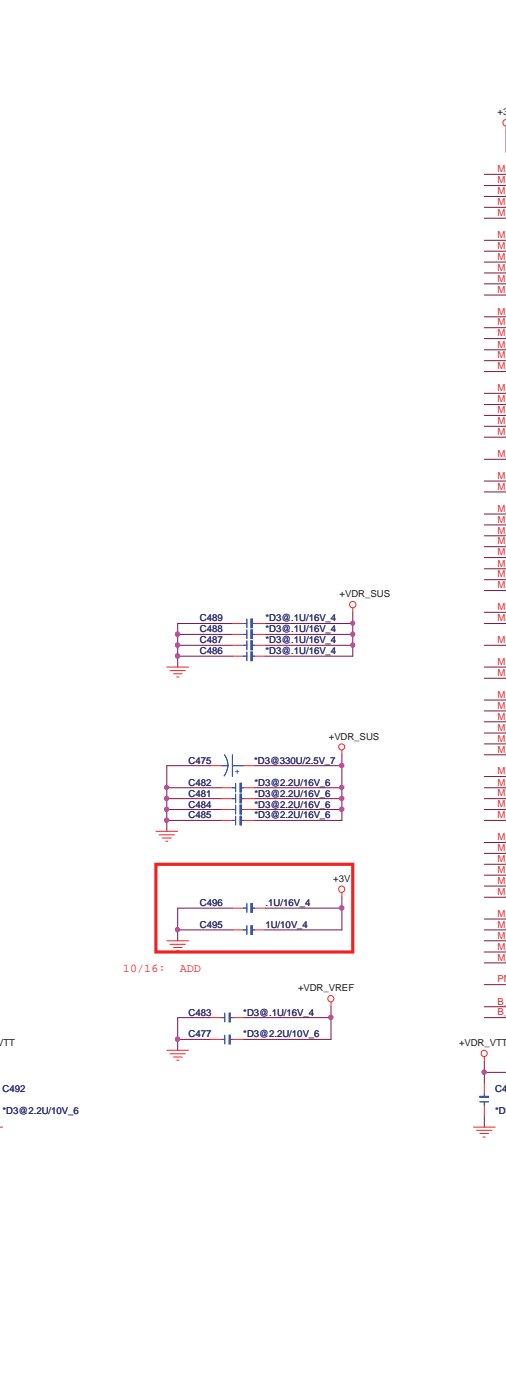
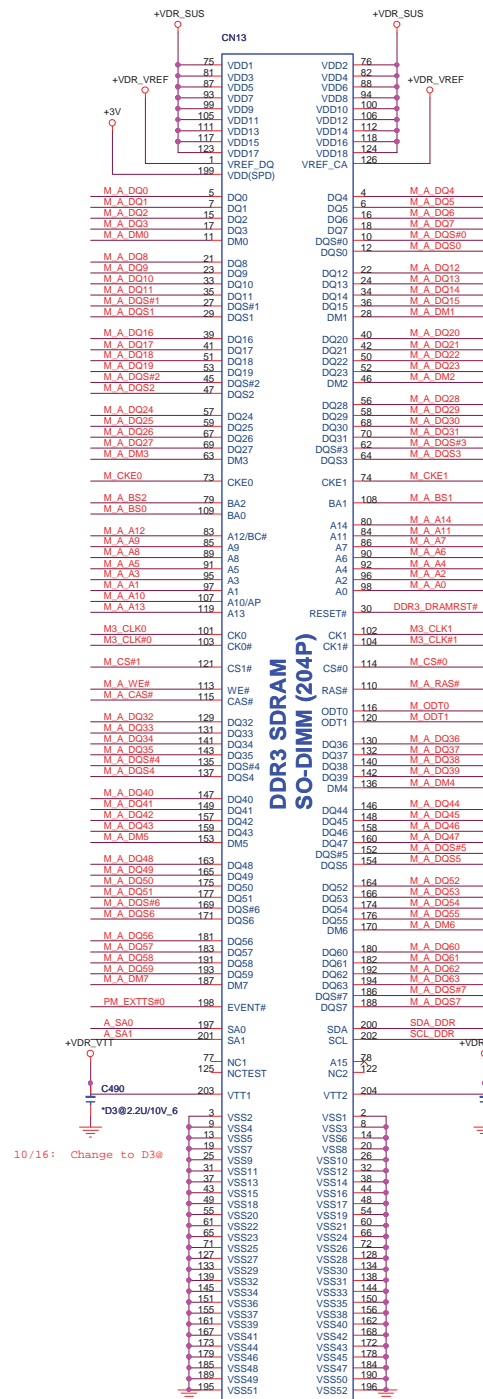


**Quanta Computer Inc.**

**PROJECT : ZY2 & ZY6**

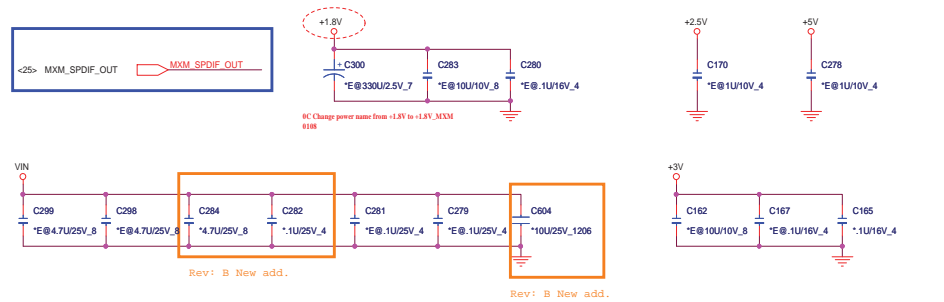
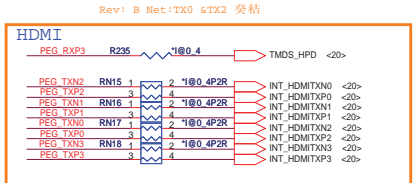
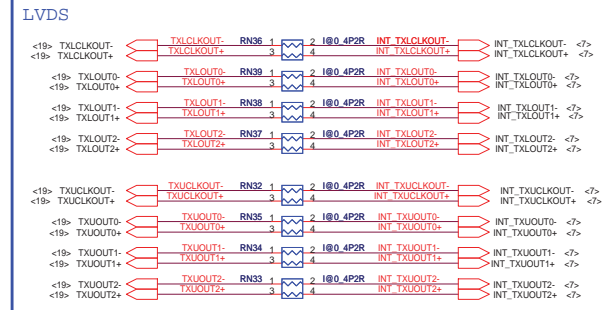
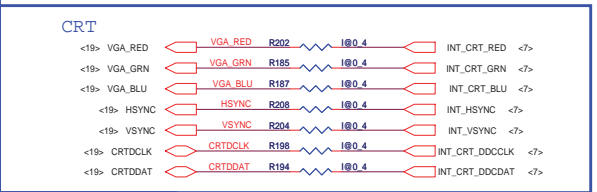
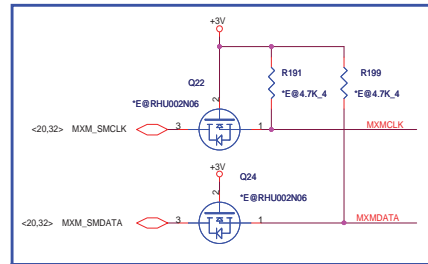
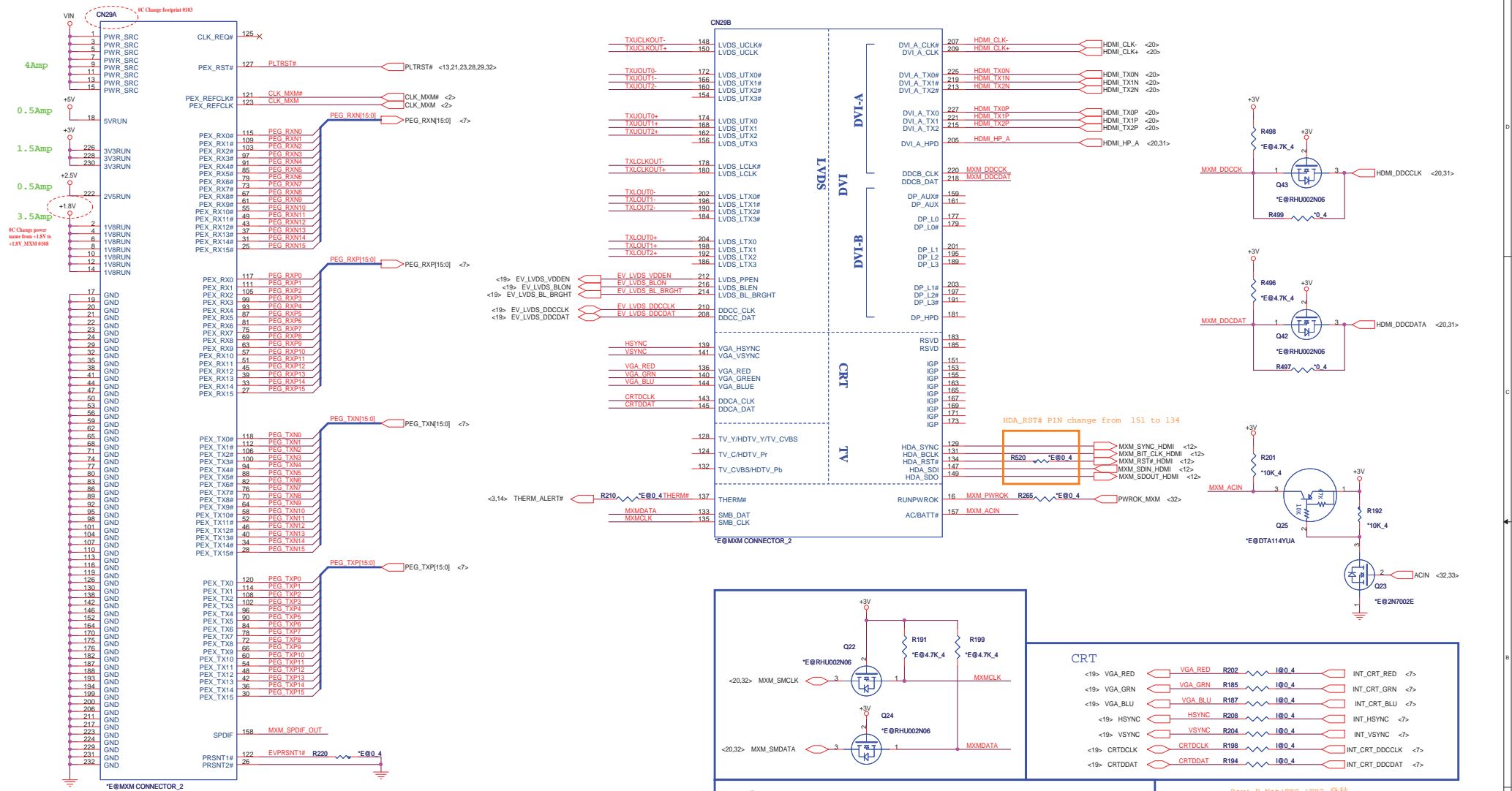
Size: Document Number: **DDR3 SO-DIMM** Rev: 1A

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SO-DIMM0 SMbus address A0

SO-DIMM1 SMbus address A2



Rev: B Net:TX0 & TX2 突结

**HDMI**

PEG\_RXP3 R235 10K.4 TMSD\_HPD <20>

PEG\_TXN0 RN15 2 100.4P2R INT\_HDMITXN0 <20>

PEG\_TXN1 RN16 3 4 INT\_HDMITXN1 <20>

PEG\_TXN2 RN17 3 4 INT\_HDMITXN2 <20>

PEG\_TXP0 RN18 2 100.4P2R INT\_HDMITXP0 <20>

PEG\_TXP1 RN19 3 4 INT\_HDMITXP1 <20>

PEG\_TXP2 RN20 3 4 INT\_HDMITXP2 <20>

PEG\_TXP3 RN21 3 4 INT\_HDMITXP3 <20>

Rev: B New add.

Rev: B New add.

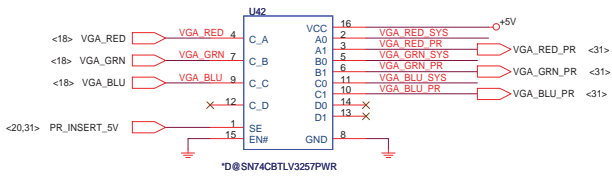
**Quanta Computer Inc.**  
PROJECT : ZY2 & ZY6

Size Document Number  
MXM

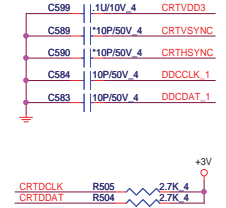
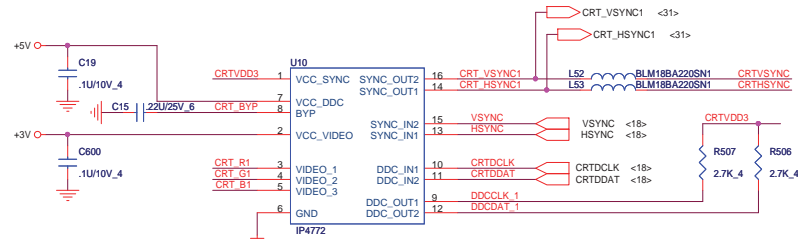
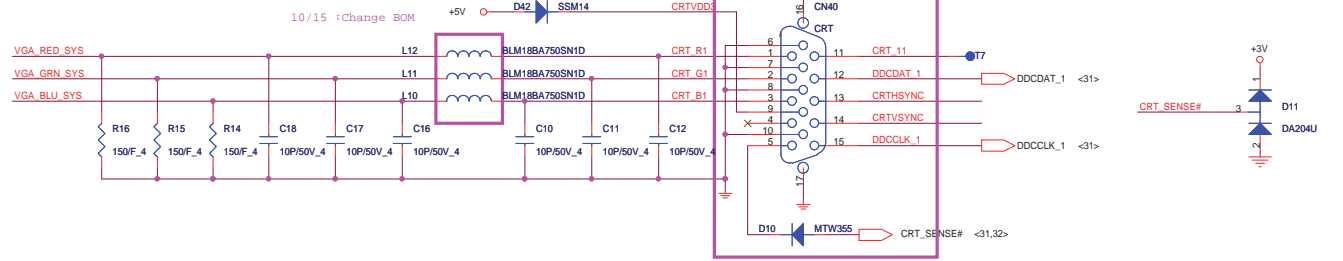
Date: Thursday, August 28, 2008 Sheet 18 of 40 Rev 1A

CRT Select

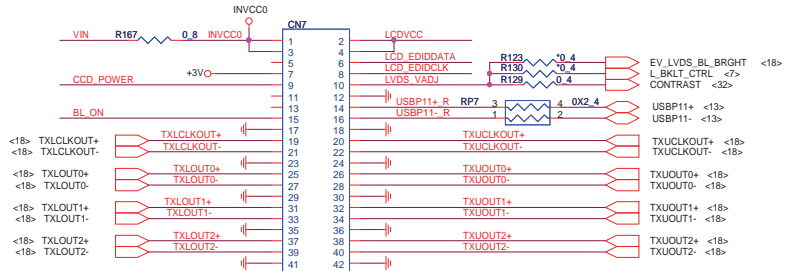
CRT SWITCH



CRT CONNECTOR AND ESD

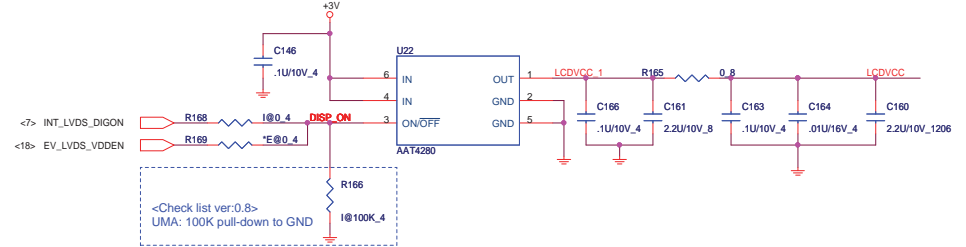
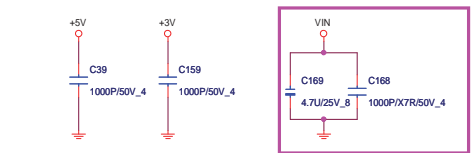
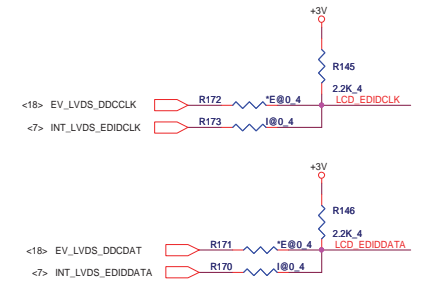


LVDS

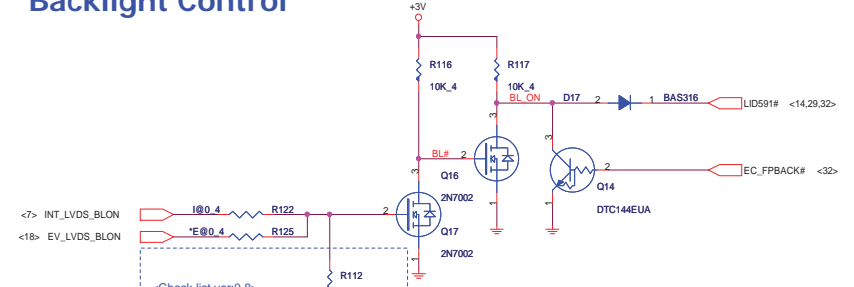


Rev:B, Modify QCI P/N.

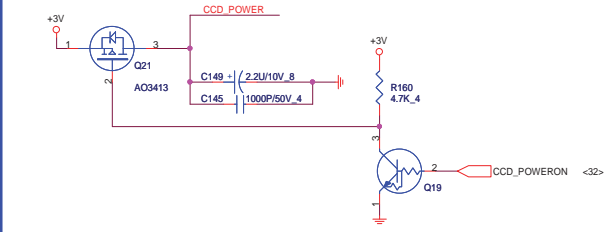
Rev:C, Change to 4.7U 0805



Backlight Control



CAMERA MODULE CONNECTOR

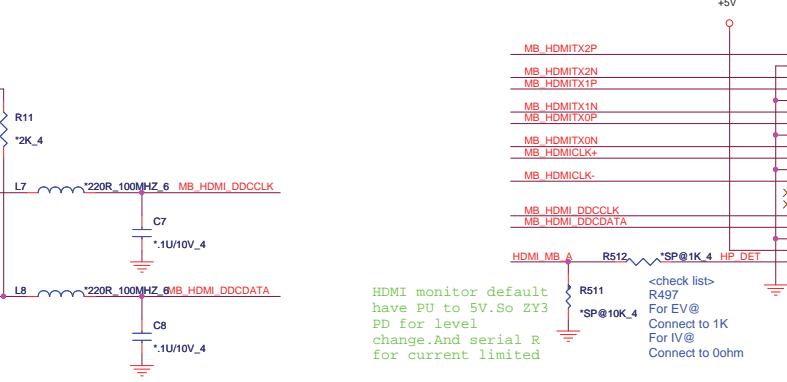
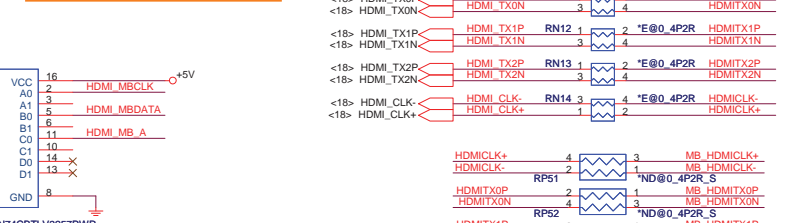
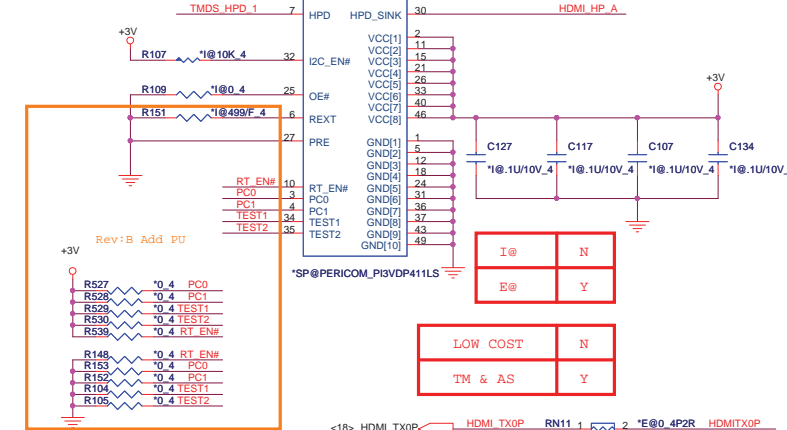
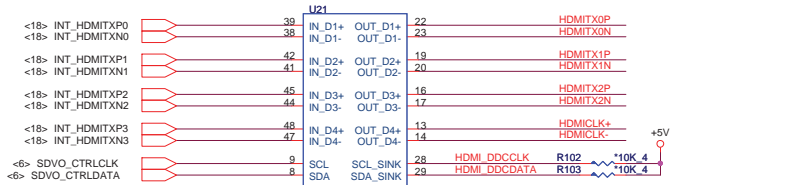


**Quanta Computer Inc.**  
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	CRT	1A
Date:	Thursday, August 28, 2008	Sheet 19 of 40

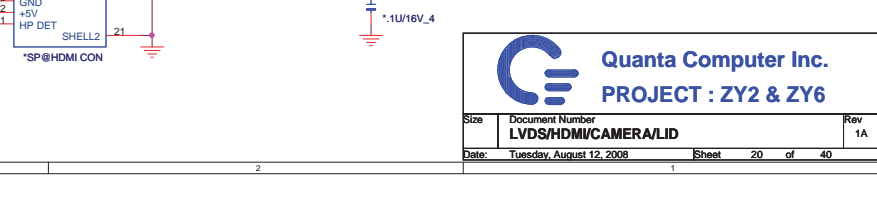
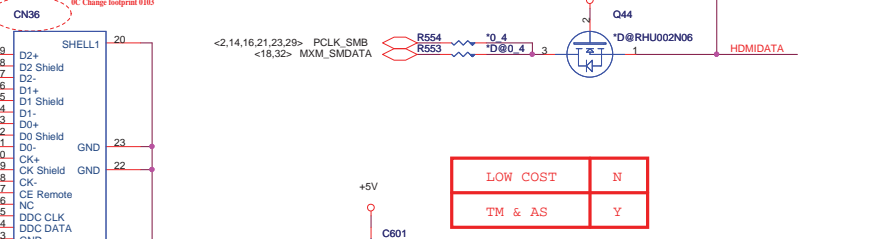
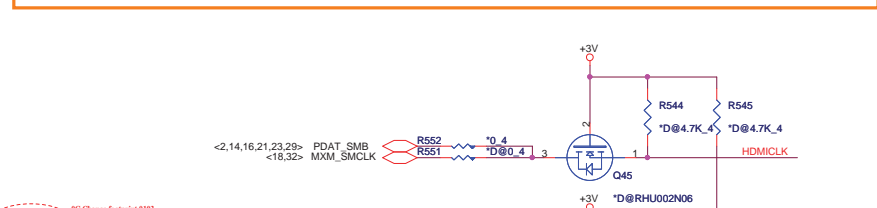
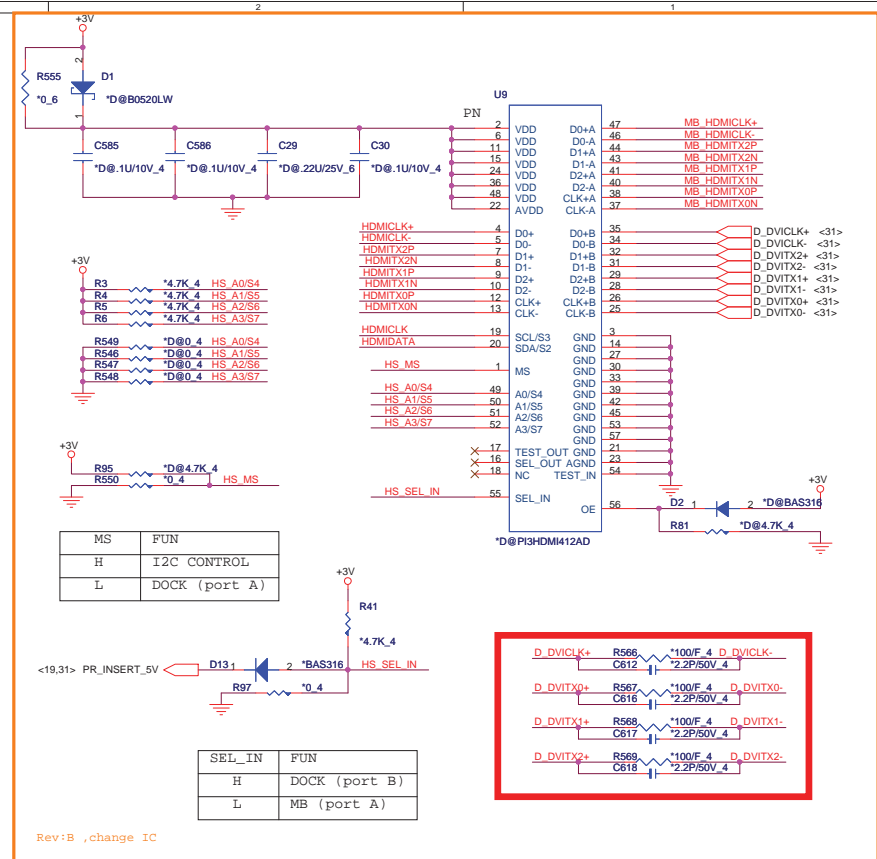
# DVI-I CONNECTOR (DVI-D)

QCI P/N	
PI3VDP411LS	ALP411LS000
Ch7318A	AL007318000
PS8101	



NV suggestion near HDMI connector

HDMI monitor default have PU to 5V. So ZY3 PD for level change. And serial R for current limited



Rev: B , change IC


I@	N
E@	Y

LOW COST	N
TM & AS	Y

SEL_IN	FUN
H	DOCK (port B)
L	MB (port A)

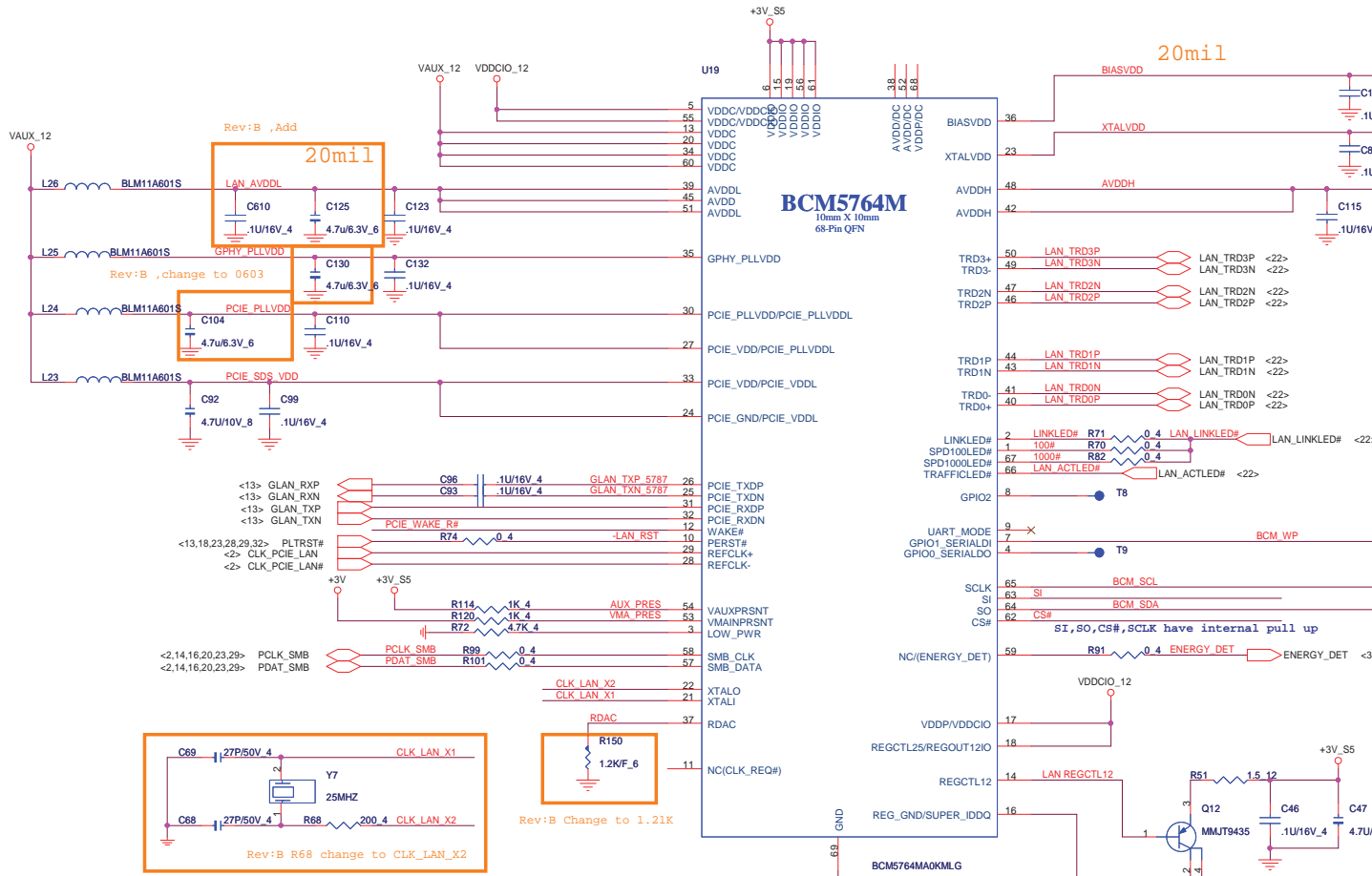
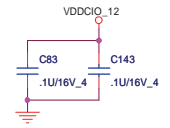
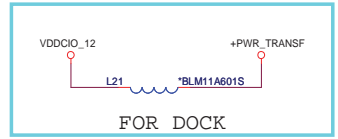
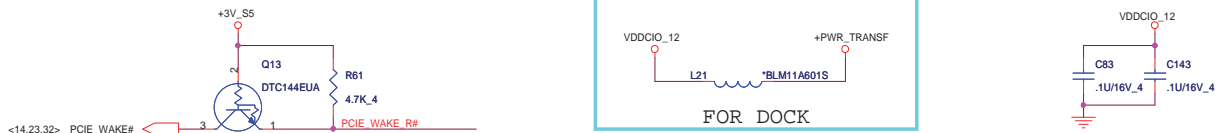
LOW COST	N
TM & AS	Y



**Quanta Computer Inc.**  
PROJECT : ZY2 & ZY6

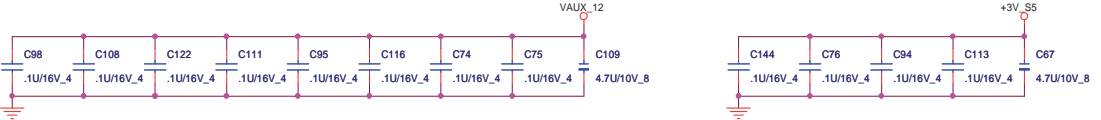
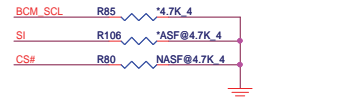
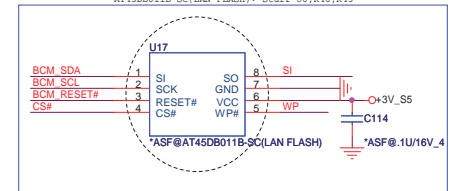
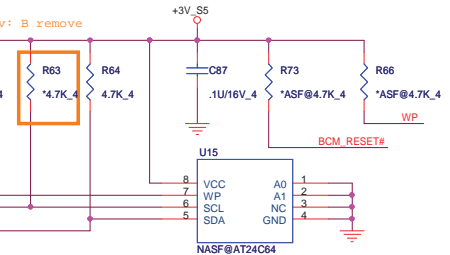
Size	Document Number	Rev
	LVDS/HDMI/CAMERA/LID	1A
Date:	Tuesday, August 12, 2008	Sheet 20 of 40

# LAN



EEPROM Strapping

	SO	SI	CS#	SCLK
24c64	1	1	0	1
AT45DB011B	1	0	1	1

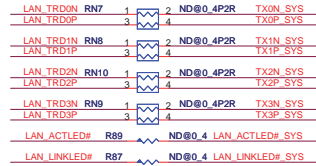
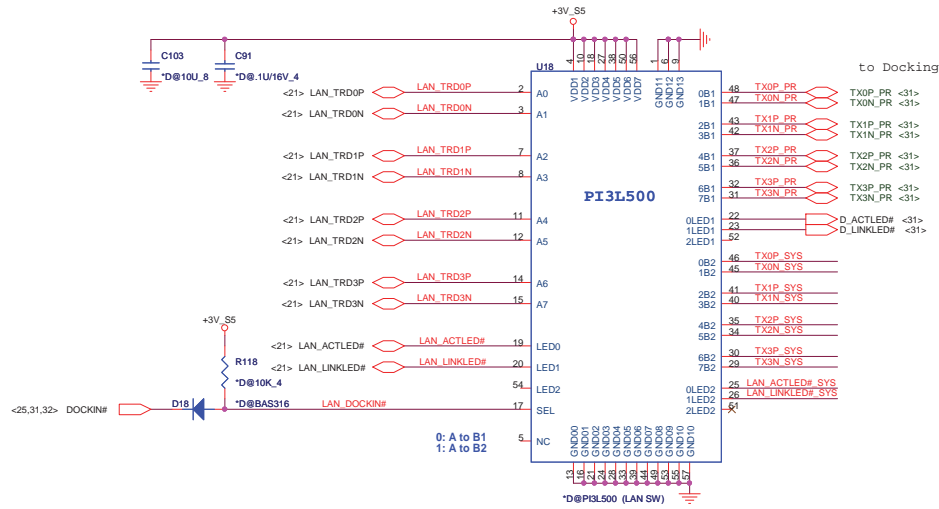


Low is normal, H->Turn Off 1.2V,  
H(>0.7V <2.5V)->L will internal  
reset

**Quanta Computer Inc.**  
**PROJECT : ZY2 & ZY6**

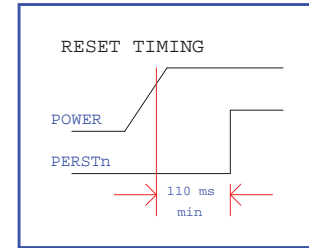
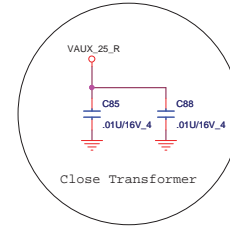
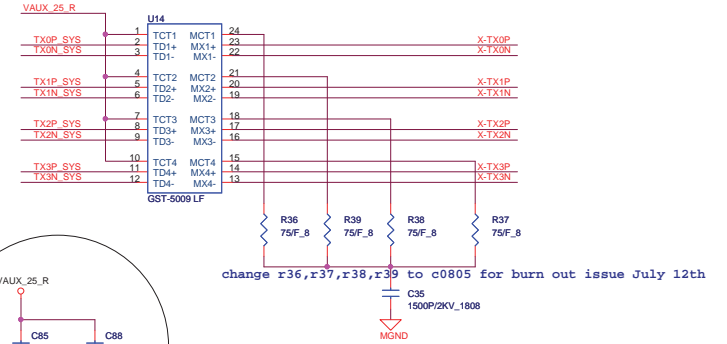
Size	Document Number	Rev
Date:	<b>BCM5787 &amp; 5764 LAN</b>	1A
Thursday, August 28, 2008	Sheet 21 of 40	

# LAN SWITCH

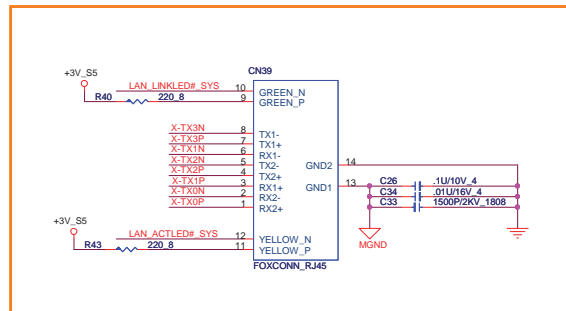


# Transformer

Source 1: DELTA LFE9249 DB0ZR1LAN11  
Source 2: Bothand GST5009 DBKN1NLAN03

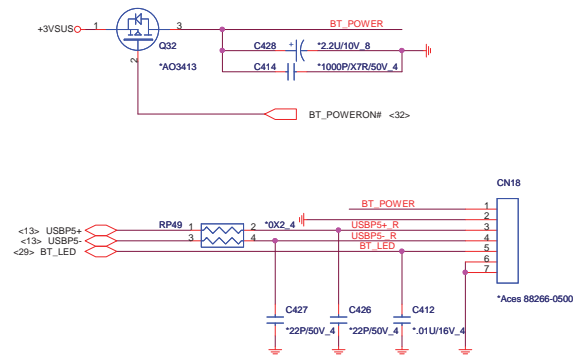


# RJ45-11



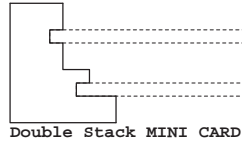
9/29: change footprint  
11/27: change footprint  
11/28: R43 & R40 Change to 0805  
1/31: Rev: C change PIN define about 9,10,11 & 12

# BLUETOOTH MODULE CONNECTOR



Quanta Computer Inc.  
PROJECT : ZY2 & ZY6

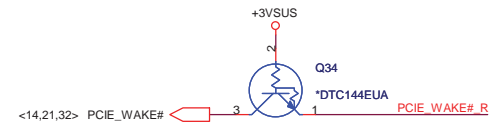
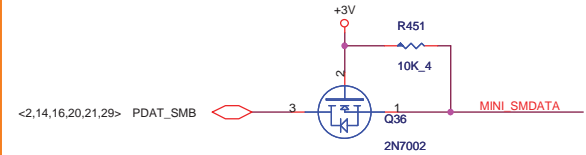
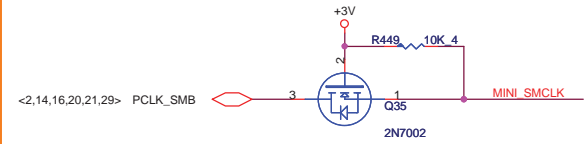
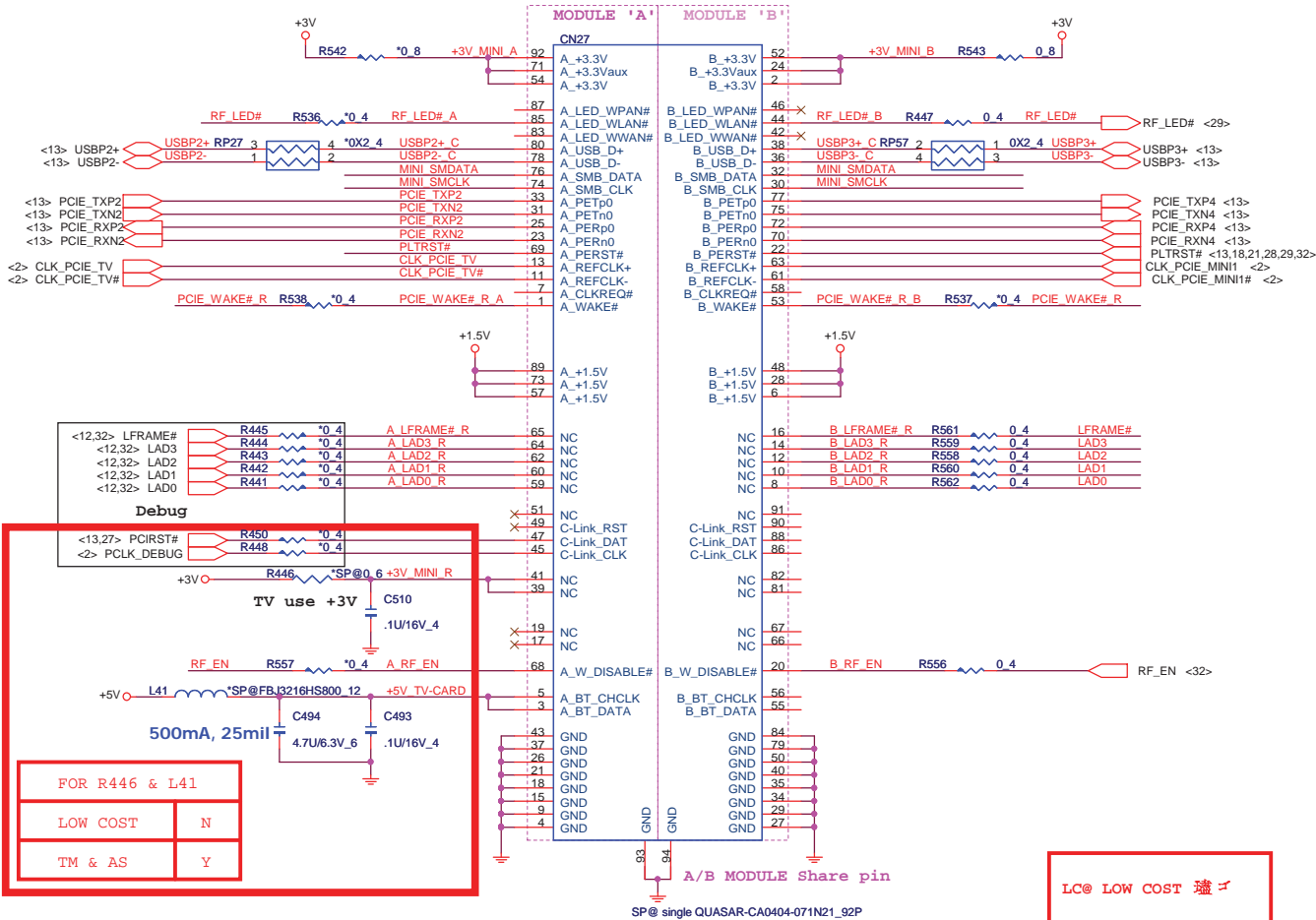
# MINI-CARD



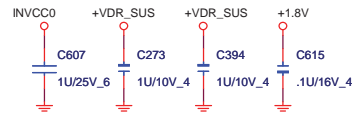
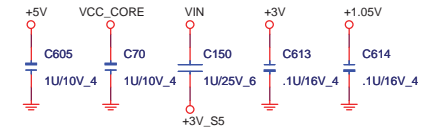
MODULE 'A' TV card

MODULE 'B' Wireless card

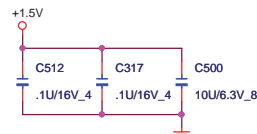
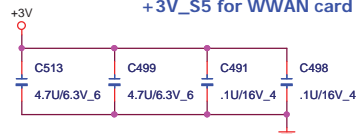
Rev:B PIN36,38 Add USB3  
PIN69 Add R536  
PIN1, 53 Add R537 & R538



## FOR EMI



+3V\_S5 for WWAN card is 2.75A



**Quanta Computer Inc.**  
**PROJECT : ZY2 & ZY6**

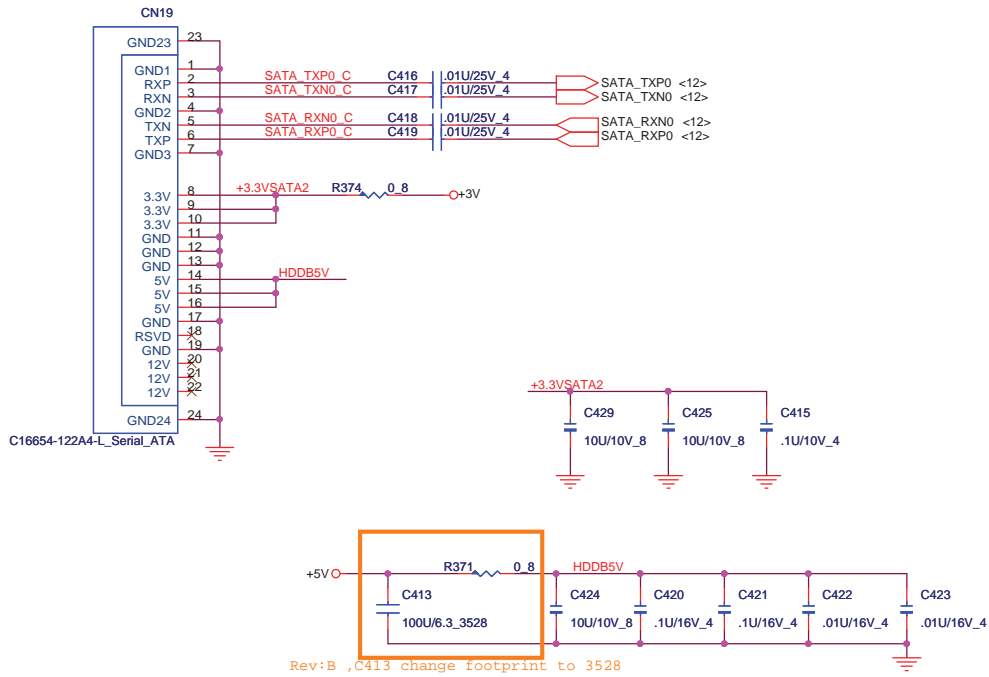
Size Document Number  
**MINI PCI-E card/TV/TPM** Rev 1A

Date: Tuesday, August 12, 2008 Sheet 23 of 40

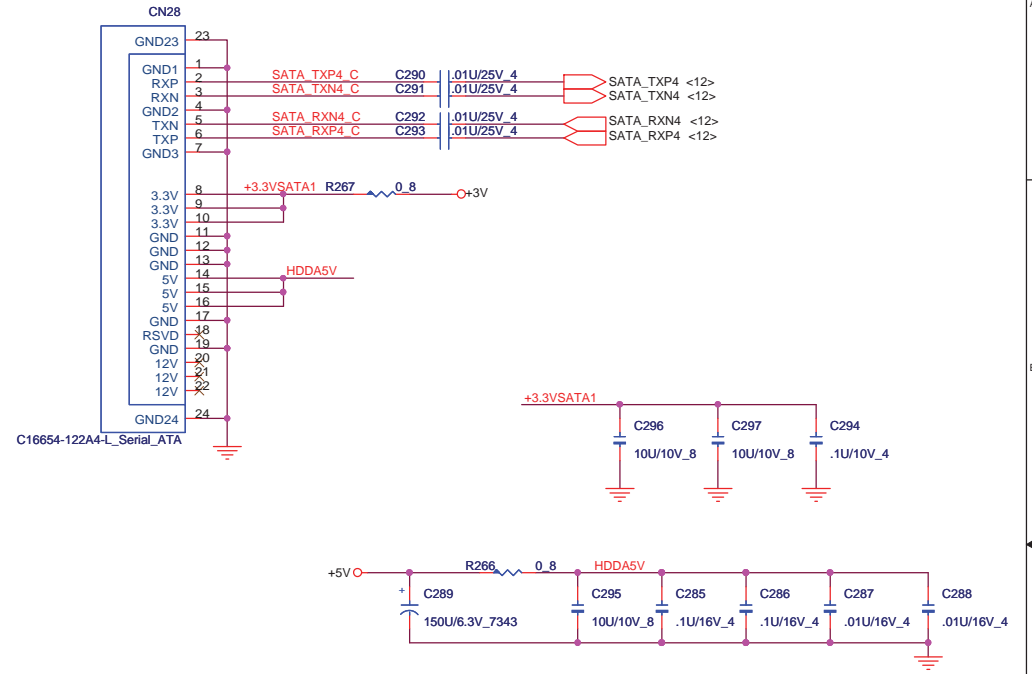
# SATA HDD

11/8 REV:B Conn. 奔奕粘 CN28 & CN19

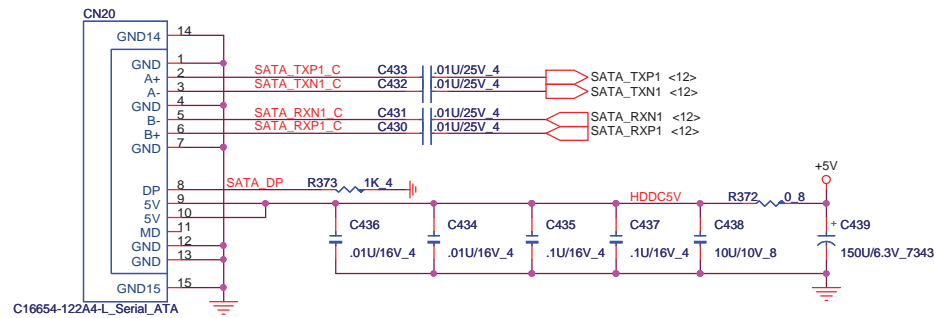
Main



# 2ND SATA HDD



# ODD (SATA)

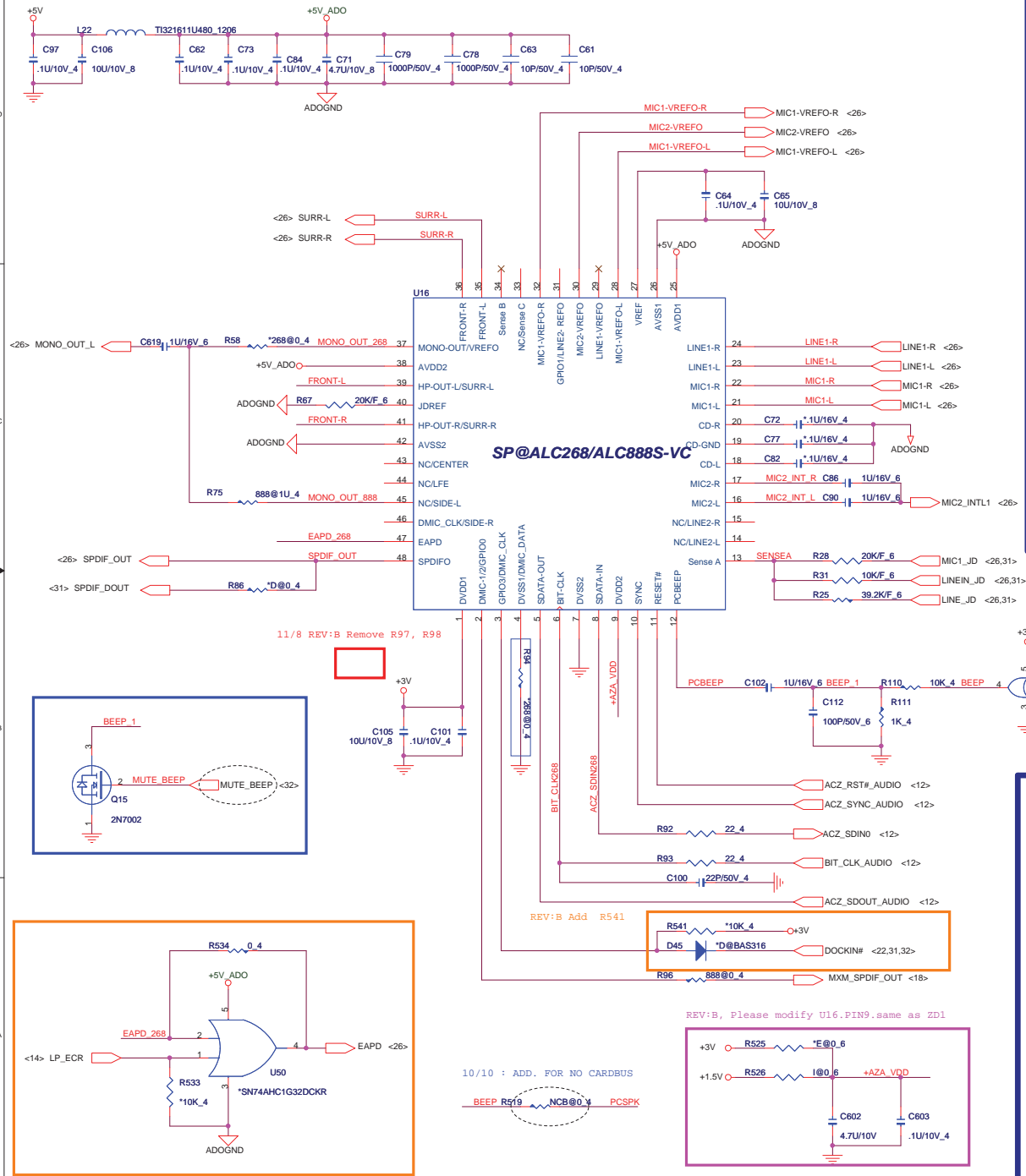


**Quanta Computer Inc.**  
PROJECT : ZY2 & ZY6

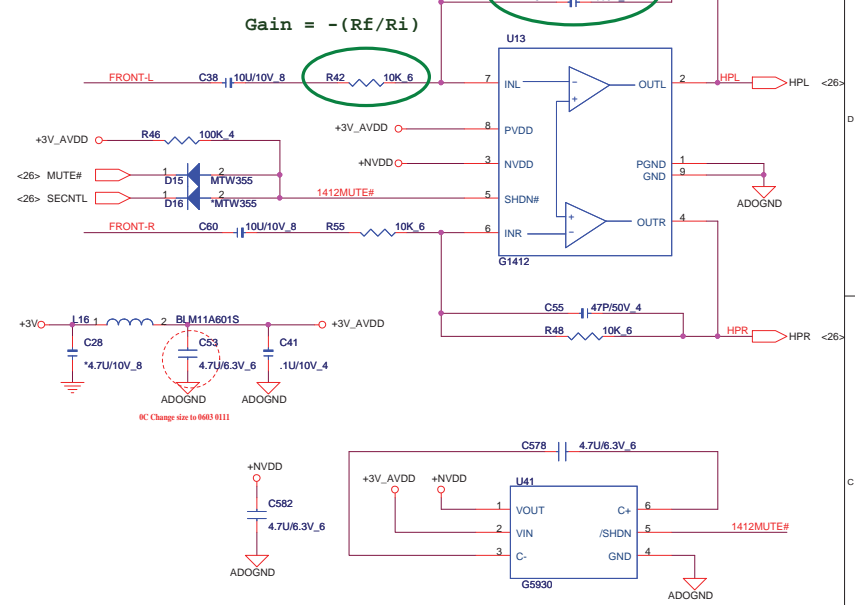
Size	Document Number	Rev
	<b>SATA-HDD &amp; ODD</b>	1A
Date:	Wednesday, August 13, 2008	Sheet 24 of 40



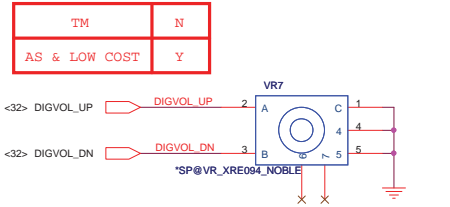
**CODEC (ALC268)**



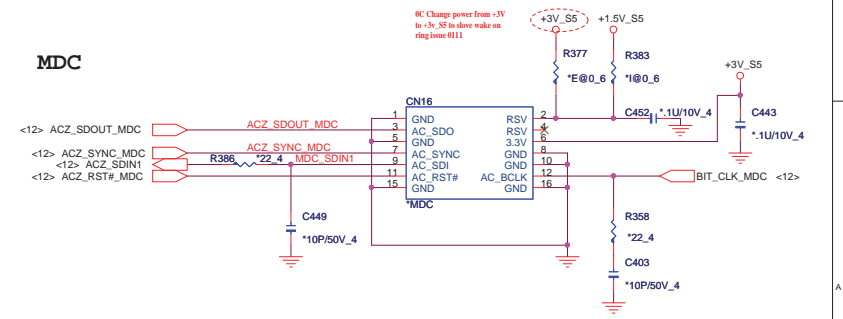
**LINE OUT Amplifier**



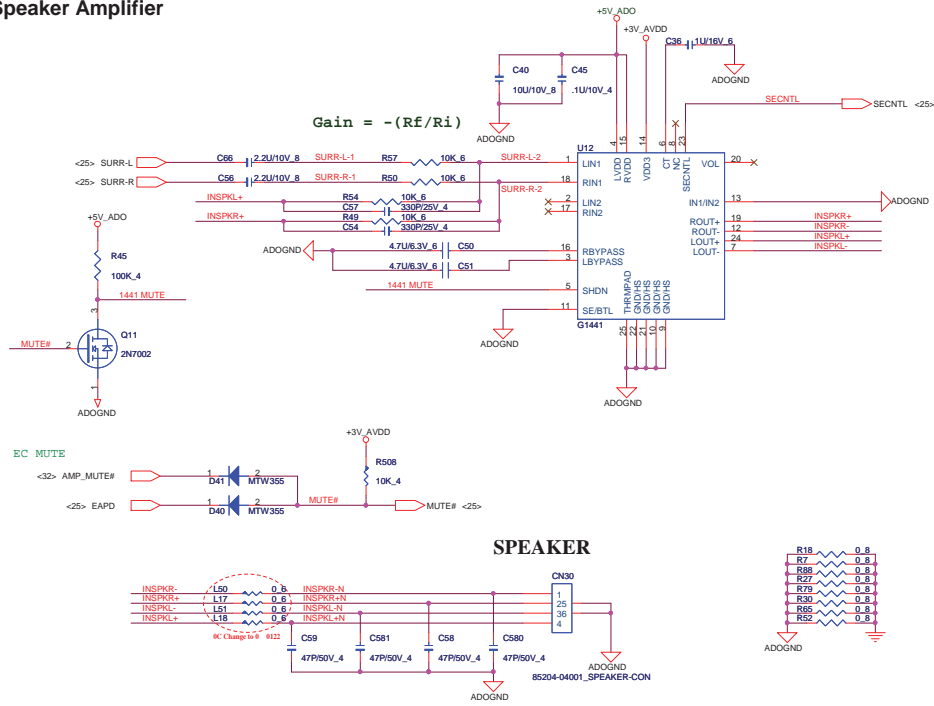
**VR**



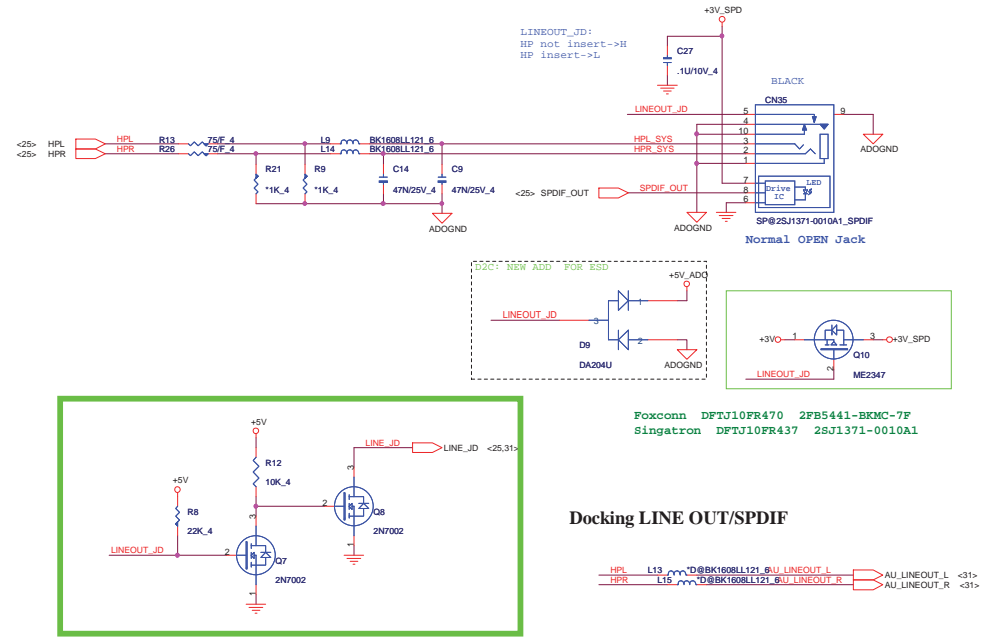
**MDC**



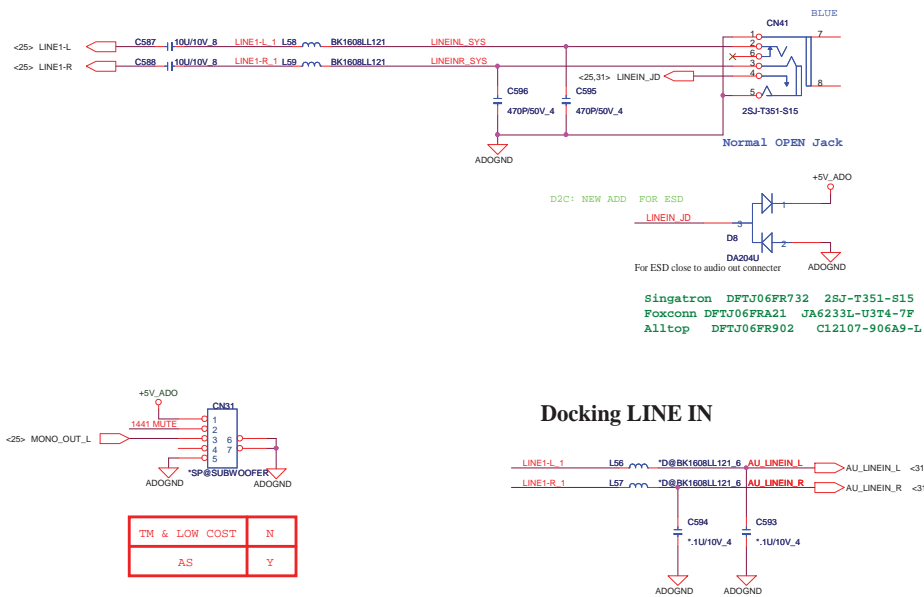
# Speaker Amplifier



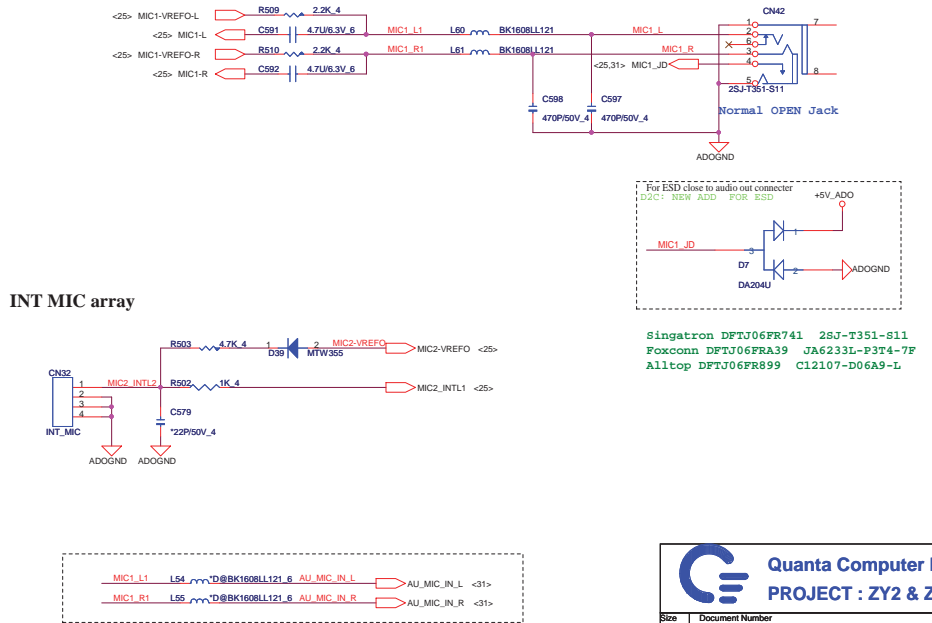
# SYSTEM LINE OUT/SPDIF



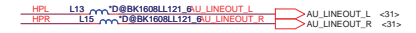
# SYSTEM LINE IN/SUBWOOFER



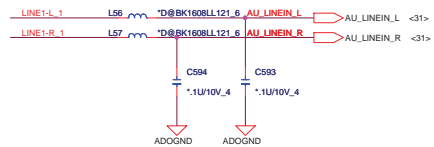
# MIC



## Docking LINE OUT/SPDIF



## Docking LINE IN



IM & LOW COST	N
AS	Y

### NOTE: IDSEL SELECTION!

THIS DEVICE UTILIZES A "SELECTABLE IDSEL" SCHEME. IDSEL CAN BE CONNECTED INTERNALLY TO ONE OF THREE PCI AD LINES OR EXTERNAL IDSEL SIGNAL.

2K TO 47K PULL-UP & PULL-DOWN RESISTORS ARE REQUIRED TO BE CONNECTED TO PINS 123 & 124 TO SELECT ONE OF THE 4 POSSIBLE IDSEL CONNECTIONS. THE TABLE BELOW SHOWS THE 4 POSSIBLE COMBINATIONS.

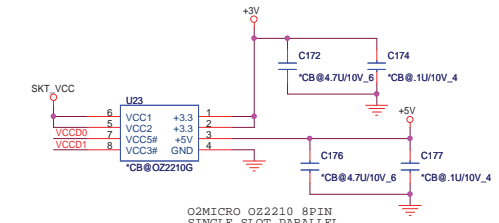
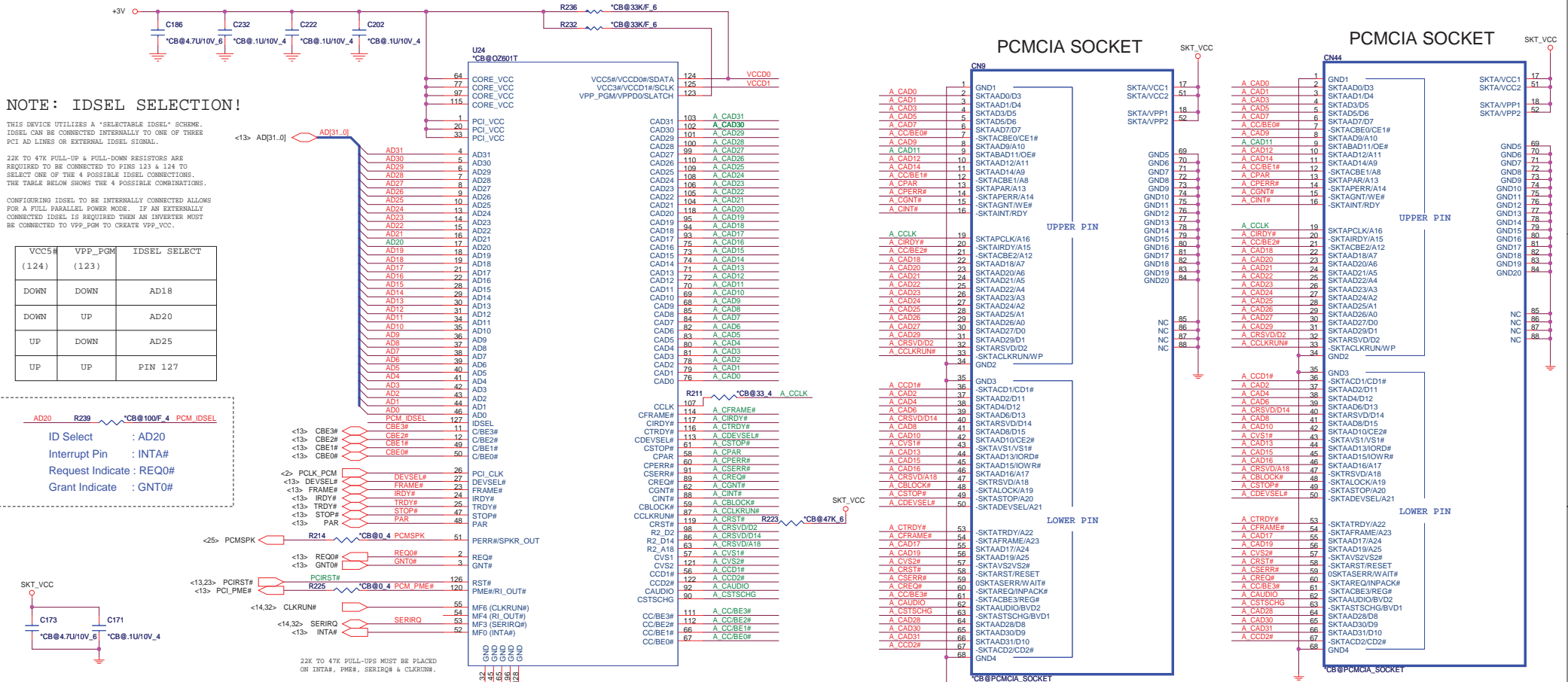
CONFIGURING IDSEL TO BE INTERNALLY CONNECTED ALLOWS FOR A FULL PARALLEL POWER MODE. IF AN EXTERNALLY CONNECTED IDSEL IS REQUIRED THEN AN INVERTER MUST BE CONNECTED TO VPP\_PGM TO CREATE VPP\_VCC.

VCC5# (124)	VPP_PGM (123)	IDSEL SELECT
DOWN	DOWN	AD18
DOWN	UP	AD20
UP	DOWN	AD25
UP	UP	PIN 127

AD20 R239 \*CB@100F.4 PCM IDSEL

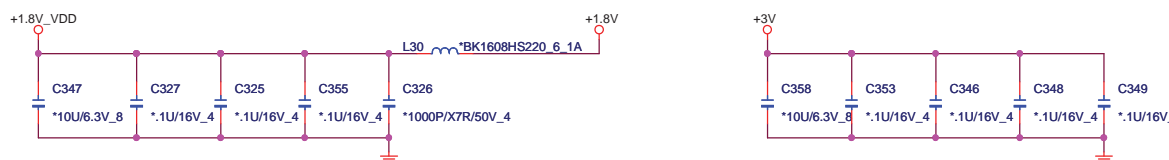
ID Select : AD20  
 Interrupt Pin : INTA#  
 Request Indicate : REQ0#  
 Grant Indicate : GNT0#

IDSEL SELECT POWER-ON-STRAPPING  
 (SEE NOTE & TABLE FOR OPTIONS)

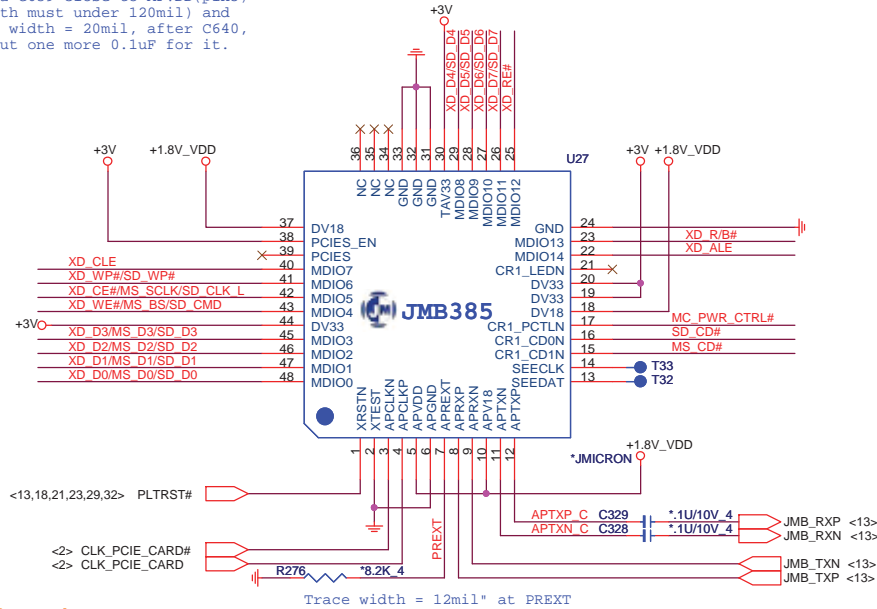


O2MICRO OZ2210 8PIN SINGLE SLOT PARALLEL POWER SWITCH

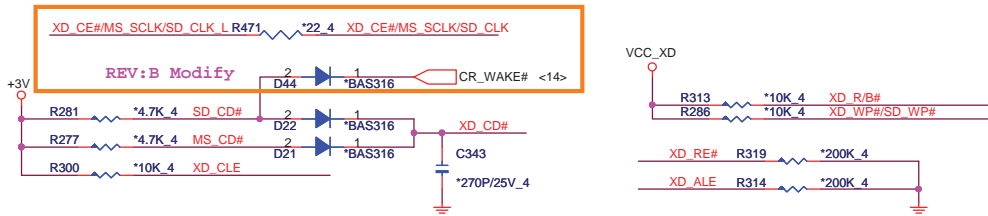
# 7 IN 1 CARD READER



C640 & C639 close to APVDD(pin5)  
(length must under 120mil) and  
trace width = 20mil, after C640,  
pls put one more 0.1uF for it.

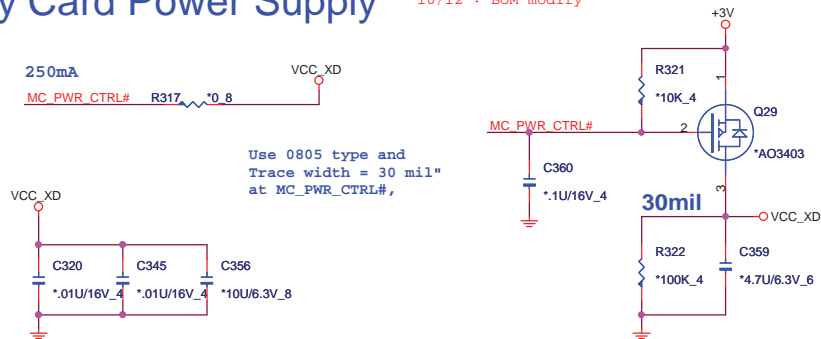


Rev: B Add. for Vendor request

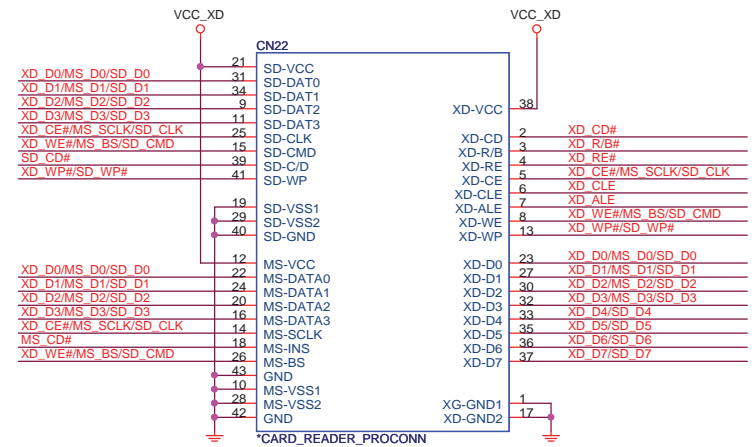
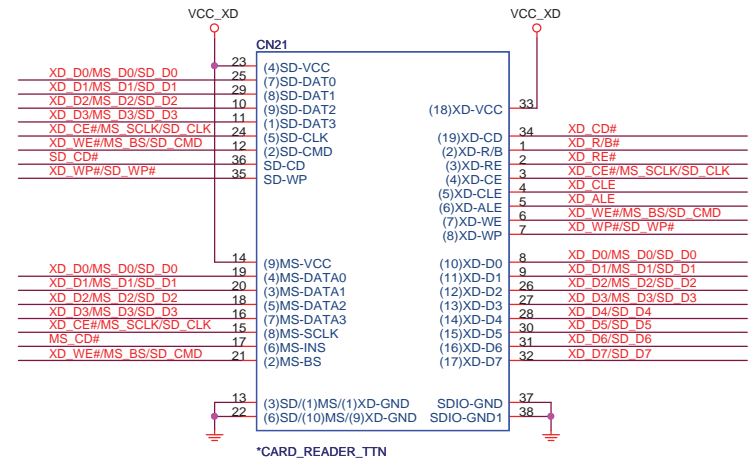



## Memory Card Power Supply

10/12 : BOM modify



Use 0805 type and  
Trace width = 30 mil"  
at MC\_PWR\_CTRL#,

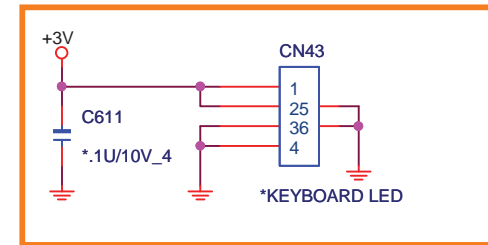
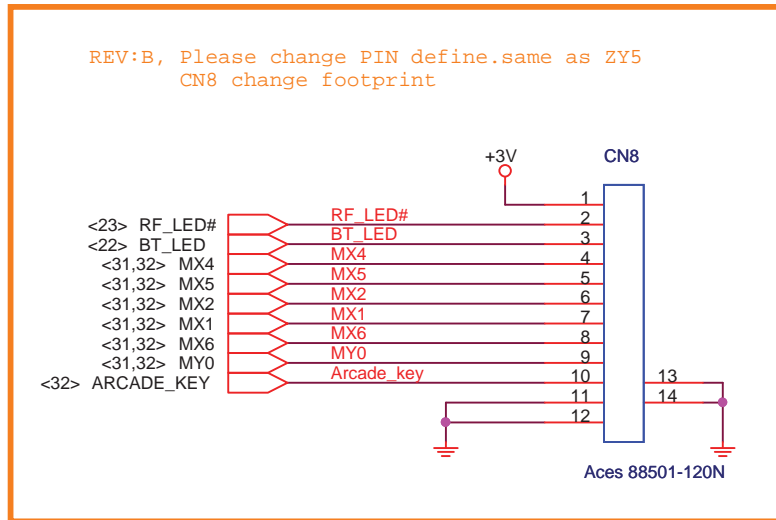
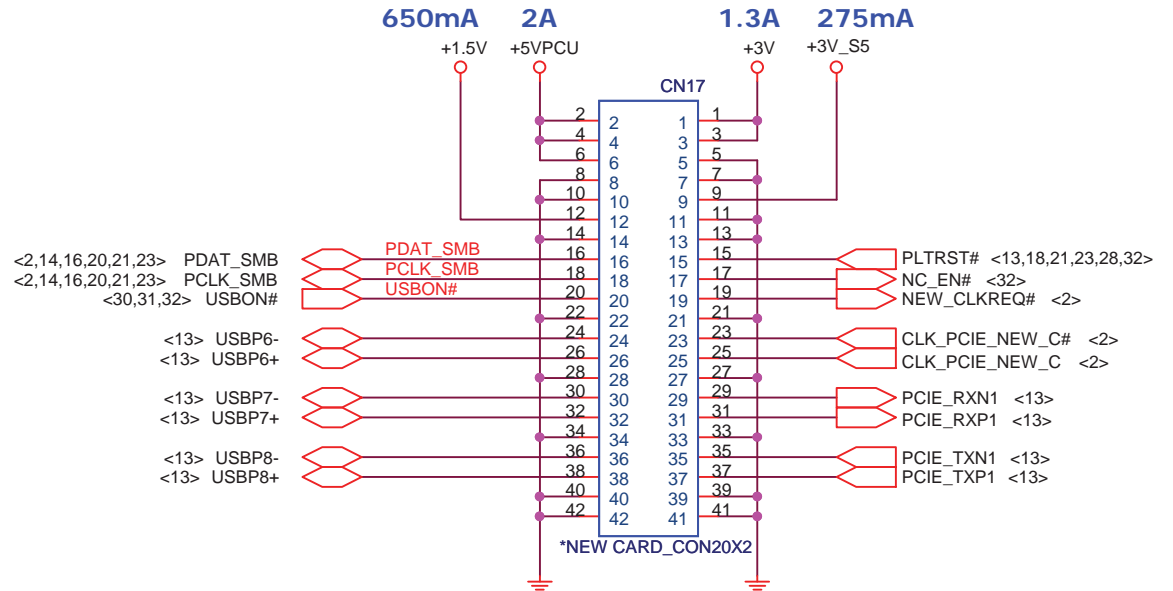
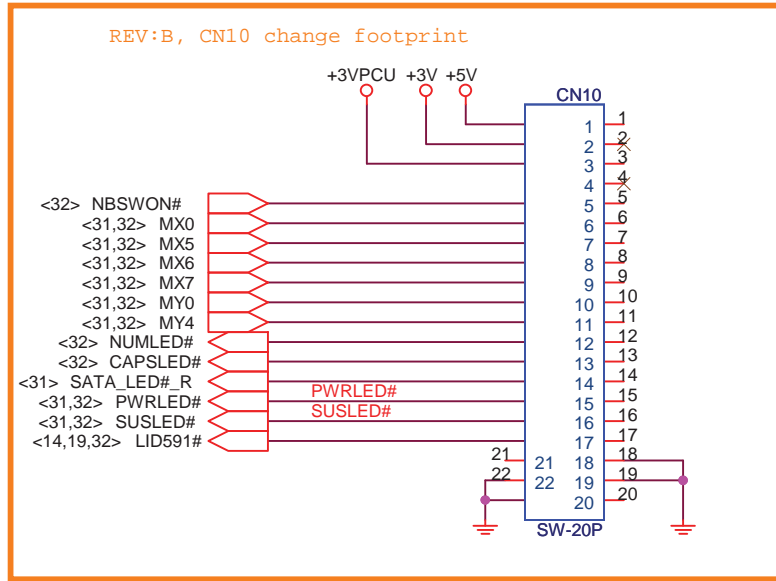




**Quanta Computer Inc.**  
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	<b>CARD READER JMB385</b>	1A
Date:	Thursday, August 28, 2008	Sheet 28 of 40

# To NEW-CARD & EXT. USB



Rev:B Add CN43 For backlight KB

Rev:B Change to 蛾 to ↓PAD  
C255,C234,C221,C199,R217,C198,R183,  
R182,R174,R257,R324,R335,R334,R349,C395

Fncion	Keyboard Matrix
E-KEY	MX0/ MY0
E-Mail	MX1/ MY0
E-WWW	MX2/ MY0
3G/TV	MX3/ MY0
Wireless	MX4/ MY0
BlueTooth	MX5/ MY0
P-KEY	MX6/ MY0
Presentation	MX5/ MY4
Lock	MX6/ MY4
Sync	MX7/ MY4

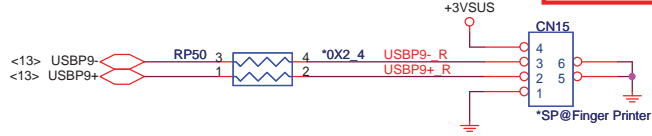
**Quanta Computer Inc.**

**PROJECT : ZY2 & ZY6**

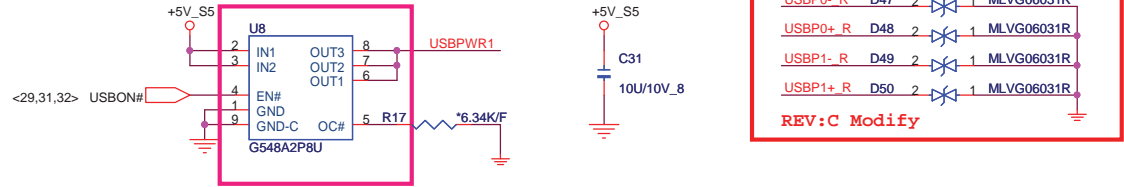
Size	Document Number	Rev
	<b>BTB CONN.</b>	1A
Date:	Tuesday, August 12, 2008	Sheet 29 of 40

# Finger Printer

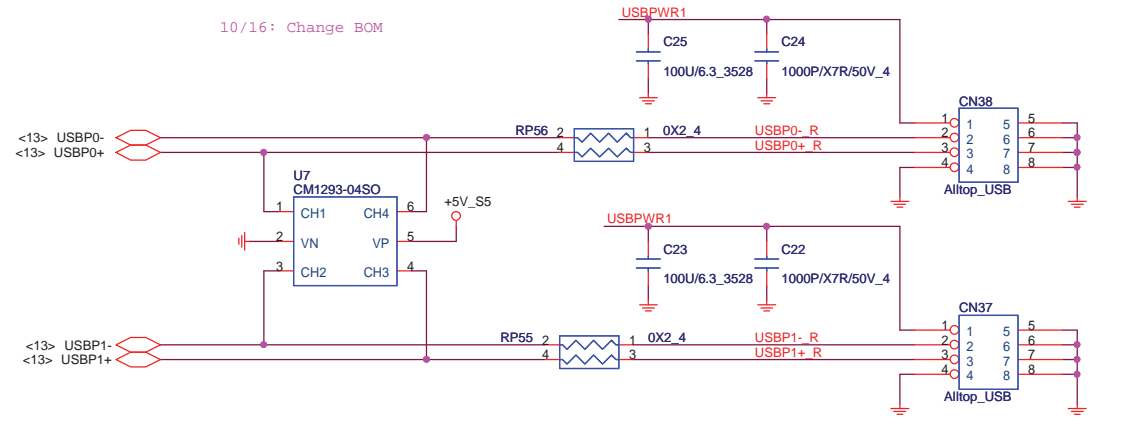
TM & AS	Y
LOW COST	N



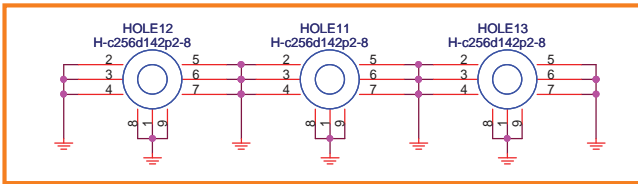
# USB



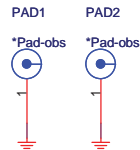
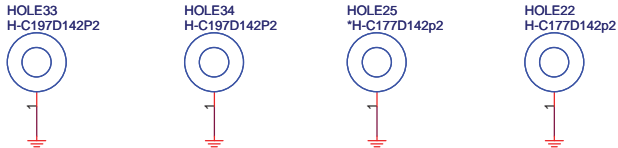
10/16: Change BOM



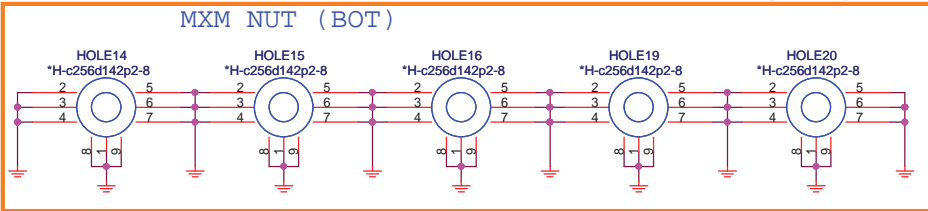
## HOLES CPU NUT (BOT)



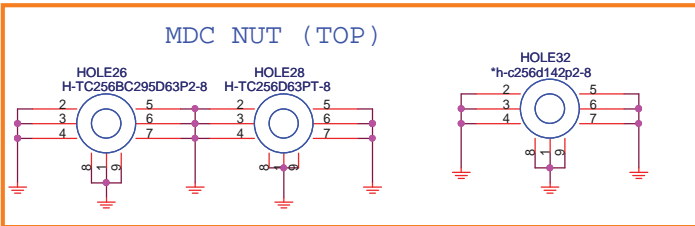
Rev : B Add MINI NUT



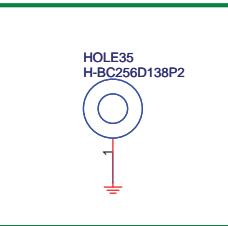
## MXM NUT (BOT)



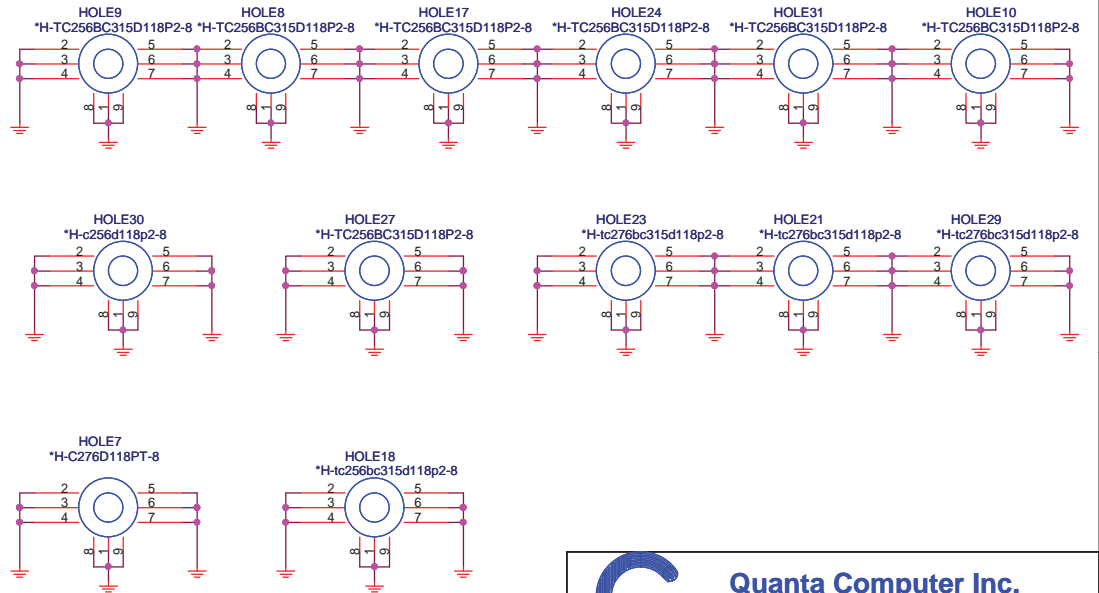
## MDC NUT (TOP)



Rev:B New add HOLE32  
HOLE26 & 28 Change footprint

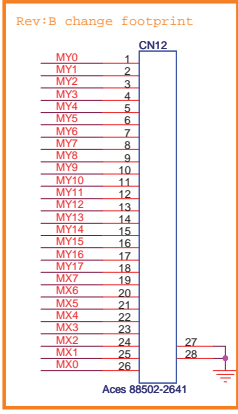
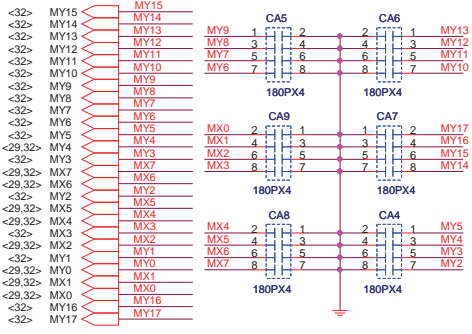


HOLE35 璫穉 BOT

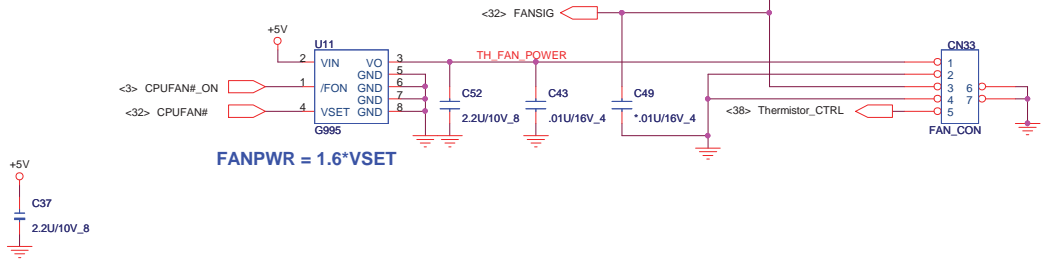


**Quanta Computer Inc.**  
**PROJECT : ZY2 & ZY6**

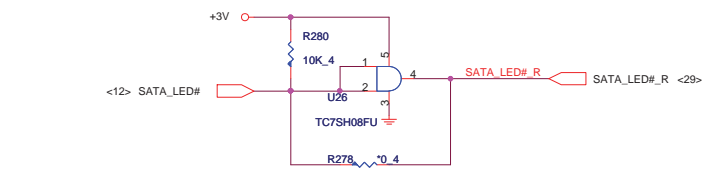
# INT K/B



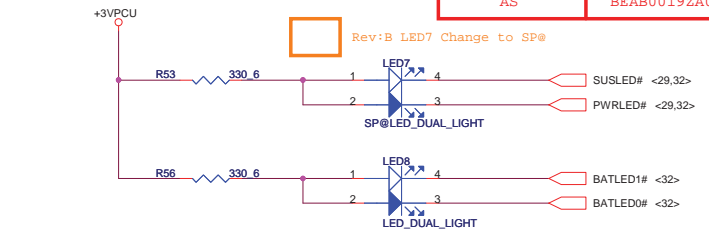
# CPU FAN



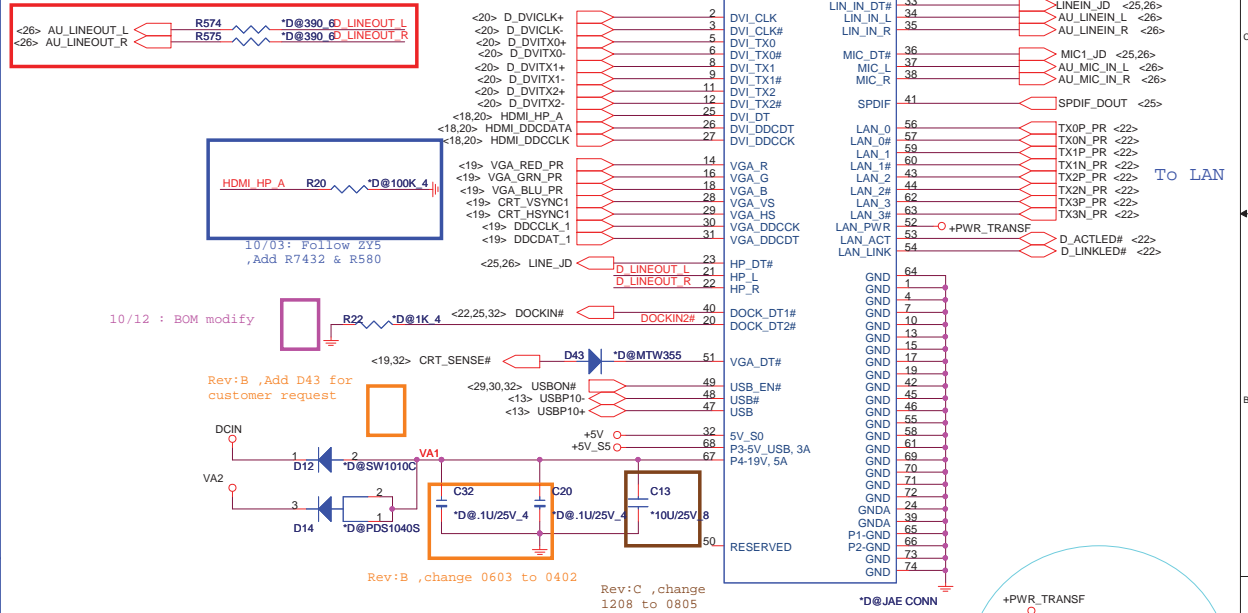
# LED



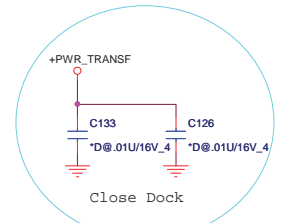
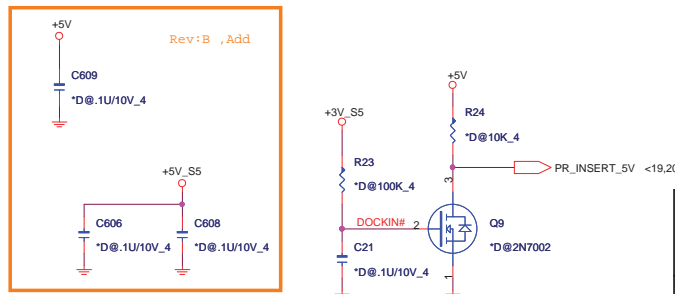
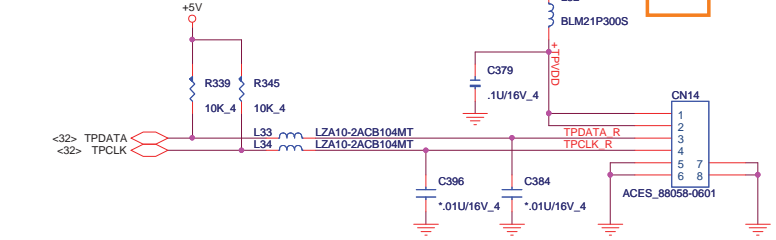
TM & LOW COST	BEGA0017ZA0
AS	BEAB0019ZA0



# CABLE DOCK



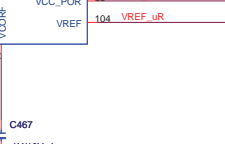
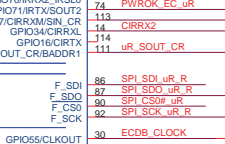
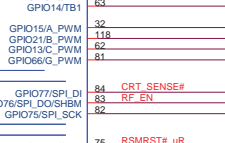
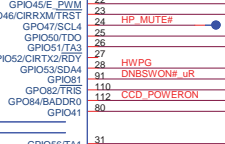
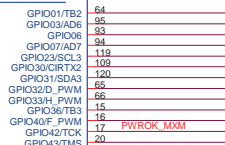
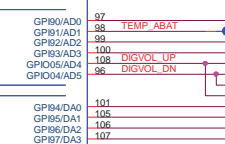
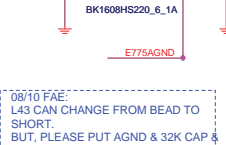
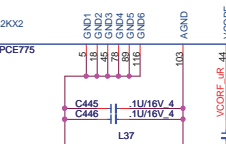
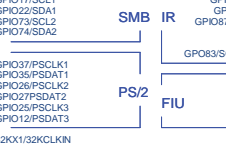
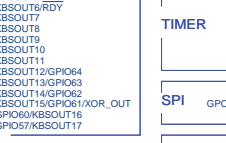
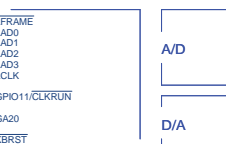
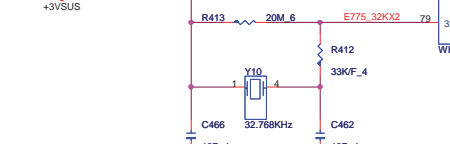
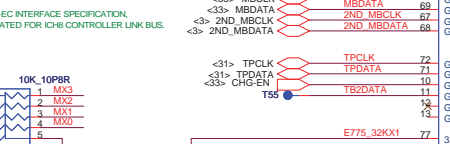
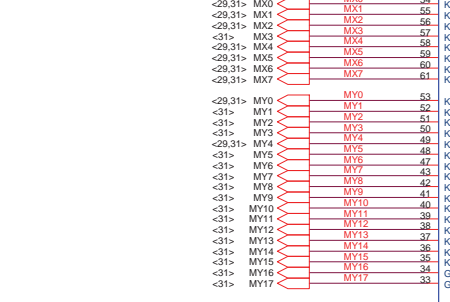
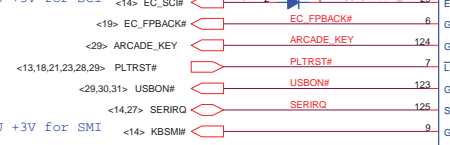
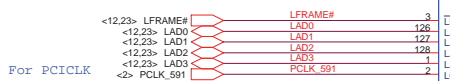
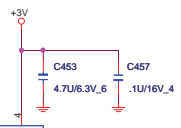
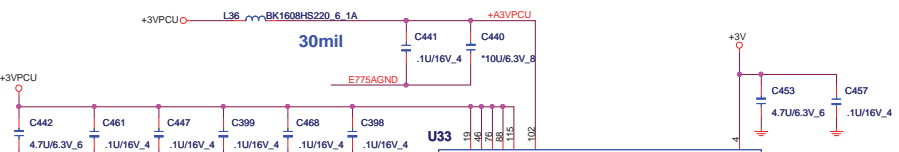
# T/P



**Quanta Computer Inc.**  
PROJECT : ZY2 & ZY6

Size: Document Number: **FAN,LED,KB,DEBUG PORT,TP** Rev: 1A

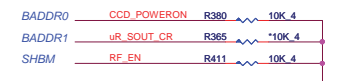
Date: Tuesday, August 21, 2008 Sheet: 31 of 40



### I/O ADDRESS SETTING

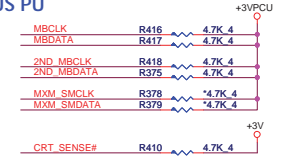
I/O Address		
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

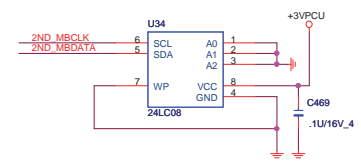


1/13 Confirm by vendor mail:  
Disabled (\*) if using FWH device on LPC.  
Enabled (0) if using SPI flash for both system BIOS and EC firmware

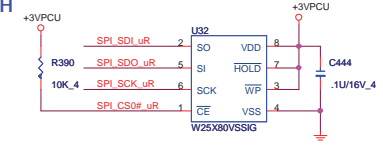
### SM BUS PU



### ACER ID

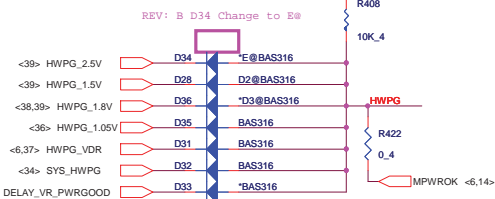


### SPI FLASH



1/13 Confirm by vendor mail:  
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

### H/W POWER GOOD

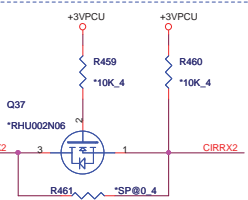


### INTERNAL KEYBOARD STRIP SET



08/10 FAE:  
L43 CAN CHANGE FROM BEAD TO SHORT.  
BUT, PLEASE PUT AGND & 32K CAP & AVCC CAP AT ONE POINT.  
ZS1 STILL USE BEAD FOR SAFE.

### CIR

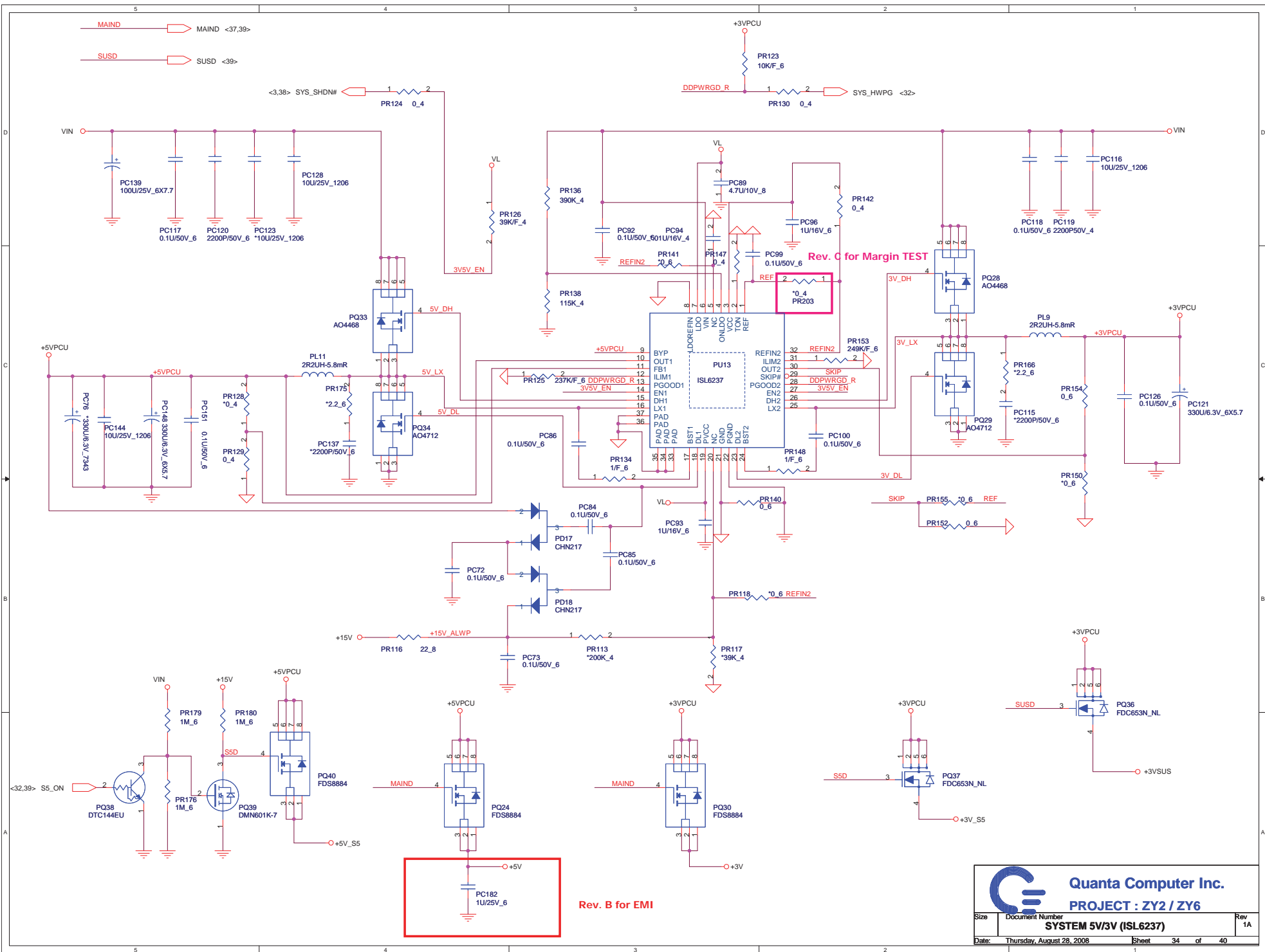


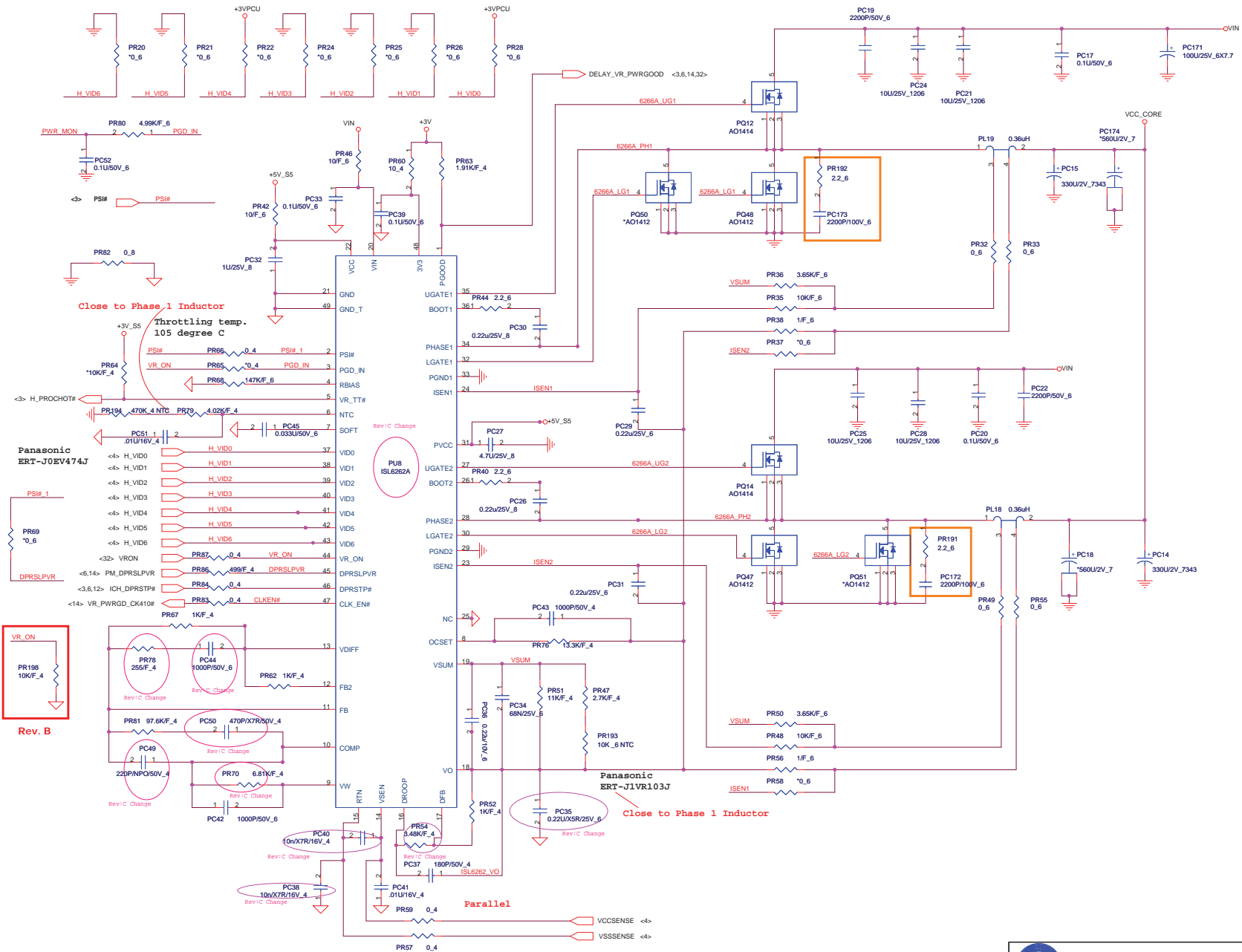
TM & LOW COST	N
AS	Y

**Quanta Computer Inc.**  
PROJECT : ZY2 & ZY6  
WPC775C\_ODG & FLASH  
Date: Tuesday, August 12, 2008  
Sheet 32 of 40









Close to Phase 1 Inductor

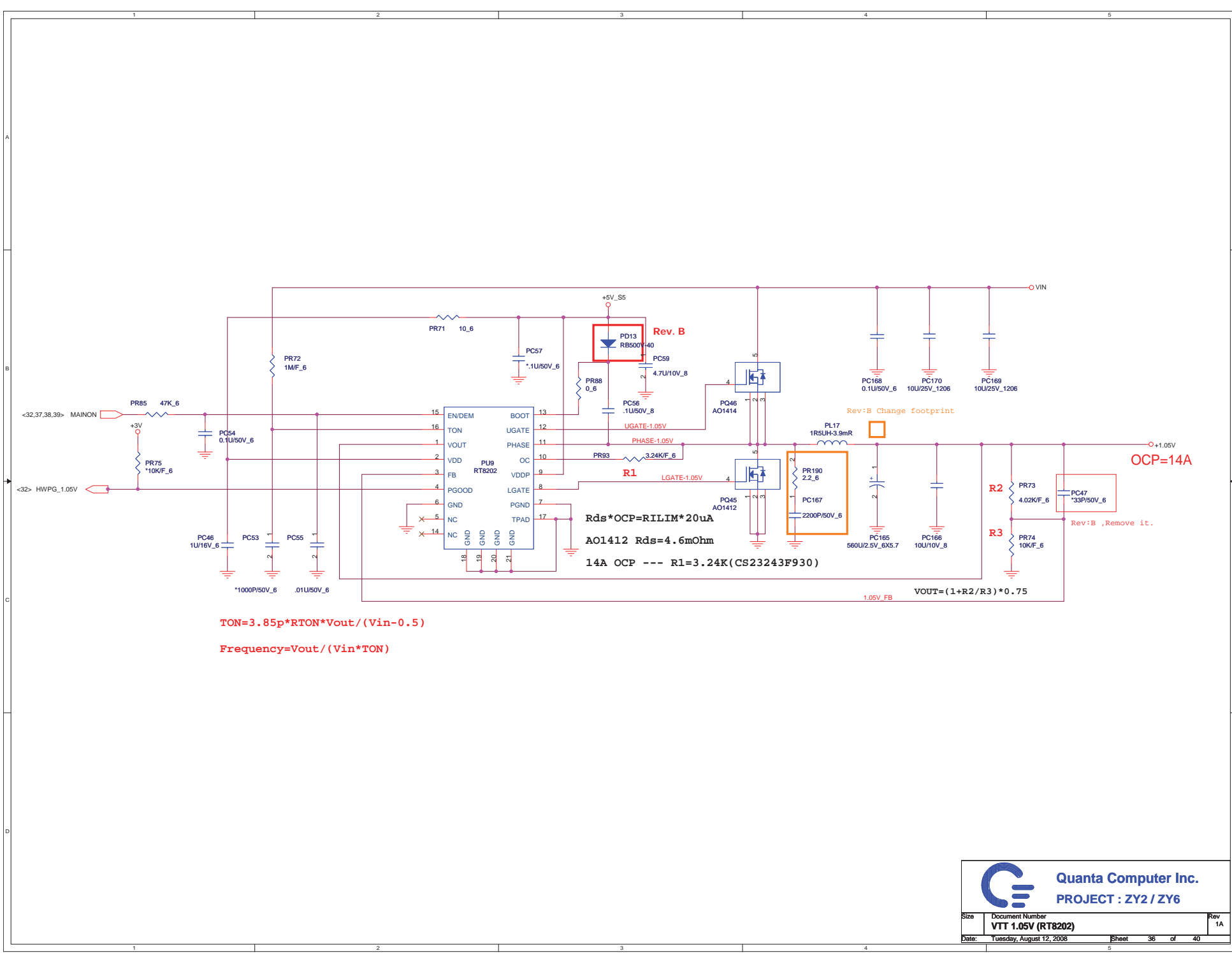
Throttling temp.  
105 degree C

Panasonic  
ERT-J0EV474J

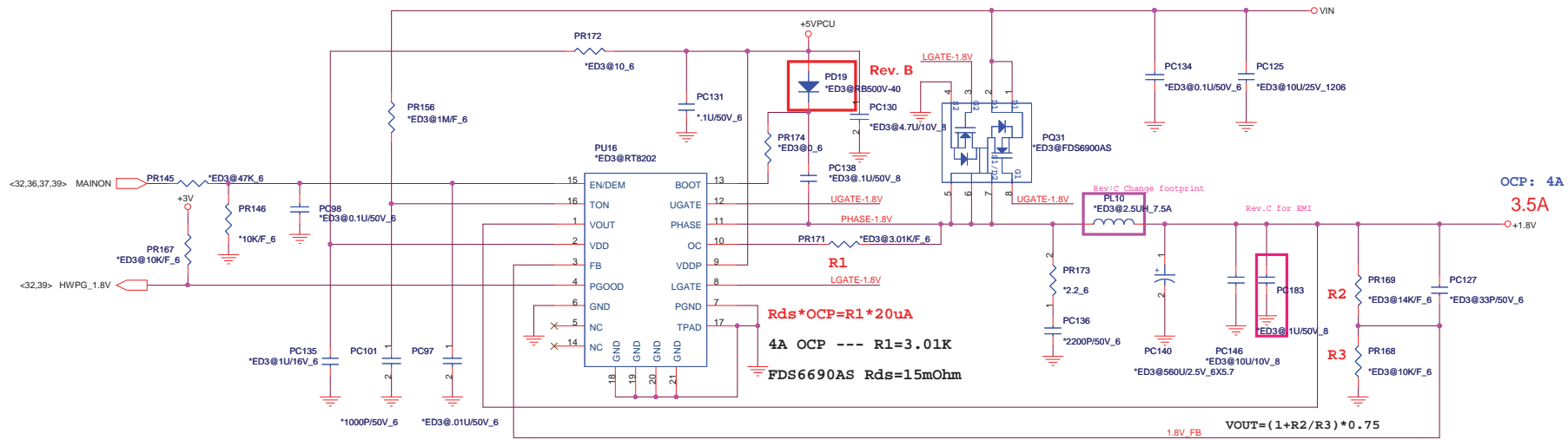
Rev. B

Close to Phase 1 Inductor

Parallel



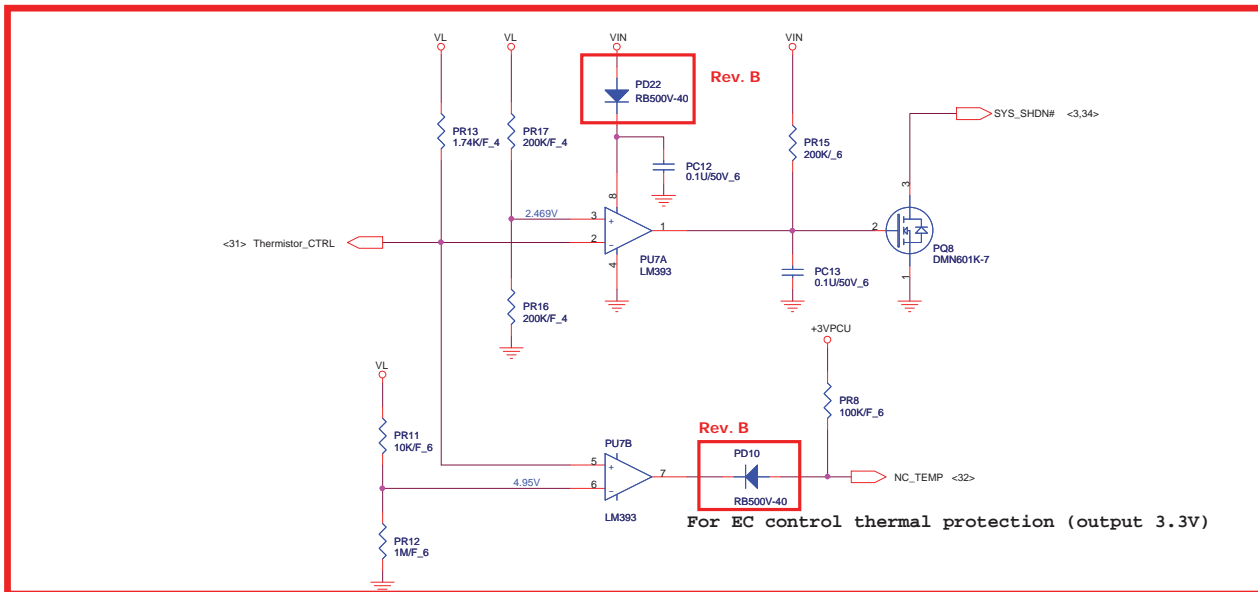




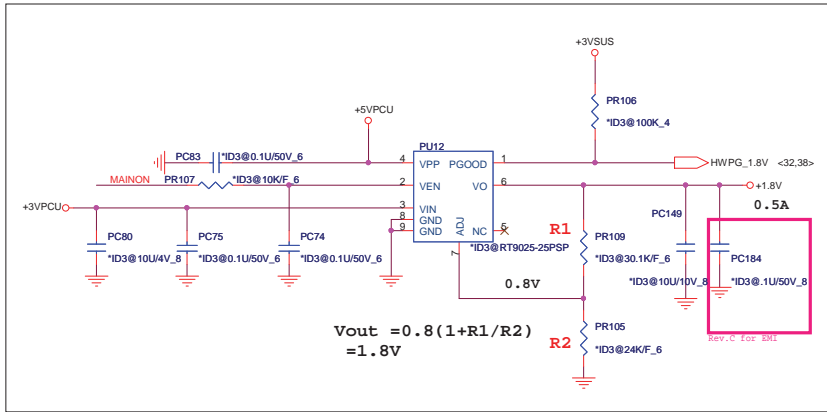
$$TON = 3.85p * RTON * Vout / (Vin - 0.5)$$

$$Frequency = Vout / (Vin * TON)$$

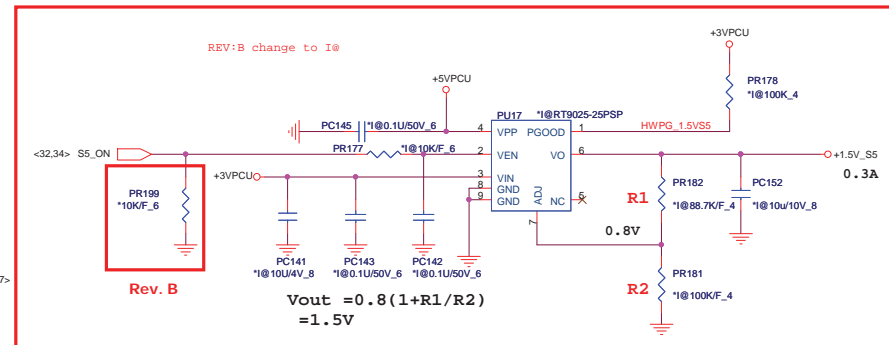
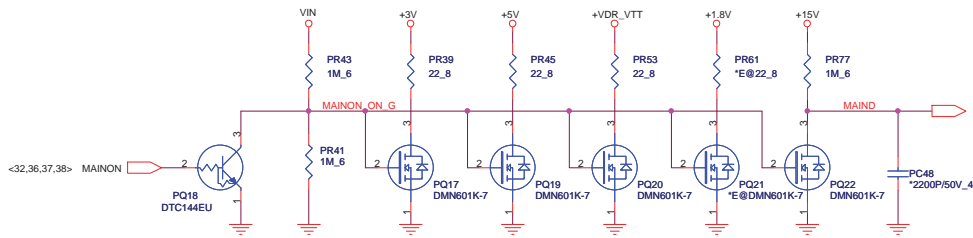
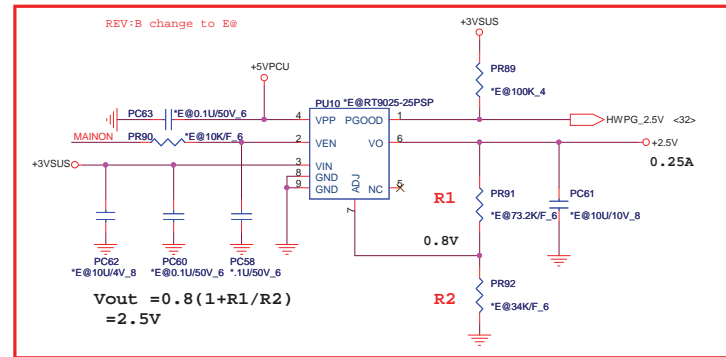
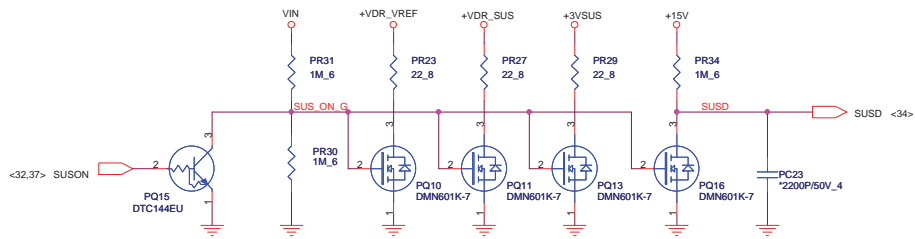
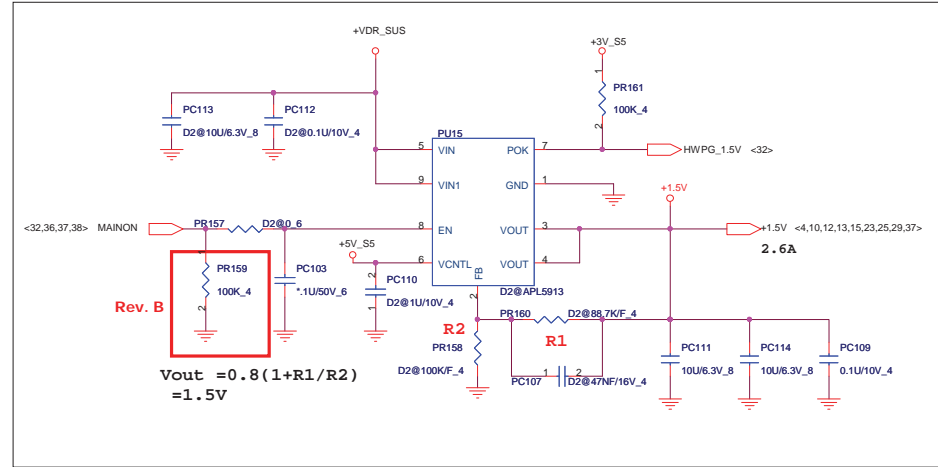
thermal protection --0928



for DDR3 and UMA

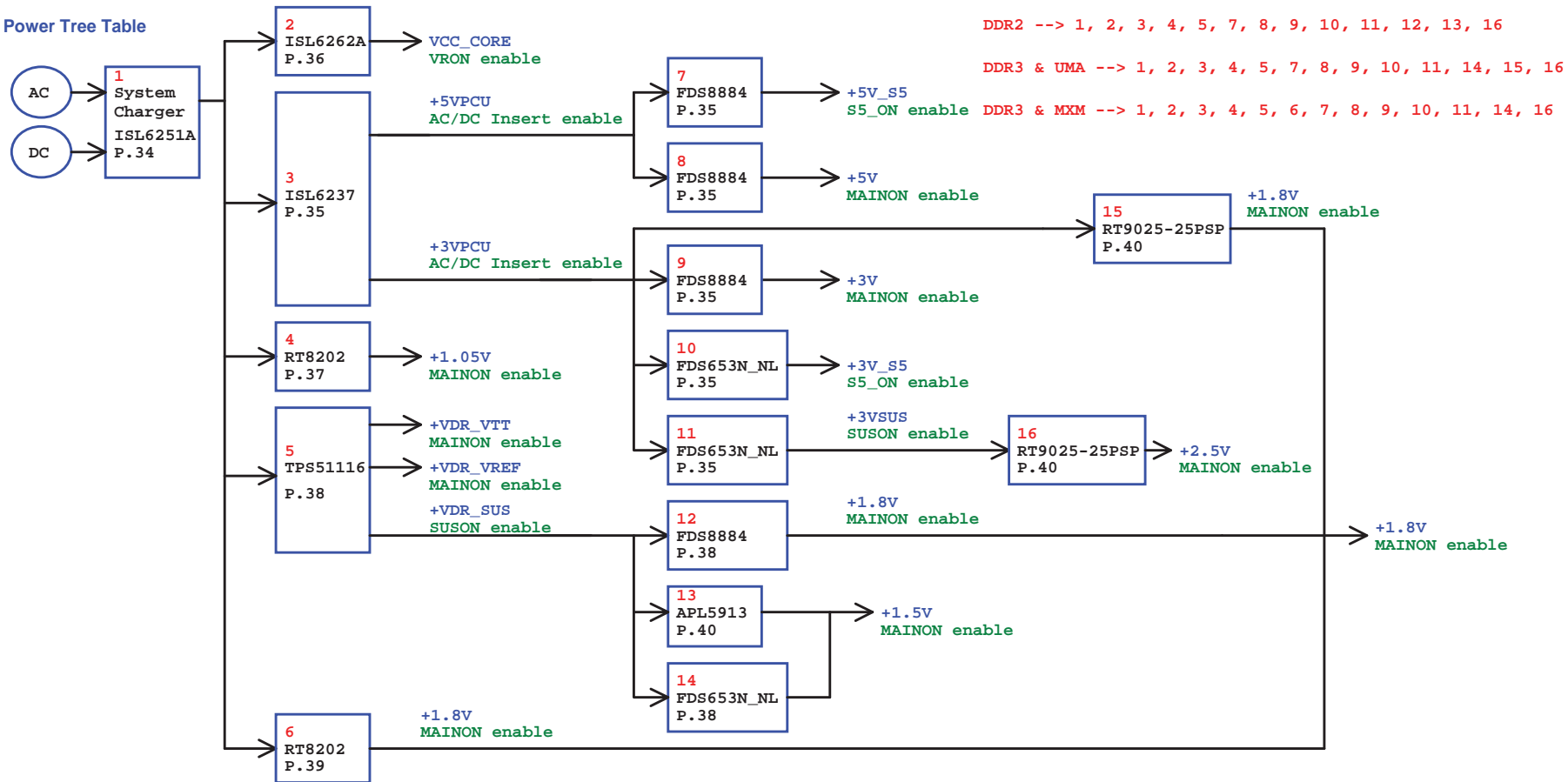


DDR3 -- NC



REV:B change to B@

**Power Tree Table**



**Power Distribution List**

Power	Distribution
VCC_CORE	CPU
+5VPCU	ICH8M, RJ45/USB /B, USB/eSATA, Satellite LED, CIR
+3VPCU	RTC, HALL SENSOR, KB, TP/FP/LED /B, Power /B, Kill SW, EC, ID, SPI Flash, CIR
+1.5V	CPU, GMCH, ICH9M, Mini Card, New Card
+VDR_SUS	GMCH, DDR
+VDR_VREF	GMCH, DDR
+VDR_VTT	DDR
+1.05V	CPU, CLK, Thermal Trip, GMCH, ICH8M
+5V_S5	ICH8M, G-SENSOR, Felica, USB/eSATA
+5V	CPU, ICH8M, VGA, Camera, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, TP/FP/LED /B, EC, Speaker, Headphone
+3V	CLK, CPU Thermal Monitor, FAN, GMCH, DDR, ICH8M, VGA, LCD/LED Panel, HALL SENSOR, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, Cardreader (OZ129T) Mini Card, KB, TP/FP/LED /B, RJ45/USB /B, Bluetooth, MMB, New Card, PC BEEP, EC, Codec (CX20561), VR, Headphone, MDC
+3V_S5	ICH8M, Mini Card, RJ45/USB /B, New Card
+3VSUS	ICH8M, FP
+1.8V	Cardreader
+2.5V	MXM



