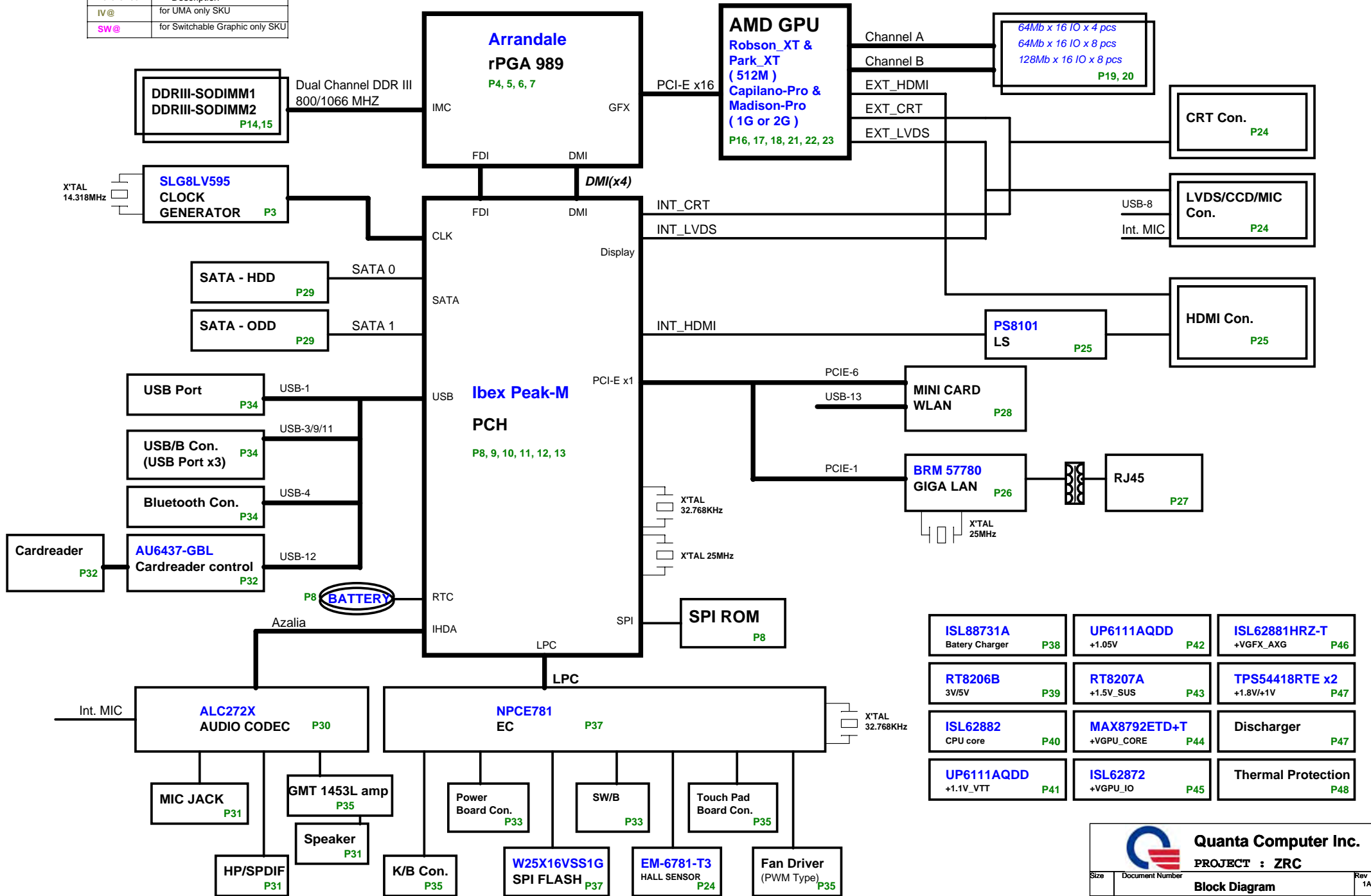


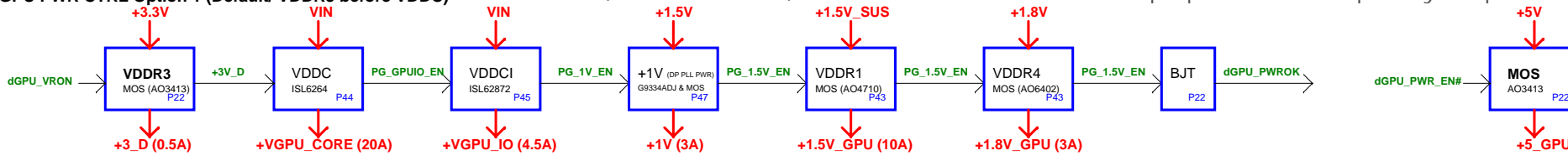
ZRC SYSTEM BLOCK DIAGRAM

BOM Option Table

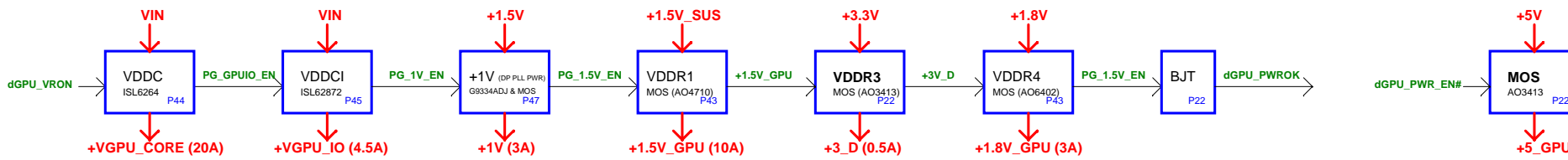
Reference	Description
IV@	for UMA only SKU
SW@	for Switchable Graphic only SKU



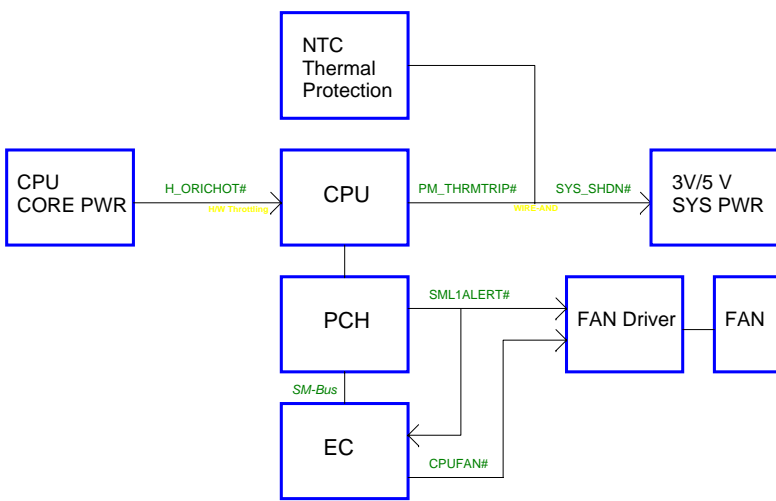
GPU PWR CTRL Option 1 (Default: VDDR3 before VDDC)



GPU PWR CTRL Option 2 (VDDR3 after VDDR1)



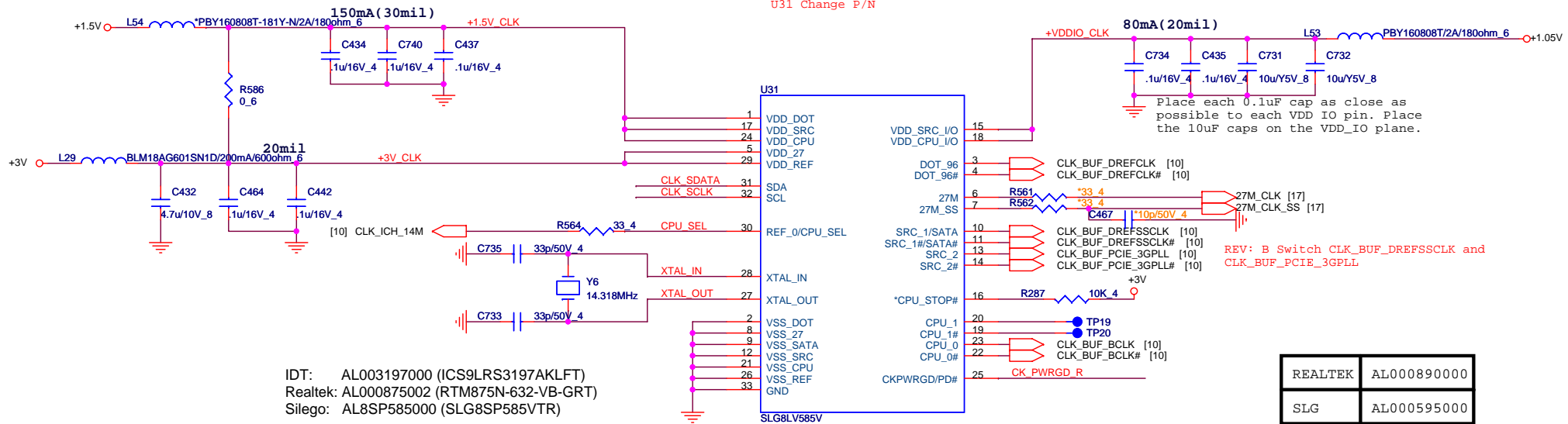
Thermal Follow Chart



Power States

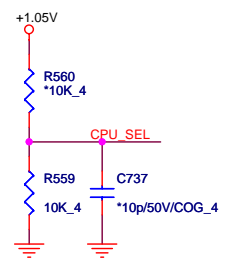
POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

6/21 add R586 for 3V CLK gen
Un-stuff L54
U31 Change P/N



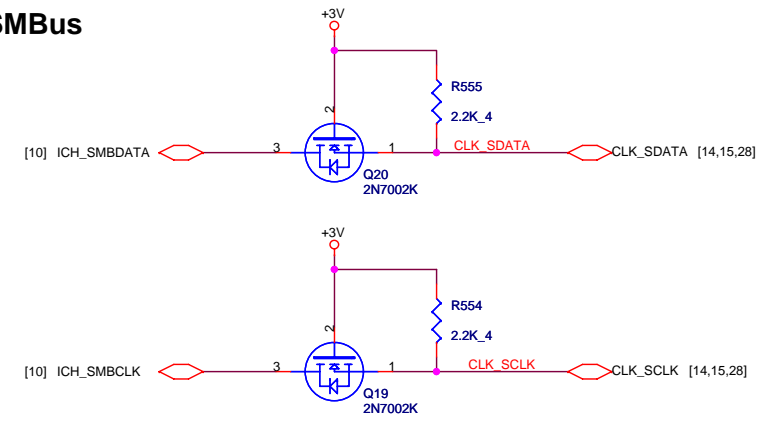
REALTEK	AL000890000
SLG	AL000595000

CPU_CLK select

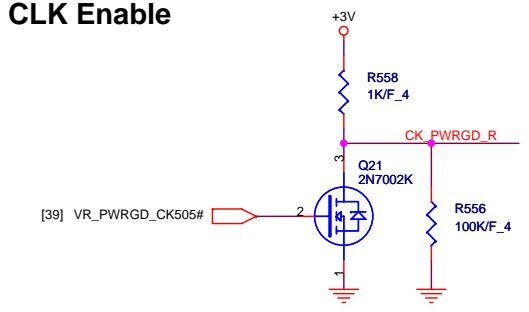


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus

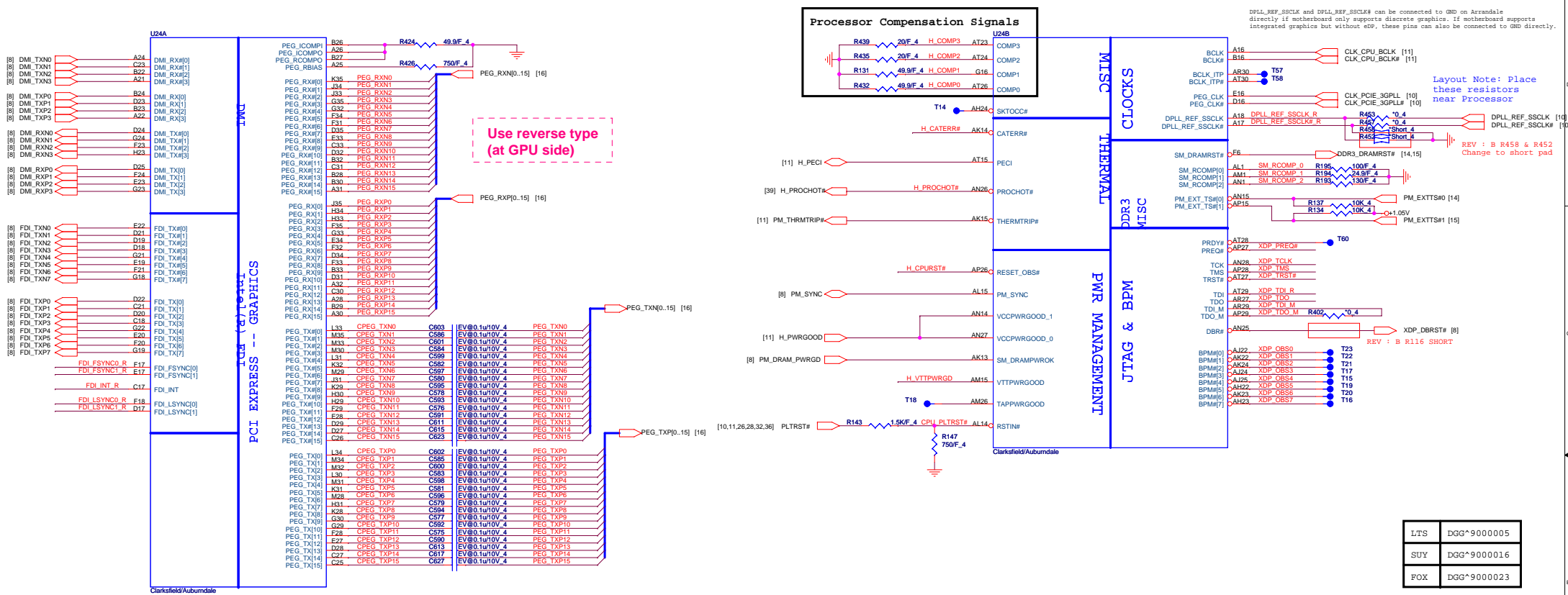


CLK Enable

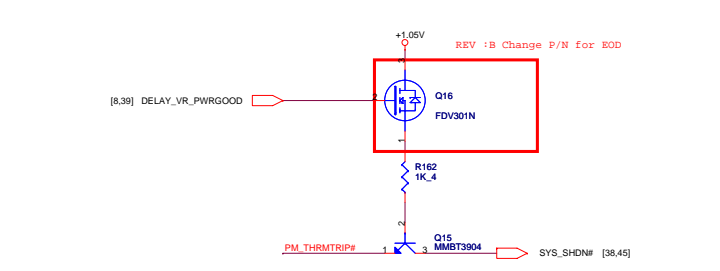


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PROJECT : ZRC

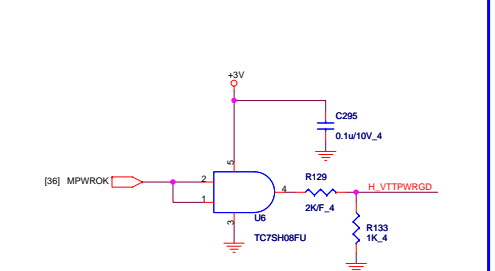
Size	Document Number	Rev
	Clock Generator	1A
Date:	Wednesday, July 21, 2010	Sheet 3 of 46



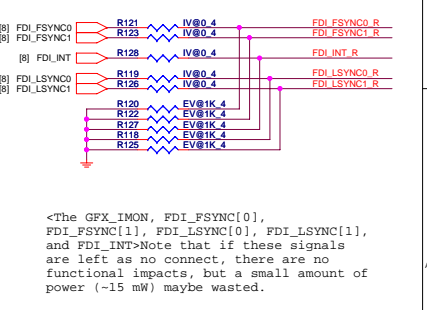
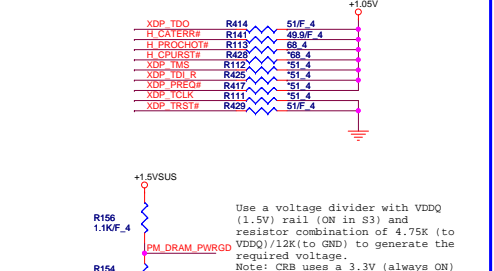
Thermaltrip protect

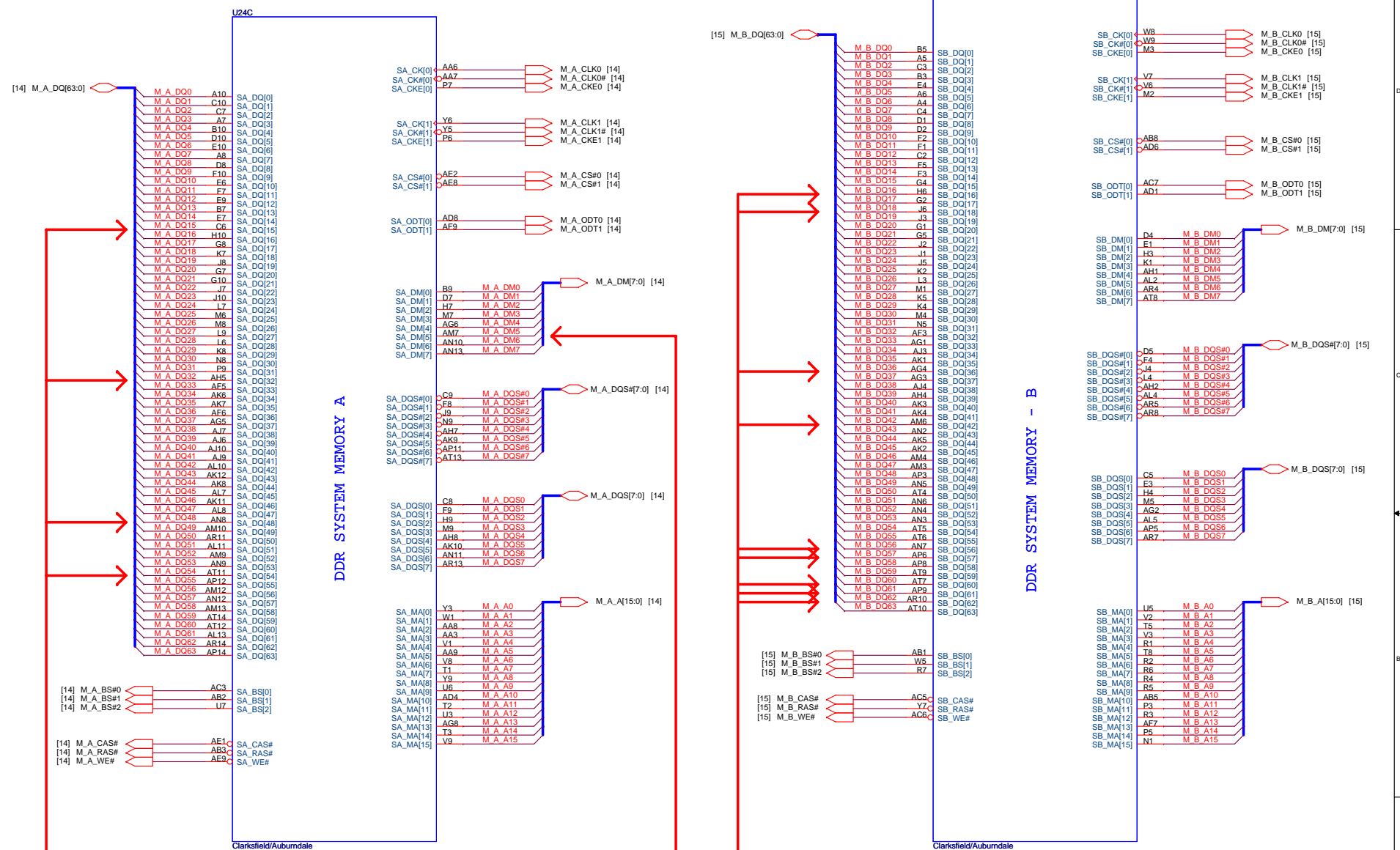


VTT PWR_Good



Processor pull-up



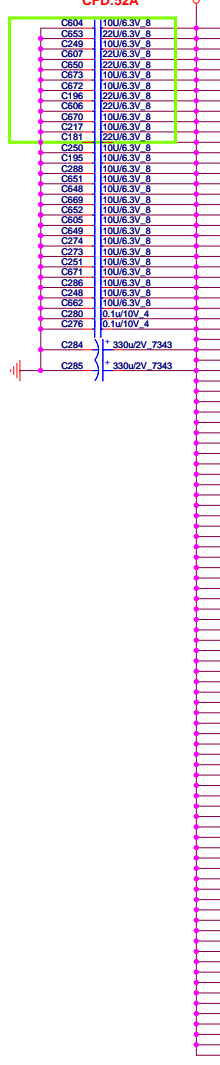


Channel A DQ[15,32,48,54], DM[5]
 Requires minimum 12mils spacing
 with all other signals, including data signals.

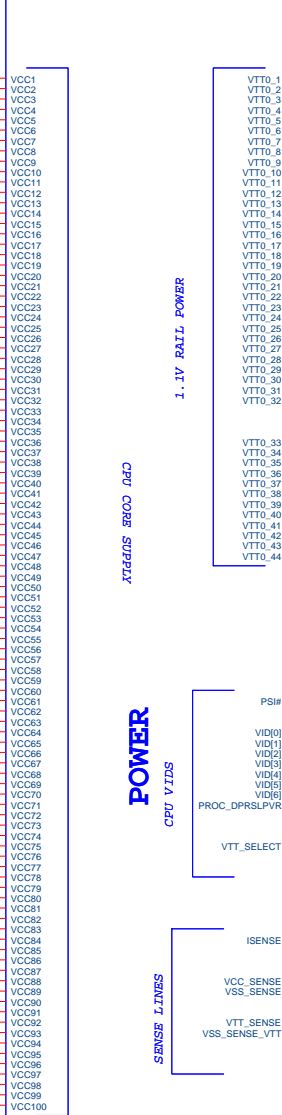
Channel B DQ[16,18,36,42,56,57,60,61,62]
 Requires minimum 12mils spacing
 with all other signals, including data signals.

CPU Core Power

ARD:48A
CFD:52A



U24F



Clarksfield/Auburndale

AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

VTT Rail Values are
Auburndale VTT=1.05V
Clarksfield VTT=1.1V

18A → +1.05V

1.1V RAIL POWER

CPU CORE SUPPLY

POWER

CPU VIDS

SENSE LINES

AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)

22A → +V GFX_AGX

+1.05V

+1.05V

+1.05V

+1.05V

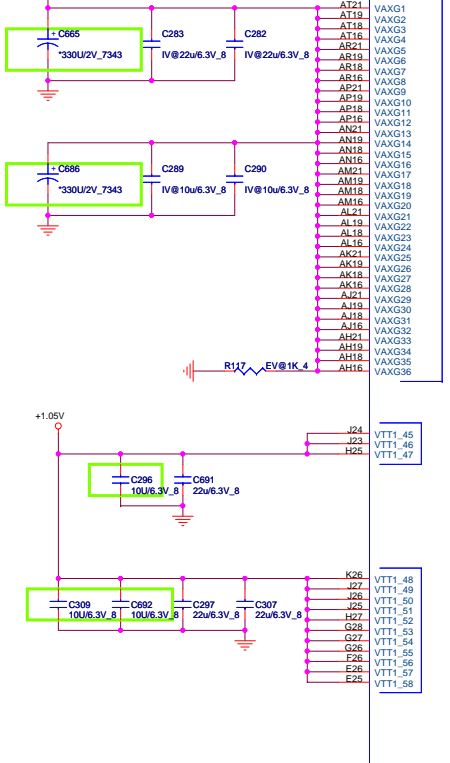
+1.05V

+1.05V

+1.05V

+1.05V

+1.05V



GRAPHICS

SENSE LINES

GRAPHICS VIDS

POWER

FDI

PG & DWT

DDR3 - 1.5V RAILS

I.1V

I.8V

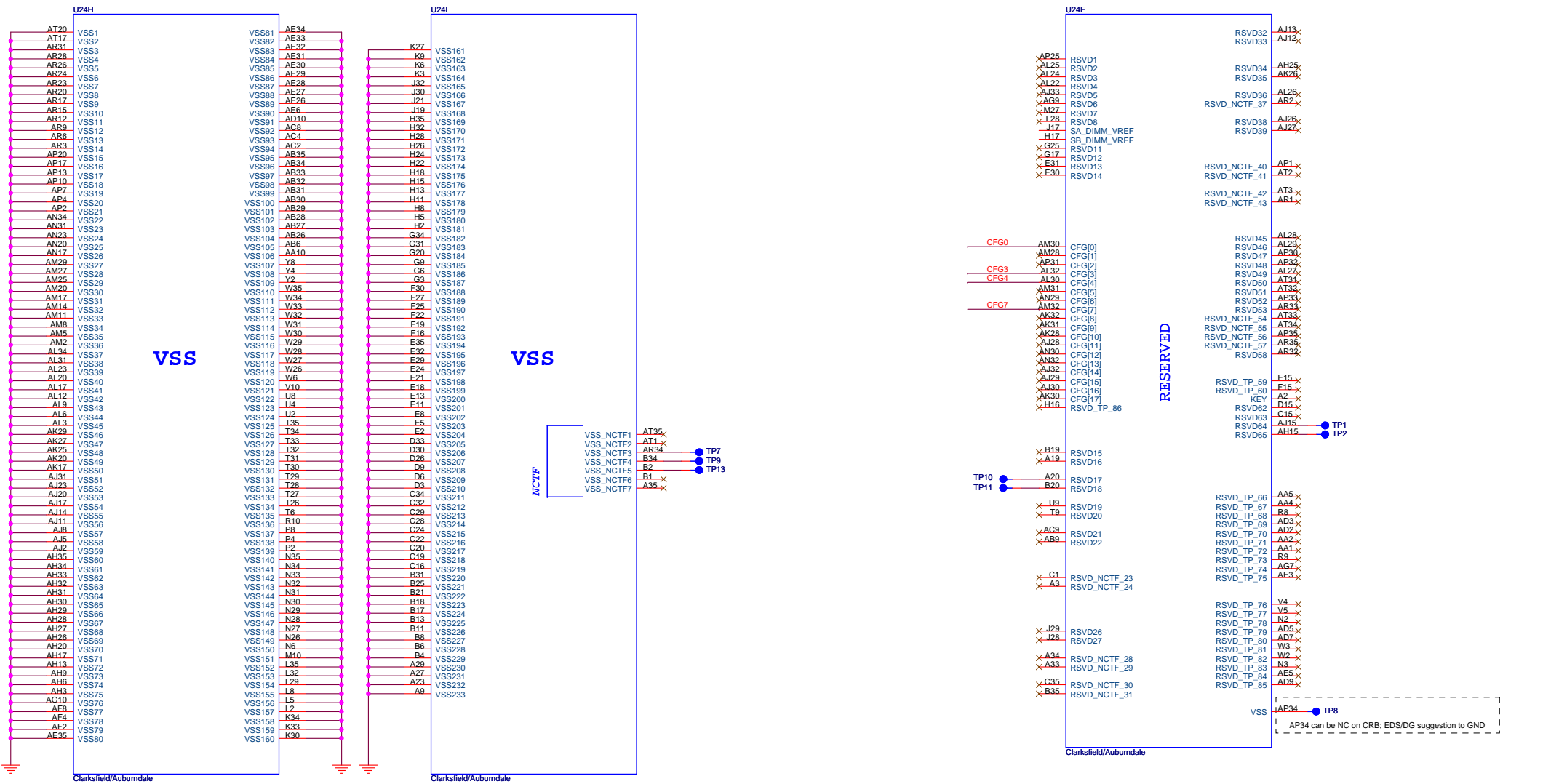
0.6A

Clarksfield/Auburndale

NOTE:
For Validating IMV9 VR R6451 should be STUFF
and R2N1 NO_STUFF

HFM_VID : Max 1.4V
LFM_VID : Min 0.65V

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Processor Strapping

	1	0	DEFAULT	
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled	1	CFG0 R110 \sim 3.01K NC
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed	1	CFG3 R102 \sim 3.01K/F 4
CFG4 (Embedded Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port	1	CFG4 R109 \sim 3.01K
The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.				CFG7 R103 \sim 3.01K/F 4

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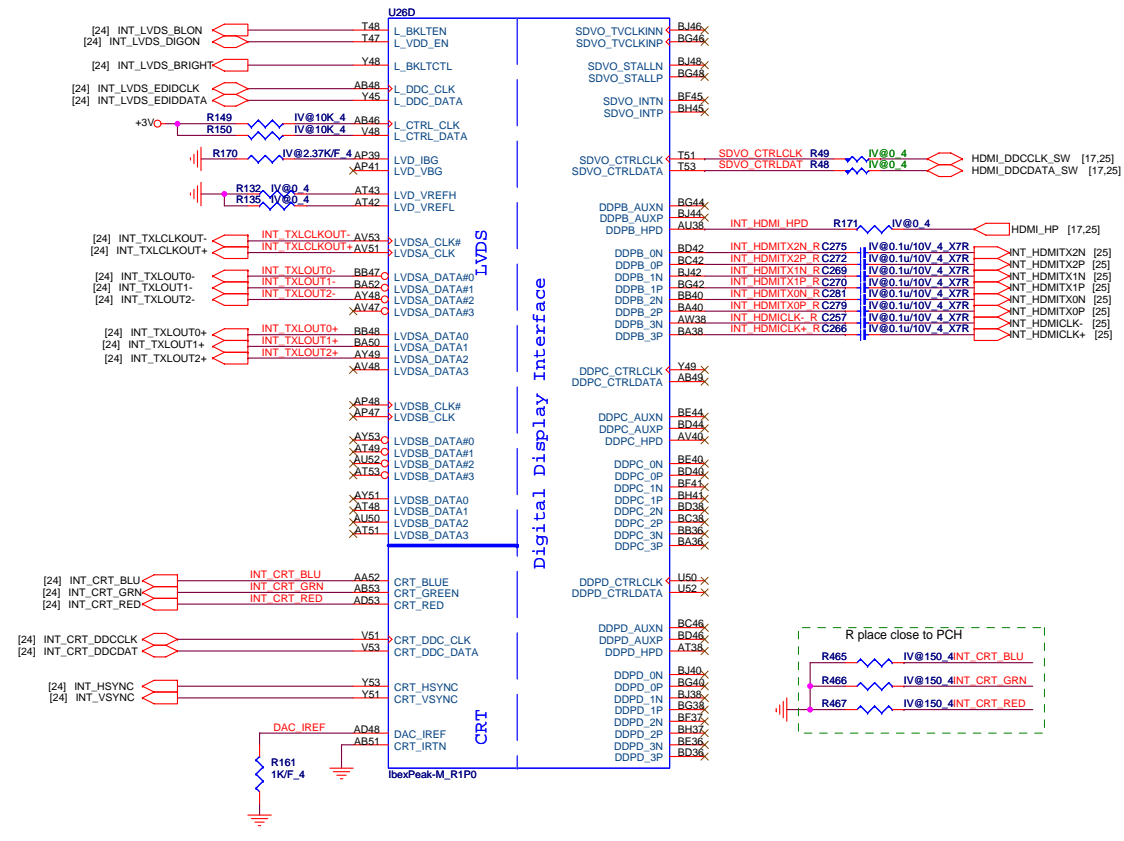
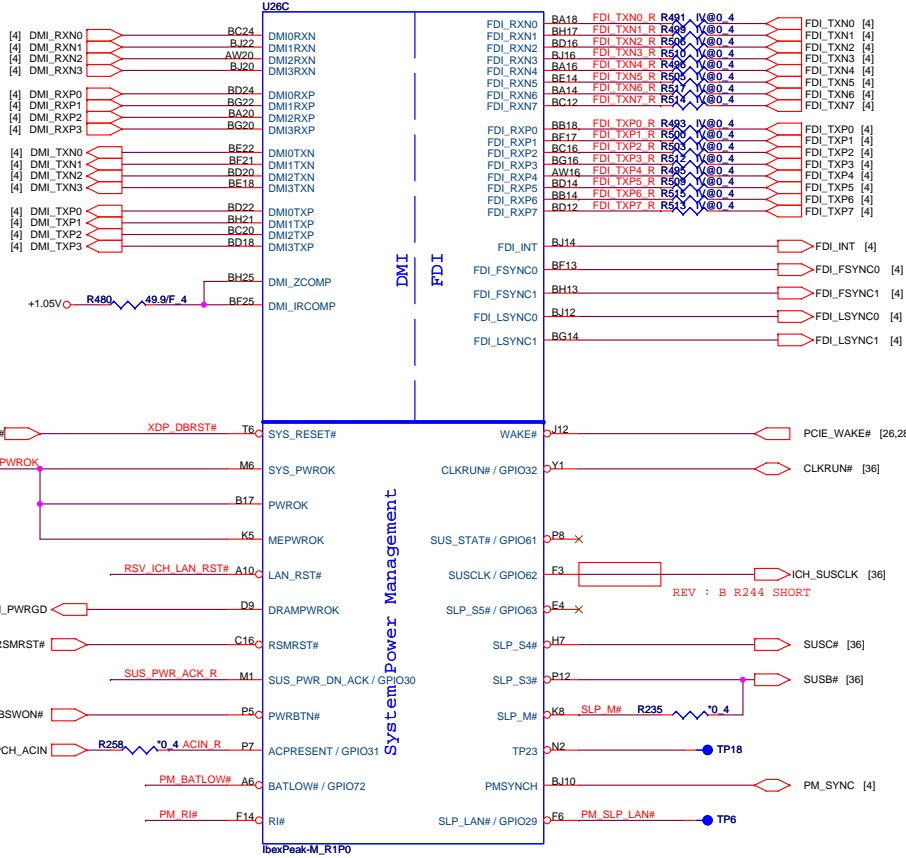
Size Document Number
AUBURND4 4/4

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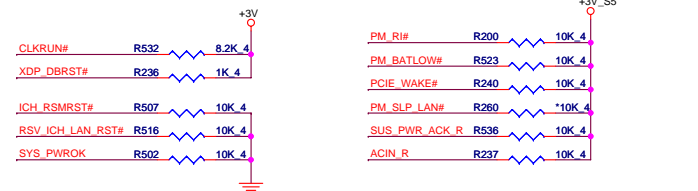
Rev 1A

0-ohm resistor place close to PCH

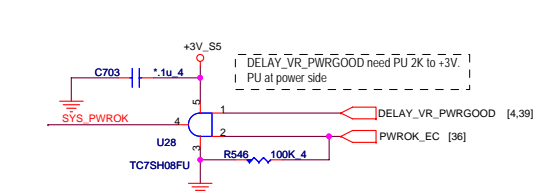
IBEX PEAK-M (LVDS, DDI)



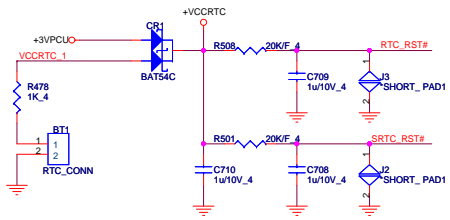
PCH Pull-high/low



System PWR_OK

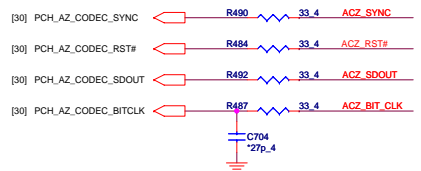


RTC Circuitry

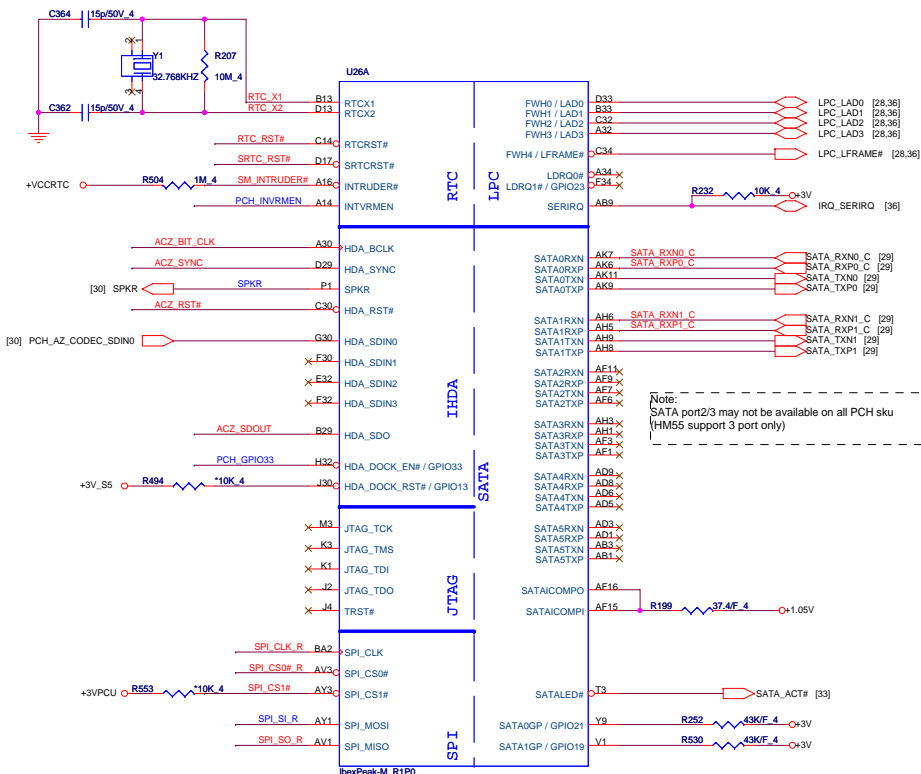
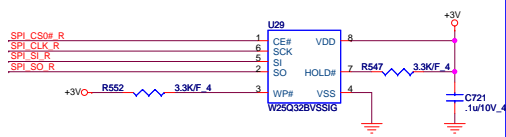


HDA_SYNC (PCH strap pin)
 Internal weak pull-down
 VCCVRM=>+1.8V (default)
 external pull-up
 VCCVRM=>+1.5V

HDA Bus

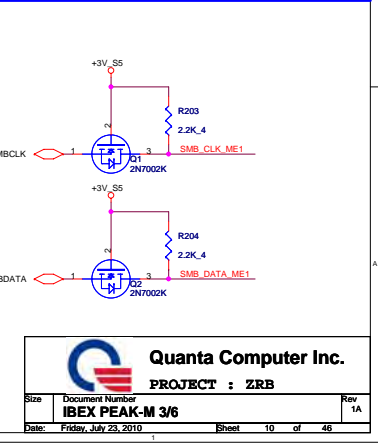
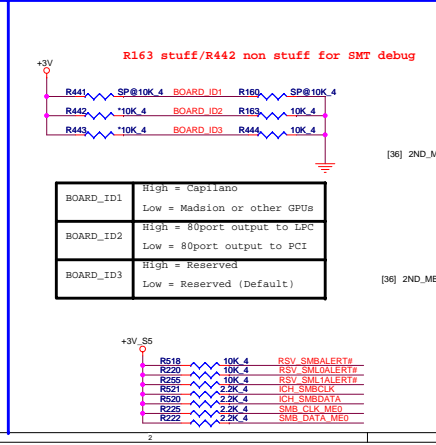
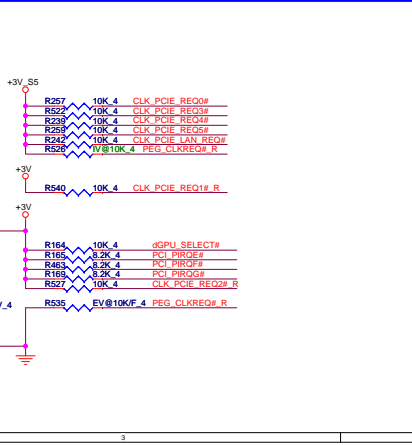
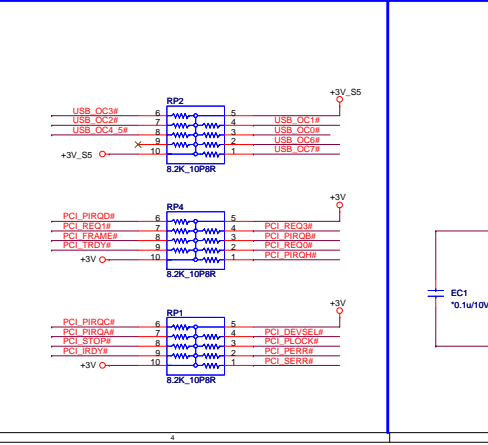
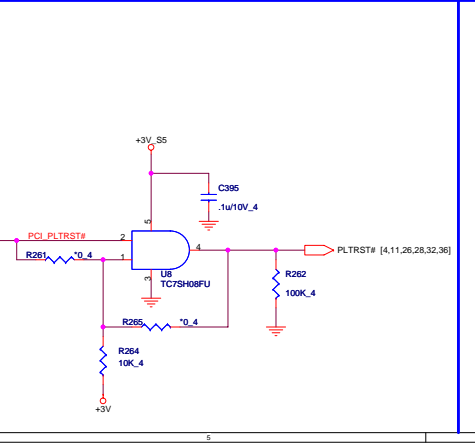
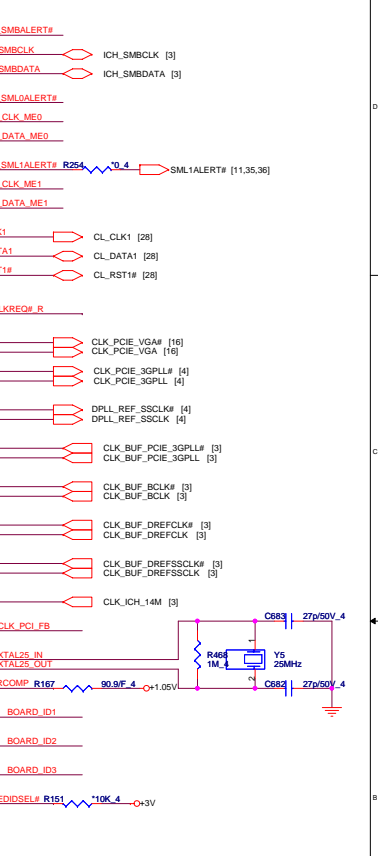
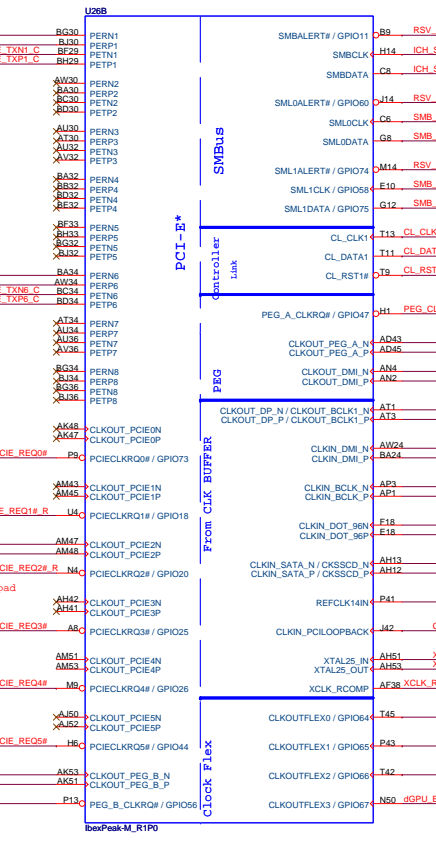
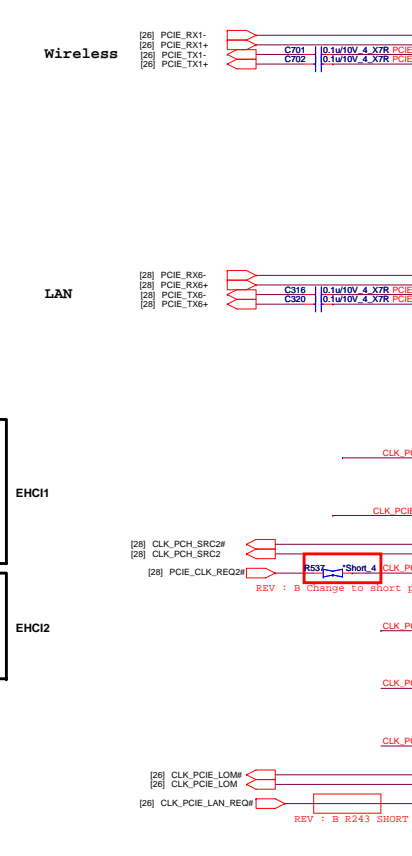
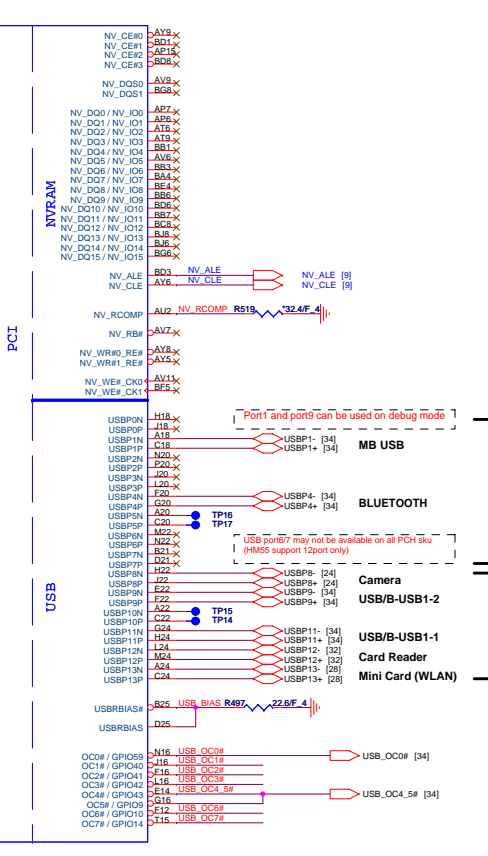
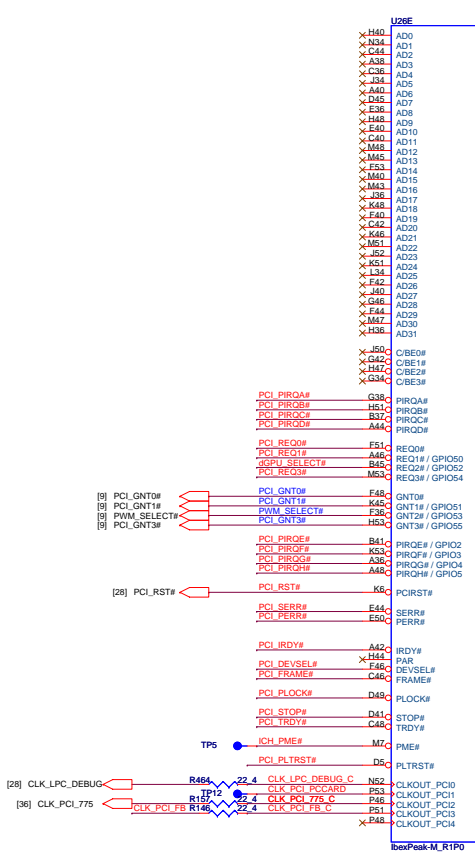


PCH SPI



PCH Strap Pin Configuration Table-1

INTVRMEN	Integrated 1.05V VRM Enable / Disable	1 = Integrated VRM is enabled 0 = Integrated VRM is disabled	+VCCRTC ○ R511 330K 6 PCH_INVRMEN
SPI_MOSI	TPM Functionality Disable	1 = Enabled 0 = Disable	+3V ○ R551 1K 4 SPI_SI_R
SPKR	Reboot option at power-up	0 = Default Mode (Internal weak Pull-down) 1 = No Reboot Mode with TCO Disabled	+3V ○ R538 1K 4 4SPKR
HDA_DOCK_EN# / GPIO33	Flash Descriptor Security Override	0 = Flash Descriptor Security will be overridden 1 = Security measure defined in the Flash Descriptor will be enabled.	PCH_GPIO33 J1 1 2 'SHORT_PADI'
GNT0#, GNT1#	Boot BIOS Strap	(0,0) = LPC (0,1) = Reserved NAND (1,0) = PCI (1,1) = SPI	[10] PCL_GNT0# R156 1K 4 [10] PCL_GNT1# R157 1K 4 R158 1K 4
GNT2# / GPIO53	ESI Strap (Server Only)	ESI compatible mode is for server platforms only	[10] PWM_SELECT# R182 1K 4
GNT3# / GPIO55	Top-Block Swap Override	0 = Top Block Swap Mode 1 = Default Mode (Internal pull-up)	[10] PCL_GNT3# R462 10K 4
NV_ALE	Intel® Anti-Theft Technology HDD Data Protection (Intel AT-d) Enable	1 = Enabled 0 = Disabled (Default)	[10] NV_ALE R213 1K 4 +1.8V
NV_CLE	DMI Termination Voltage	DMI termination voltage. Weak internal pull-up. Do not pull low.	[10] NV_CLE R216 1K 4 +1.8V
GPIO8	Reserved	This signal has a weak internal pull up. NOTE: This signal should not be pulled low	[11] RSV_GPIO8 R215 10K 4 +3V_S5 R214 1K 4
GPIO15	Reserved	0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality	[11] CR_WAKE# R256 1K 4 +3V_S5
GPIO27	On-Die PLL Voltage Regulator <internal weak pull-up>	0 = Disables the VccVRM. 1 = Enables the internal VccVRM to have a clean supply for analog rails.	[11] PCH_GPIO27 R231 10K 4



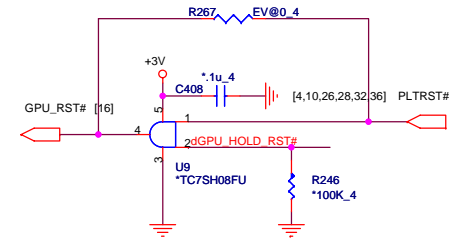
R163 stuff/R442 non stuff for SMT debug

BOARD_ID1	High = Capilano
	Low = Madison or other GPUs
BOARD_ID2	High = 80port output to LPC
	Low = 80port output to PCI
BOARD_ID3	High = Reserved
	Low = Reserved (Default)

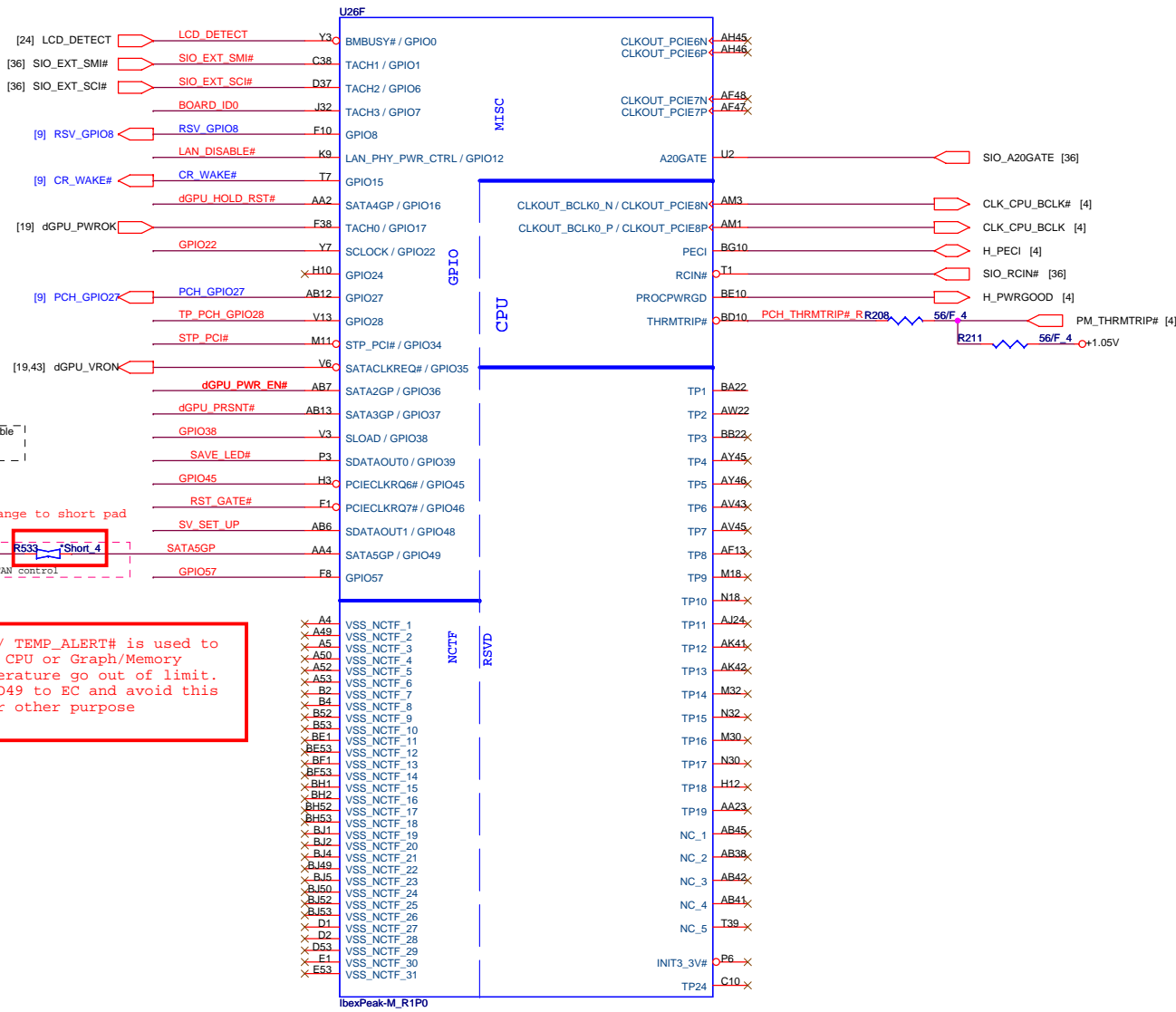
R518	10K_4	RSV_SMBALERT#
R256	10K_4	RSV_SMBALERT#
R521	10K_4	RSV_SMBALERT#
R520	2.2K_4	ICH_SMBDATA
R228	2.2K_4	SMB_CLK_MEO
R222	2.2K_4	SMB_DATA_MEO
R227	2.2K_4	SMB_DATA_MEO

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GPU_RST#



IBEX PEAK-M (GPIO, VSS_NCTF, RSVD)



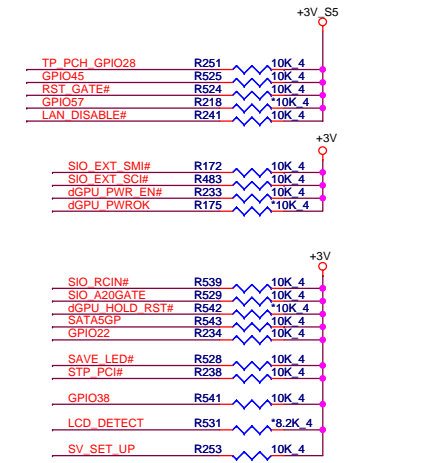
[dGPU_PWR_EN# should be stable]
before dGPU_VRON enable

REV : B Change to short pad

[10,35,36] SML1ALERT# R533 Short 4
EC suggestion use GPIO49 for FAN control

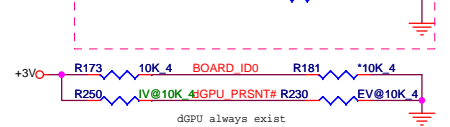
SATA5GP / GPIO49 / TEMP_ALERT# is used to alert for EC when CPU or Graph/Memory controllers' temperature go out of limit. So connecting GPIO49 to EC and avoid this pin to be used for other purpose

GPIO Pull-up/Pull-down



SV_SET_UP 1-X High = Strong (Default)

GPIO57 stuff PD and not stuff PU for Intel suggestion at 6/1

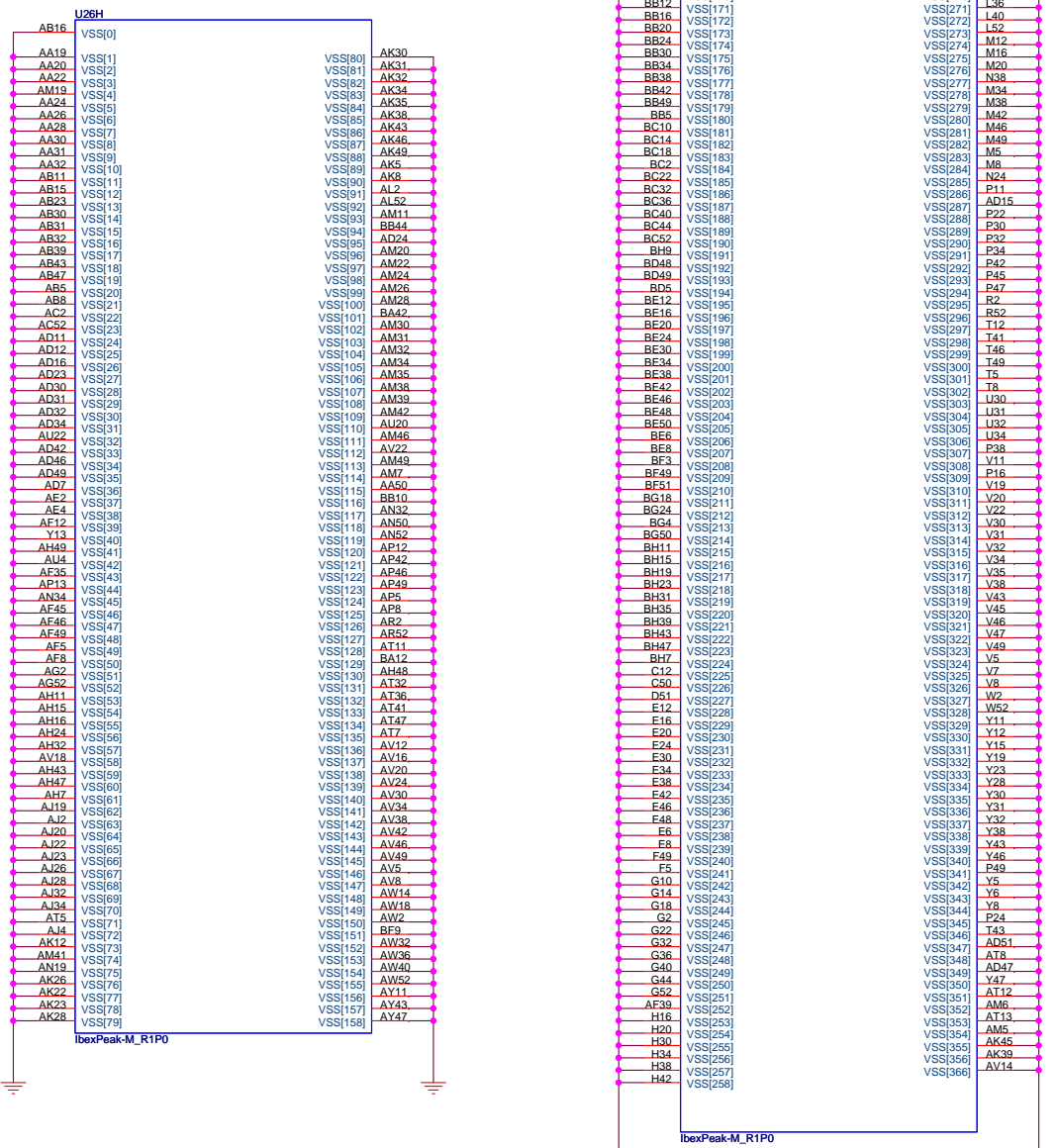



BOARD_ID0 High = 15"
Low = 14"

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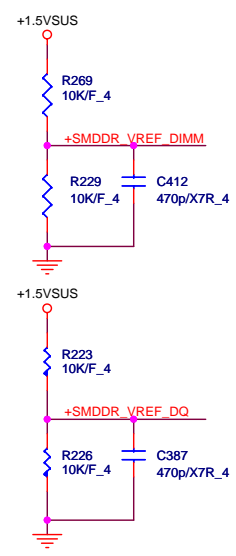
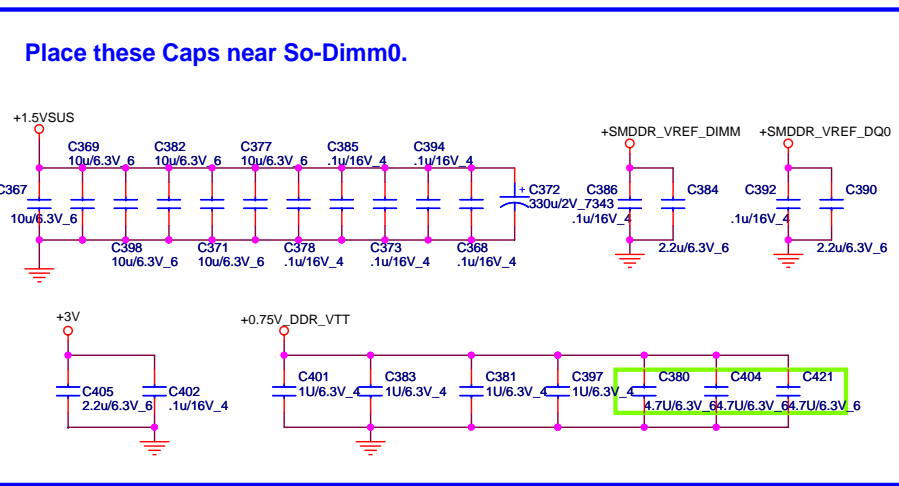
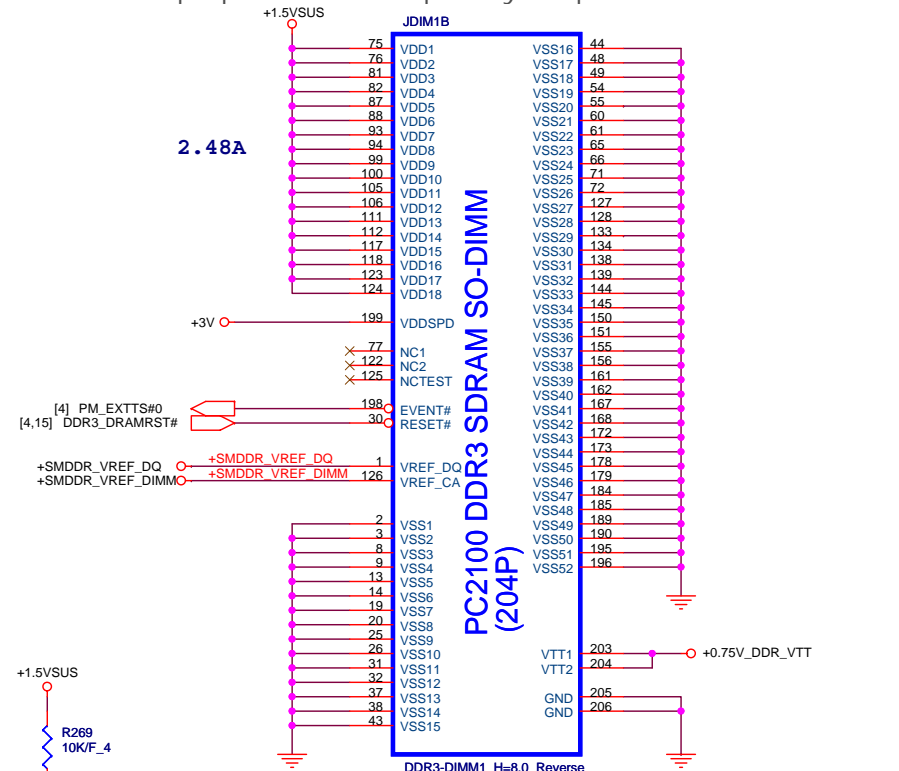
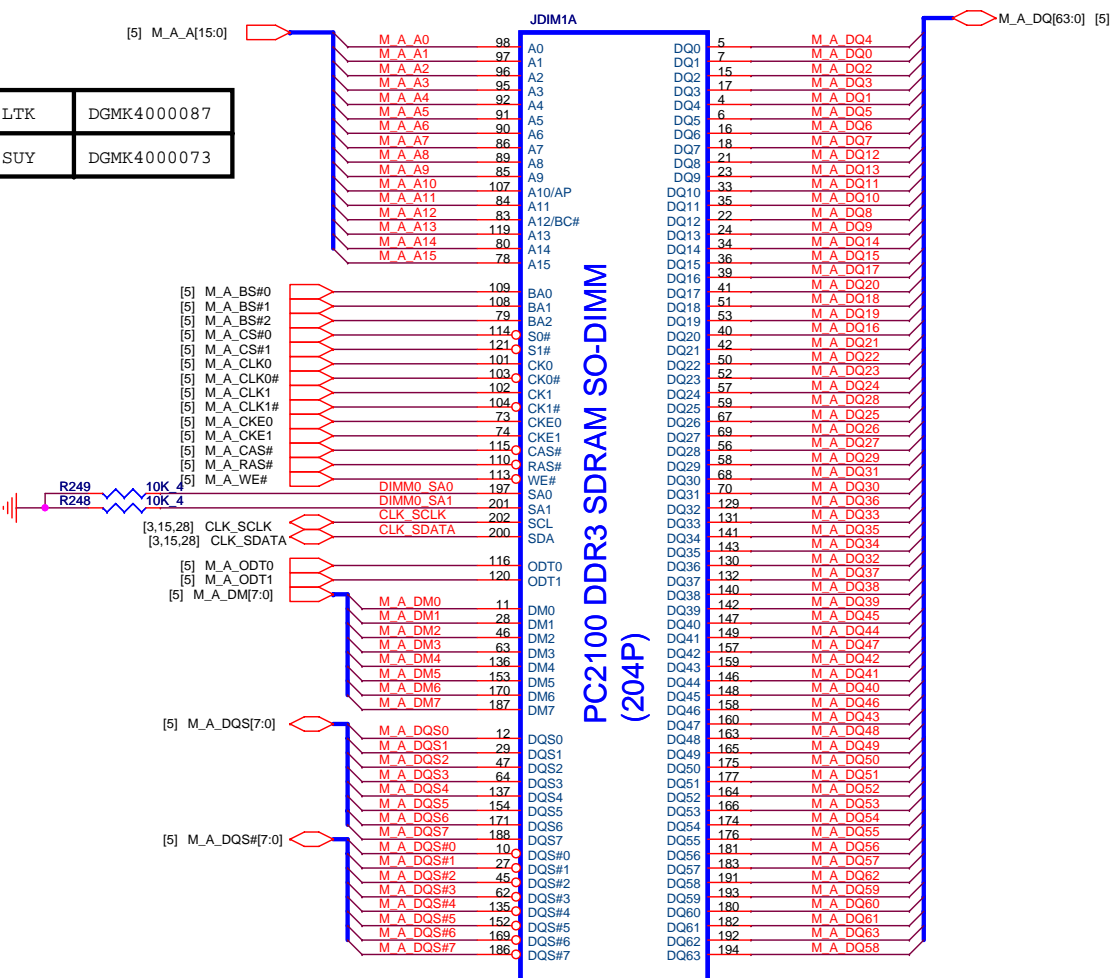
Size	Document Number	Rev
	IBEX PEAK-M 4/6	1A
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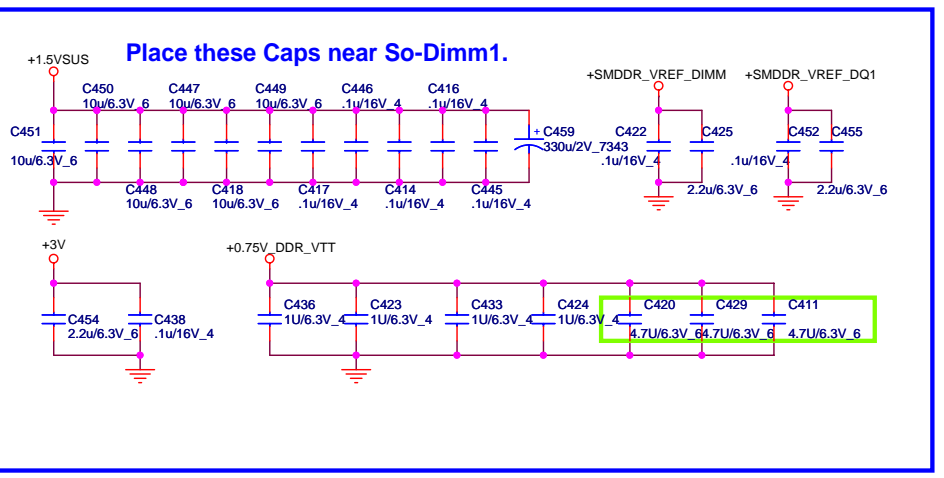
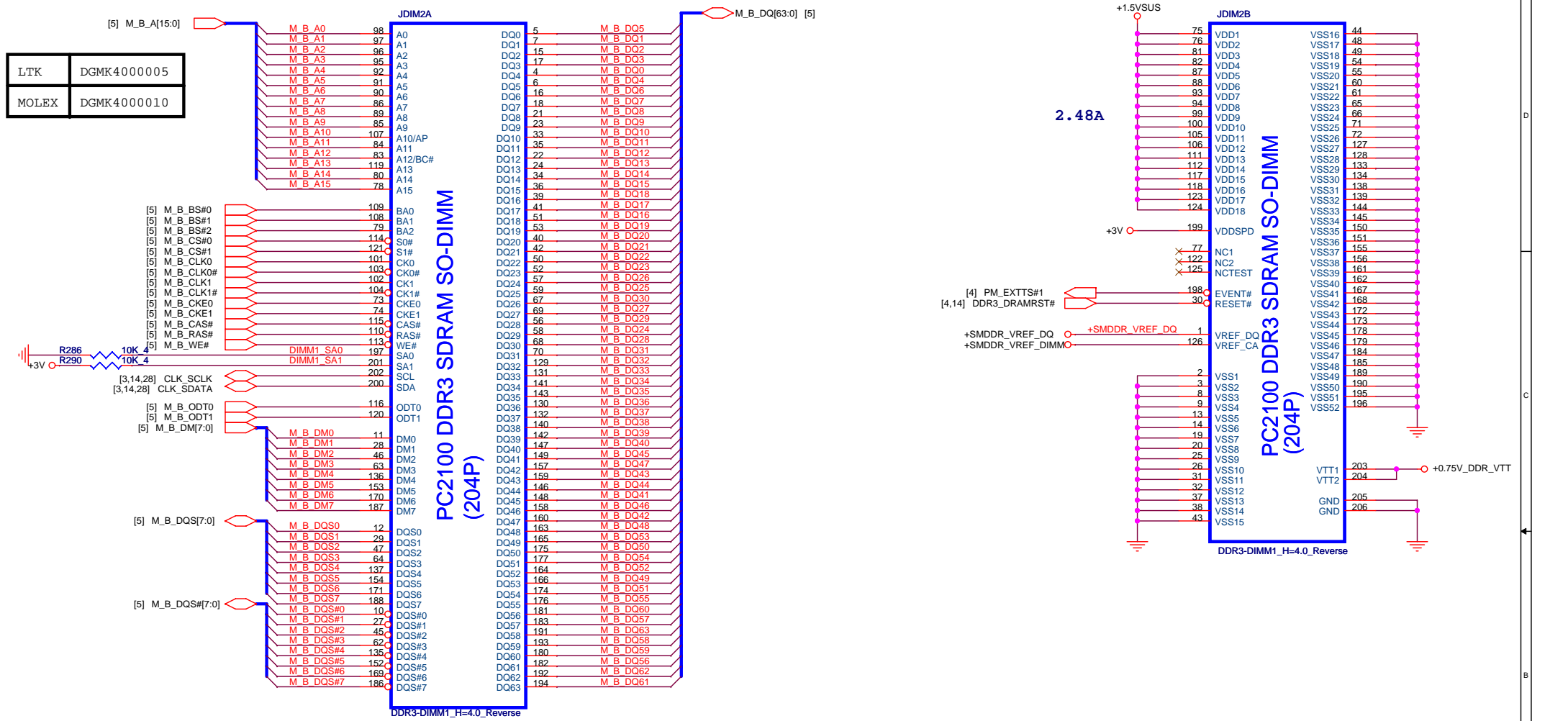
IBEX PEAK-M (GND)



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LTK	DGMK4000087
SUY	DGMK4000073





GPU_1(VGA)



Madison	AJ007720T02
Park	AJ077400T08

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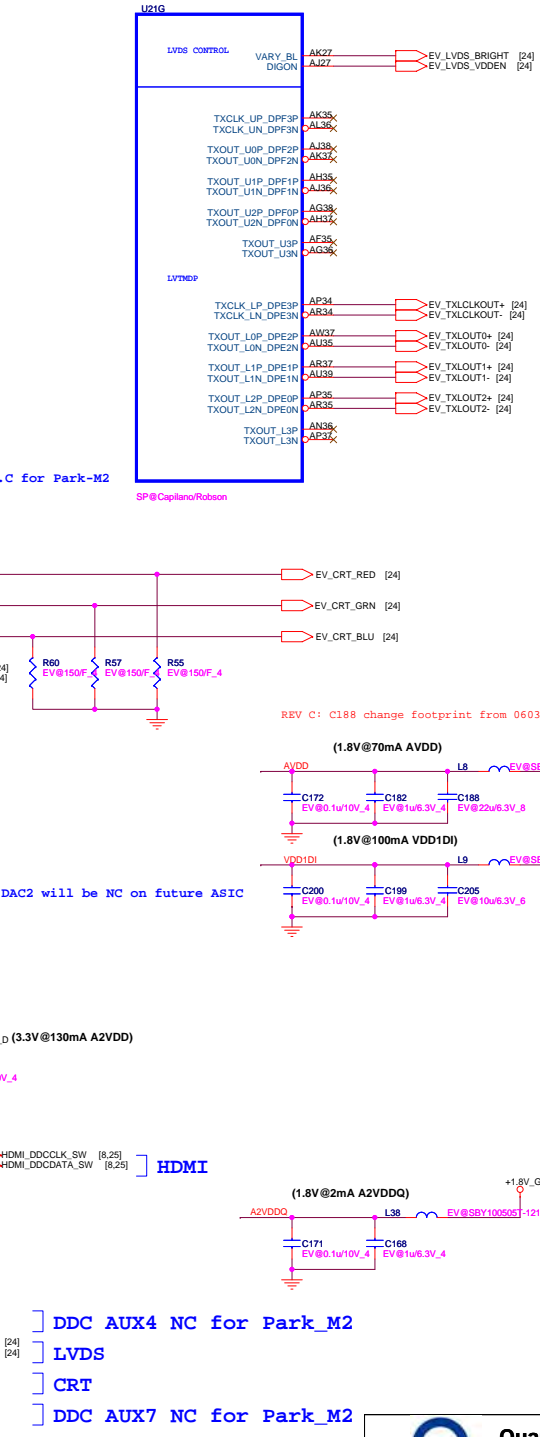
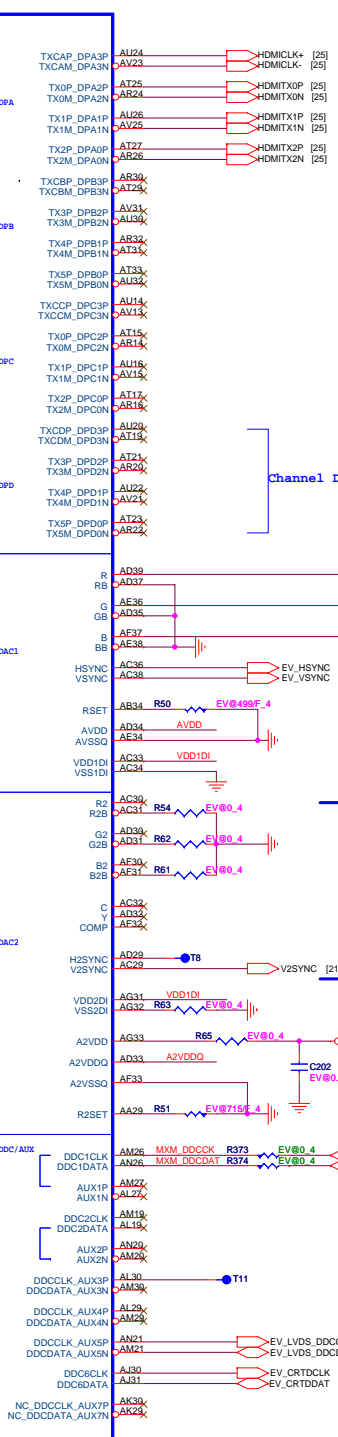
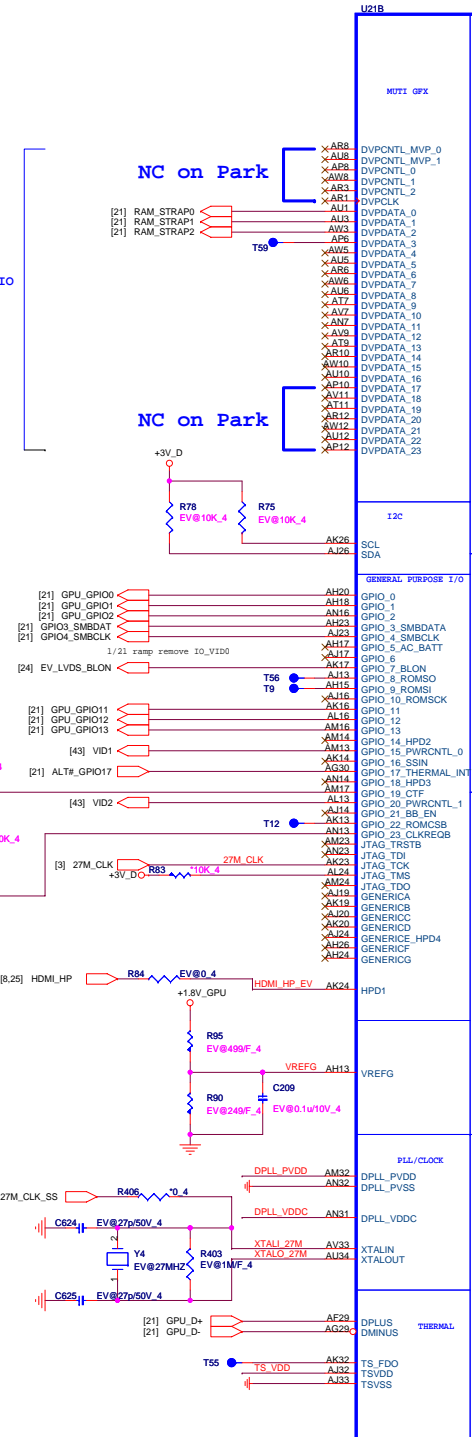
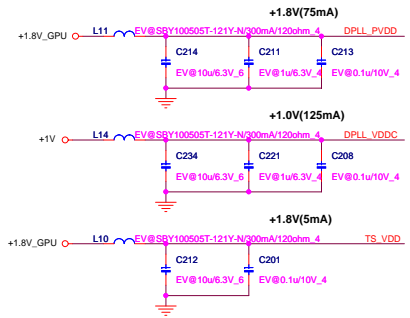
GPU_2(VGA)

GPU Power-on sequence

- 1 => +VGPU_CORE
- 2 => +VGPU_IO
- 3 => +1V
- 4 => +1.5V_GPU
- 5 => +3V_D
- 6 => +1.8V_GPU
- 7 => dGPU_PWROK

1.8V GPIO

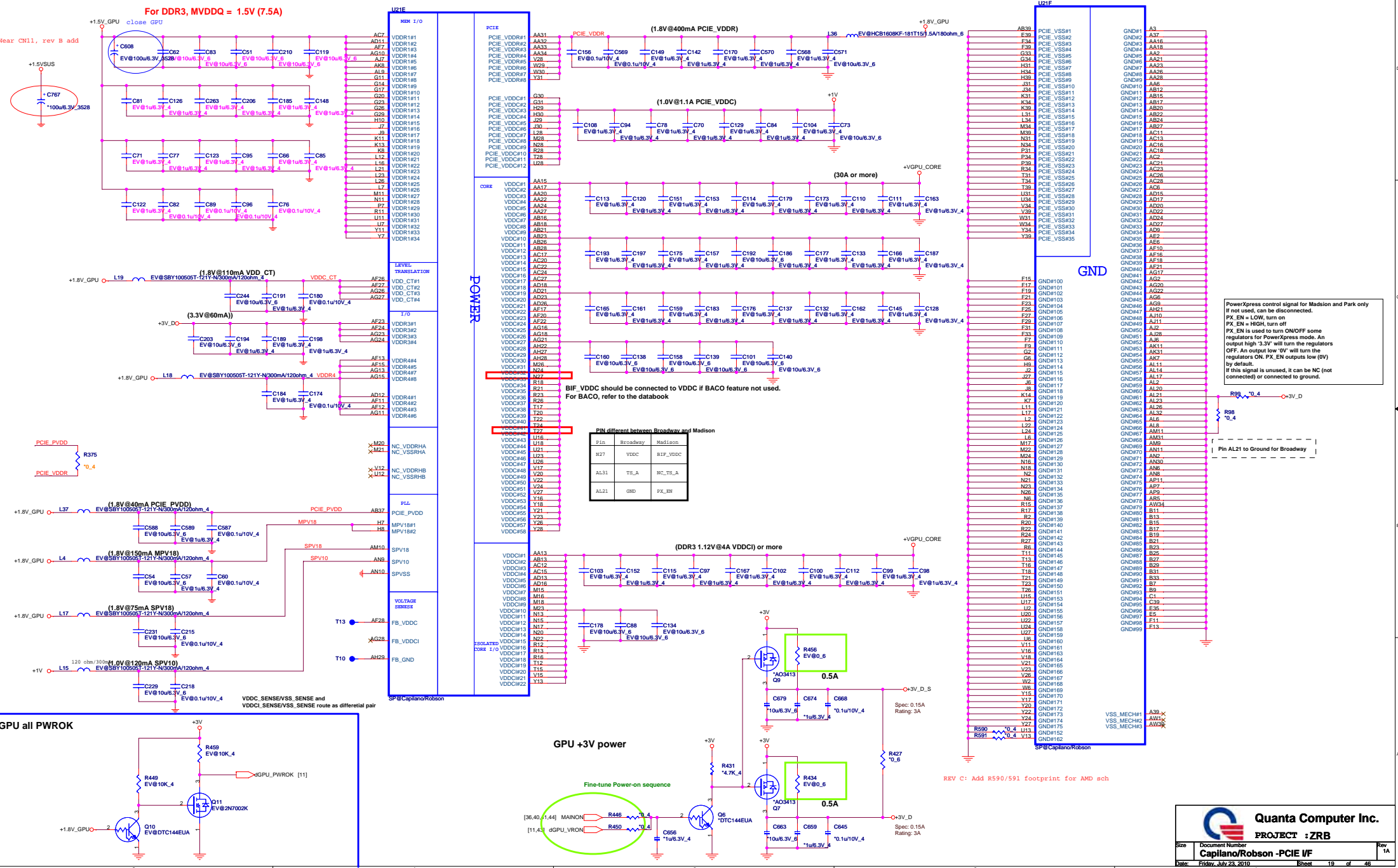
3.3V GPIO



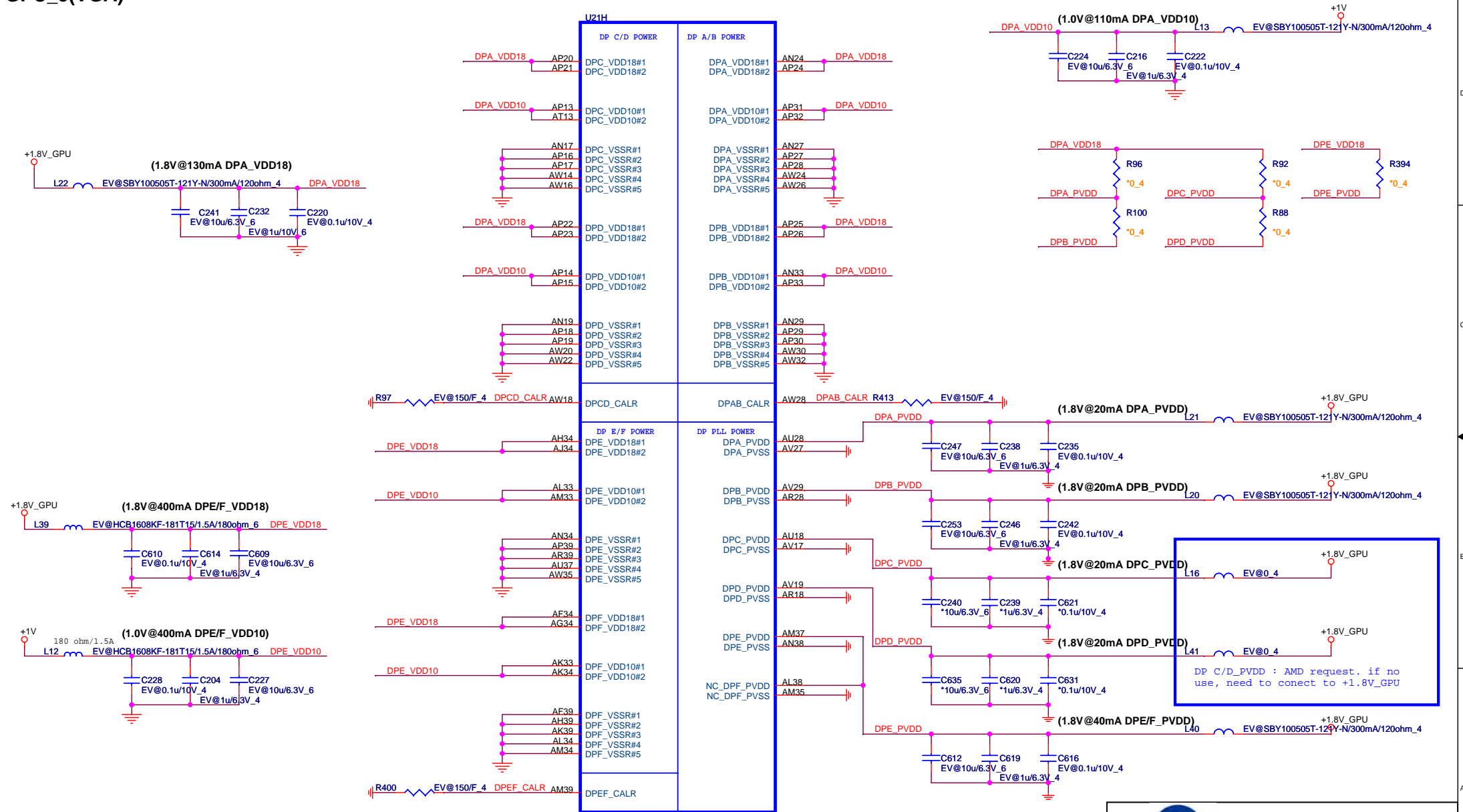
-] DDC AUX4 NC for Park_M2
-] LVDS
-] CRT
-] DDC AUX7 NC for Park_M2

SP@Caplano/Robson

GPU_4(VGA)



GPU_5(VGA)

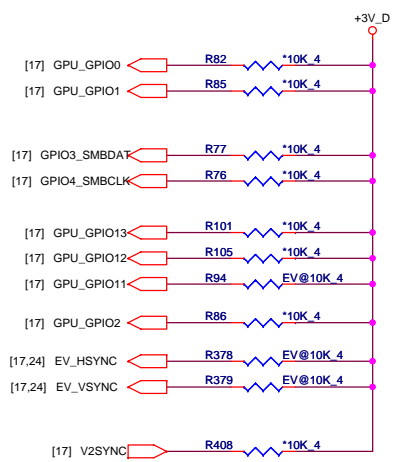


SP@Capilano/Robson

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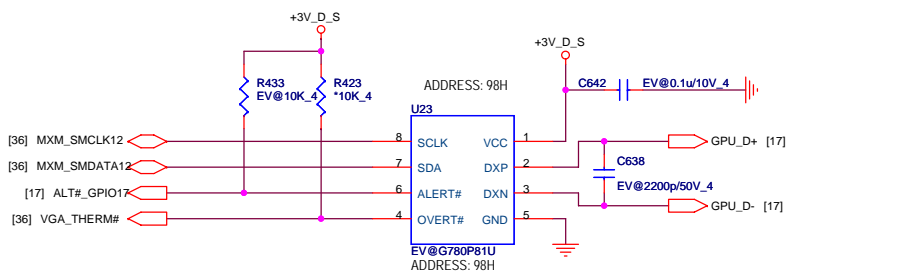
PIN STRAPS(VGA)



Size of the primary memory apertures	GPIO[13:11]
128 MB	000
256MB	001
64 MB	010
32 MB	011
More than 512 MB	Not Supported

CONFIGURATION STRAPS				
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET				
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	0	
ROMIDCFG[2:0]	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	001	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

Thermal Sensor(VGA)

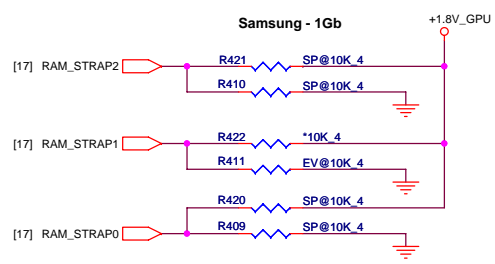


Vendor	P/N
WINDBOND	AL83L771K01
GMT	AL000780000

USD0.16

DDR3 Memory Aperture size(GPU)

DDR3 Memory size					
Vendor	Vendor P/N	STN B/S P/N	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix			1	1	0
	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	1	0	0
	H5TQ2G63BFR-12C	AKD5MGGTW03 (128M*16)	1	0	1
Samsung			0	0	0
	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	0	0	0
	K4W2G1646B-HC12	AKD5MGGT500 (128m*16)	0	0	1
AMD			0	1	0
	23EY2387MA12-SZ	AKD5LGGT700	0	1	0



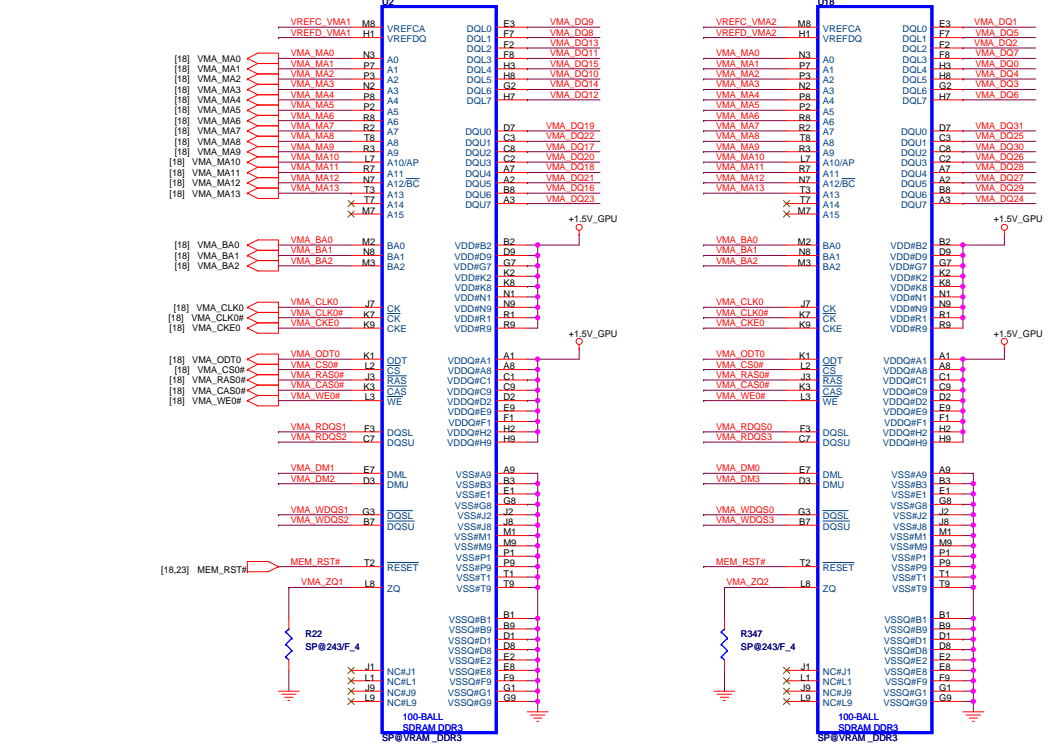
RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

Quanta Computer Inc.
PROJECT : ZRB

Size Document Number Strip/Thermal Rev 1A
Date: Wednesday, July 21, 2010 Sheet 21 of 46

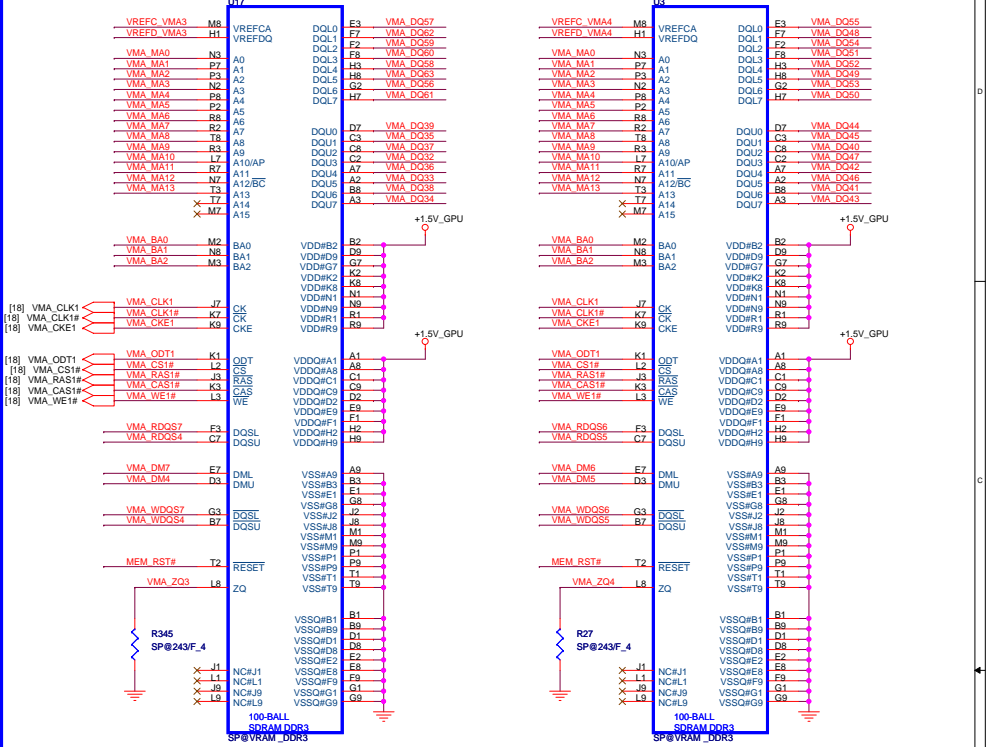
Maintenance and Service Guide, Service Manual, Motherboard Schematics for Laptop/notebook <http://mycomp.su/x/>
CHANNEL A: 512MB DDR3 (64M*16*4pcs)

- [18] VMA_DQ[63..0] VMA_DQ[63..0]
 - [18] VMA_DM[7..0] VMA_DM[7..0]
 - [18] VMA_RDQS[7..0] VMA_RDQS[7..0]
 - [18] VMA_WDQS[7..0] VMA_WDQS[7..0]
- QSA[7..0]
QSA#[7..0]



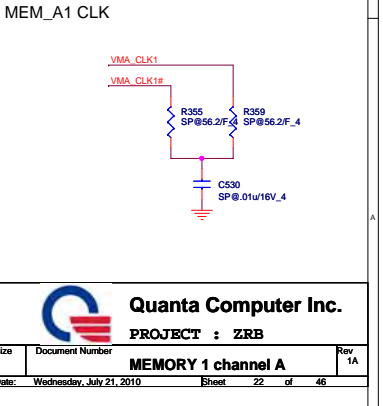
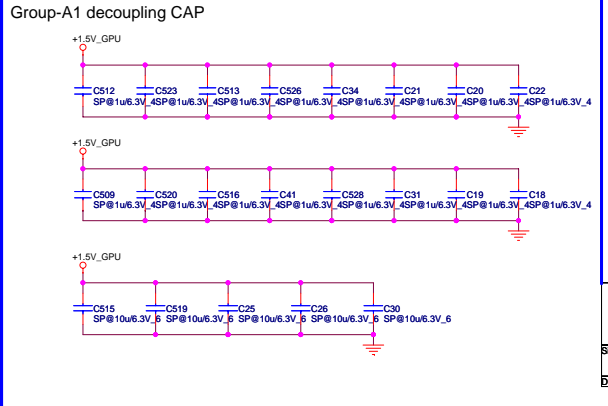
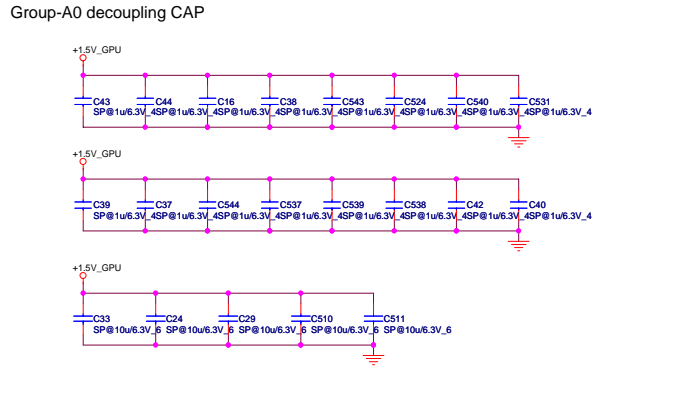
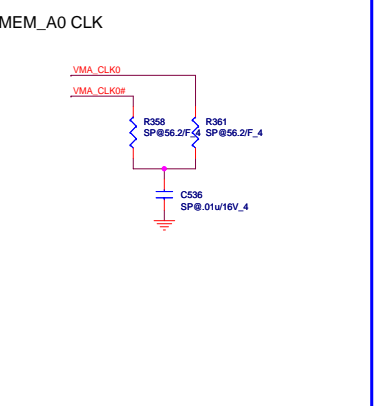
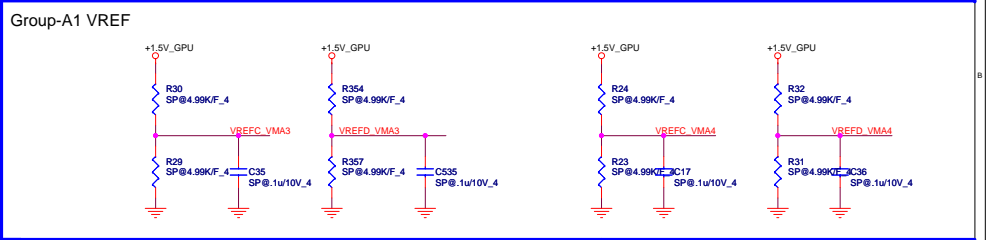
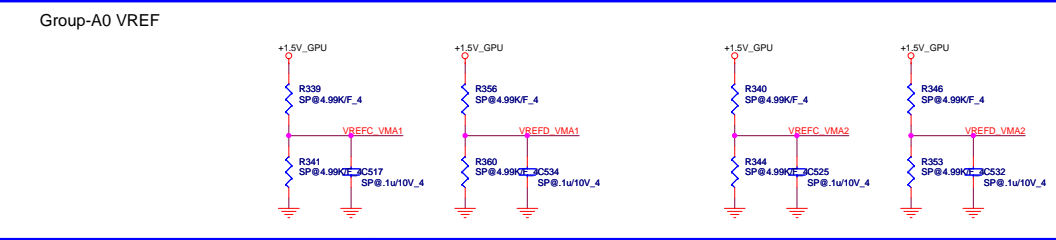
TOP Left

BOT Left



BOT Right

TOP Right



Quanta Computer Inc.
PROJECT : ZRB

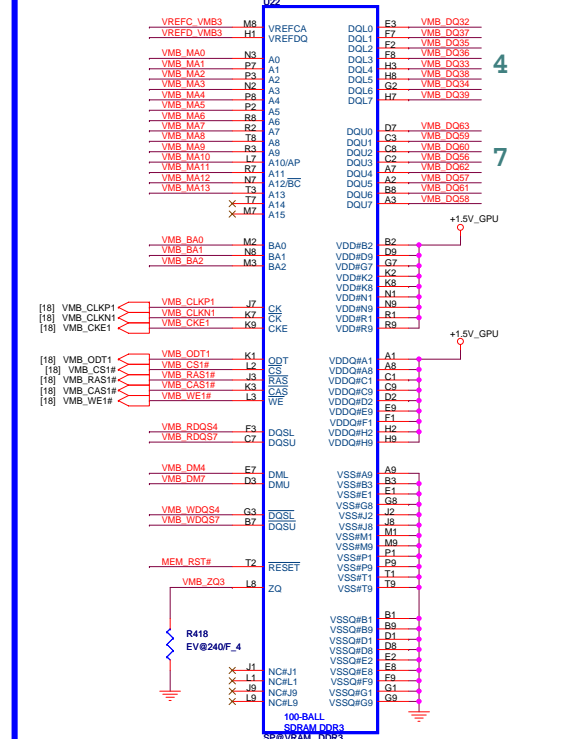
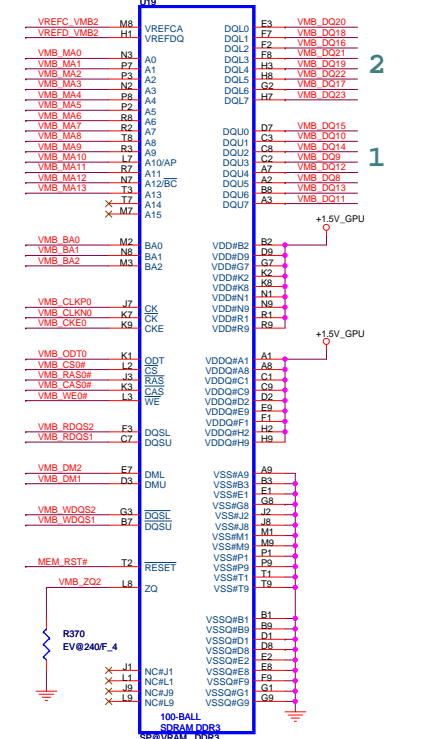
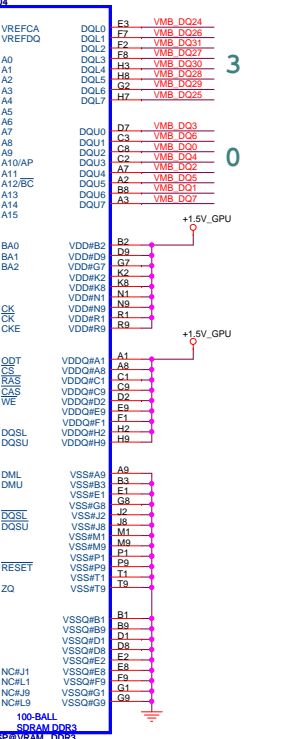
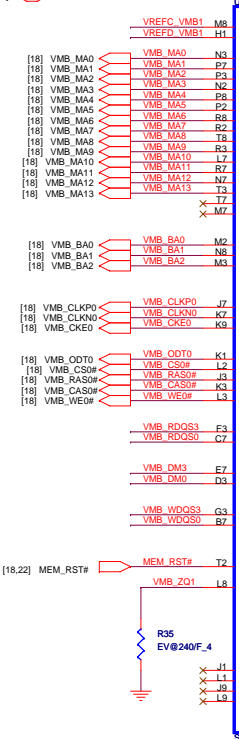
Size	Document Number	MEMORY 1 channel A	Rev
Date: Wednesday, July 21, 2010	Sheet	22	of 46

CHANNEL B: 512MB DDR3 (16*64M 4pcs)

Park, M92M Use Channel B Memory Interface Only

- [18] VMB_DO[63..0] VMB DO[63..0]
- [18] VMB_DM[7..0] VMB DM[7..0]
- [18] VMB_RDOS[7..0] VMB RDOS[7..0]
- [18] VMB_WDOS[7..0] VMB WDOS[7..0]

QSA#7..0
QSA#17..0



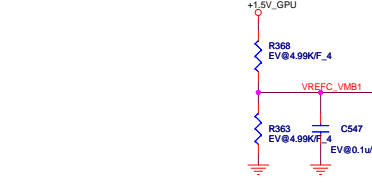
BOT Down

TOP Down

TOP Up

BOT Up

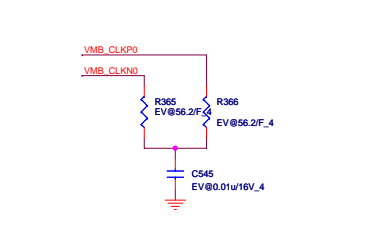
Group-B0 VREF



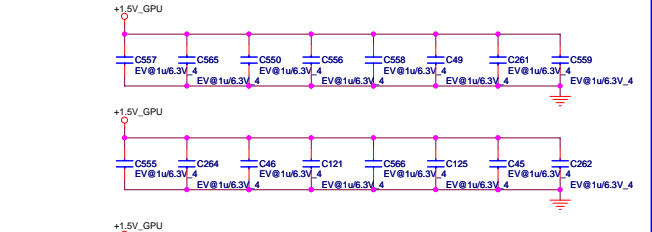
Group-B1 VREF



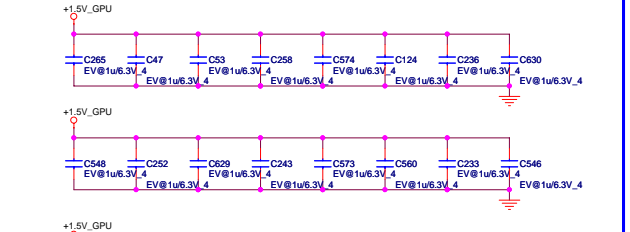
MEM_B0 CLK



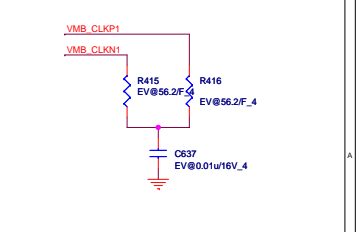
Group-B0 decoupling CAP



Group-B1 decoupling CAP



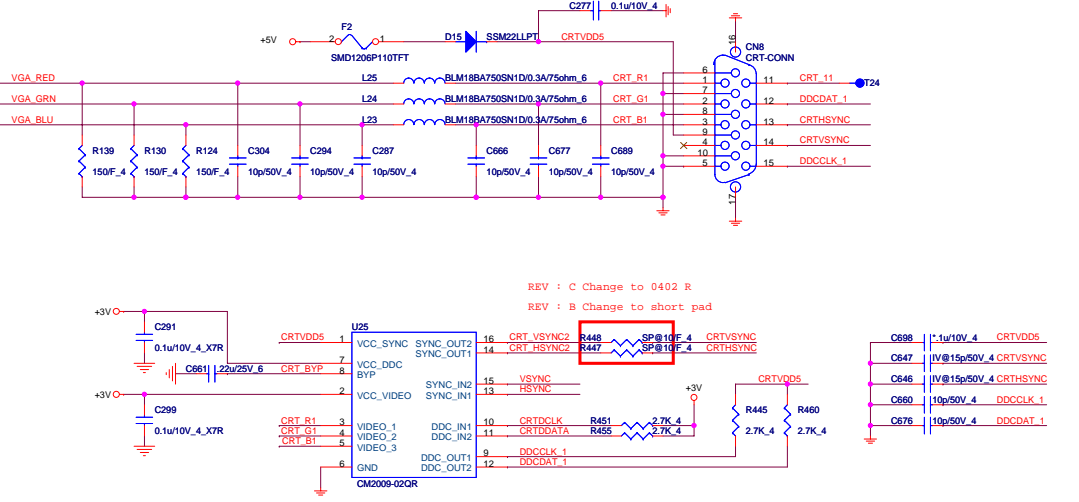
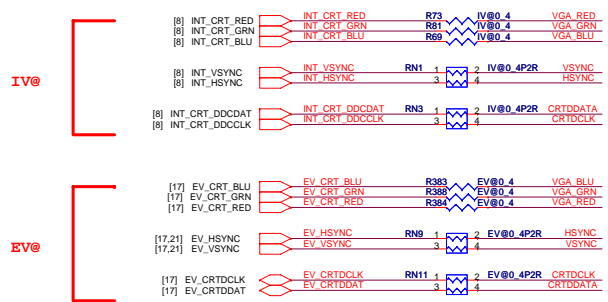
MEM_B1 CLK



CRT Switch

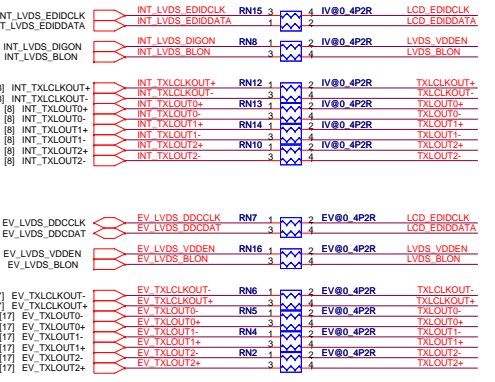
CRT

0_ohm Resistor place close to Joint-Point

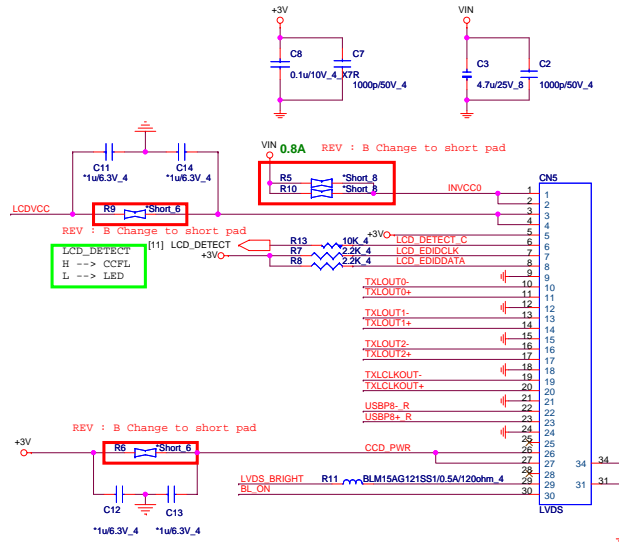


LVDS

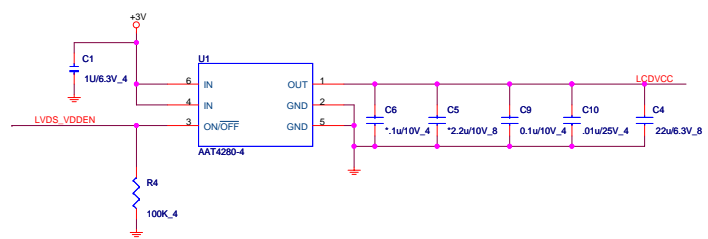
0_ohm Resistor place close to Joint-Point



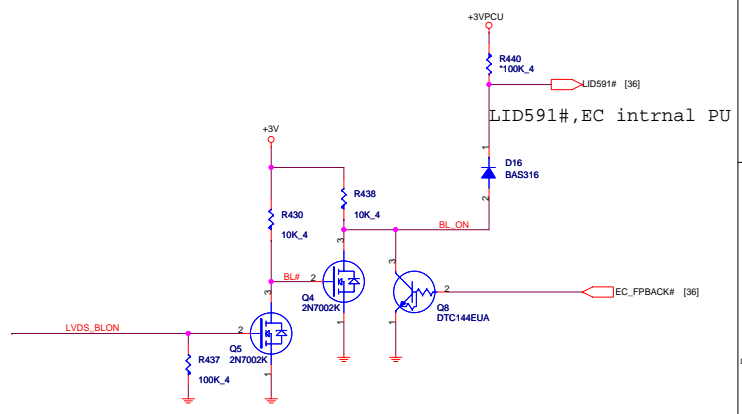
LVDS



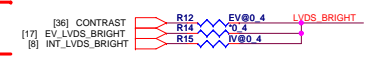
LCD Power



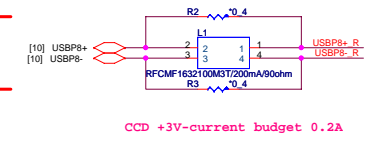
Backlight Control



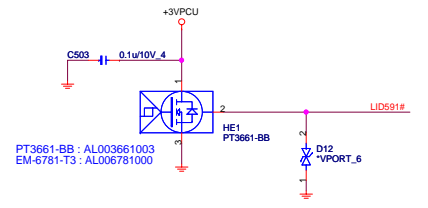
LVDS_BRIGHT



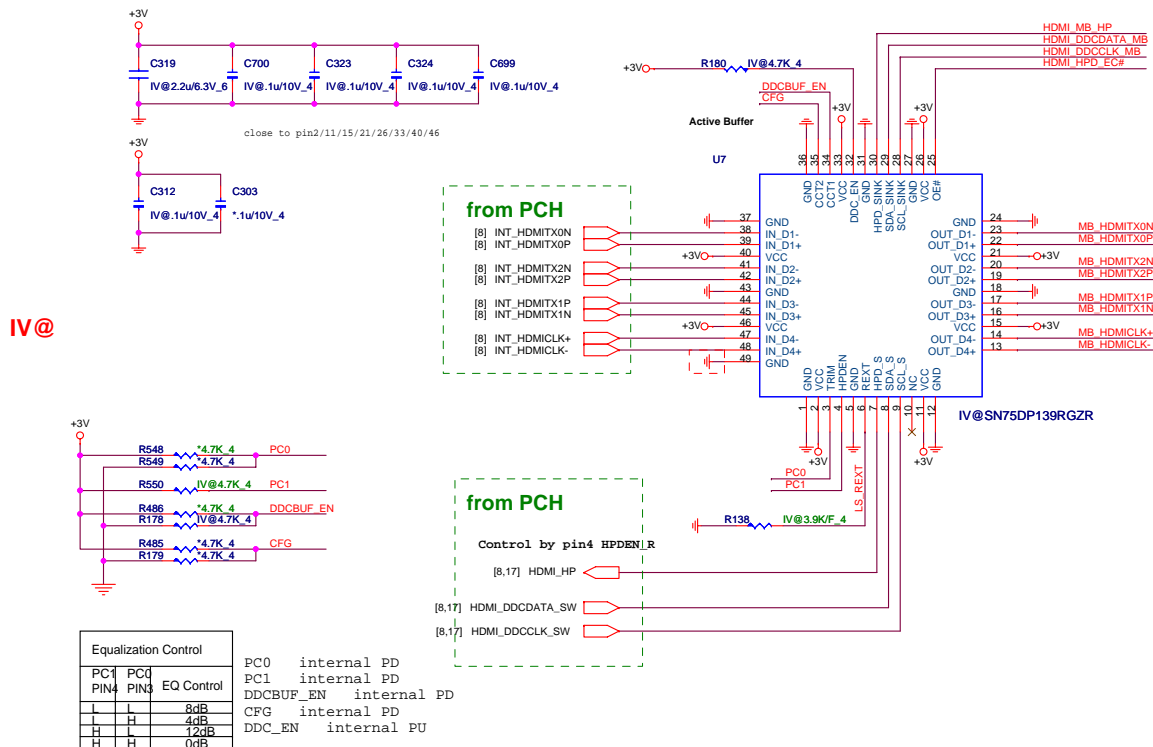
CCD-USB



Lid Switch (Hall sensor)



HDMI LEVEL SHIFTER

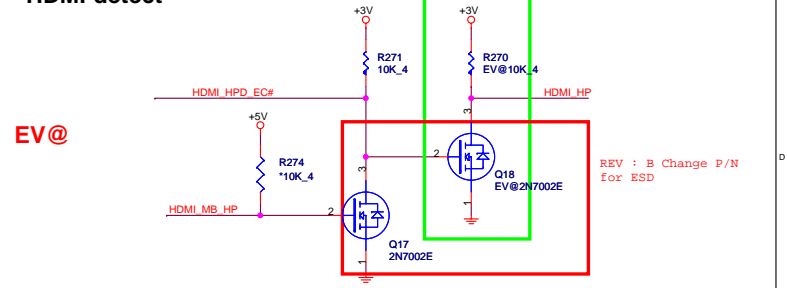


Equalization Control

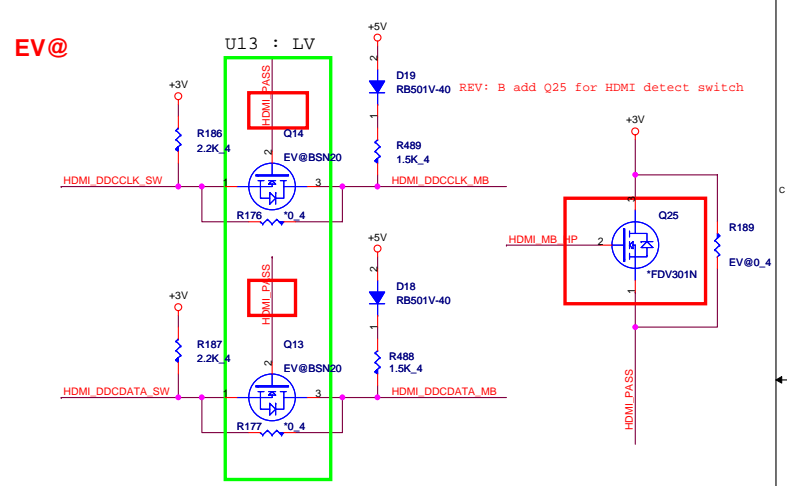
PC0	PC1	EQ Control
L	L	8dB
H	H	4dB
L	H	12dB
H	H	0dB

PC0 internal PD
 PC1 internal PD
 DDCBUF_EN internal PD
 CFG internal PD
 DDC_EN internal PU

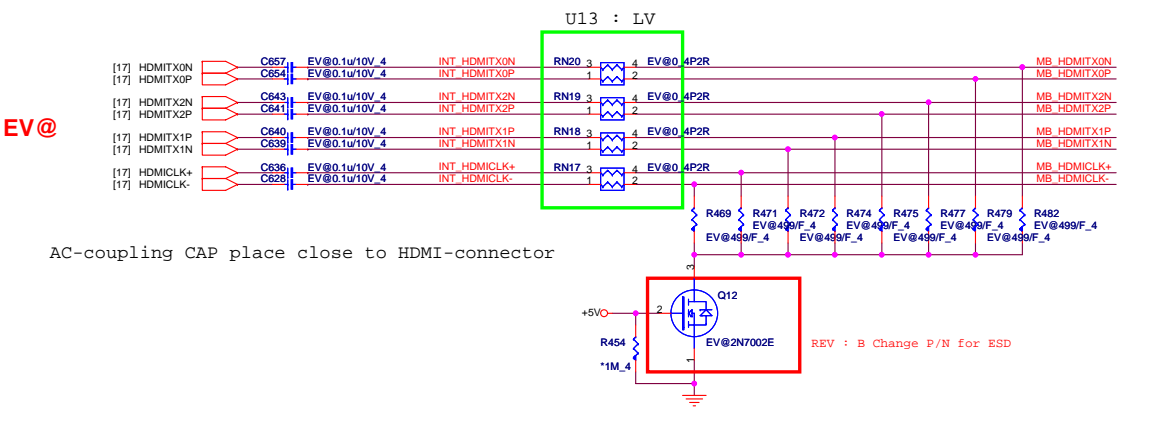
HDMI-detect



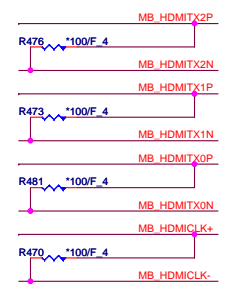
I2C



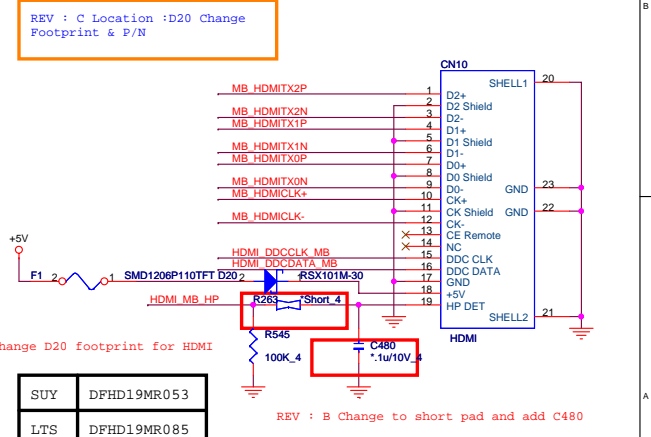
Switchable Graphic HDMI source



EMI

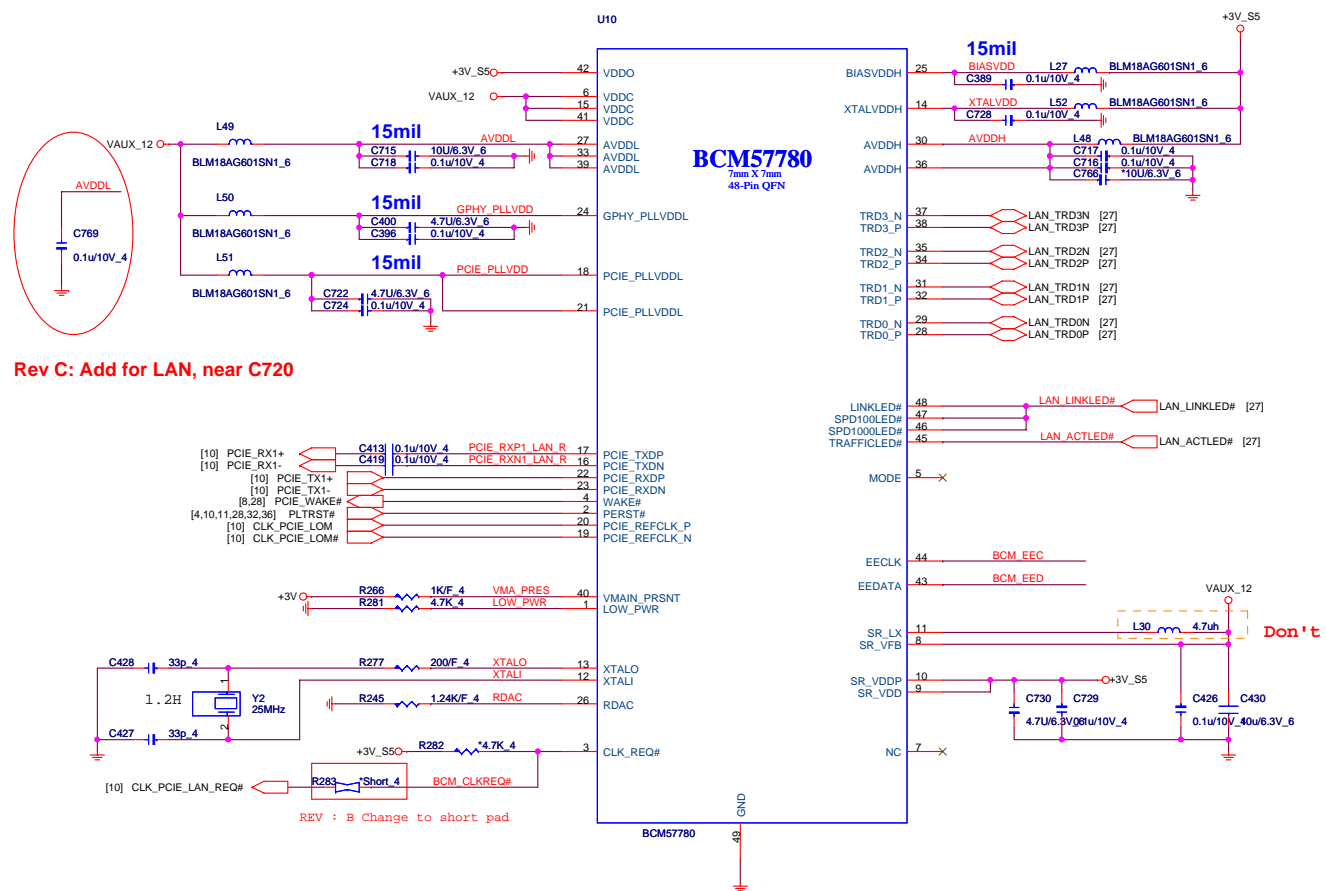


HDMI connector



SUY	DFPHD19MR053
LTS	DFPHD19MR085

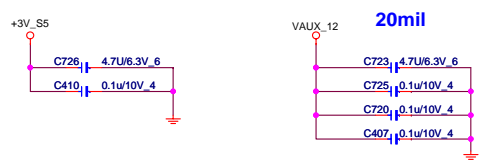
Giga-LAN BCM57780



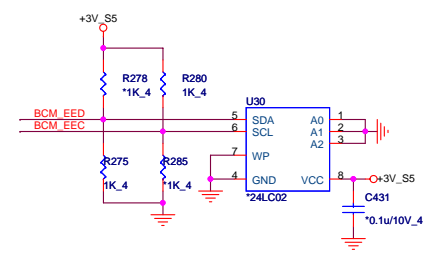
Rev C: Add for LAN, near C720

REV : B Change to short pad

LAN POWER



EEPROM

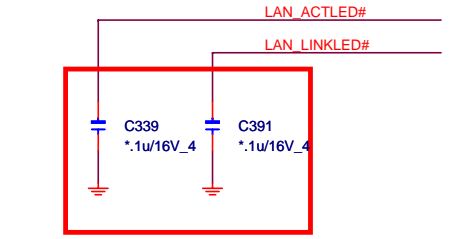
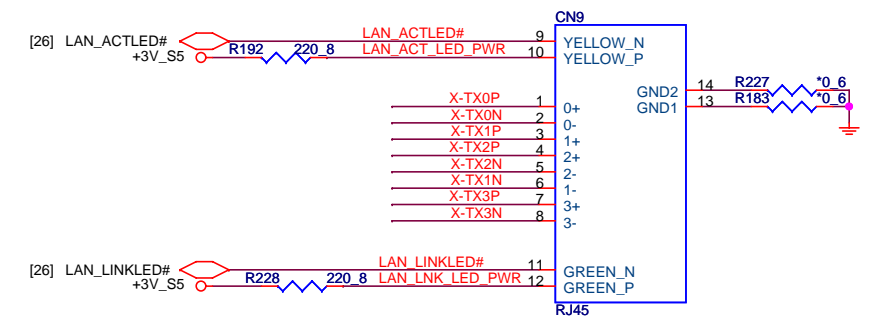
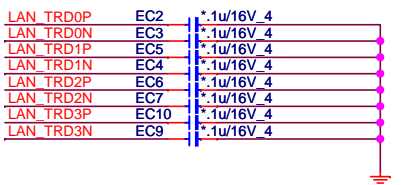
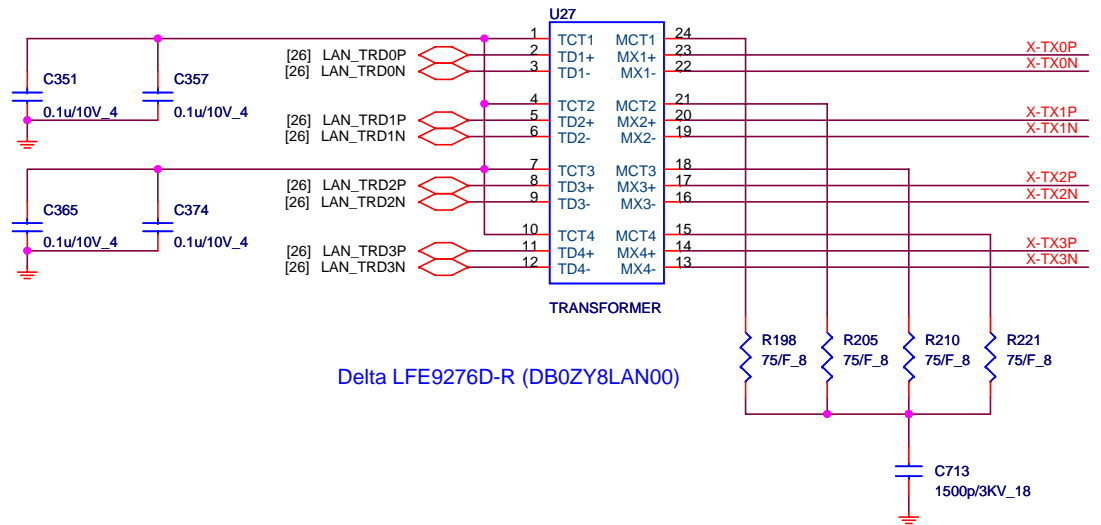


EEPROM Strapping


EEPROM Type	EECLK	EEDATA
24LC02	1	1
Internal	1	0

TRANSFORMER

SUY	DFTJ12FR109
AEC	DFTJ12FR135



REV : B Change to 0402 for ESD



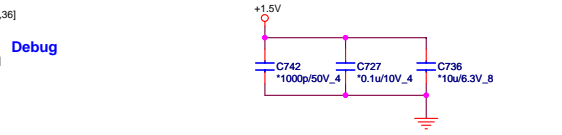
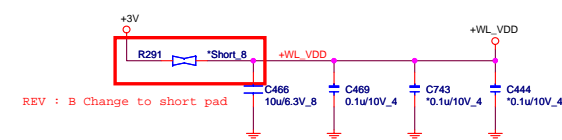
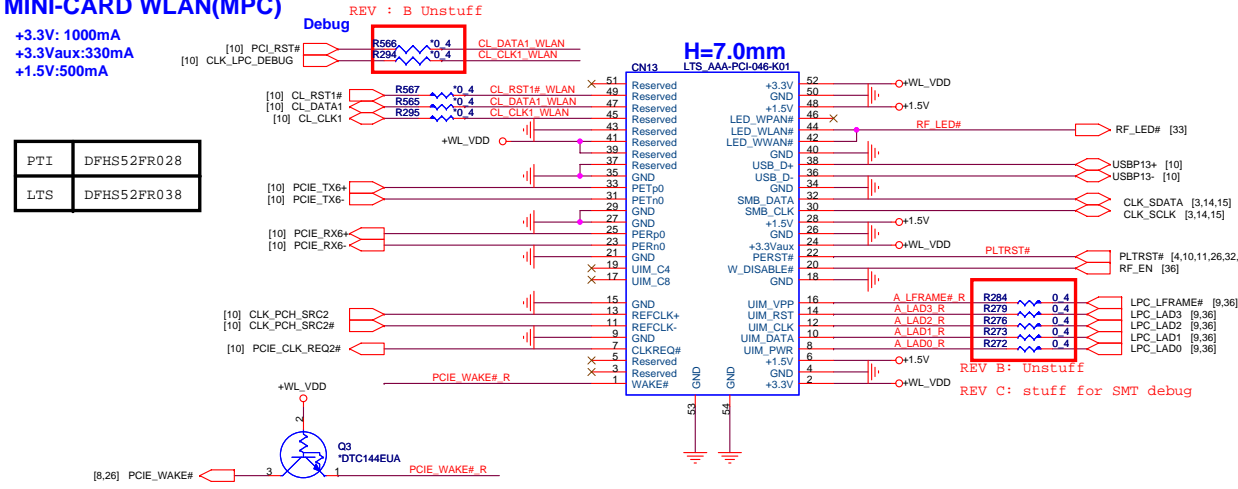
Quanta Computer Inc.
PROJECT : ZRB

Size	Document Number	Rev
	LAN Transformer and RJ45	1A
Date:	Thursday, July 22, 2010	Sheet 27 of 46

MINI-CARD WLAN(MPC)

+3.3V: 1000mA
 +3.3Vaux: 330mA
 +1.5V: 500mA

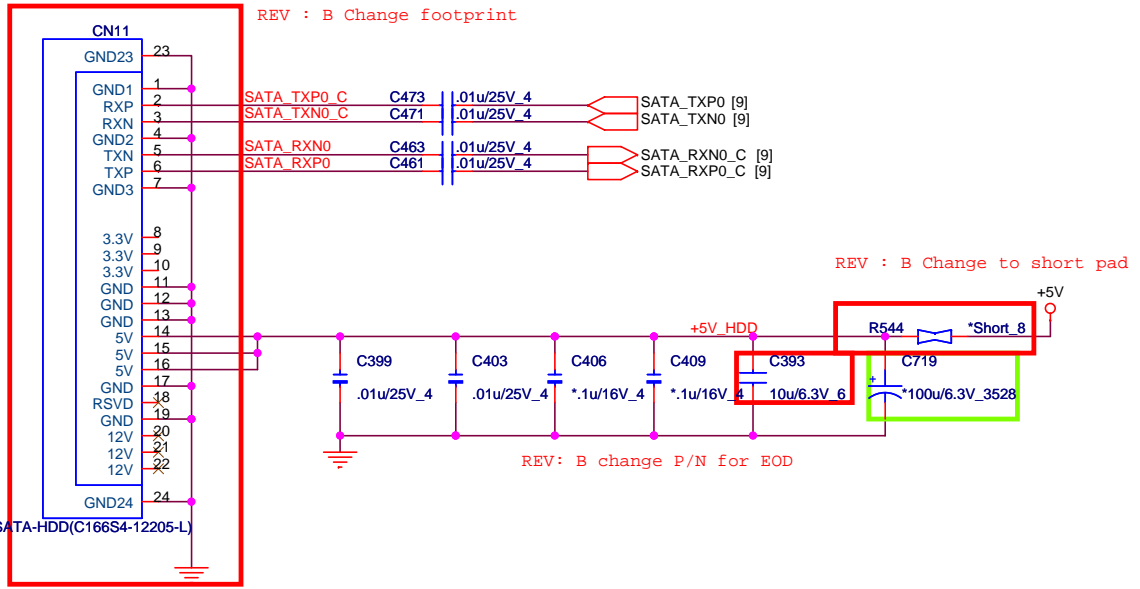
PTI	DFHS52FR028
LTS	DFHS52FR038



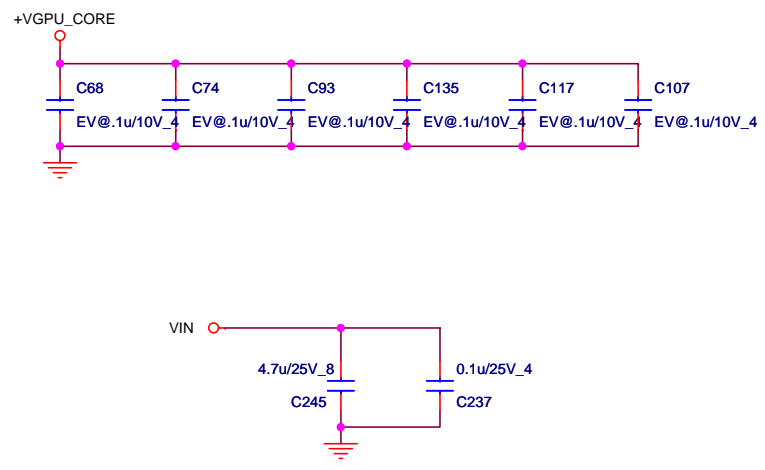
Quanta Computer Inc.
 PROJECT : ZRB

Size	Document Number	Rev
	MINI PCI-E card/TV	1A
Date:	Friday, July 23, 2010	Sheet 28 of 46

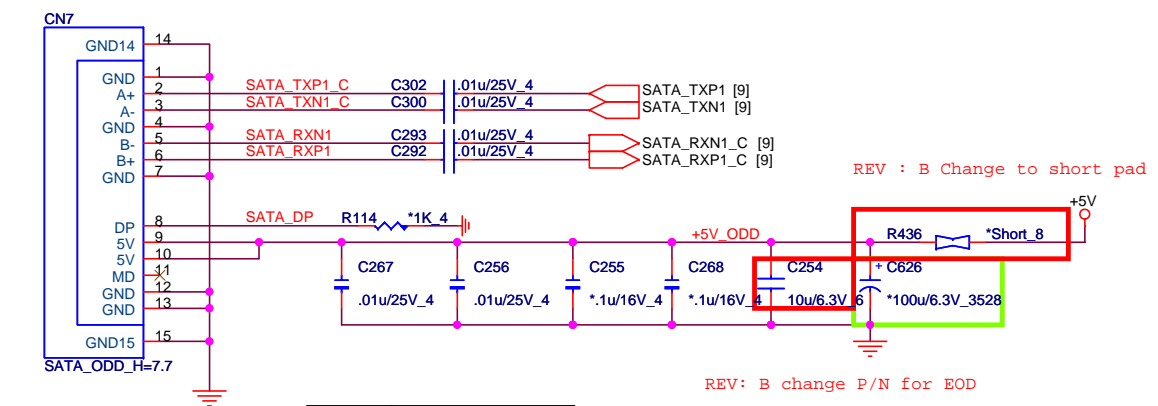
MAIN SATA HDD



EE RETURN-PATH CAPACITORS



ODD (SATA)



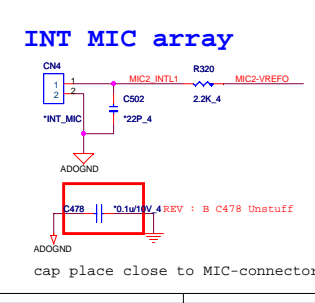
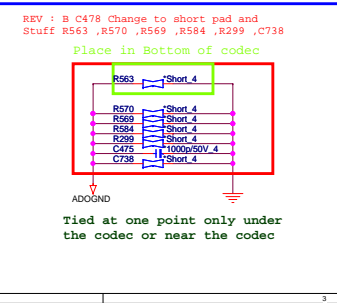
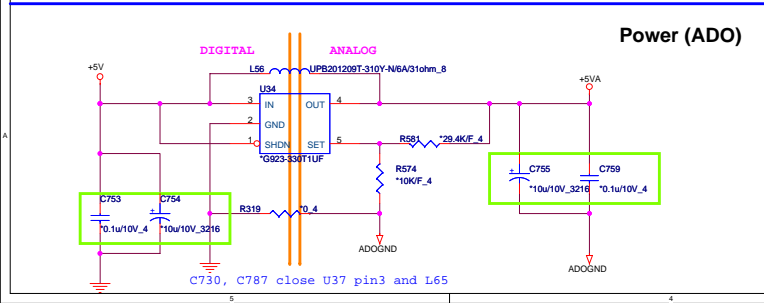
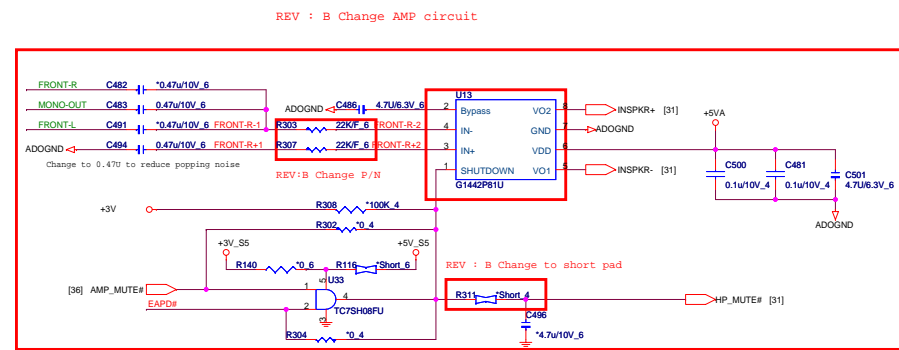
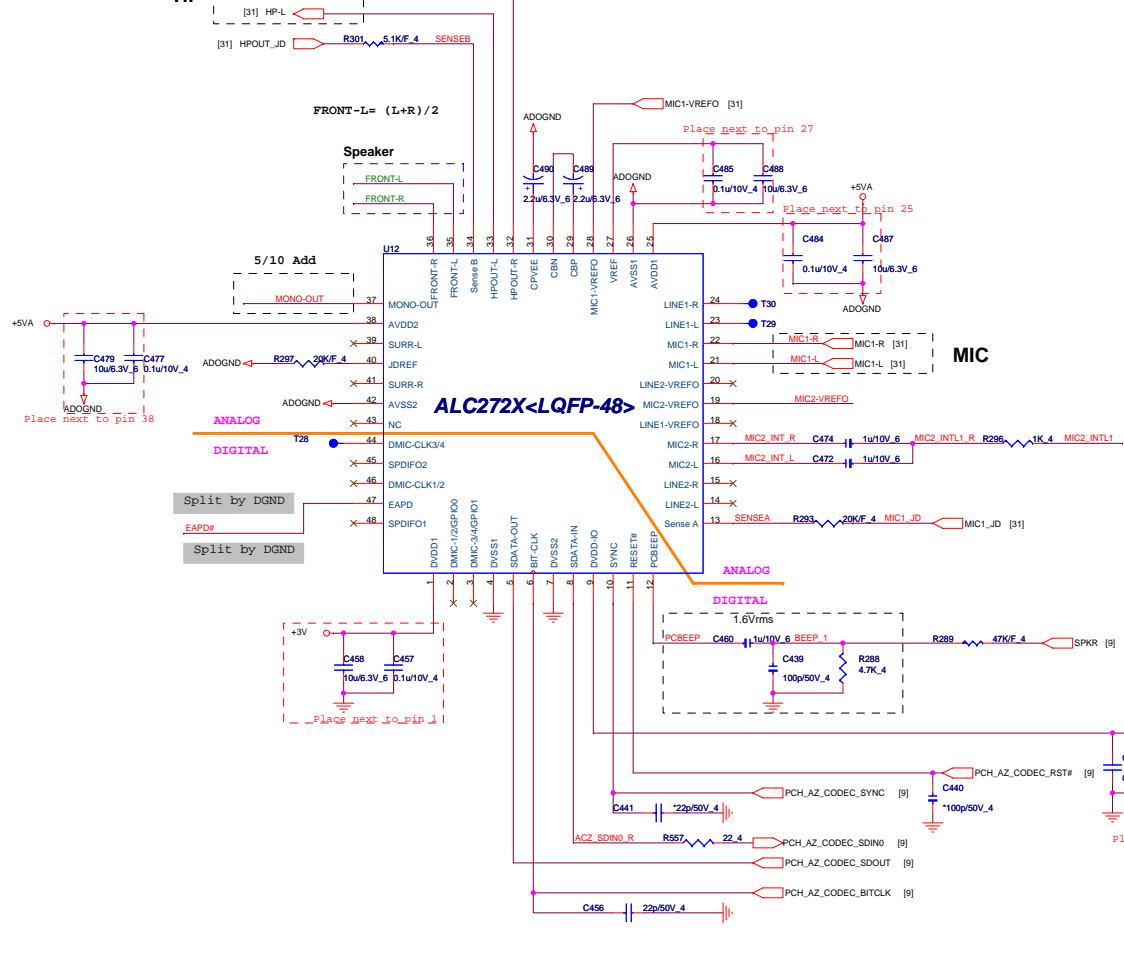
SUY	DFHS22FR214
AOP	DFHS22FR232
AEC	DFHS22FR216

AOP	DFHS13FR011
OTK	DFHS13FR010

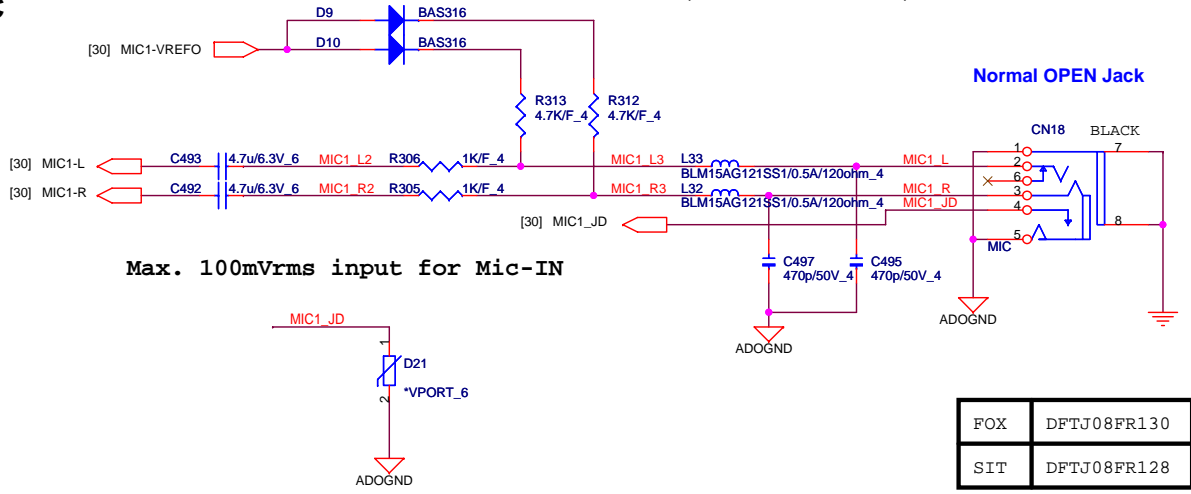
Quanta Computer Inc.

PROJECT : ZRB

Size	Document Number	Rev
	SATA-HDD/ODD/RETURN-PATH	1A
Date:	Wednesday, July 21, 2010	Sheet 29 of 46

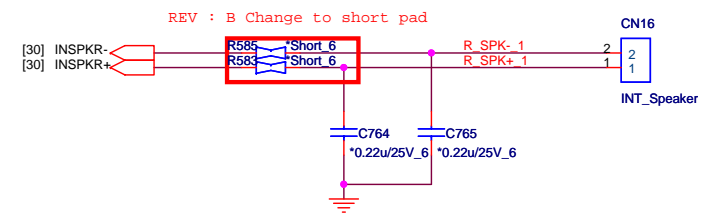


MIC



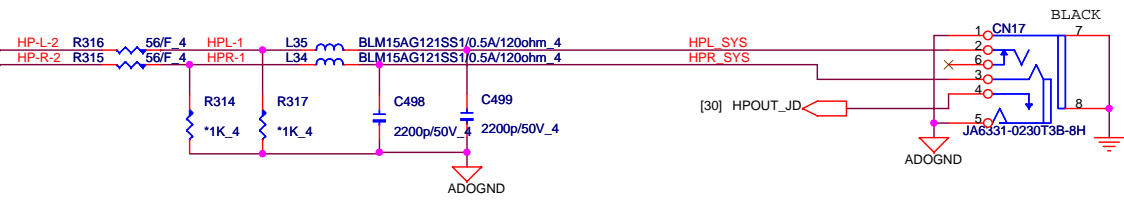
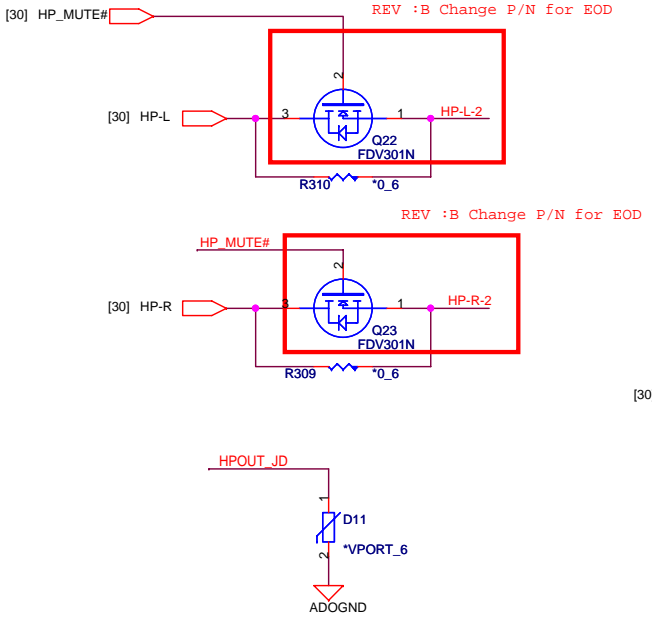
FOX	DFTJ08FR130
SIT	DFTJ08FR128

Internal Speaker

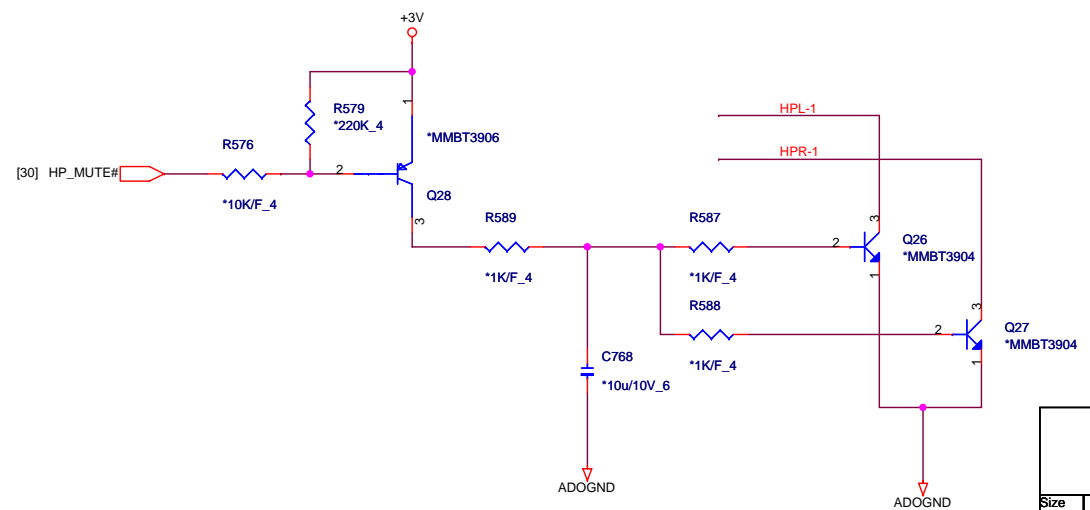


ACS	DFHD02MR311
PTI	DFHD02MR508

HP/SPDIF



De-pop noise

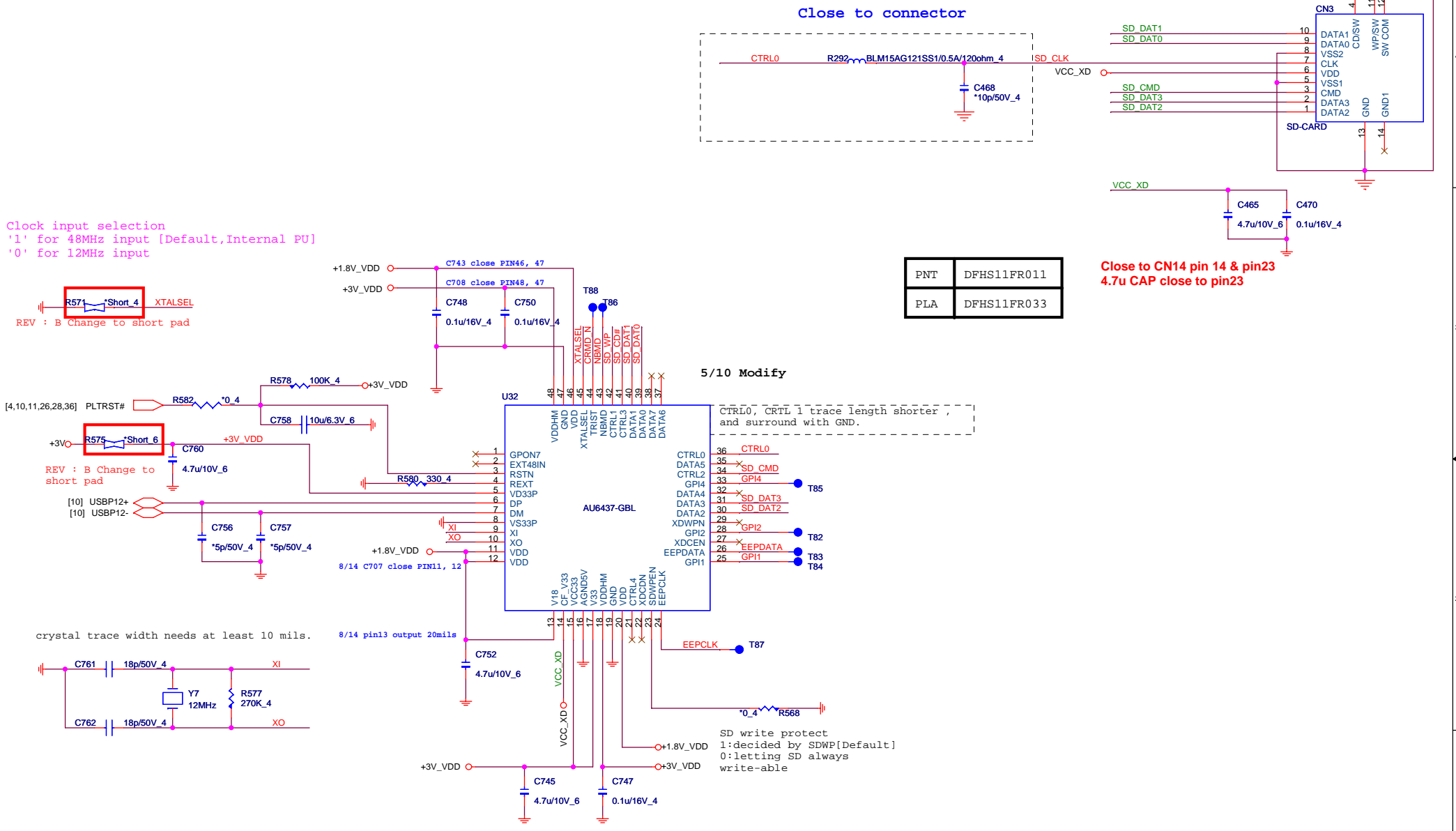


Quanta Computer Inc.
PROJECT : ZRB
AMP /AUDIO JACK CONN

Size	Document Number	Rev
		1A
Date:	Wednesday, July 21, 2010	Sheet 31 of 46

CARD READER Controller

2 IN 1 CARD READER (SD/MMC)



PNT	DFHS11FR011
PLA	DFHS11FR033

Close to CN14 pin 14 & pin23
4.7u CAP close to pin23

Clock input selection
'1' for 48MHz input [Default, Internal PU]
'0' for 12MHz input

REV : B Change to short pad

REV : B Change to short pad

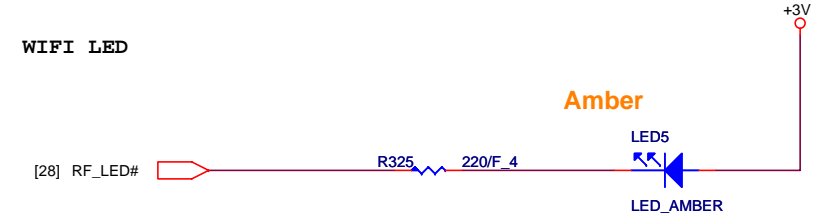
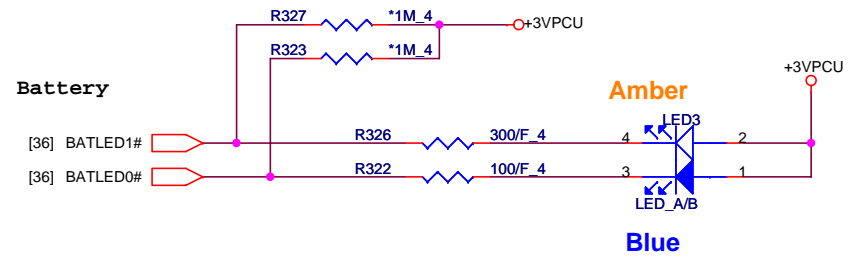
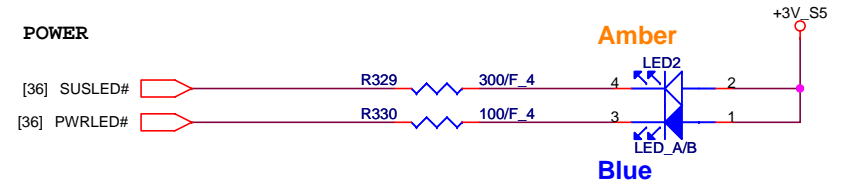
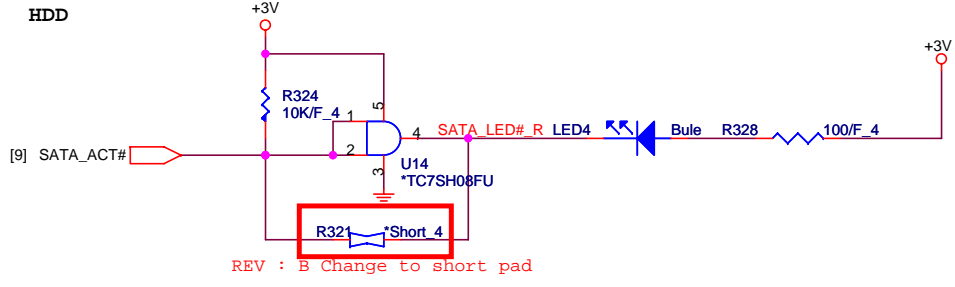
crystal trace width needs at least 10 mils.


CTRL0, CTRL1 trace length shorter,
and surround with GND.

SD write protect
1:decided by SDWP[Default]
0:letting SD always
write-able

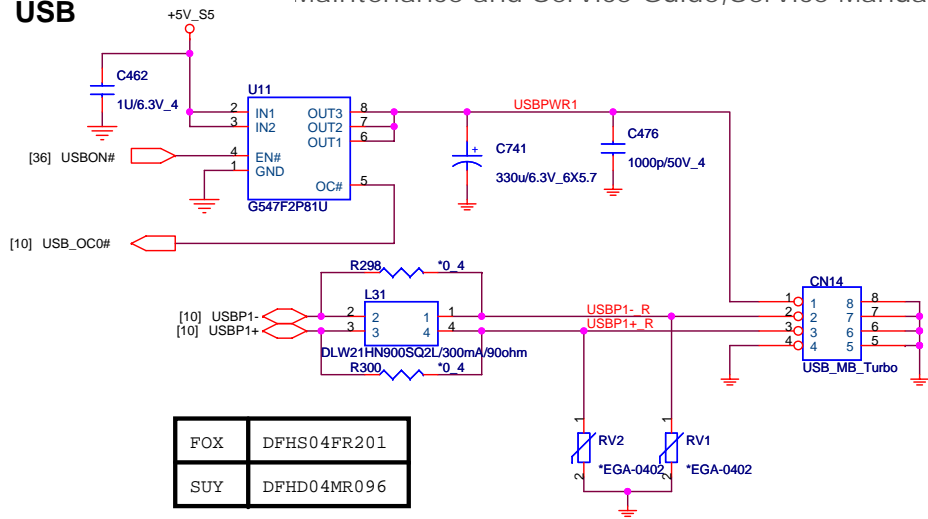
	PROJECT : ZQ5 Quanta Computer Inc.	
	Size AU6433 CardReader	Document Number AU6433 CardReader
Date: Wednesday, July 21, 2010		Sheet 32 of 43

LED

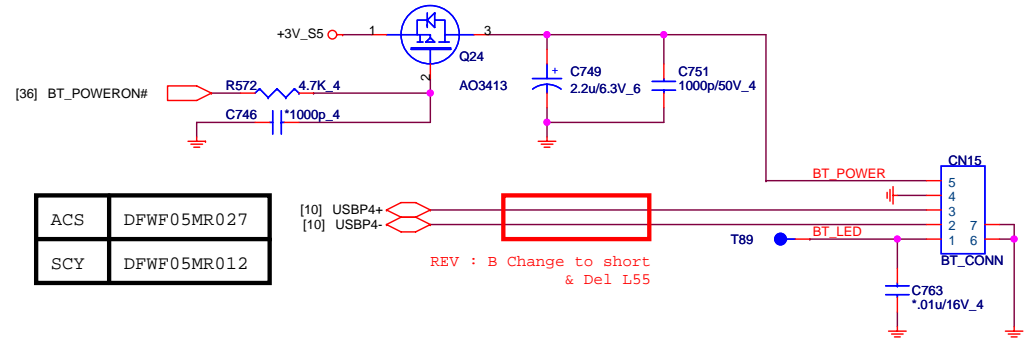


 Quanta Computer Inc. PROJECT : ZRB		Size	Document Number	Rev
				1A
Date: Monday, July 26, 2010		Sheet 33 of 46		

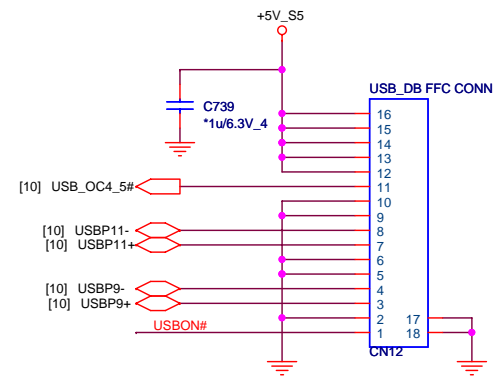
USB



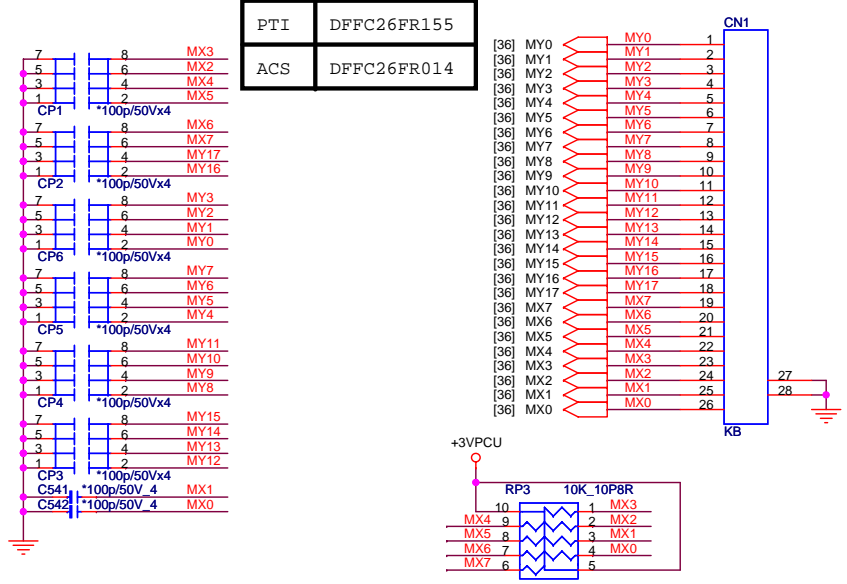
BLUETOOTH CONNECTOR



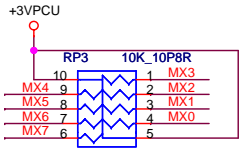
USB/B



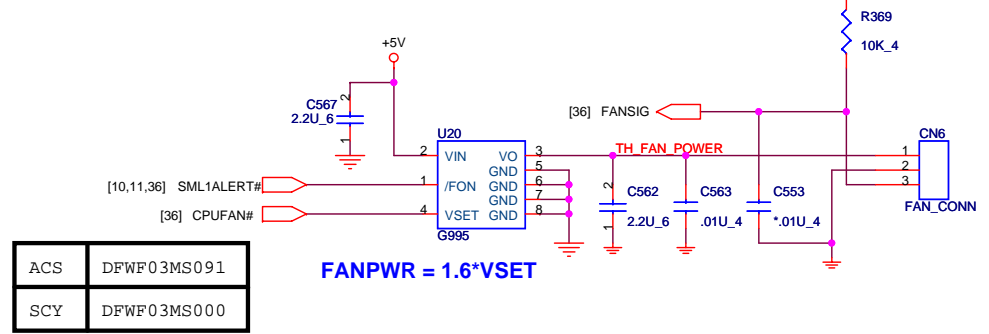
K/B



PTI	DFFC26FR155
ACS	DFFC26FR014



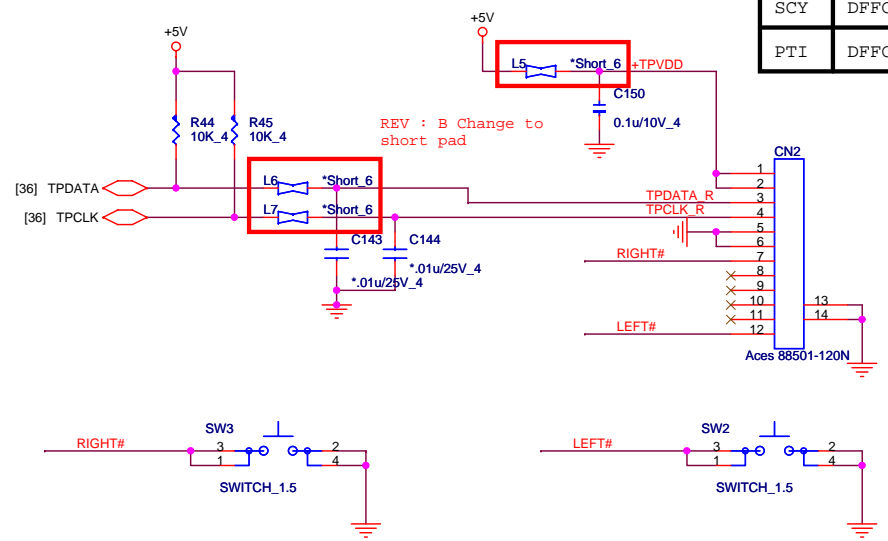
CPU FAN



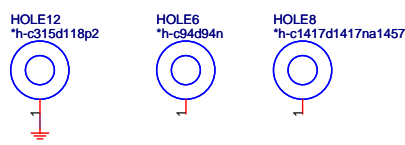
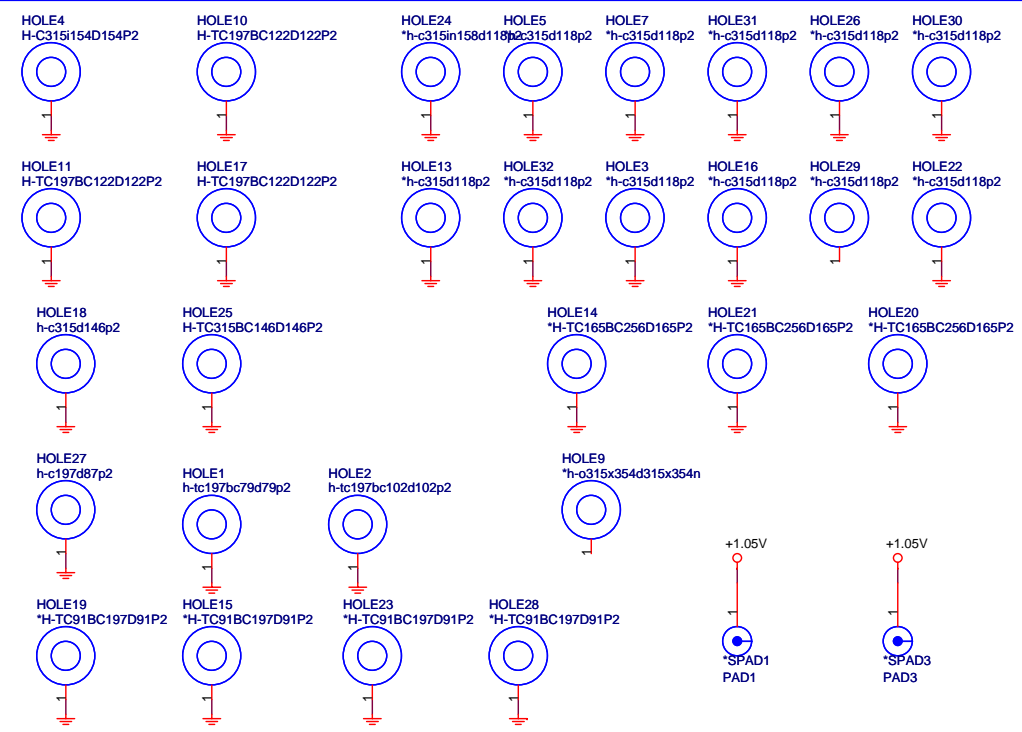
ACS	DFWF03MS091
SCY	DFWF03MS000

FANPWR = 1.6*VSET

TOUCHPAD & Switch CONN.

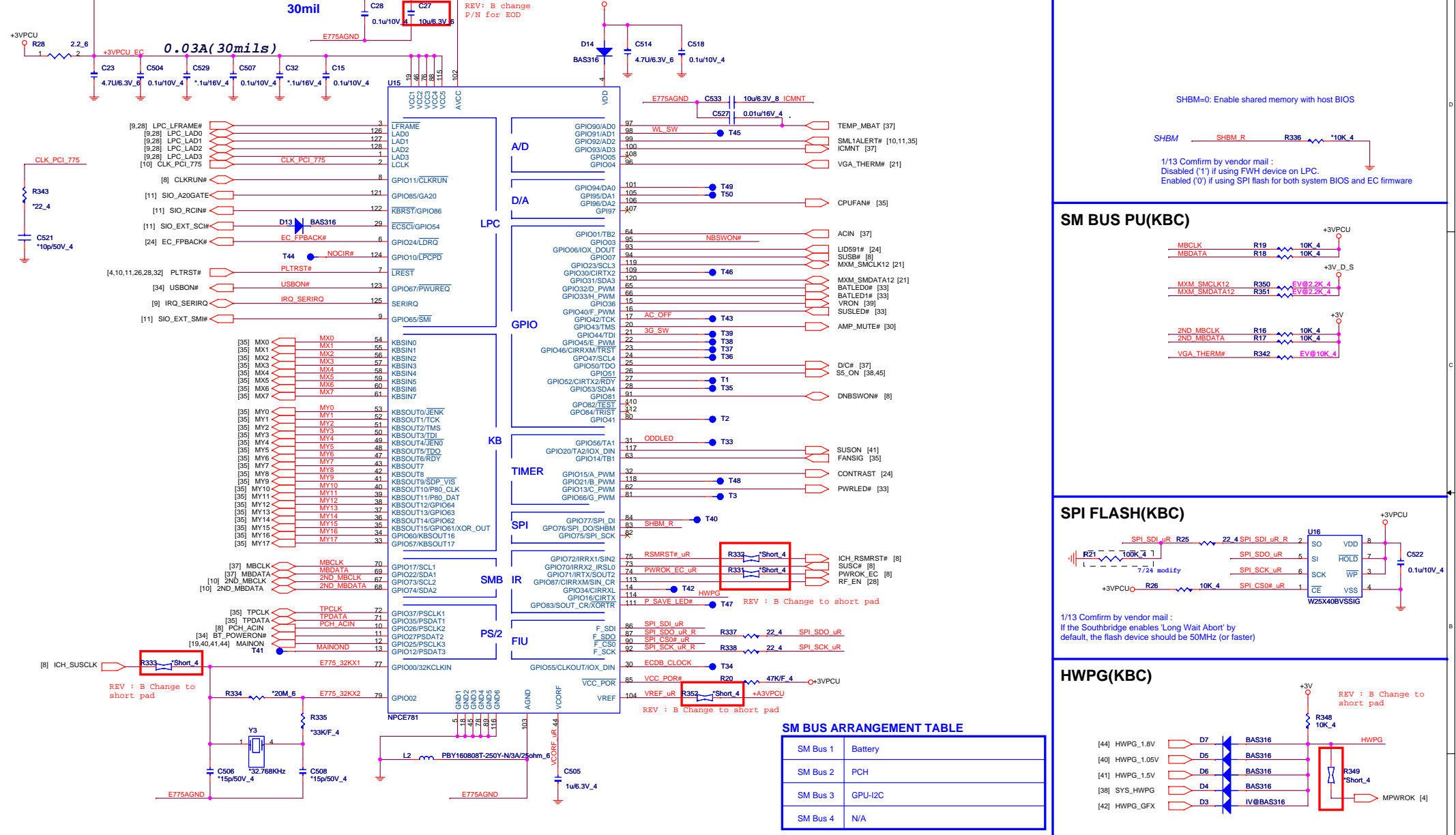


ACS	DFFC12FR017
SCY	DFFC12FR015
PTI	DFFC12FR234



Quanta Computer Inc.
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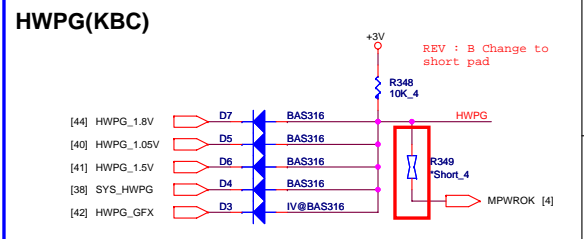
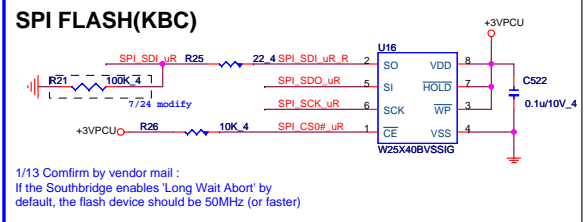
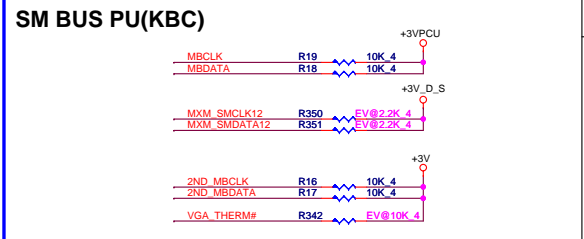
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	KB/FAN/TP+FP	1A
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SHBM=0: Enable shared memory with host BIOS

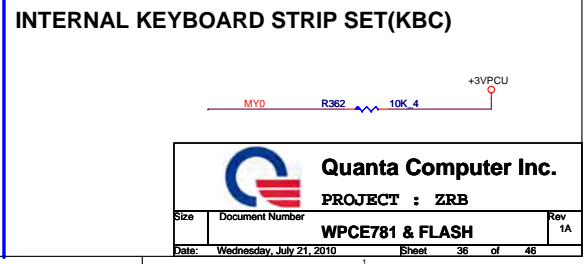
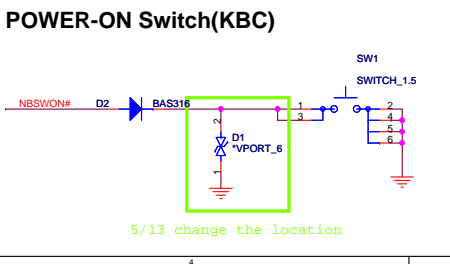
SHBM — SHBM_R — R336 — *10K_4

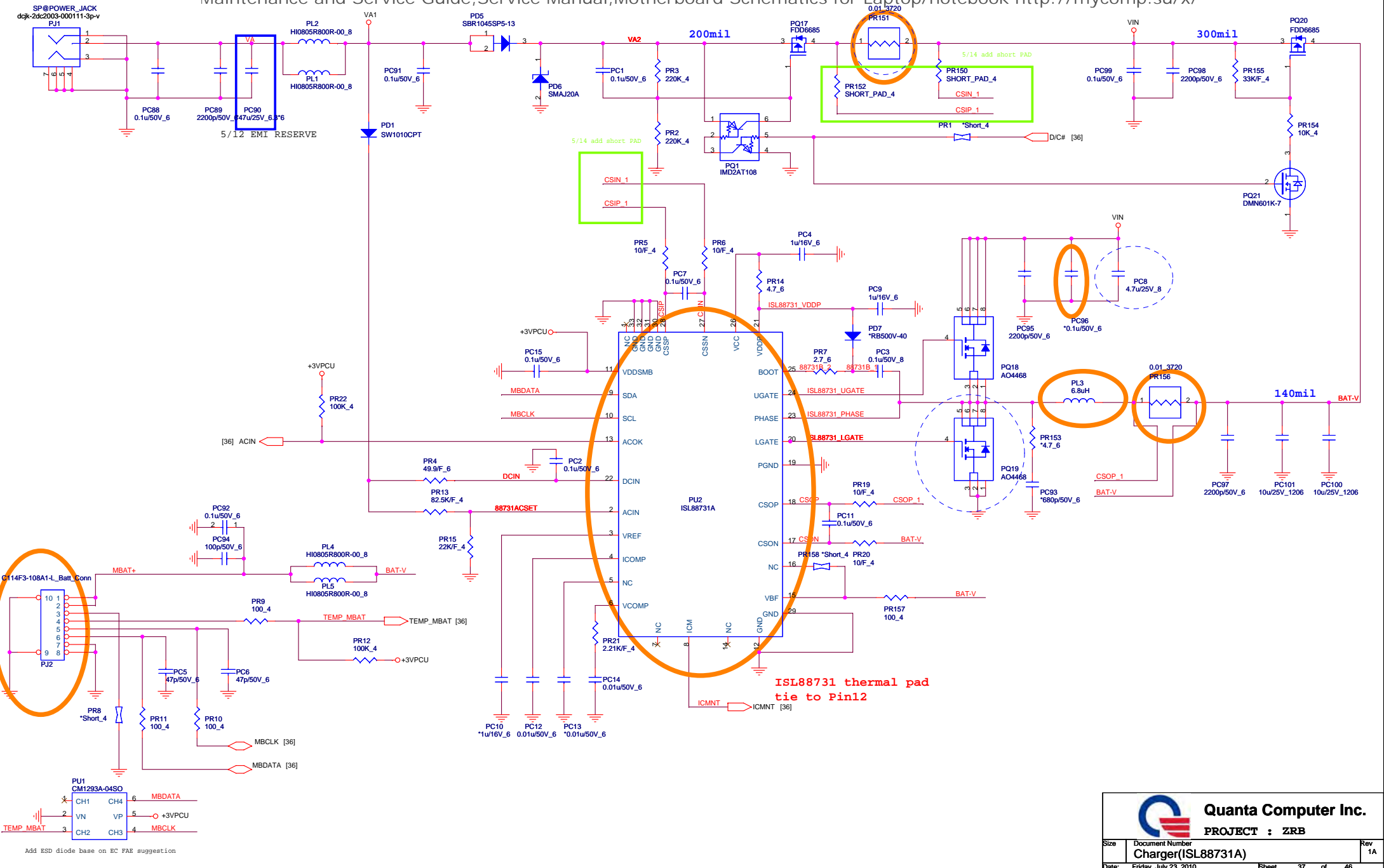
1/13 Confirm by vendor mail :
Disabled (*) if using FW device on LPC.
Enabled (0) if using SPI flash for both system BIOS and EC firmware




SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	GPU-I2C
SM Bus 4	N/A

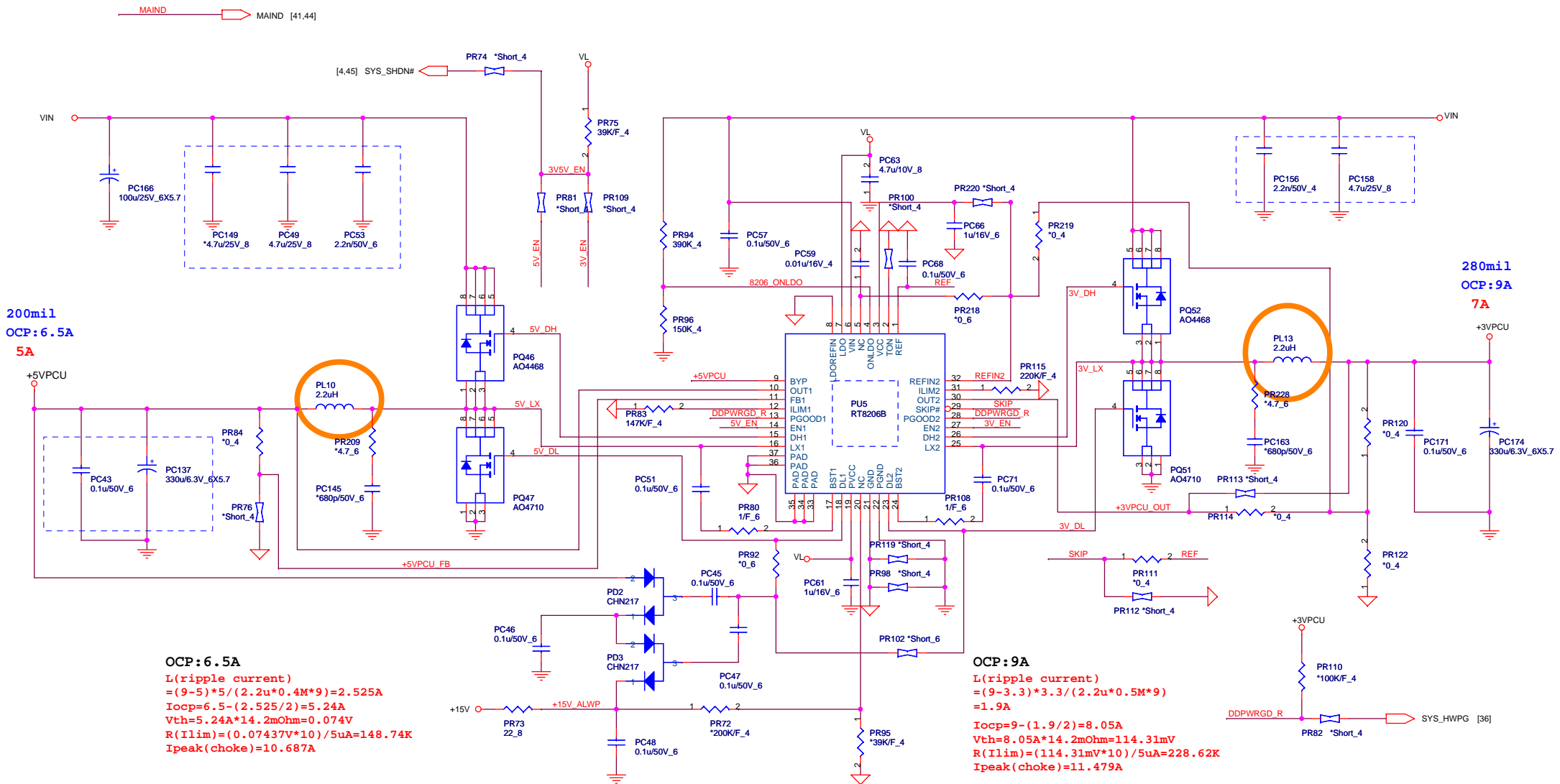




ISL88731 thermal pad tie to Pin12

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		Charger (ISL88731A)		
		Sheet 37 of 46		

Add ESD diode base on EC FAE suggestion

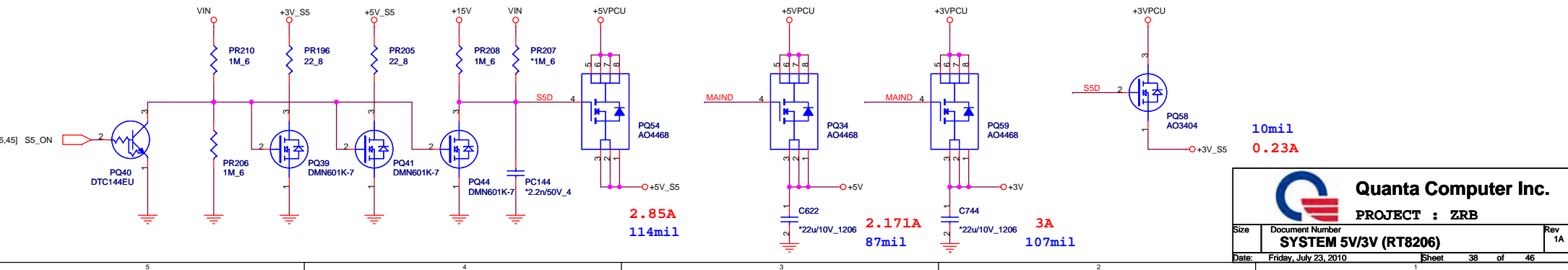


200mili
OCP: 6.5A
5A

280mili
OCP: 9A
7A

OCP: 6.5A
 $L(\text{ripple current}) = (9-5) * 5 / (2.2u * 0.4M * 9) = 2.525A$
 $I_{ocp} = 6.5 - (2.525 / 2) = 5.24A$
 $V_{th} = 5.24A * 14.2m\Omega = 0.74V$
 $R(I_{lim}) = (0.07437V * 10) / 5uA = 148.74K$
 $I_{peak}(\text{choke}) = 10.687A$

OCP: 9A
 $L(\text{ripple current}) = (9-3.3) * 3.3 / (2.2u * 0.5M * 9) = 1.9A$
 $I_{ocp} = 9 - (1.9 / 2) = 8.05A$
 $V_{th} = 8.05A * 14.2m\Omega = 114.31mV$
 $R(I_{lim}) = (114.31mV * 10) / 5uA = 228.62K$
 $I_{peak}(\text{choke}) = 11.479A$



2.85A
114mili

2.171A
87mili

3A
107mili

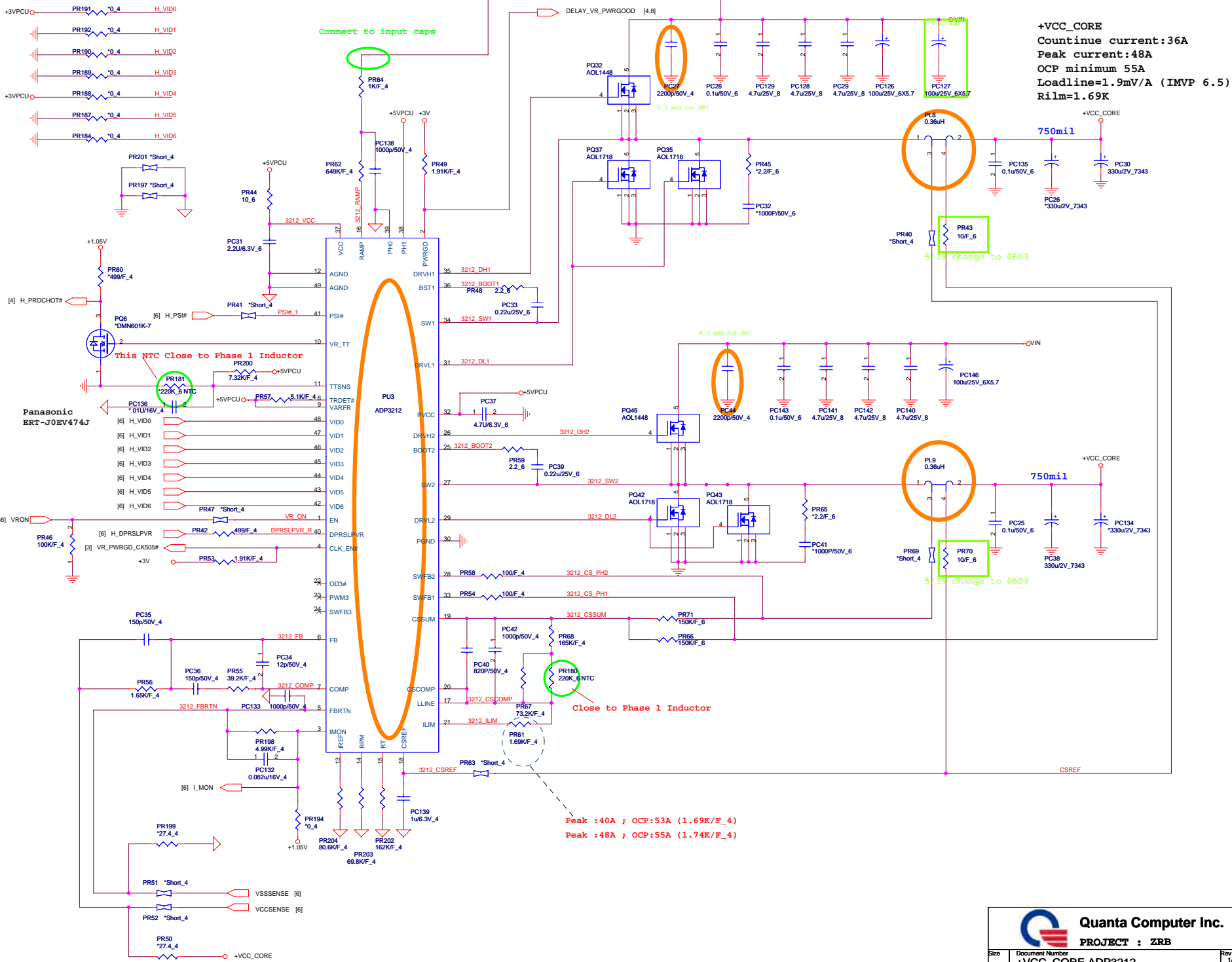
10mili
0.23A

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VID 1.2875V

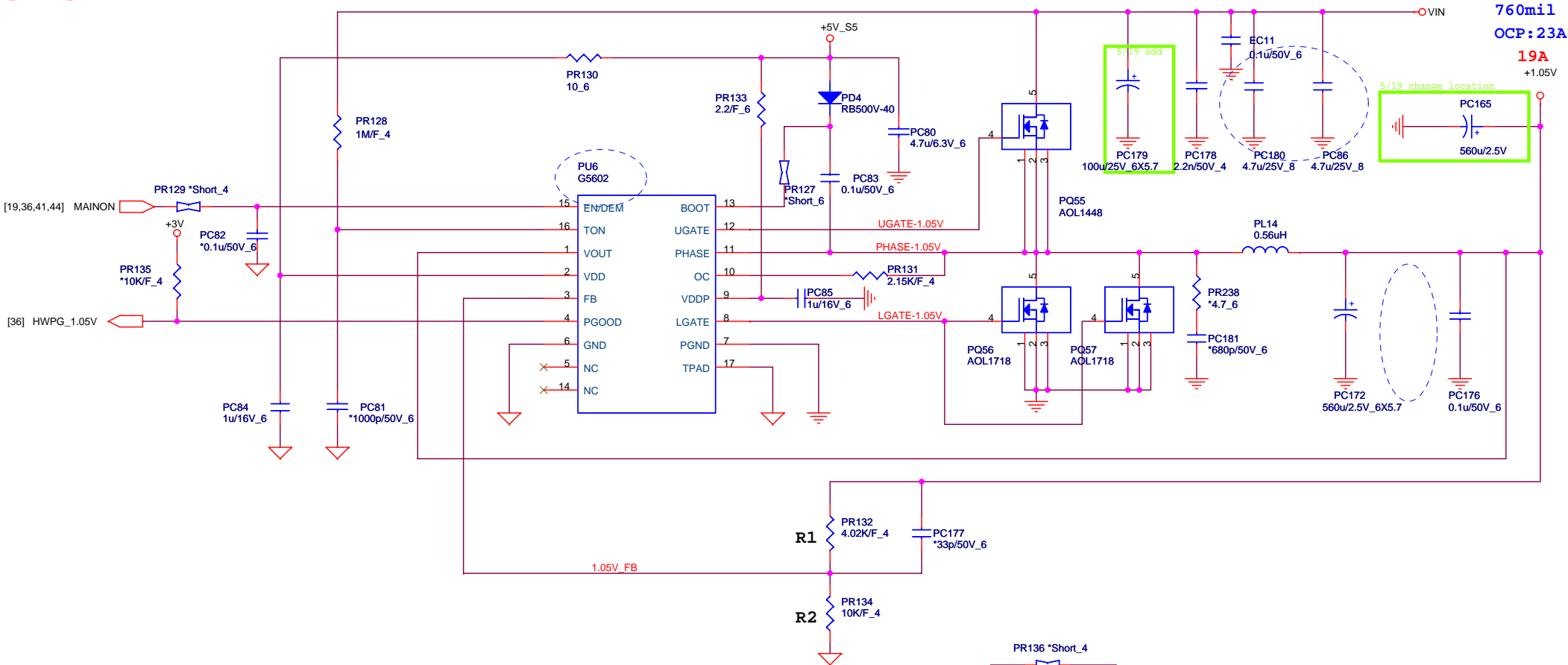


+VCC_CORE
 Continue current: 36A
 Peak current: 48A
 OCP minimum 55A
 Loadline=1.9mV/A (IMVP 6.5)
 Rilm=1.69K

Peak : 40A ; OCP: 53A (1.69K/F_4)
 Peak : 48A ; OCP: 55A (1.74K/F_4)

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		1A
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	+VCC_CORE ADP3212	Friday, July 23, 2010
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[PWM]



760mil
OCP: 23A
19A
+1.05V

$$TON = 3.85p \cdot RTON \cdot Vout / (Vin - 0.5)$$

$$Frequency = Vout / (Vin \cdot TON)$$

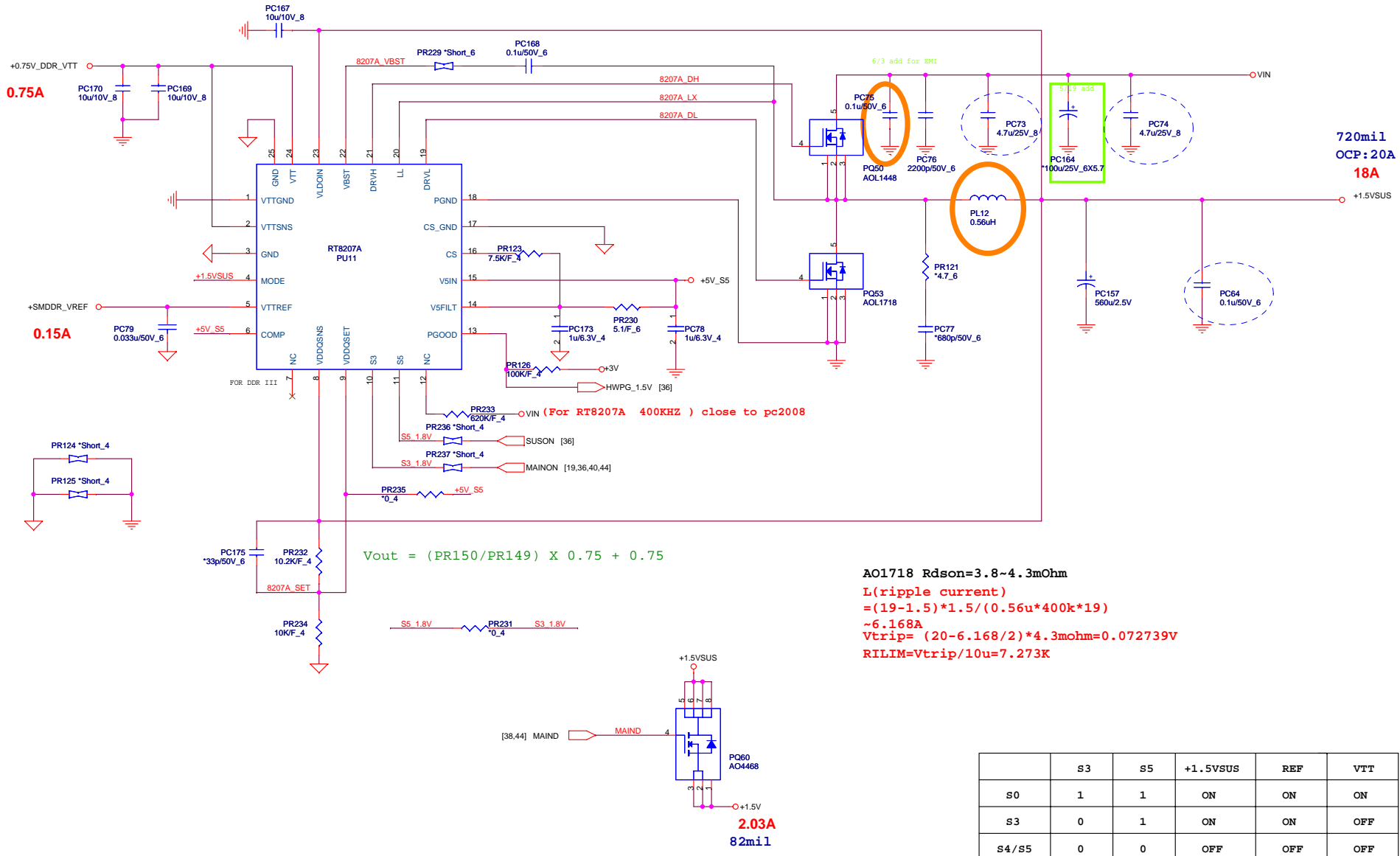
$$TON = 3.85p \cdot 1M \cdot 1 / (Vin - 0.5)$$

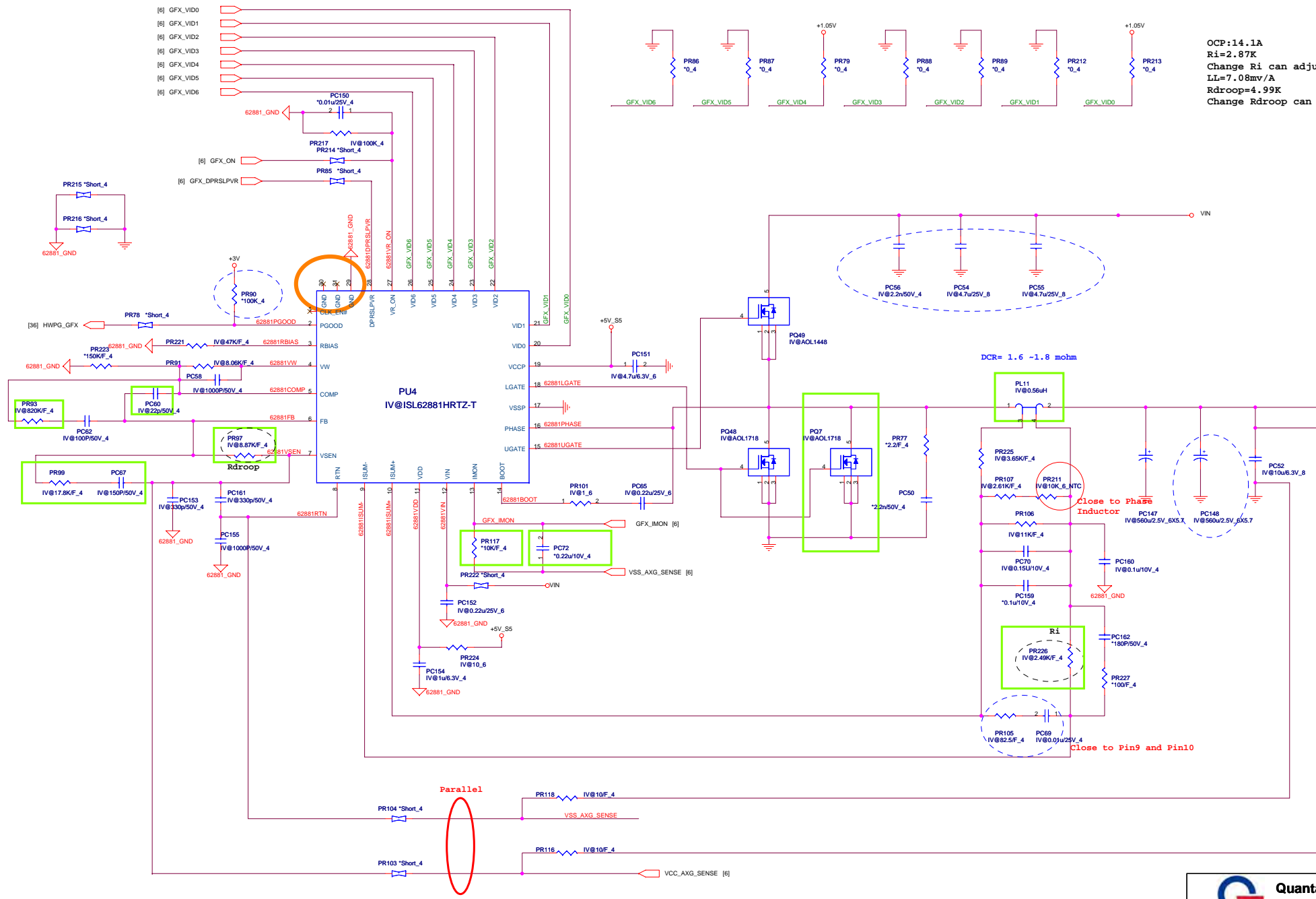
$$Frequency = 1 / (0.0036767) = 272K$$

AOL1718 $R_{dson} = 3 \sim 4.3m\Omega$
 $L(\text{ripple current}) = (19 - 1.05) \cdot 1.05 / (0.56 \cdot 272k \cdot 19) \sim 6.512A$
 $RILIM = 2.15m\Omega \cdot 23 - 3.256 / 20\mu A = 2.122K\Omega$
 $I(\text{choke})_{peak} = 29.512A$

		Quanta Computer Inc. PROJECT : ZRB	
		Size Document Number +VTT (UP6111A)	Rev 1A
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[PWM]





OCP:14.1A
 Ri=2.87K
 Change Ri can adjust OCP point
 LL=7.08mV/A
 Rdroop=4.99K
 Change Rdroop can adjust loadline

DCR= 1.6 ~1.8 mohm

660mil
 OCP:22A
 16.5A

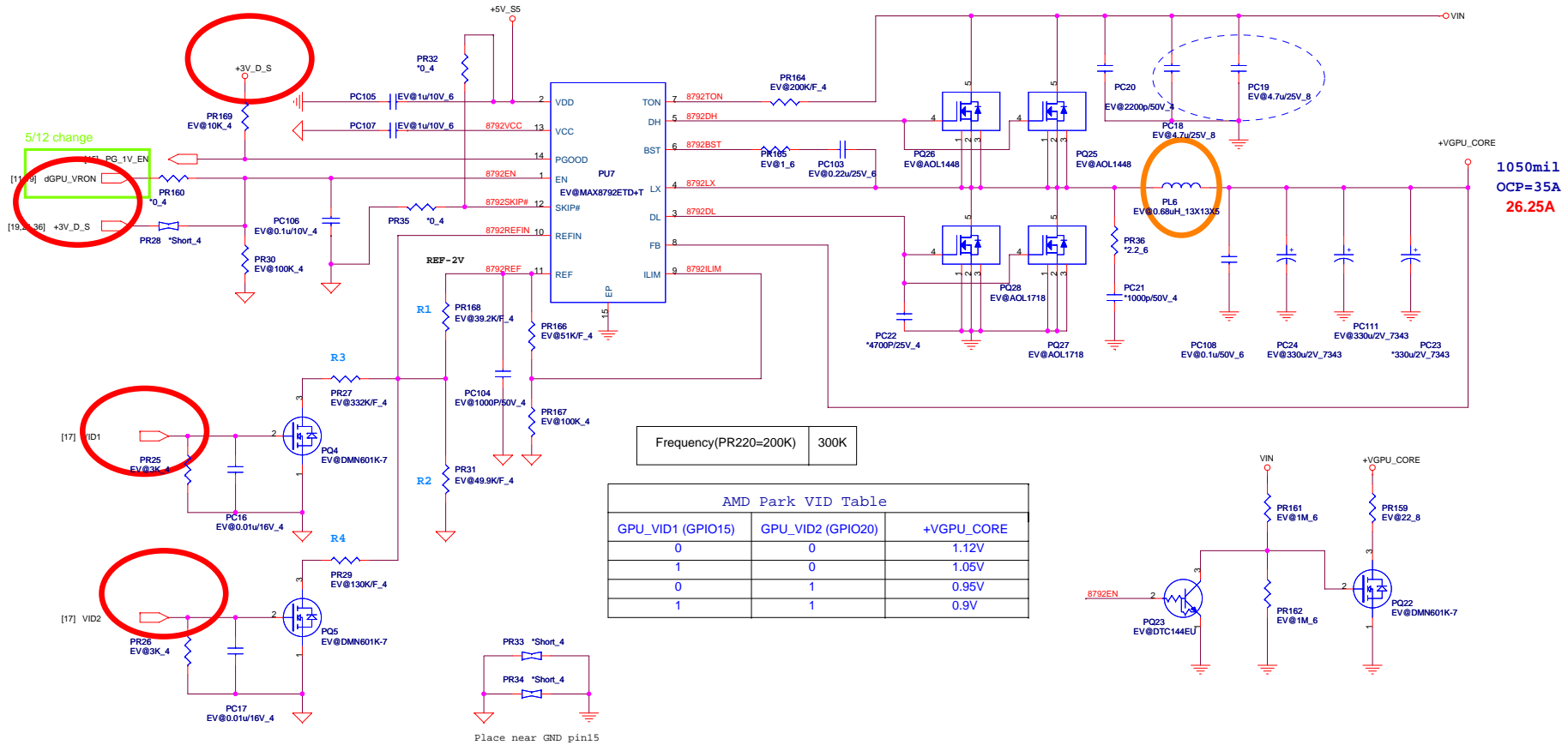
DCR=1.6~1.8mohm
 Load Line=7mV/A
 1.6m*0.6168=0.986m
 0.986m/.49K=396p
 392p*2*8.87K=7.03m
 OCP
 20u/2*2.49K=24.9m
 24.9m/0.6168=40.3m
 40.3m/1.6m=25.2A

Close to Phase Inductor

Close to Pin9 and Pin10

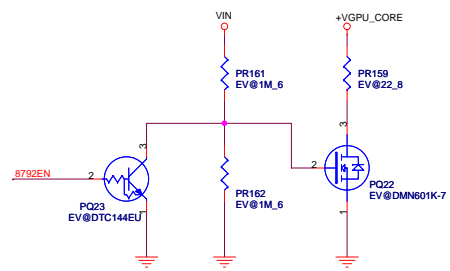
Quanta Computer Inc.
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 Size Document Number Rev
+VGFX_AXG (ISL62881)
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1.Level 1 Environment-related Substances should NEVER be used.
 2.purchased Ink, paste, wire leads, and holding resins only from the business partners that only approves as green partners.

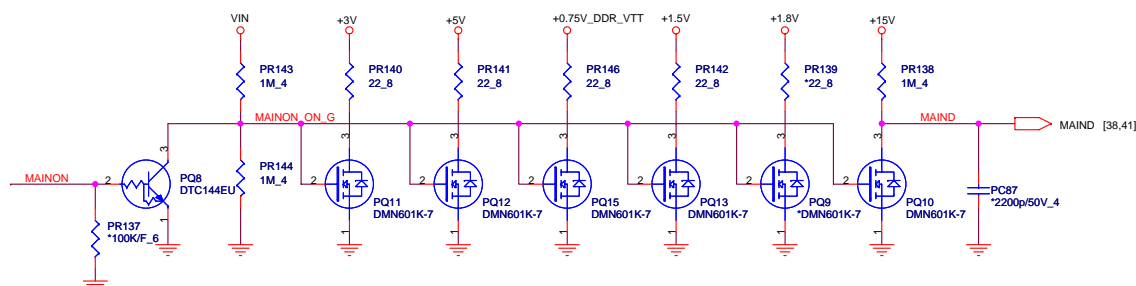
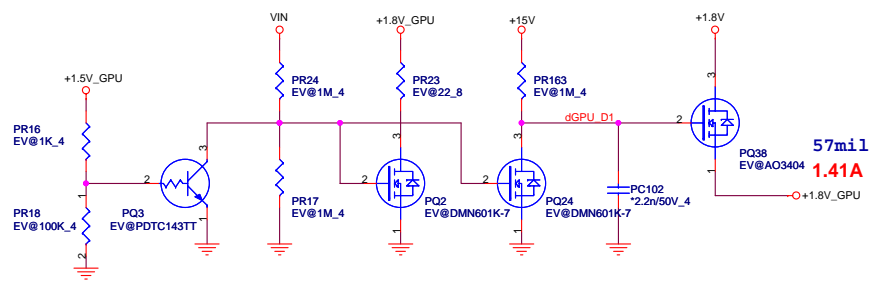
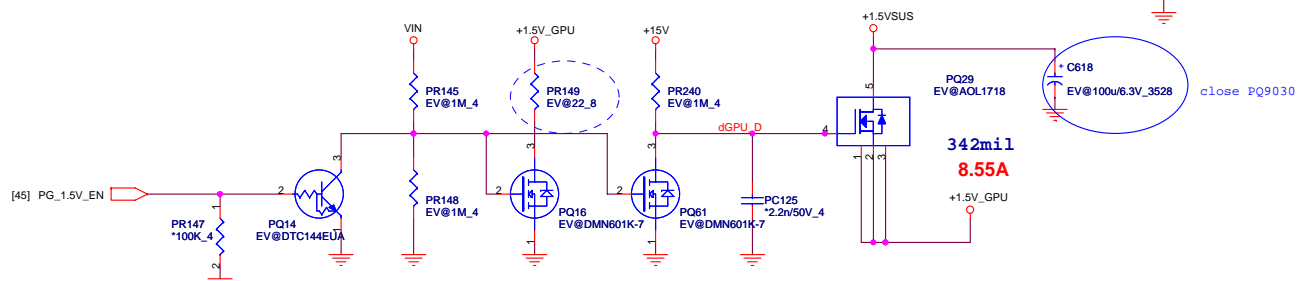
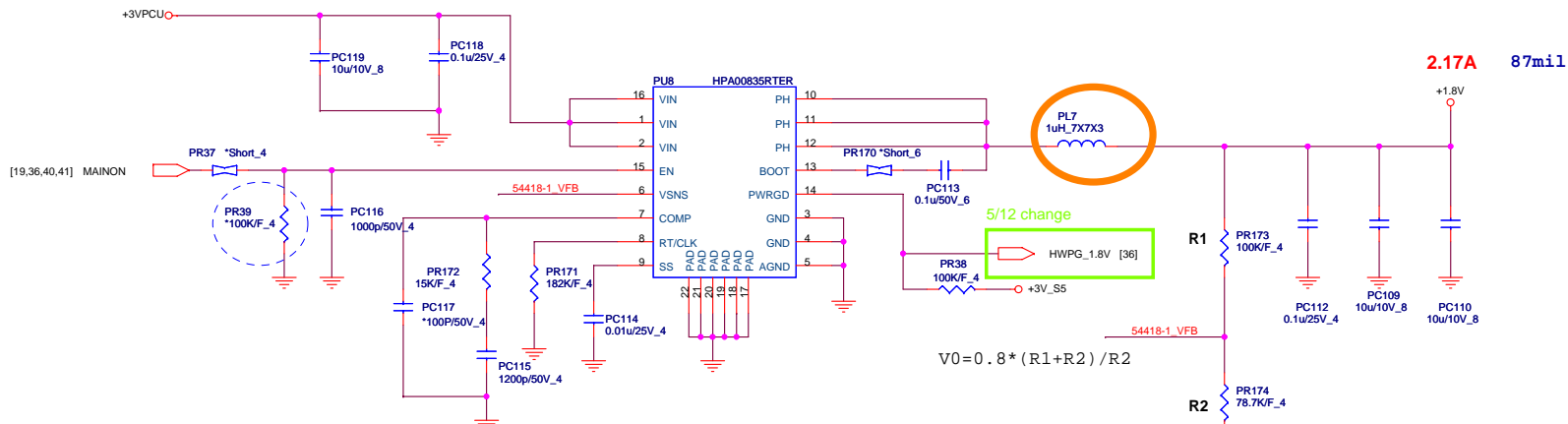


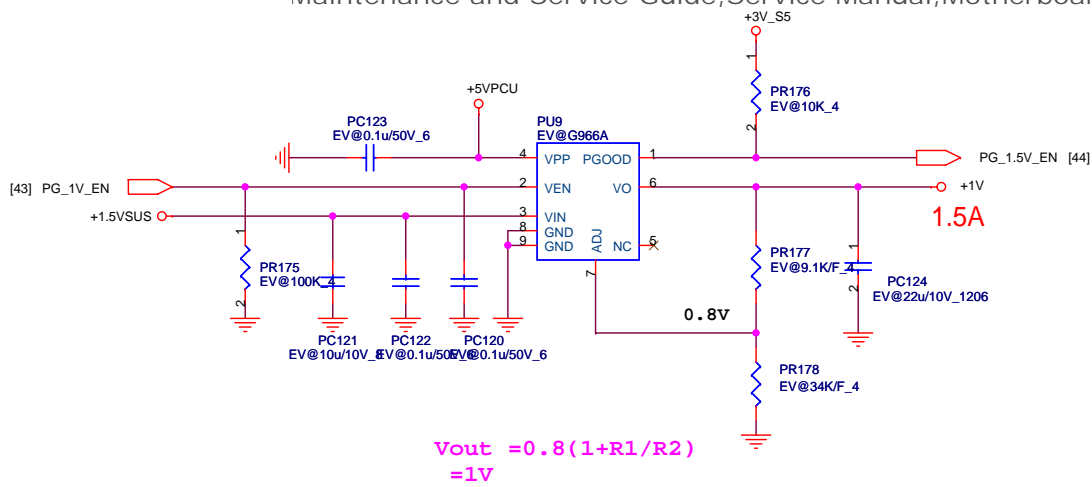
Frequency(PR220=200K) 300K

GPU_VID1 (GPIO15)	GPU_VID2 (GPIO20)	+VGPU_CORE
0	0	1.12V
1	0	1.05V
0	1	0.95V
1	1	0.9V

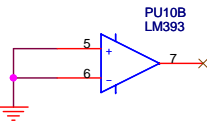


Place near GND pin15



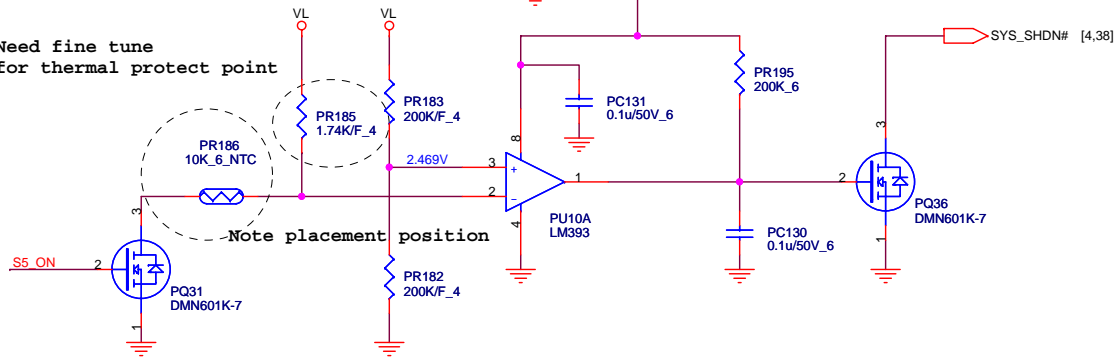



Thermal protection



For EC control thermal protection (output 3.3V)

Need fine tune for thermal protect point



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