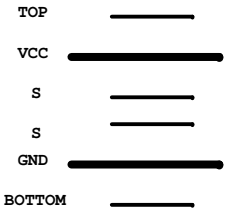
JV42-DN Block Diagram

Project code: 91.4HD01.001
PCB P/N : 48.4GX01.0SA
PCB 版號 : 09919 SA
REVISION : PCB STACKUP



DDR3 16,17 — 800/1066/1333MHz
DDR3 800/1066/1333 MHz 16,17 — 800/1066/1333MHz

AMD Champlain CPU
S1G4 (45W)
638-Pin uFCPGA638
4,5,6,7

OUT / IN — HT 3.0 16X16

CLK GEN. 3
ICS9LPRS480BKLFT 71.09480.A03
RTM880N-796-VB-GRT 71.00880.A03

North Bridge
AMD RS880M
CPU I/F LVDS, CRT I/F
INTEGRATED GRAHPICS
8,9,10

16X
PCI EXPRESS GRAPHIC

CRT 20
LCD 19
HDMI 21

Madison
ATI
53,54,55,56,57

DDR3 VRAM 58, 59, 60, 61

LAN Giga LAN BCM57780 26
TXFM 27
RJ45 27

A-Link 4X1

PCIex1
Mini Card WLAN 33

INT MIC 30
Codec ALC272 28
AZALIA

MIC In 30
INT.SPKR 30
OP AMP 29
Line Out
30

South Bridge
AMD SB820
USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
ATA 66/100
ACPI 1.1
LPC I/F
PCI/PCI BRIDGE
11,12,13,14,15

LPC BUS

KBC Novoton NPCE781B 36
BIOS MXIC MX25L1605 37
LPC DEBUG CONN. 37
Touch Pad 38
INT. KB 36

SATA
USB

HDD SATA 22
ODD SATA 23
Mini USB Blue Tooth 24
CardReader AU6433 32
MS/MS Pro/xD /MMC/SD 5 in 1 32
USB 3 Port 25
Camera
Daughter Board USB Board
Daughter Board PWR+LED Board

SYSTEM DC/DC RT8223 46	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(5.5A) 3D3V_S5(5A)

SYSTEM DC/DC RT8209E 47	
5V_S5	1D5V_S3(14A)
RT9026 47	
5V_S5	0D75_S3(1.2A)

SYSTEM DC/DC RT8209E 48	
INPUTS	
DCBATOUT	1D1V_S0(11A)
RT9025 48	
3D3V_S5	1D1V_S5(1.4A)

RT9025 49	
5V_S5	1D1V_VGA
RT9161 49	
3D3V_S0	2D5V_S0 (200mA)
RT9025 49	
1D5V_S3	1D05V_S0 (1.4A)

CHARGER BQ24745 50	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA

CPU DC/DC ISL6265AHR 45	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.55V 18A VDDNB 0~1.55V 4A

UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM
Size: A3 | Document Number: JV42-DN | Rev: SA
Date: Wednesday, November 18, 2009 | Sheet 1 of 63

UMA

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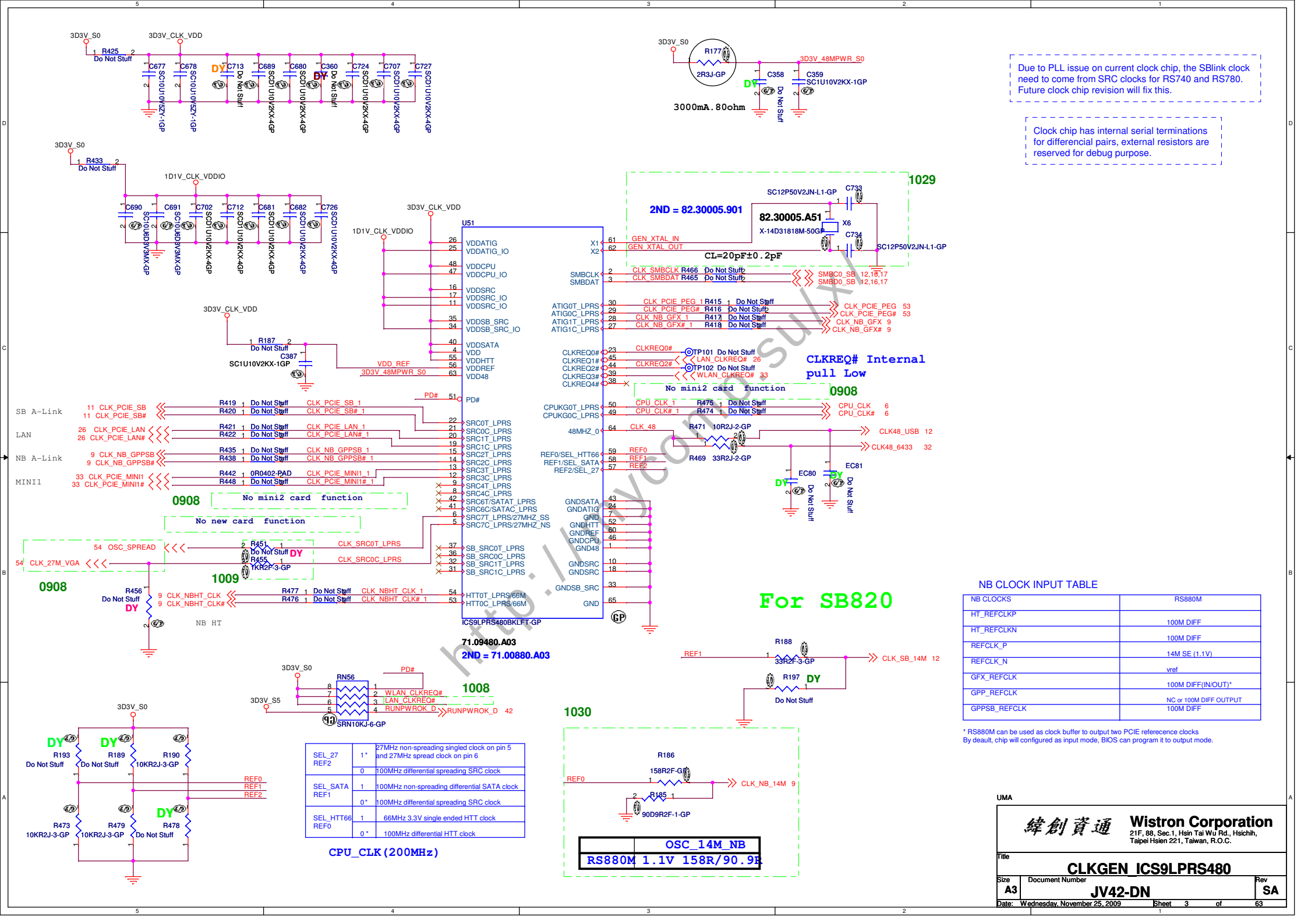
Taipei Hsien 221, Taiwan, R.O.C.

Title: **History**

Size	Document Number	Rev
A3	JV42-DN	SA

Date: Thursday, November 05, 2009 Sheet 2 of 63

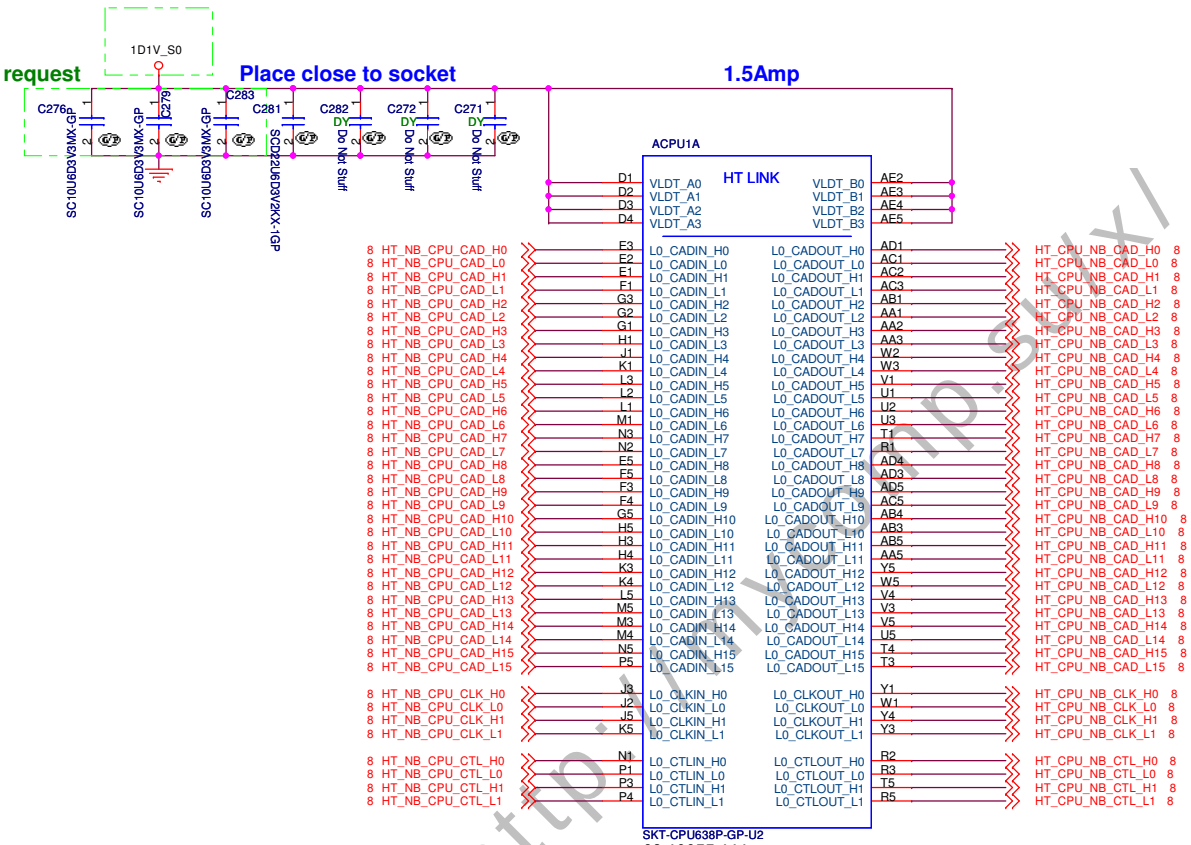


0904

1027 For AMD review request

Place close to socket

1.5Amp



SKT-BGA638H176

UMA

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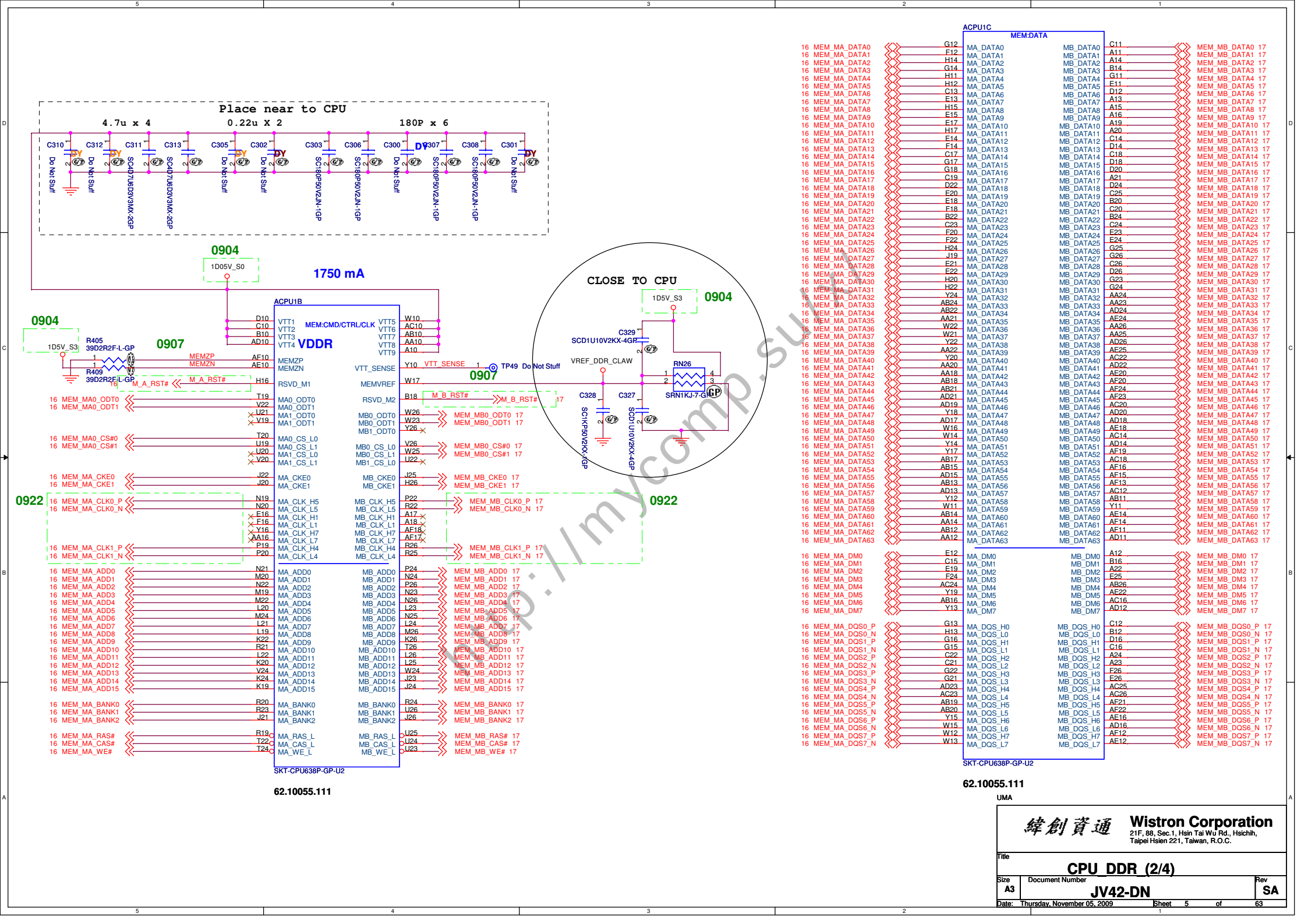
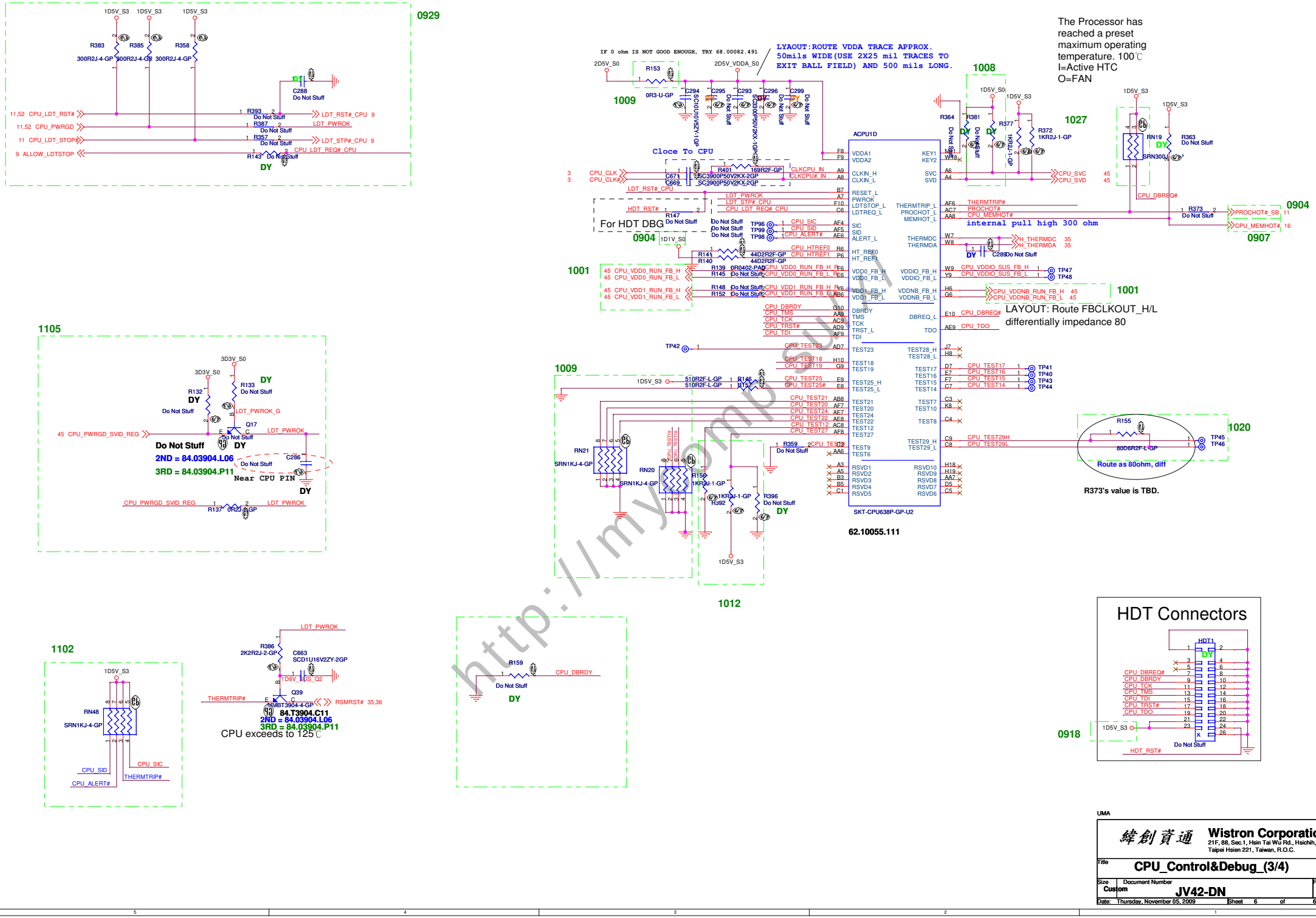
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

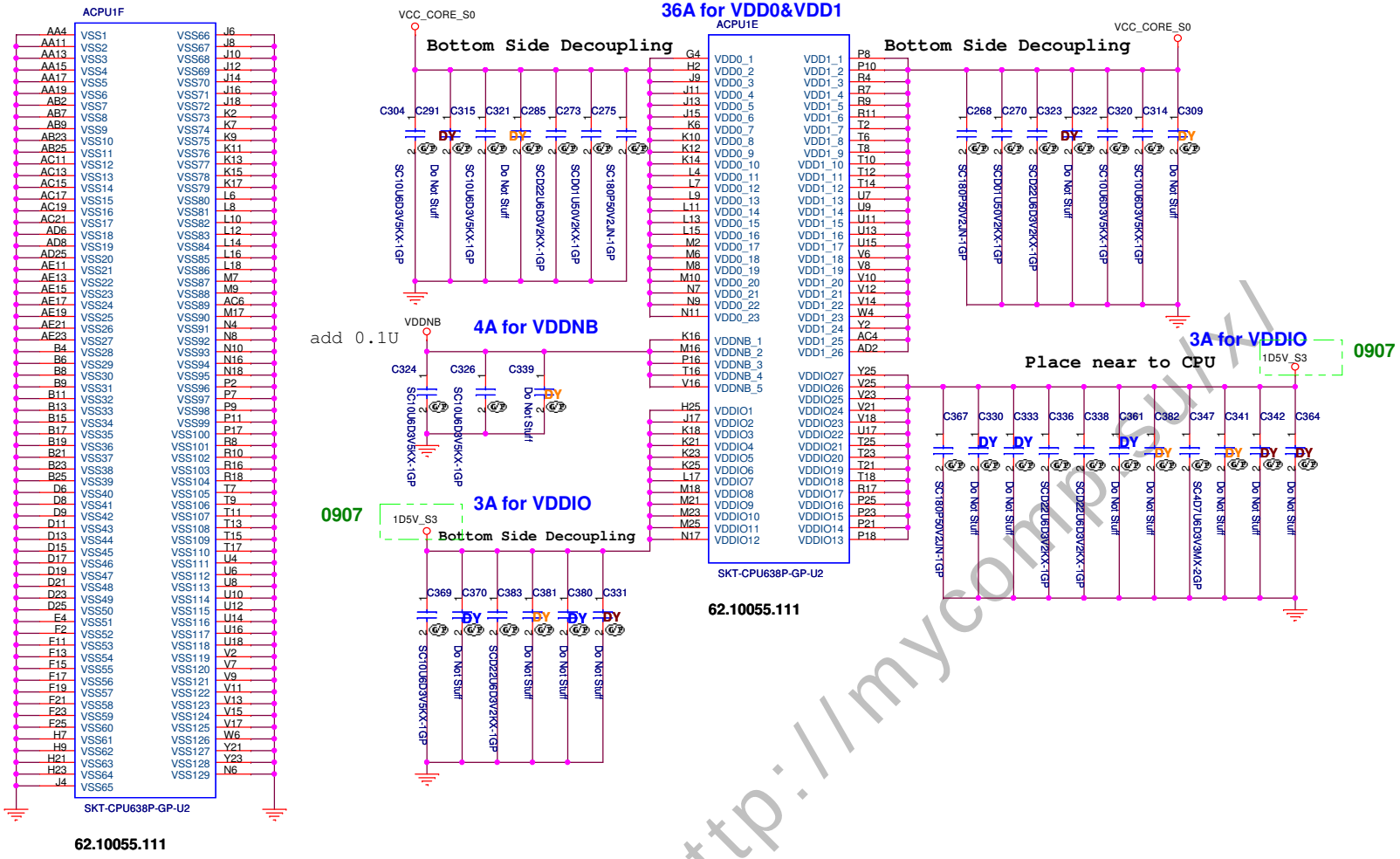
Title: CPU_HT_LINK I/F_(1/4)

Size: A3 | Document Number: JV42-DN | Rev: SA

Date: Thursday, November 05, 2009 | Sheet 4 of 63

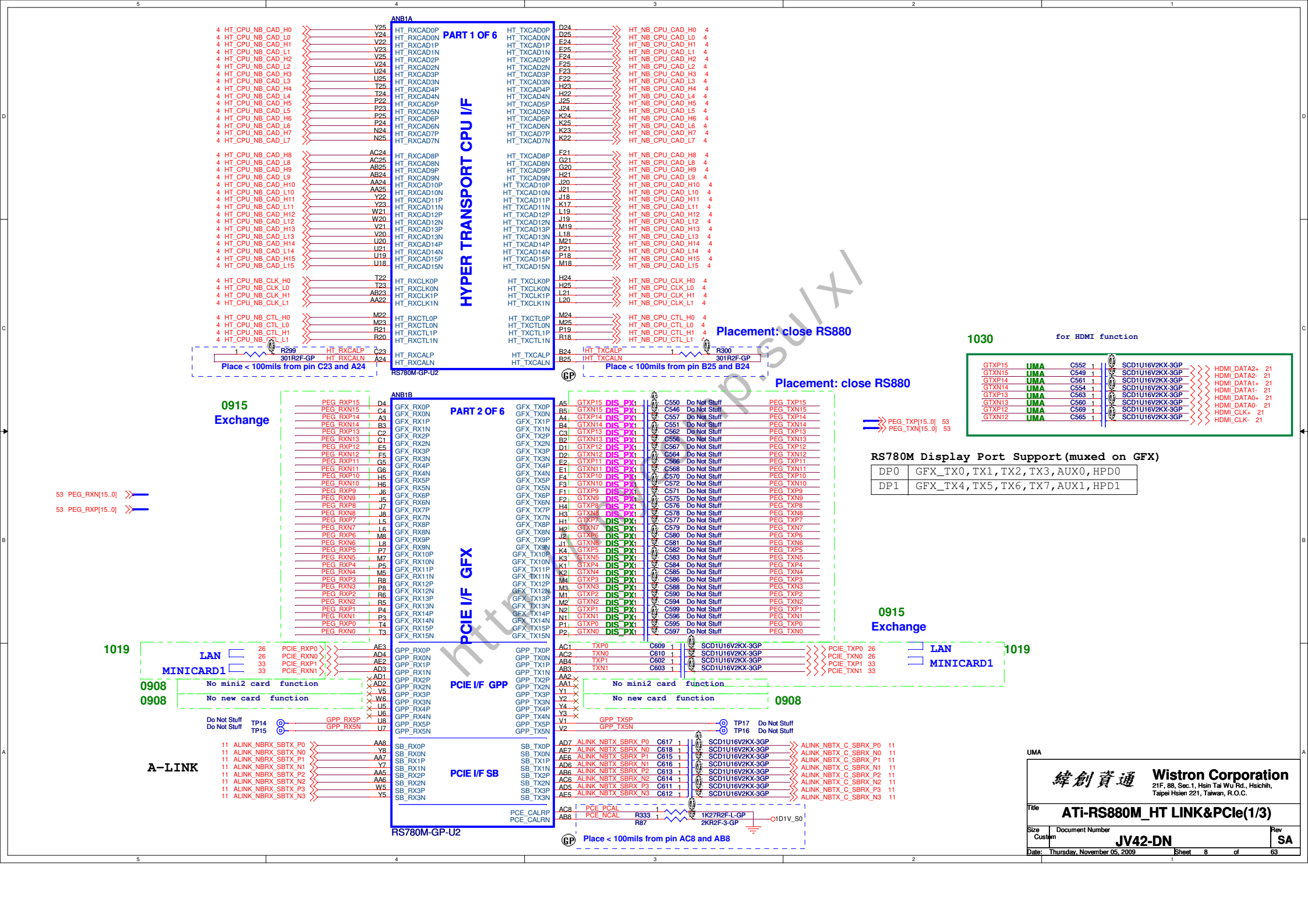

Place near to CPU
4.7u x 4
0.22u X 2
180P x 6
C310
C312
C311
C313
C305
C302
C303
C306
C300
C307
C308
C301
SC407U6D3V3MX-2GP
SC180P50V2JN-1GP
Do Not Stuff
0904
1D05V_S0
1750 mA
ACPU1B
MEM:CMD/CTRL/CLK
VDDR
0907
R405
R409
39D2R2F-L-GP
MEMZP
MEMZN
M_A_RST#
M_B_RST#
VTT_SENSE
TP49
MA0_ODT0
MA0_ODT1
MA1_ODT0
MA1_ODT1
MA0_CS_L0
MA0_CS_L1
MA1_CS_L0
MA1_CS_L1
MA_CKE0
MA_CKE1
MA_CLK_H5
MA_CLK_L5
MA_CLK_H1
MA_CLK_L1
MA_CLK_H7
MA_CLK_L7
MA_CLK_H4
MA_CLK_L4
MA_ADD0
MA_ADD1
MA_ADD2
MA_ADD3
MA_ADD4
MA_ADD5
MA_ADD6
MA_ADD7
MA_ADD8
MA_ADD9
MA_ADD10
MA_ADD11
MA_ADD12
MA_ADD13
MA_ADD14
MA_ADD15
MA_BANK0
MA_BANK1
MA_BANK2
MA_RAS_L
MA_CAS_L
MA_WE_L
MB_ADD0
MB_ADD1
MB_ADD2
MB_ADD3
MB_ADD4
MB_ADD5
MB_ADD6
MB_ADD7
MB_ADD8
MB_ADD9
MB_ADD10
MB_ADD11
MB_ADD12
MB_ADD13
MB_ADD14
MB_ADD15
MB_BANK0
MB_BANK1
MB_BANK2
MB_RAS_L
MB_CAS_L
MB_WE_L
SKT-CPU638P-GP-U2
62.10055.111
CLOSE TO CPU
VREF_DDR_CLAW
C329
C328
C327
SCD1U10V2KX-4GP
SC1KP50V2KX-1GP
RN26
SRN1KJ-7-GP
ACPU1C
MEM:DATA
SKT-CPU638P-GP-U2
62.10055.111
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU_DDR_(2/4)
Size
A3
Document Number
JV42-DN
Rev
SA
Date: Thursday, November 05, 2009
Sheet 5 of 63

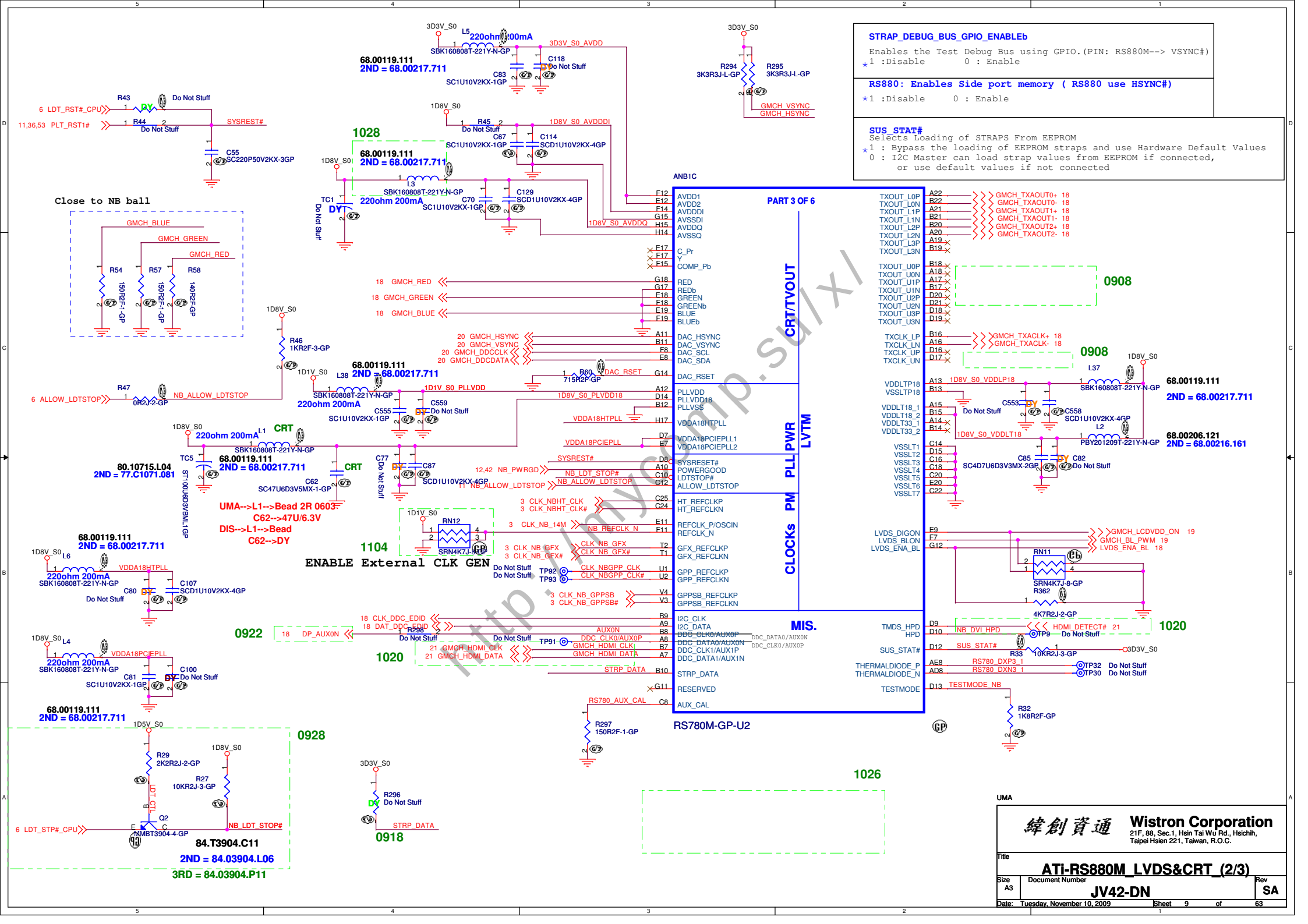


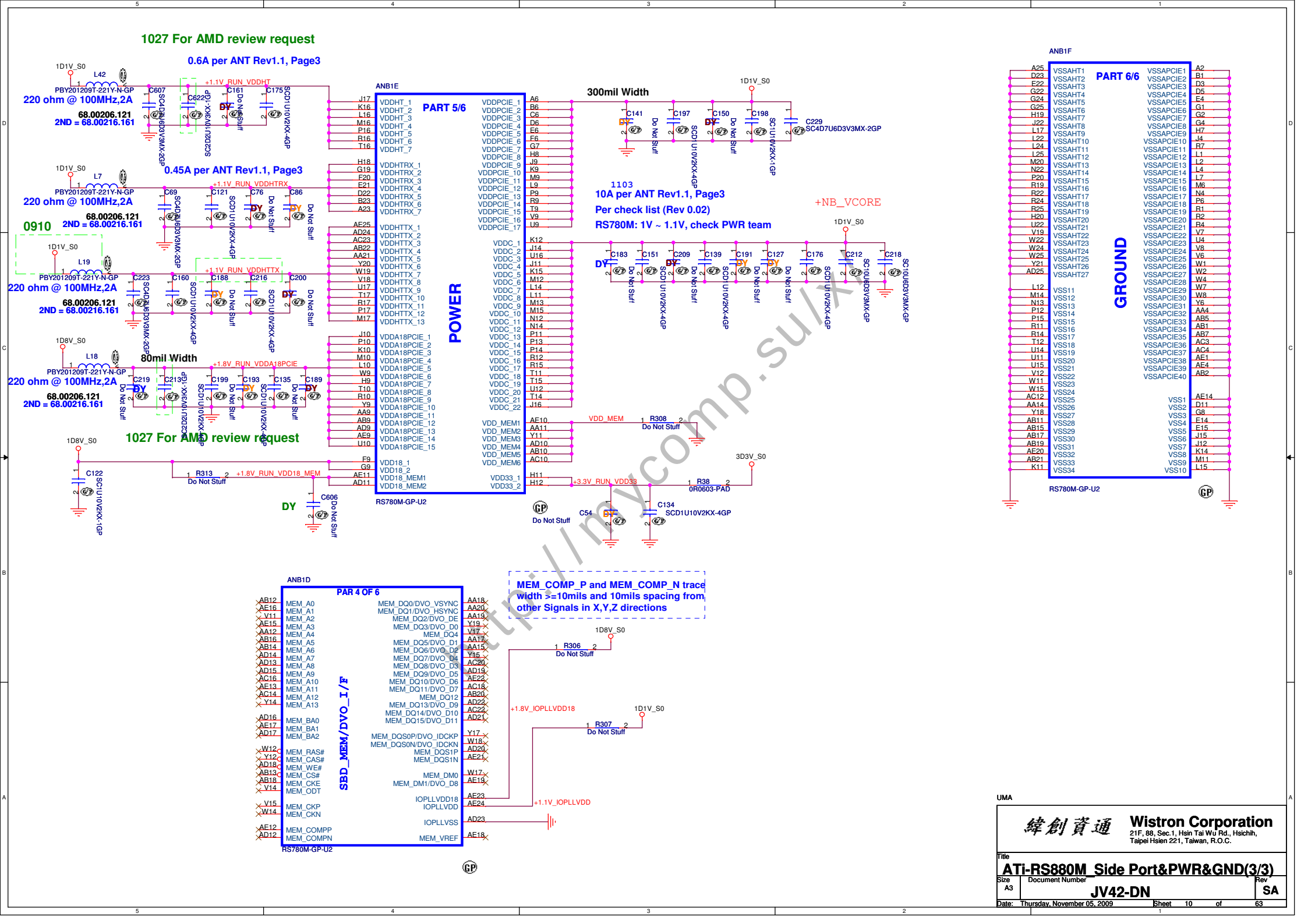


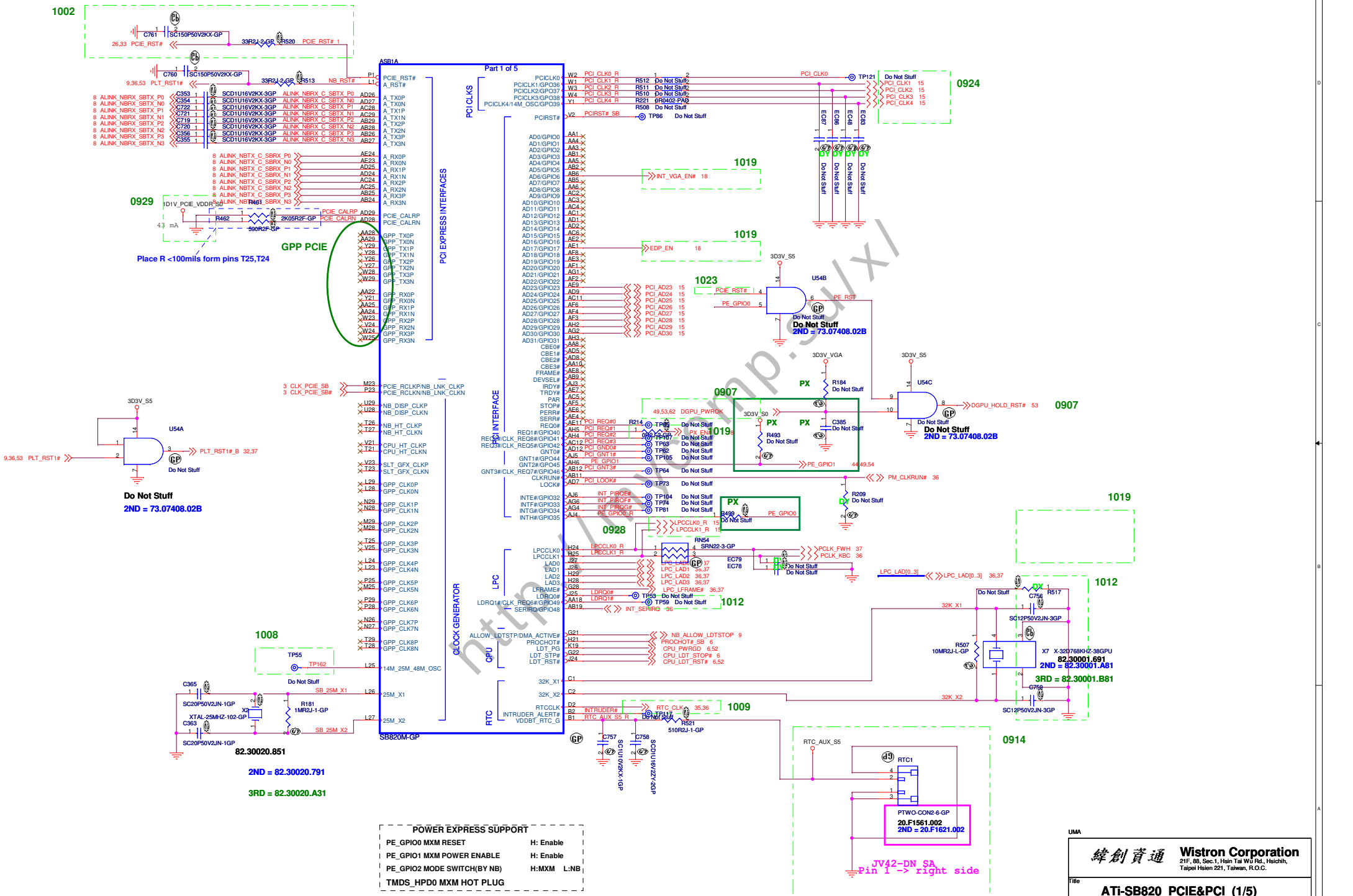
UMA

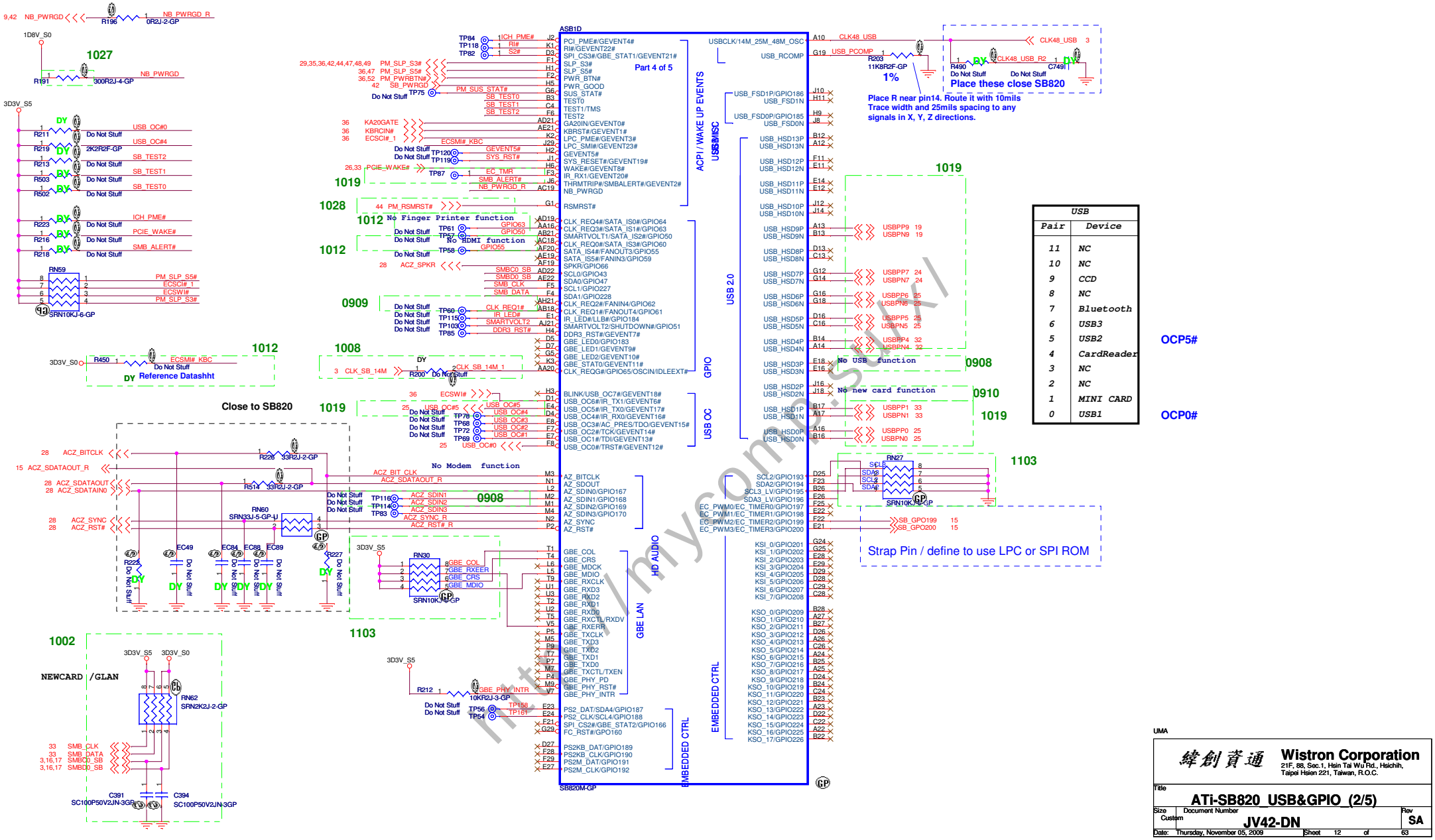
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CPU_Power_(4/4)		
Size: A3	Document Number: JV42-DN	Rev: SA
Date: Thursday, November 05, 2009	Sheet 7 of 63	

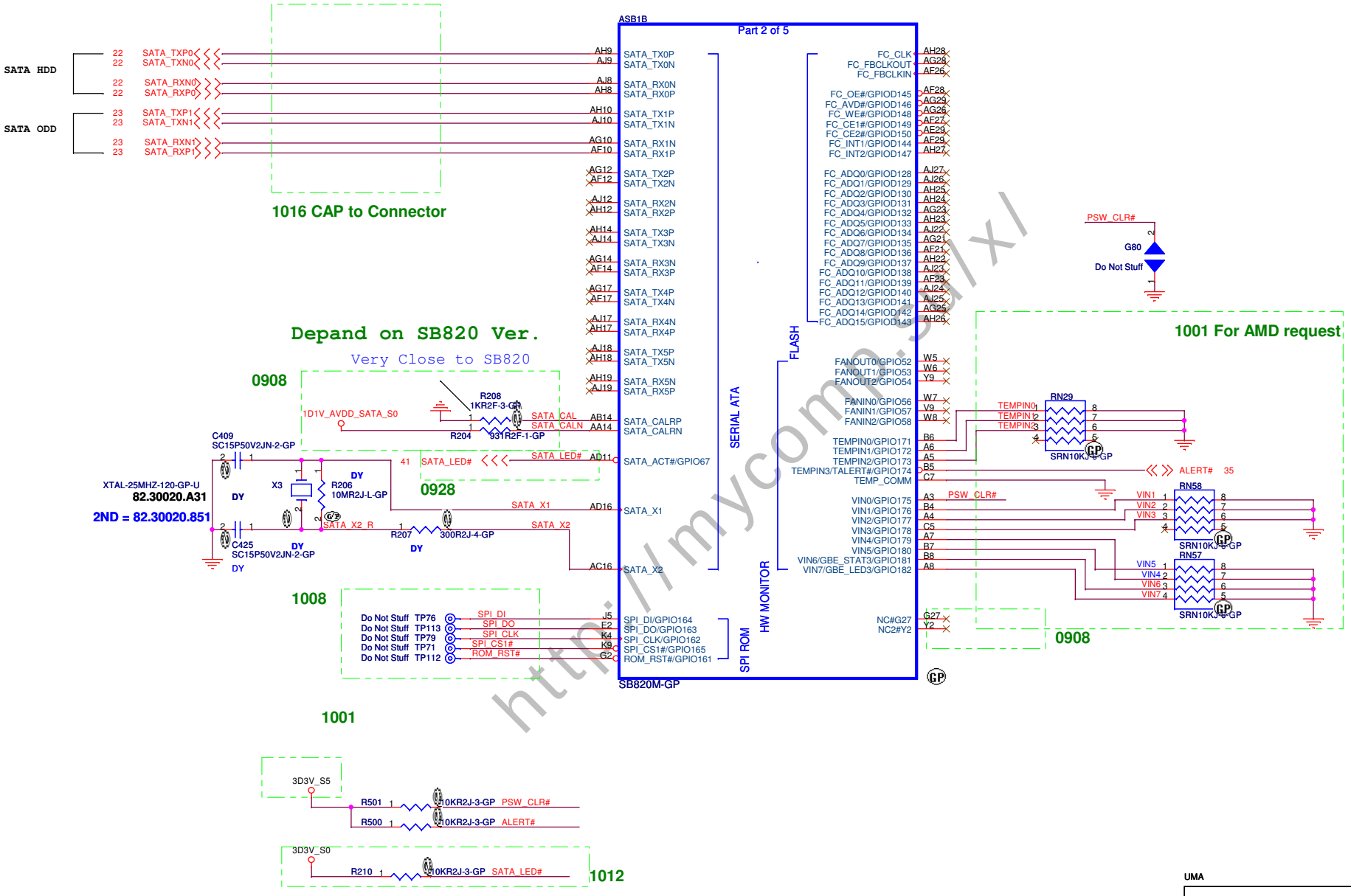

ANB1A
PART 1 OF 6
HYPER TRANSPORT CPU I/F
RS780M-GP-U2
Placement: close RS880
Place < 100mils from pin C23 and A24
Place < 100mils from pin B25 and B24
1030
for HDMI function
ANB1B
PART 2 OF 6
PCIE I/F GFX
PCIE I/F GPP
PCIE I/F SB
0915
Exchange
RS780M Display Port Support(muxed on GFX)
DP0 GFX_TX0,TX1,TX2,TX3,AUX0,HPD0
DP1 GFX_TX4,TX5,TX6,TX7,AUX1,HPD1
1019
LAN
MINICARD1
0908
No mini2 card function
No new card function
A-LINK
Place < 100mils from pin AC8 and AB8
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-RS880M_HT LINK&PCIe(1/3)
Size Custom
Document Number
JV42-DN
Rev
SA
Date: Thursday, November 05, 2009
Sheet 8 of 63


STRAP_DEBUG_BUS_GPIO_ENABLEb
Enables the Test Debug Bus using GPIO.(PIN: RS880M--> VSYNC#)
*1 :Disable 0 : Enable
RS880: Enables Side port memory (RS880 use HSYNC#)
*1 :Disable 0 : Enable
SUS_STAT#
Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected,
or use default values if not connected
ANB1C
PART 3 OF 6
RS780M-GP-U2
CRT/TVOUT
PWR
LVTM
PLL
CLOCKs
PM
MIS.
Close to NB ball
ENABLE External CLK GEN
UMA-->L1-->Bead 2R 0603
C62-->47U/6.3V
DIS-->L1-->Bead
C62-->DY
0908
1028
1104
0922
1020
0928
0918
1026
68.00119.111
2ND = 68.00217.711
68.00206.121
2ND = 68.00216.161
80.10715.L04
2ND = 77.C1071.081
84.T3904.C11
2ND = 84.03904.L06
3RD = 84.03904.P11
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ATi-RS880M_LVDS&CRT_(2/3)
Document Number
JV42-DN
Size A3
Rev SA
Date: Tuesday, November 10, 2009
Sheet 9 of 63


1027 For AMD review request
0.6A per ANT Rev1.1, Page3
0.45A per ANT Rev1.1, Page3
80mil Width
1027 For AMD review request
300mil Width
1103
10A per ANT Rev1.1, Page3
Per check list (Rev 0.02)
RS780M: 1V ~ 1.1V, check PWR team
+NB_VCORE
0910
220 ohm @ 100MHz,2A
68.00206.121
2ND = 68.00216.161
ANB1E
PART 5/6
POWER
RS780M-GP-U2
ANB1F
PART 6/6
GROUND
ANB1D
PAR 4 OF 6
SBD_MEM/DVO_I/F
MEM_COMP_P and MEM_COMP_N trace width >=10mils and 10mils spacing from other Signals in X,Y,Z directions
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-RS880M_Side Port&PWR&GND(3/3)
Size A3
Document Number JV42-DN
Rev SA
Date: Thursday, November 05, 2009
Sheet 10 of 63


1002
ASB1A
Part 1 of 5
SB820M-GP
PCI CLKS
PCI EXPRESS INTERFACES
PCI INTERFACE
CLOCK GENERATOR
LPC
GPU
RTC
GPP PCIE
Place R <100mils form pins T25,T24
0929
0924
0907
0928
1008
1019
1023
1012
1009
0914
Do Not Stuff
2ND = 73.07408.02B
2ND = 82.30020.791
3RD = 82.30020.A31
82.30020.851
82.30001.691
2ND = 82.30001.A81
3RD = 82.30001.B81
20.F1561.002
2ND = 20.F1621.002
JV42-DN SA
Pin 1 -> right side
POWER EXPRESS SUPPORT
PE_GPIO0 MXM RESET H: Enable
PE_GPIO1 MXM POWER ENABLE H: Enable
PE_GPIO2 MODE SWITCH(BY NB) H:MXM L:NB
TMDS_HPD0 MXM HOT PLUG
UMA
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB820 PCIE&PCI (1/5)
Size
Document Number
JV42-DN
Rev
SA
Date: Thursday, November 26, 2009
Sheet 11 of 63





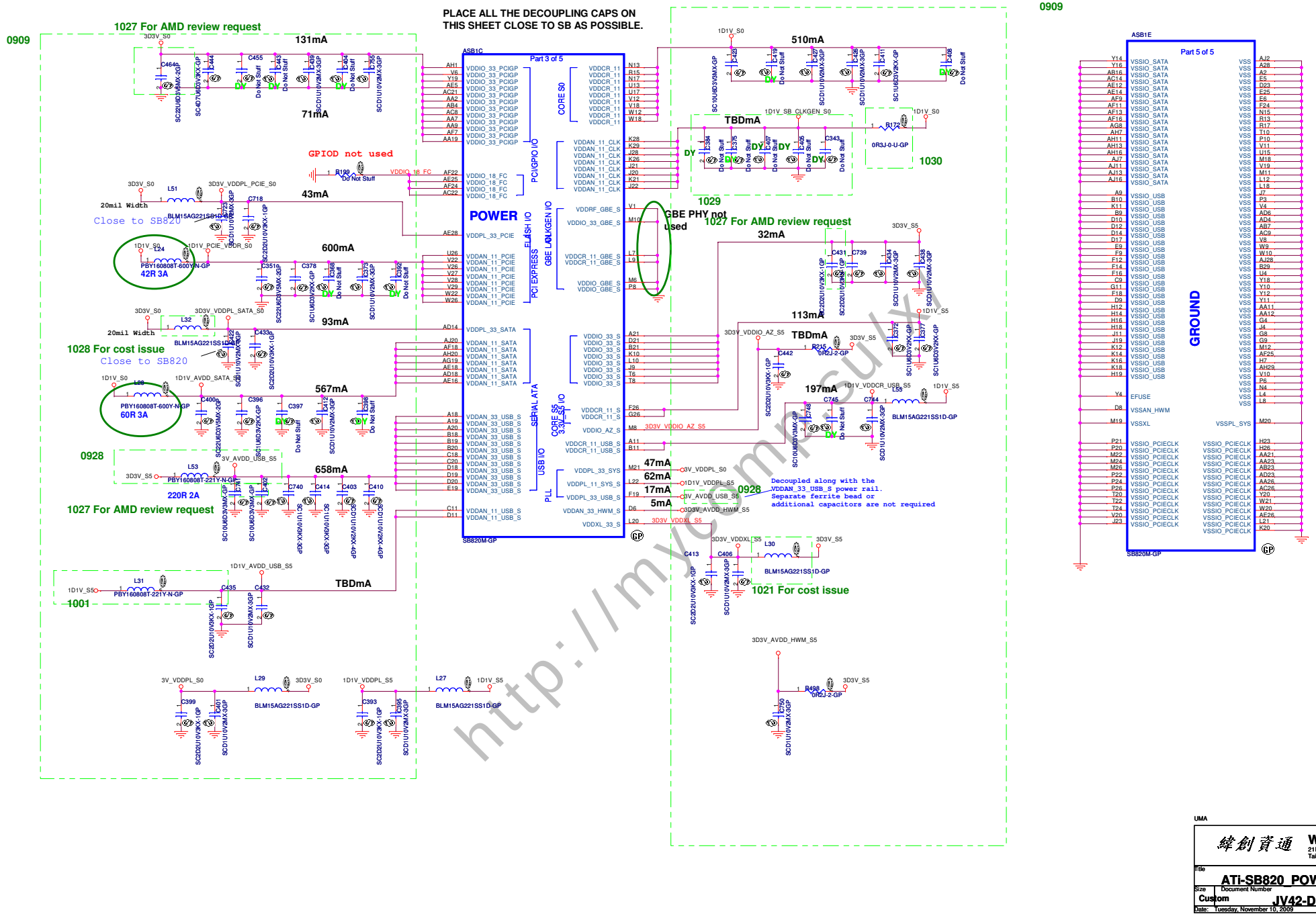
UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB820_SATA-IDE_(3/5)

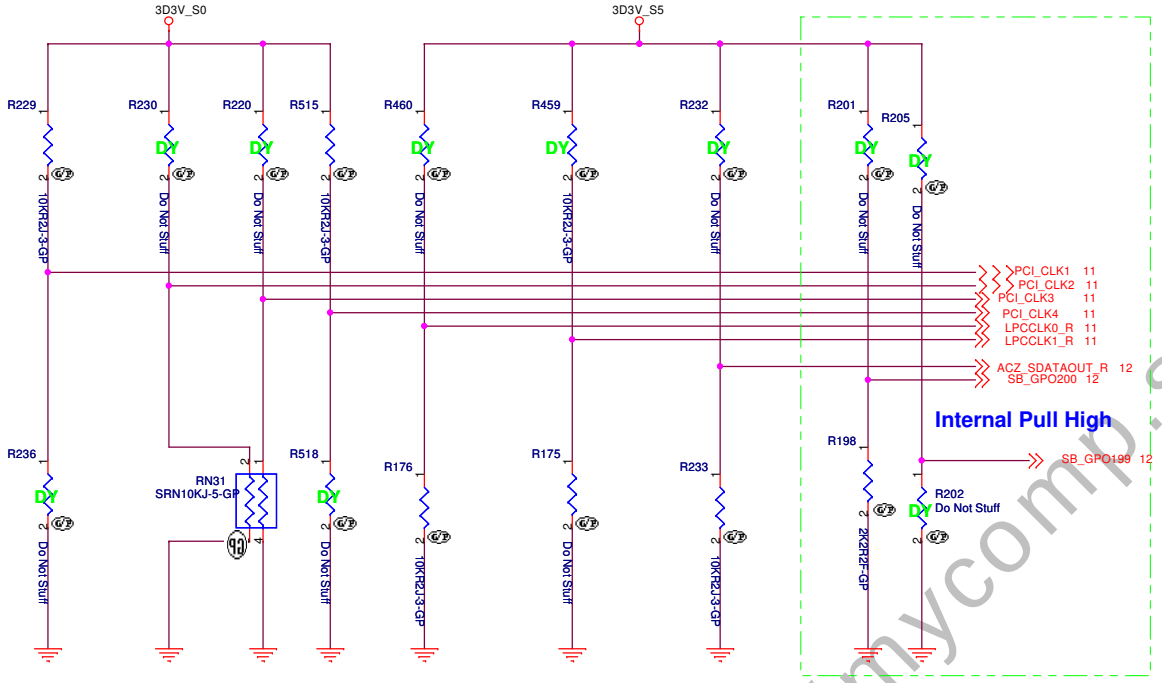
Size: A3 | Document Number: JV42-DN | Rev: SA

Date: Thursday, November 19, 2009 | Sheet 13 of 63



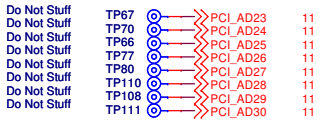
REQUIRED STRAPS

REQUIRED SYSTEM STRAPS



	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	AZ_SDOUT	GPIO200 GPIO199
PULL HIGH	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED DEFAULT	CLKGEN ENABLED DEFAULT	LOW POWER MODE	H,H = Reserved H,L = SPI ROM
PULL LOW	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED	CLKGEN DISABLED	PERFORMANCE MODE DEFAULT	L,H = LPC ROM (Default) L,L = FWH ROM

DEBUG STRAPS



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

UMA

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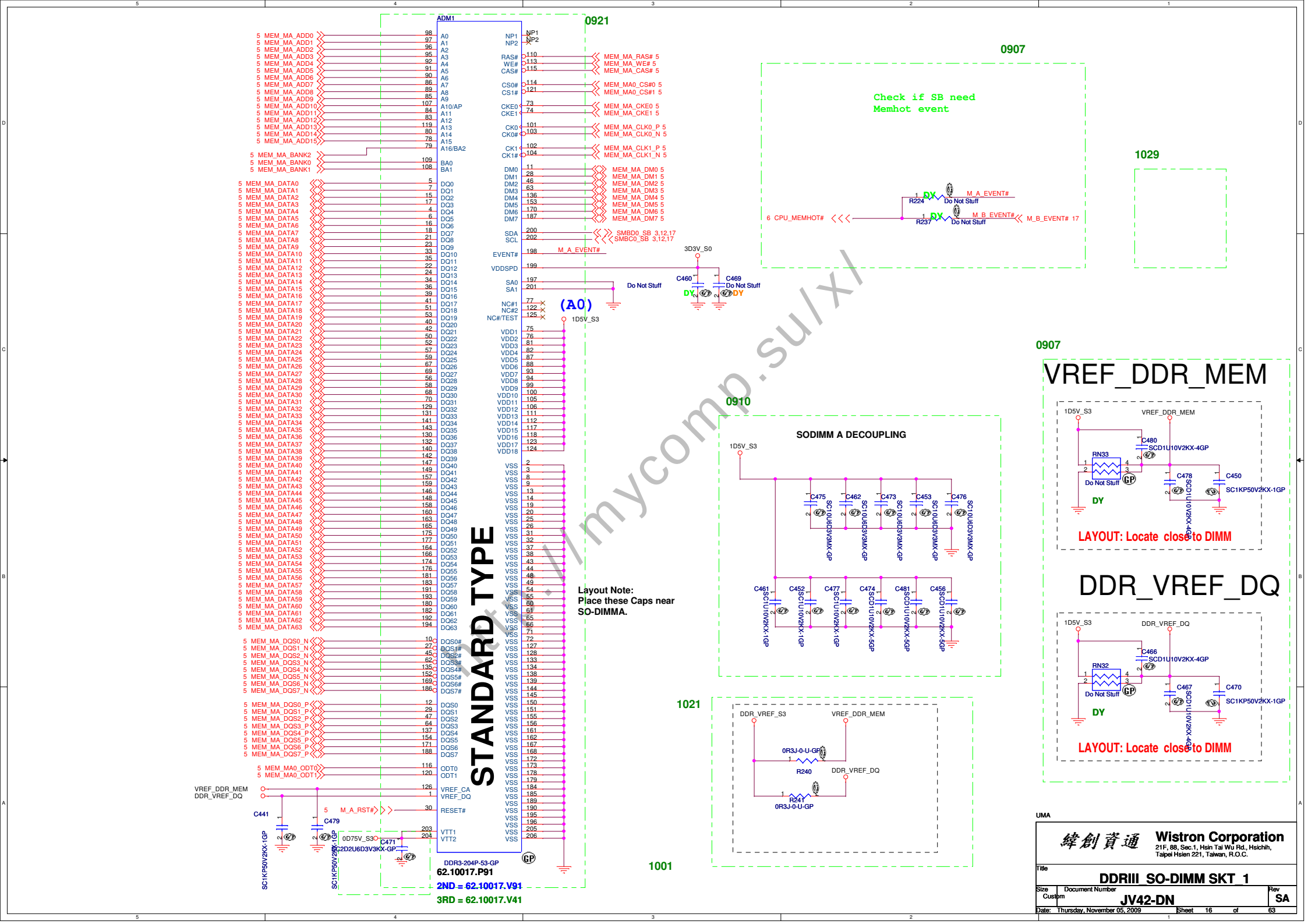
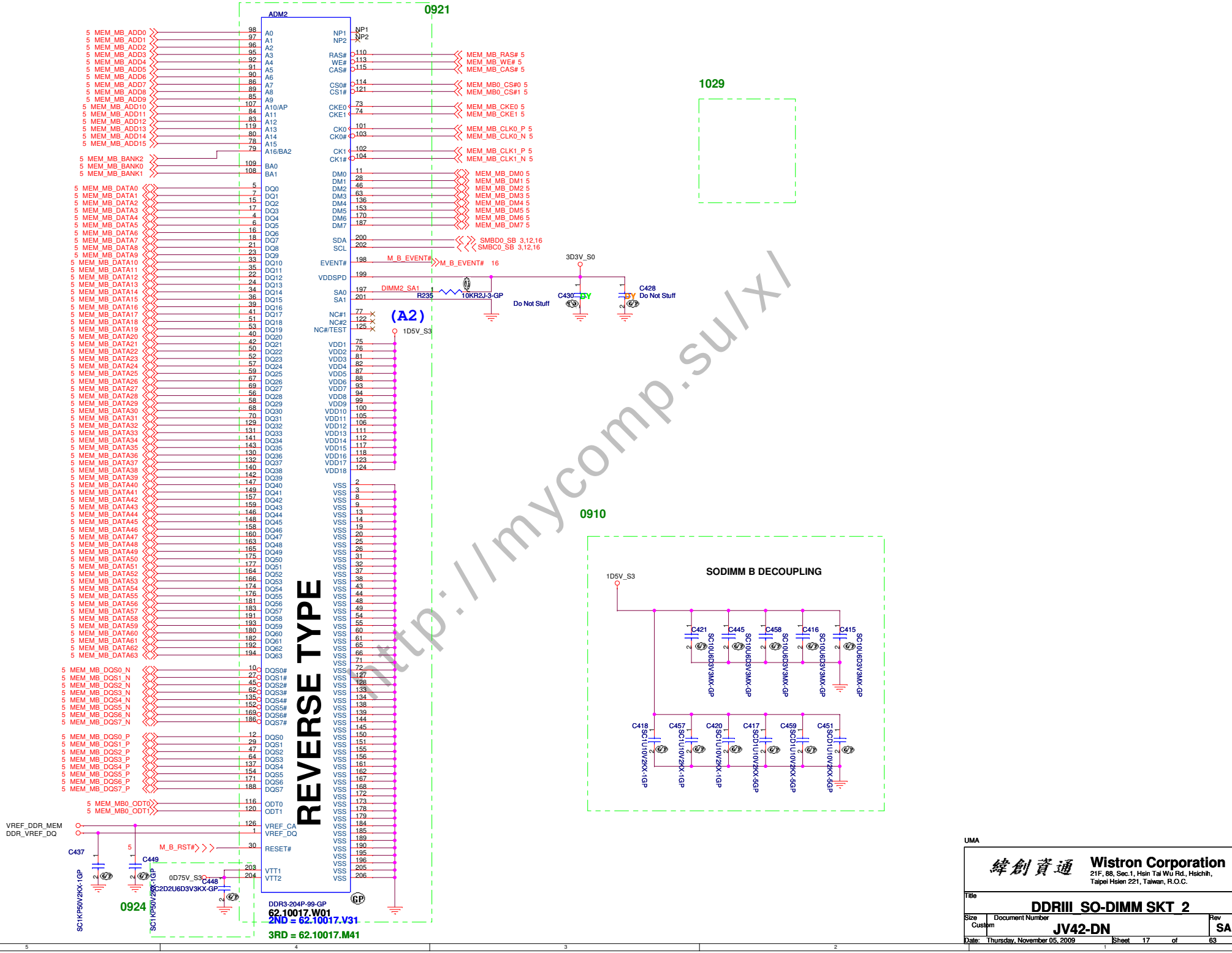
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB820_STRAPPING_(5/5)

Size: A3 | Document Number: JV42-DN | Rev: SA

Date: Wednesday, November 18, 2009 | Sheet 15 of 63


ADM1
STANDARD TYPE
DDR3-204P-53-GP
62.10017.P91
2ND = 62.10017.V91
3RD = 62.10017.V41
0921
0907
Check if SB need
Memhot event
1029
0907
VREF_DDR_MEM
LAYOUT: Locate close to DIMM
DDR_VREF_DQ
LAYOUT: Locate close to DIMM
0910
SODIMM A DECOUPLING
Layout Note:
Place these Caps near
SO-DIMMA.
1021
1001
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DDRIII_SO-DIMM SKT_1
JV42-DN
SA
Thursday, November 05, 2009
16
63

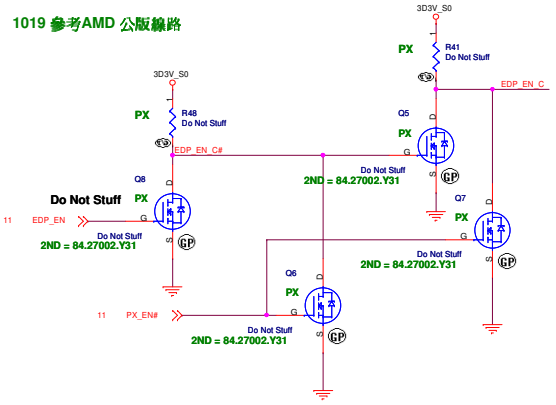


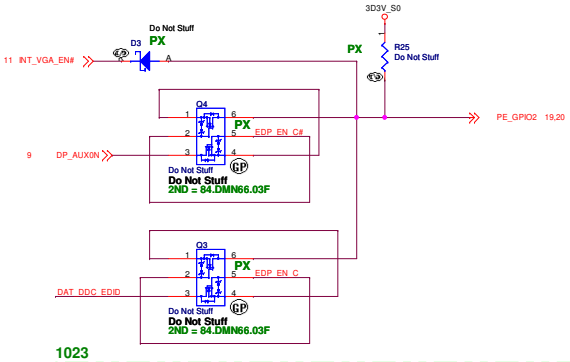
UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DDRIII_SO-DIMM SKT_2	
Size: Custom	Document Number: JV42-DN	Rev: SA
Date: Thursday, November 05, 2009	Sheet 17 of 63	

1019 參考AMD 公版線路





Truth Table

LVDS

Function	SEL
A_N to $_NB_1$	L
A_N to $_NB_2$	H

CRT

$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

EDID

Function Table

Input (S)	Function
L	B_0 Connected to A
H	B_1 Connected to A

H = HIGH Logic Level L = LOW Logic Level

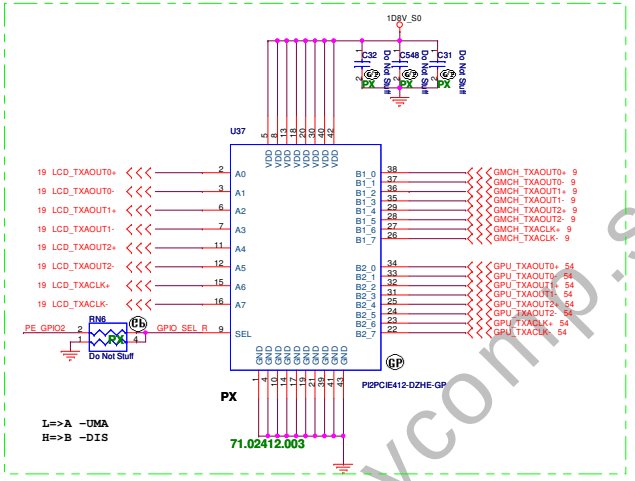
BLON_IN

Function Table

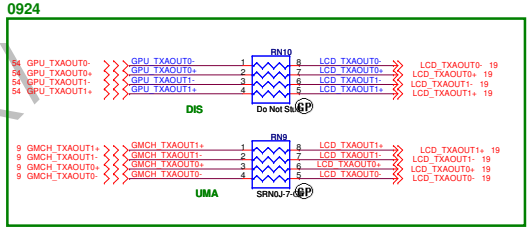
Input (S)	Function
L	B_0 Connected to A
H	B_1 Connected to A

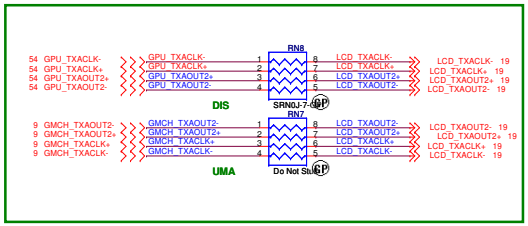
H = HIGH Logic Level L = LOW Logic Level

1023

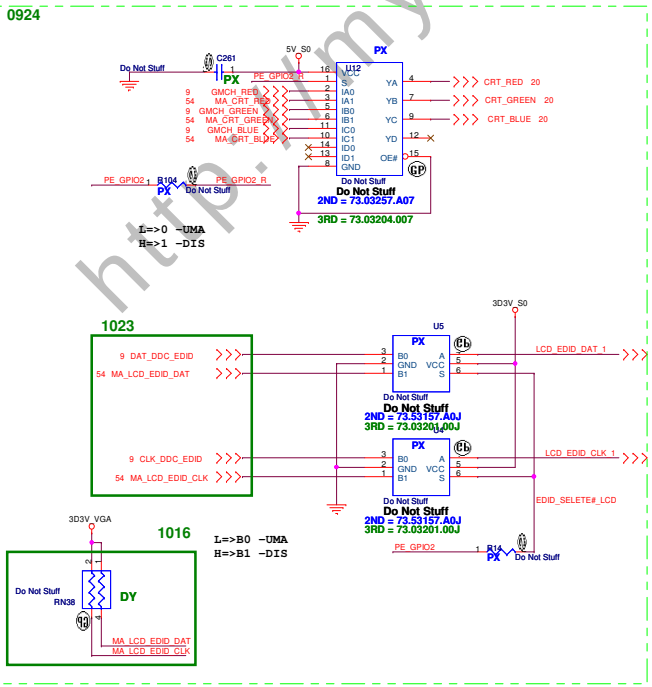


0924

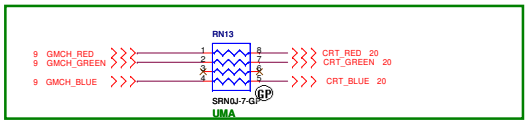


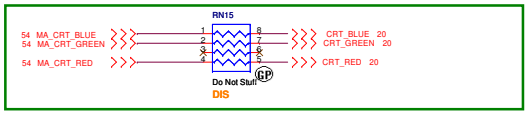


0924

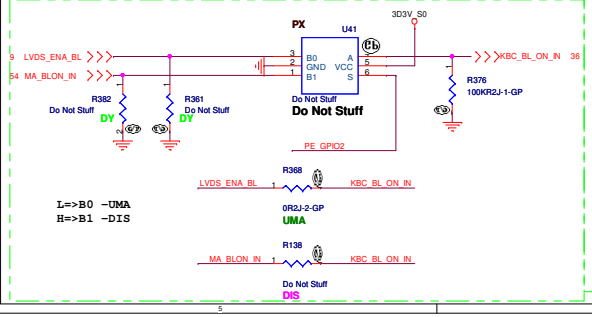


0924



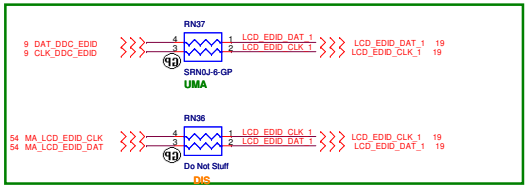


1026



1023

0924



UMA

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Title: PX

Size: A2 | Document Number: JV42-DN | Rev: SA

Date: Monday, November 16, 2009 | Sheet 18 of 63

LCD/INVERTER/CCD CONN

Change PX

0922

Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND

1028 for EMC request

0923

0929 del CCD CON

1005

1026

1016

JV42-DN SA

20.F1093.040

define same as SJM50-PU,can use SJM50 Cable

2nd = 20.F1289.040

JV42_DN SA

JV42_DN_PX SA

Reserve direct connector to KBC

Layout 40 mil

UMA

Wistron Corporation	緯創資通
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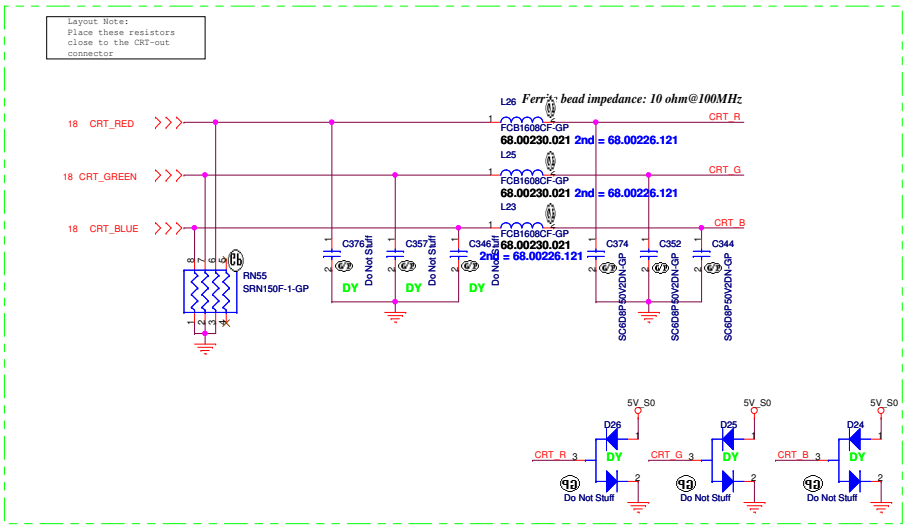
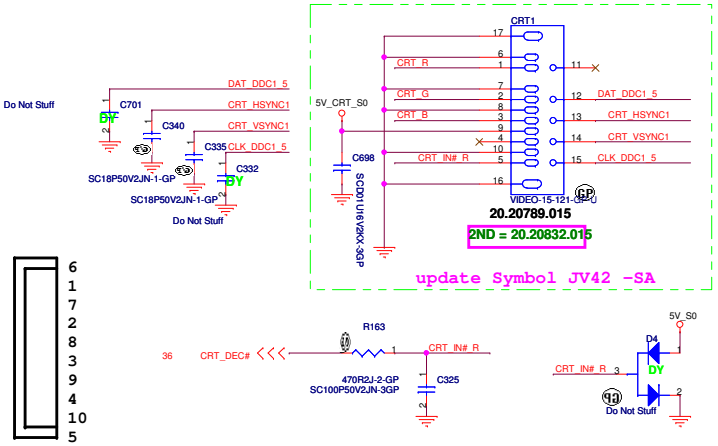
Title: LCD CONN	
Size: Custom	Document Number: JV42-DN	Rev: SA
Date: Thursday, November 05, 2009	Sheet 19 of 63	

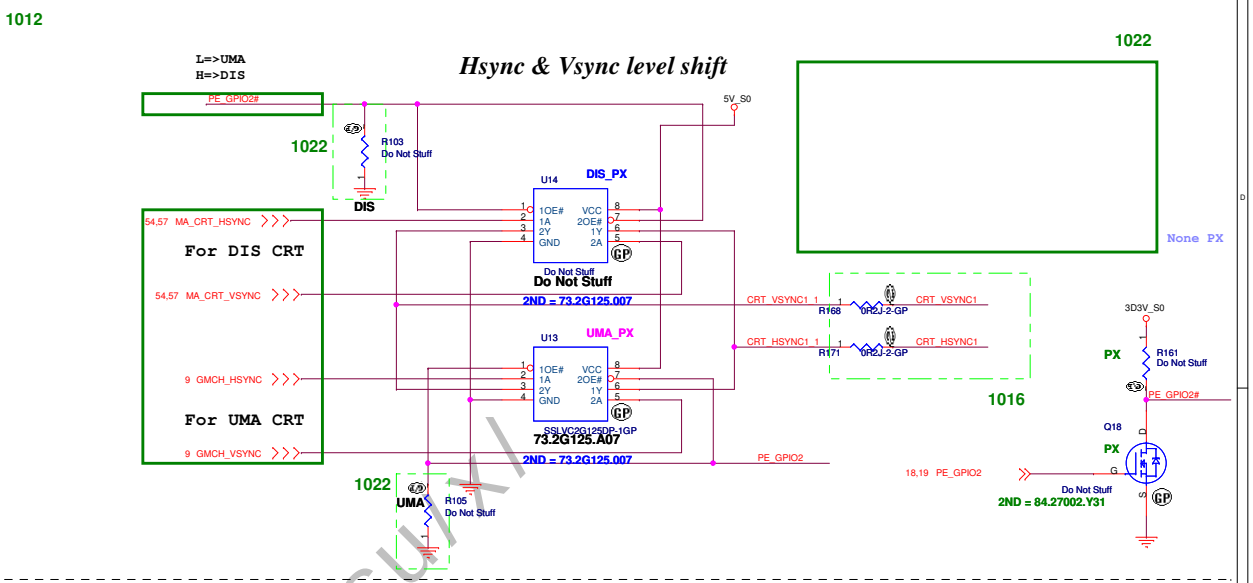


Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

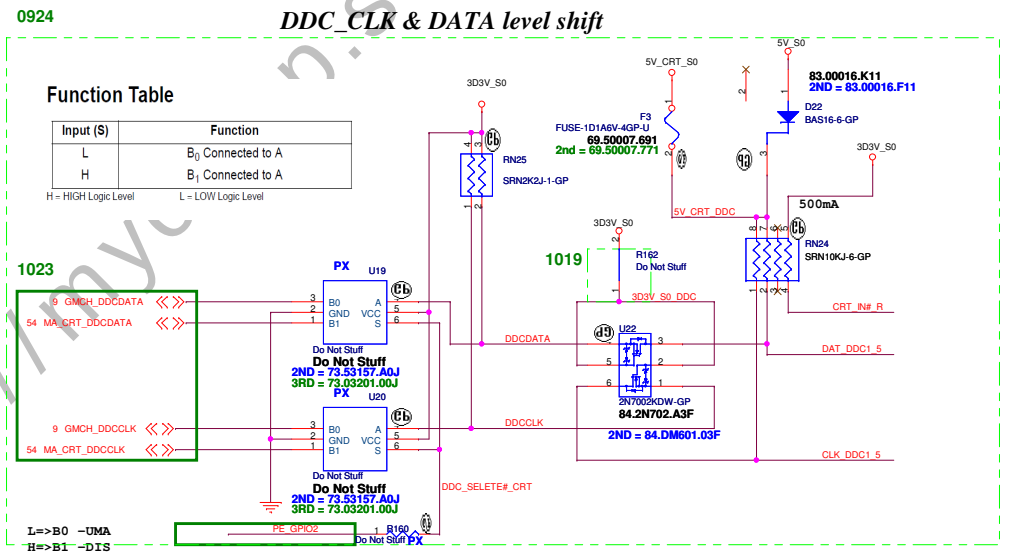
CRT I/F & CONNECTOR

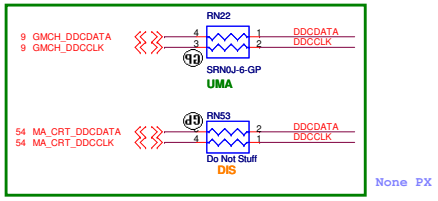


1012



0924





UMA

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Title: **CRT Connector**

Size	Document Number	Rev
	JV42-DN	SA

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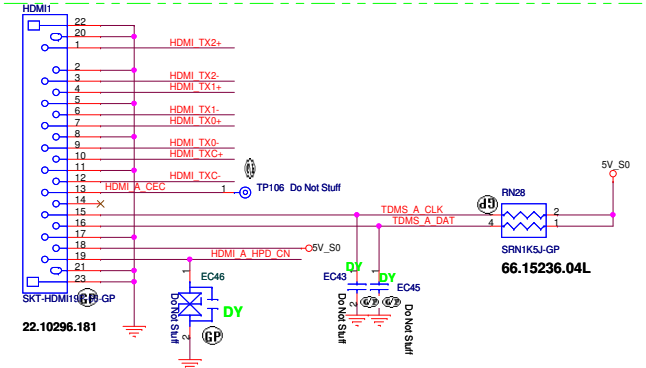
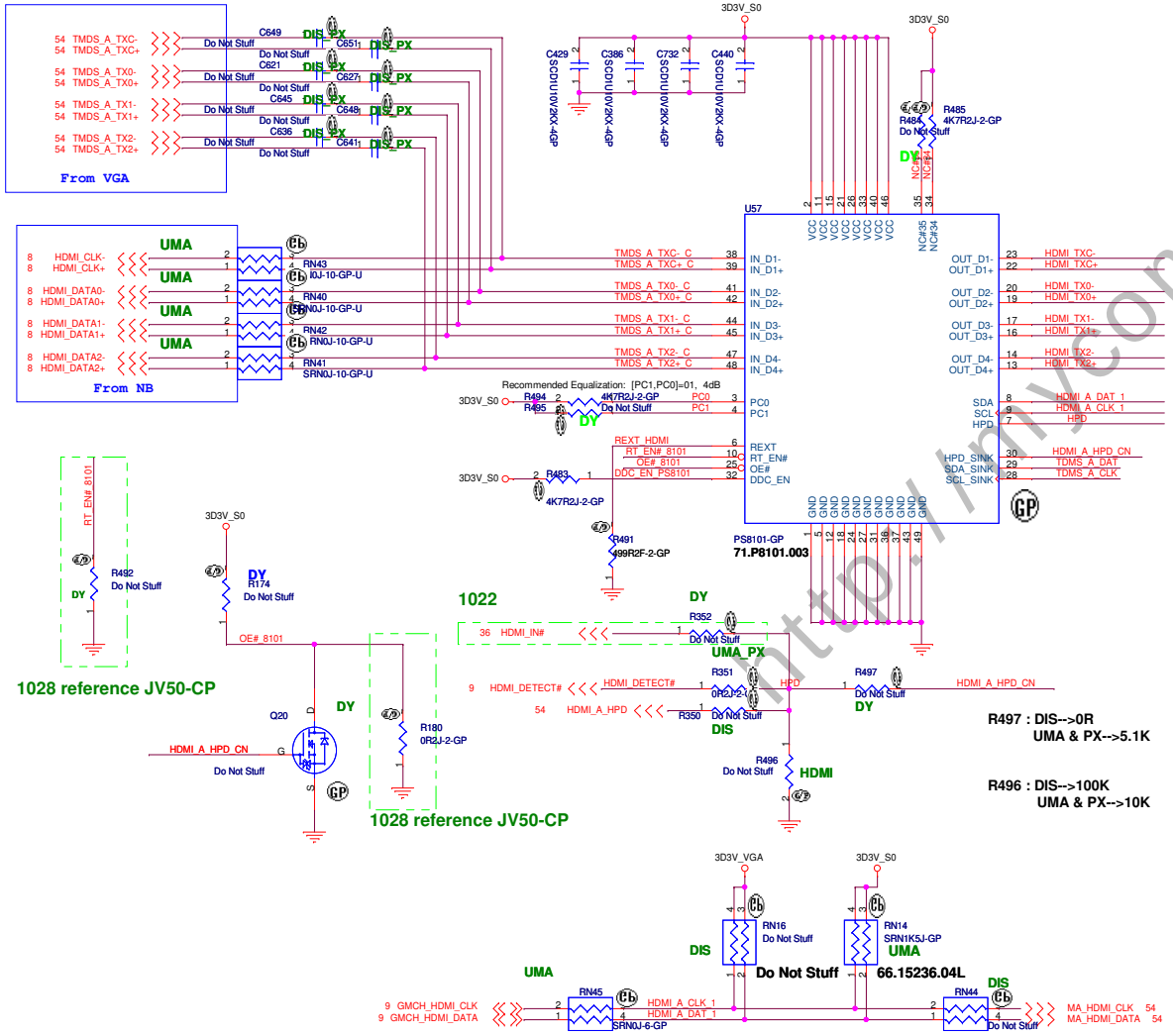
1026 for Layout request

1012





1026 for Layout request

1026 for Layout request

UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Connector

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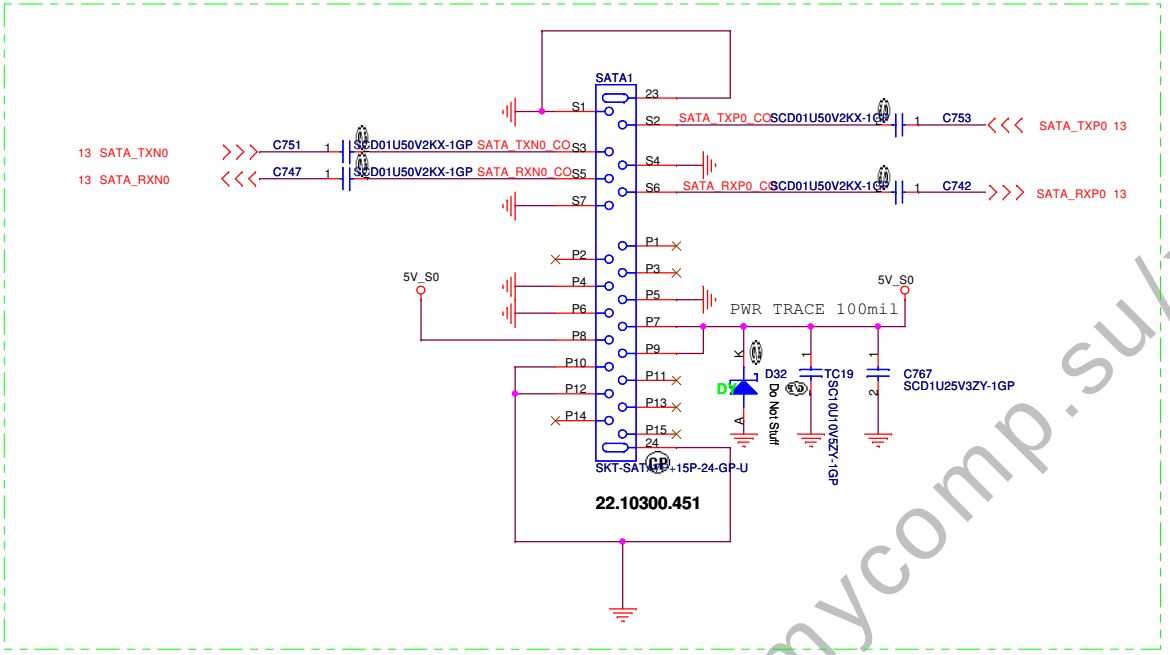
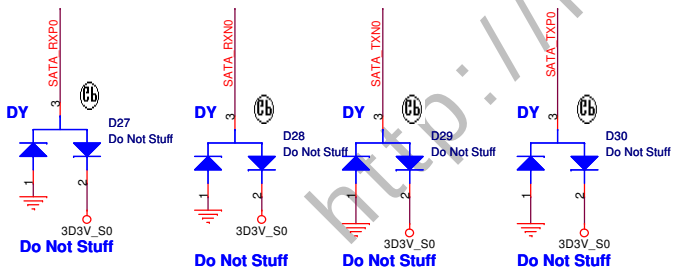
SATA Connector

0923





UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD

Size | Document Number: JV42-DN | Rev: SA

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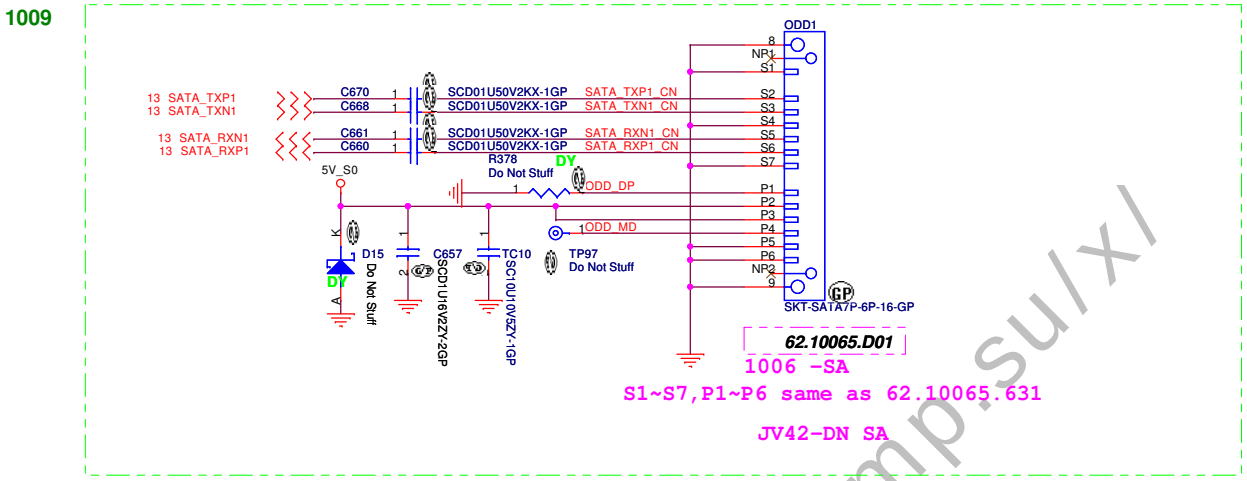
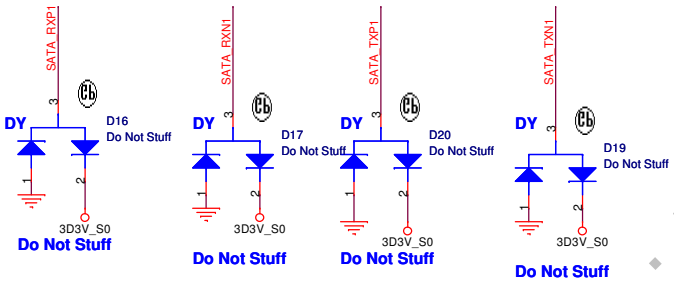
ODD Connector





UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title		
ODD		
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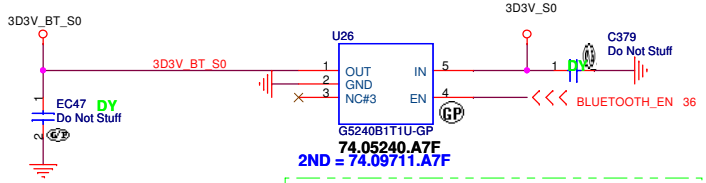
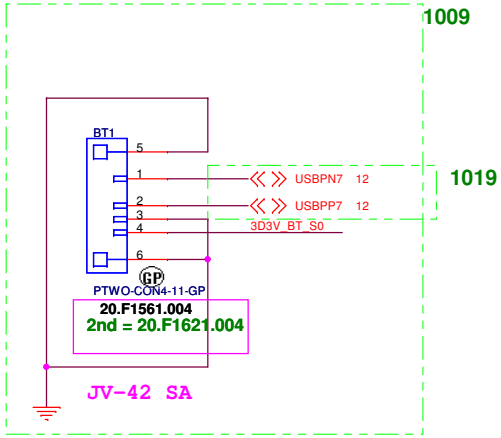
BLUETOOTH MODULE

1.5A / High Active Voltage 2V



EC21 put near
BLUE1 / all
USB put one
choke near
connector by
EMI request



Pin 1 ->right side
20.D0197.104 Pin1 -> left side
change net sequence
can us JV50-CP Cable

UMA

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Title: BLUETOOTH		
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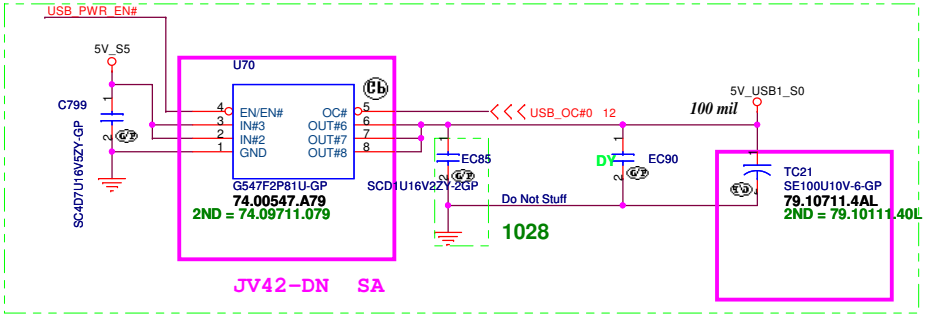
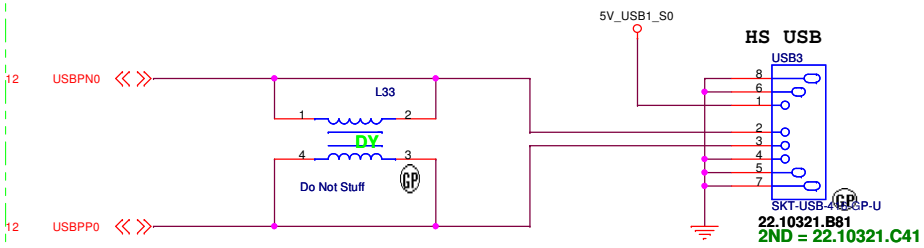
0910

0914

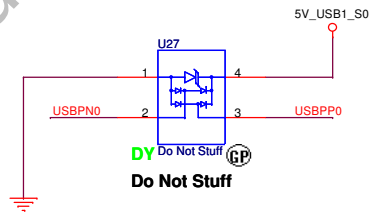


1028 for EMC request



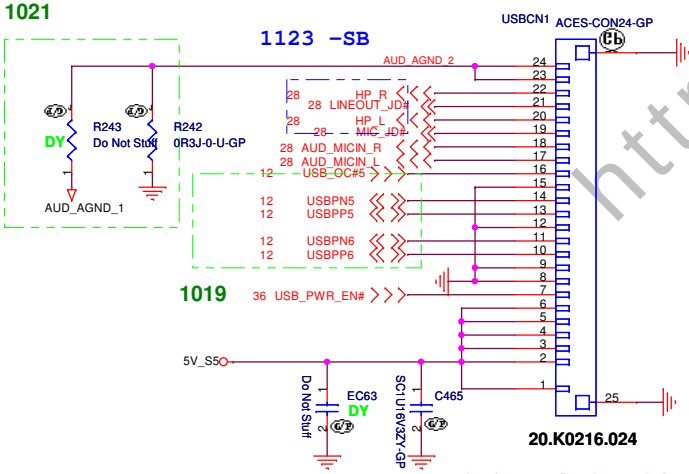
Pin1 -> right side
22.10218.T51 Pin1 -> left side (JV42-DN)

change Net sequence



0910

1021



Pin1 -> left side

UMA

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Title: USB		
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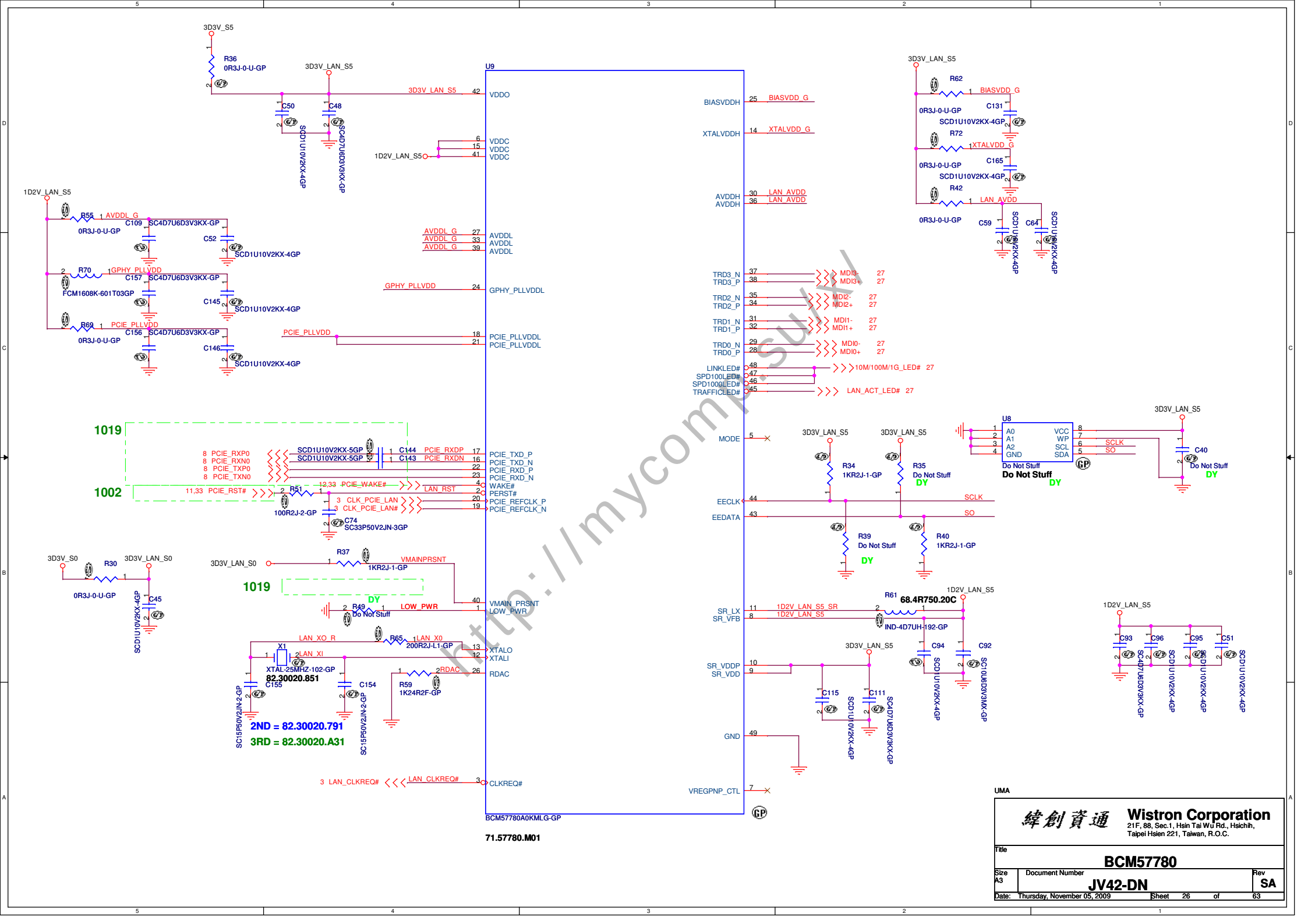
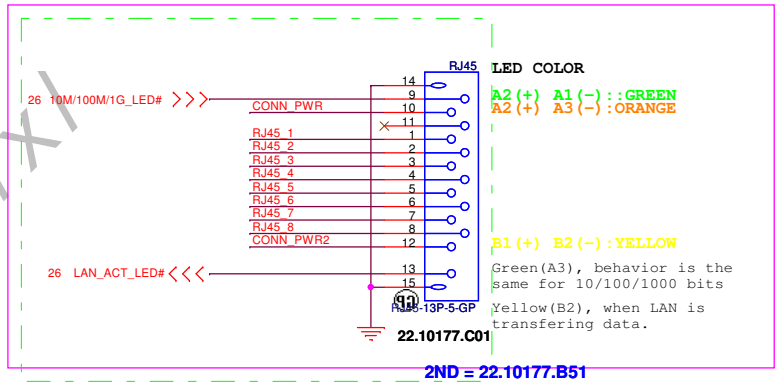


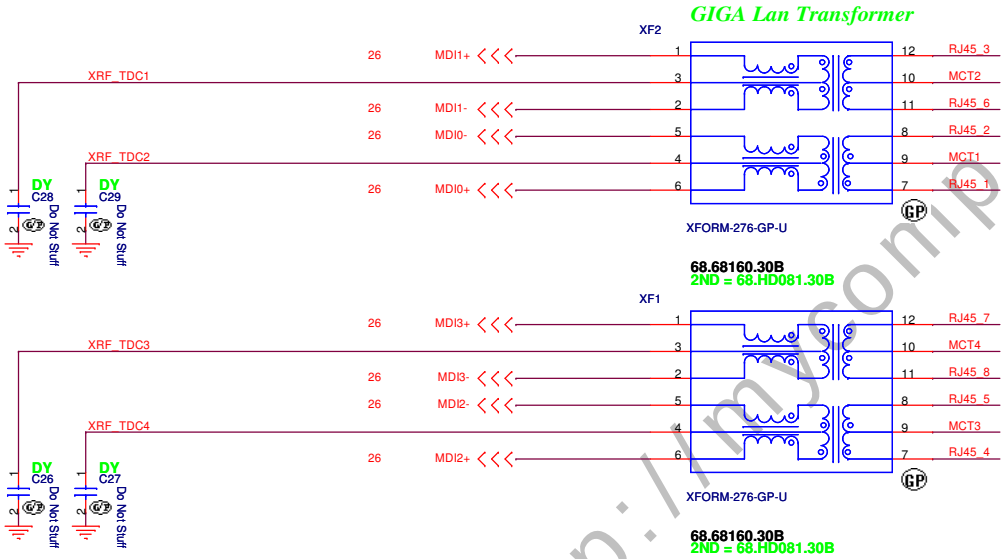
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

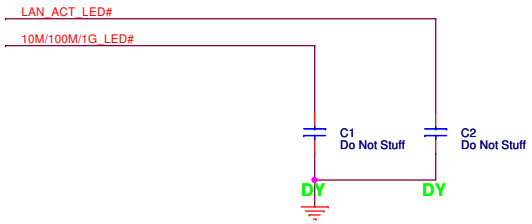
LAN Connector

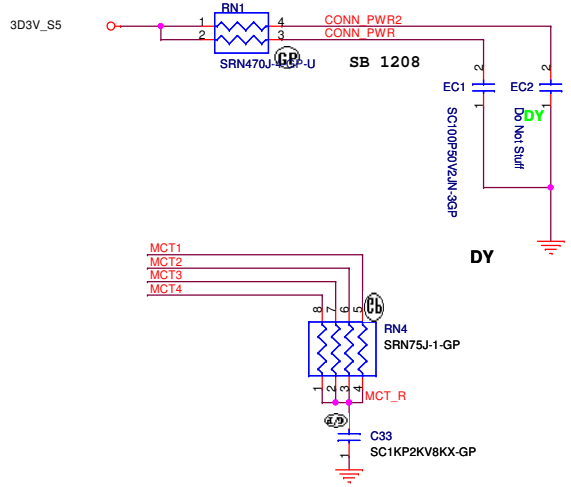
LAN Connector

0923









UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN CONN

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A3	JV42-DN	SA

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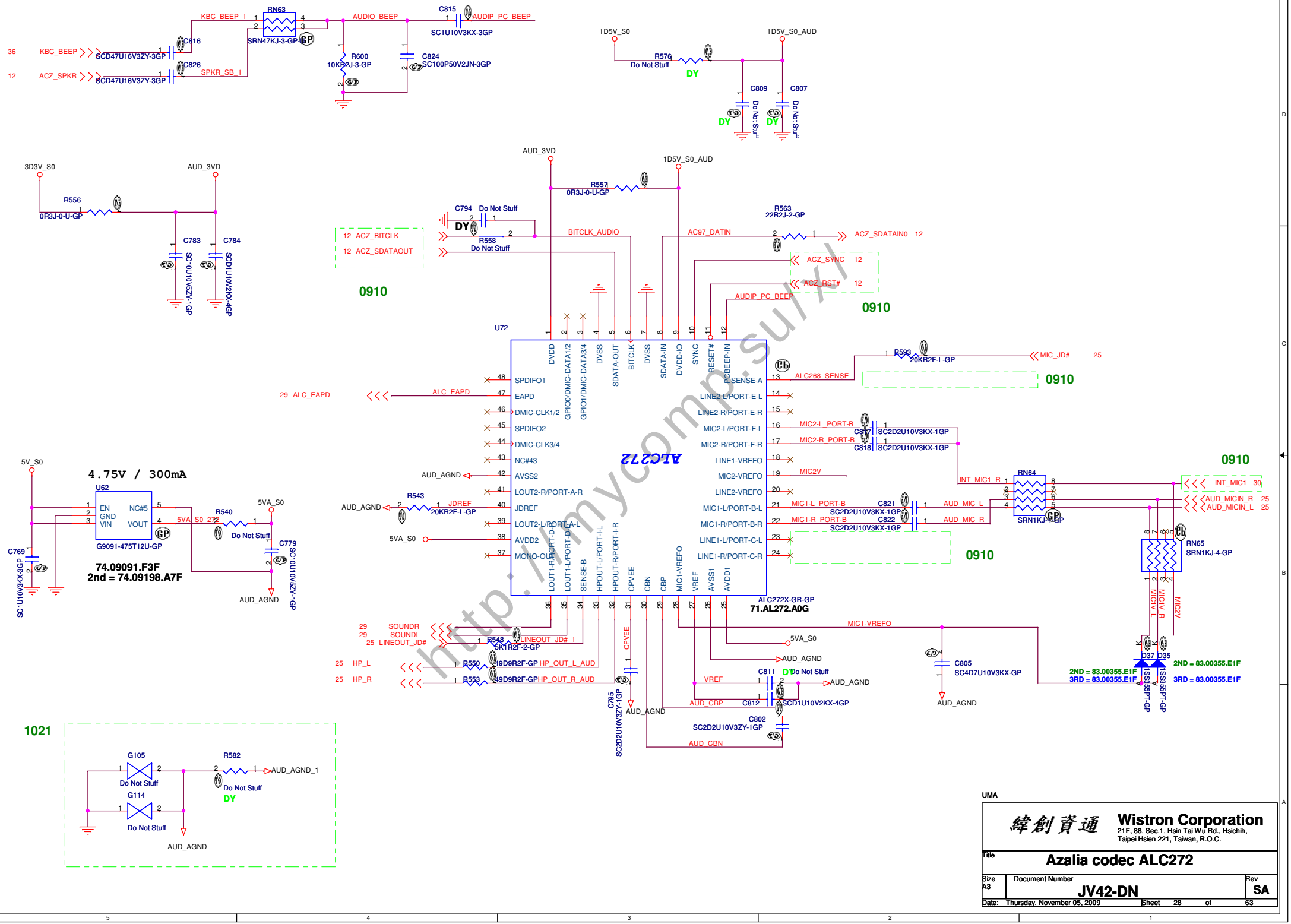

UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Azalia codec ALC272**

Size	Document Number	Rev
A3	JV42-DN	SA

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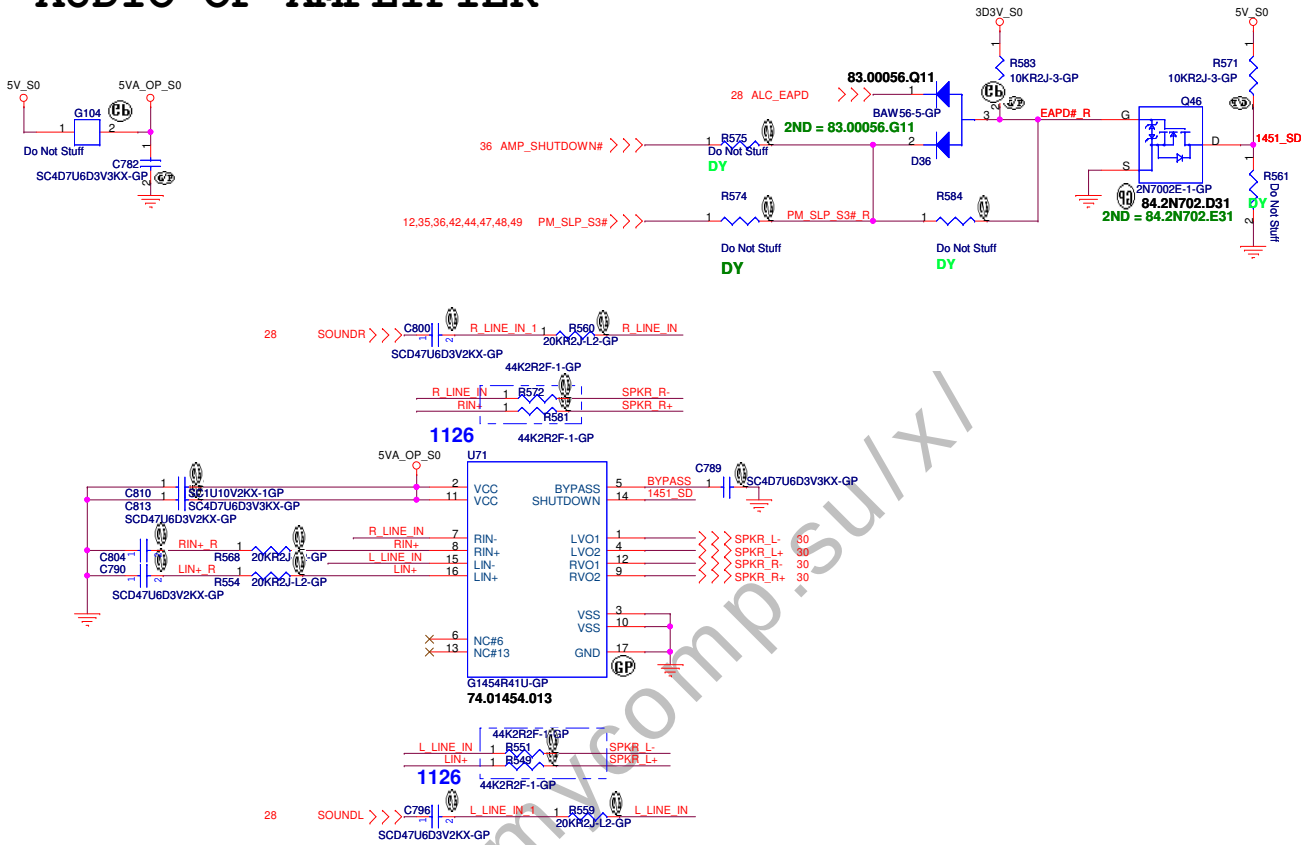
AUDIO OP AMPLIFIER



Gain= Rf/Ri=52K/20K=2.6V/V
f(HP)=1/(2 Pi*20K*0.47uf)=16.9Hz
If VIN= 1.54V Gain=2.6V/V RL=4Ω VO(peak) = 4V V(rms)=2.828V
Power= 2.828^2/4=1.999W

UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
AUDIO AMP		
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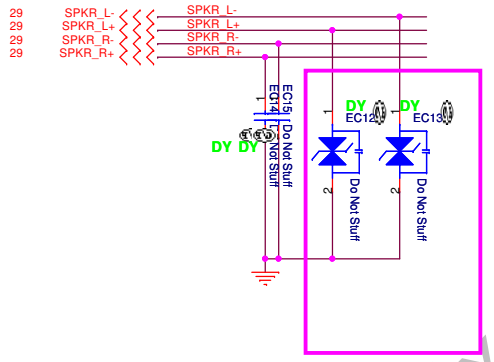
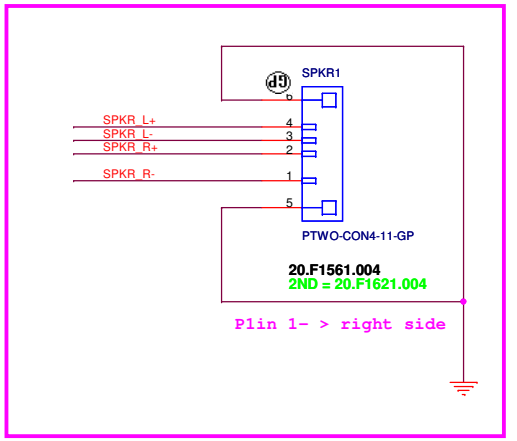
	JV42-DN	SA
Date: Thursday, November 26, 2009	Sheet 29 of 63	

Internal Speaker

0914

0910





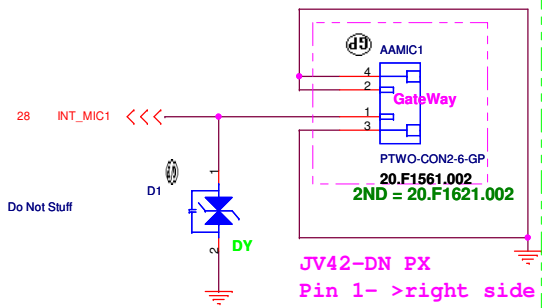
0910

LINE OUT

0911

1016

Internal Mic



UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO JACK

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No Modem Function

UMA

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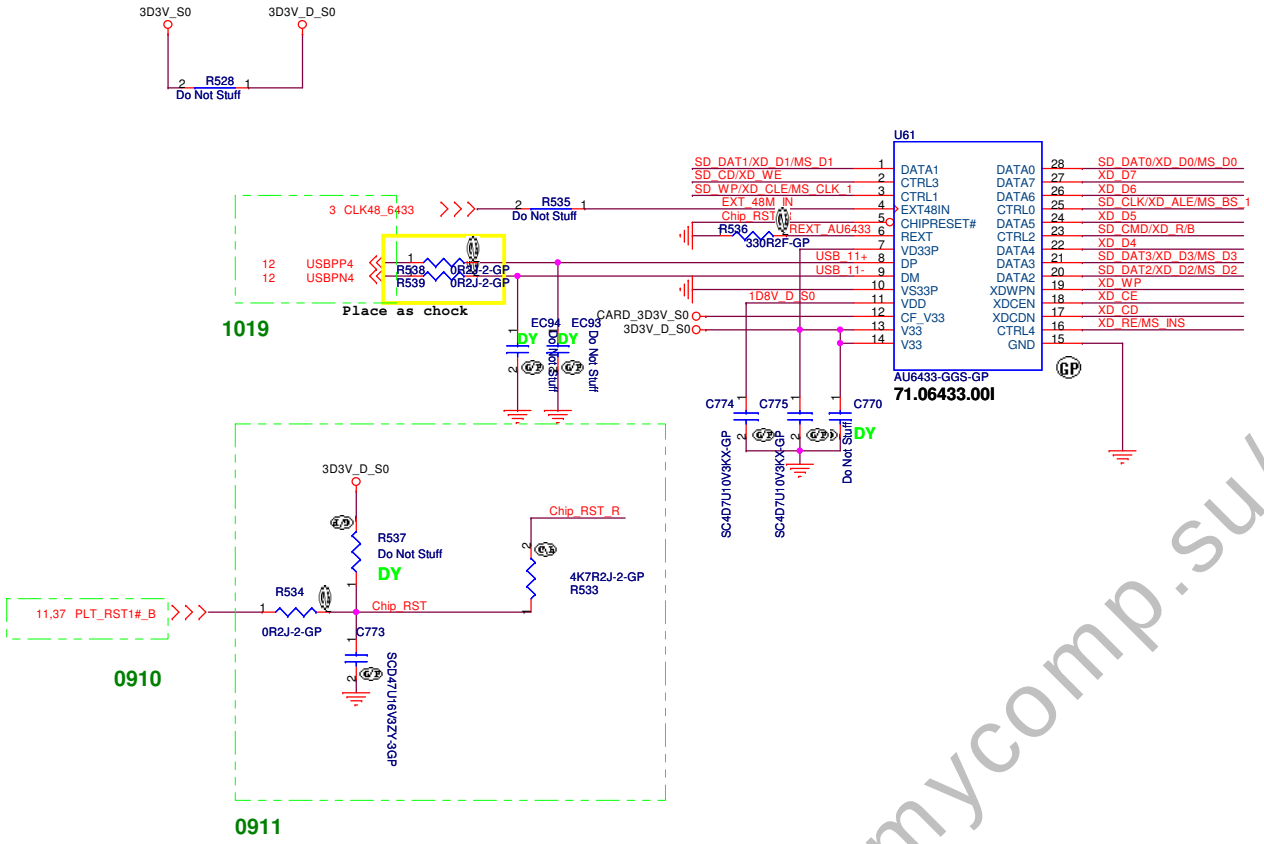
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

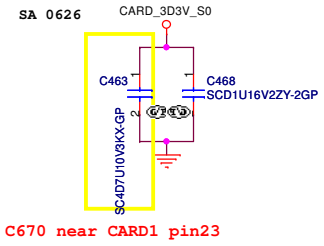
Title: MDC

Size | Document Number: JV42-DN | Rev: SA

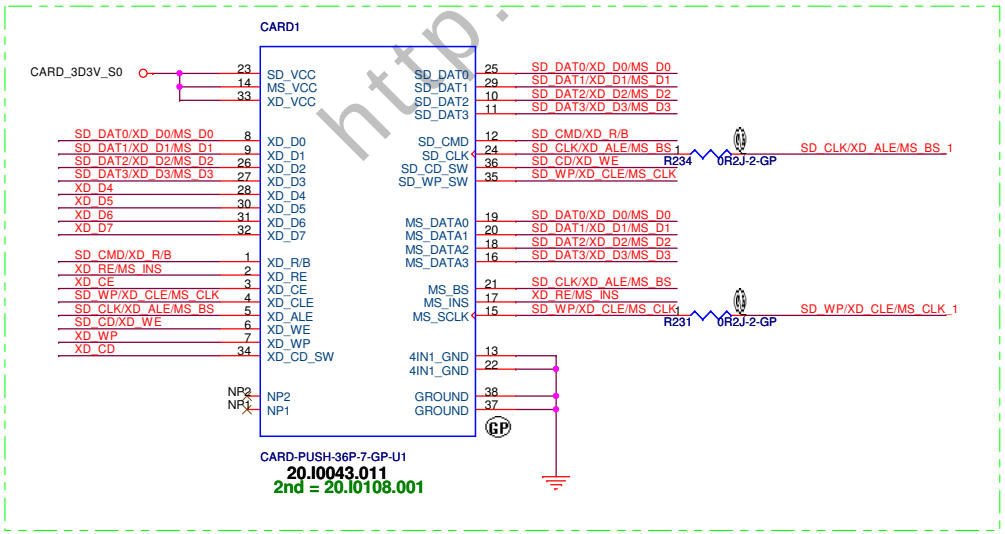
Date: Thursday, November 05, 2009 | Sheet 31 of 63



5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)

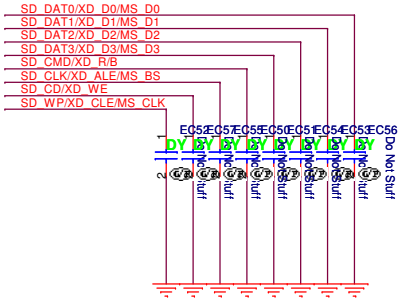


C670 near CARD1 pin23



0914

EMI capacitor



UMA

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Title: CARDREADER		
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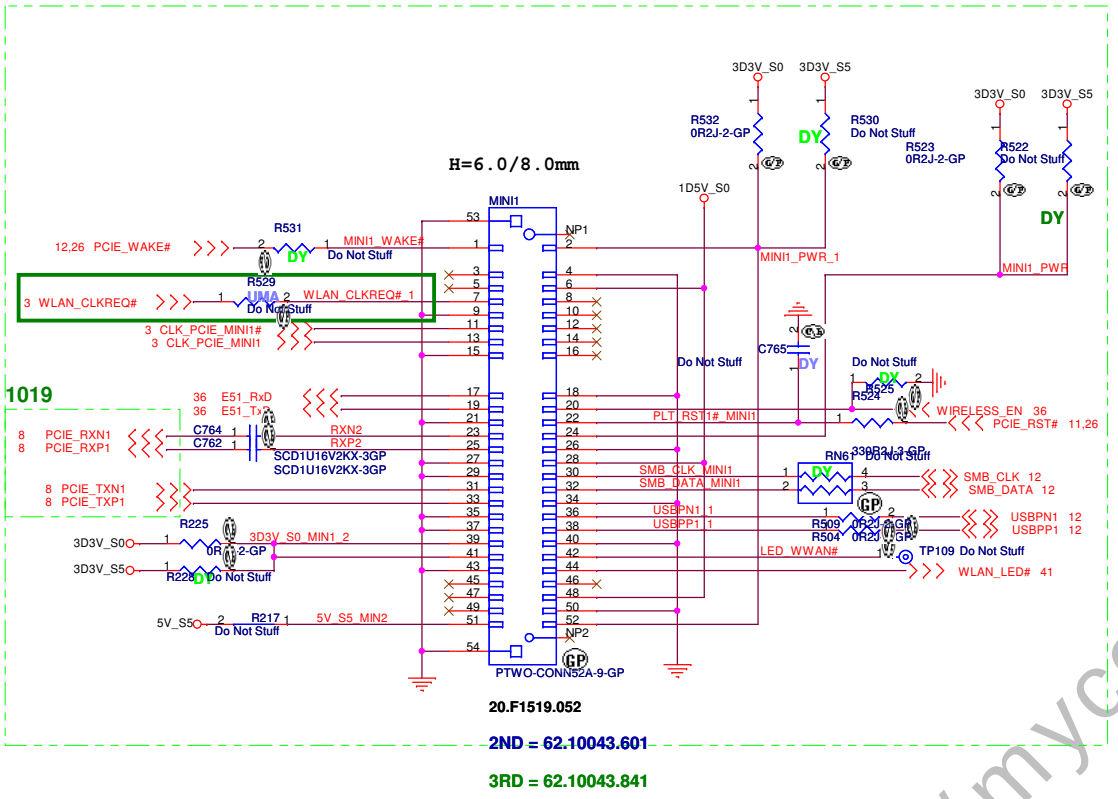
Mini Card Connector(WLAN)

0923

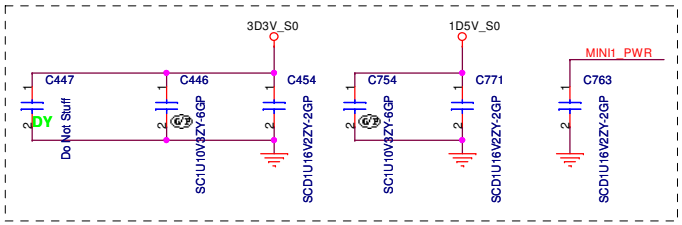


20.F1519.052

2ND = 62.10043.601

3RD = 62.10043.841

Place near MINI1



No Mini Card Function (Robson2 and 3G)

UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MINI CARD		
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No NEWCARD Function

UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **NEW CARD**

Size	Document Number	Rev
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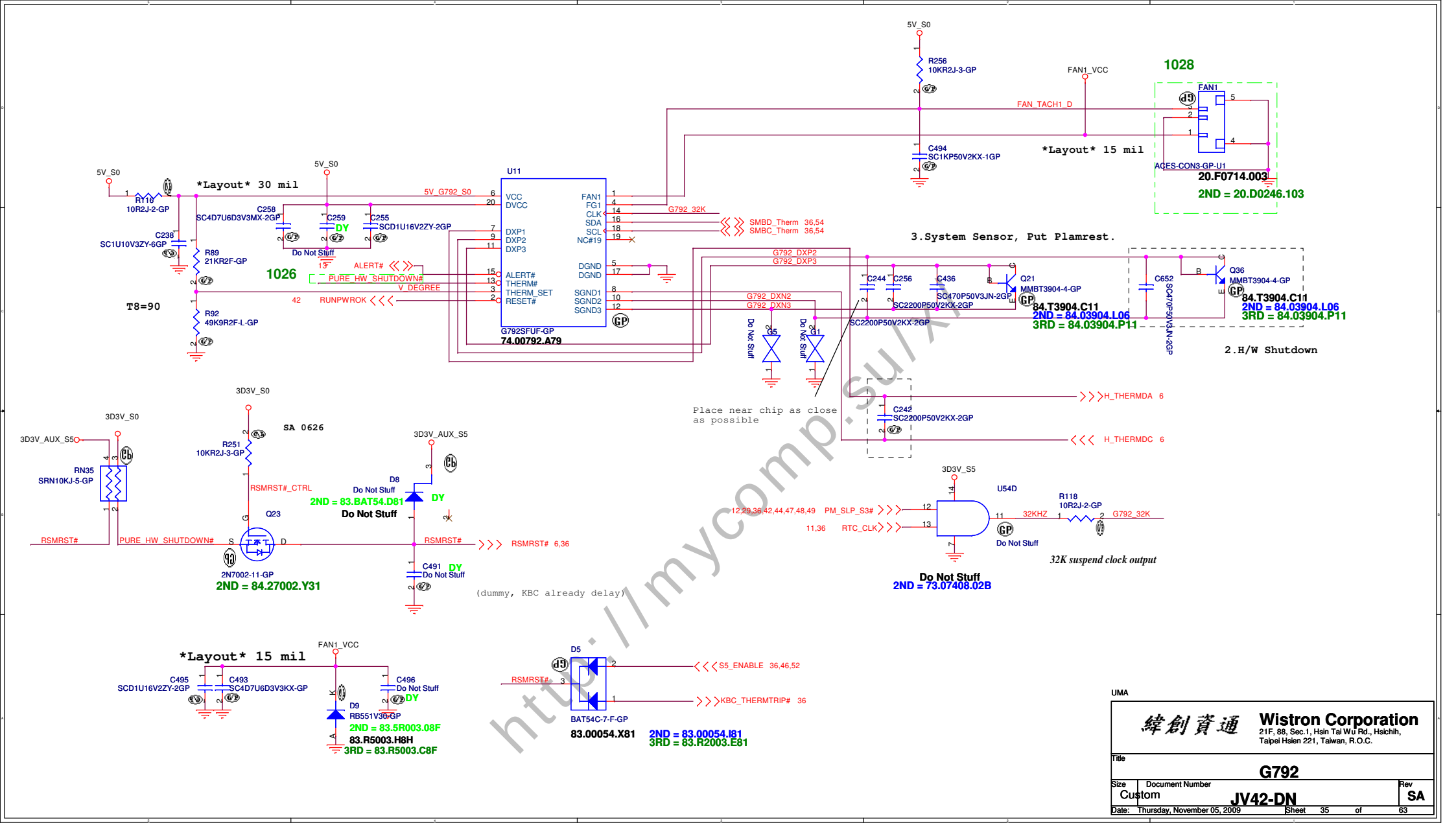

UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	G792	
Size: Custom	Document Number: JV42-DN	Rev: SA
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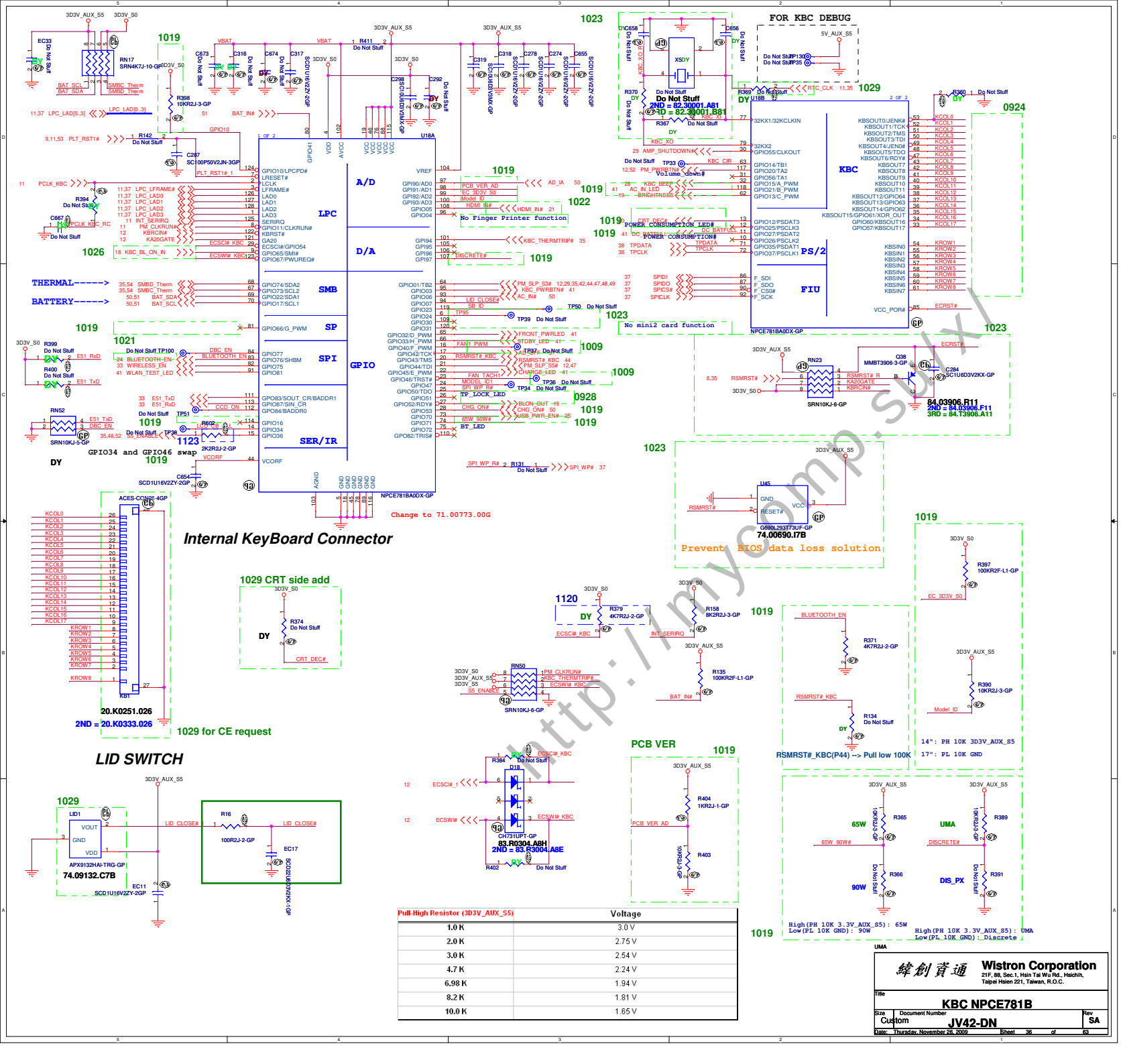
FOR KBC DEBUG
KBC
PS/2
FIU
LPC
A/D
D/A
SMB
SP
SPI
GPIO
SER/IR
NPCE781BA0DX-GP
No Finger Printer function
No mini2 card function
THERMAL------>
BATTERY------>
GPIO34 and GPIO46 swap
Internal KeyBoard Connector
20.K0251.026
2ND = 20.K0333.026
1029 for CE request
1029 CRT side add
LID SWITCH
74.09132.C7B
74.00690.I7B
84.03906.R11
2ND = 84.03906.F11
3RD = 84.T3906.A11
2ND = 82.30001.A81
3RD = 82.30001.B81
83.R0304.A8H
2ND = 83.R3004.A8E
Change to 71.00773.00G
Prevent BIOS data loss solution
RSMRST#_KBC(P44) --> Pull low 100K
14": PH 10K 3D3V_AUX_S5
17": PL 10K GND
High(PH 10K 3.3V_AUX_S5): 65W
Low(PL 10K GND): 90W
High(PH 10K 3.3V_AUX_S5): UMA
Low(PL 10K GND): Discrete
PCB VER
Pull-High Resistor (3D3V_AUX_S5)
Voltage
1.0 K 3.0 V
2.0 K 2.75 V
3.0 K 2.54 V
4.7 K 2.24 V
6.98 K 1.94 V
8.2 K 1.81 V
10.0 K 1.65 V
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC NPCE781B
Custom
JV42-DN
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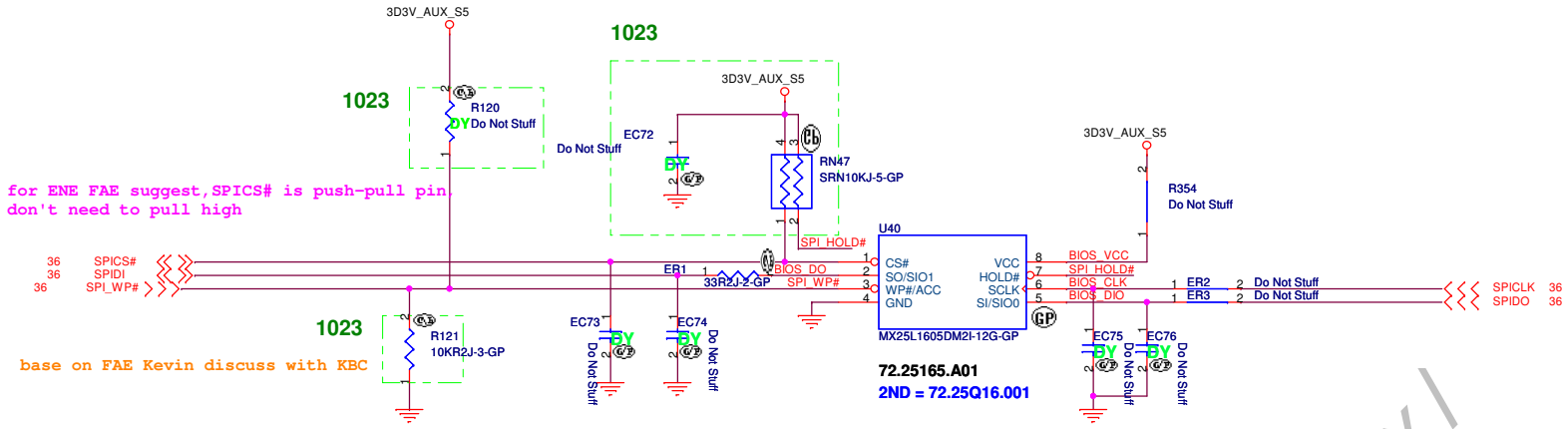
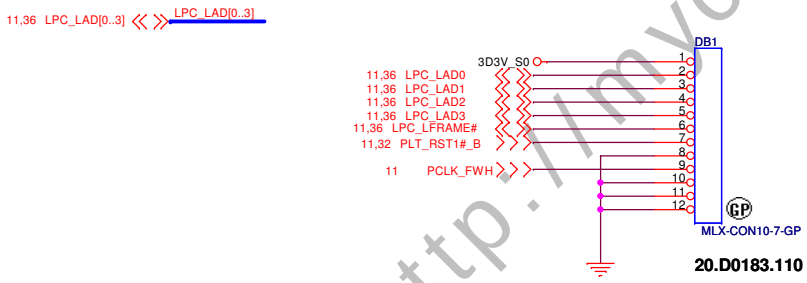


16M Bits

SPI FLASH ROM

GOLDEN FINGER FOR DEBUG BOARD



UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: BIOS

Size: A3 | Document Number: JV42-DN | Rev: SA

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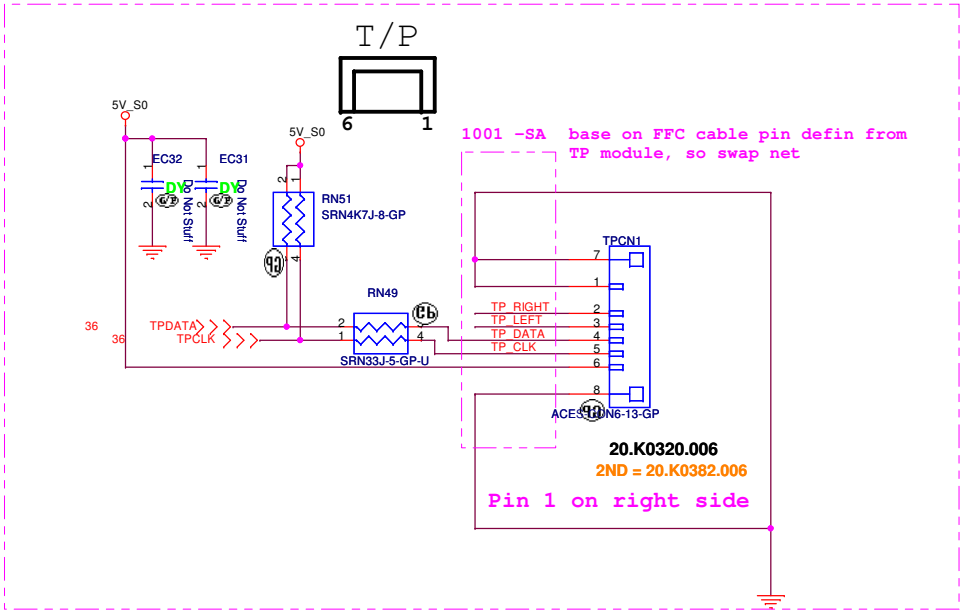

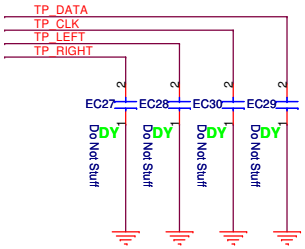

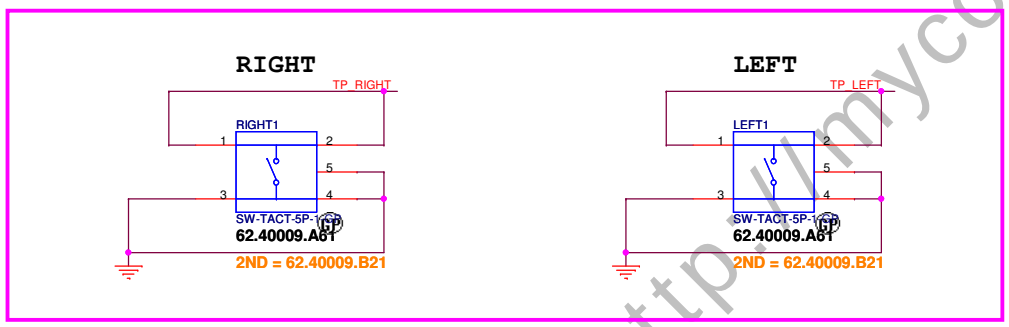

No Finger printer Function

UMA

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Title		
Touch PAD		
Size: A3	Document Number: JV42-DN	Rev: SA
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NONE BOARD

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Taipei Hsien 221, Taiwan, R.O.C.

Title: NONE BOARD

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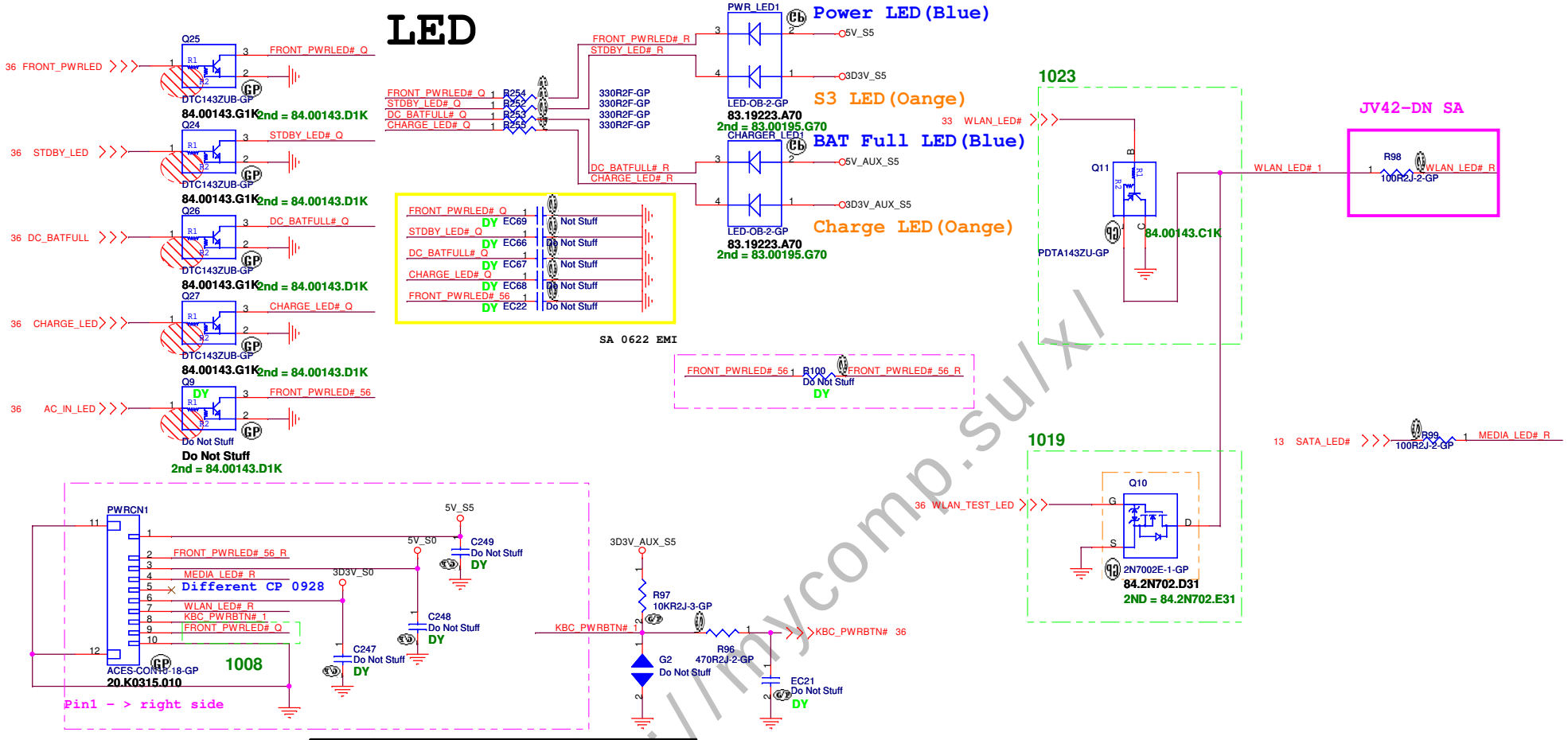
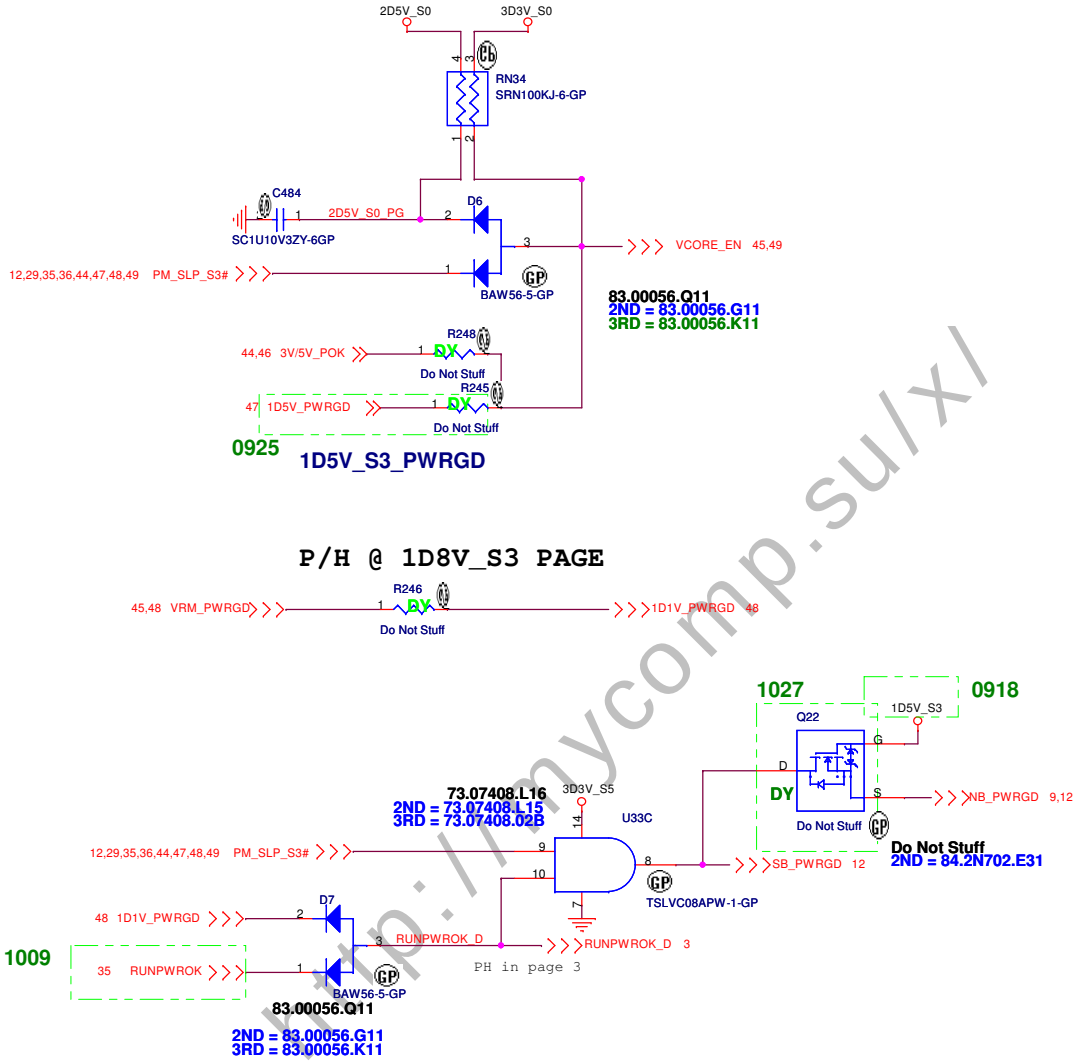
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: SWITCH		
Size: A2	Document Number: JV42-DN	Rev: SA
Date: Thursday, November 05, 2009	Sheet 40 of 63	

LED



Pin 1	5V_S5	
Pin 2	(DY)FRONT_PWRLED#_56_R	AC IN
Pin 3	5V_S0	
Pin 4	MEDIA_LED#_R	HDD
Pin 5	3G_LED#_R	3G
Pin 6	3D3V_S0	
Pin 7	WLAN_LED#_R	WLAN
Pin 8	KBC_PWRBTN#_1	Power button
Pin 9	NC	
Pin 10	GND	

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: LED		
Size: A3	Document Number: JV42-DN	Rev: SA
Date: Thursday, November 05, 2009	Sheet 41 of 63	



UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER ON LOGIC

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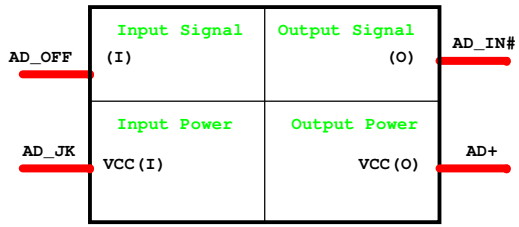
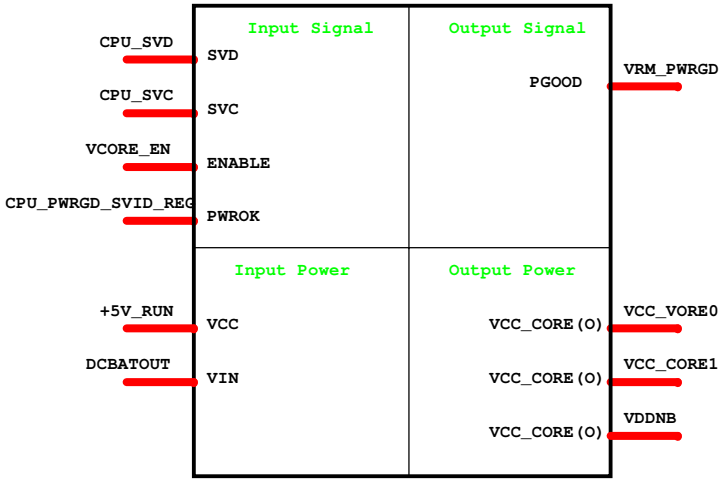
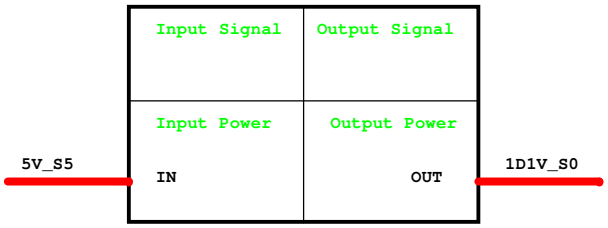
Adapter



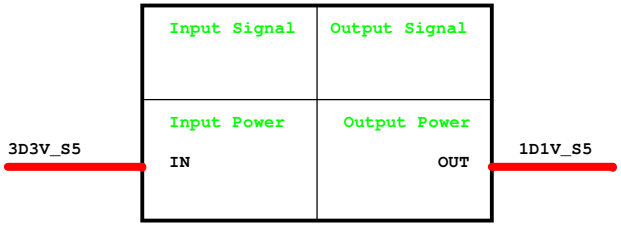
CPU_CORE
ISL6265HRTZ



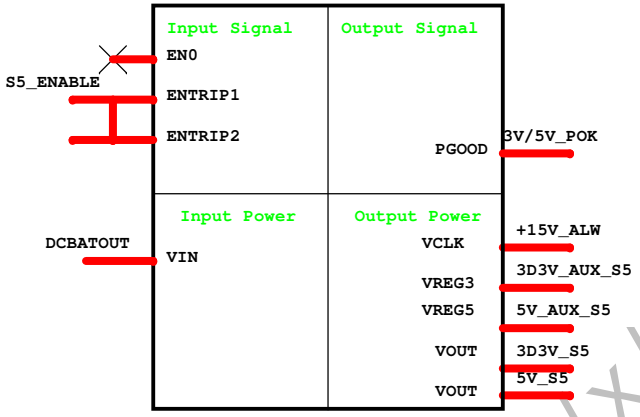
1D1V LDO RT8209E



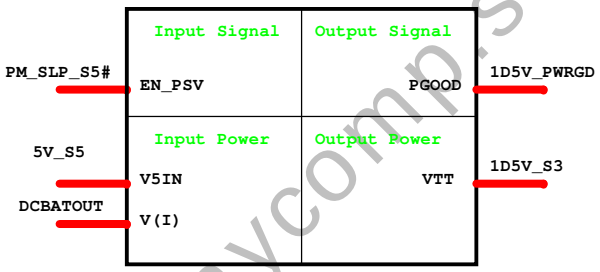
1D1V LDO RT9025



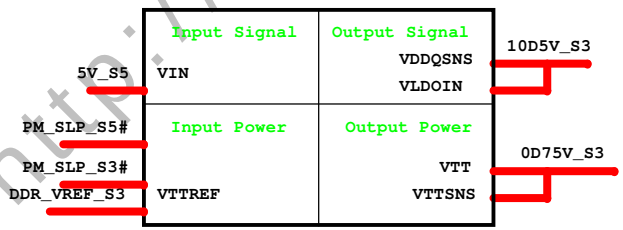
DCDC 5V/3D3V(RT8223)



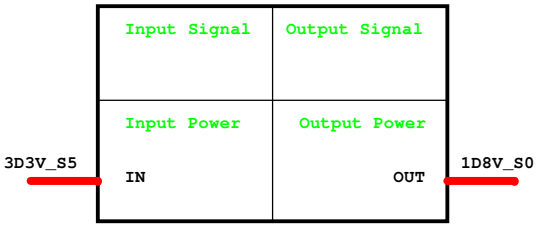
DCDC 1D5V(RT8209E)



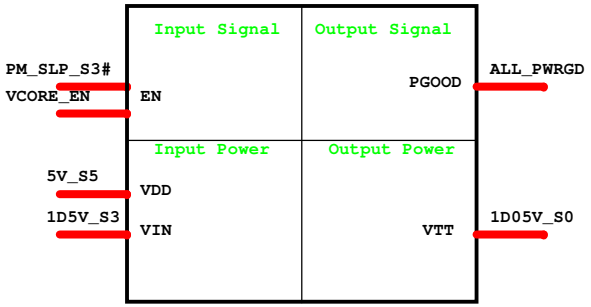
0D75V LDO RT9026



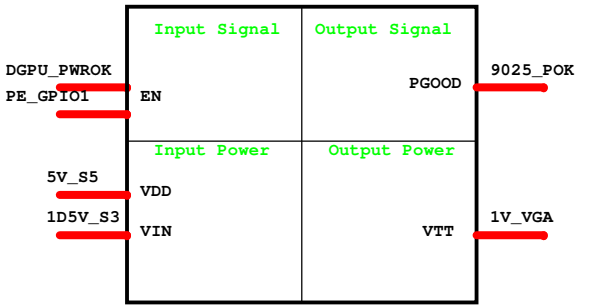
1D8V LDO RT8015A



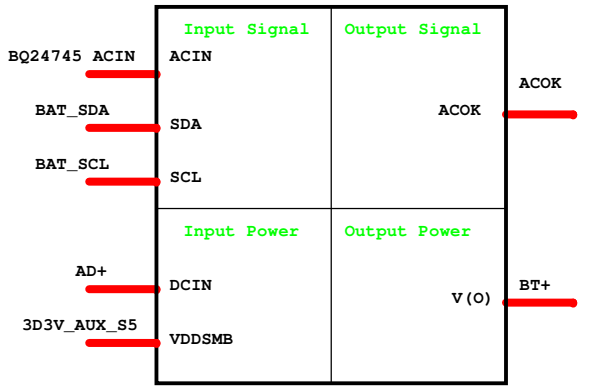
DCDC 1D05V_S0(RT9025)



DCDC 1V_VGA(RT9025)



CHARGER BQ24745



UMA

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Title: Power Block Diagram

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Run Power

Aux Power

3D3V_AUX_S5

I min = 150 mA

U32

Do Not Stuff

Do Not Stuff

2nd source:74.09198.G7F

SB For 2KV ESD protect

1008

+3VS to 3.3V_DELAY Transfer

3D3V_VGA discharge CKT

Do Not Stuff

2ND = 84.27002.Y31

0922

0918

0918

1008

1021

1021

1021

Please closed U77 for Park issue

1022

UMA

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Title: RUN AND AUX POWER

Size: Custom | Document Number: JV42-DN | Rev: SA

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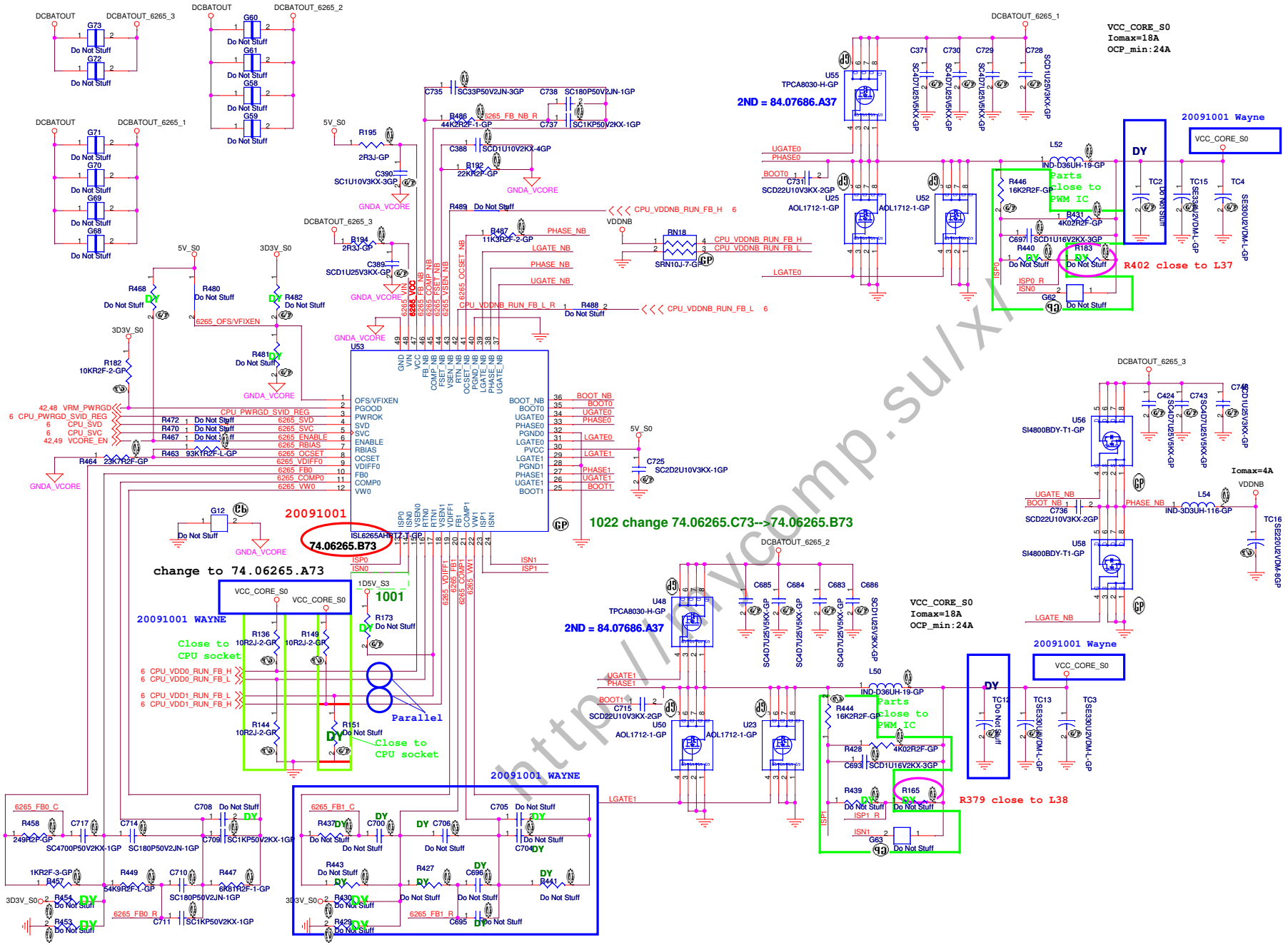

UMA

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Title: **CPU Vcore(ISL6265HR)**

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Custom	JV42-DN	SB

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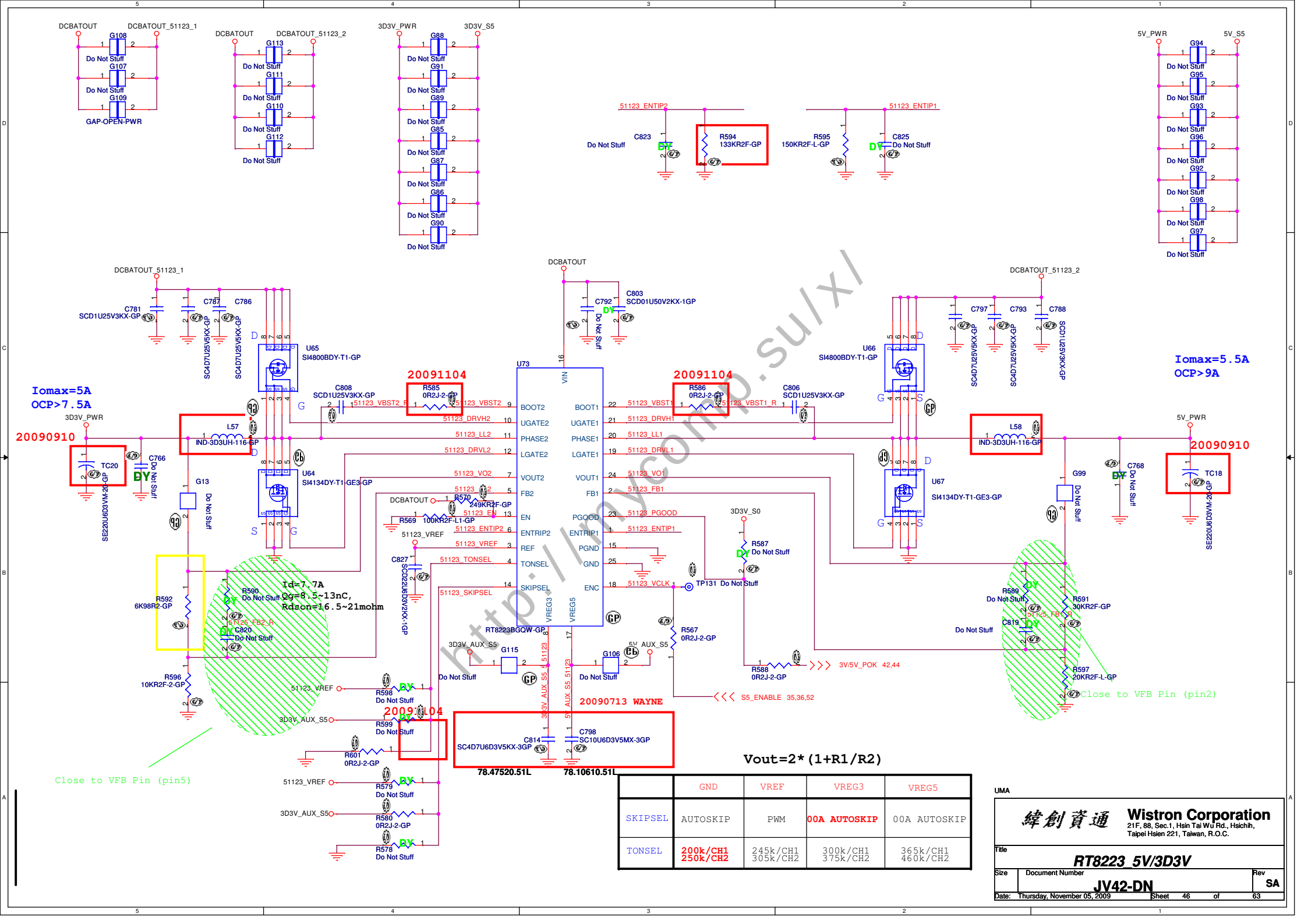

	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

UMA

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Title: RT8223_5V/3D3V

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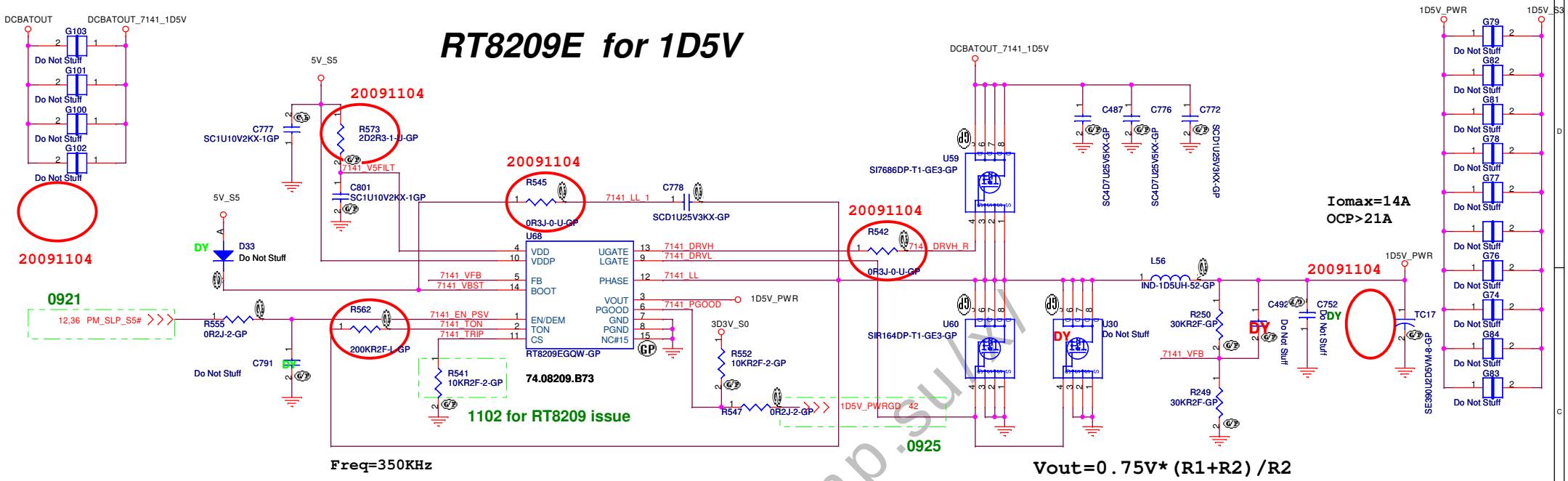
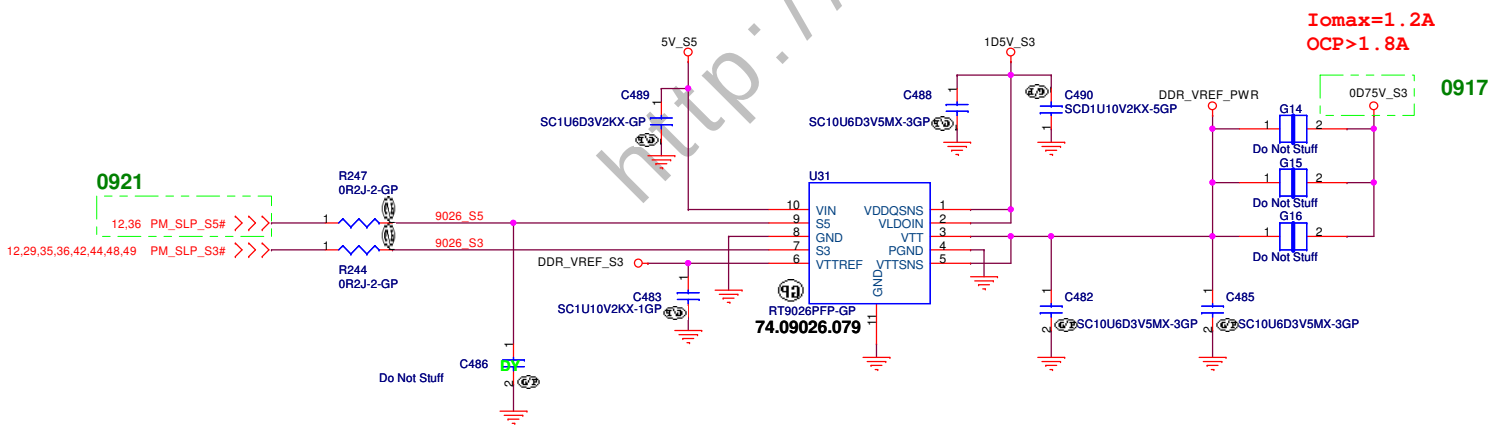
RT8209E for 1D5V



RT9026 for 0D75V_S3



UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8209E 1D5V

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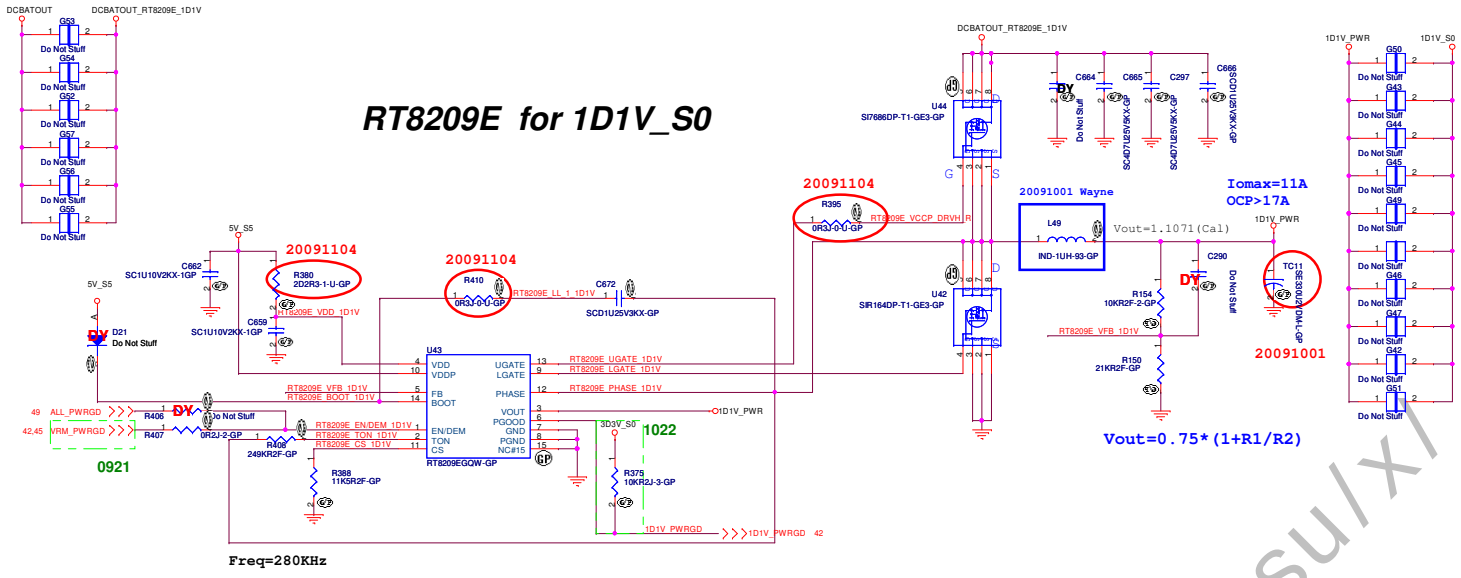

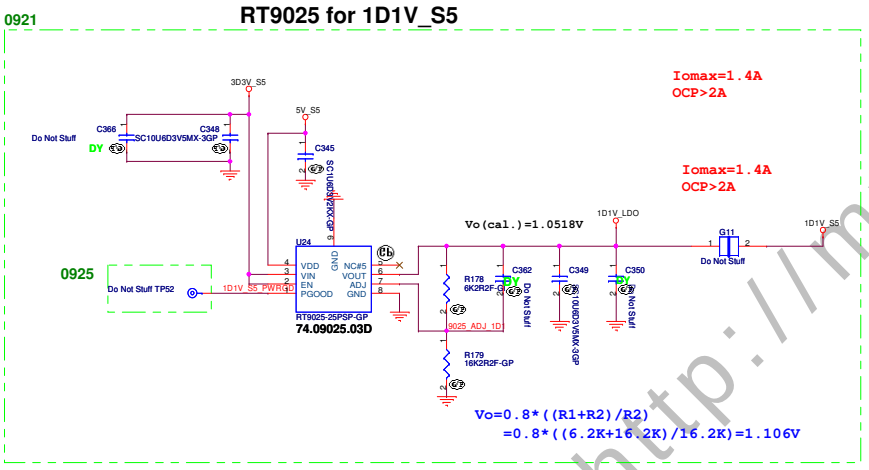

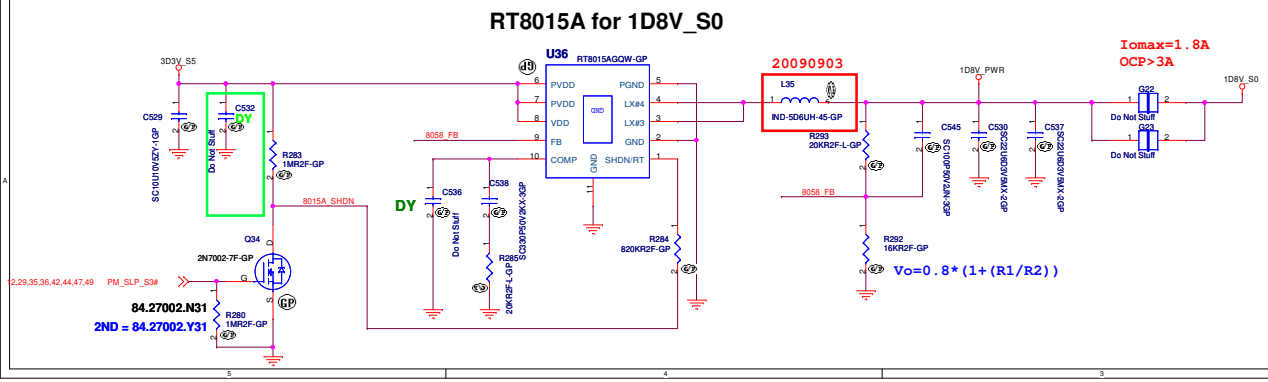

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Taipei Hsien 221, Taiwan, R.O.C.

Title: 1D1V_S0 & 1D1V_S5 & 1D8V_S0

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	JV42-DN	SA

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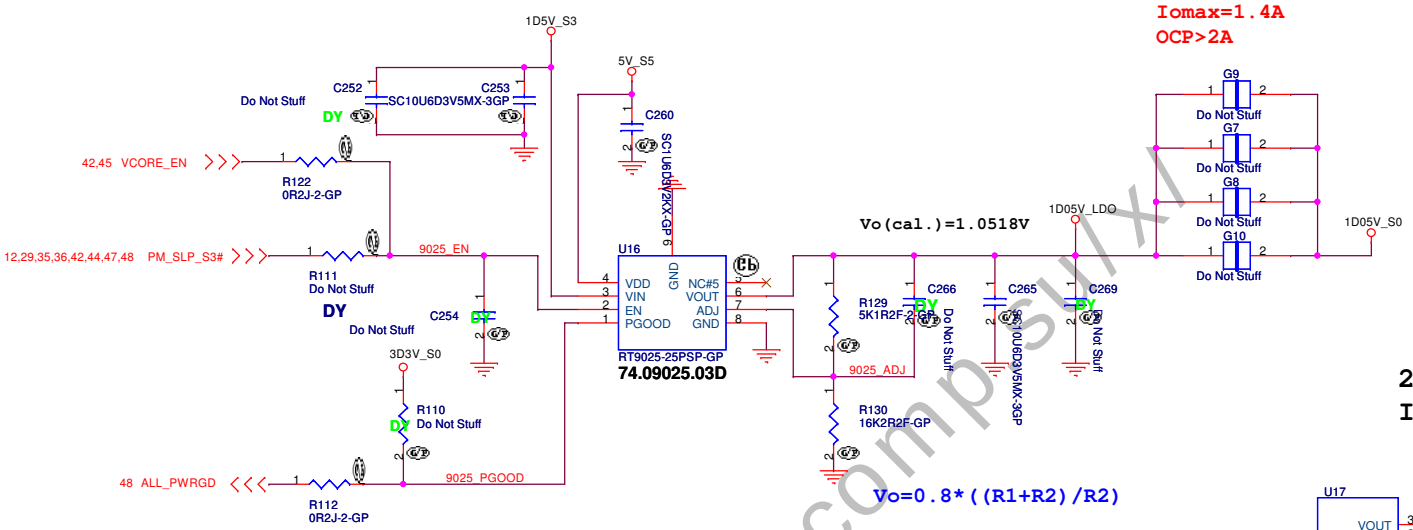
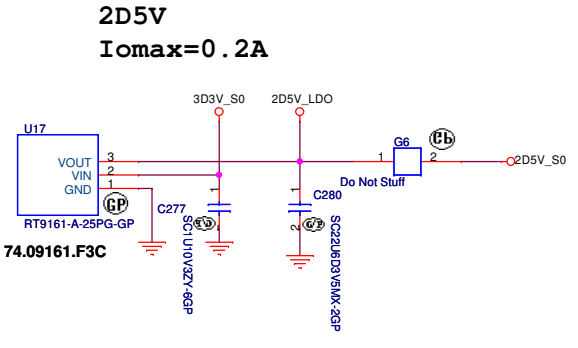
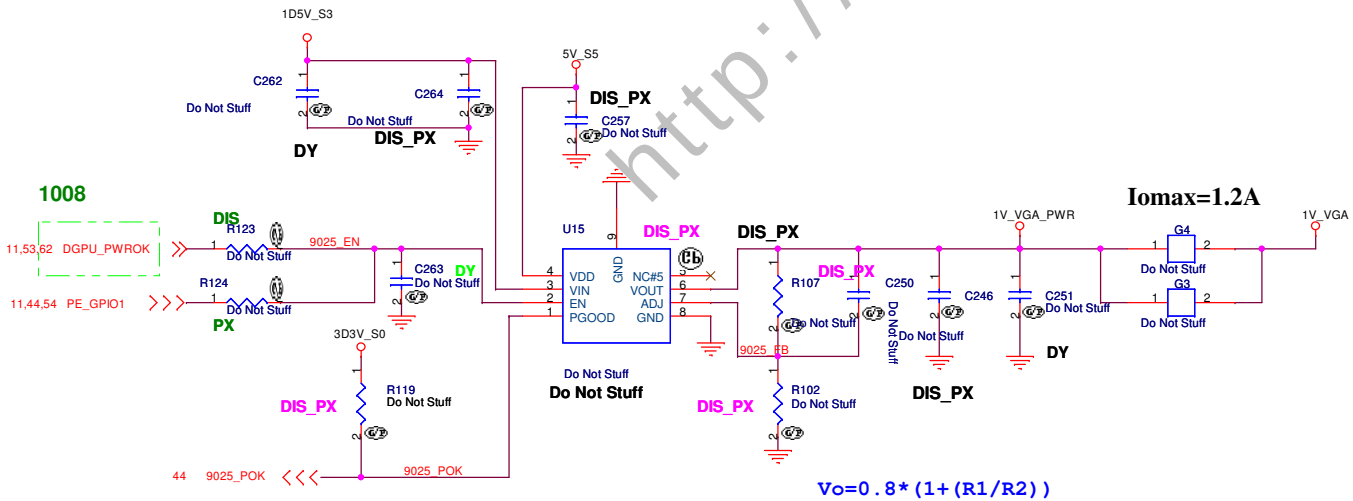
RT9025 for 1D05V_S0







UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **LDO 1D05V/2D5V/1V**

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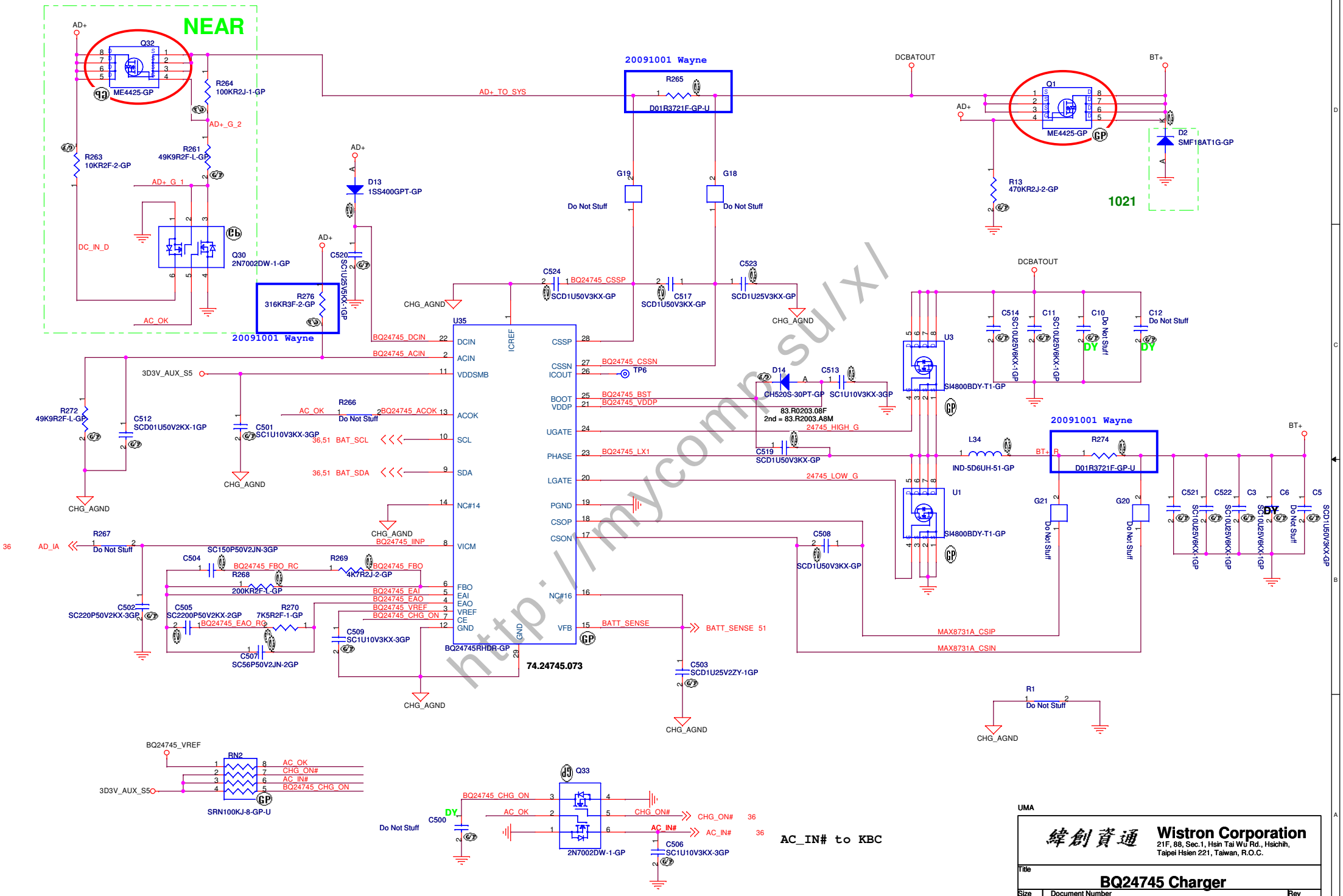

UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: BQ24745 Charger		
Size: A3	Document Number: JV42-DN	Rev: SA
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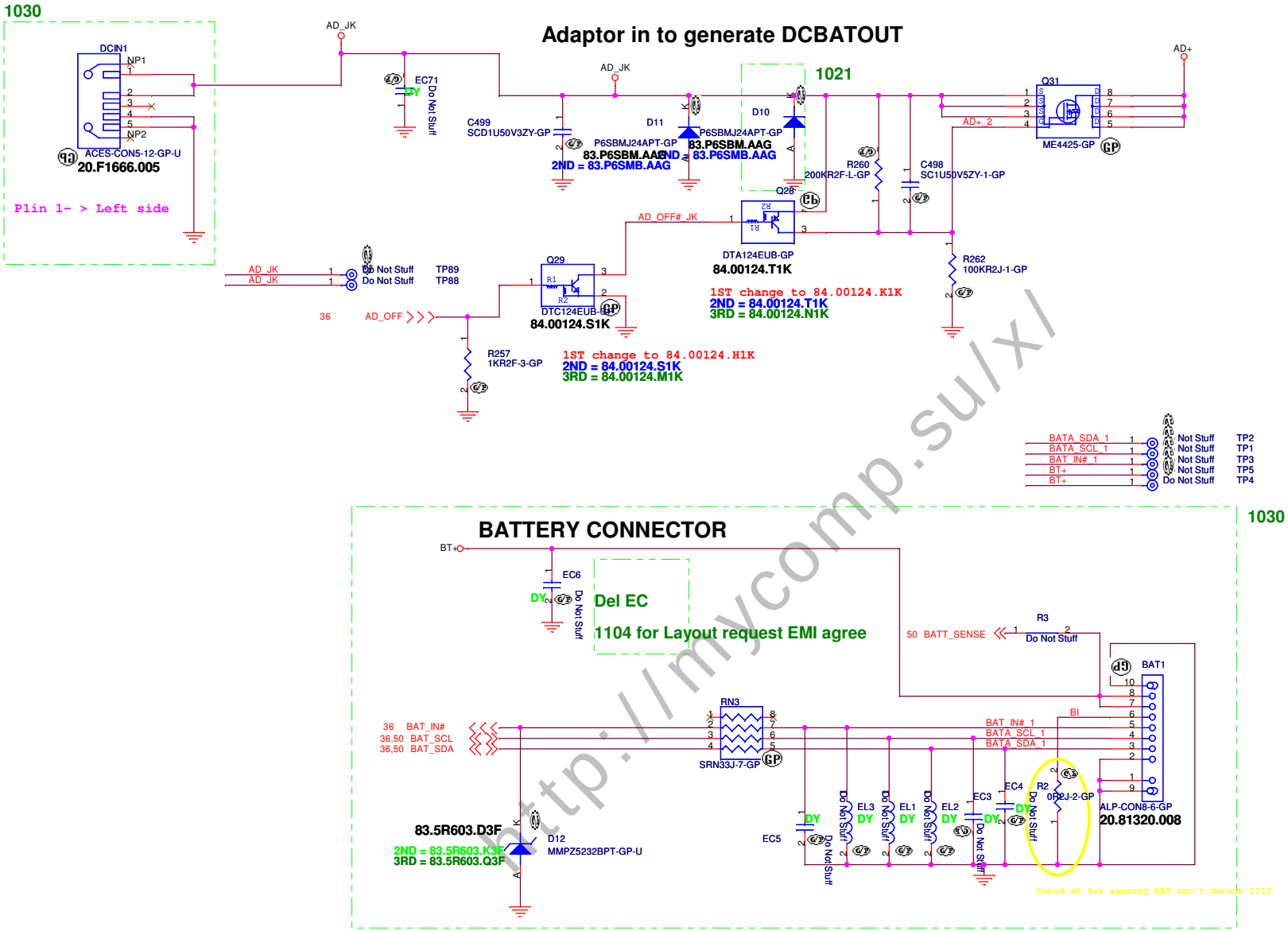

UMA

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Title: AD/BATT CONN

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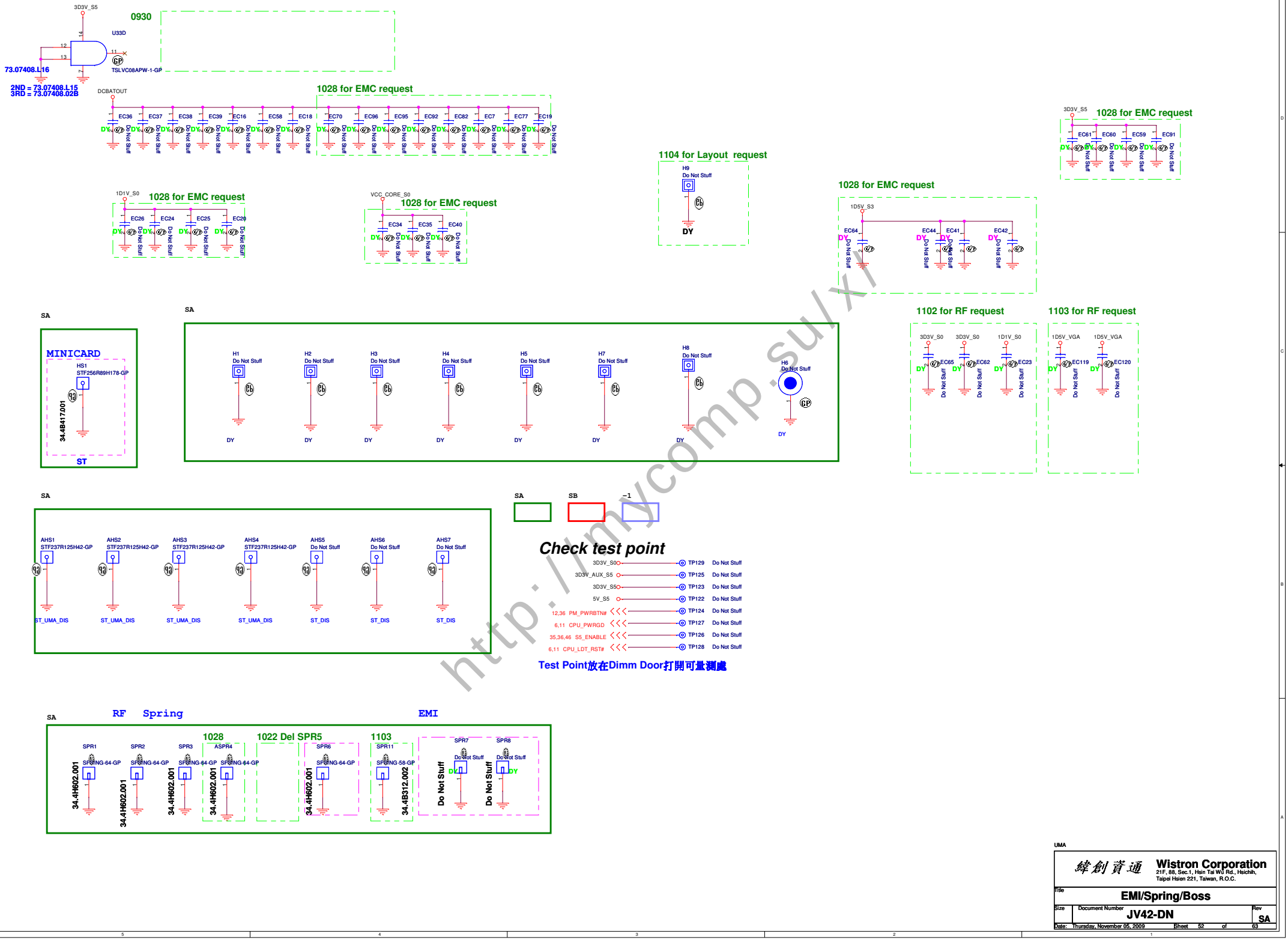

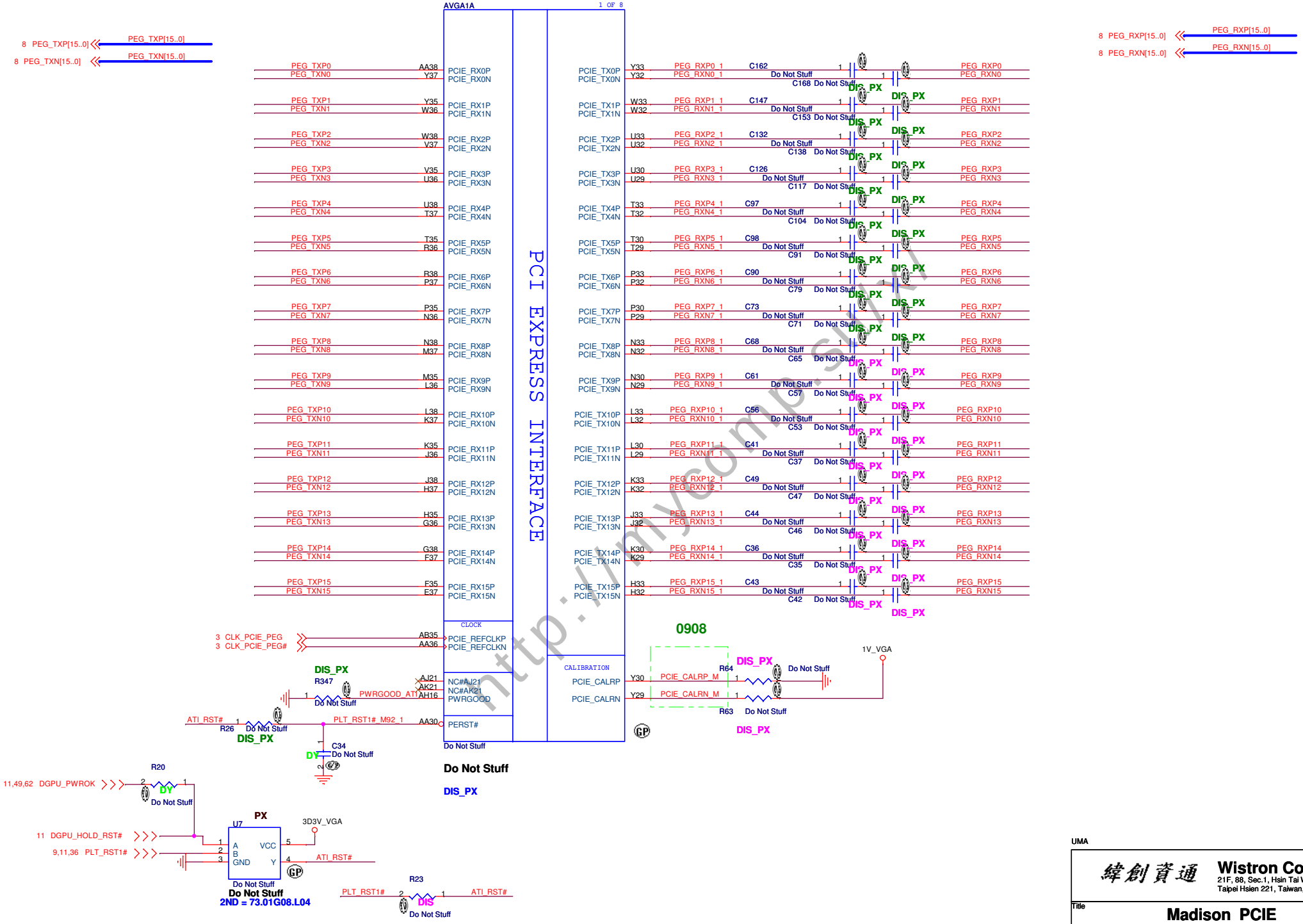

UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Madison PCIE		
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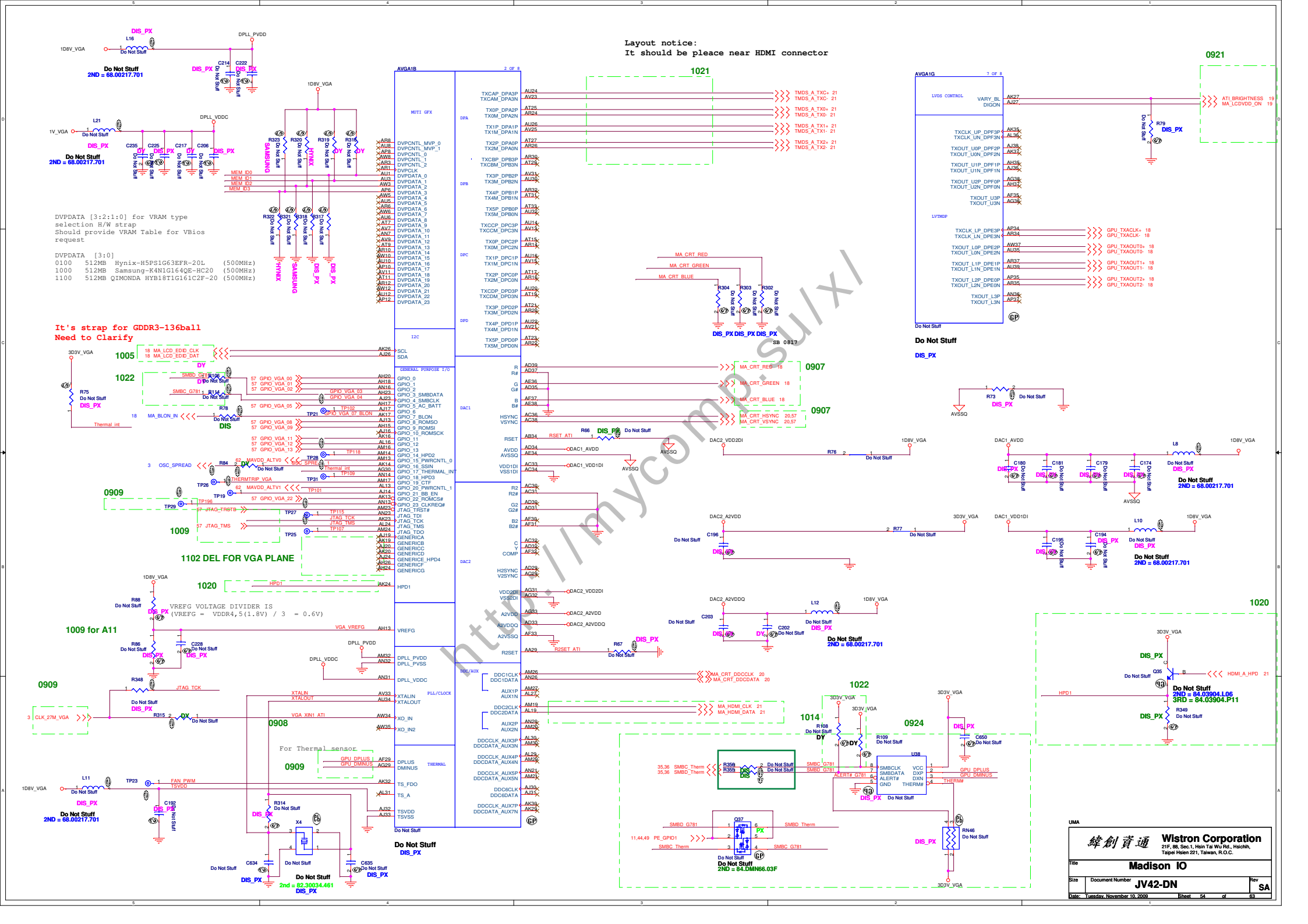
Layout notice:
It should be pleace near HDMI connector
DVPDATA [3:2:1:0] for VRAM type selection H/W strap
Should provide VRAM Table for VBios request
DVPDATA [3:0]
0100 512MB Hynix-H5PS1G63EFR-20L (500MHz)
1000 512MB Samsung-K4N1G164QE-HC20 (500MHz)
1100 512MB QIMONDA HYB18T1G161C2F-20 (500MHz)
It's strap for GDDR3-136ball
Need to Clarify
1102 DEL FOR VGA PLANE
VREFG VOLTAGE DIVIDER IS (VREFG = VDDR4,5(1.8V) / 3 = 0.6V)
For Thermal_sensor
Do Not Stuff
DIS_PX
2ND = 68.00217.701
2ND = 84.03904.L06
3RD = 84.03904.P11
2ND = 84.DMN66.03F
2nd = 82.30034.461
SB 0817
UMA
緯創資通
Wistron Corporation
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Title
Madison IO
Size
Document Number
JV42-DN
Rev
SA
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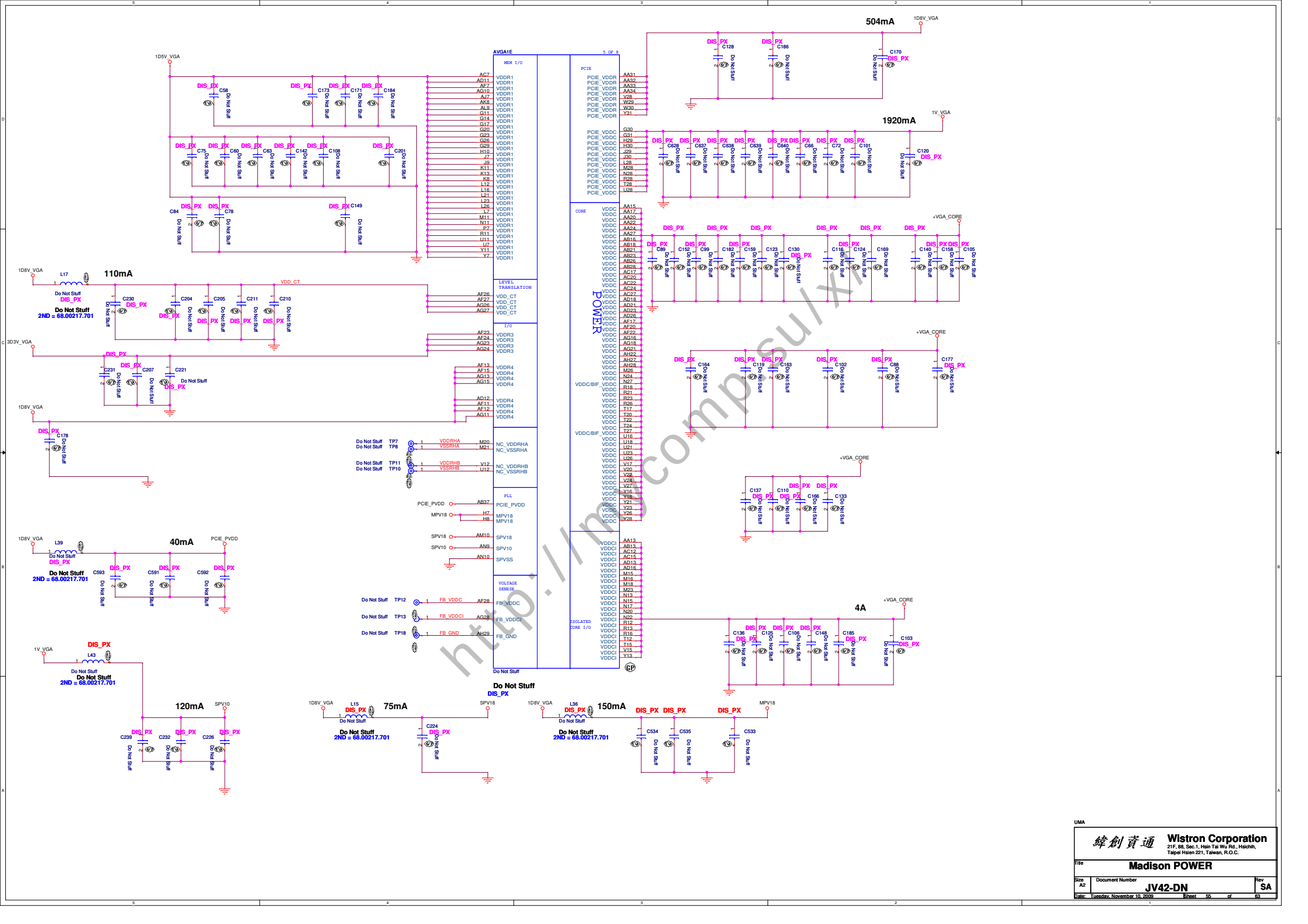
504mA
1D8V_VGA
1V_VGA
1920mA
+VGA_CORE
1D5V_VGA
3D3V_VGA
AVGA1E
MEM I/O
PCIE
CORE
POWER
LEVEL TRANSLATION
I/O
PLL
VOLTAGE SENSE
ISOLATED CORE I/O
110mA
VDD_CT
40mA
PCIE_PVDD
4A
120mA
SPV10
75mA
SPV18
150mA
MPV18
Do Not Stuff
DIS_PX
2ND = 68.00217.701
UMA
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
Madison POWER
JV42-DN
SA
Tuesday, November 10, 2009
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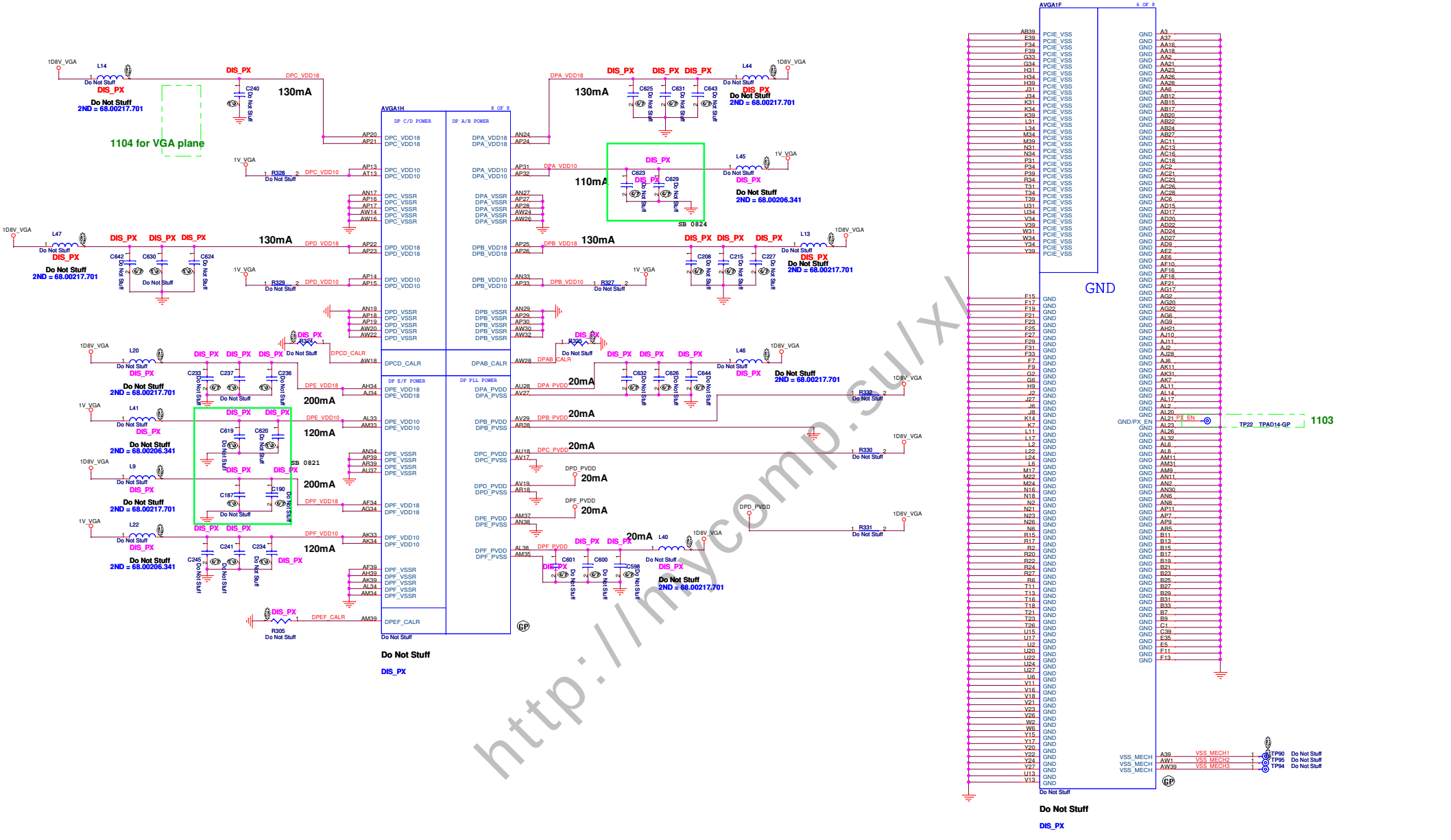

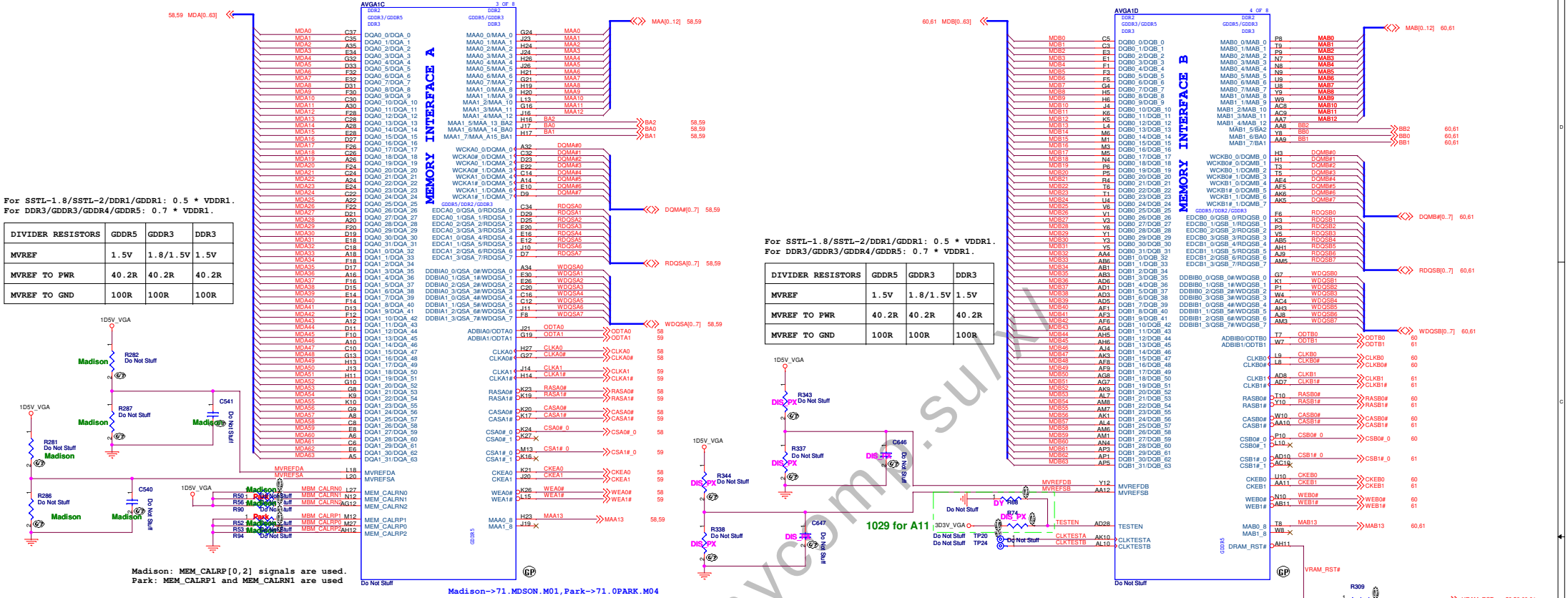

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIE FULL TX OUTPUT SWING Tansmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	X
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	X
RESERVED	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RESERVED	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
VIP_DEVICE_STRAP_ENA (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size	X X X
RSVD	V2SYNC		0
RSVD	H2SYNC		0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	X X

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC, GPIO2, GPIO21

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
128MB	x000	ST Microelectronics	M25P05A	0100
256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			

V

Designator	For M97-M2	For Mannhatton
R_MEM_1	10K	10K
R_MEM_2	40R/Short	680R
R_MEM_3	DY	DY
C_MEM	2.2nF	68pF

UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Madison Memory / Straps

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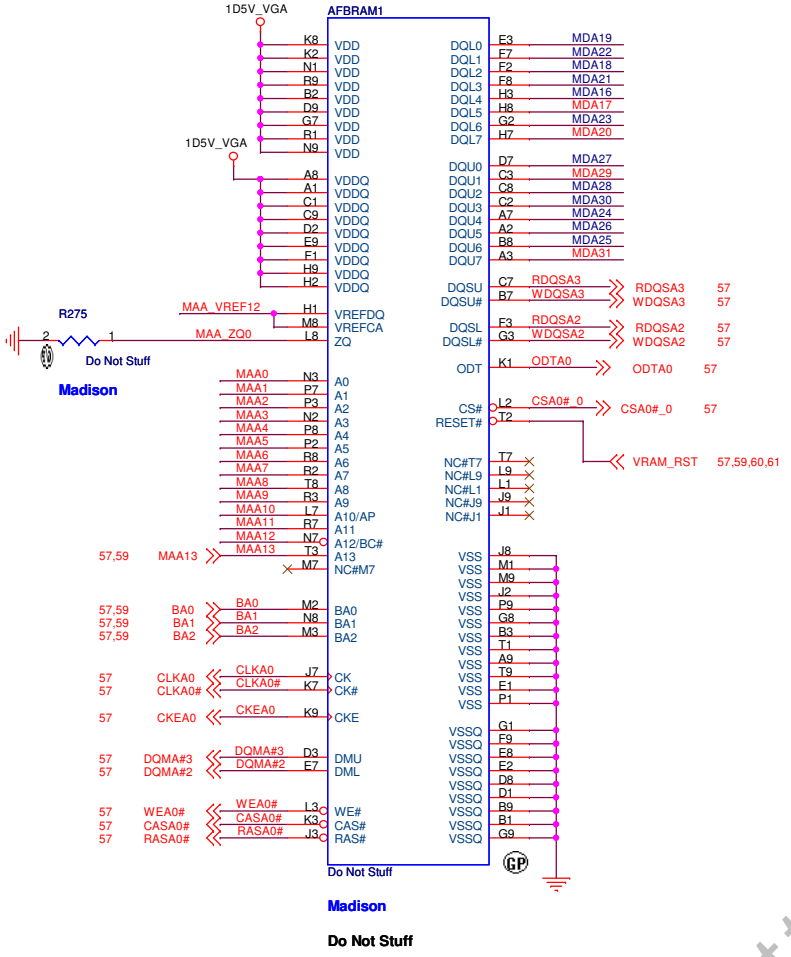
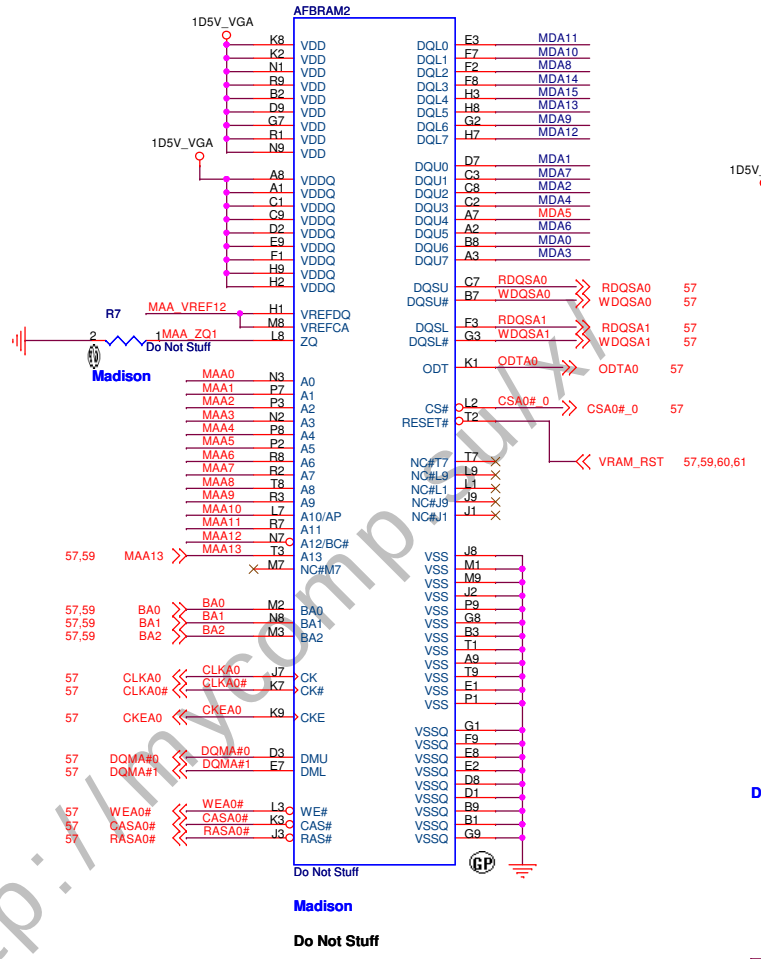
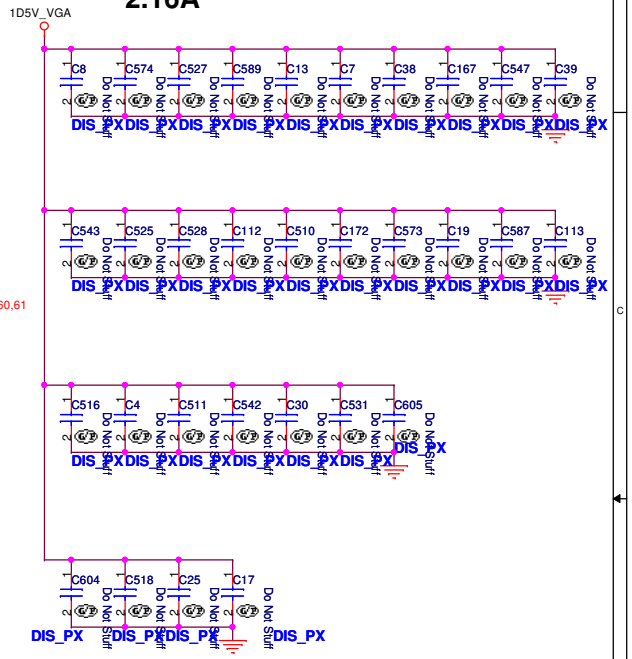
DDR3

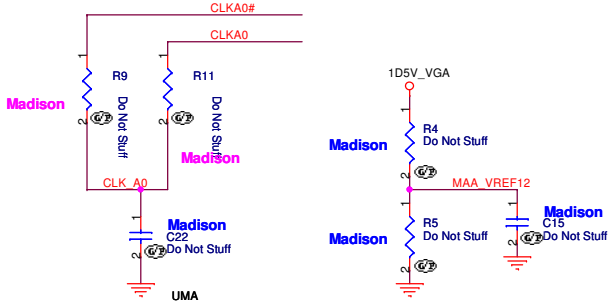






SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U

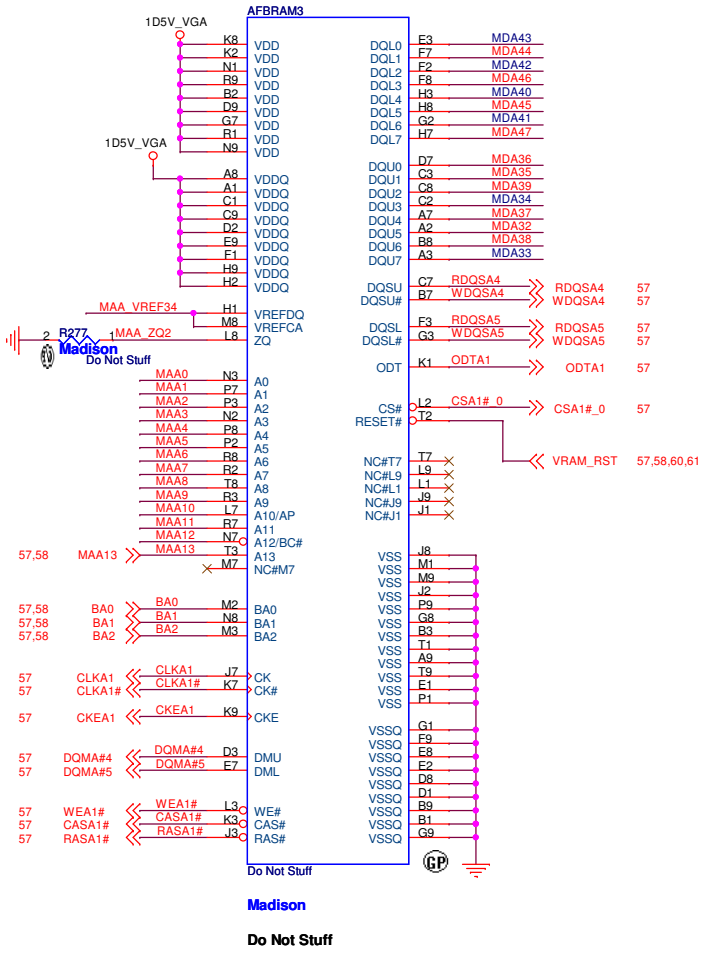
57,59 DQMA#[0..7]
57,59 RDQSA[0..7]
57,59 WDQSA[0..7]
57,59 MAA[0..12] MAA[0..12]
57,59 MDA[0..63] MDA[0..63]

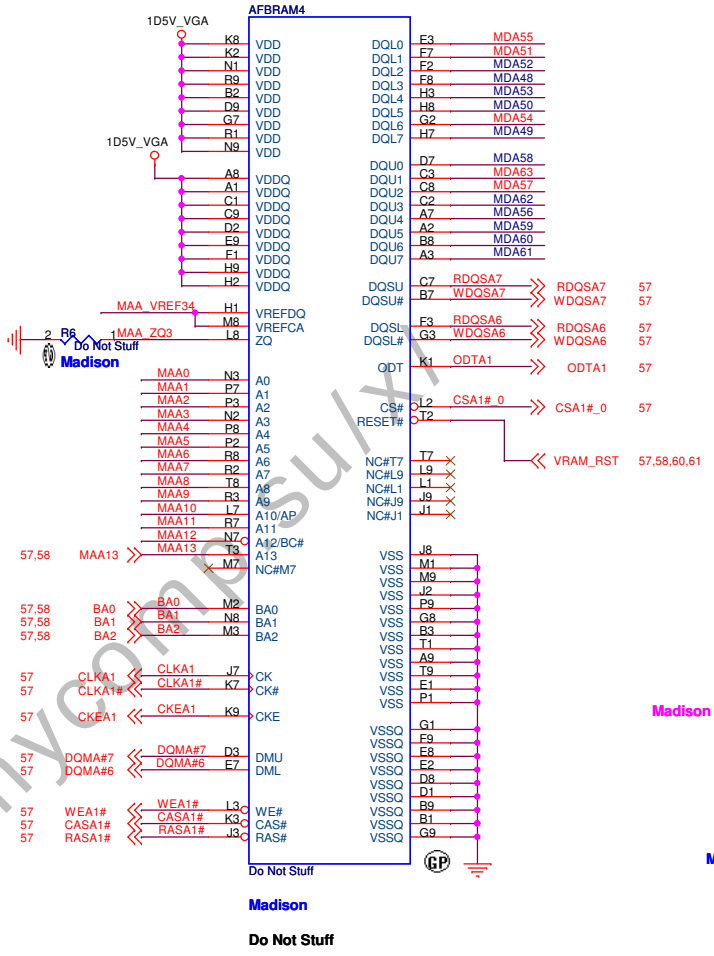


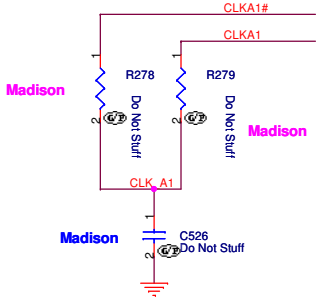
UMA

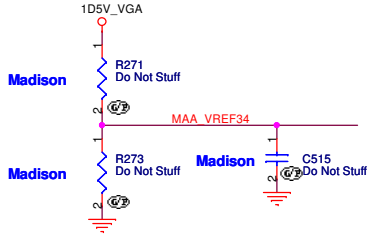
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: VRAM(1/4)		
Size: A3	Document Number: JV42-DN	Rev: SA
Date: Thursday, November 05, 2009	Sheet 58 of 63	

DDR3









SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U

57,58 DQMA#[0..7]
57,58 RDQSA[0..7]
57,58 WDQSA[0..7]
57,58 MAA[0..12] MAA[0..12]
57,58 MDA[0..63] MDA[0..63]

UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***VRAM(2/4)***

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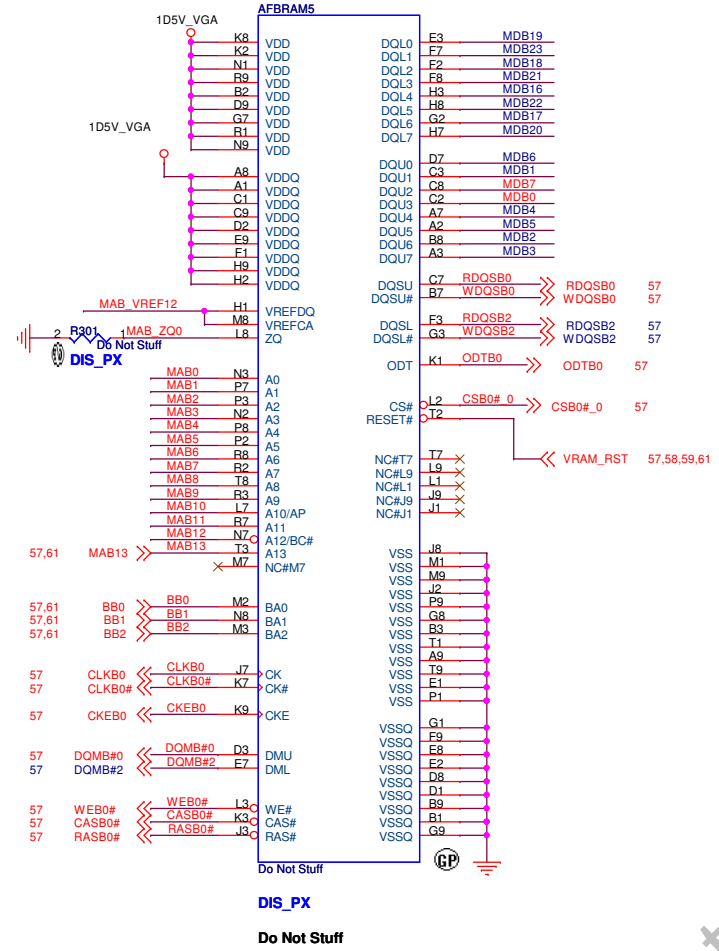
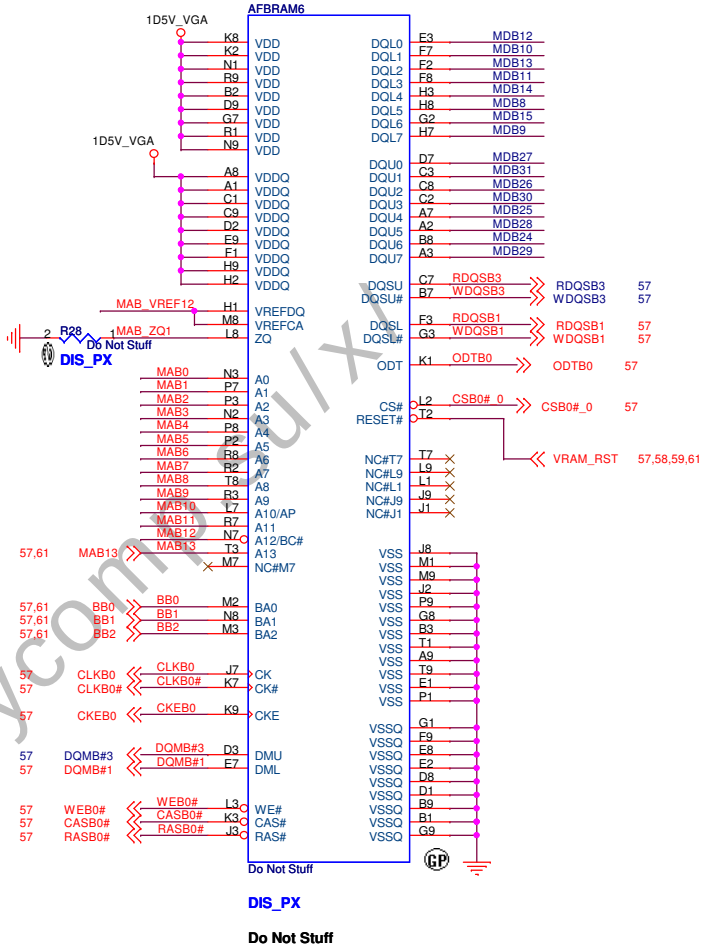
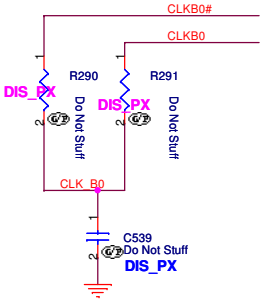
DDR3







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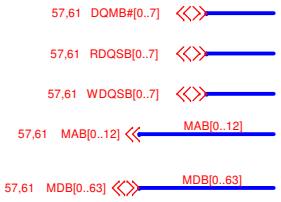

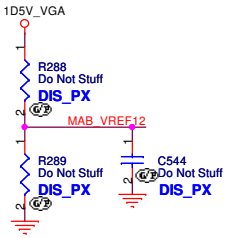

UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *VRAM(3/4)*		
Size: A3	Document Number: JV42-DN	Rev: SA
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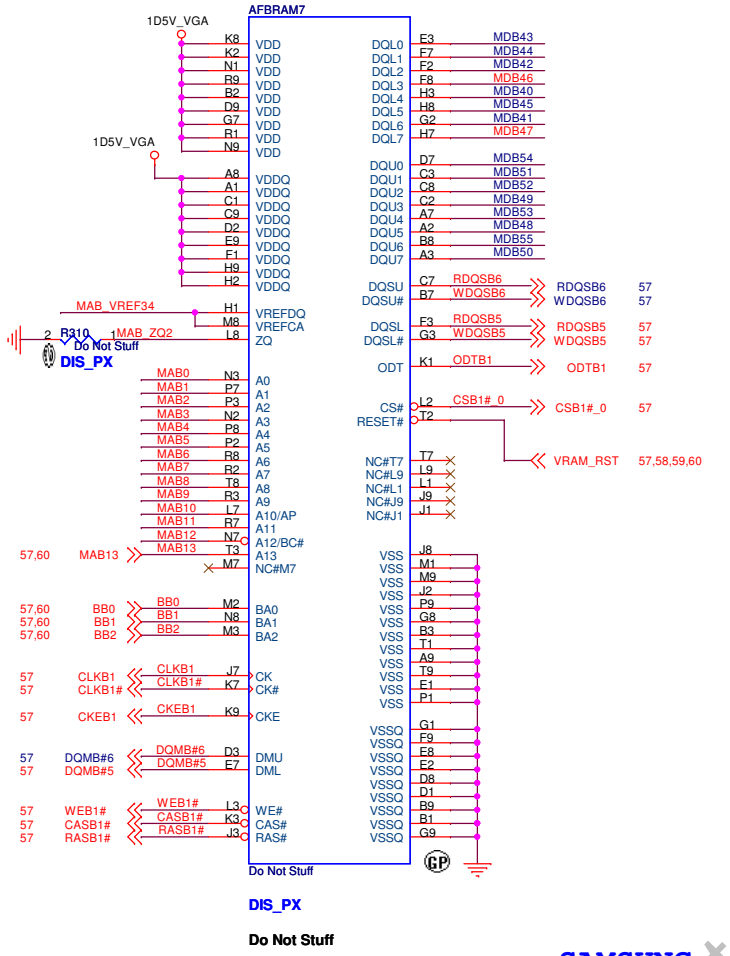
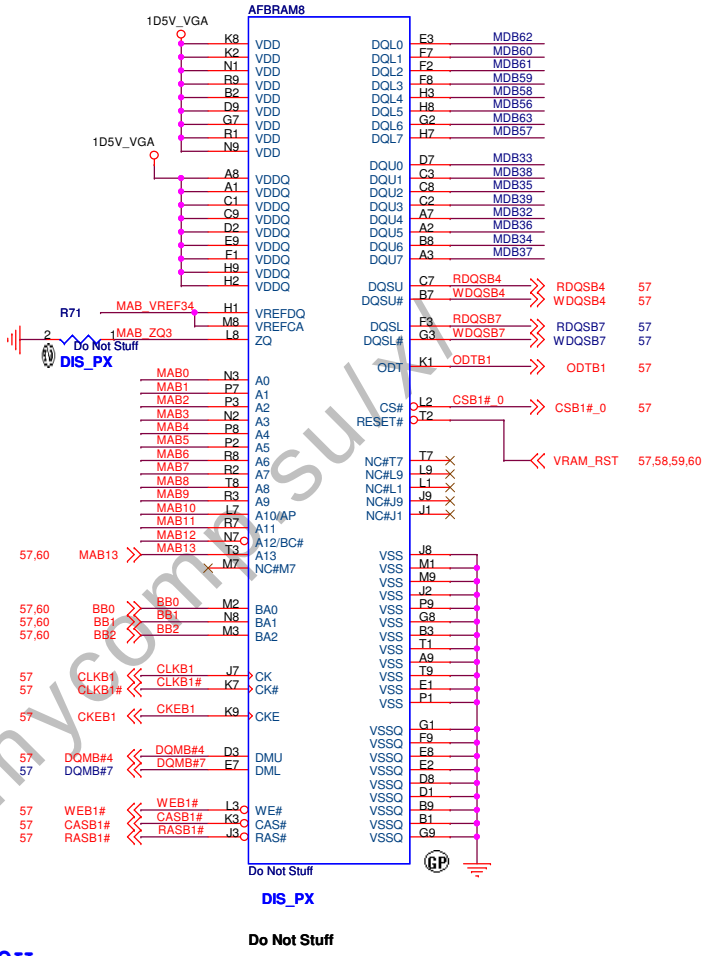
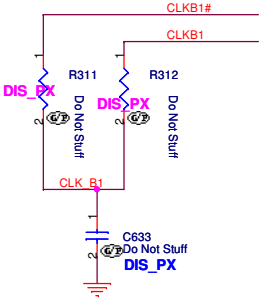
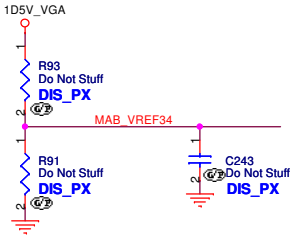
DDR3









SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U

57,60 DQMB#[0..7]
57,60 RDQSB[0..7]
57,60 WDQSB[0..7]
57,60 MAB[0..12] — MAB[0..12]
57,60 MDB[0..63] — MDB[0..63]

UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***VRAM(4/4)***	
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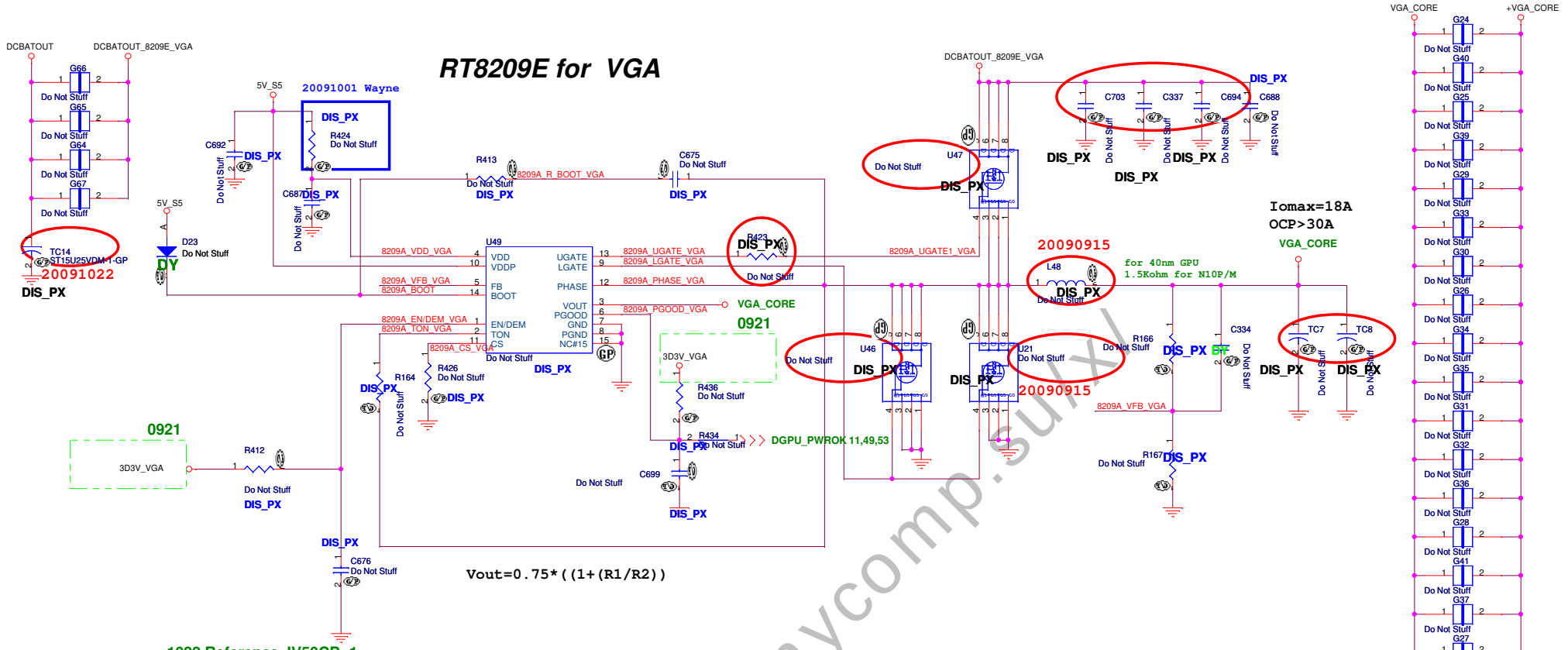
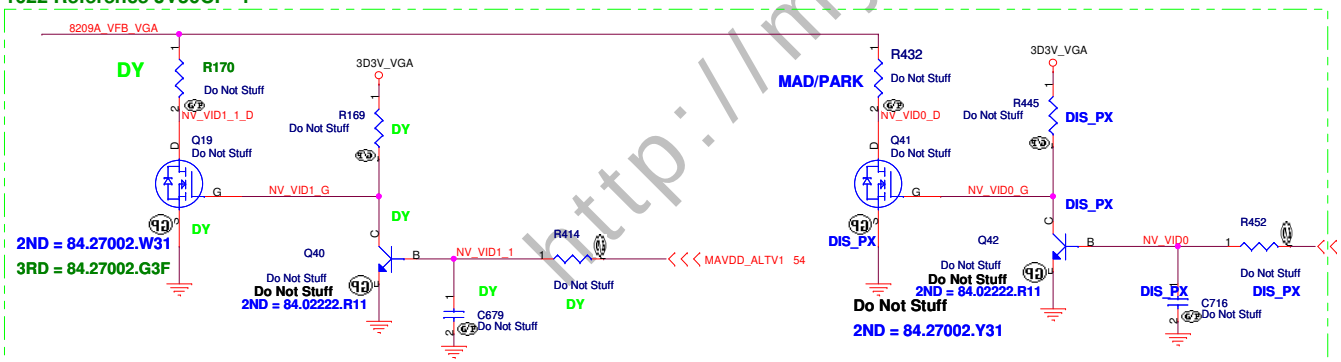
RT8209E for VGA



1022 Reference JV50CP -1



MADSION PRO

	I/O	Inter Pull Low	GPIO TABLE
NVVDD_ALTV0	O	YES	GPU VOLTAGE L: 1.00V GPU VOLTAGE H: 0.90V

PARK XT

	I/O	Inter Pull Low	GPIO TABLE
NVVDD_ALTV0	O	YES	GPU VOLTAGE L: 1.12V GPU VOLTAGE H: 0.90V

	R432
MADSION PRO	15KR2F 64.15025.6DL
PARK XT	6R81K 64.68115.6DL

UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8209E_VGA_CORE

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NB

RS780-->RS880M

71.RS780.M02-->71.RS880.M02

SB

SB820M-1-GP

71.SB820.00U-->71.SB820.M03

SATA_CALRP

A11: 80歐姆 1% resistor to GND

A12: TBD歐姆 1% resistor to GND

SATA_CALRN

A11:A11: 931歐姆1% resistor to VDDAN_11_SATA

A12: TBD歐姆 1% resistor to VDDAN_11_SATA.

VGA

Madison--> PN:71.MDSON.M01

Park--> PN:71.0PARK.M04

VRAM

Samsung-->VRAM FBRAM1~8 PN:VR.1GB0B.006

Hynix--> VRAM FBRAM1~8 PN:VR.1GB0G.004

CRT

UMA-->L1-->2R 0603

C62-->47U/6.3V

DIS-->L1-->Bead(L1 68.00217.711 L1608-UH38 SBK160808T-221Y-N-GP)

C62-->DY

HDMI

R497 : DIS-->0R

UMA & PX-->5.1K (R497 63.51234.1DL R402H16 5K1R2J-4-GP)

R496 : DIS-->100K

UMA & PX-->10K(R496 63.10334.1DL R402H16 10KR2J-3-GP)

R432(MAD/PARK)

Madison-->V15KR2F 64.15025.6DL

Park-->R432 64.68115.6DL

BOM

1st -> Diserete Madison Hynix(S02G)

2nd -> UMA (S01G)

1st +3rd -> Diserete Park Hynix(S03G)

1st +3rd -> Diserete Park Samsung(S04G)

1st -> Diserete Madison Samsung (S05G)

PX=PARK+Hynix(1st +3rd)

UMA

緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NOTE

Size: A3 | Document Number: JV42-DN | Rev: SA

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