

Yukon Block Diagram

Project code: 91.4BC01.001
 PCB P/N : 48.4BC01.001
 REVISION : 08226- -1

PCB Layer Stackup

L1: Signal 1
 L2: VCC
 L3: Inner Signal 2
 L4: Inner Signal 3
 L5: GND
 L6: Signal 4

CPU V_CORE

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	ID2V_S0 ID8V_S3

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO

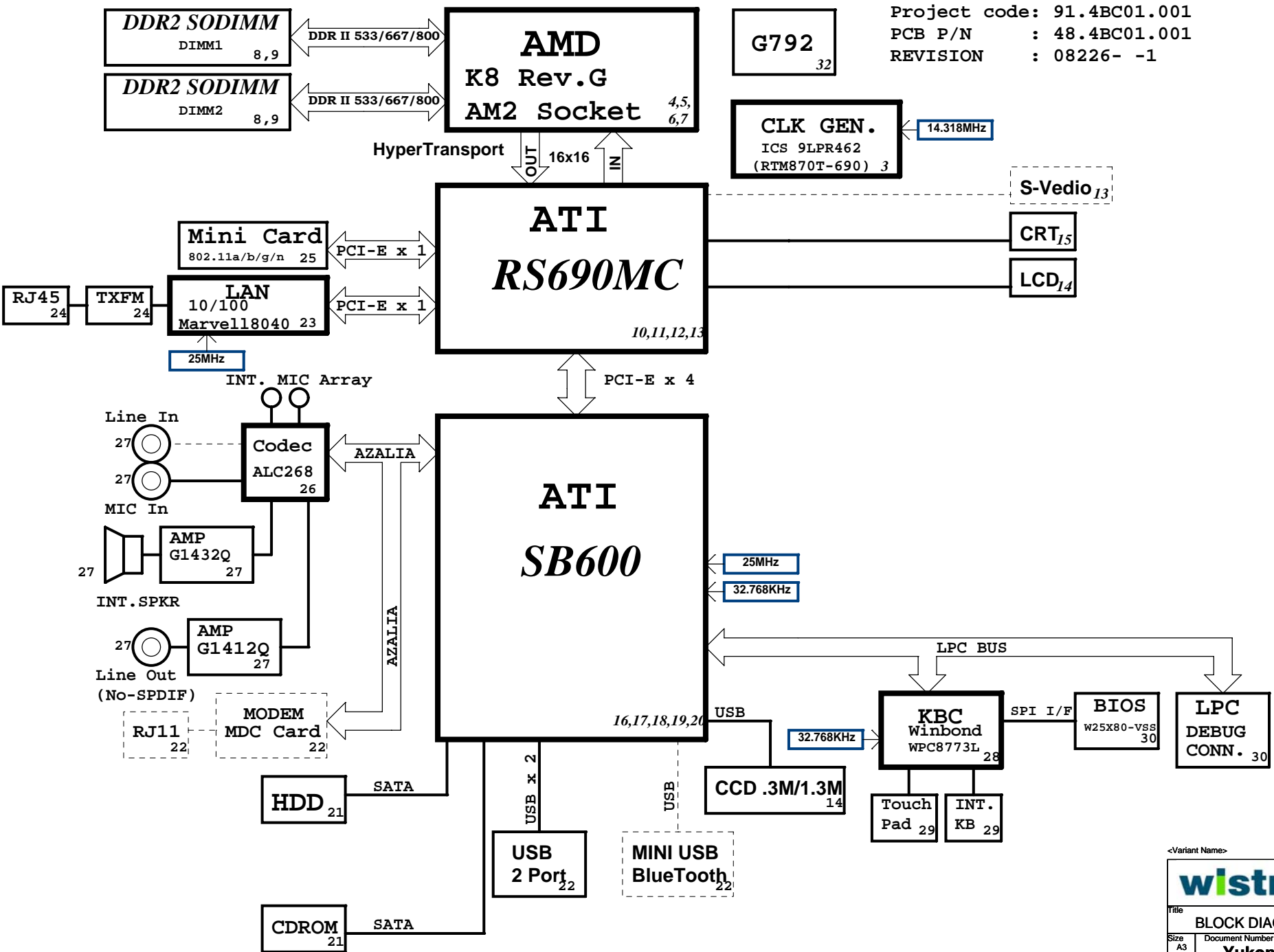
INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

SYSTEM LDO

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT



<Variant Name>

wistron Wistron Incorporated
 21F, 88, Hsin Tai Wu Rd
 Hsichih, Taipei

Title: **BLOCK DIAGRAM**

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5

4

3

2

1

D

D

C

C

B

B

A

A

<Core Design>

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Title **CHANGE HISTORY**

Size A3	Document Number Yukon	Rev 1
Date: Wednesday, August 06, 2008	Sheet 2 of	43

5

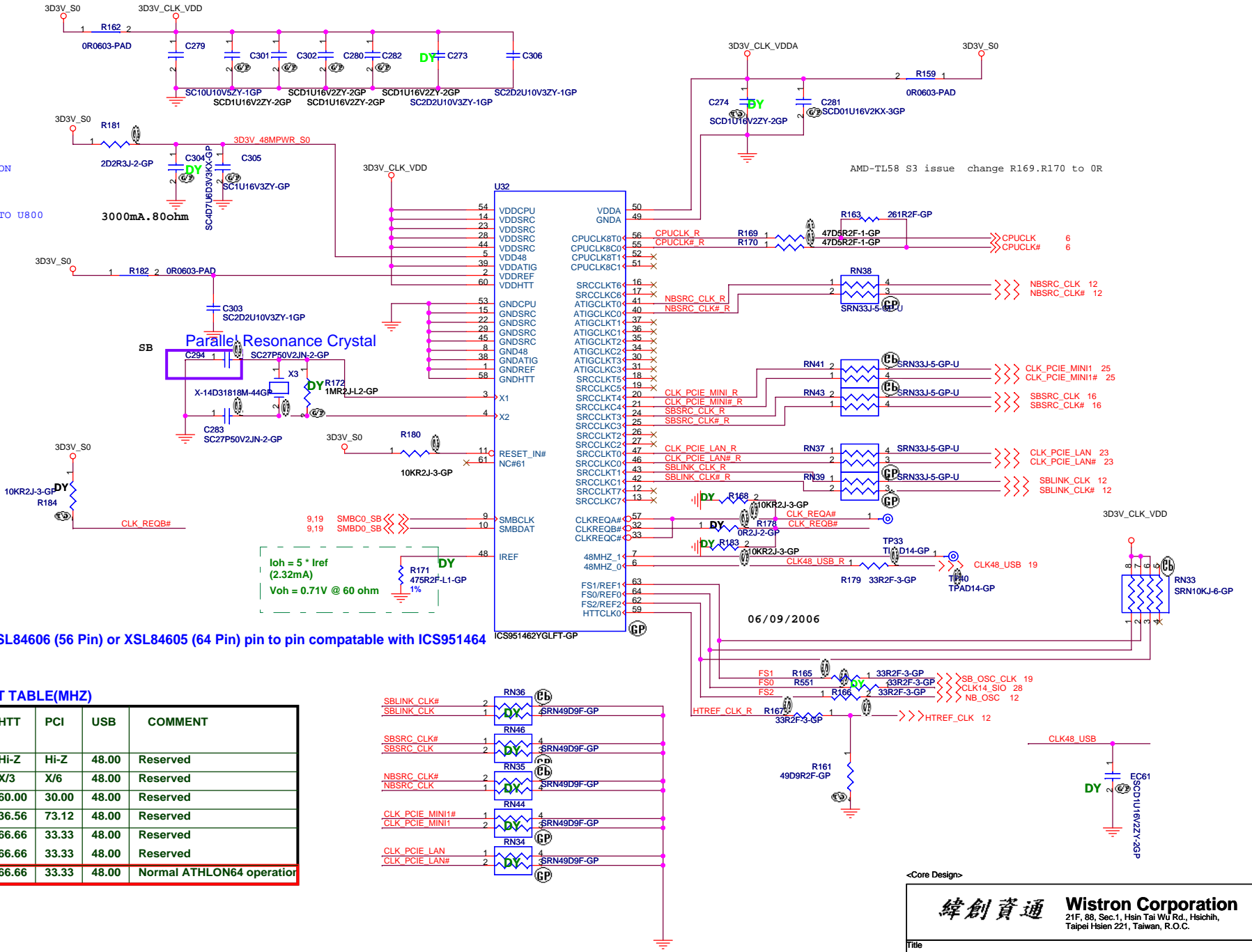
4

3

2

1

- 1- PLACE ALL SERIAL TERMINATION RESISTORS CLOSE TO U800
- 2- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN



Check SLGO EXT CLK XSL84606 (56 Pin) or XSL84605 (64 Pin) pin to pin compatible with ICS951464

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operator

$I_{oh} = 5 \cdot I_{ref}$
 $(2.32mA)$
 $V_{oh} = 0.71V @ 60 \text{ ohm}$

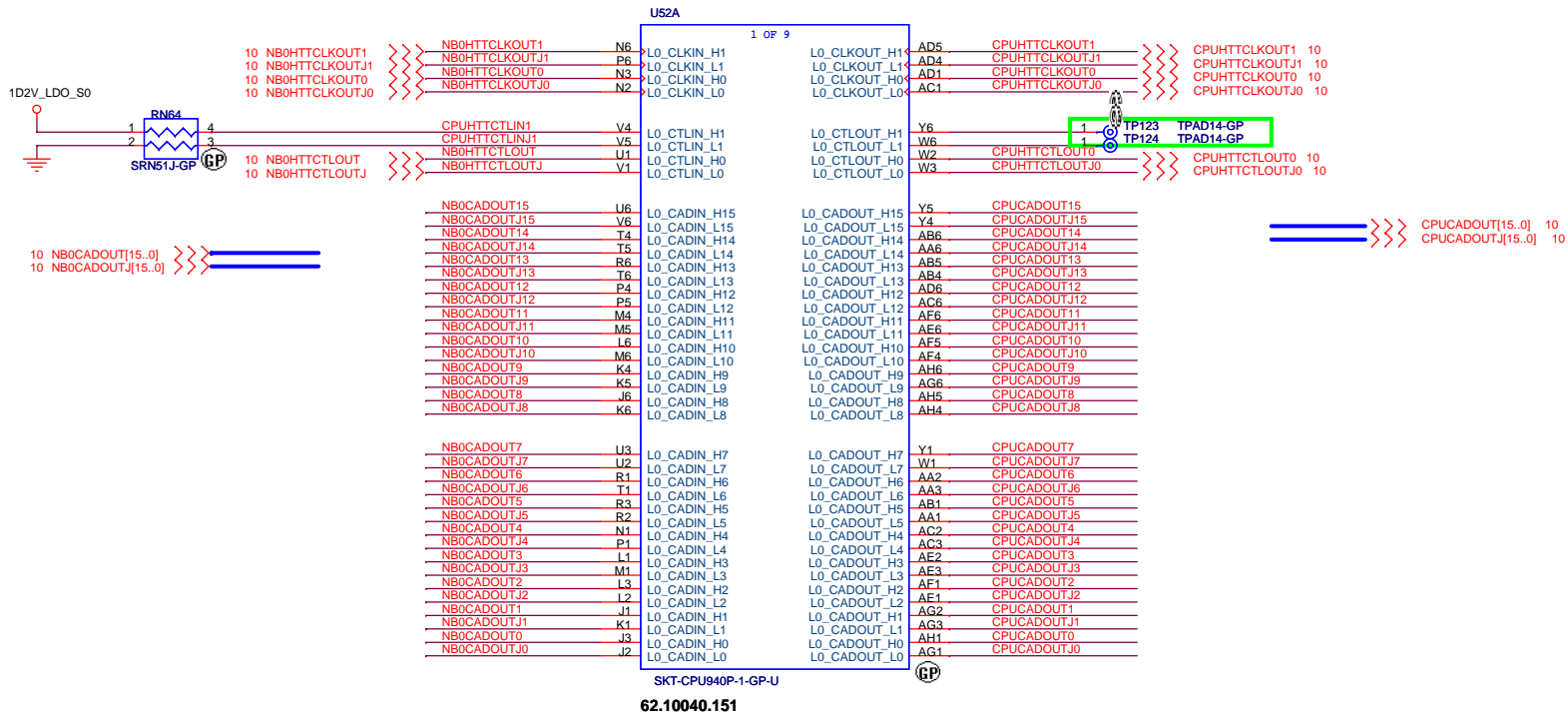
<Core Design>

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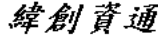
Title: **CLKGEN_ICS951412**

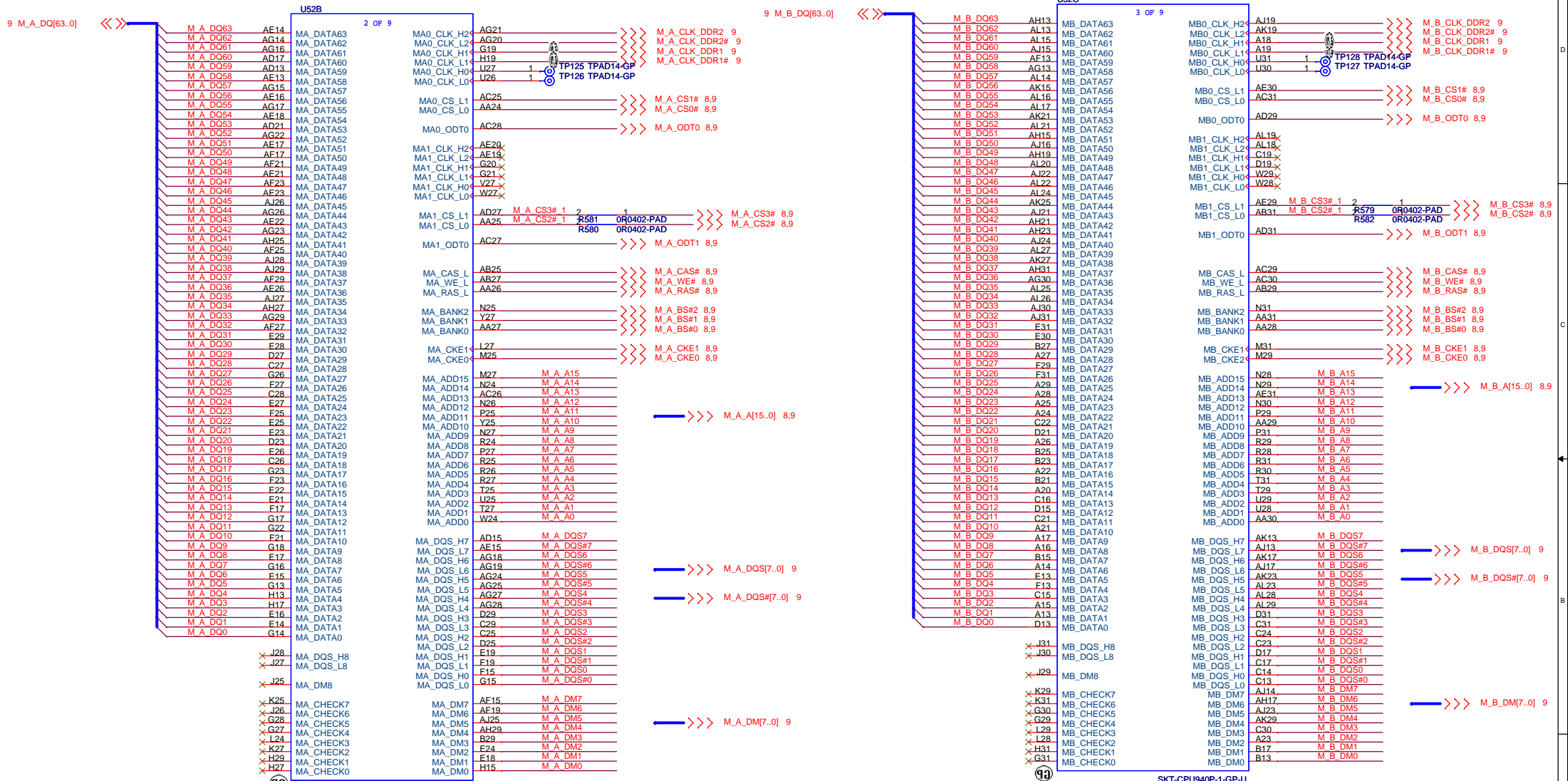
Size: A3 Document Number: **Yukon** Rev: -1

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CPU(1/4)_HyperTransport I/F	
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62.10040.151

62.10040.151

<Core Design>

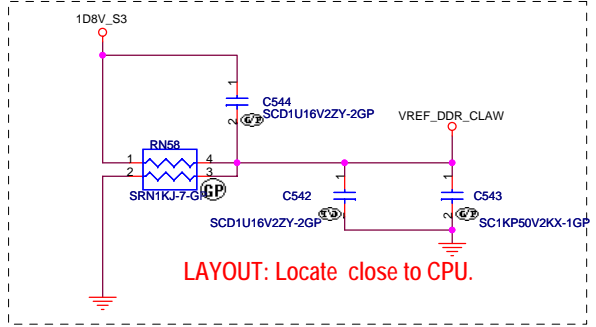
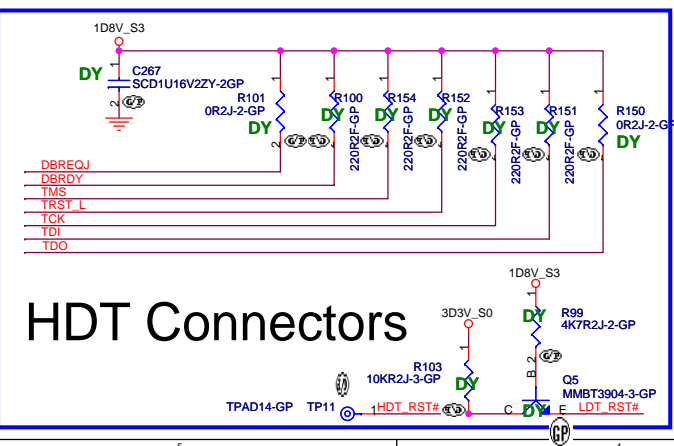
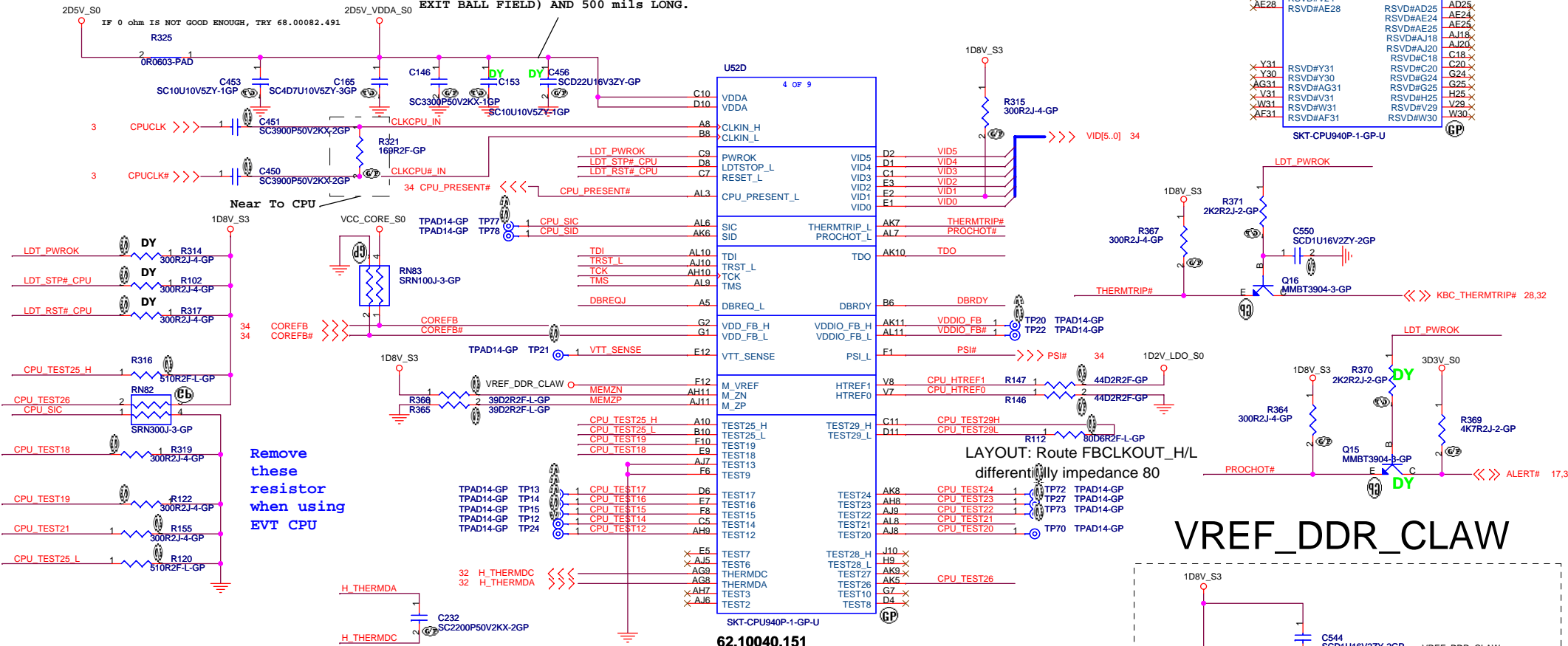
緯創資通 **Wistron Corporation**
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Title: **CPU(2/4) DDR**

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LYAOUT:ROUTE VDDA TRACE APPROX.
50mils WIDE(USE 2X25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.



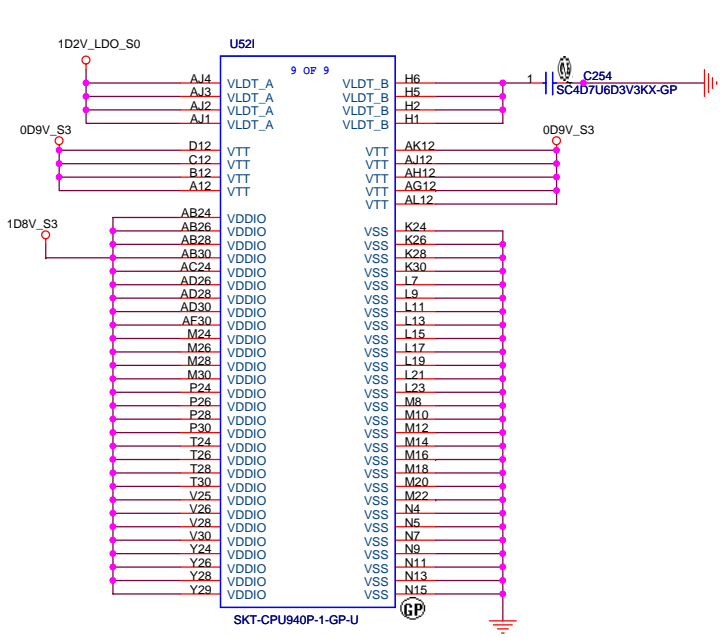
<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU(3/4)_Control & Debug**

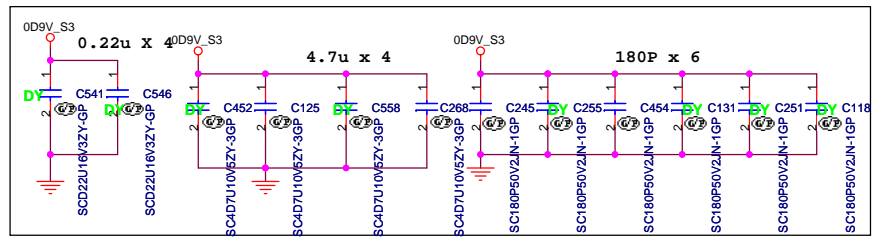
Size: A3 Document Number: **Yukon** Rev: -1

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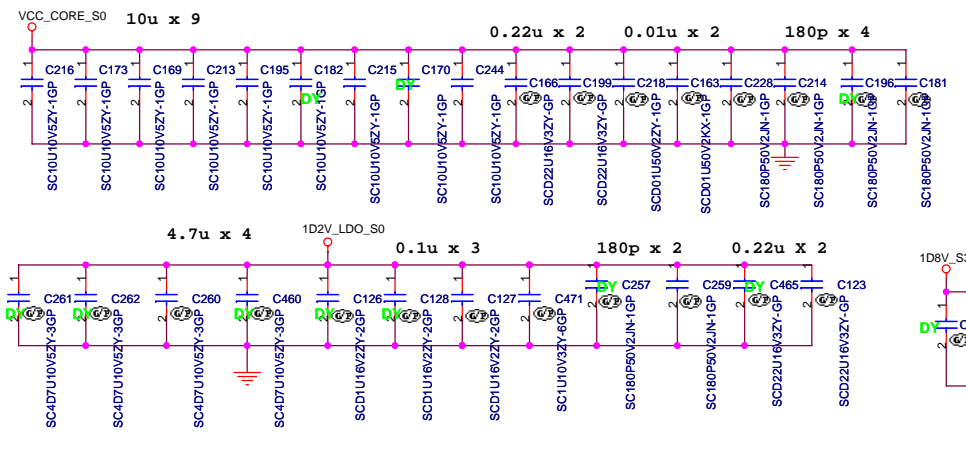


62.10040.151

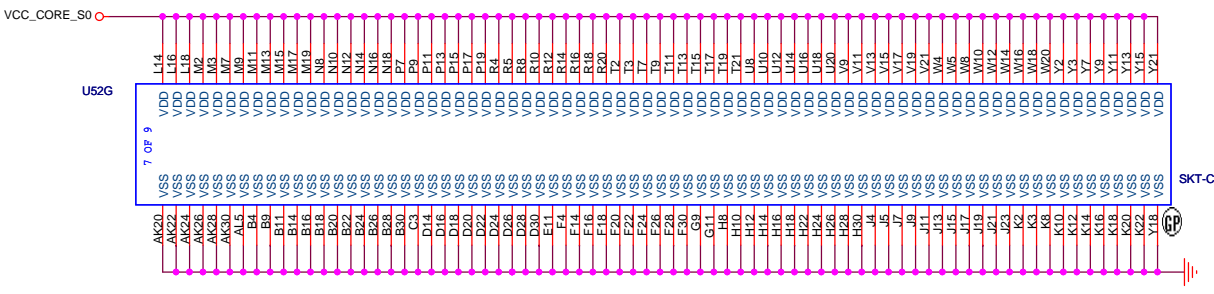
Place near to CPU



LAYOUT: Place on backside of processor.



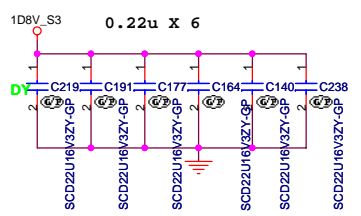
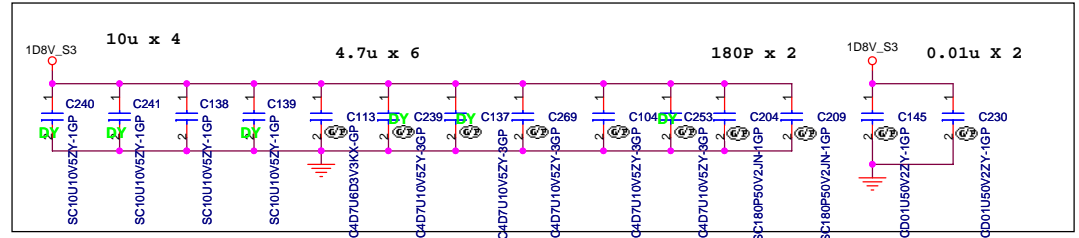
SKT-CPU940P-1-GP-U



SKT-CPU940P-1-GP-U



SKT-CPU940P-1-GP-U



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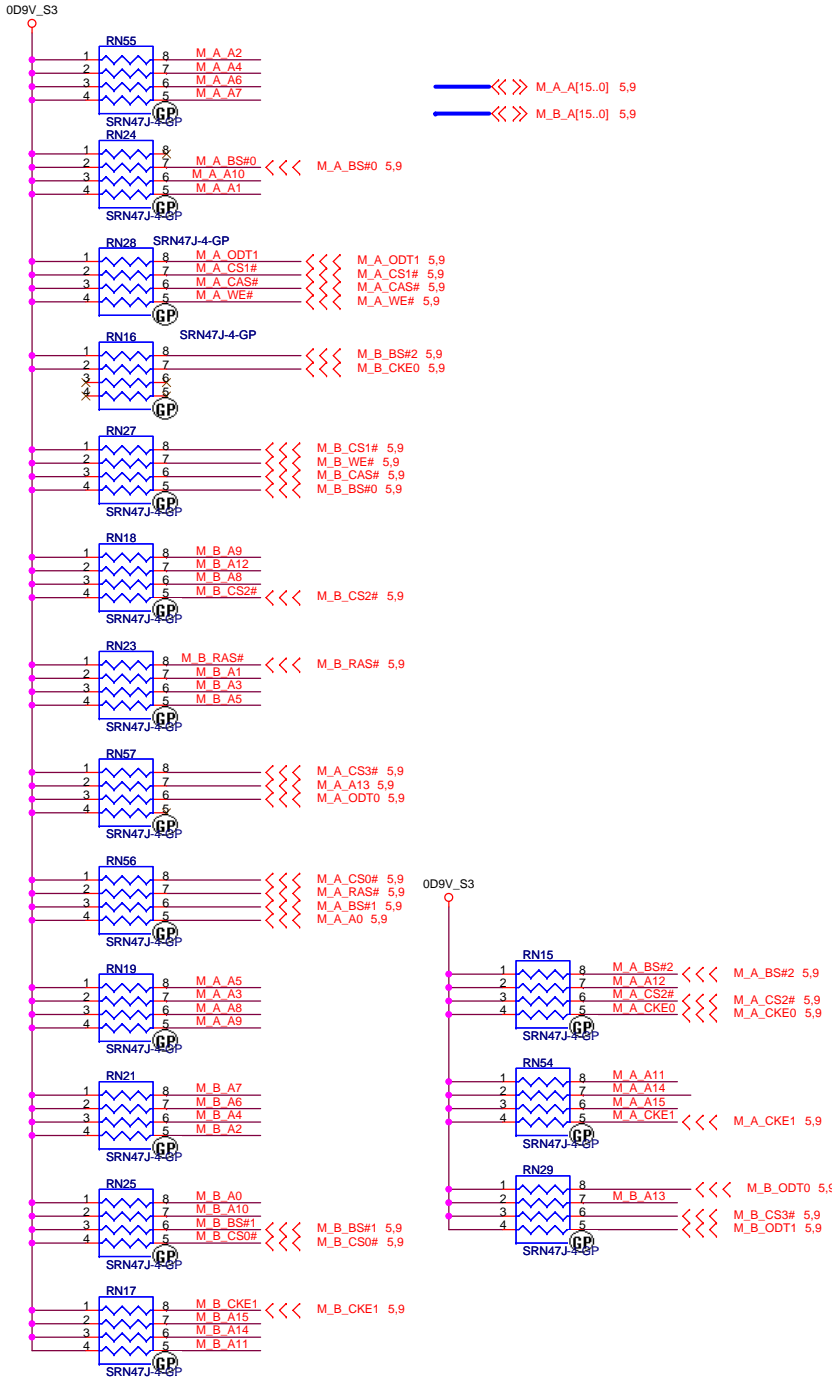
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Size: A3 Document Number: **Yukon** Rev: -1

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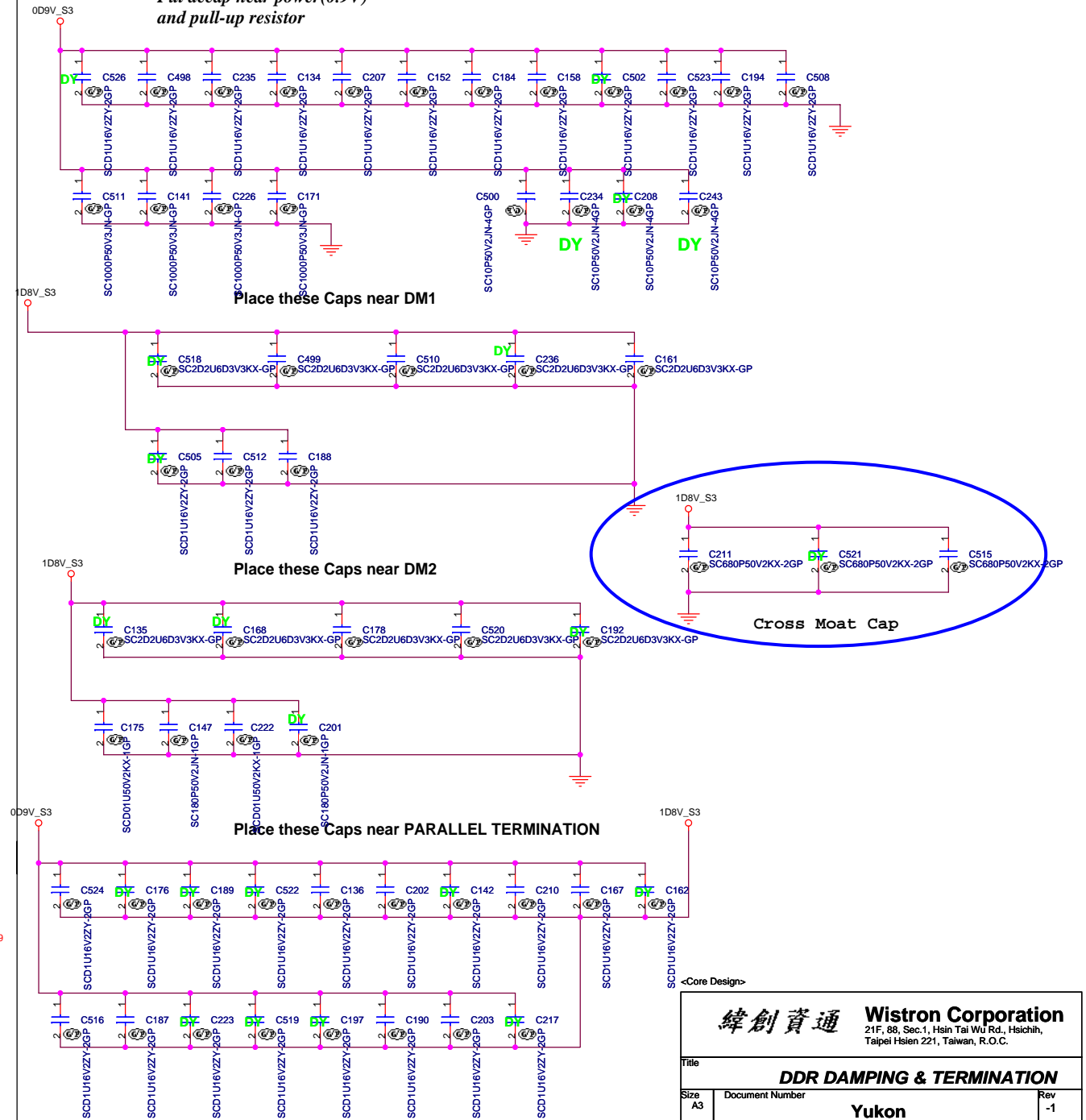
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

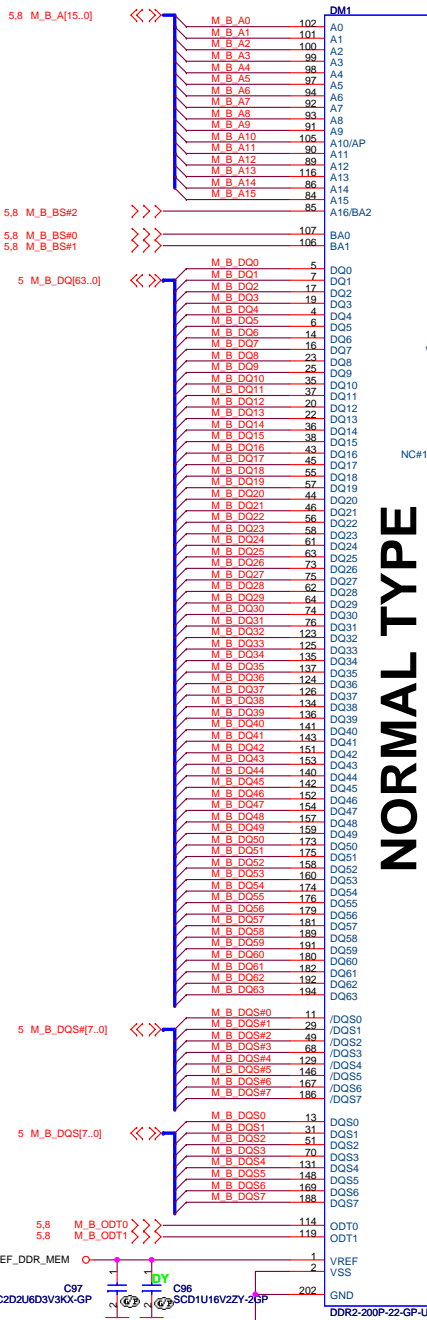


Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor



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DDR DAMPING & TERMINATION	
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NORMAL TYPE

High 9.2mm

2nd: 62.10017.A51

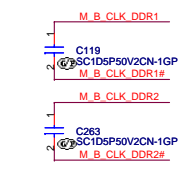


NORMAL TYPE

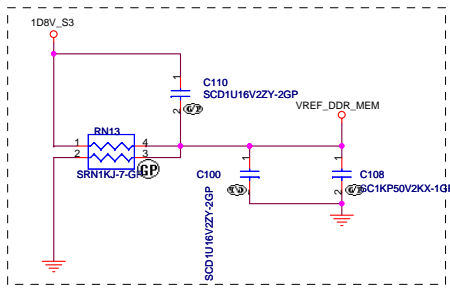
High 5.2mm

2nd: 62.10017.A41

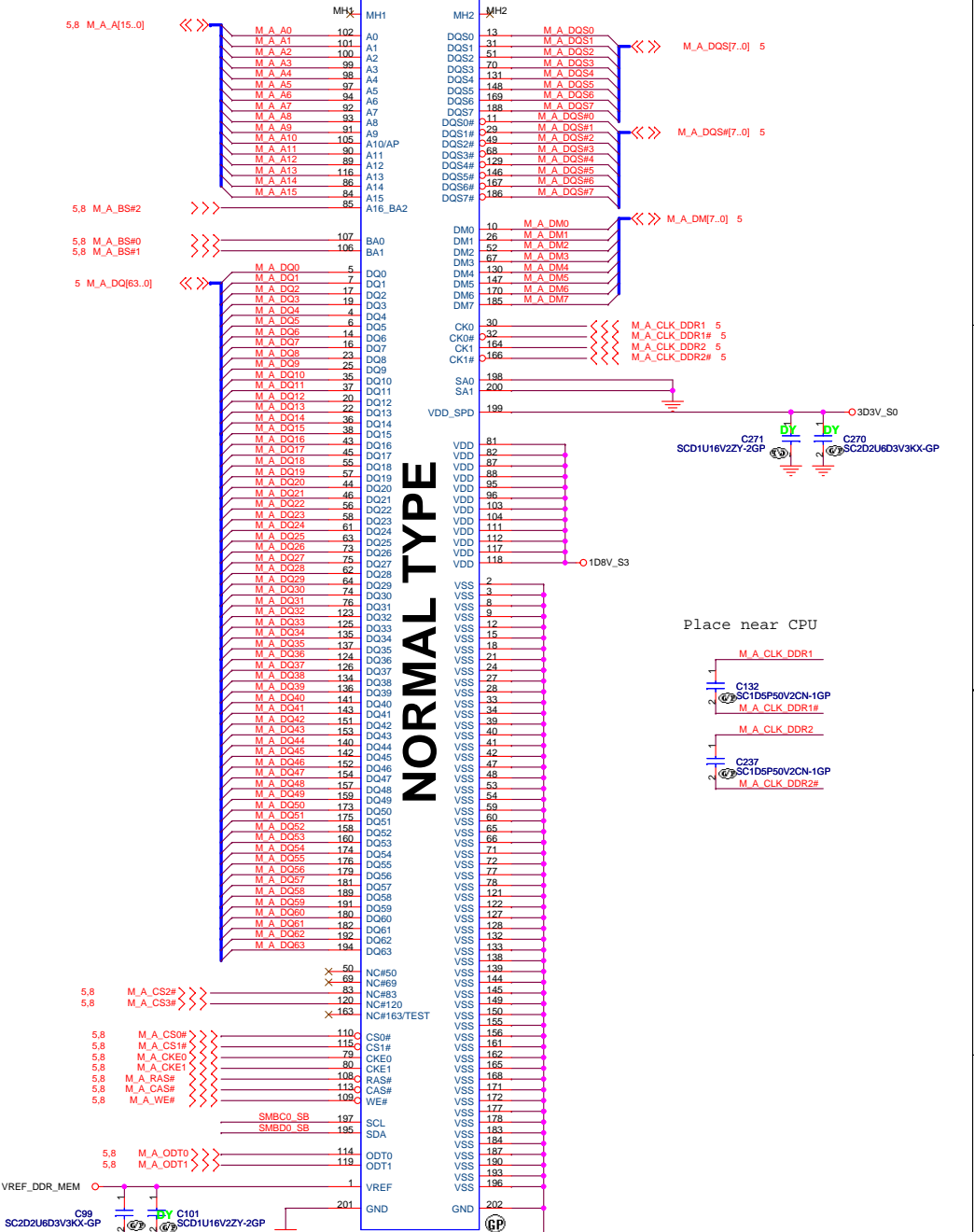
Place near CPU



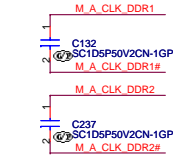
DDR_VREF



LAYOUT: Locate close to DIMM



Place near CPU



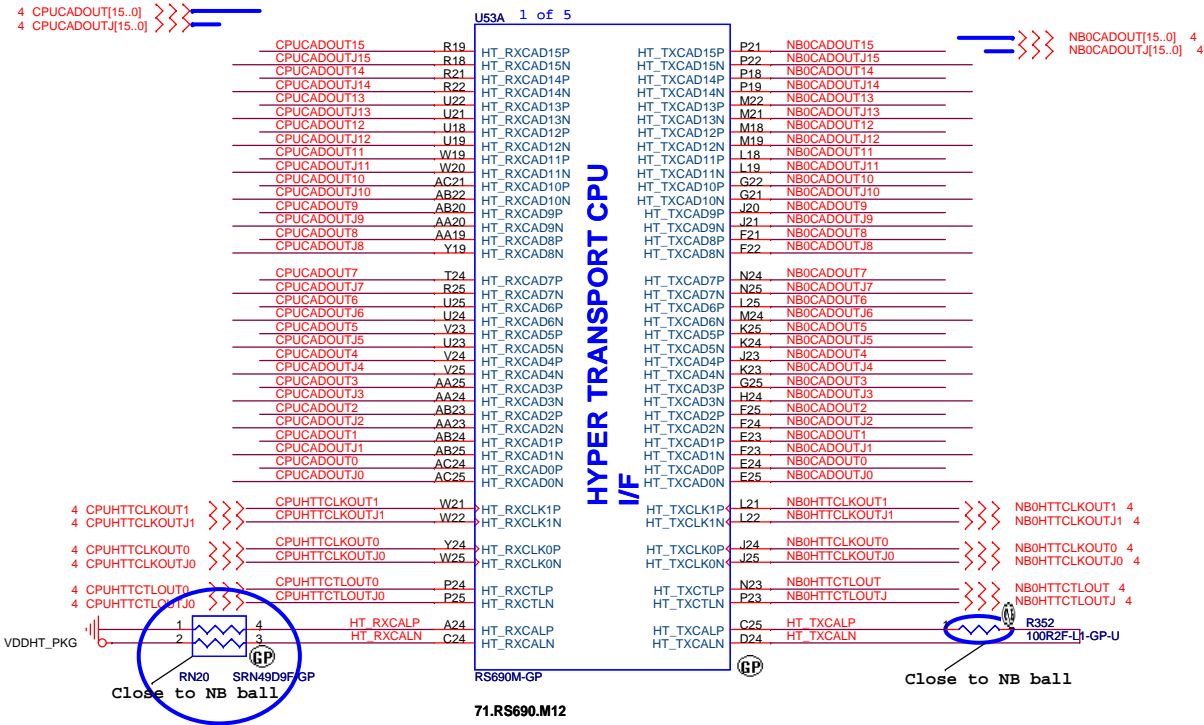
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Title			
DDR SO-DIMM SKT			
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CLAW HAMMER TO NB

NB TO CLAW HAMMER

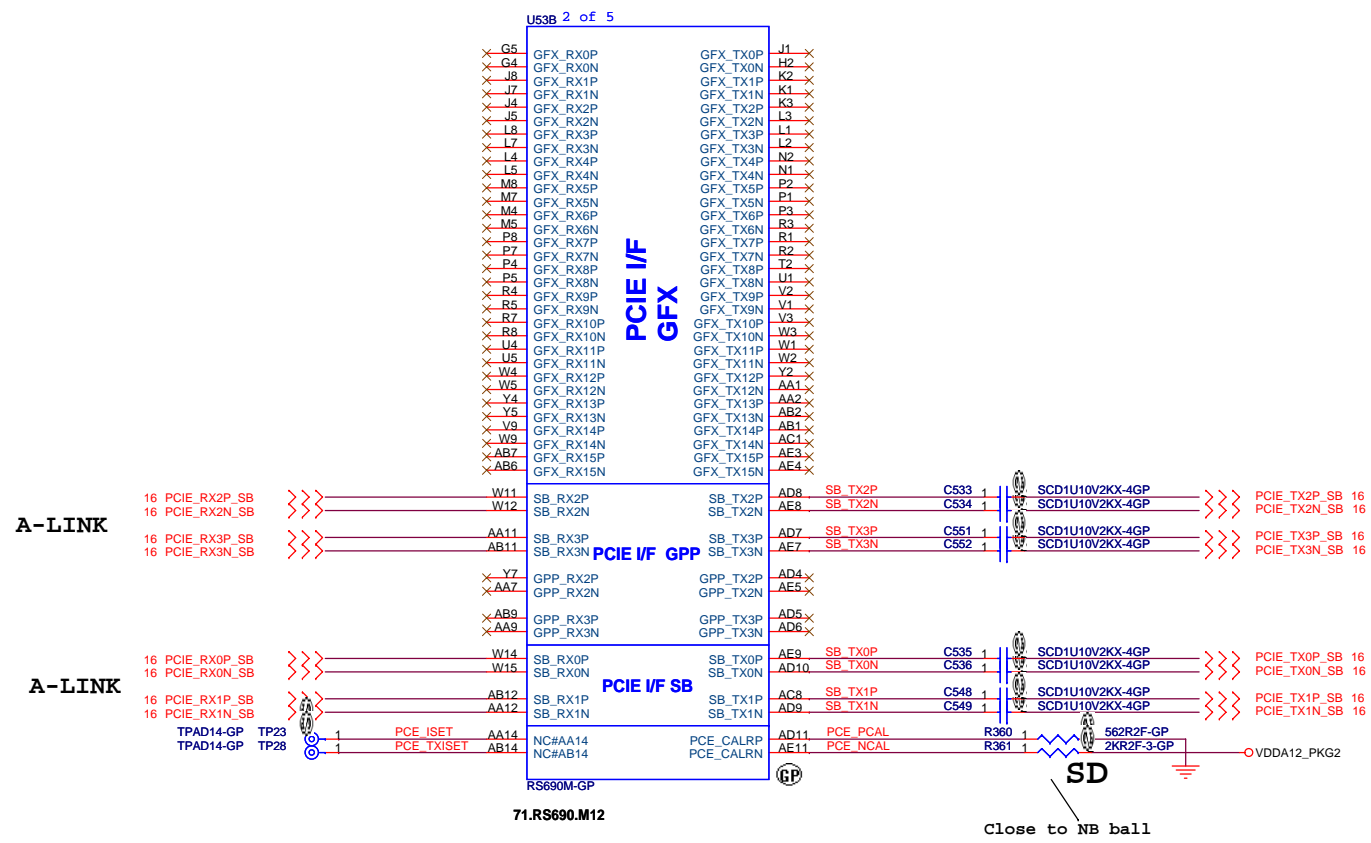


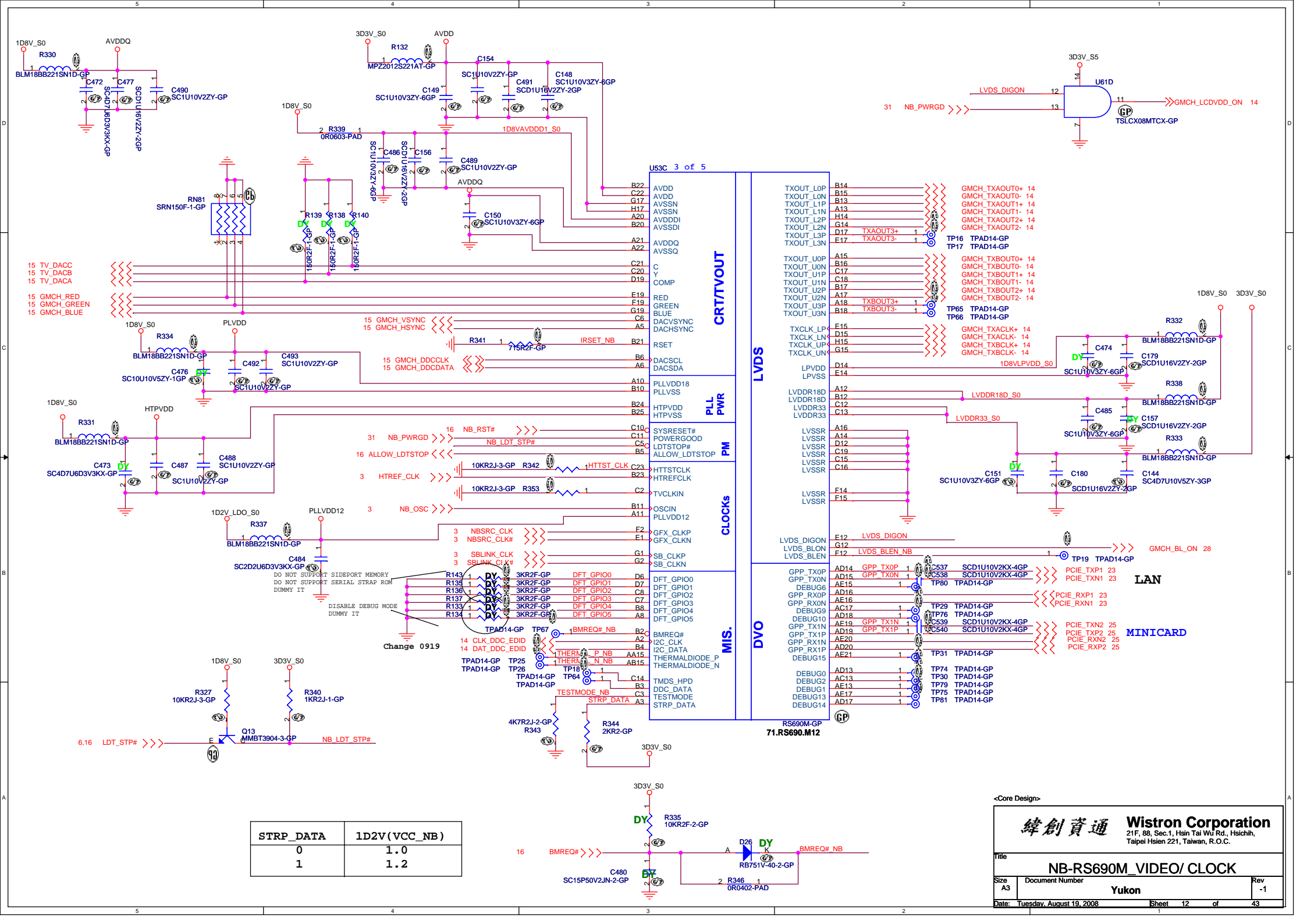
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Title
NB-RS690M HT

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15 TV_DACB
15 TV_DACB
15 TV_DACA

15 GMCH_RED
15 GMCH_GREEN
15 GMCH_BLUE

DO NOT SUPPORT SIDEPORT MEMORY
DO NOT SUPPORT SERIAL STRAP ROM
DUMMY IT

DISABLE DEBUG MODE
DUMMY IT

STRP_DATA	1D2V(VCC_NB)
0	1.0
1	1.2

U53C 3 of 5

CRT/TVOUT

LVDS

PLL PWR

PM

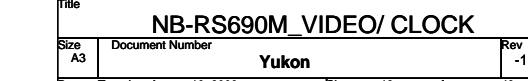
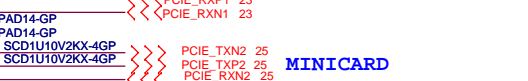
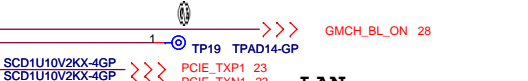
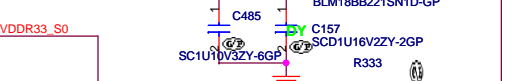
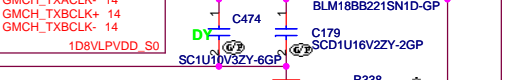
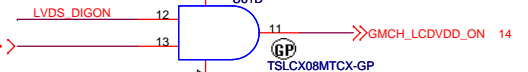
CLOCKS

MIS.

DVO

RS690M-GP
71.RS690.M12

B14 TXOUT_L0P
B15 TXOUT_L0N
B13 TXOUT_L1P
A13 TXOUT_L1N
H14 TXOUT_L2P
G14 TXOUT_L2N
D17 TXAOUT3+
E17 TXAOUT3-
A15 TXOUT_U0P
B16 TXOUT_U0N
C17 TXOUT_U1P
C18 TXOUT_U1N
B17 TXOUT_U2P
A18 TXBOUT3+
B18 TXBOUT3-
E15 TXCLK_LP
D15 TXCLK_LN
G15 TXCLK_UP
G15 TXCLK_UN
D14 LPVDD
E14 LPVSS
A12 LVDDR18D
B12 LVDDR18D
C12 LVDDR33
C13 LVDDR33
A16 LVSSR
A14 LVSSR
D12 LVSSR
C19 LVSSR
C15 LVSSR
C16 LVSSR
F14 LVSSR
F15 LVSSR



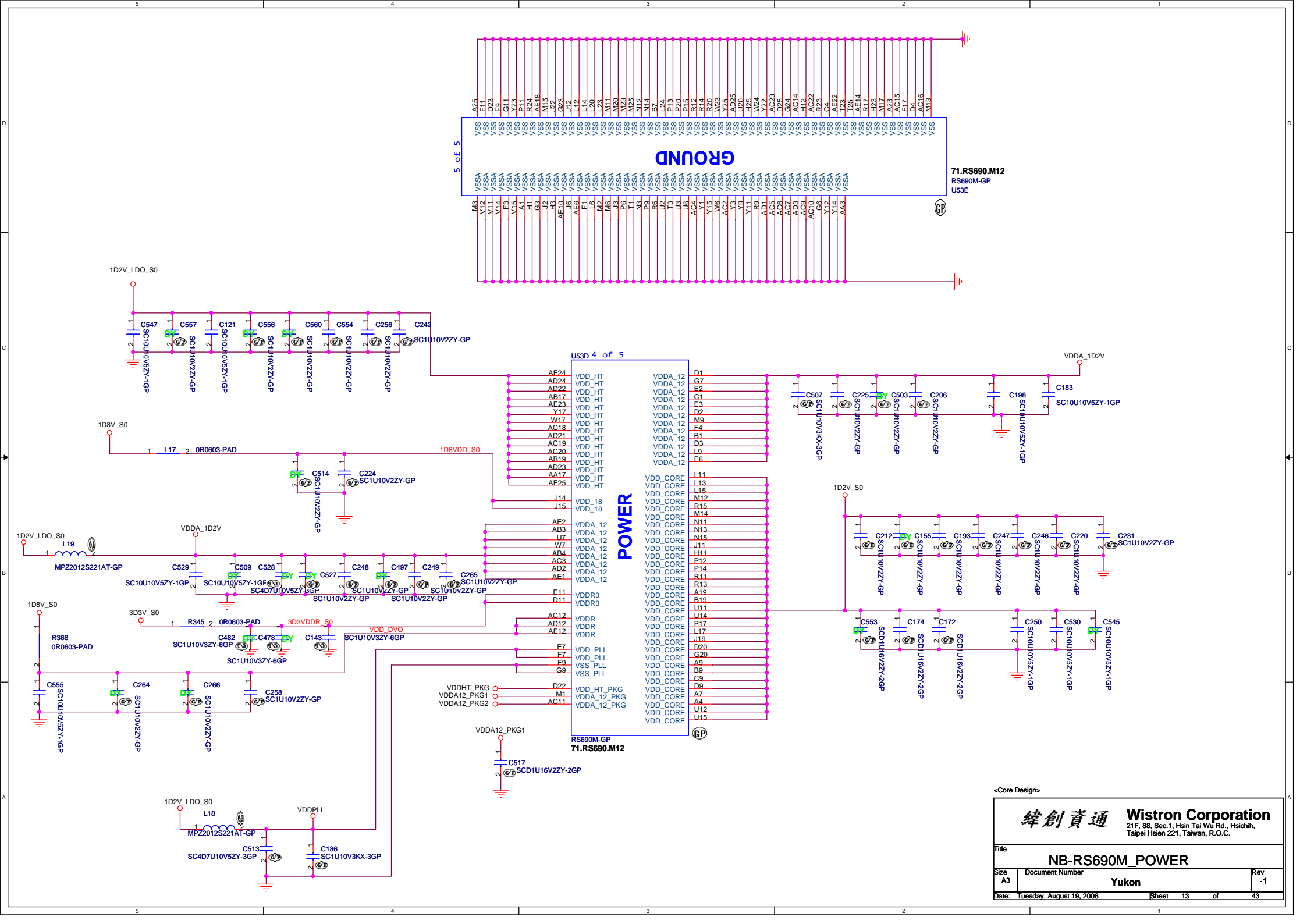
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緯創資通 Wistron Corporation
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Title: **NB-RS690M_VIDEO/ CLOCK**

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GROUND

71.RS690.M12
RS690M-GP
U53E

U53D 4 of 5

POWER

RS690M-GP
71.RS690.M12

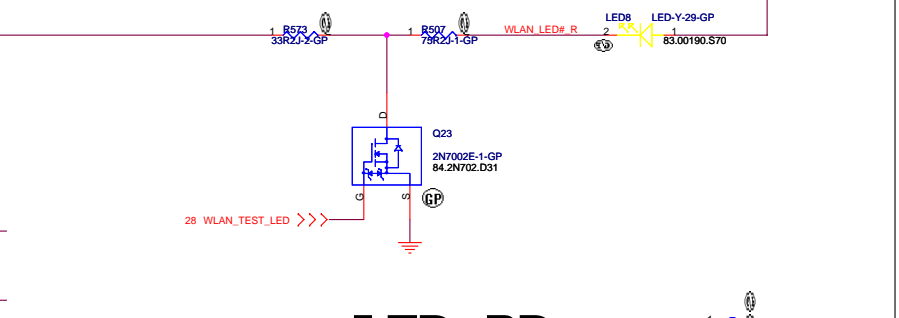
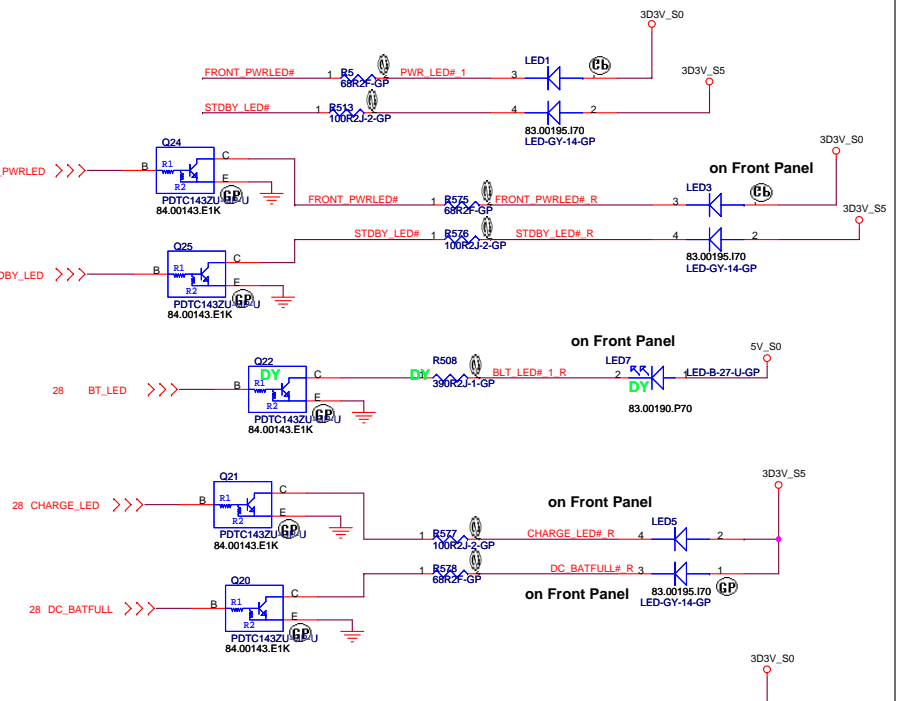
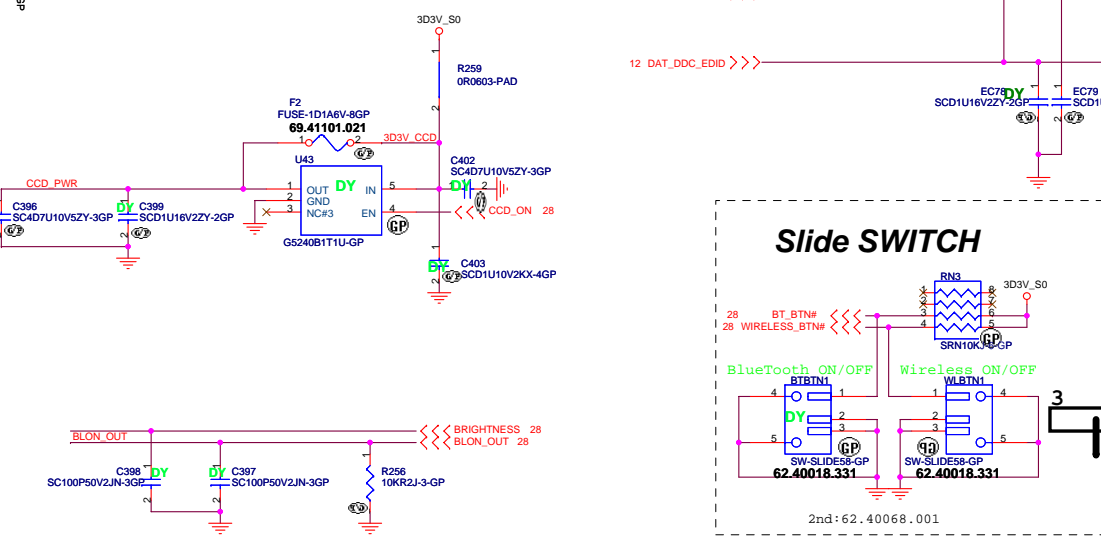
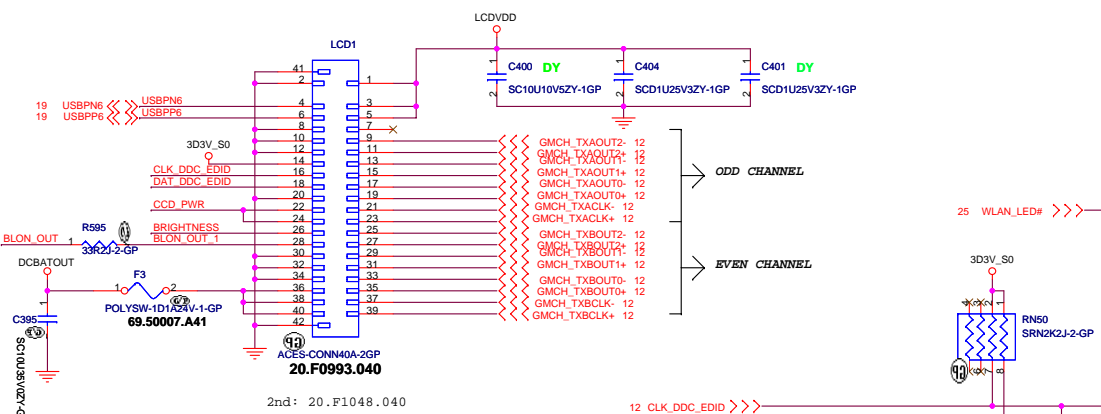
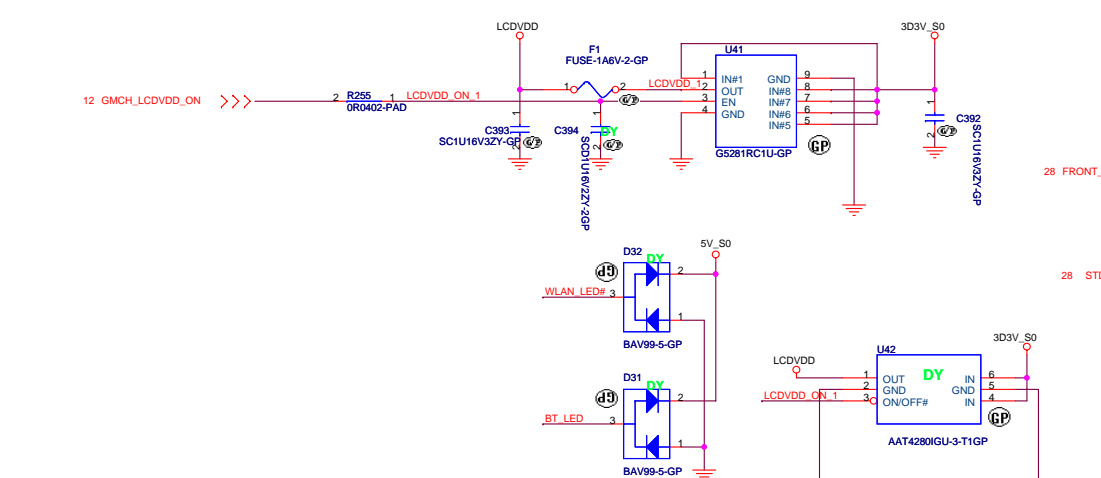
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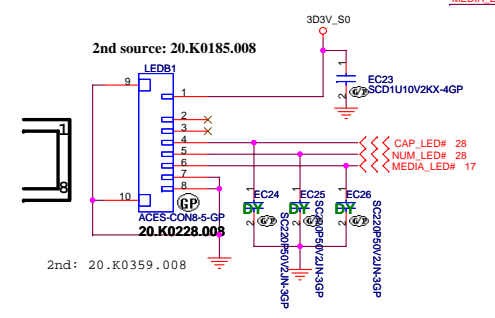
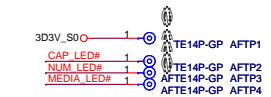
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LCD/INVERTER CONN

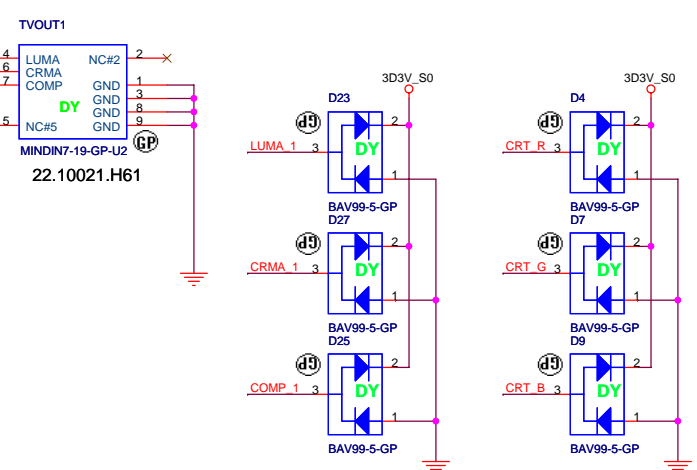
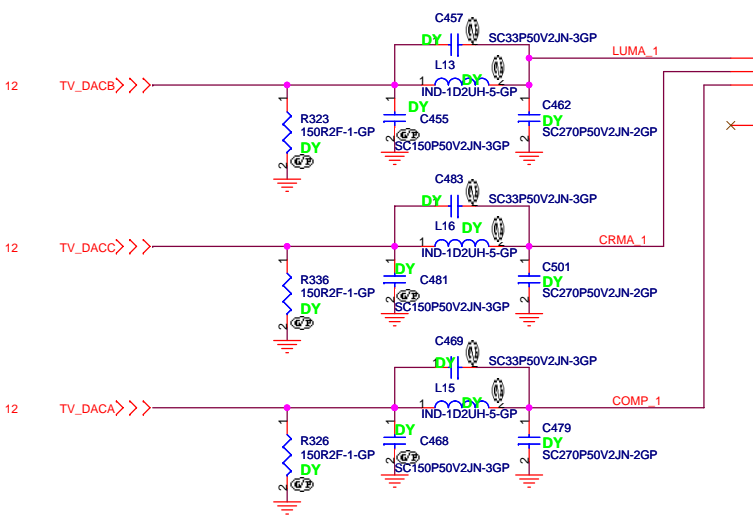
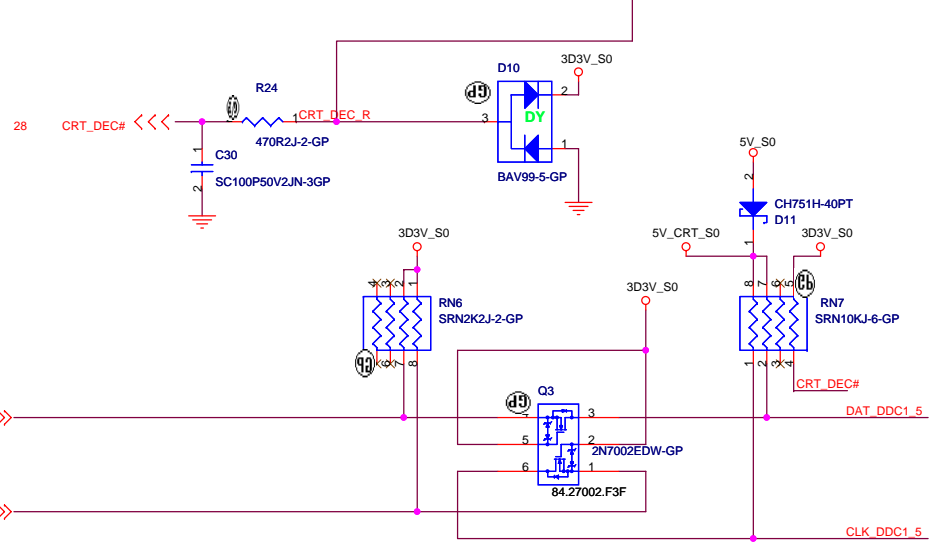
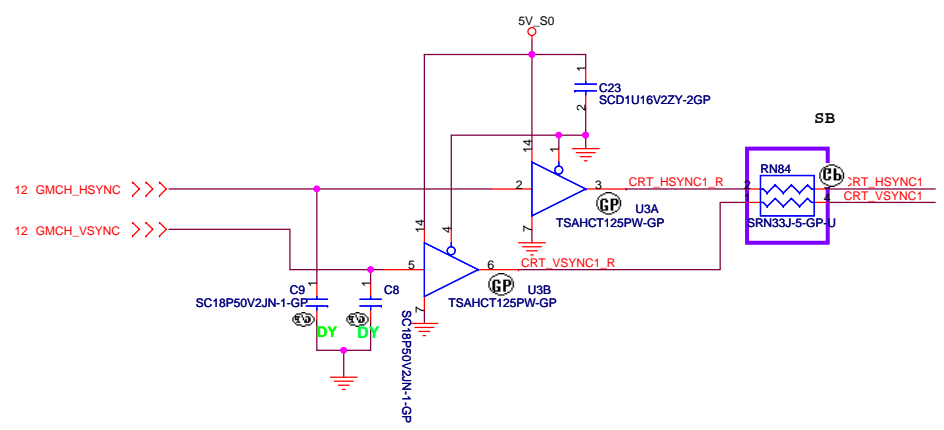
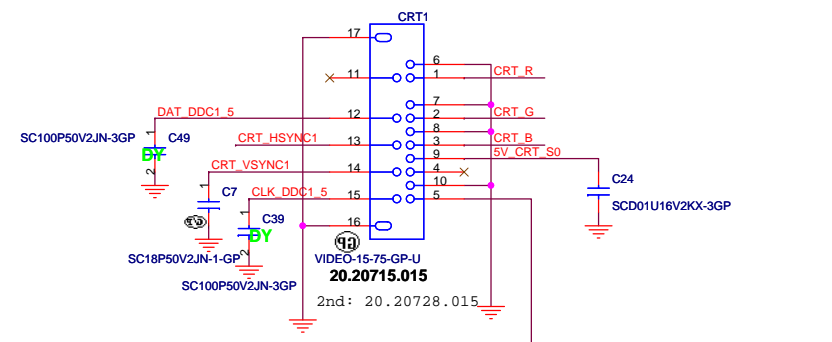
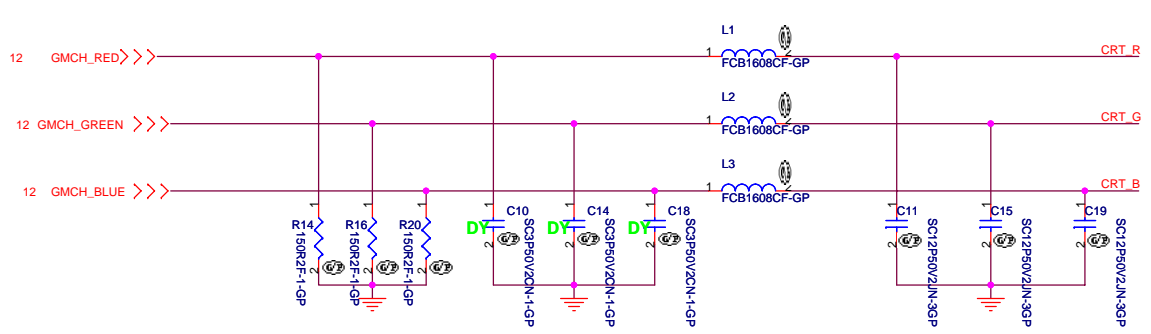


LED BD



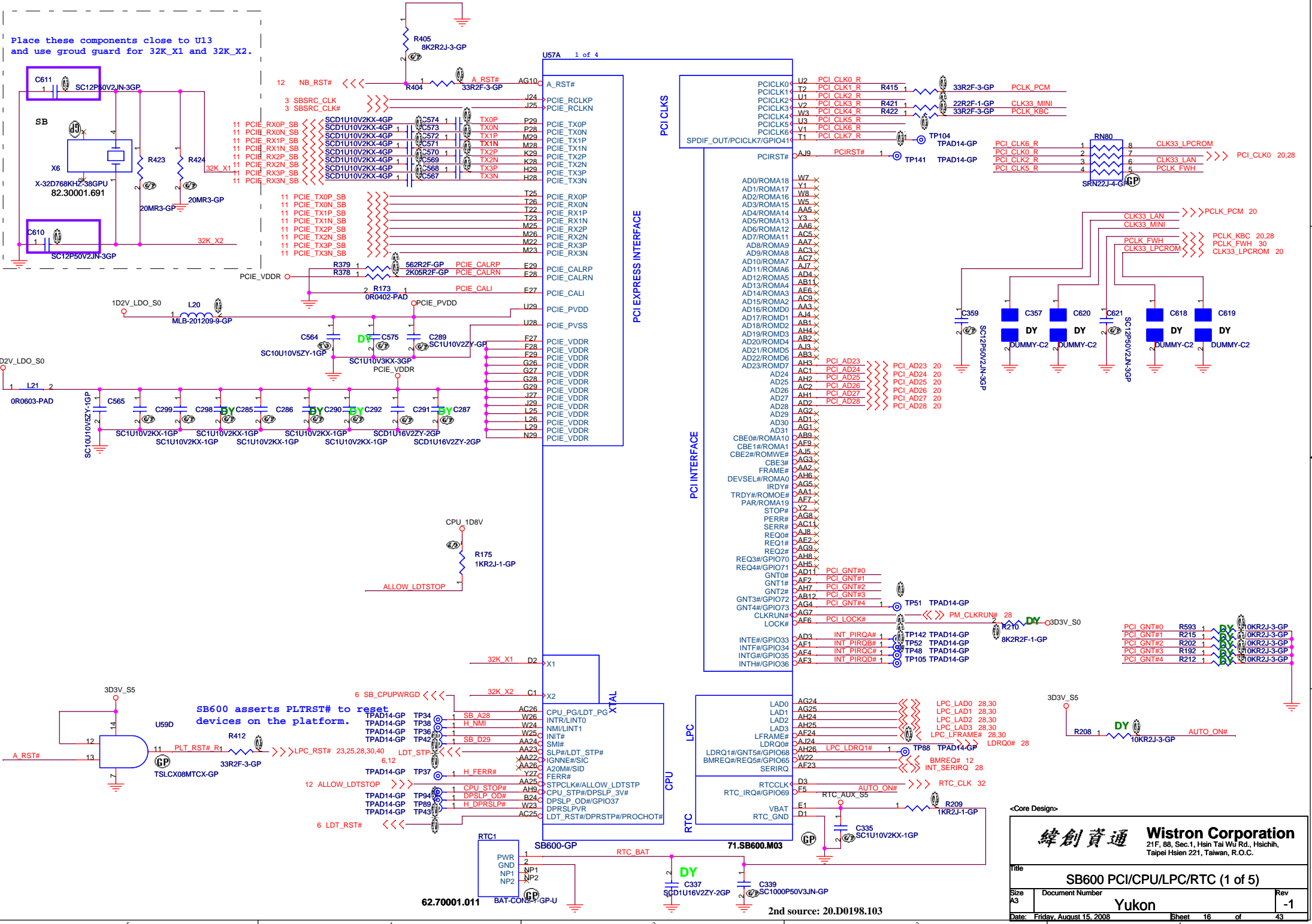
<Variant Name>

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File LCD CONN & LED	
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Title: CRT/TV Connector	
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Place these components close to U13 and use ground guard for 32K_X1 and 32K_X2.



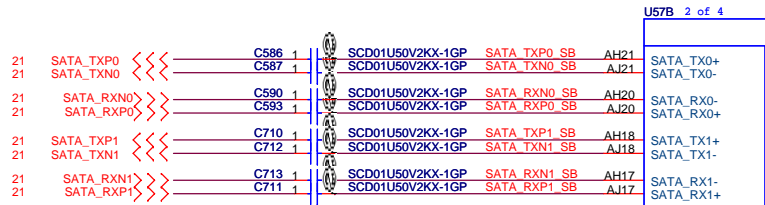
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 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **SB600 PCI/CPU/LPC/RTC (1 of 5)**

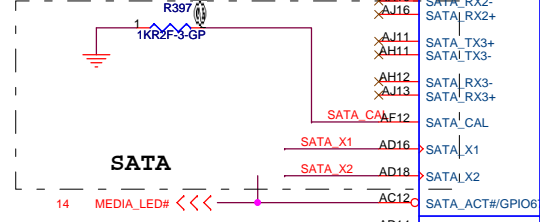
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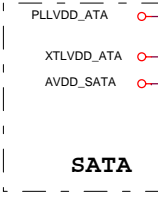
PLACE SATA AC DECOUPLING CAPS CLOSE TO SB460



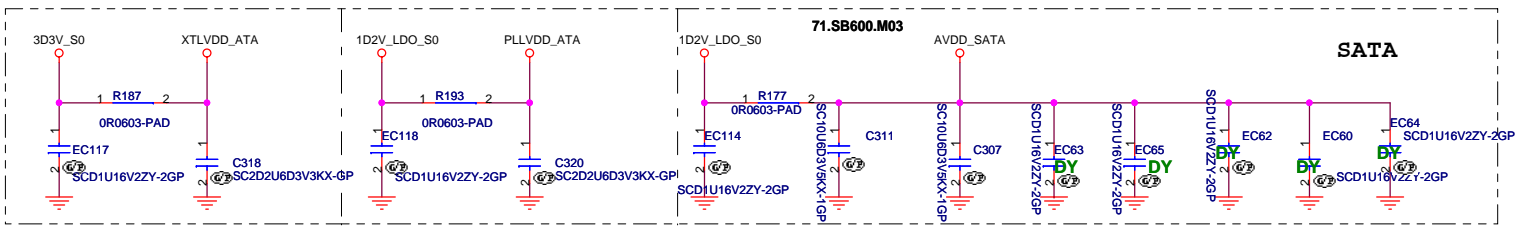
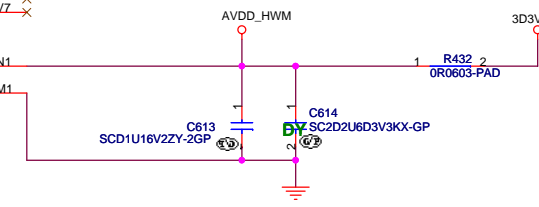
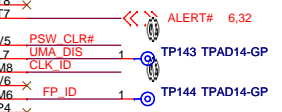
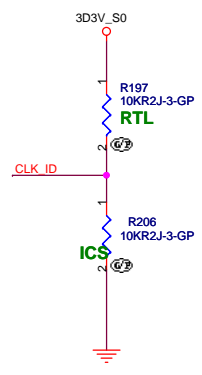
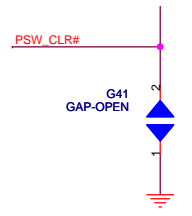
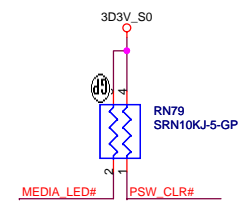
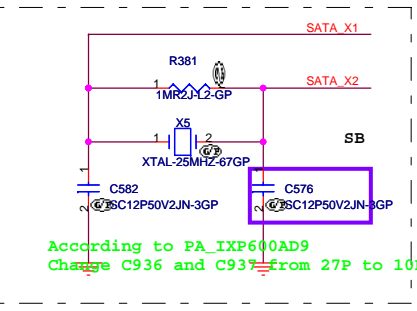
SATA



SATA



SATA



<Core Design>

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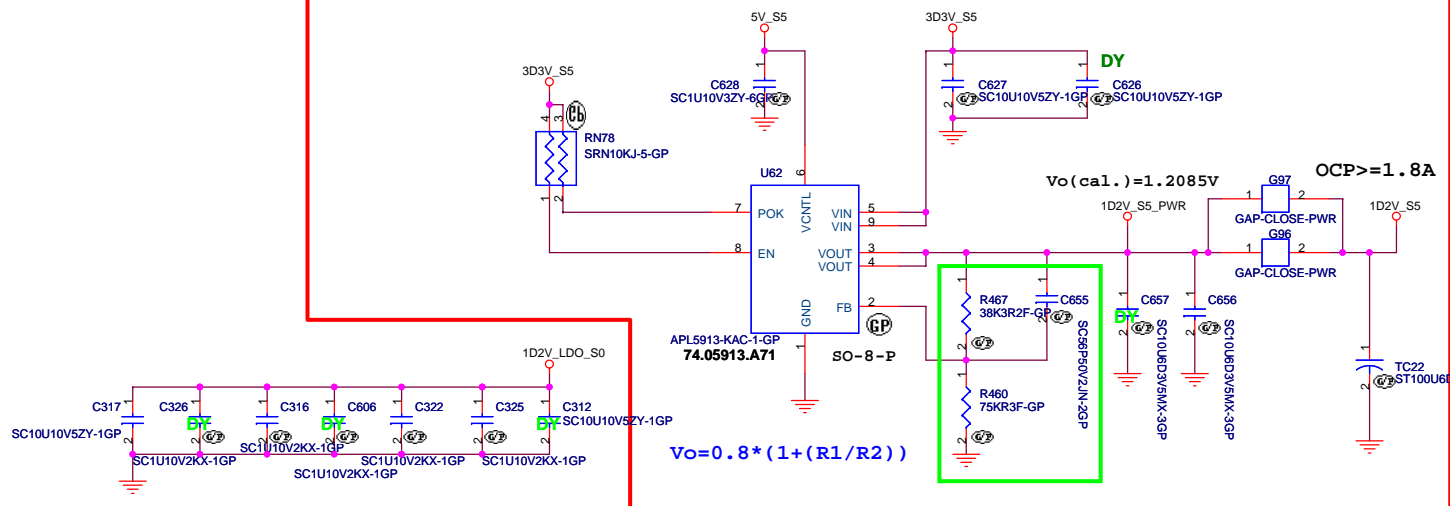
Title: SB600 ACPI/GPIO/SATA/IDE (2 of 5)

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Date: Friday, August 15, 2008

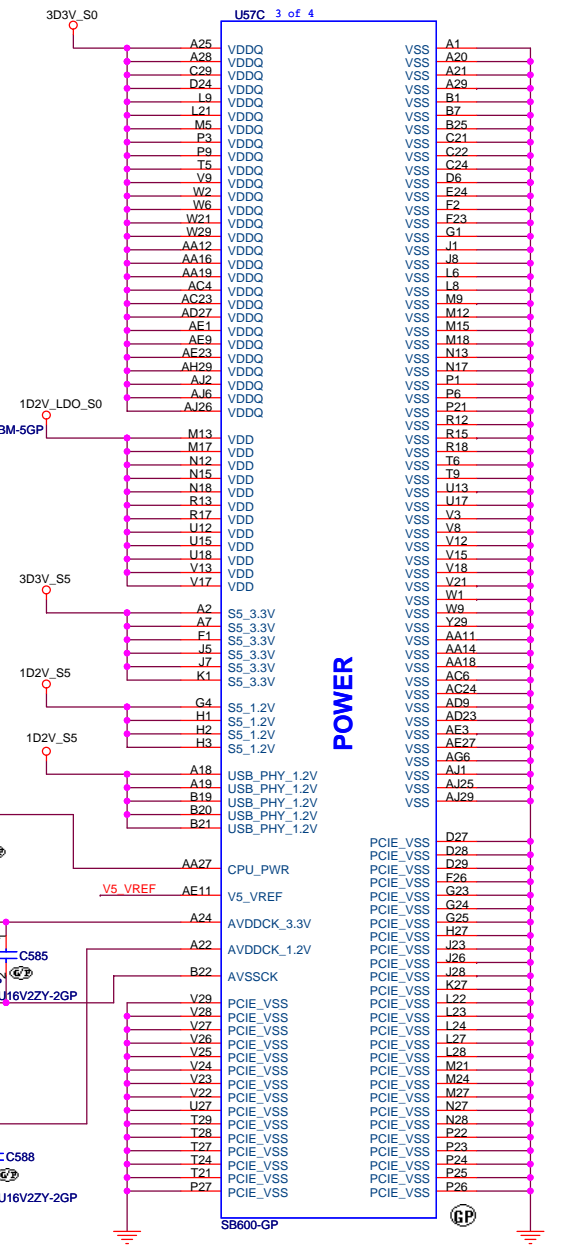
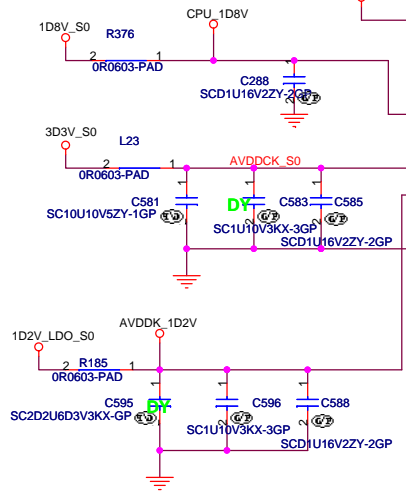
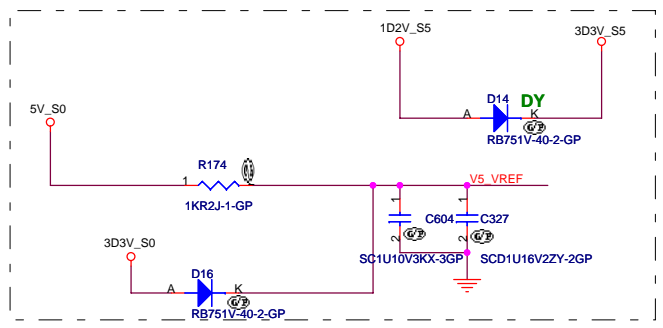
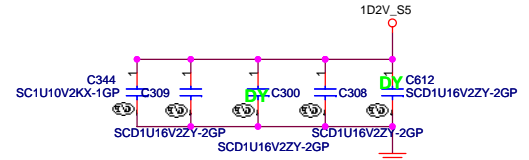
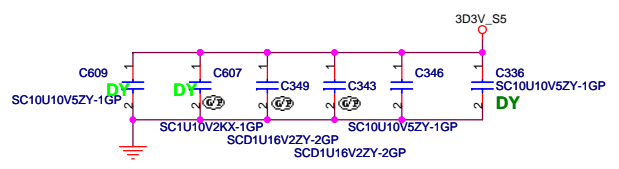
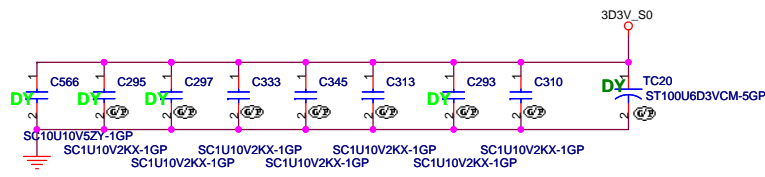
Yukon

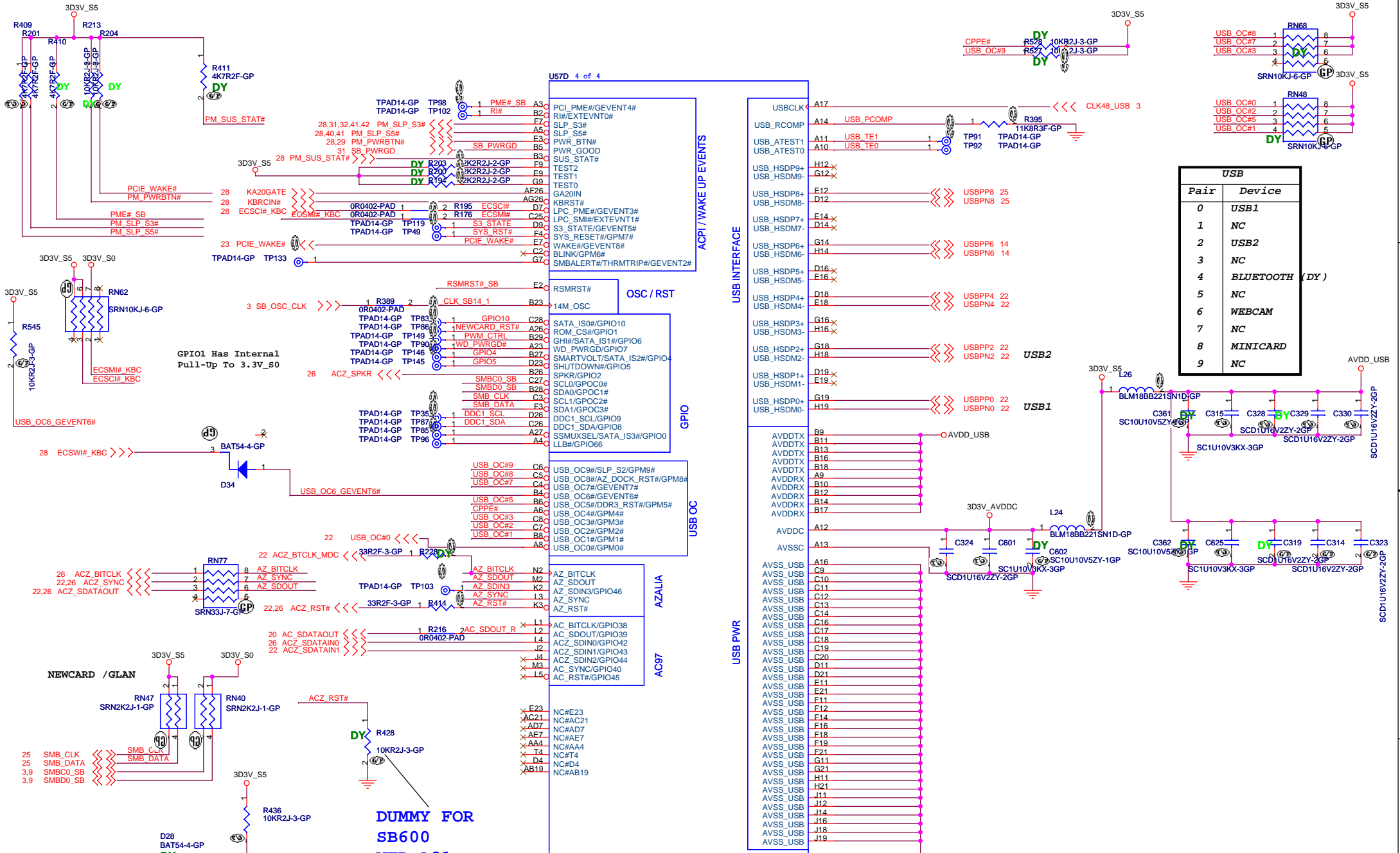
Rev: -1
Sheet 17 of 43

1D2V_S5
Iomax=1A




Place near to SB600





USB	
Pair	Device
0	USB1
1	NC
2	USB2
3	NC
4	BLUETOOTH (DY)
5	NC
6	WEBCAM
7	NC
8	MINICARD
9	NC

<Core Design>


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 Taipei Hsien 221, Taiwan, R.O.C.

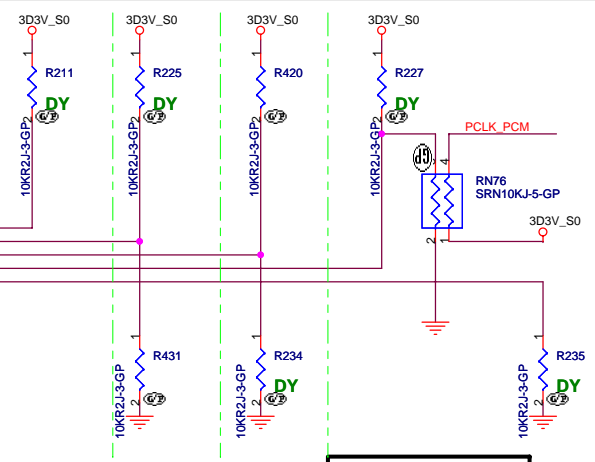
SB600 AC97/USB		
Title	Document Number	Rev
Yukon		-1
Date: Monday, August 18, 2008	Sheet 19 of 43	

DUMMY FOR SB600 VER. A21

71.SB600.M03

PCI_CLK4
PCI_CLK6
PCI_CLK0
PCI_CLK1

19 AC_SDATAOUT
16,28 PCLK_KBC
15 CLK33_LPCROM
16,28 PCL_CLK0
16 PCLK_PCM

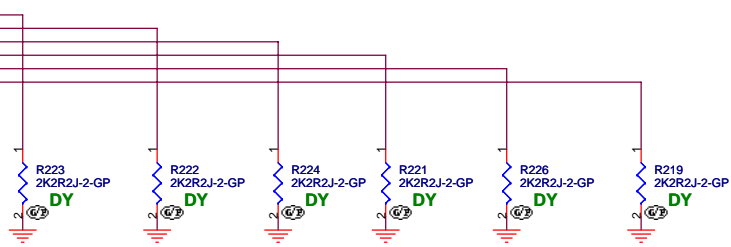


REQUIRED SYSTEM STRAPS

		SB600				
		AC_SDATAOUT	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM		
	IGNORE DEBUG STRAPS DEFAULT	USE EXT. 48MHZ DEFAULT	CPU IF=P4	DEFAULT		

SB600 HAS 15K INTERNAL PU FOR PCI_AD[23..28]

16 PCI_AD28
16 PCI_AD27
16 PCI_AD26
16 PCI_AD25
16 PCI_AD24
16 PCI_AD23



DEBUG STRAPS

	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
STRAP HIGH	RESERVED	RESERVED	RESERVED	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOT FAIL TIMER DISABLE DEFAULT
STRAP LOW				USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOT FAIL TIMER ENABLE

<Core Design>

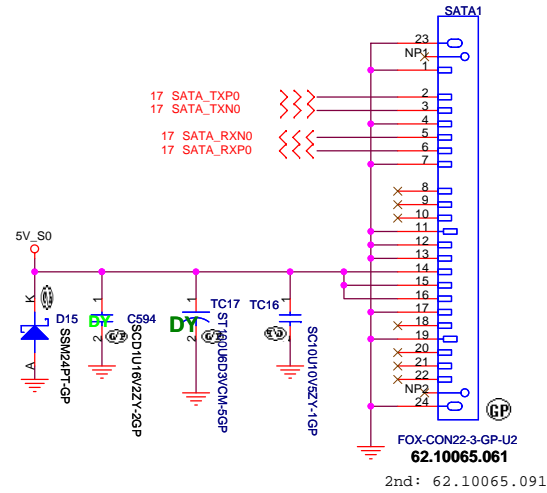
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **SB600 STRAPPING PIN**

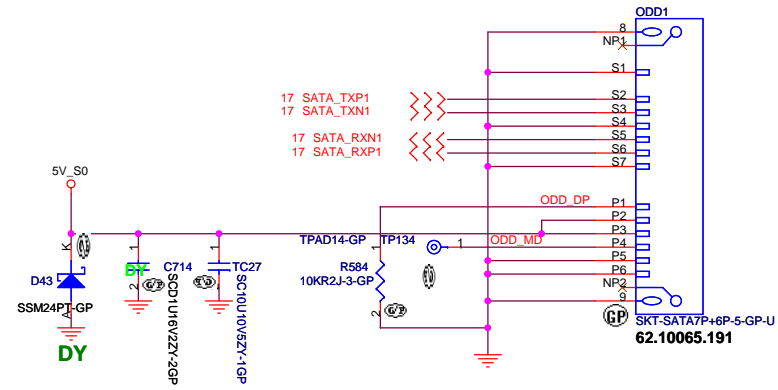
Size A3 Document Number Yukon Rev -1

Date: Monday, August 18, 2008 Sheet 20 of 43

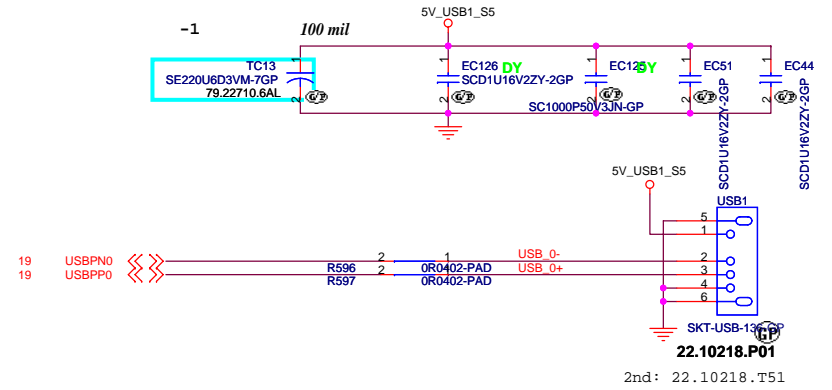
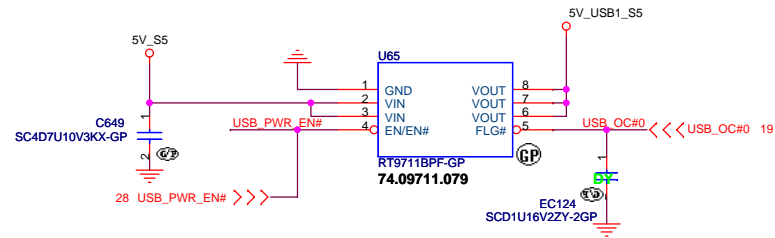
SATA HD Connector



SATA ODD Connector

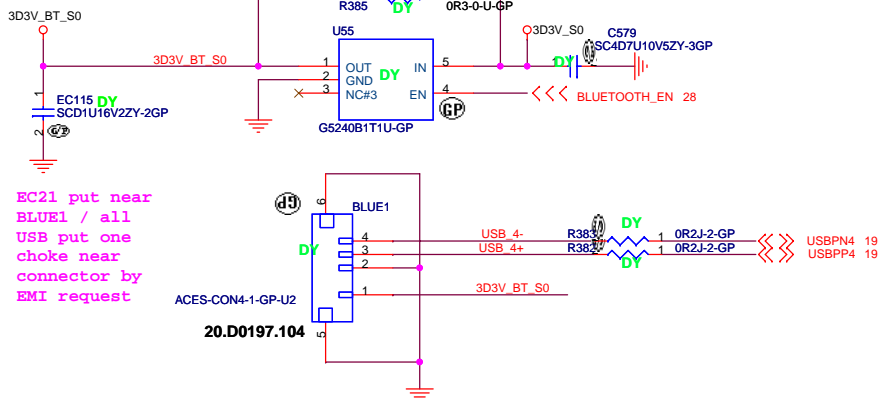


bom1

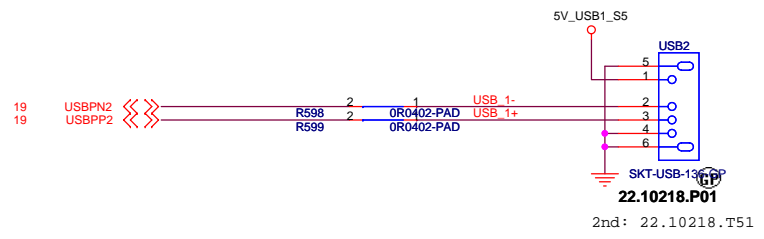


2nd: 22.10218.T51

BLUETOOTH MODULE

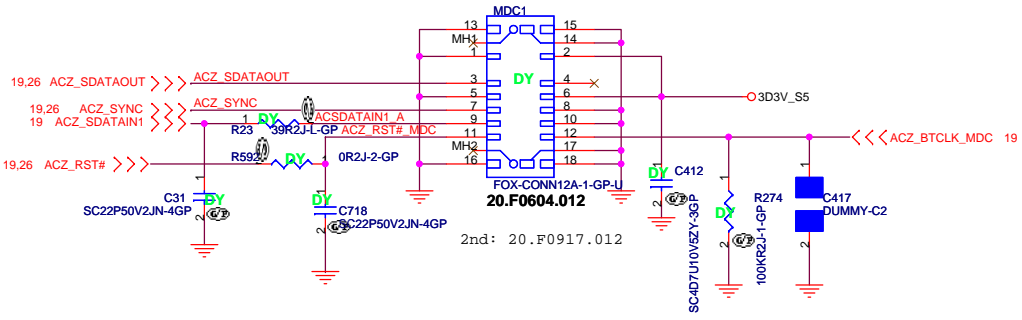


EC21 put near BLUE1 / all USB put one choke near connector by EMI request

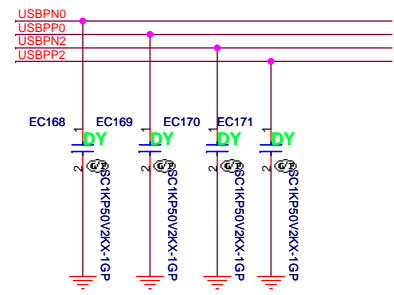


2nd: 22.10218.T51

MDC 1.5 CONN

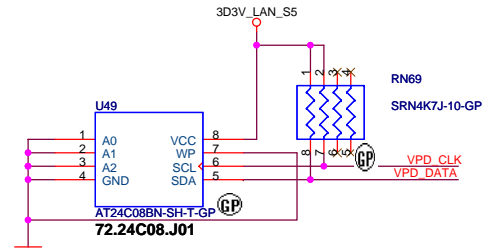
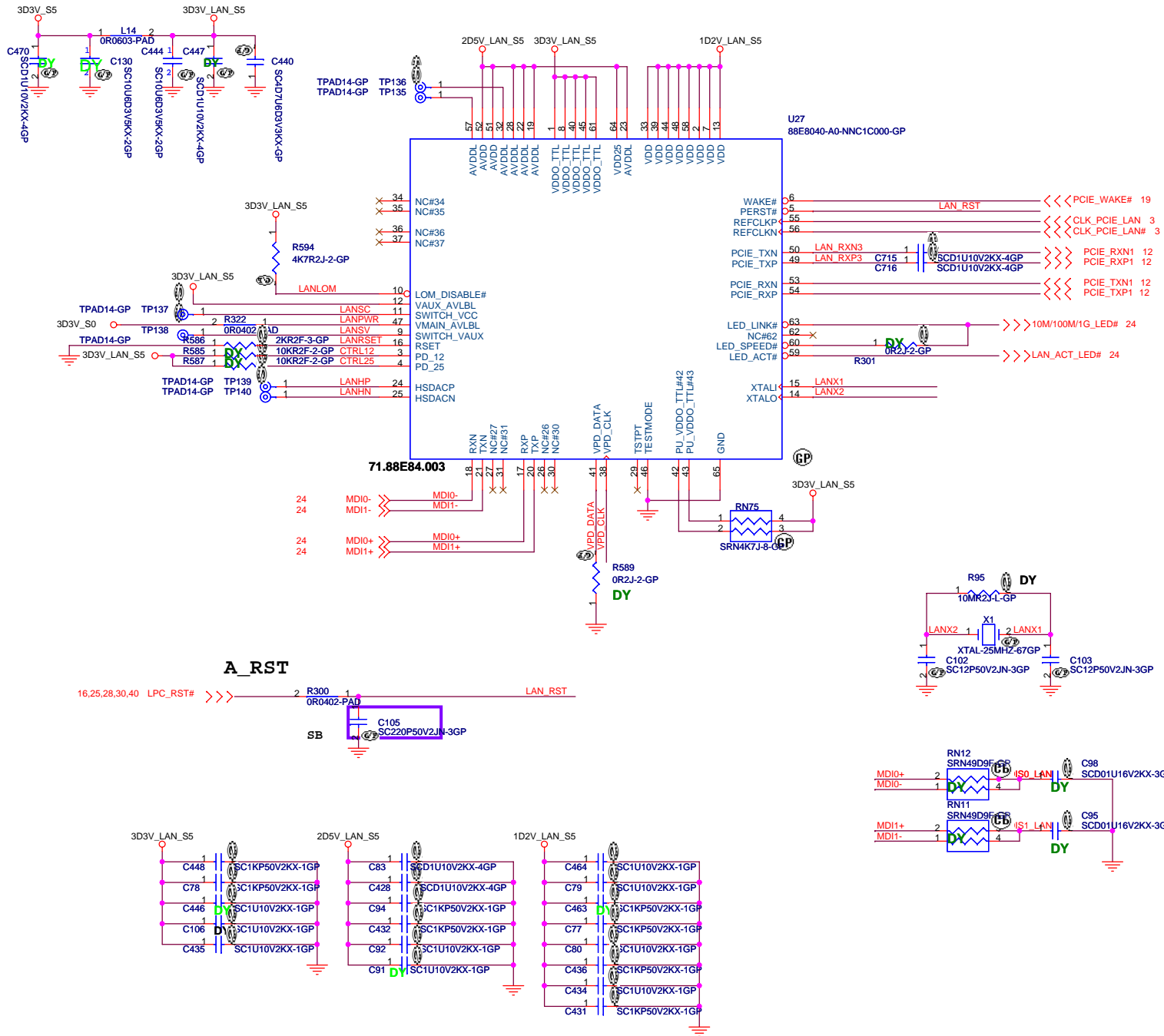


2nd: 20.F0917.012



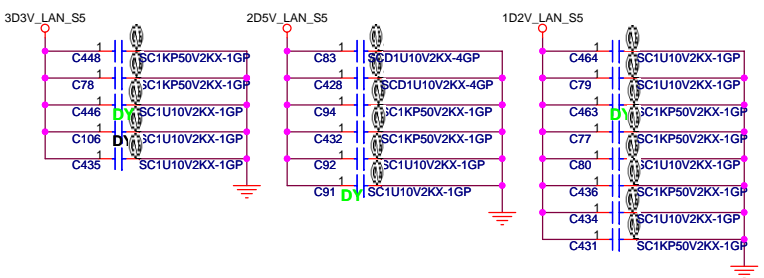
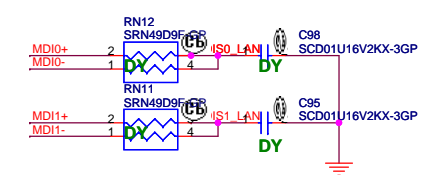
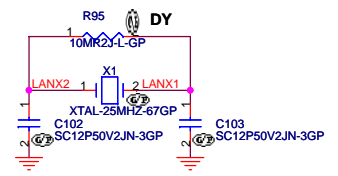
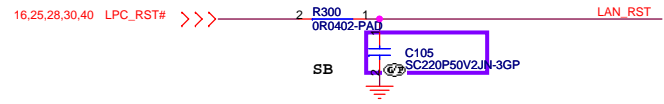
bom1

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USB / MDC / BLUETOOTH			
Title	Document Number	Rev	
		Yukon	
Date: Wednesday, August 13, 2008	Sheet 22	of	43



Pull up for AT24C08 another pull low

A_RST



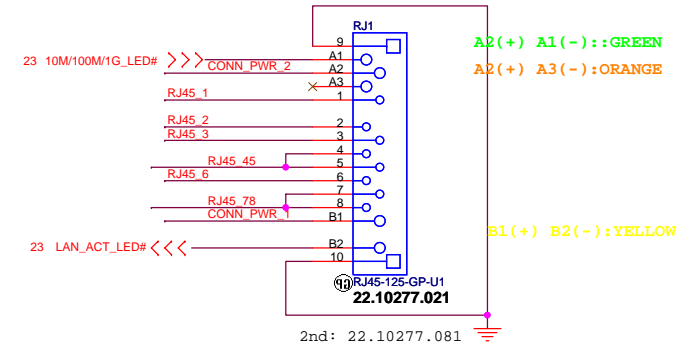
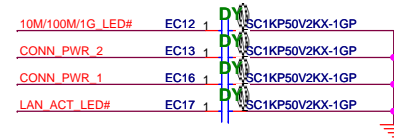
<Variant Name>

緯創資通 Wistron Corporation
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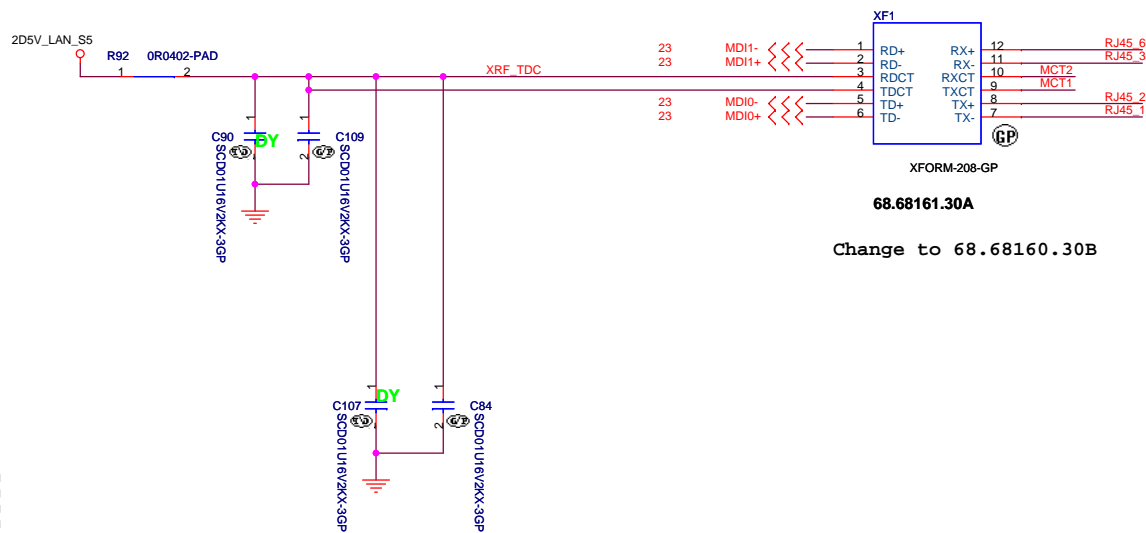
Title: **MARVELL 88E8040**

Size A3	Document Number	Rev
	Yukon	-1
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LAN Connector



10/100 Lan Transformer



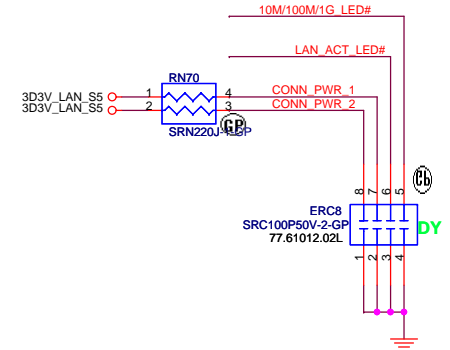
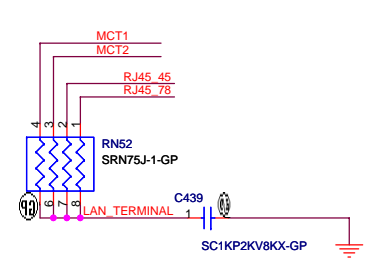
Change to 68.68160.30B

1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6



<Variant Name>

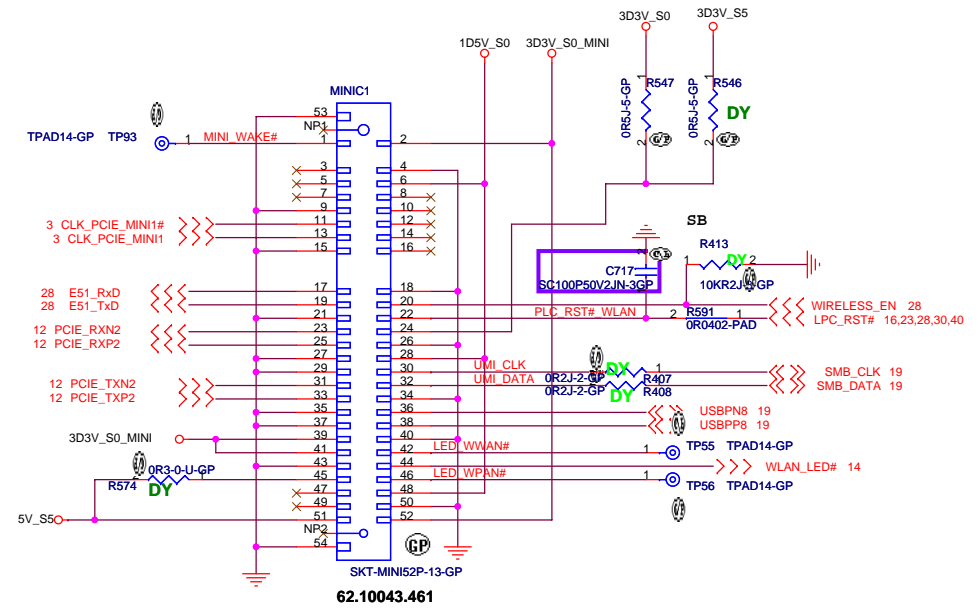
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN Connector**

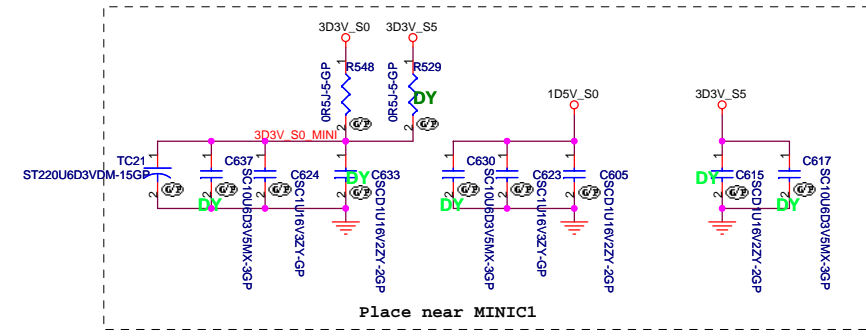
Size A3 Document Number **Yukon** Rev **-1**

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Mini Card Connector



2nd: 20.F1049.052



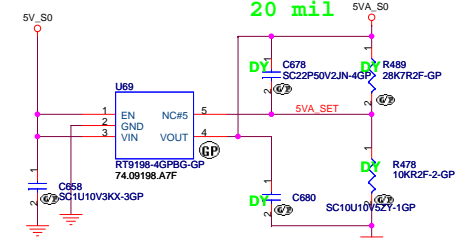
bom1

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
MINI CARD			
Size	Document Number		Rev
	Yukon		-1
Date:	Thursday, August 14, 2008		Sheet 25 of 43

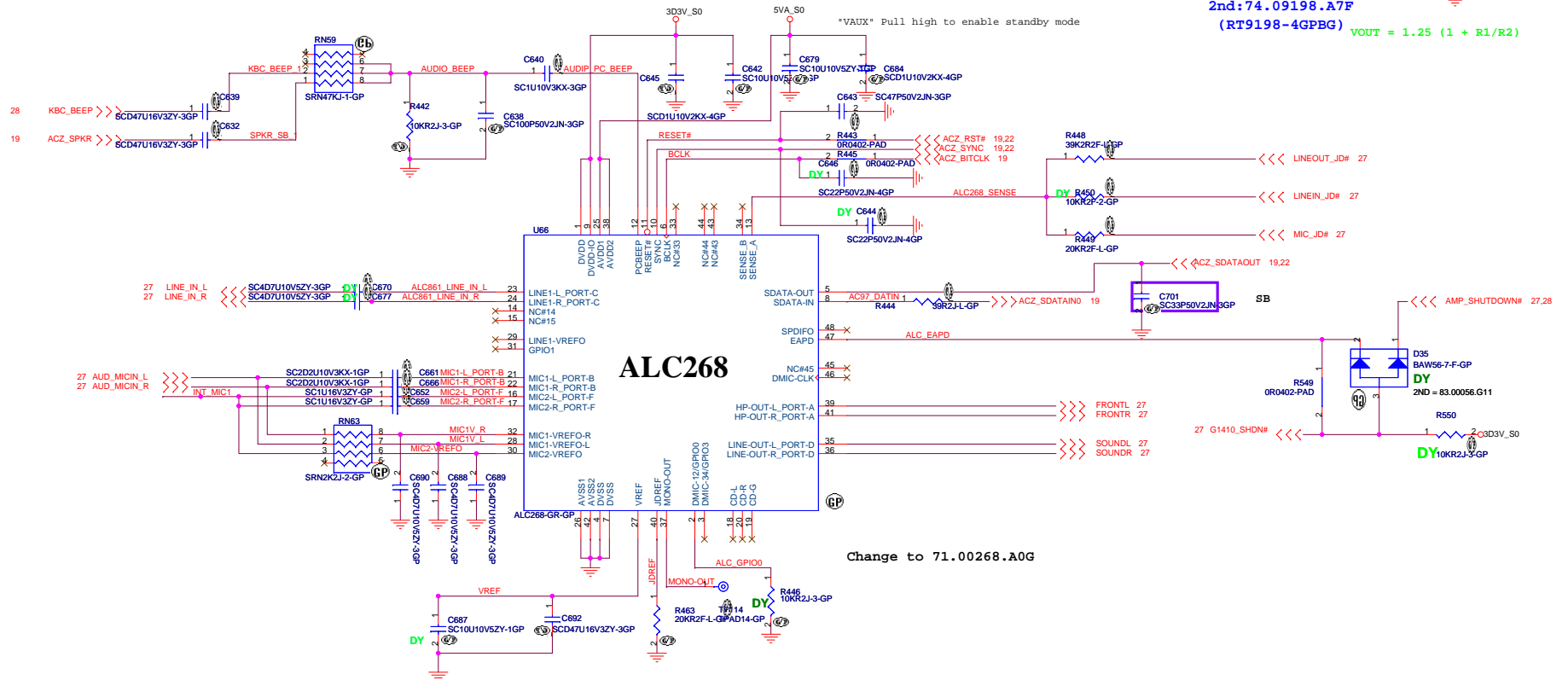
POWER GENERATE

Layout

20 mil

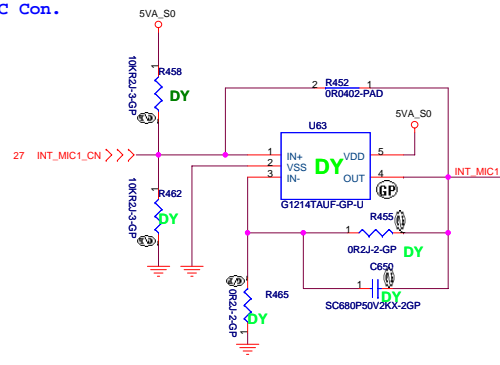


2nd: 74.09198.A7F
(RT9198-4GPBG) VOUT = 1.25 (1 + R1/R2)



Change to 71.00268.A0G

Near INTMIC Con.



<-Variant Name>

緯創資通 Wistron Corporation
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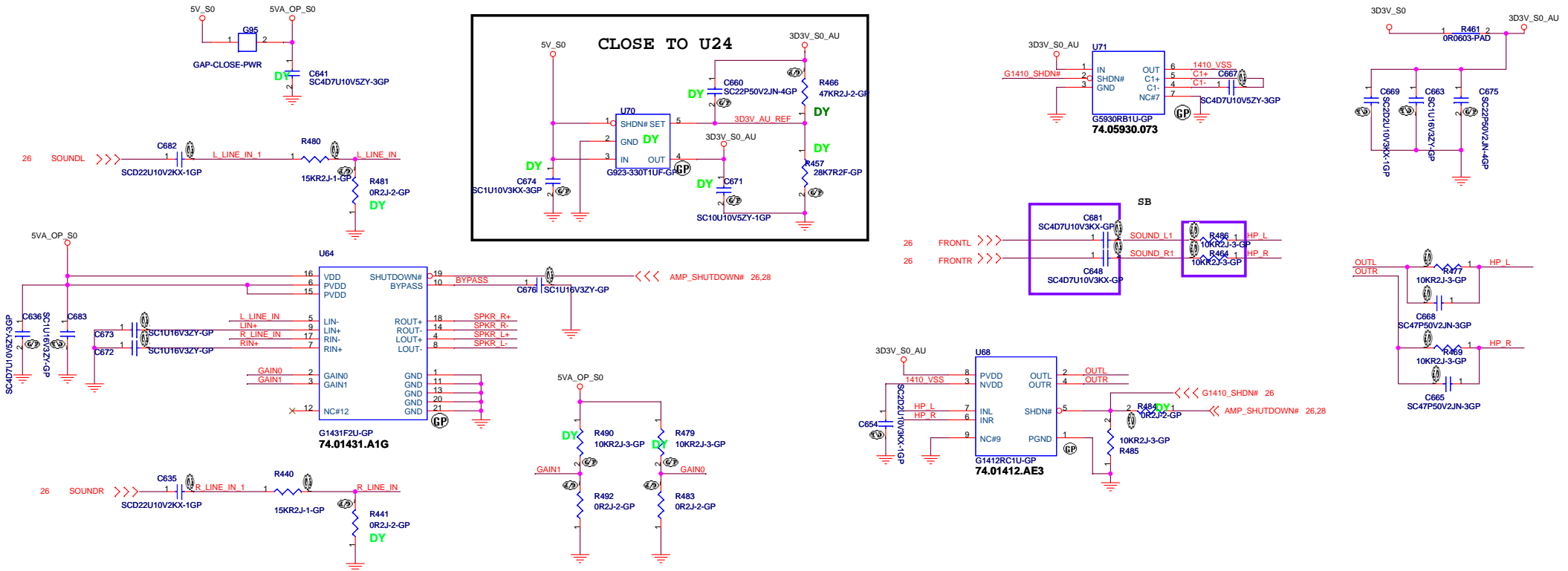
Title AZALIA CODEC - ALC268

Size Document Number Yukon Rev -1

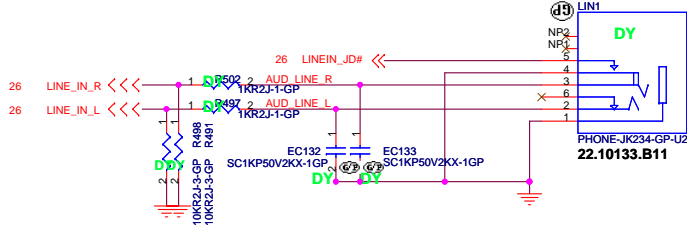
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AUDIO OP AMPLIFIER

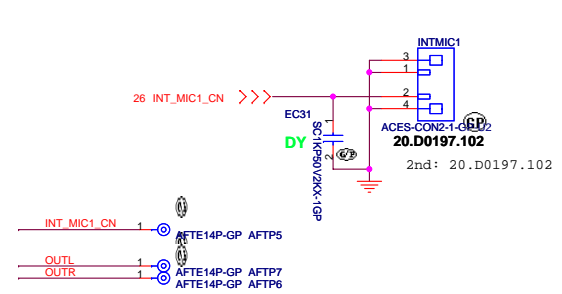
KBC_MUTE_GPIO8



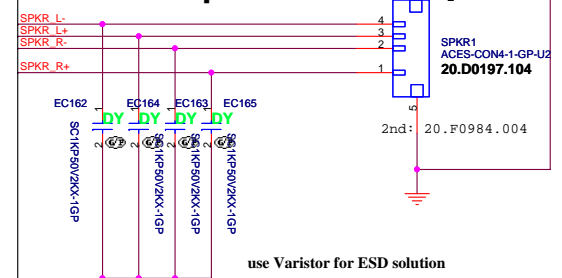
LINE IN



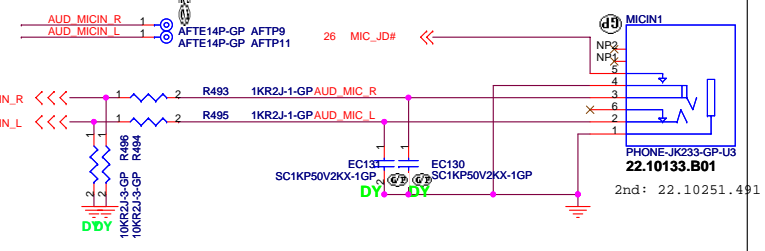
Internal Microphone



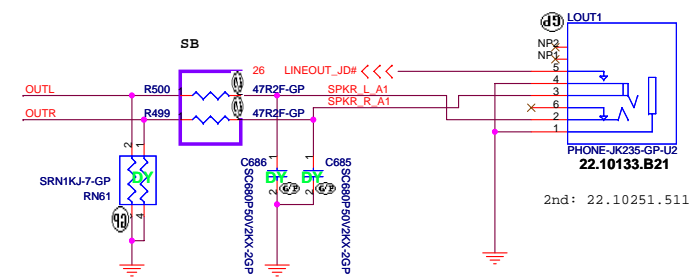
Internal Speaker



MIC IN



LINE OUT



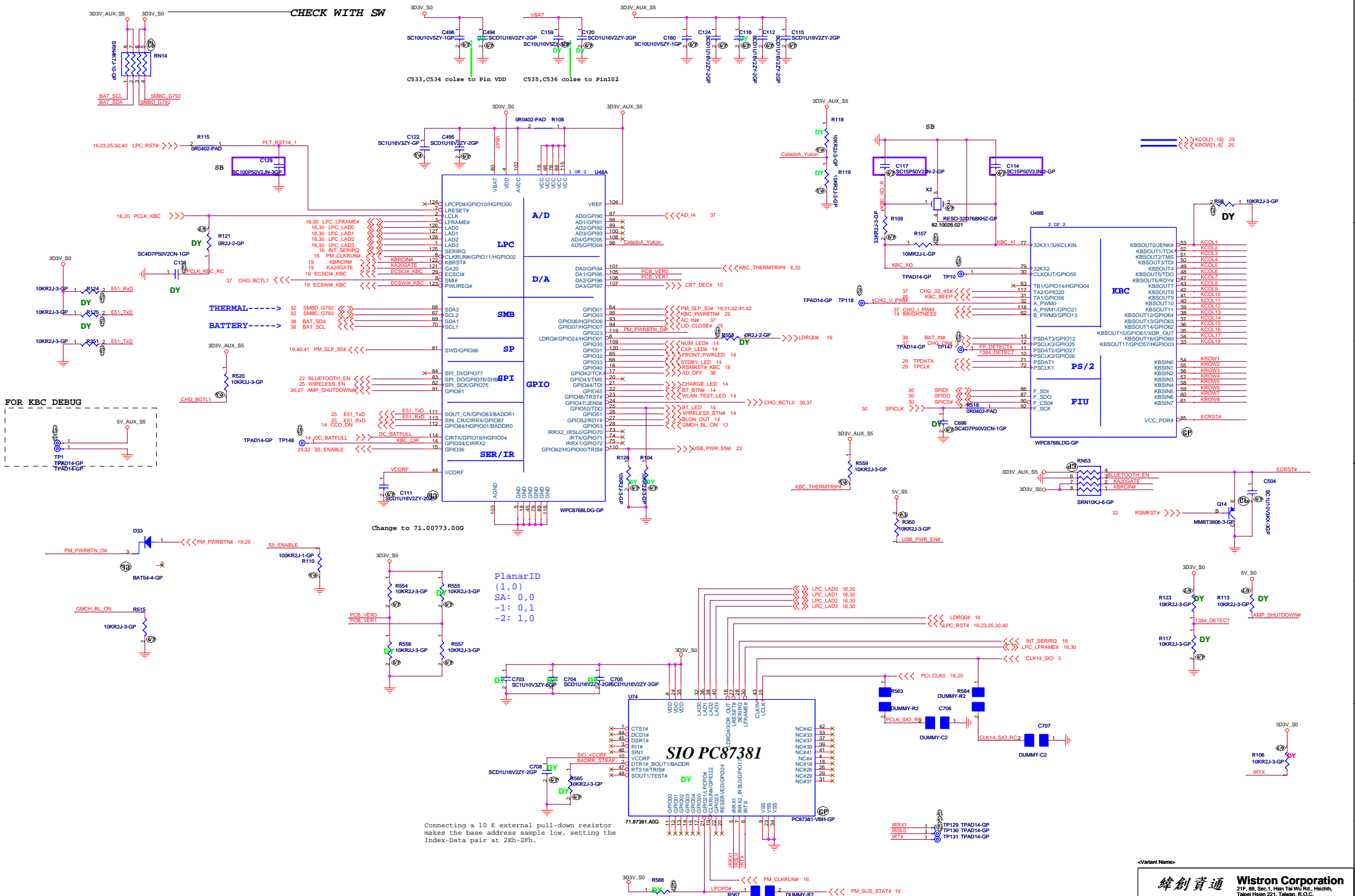
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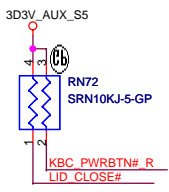
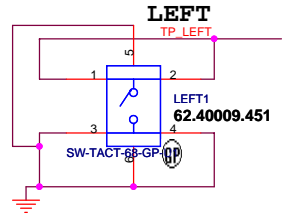
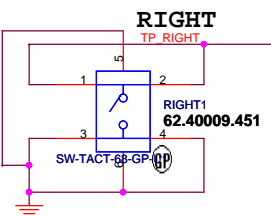
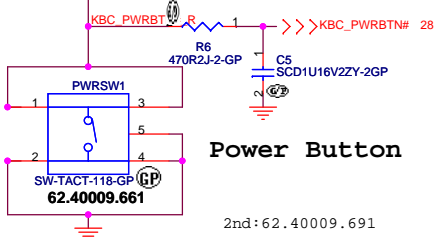
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AUDIO AMP AND JACK

Yukon

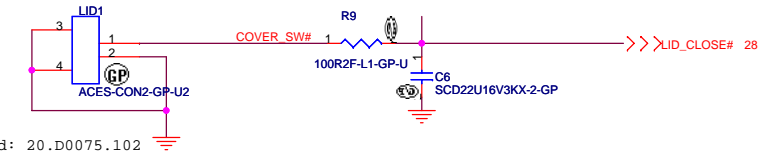
Date: Thursday, August 14, 2008 Sheet 27 of 43



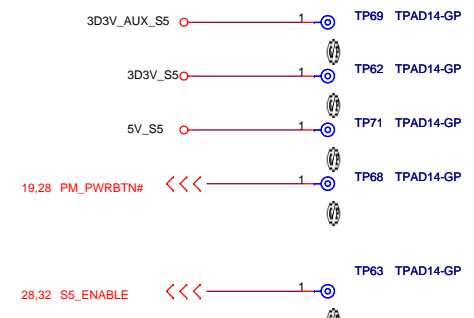


Cover Up Switch

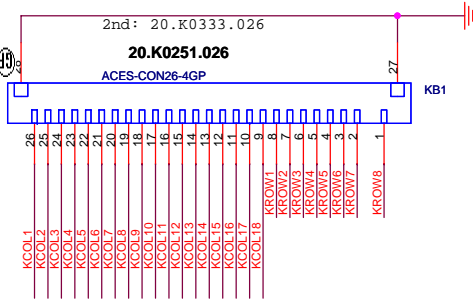
2nd source: 20.F00984.002



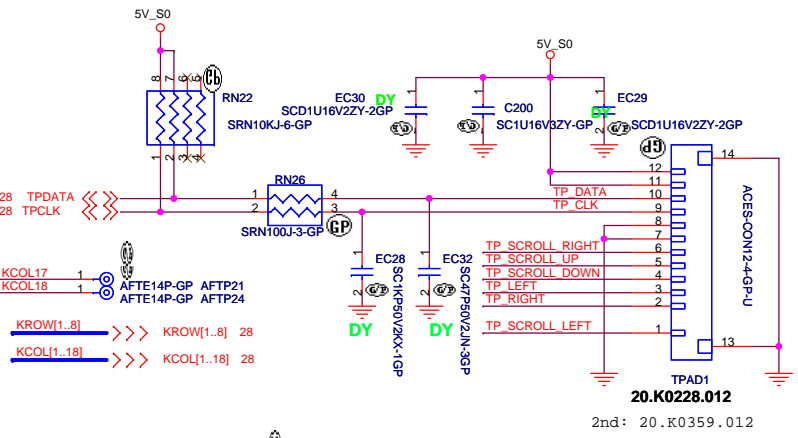
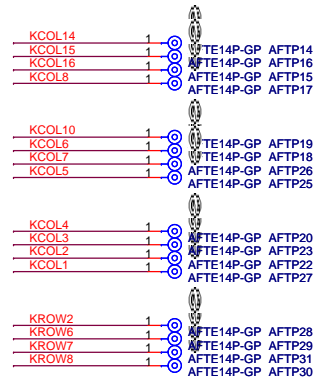
Check test point



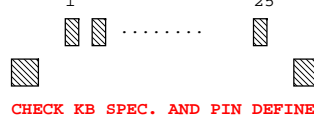
Test Point 放在 Dimm Door 打開可量測處



EMI Bypass cap.



Internal Keyboard CONN



bom1

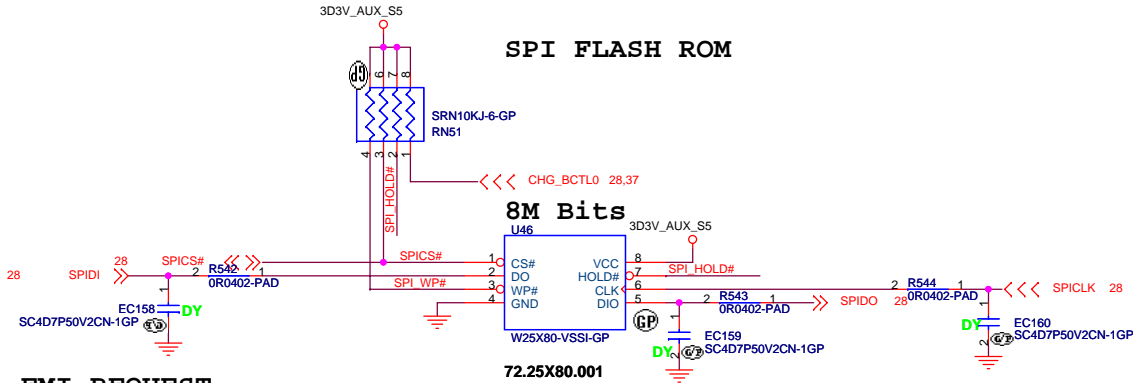
緯創資通 Wistron Corporation
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Title: **BUTTONS / KB / TOUCHPAD**

Size: Document Number: **Yukon** Rev: -1

Date: Monday, August 18, 2008 Sheet 29 of 43

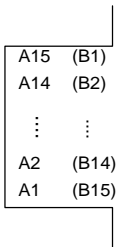
SPI FLASH ROM



EMI REQUEST

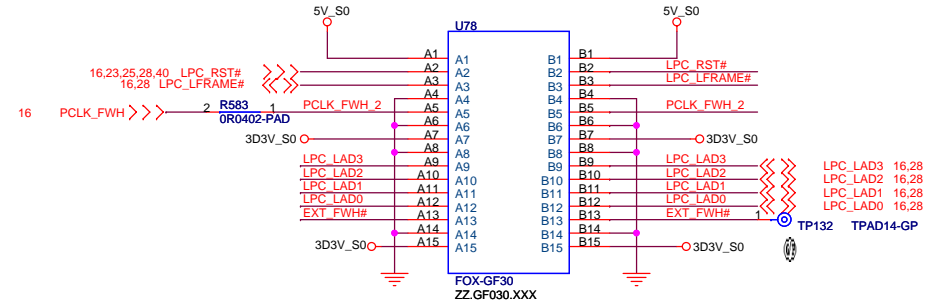
change to 72.25X80.A01

TOP VIEW

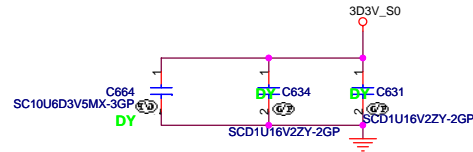


(BOTTOM VIEW)

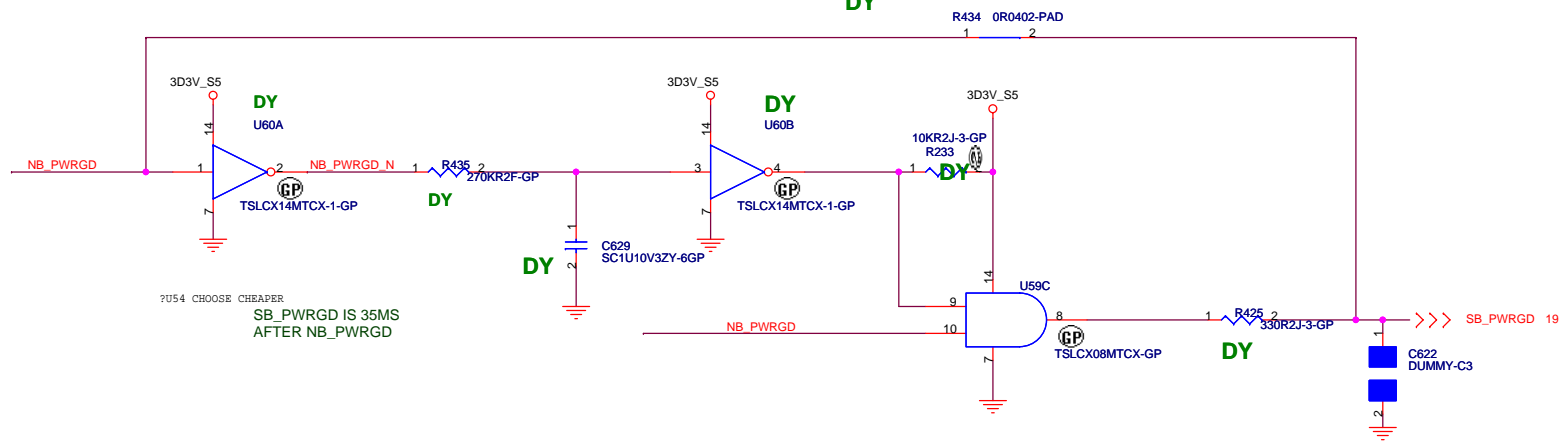
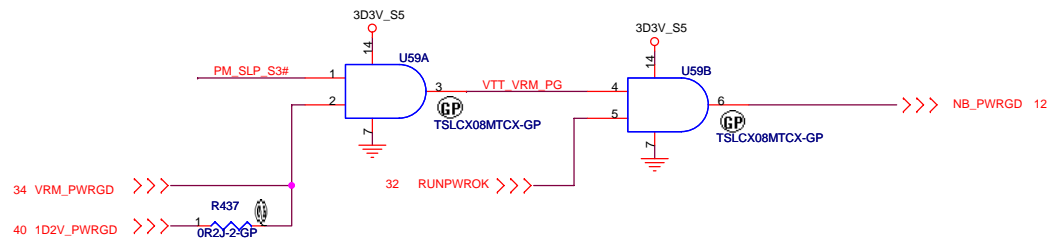
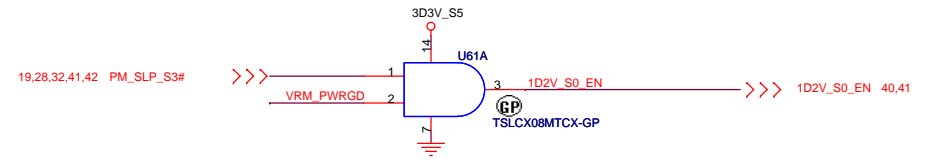
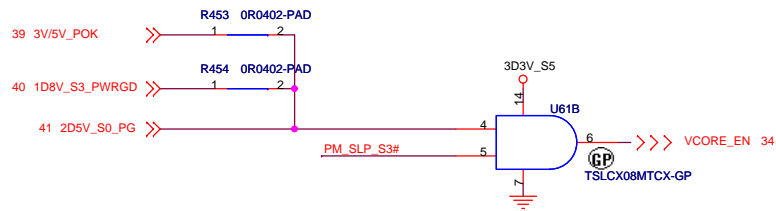
GOLDEN FINGER FOR DEBUG BOARD



Boot Device must have ID[3:0] = 0000
 Has internal pull-down resistors
 All may be left floated
 FPET7 Elec. P3-46

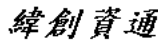


<Core Design>



?U54 CHOOSE CHEAPER
SB_PWRGD IS 35MS
AFTER NB_PWRGD

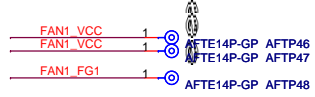
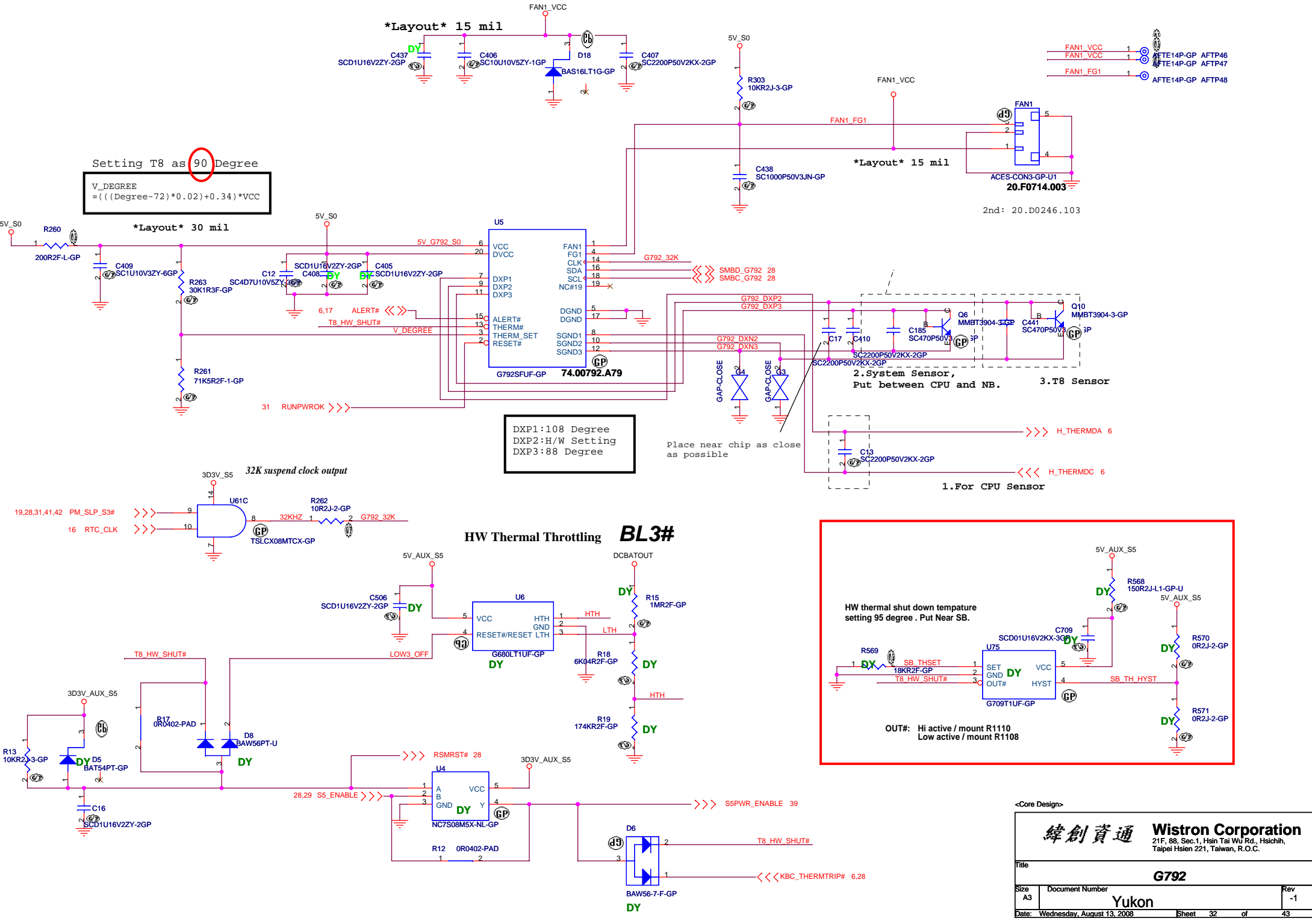
<Core Design>

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
POWERGOOD&ENABLES(1/2)	
Size A3	Document Number Yukon
Date: Wednesday, August 13, 2008	Rev -1
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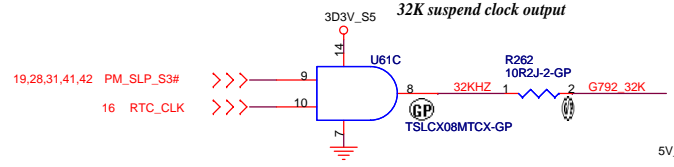
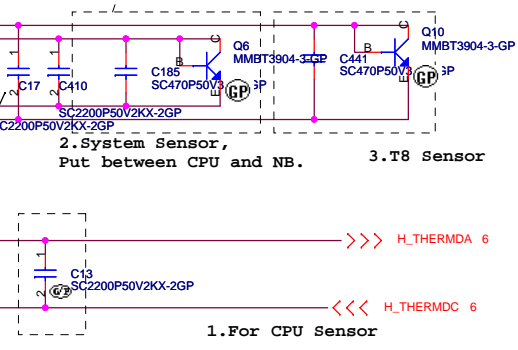
Setting T8 as 90 Degree

$$V_DEGREE = (((Degree - 72) * 0.02) + 0.34) * VCC$$

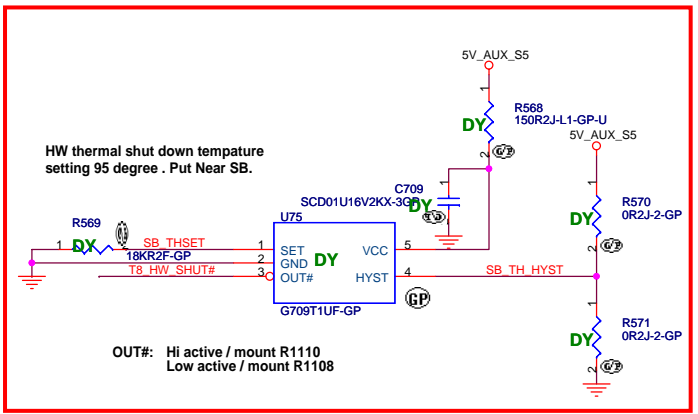
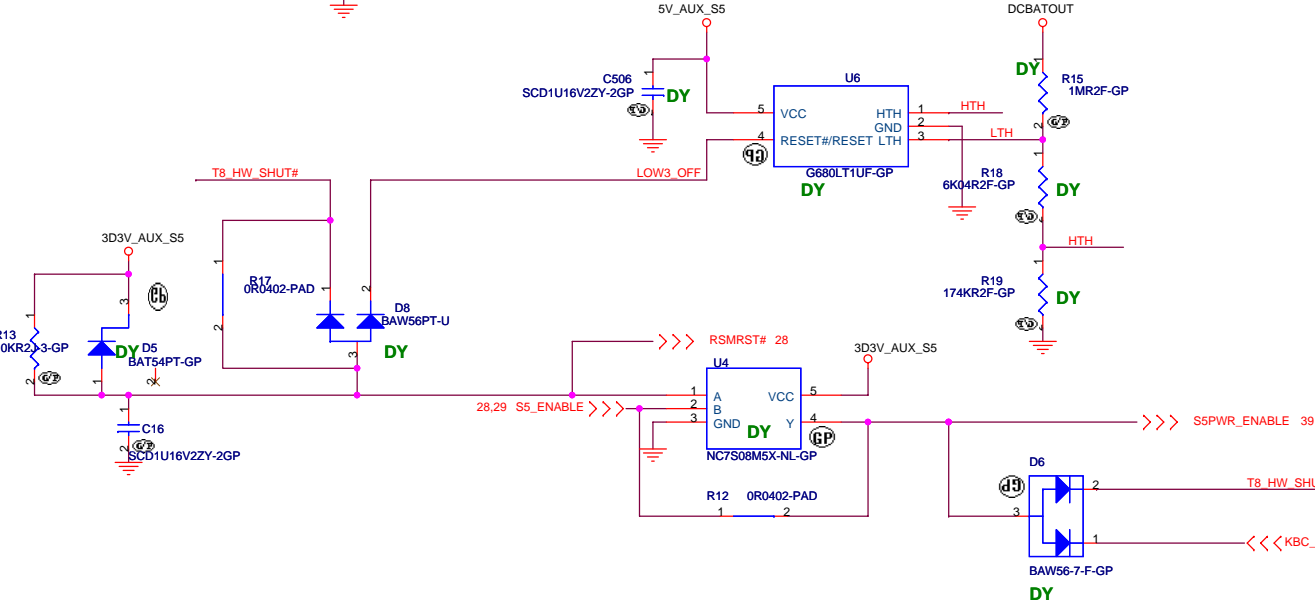
DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree



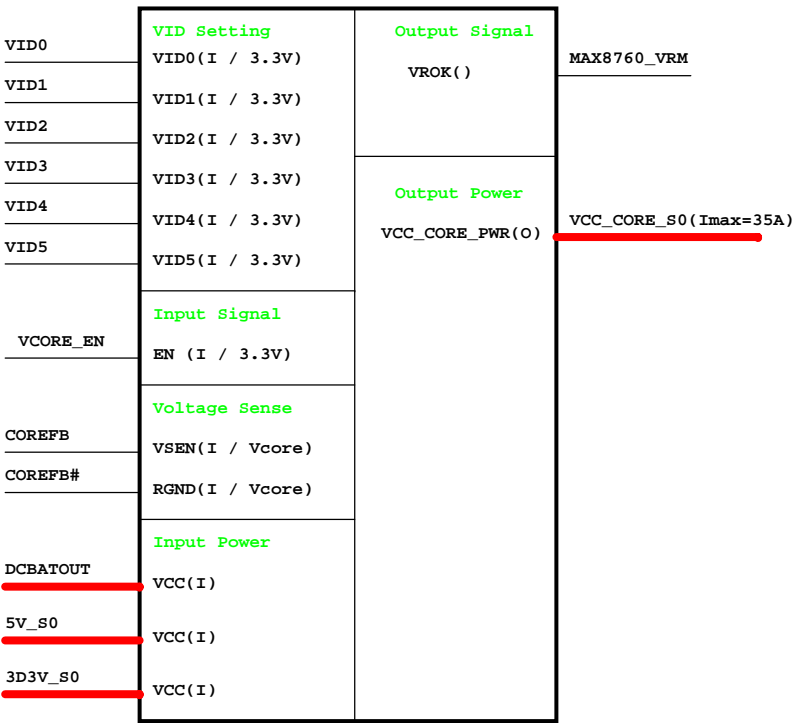
Layout 15 mil
ACES-CON3-GP-U1
20.F0714.003
2nd: 20.D0246.103



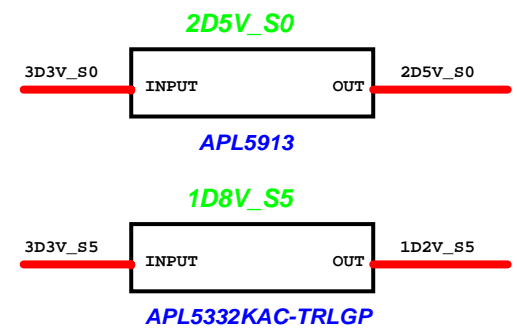
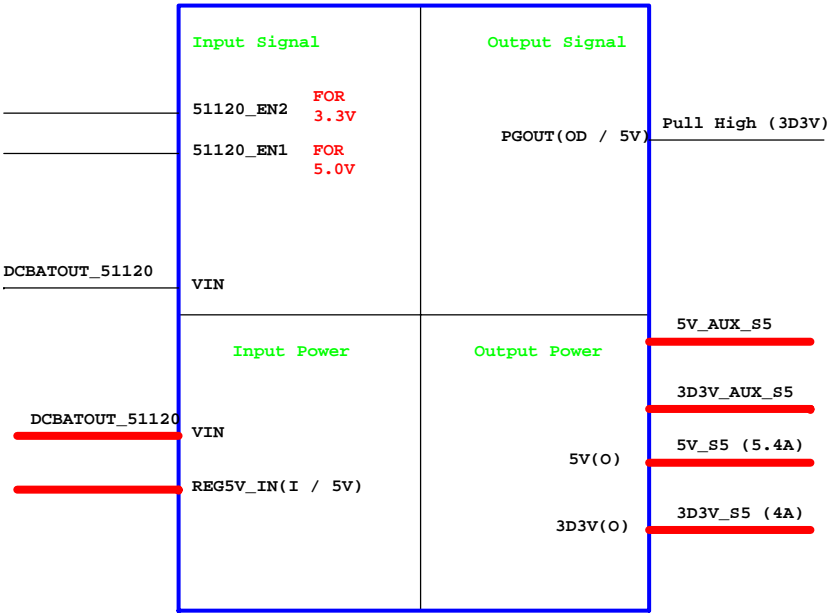
HW Thermal Throttling BL3#



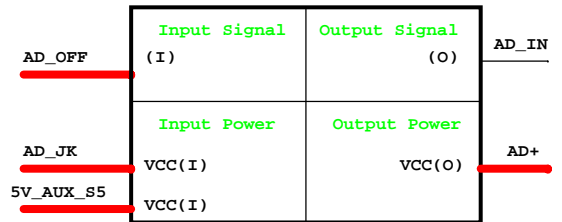
CPU_CORE
ISL6264CRZ



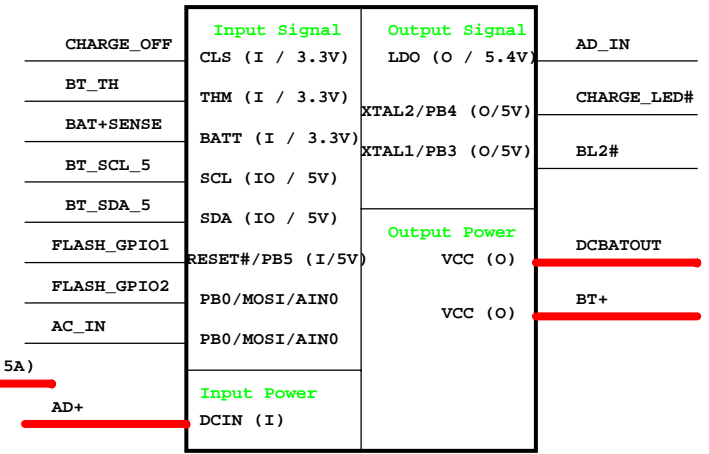
TI TPS51120
3D3V/5V



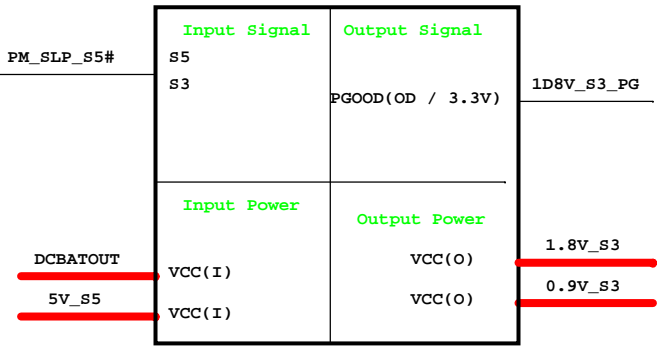
Adapter



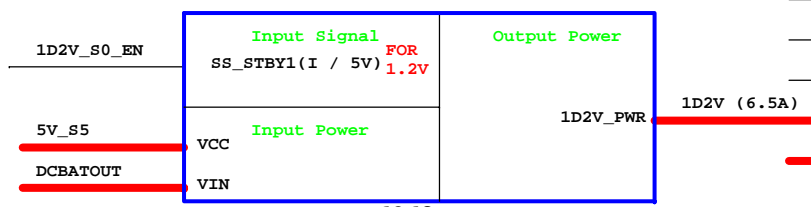
Charger_ISL6255



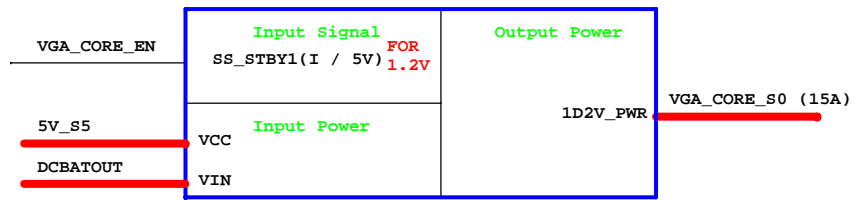
TI TPS51116
1.8V / 0.9V



ISL6268_1D2V



ISL6268_VGA_CORE



<Core Design>

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Title: **Power Block Diagram**

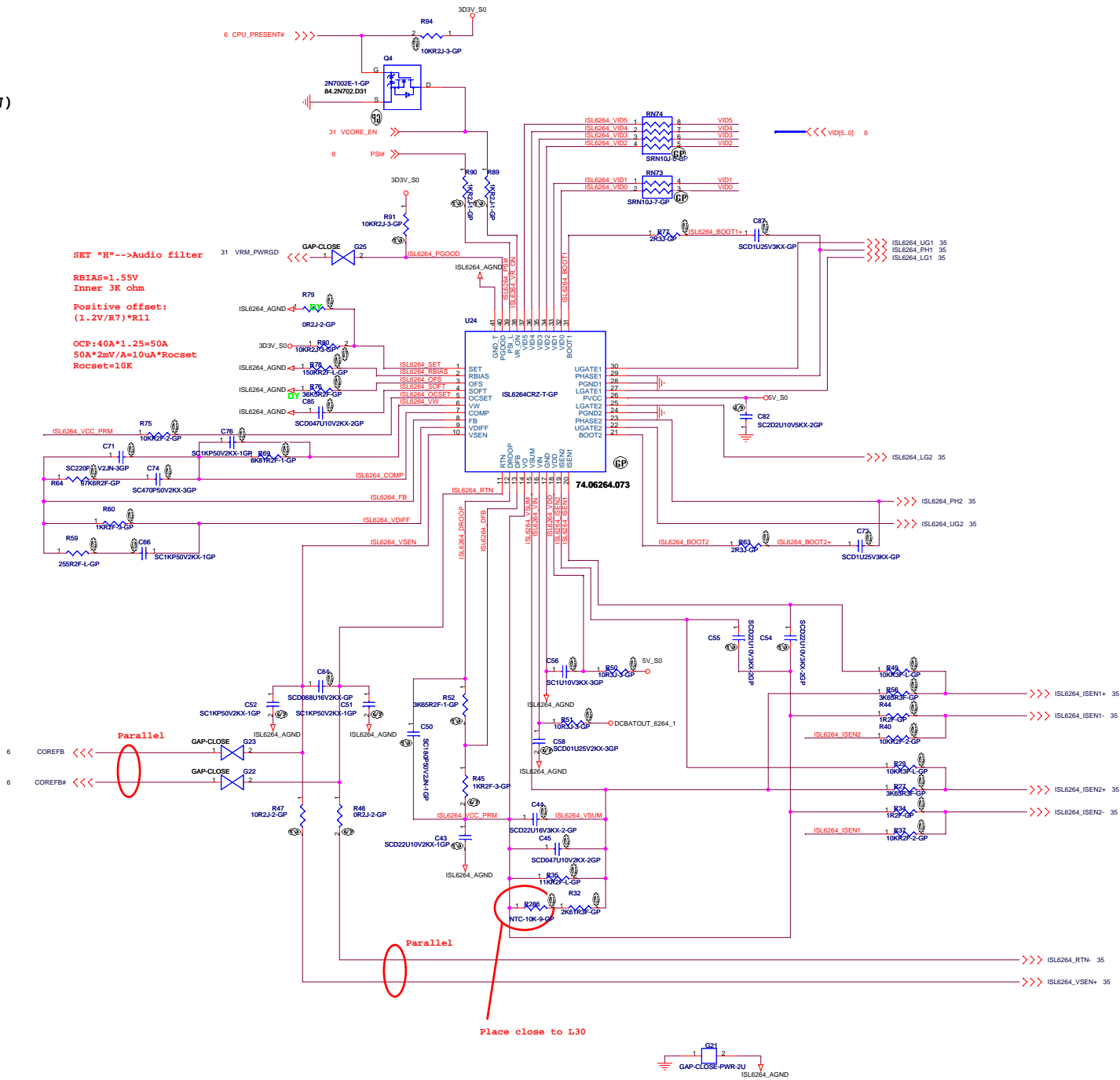
Size: A3 Document Number: **Yukon** Rev: **-1**

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CPU_VCORE
VID=1.20V(25W)/1.15V(35W)
I_{omax}=21A(25W)/35A(35W)
OCP=40A~45A

TABLE 1. VOLTAGE IDENTIFICATION CODES

VID5	VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	0	1.550
0	0	0	0	0	1	1.525
0	0	0	0	0	1	1.500
0	0	0	0	1	1	1.475
0	0	0	1	0	0	1.450
0	0	0	1	0	1	1.425
0	0	0	1	1	0	1.400
0	0	0	1	1	1	1.375
0	0	1	0	0	0	1.350
0	0	1	0	0	1	1.325
0	0	1	0	1	0	1.300
0	0	1	0	1	1	1.275
0	0	1	1	0	0	1.250
0	0	1	1	0	1	1.225
0	0	1	1	1	0	1.200
0	1	0	0	0	0	1.175
0	1	0	0	0	1	1.150
0	1	0	0	1	0	1.125
0	1	0	0	1	1	1.100
0	1	0	1	0	0	1.075
0	1	0	1	0	1	1.050
0	1	0	1	1	0	1.025
0	1	0	1	1	1	1.000
0	1	1	0	0	0	0.975
0	1	1	0	0	1	0.950
0	1	1	0	1	0	0.925
0	1	1	0	1	1	0.900
0	1	1	1	0	0	0.875
0	1	1	1	0	1	0.850
0	1	1	1	1	0	0.825
0	1	1	1	1	1	0.800
1	0	0	0	0	0	0.775
1	0	0	0	0	1	0.750
1	0	0	0	1	0	0.725
1	0	0	0	1	1	0.700
1	0	0	1	0	0	0.675
1	0	0	1	0	1	0.650
1	0	0	1	1	0	0.625
1	0	0	1	1	1	0.600
1	1	0	0	0	0	0.575
1	1	0	0	0	1	0.550
1	1	0	0	1	0	0.525
1	1	0	0	1	1	0.500
1	1	1	0	0	0	0.475
1	1	1	0	0	1	0.450
1	1	1	0	1	0	0.425
1	1	1	0	1	1	0.400
1	1	1	1	0	0	0.375
1	1	1	1	0	1	0.350
1	1	1	1	1	0	0.325
1	1	1	1	1	1	0.300



SET "H"--->Audio filter
 RBIAS=1.55V
 Inner 3K ohm
 Positive offset:
 (1.2V/R7)*R11
 OCP:40A*1.25=50A
 50A*2mV/A=10uA*Rocset
 Rocset=10K

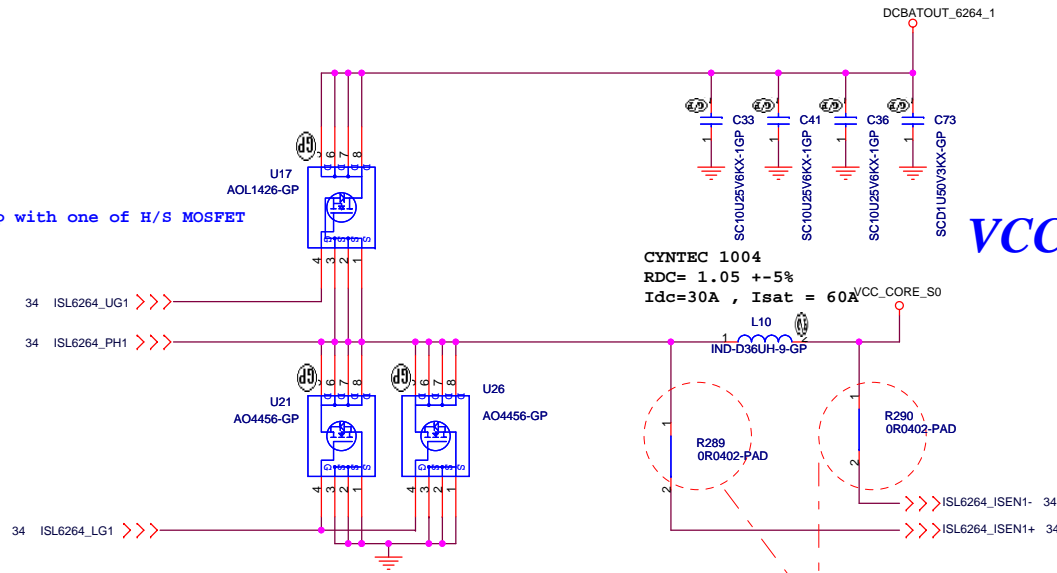
Parallel

Parallel

Place close to L30



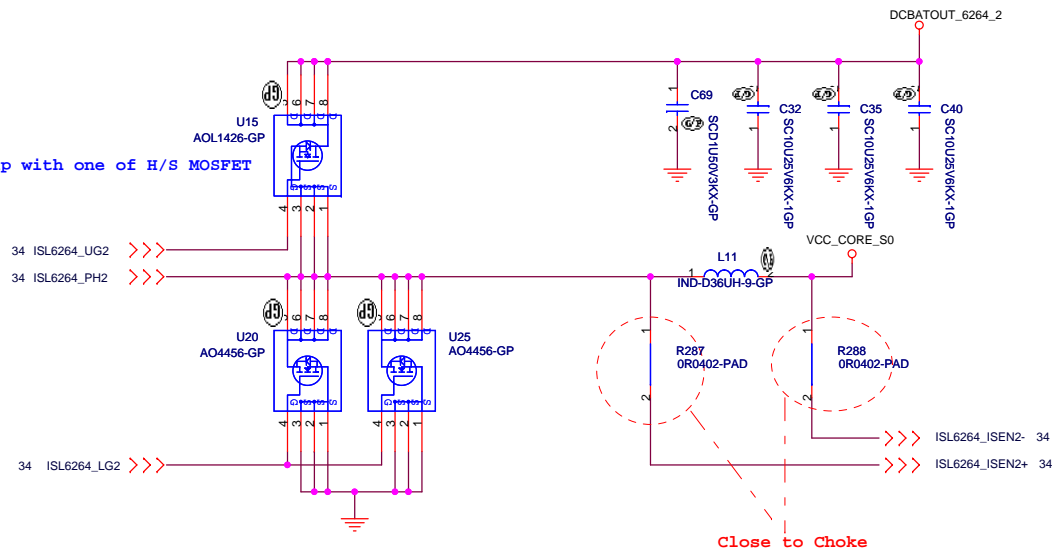
Overlap with one of H/S MOSFET



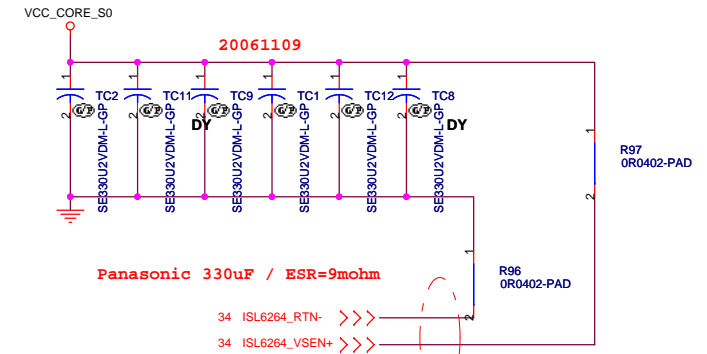
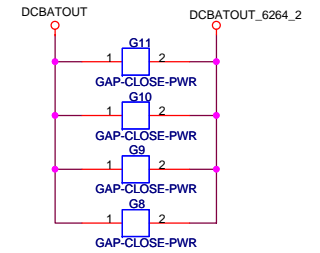
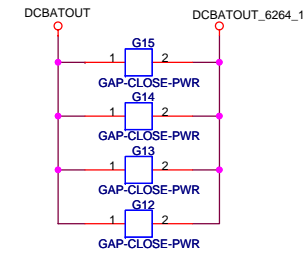
VCC_CORE_S0

Close to Choke

Overlap with one of H/S MOSFET



Close to Choke



Parallel

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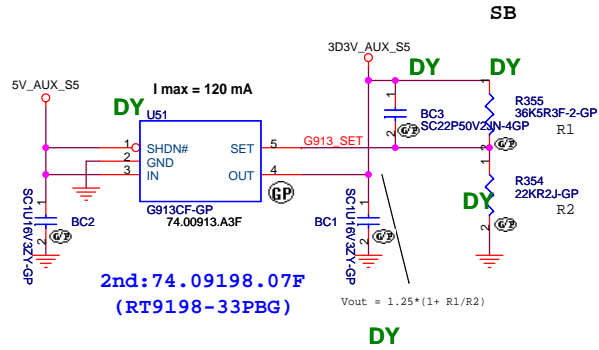
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Yukon

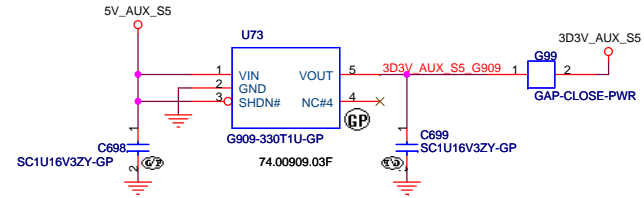
Aux Power

3D3V_AUX_S5



Aux Power

3D3V_AUX_S5



<Core Design>

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

3D3V AUX

Size

A3

Document Number

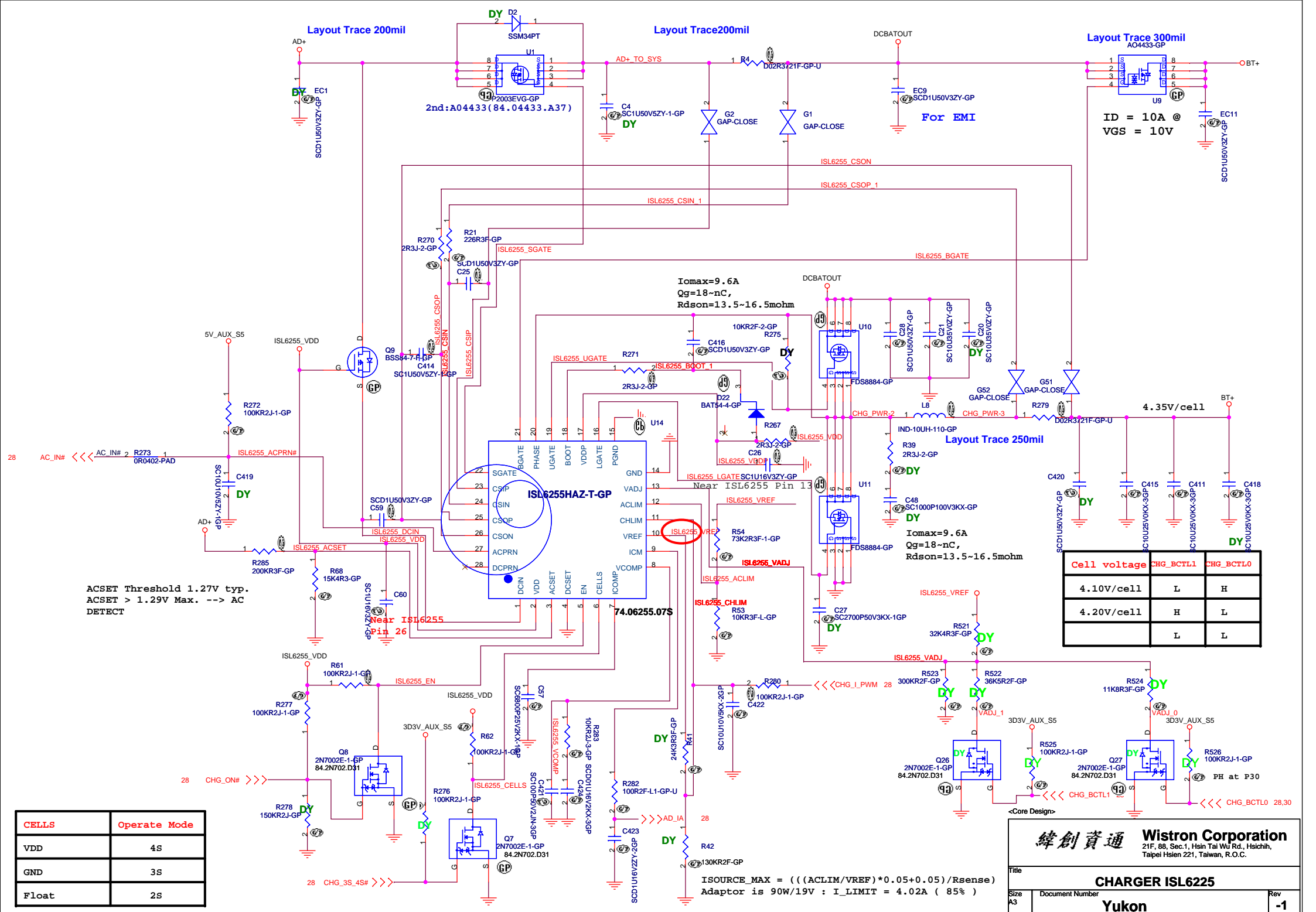
Yukon

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-1

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Layout Trace 200mil

Layout Trace 200mil

Layout Trace 300mil

For EMI

ID = 10A @
VGS = 10V

I_{omax}=9.6A
Q_g=18-nC,
R_{dson}=13.5~16.5mohm

I_{omax}=9.6A
Q_g=18-nC,
R_{dson}=13.5~16.5mohm

ACSET Threshold 1.27V typ.
ACSET > 1.29V Max. --- AC
DETECT

Cell voltage	CHG_BCTL1	CHG_BCTL0
4.10V/cell	L	H
4.20V/cell	H	L
	L	L

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

ISOURCE_MAX = ((ACLIM/VREF)*0.05+0.05)/Rsense)
Adaptor is 90W/19V : I_LIMIT = 4.02A (85%)

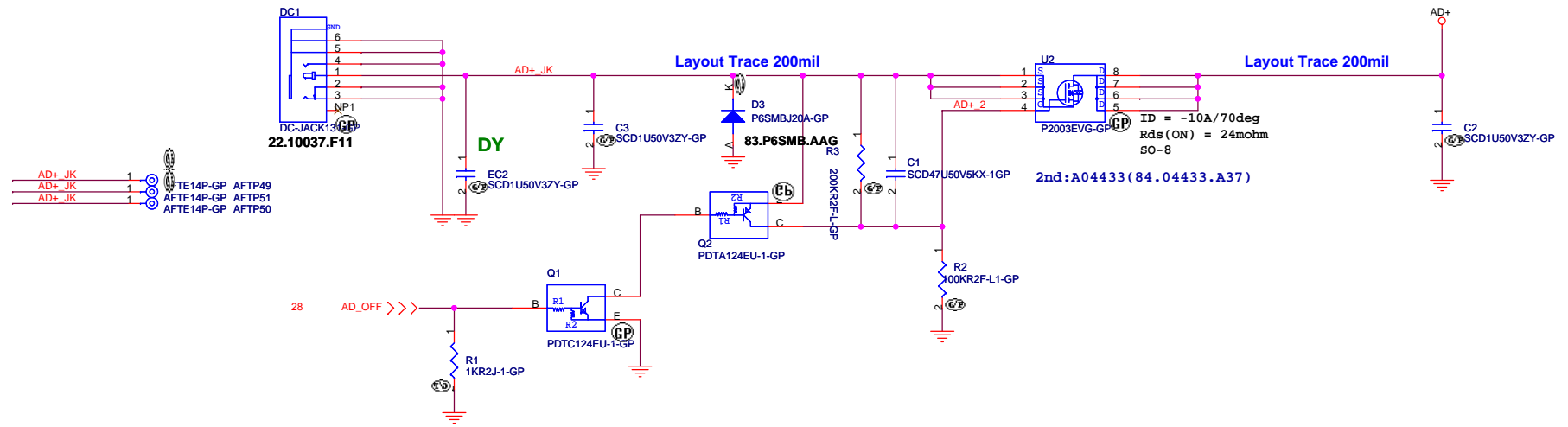
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **CHARGER ISL6255**

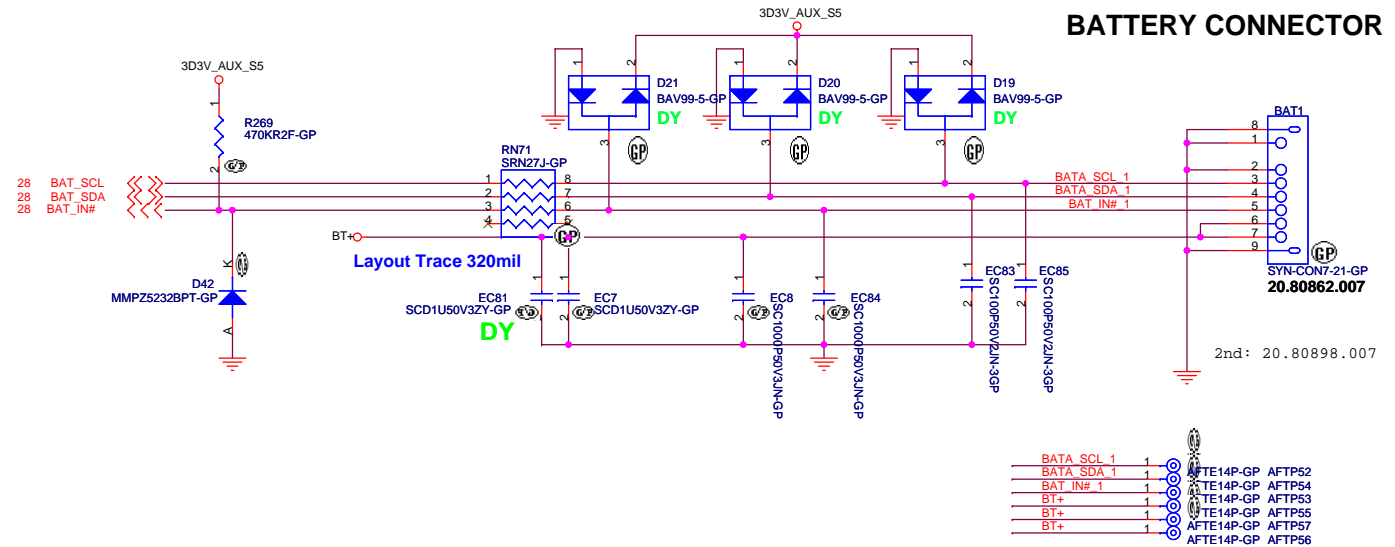
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Adaptor in to generate DCBATOUT

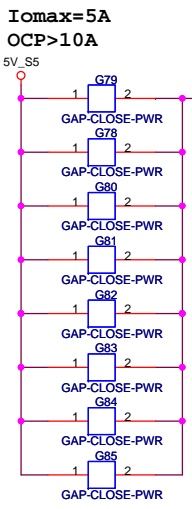
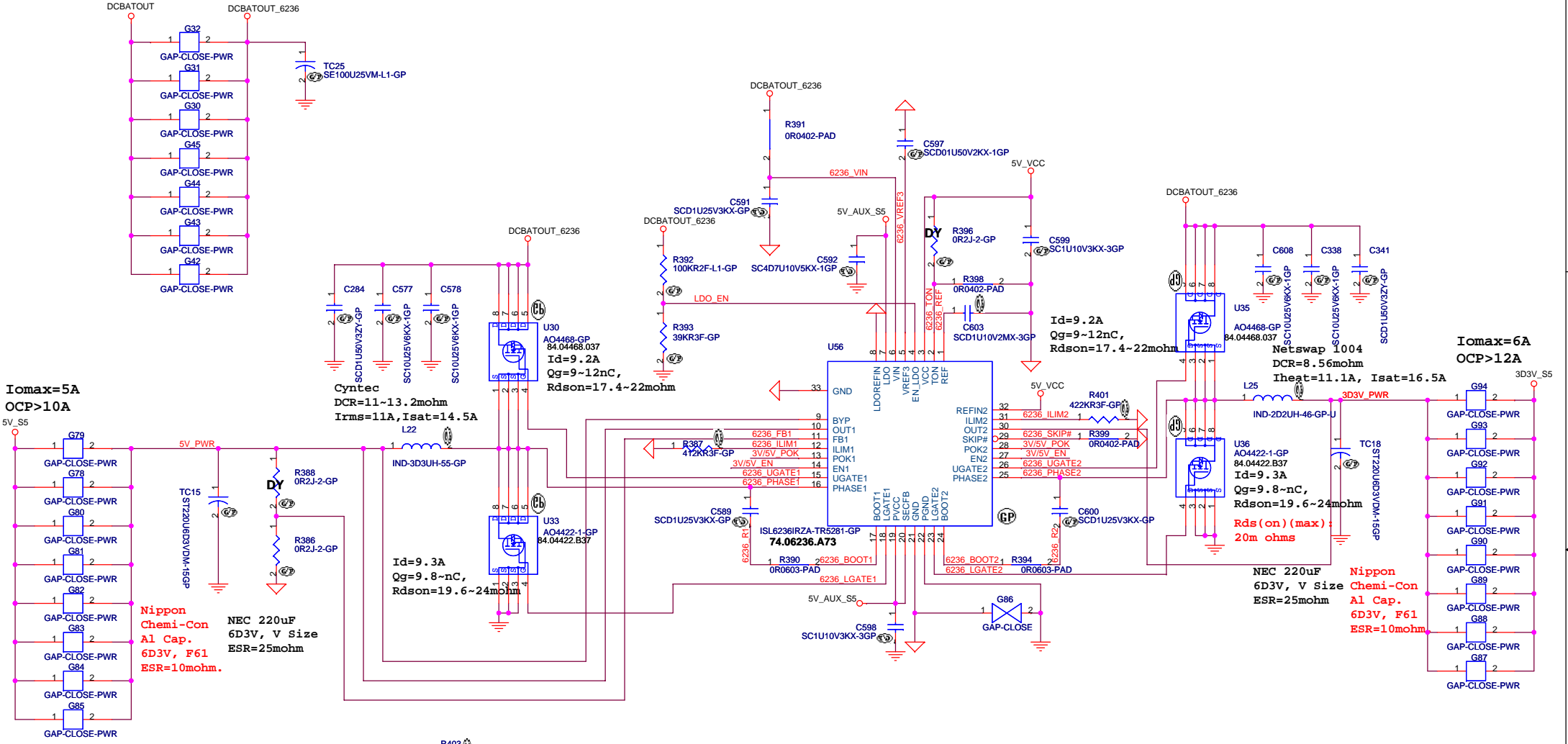


BATTERY CONNECTOR



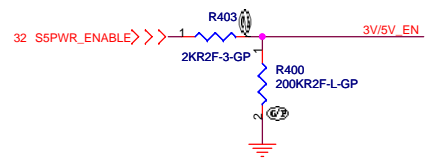
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AD/BATT CONN	
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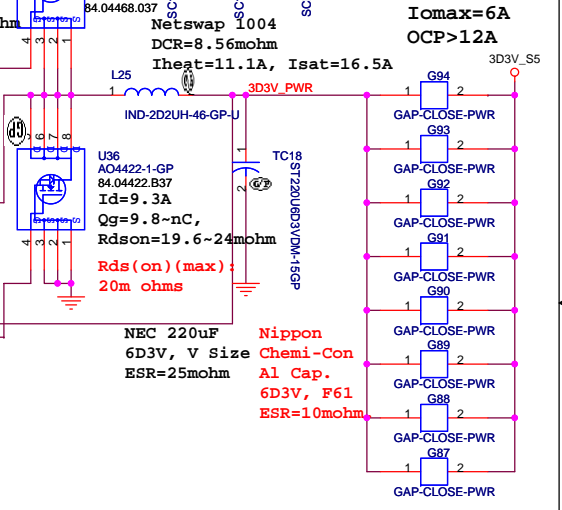


Iomax=5A
OCP>10A
 5V_S5

Maximum current:5A
 If LIR=0.35
 $\Delta I = 5 \times 0.35 = 1.75A$
 $V_{in} = 20V; F_{sw} = 400K$
 $L \sim 3.3\mu H$
OCP: 5x2=10A
 $I_{ocp} = 10 - (1.75/2) \sim 9.125A$
 $V_{th} = 9.125A \times 24m\Omega = 219mV$
 $R(I_{lim}) = (219mV \times 10) / 5uA$
 $\sim 438K \rightarrow 442K$

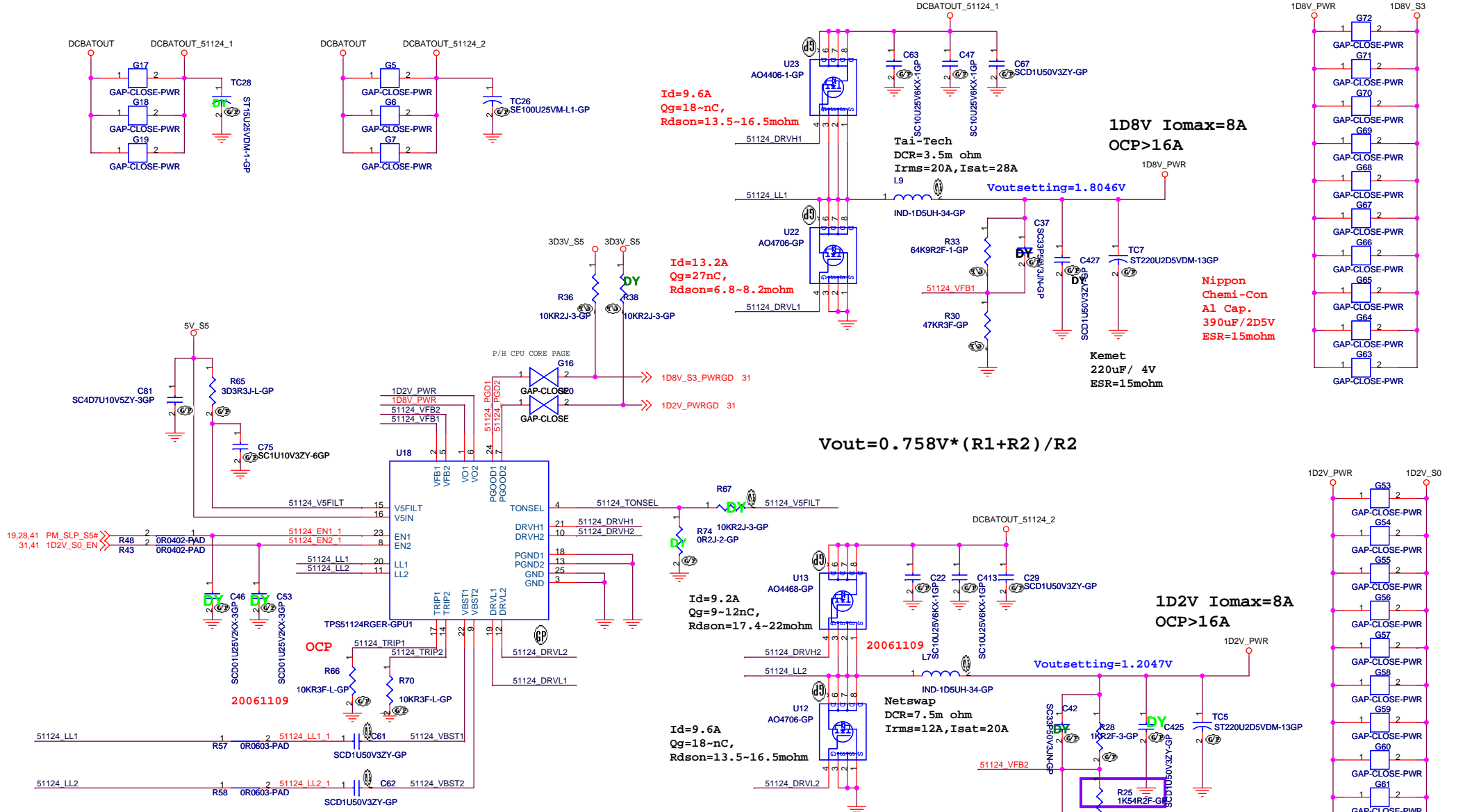


32 S5PWR_ENABLE >>> 3V/5V_EN



Iomax=6A
OCP>12A
 3D3V_S5

Maximum current:5A
 If LIR=0.35
 $\Delta I = 5 \times 0.35 = 1.75A$
 $V_{in} = 20V; F_{sw} = 500K$
 $L \sim 2.2\mu H$
OCP: 5x2=10A
 $I_{ocp} = 10 - (1.75/2) \sim 9.125A$
 $V_{th} = 9.125A \times 24m\Omega = 219mV$
 $R(I_{lim}) = (219mV \times 10) / 5uA$
 $\sim 438K \rightarrow 442K$



$V_{trip}(mV) = R_{trip}(Kohm) * 10(uA)$
 $I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2*L*f)) * ((V_{in}-V_{out}) * V_{out}) / V_{in})$

	GND	OPEN	V5FILT
TONSEL	230k/CH1 283k/CH2	283k/CH1 346k/CH2	346k/CH1 423k/CH2

STRP_DATA	1D2V(VCC_NB)
0	1.0
1	1.2

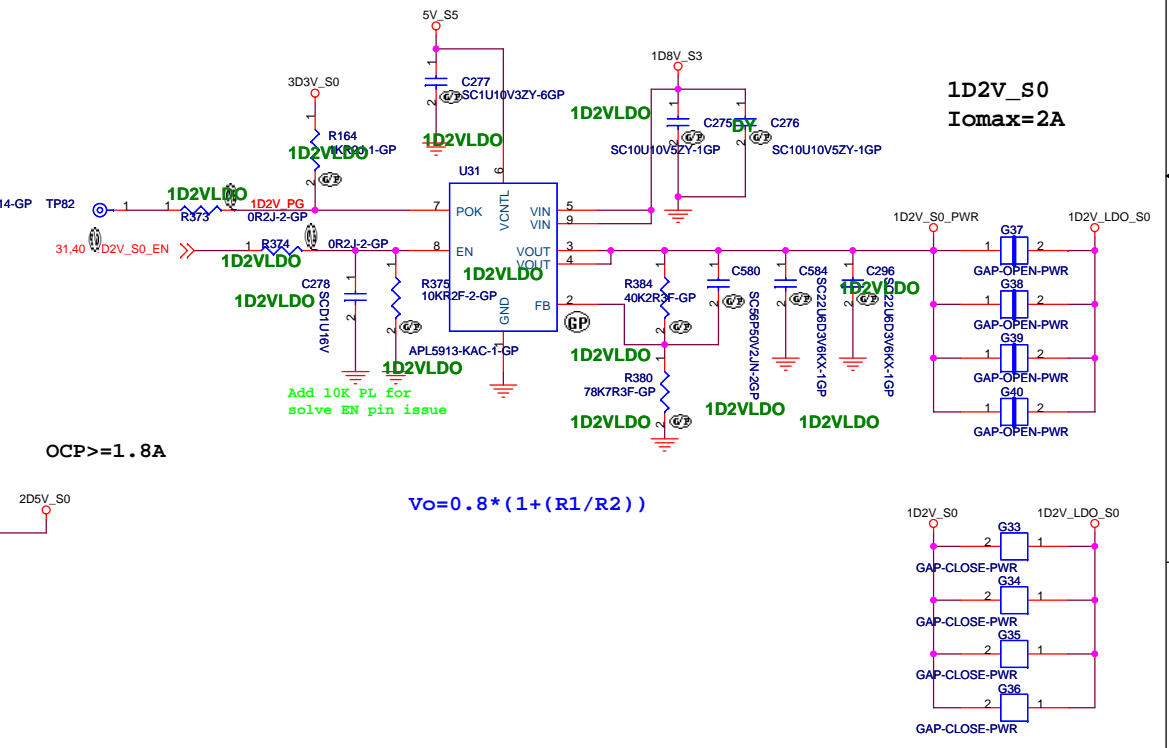
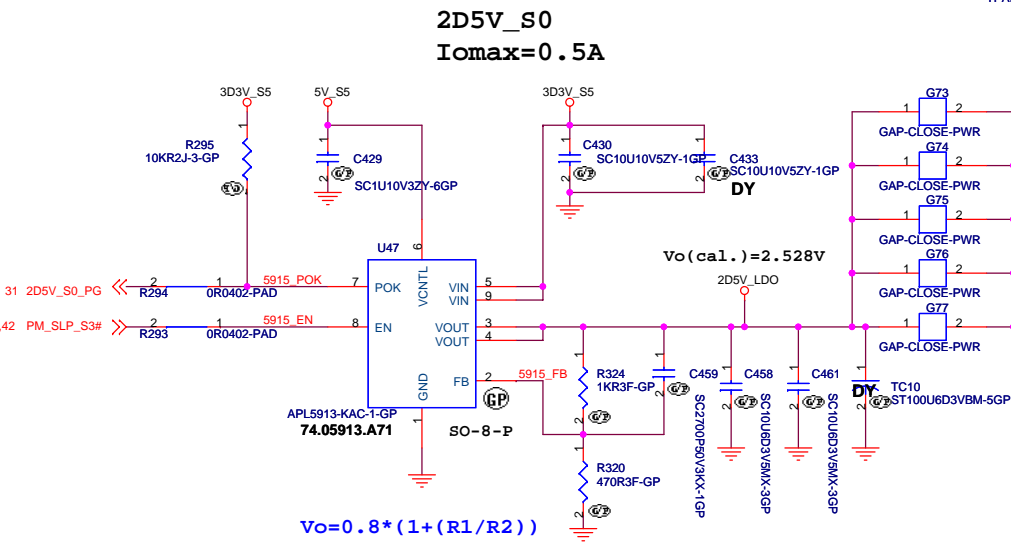
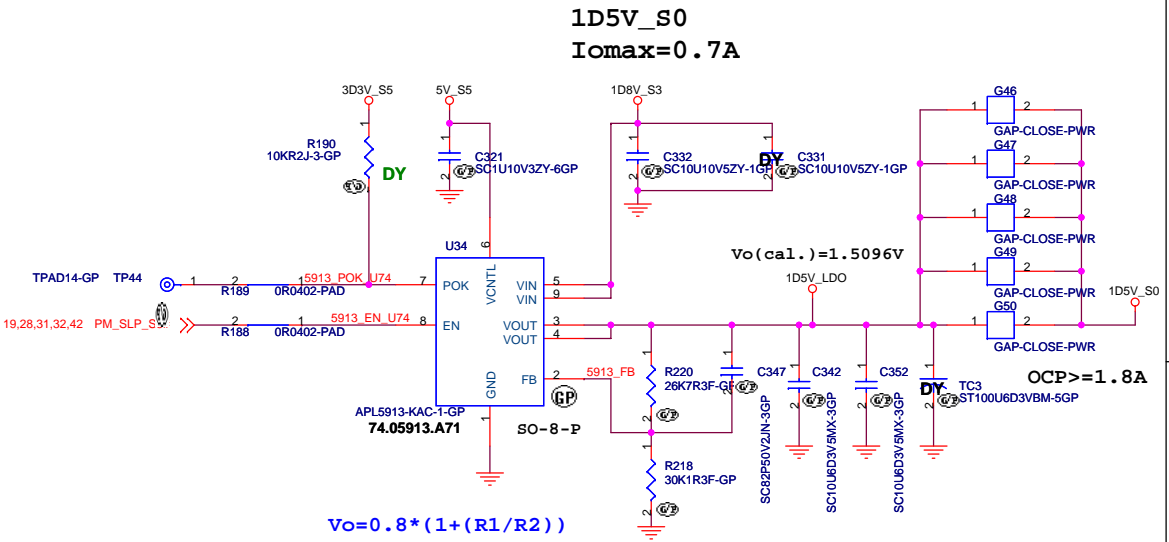
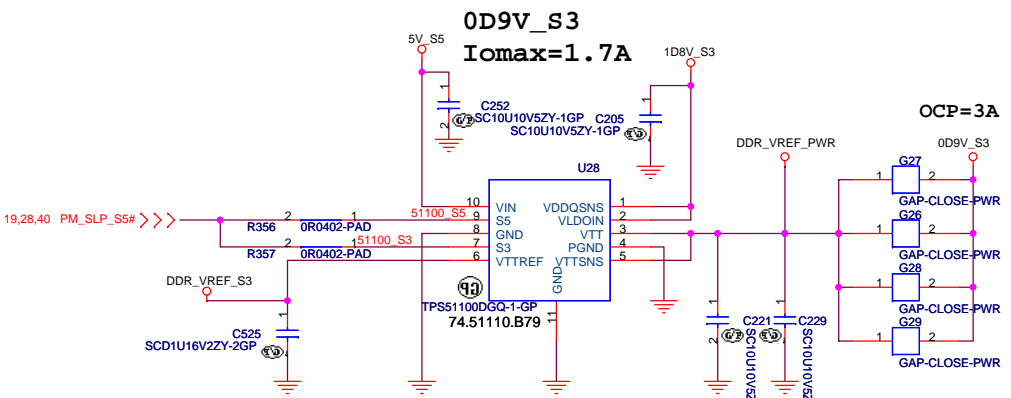
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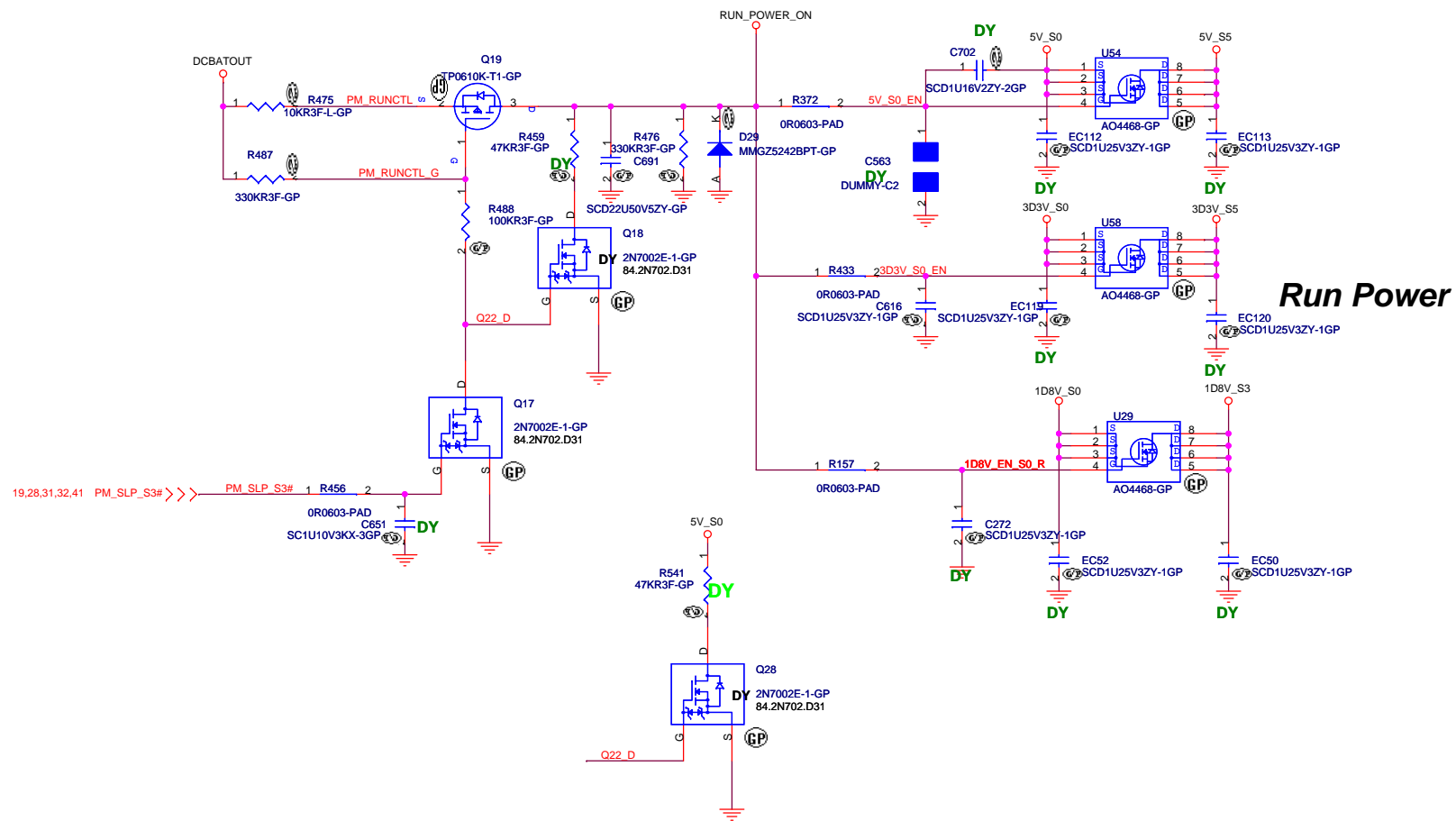
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Title: **TPS51124 1D8V 1D2V**

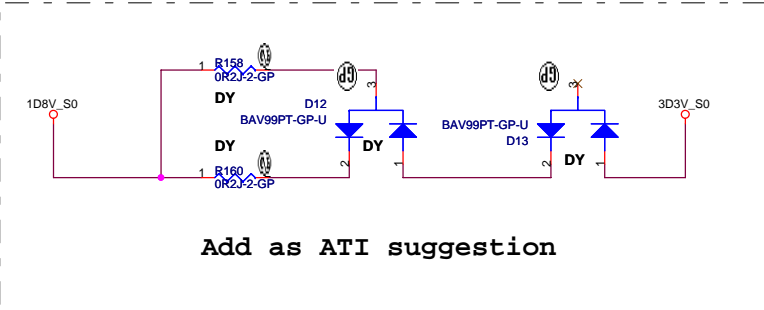
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Run Power

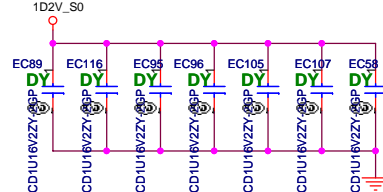
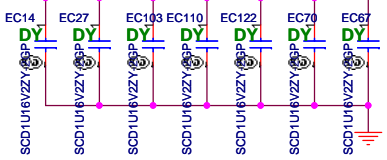
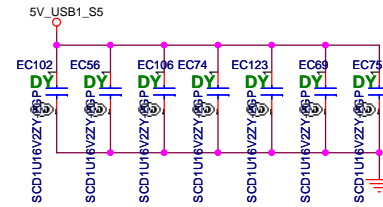
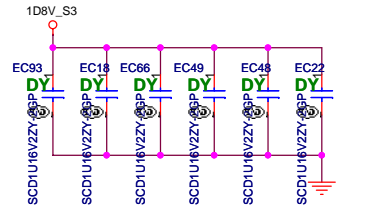
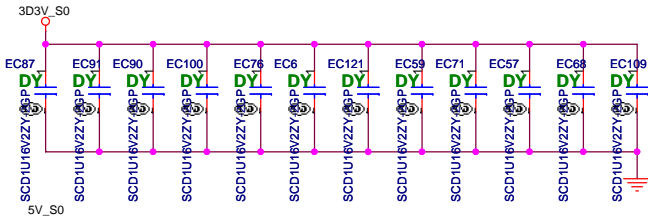
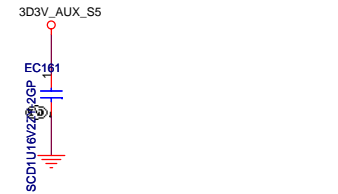
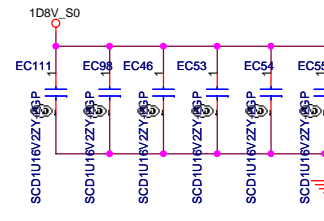
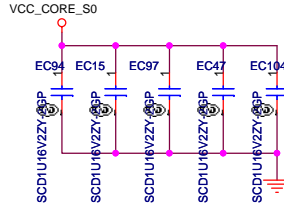
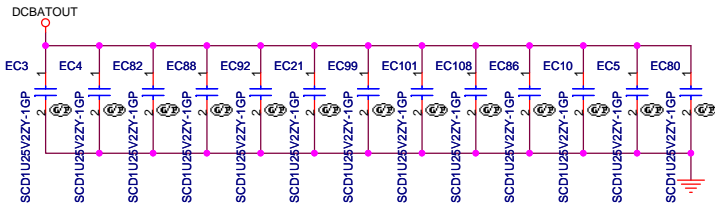
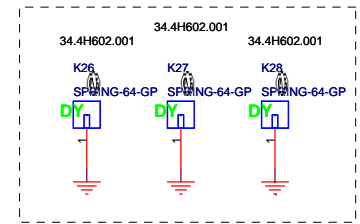
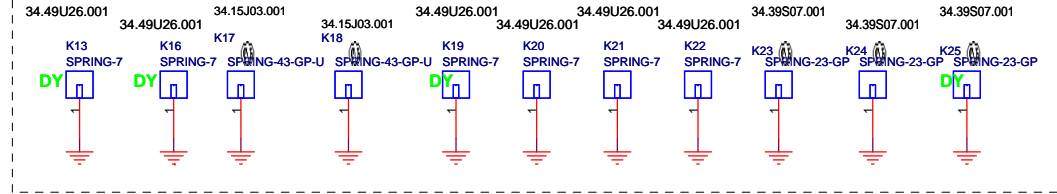
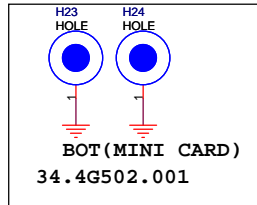
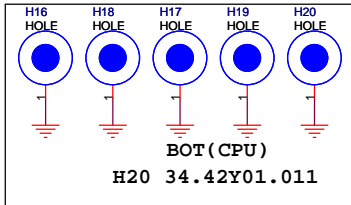
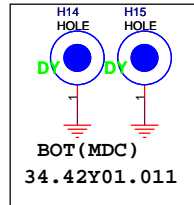
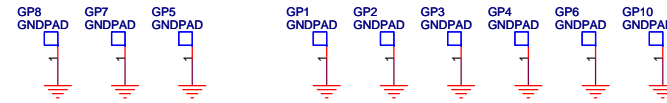
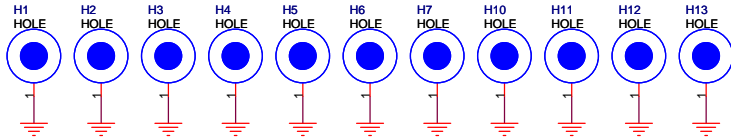
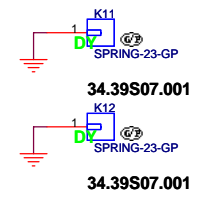
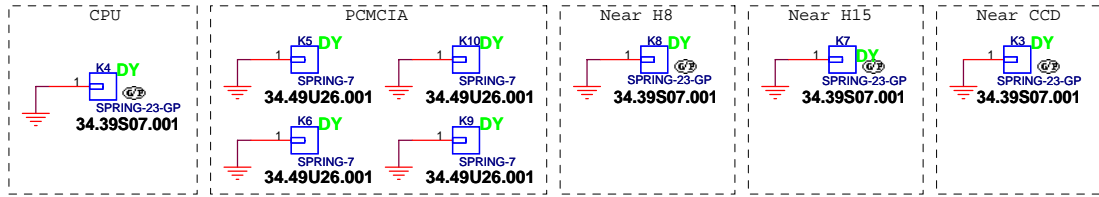
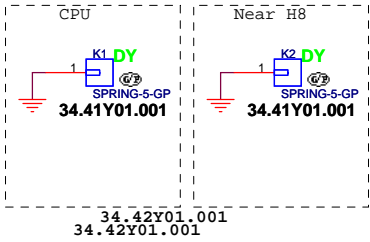
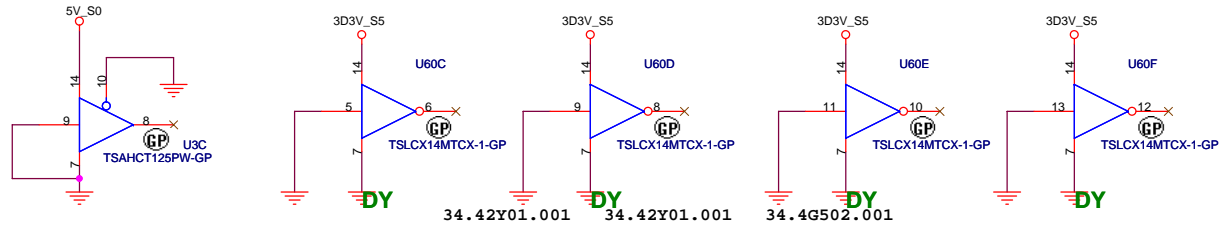
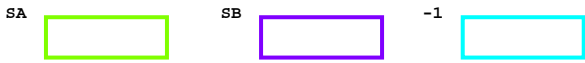


Add as ATI suggestion

Power On Logic

<Core Design>

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Title: RUB POWER		
Size: A3	Document Number: Yukon	Rev: -1
Date: Wednesday, August 06, 2008	Sheet: 42	of: 43



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Title: **EMI/Spring/Boss**

Size: Document Number: **Yukon** Rev: -1

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