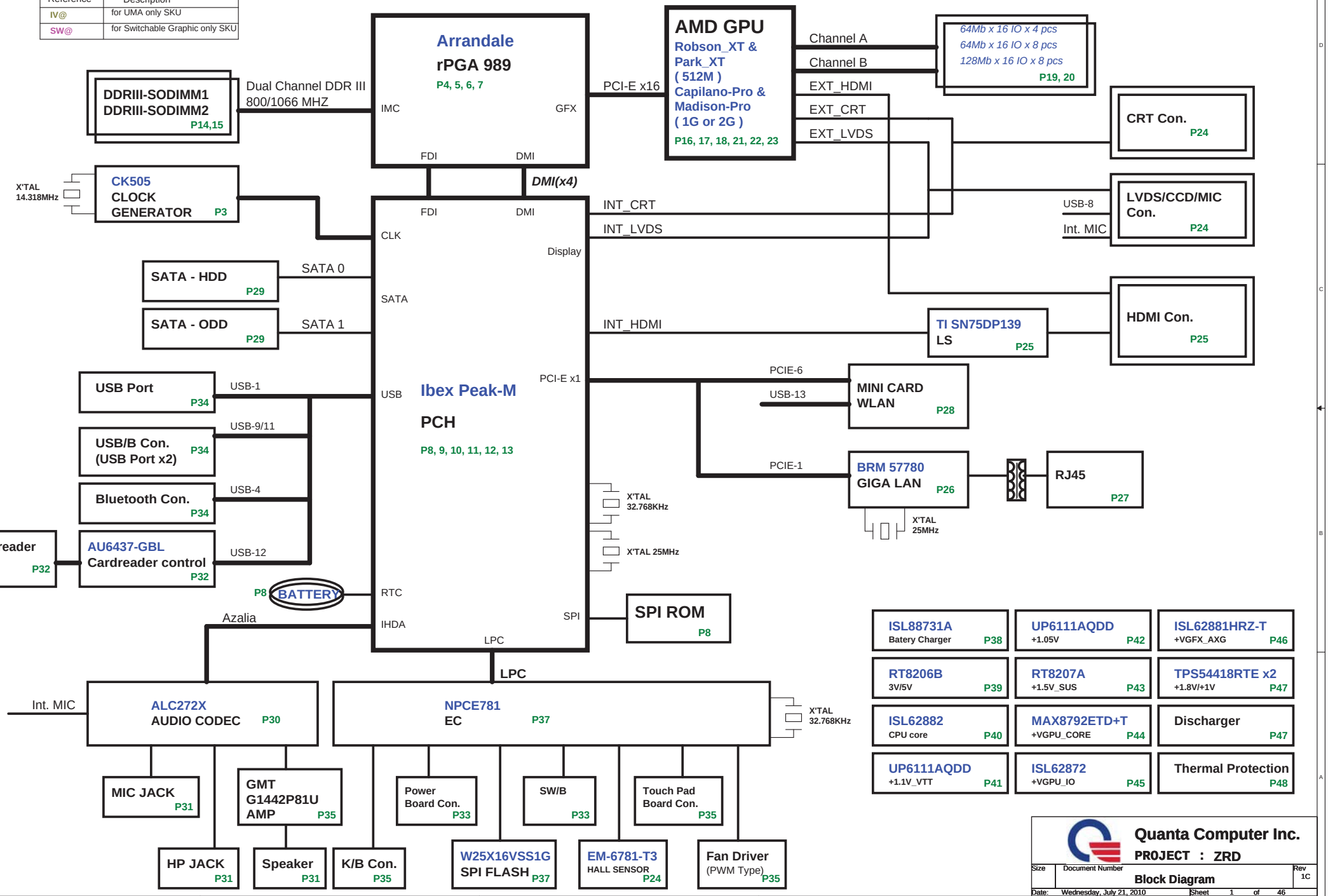
HM55_CP (ZRD) SYSTEM BLOCK DIAGRAM

BOM Option Table

Reference	Description
IV@	for UMA only SKU
SW@	for Switchable Graphic only SKU

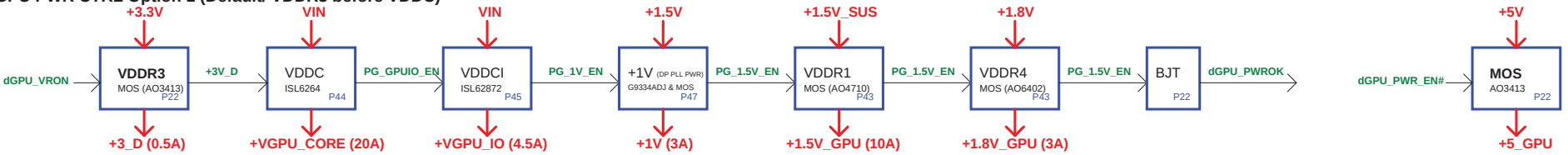


Quanta Computer Inc.
PROJECT : ZRD

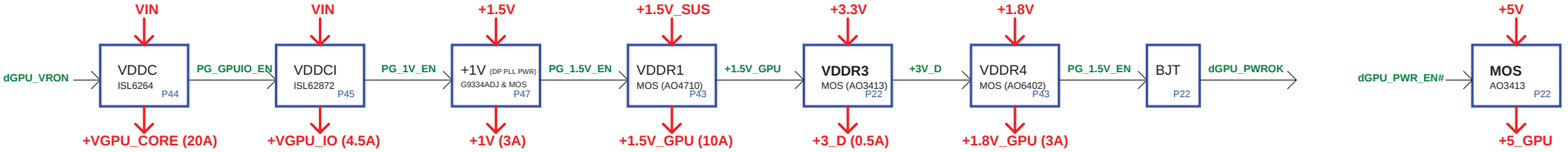
Size	Document Number	Rev
	Block Diagram	1C

Date: Wednesday, July 21, 2010 Sheet 1 of 46

GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



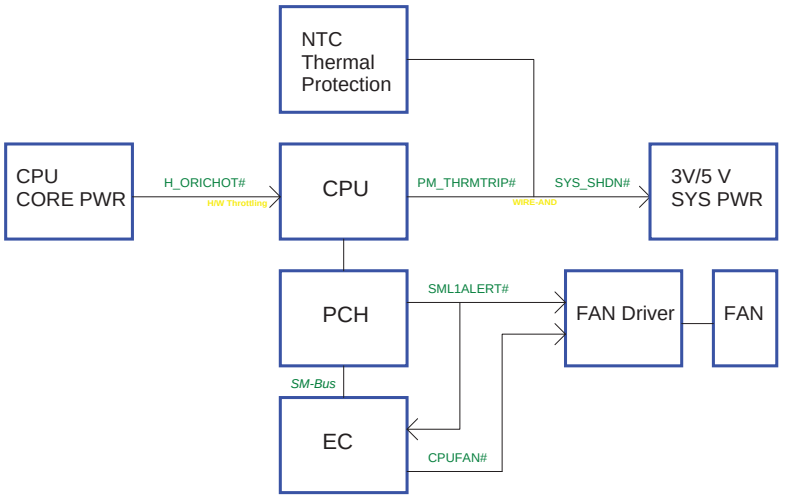
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

Thermal Follow Chart



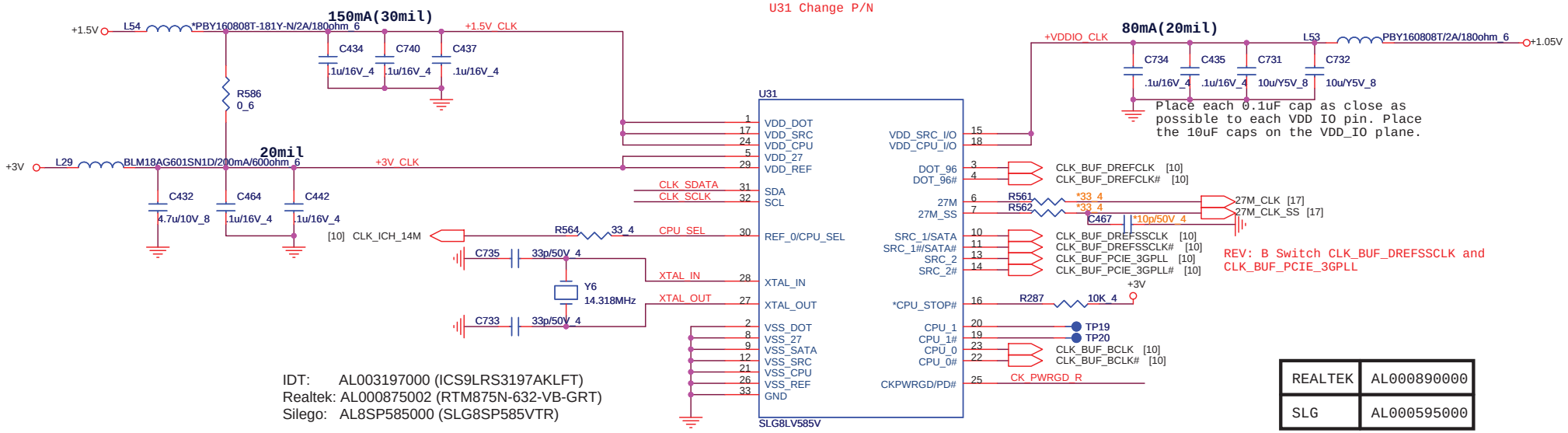
Quanta Computer Inc.

PROJECT : ZRD

Size	Document Number	Rev
	PWR Status & GPU PWR CRL & THRM	1C

Date: Wednesday, July 21, 2010 Sheet 2 of 46

6/21 add R586 for 3V CLK gen
Un-stuff L54
U31 Change P/N

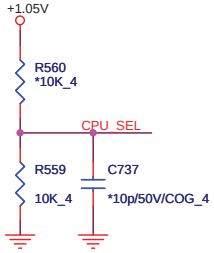


REV: B Switch CLK_BUF_DREFSSCLK and CLK_BUF_PCIE_3GPLL

IDT: AL003197000 (ICS9LRS3197AKLFT)
Realtek: AL000875002 (RTM875N-632-VB-GRT)
Silego: AL8SP585000 (SLG8SP585VTR)

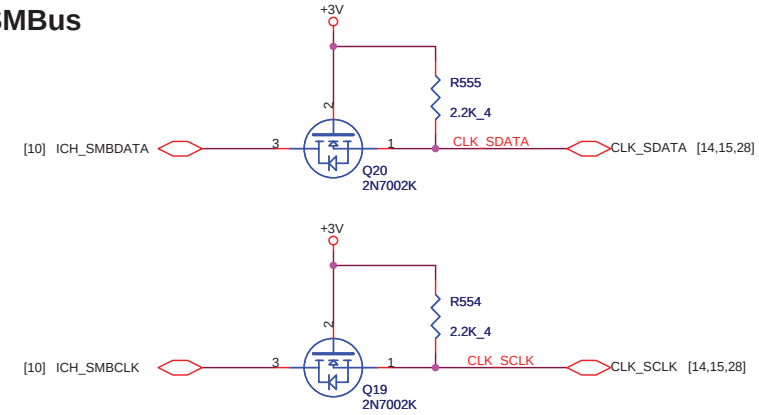
REALTEK	AL000890000
SLG	AL000595000

CPU_CLK select

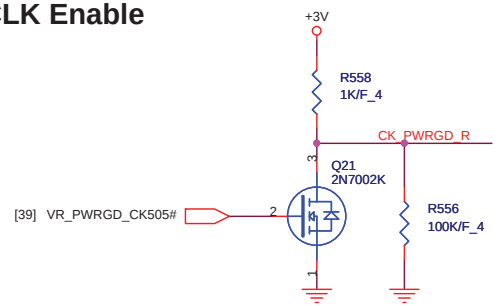


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus



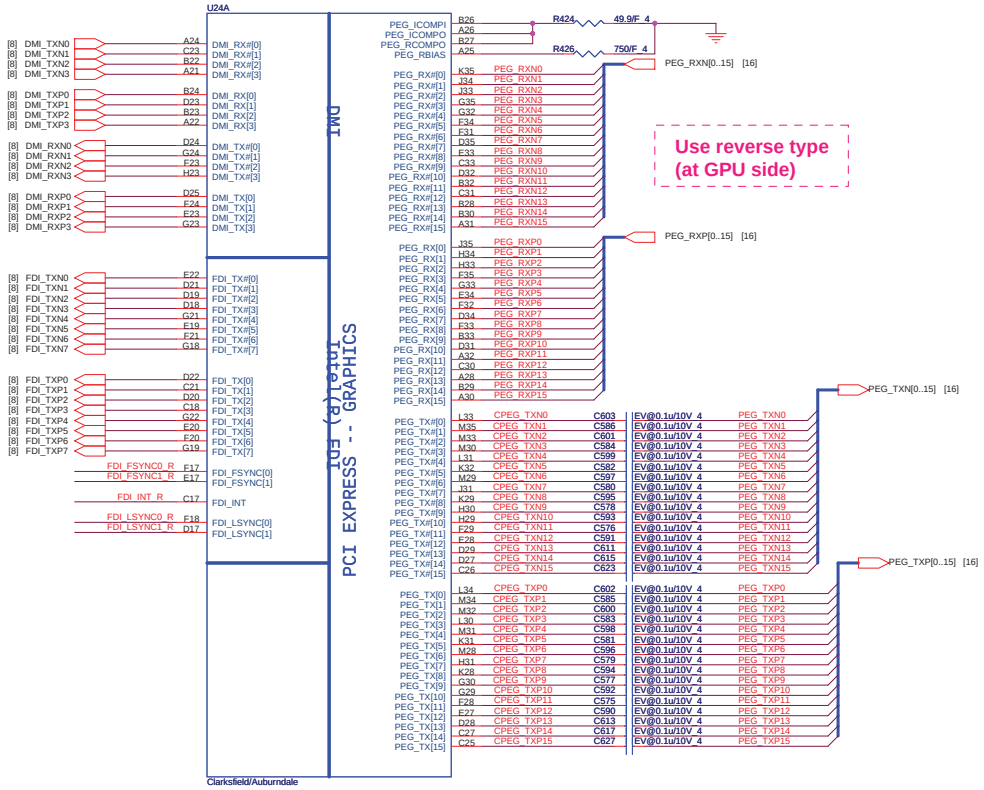
CLK Enable



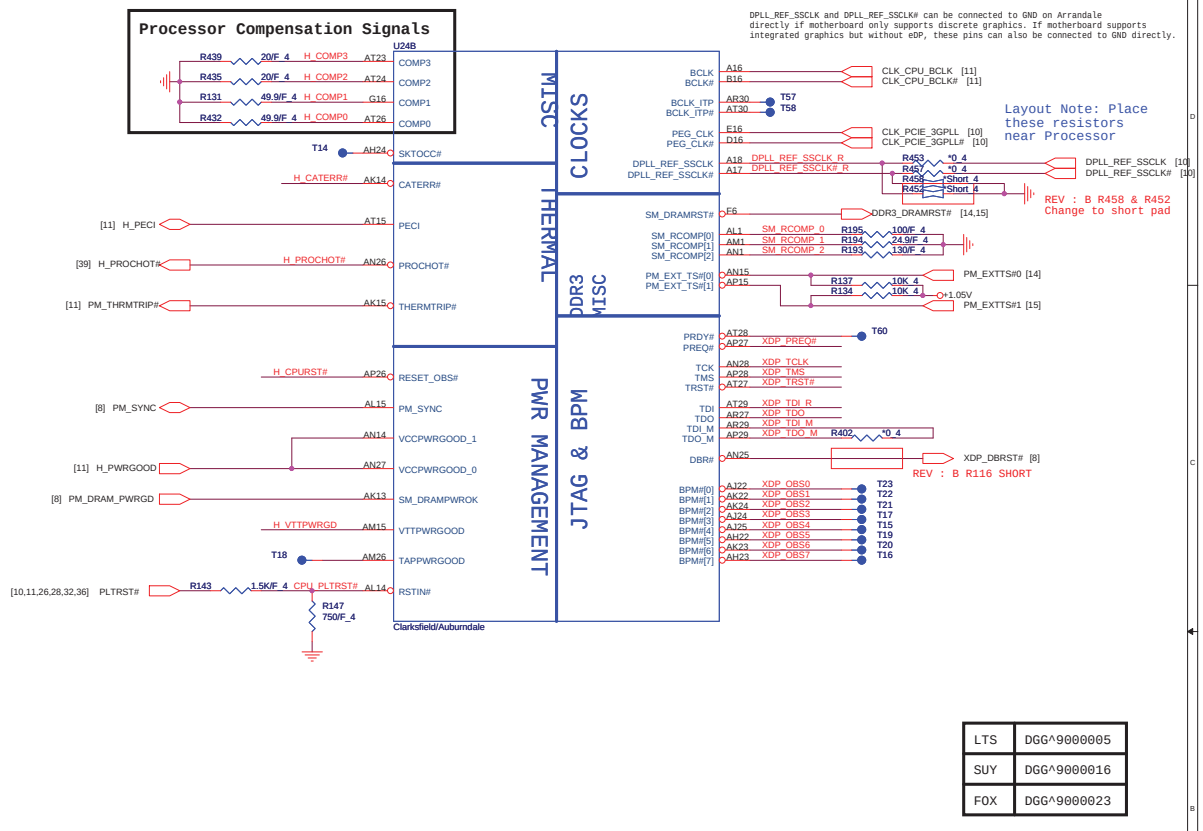
Quanta Computer Inc.
PROJECT : ZRD

Size	Document Number	Rev
	Clock Generator	1C
Date: Wednesday, July 21, 2010	Sheet 3 of 46	

AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)



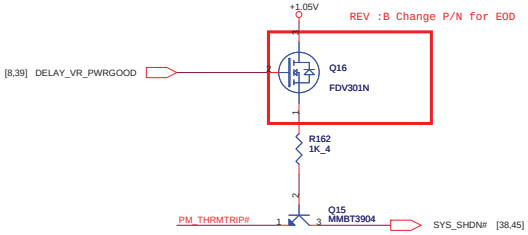
AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)



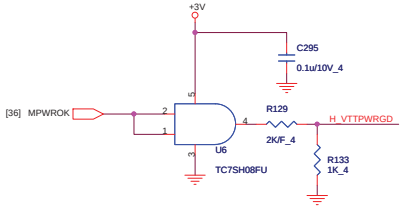
DPLL_REF_SSCLK and DPLL_REF_SSCLK# can be connected to GND on Arrandale directly if motherboard only supports discrete graphics. If motherboard supports integrated graphics but without eDP, these pins can also be connected to GND directly.

LTS	DGG^9000005
SUY	DGG^9000016
FOX	DGG^9000023

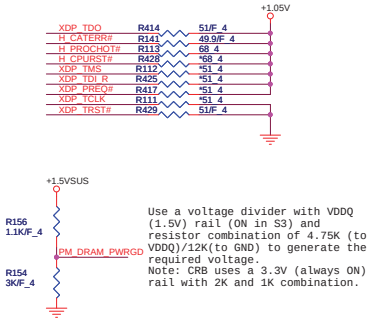
Thermaltrip protect



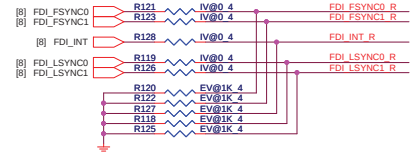
VTT PWR_Good



Processor pull-up



Use a voltage divider with VDDQ (1.5V) rail (ON in S3) and resistor combination of 4.75K (to VDDQ)/12K(to GND) to generate the required voltage.
Note: CRB uses a 3.3V (always ON) rail with 2K and 1K combination.



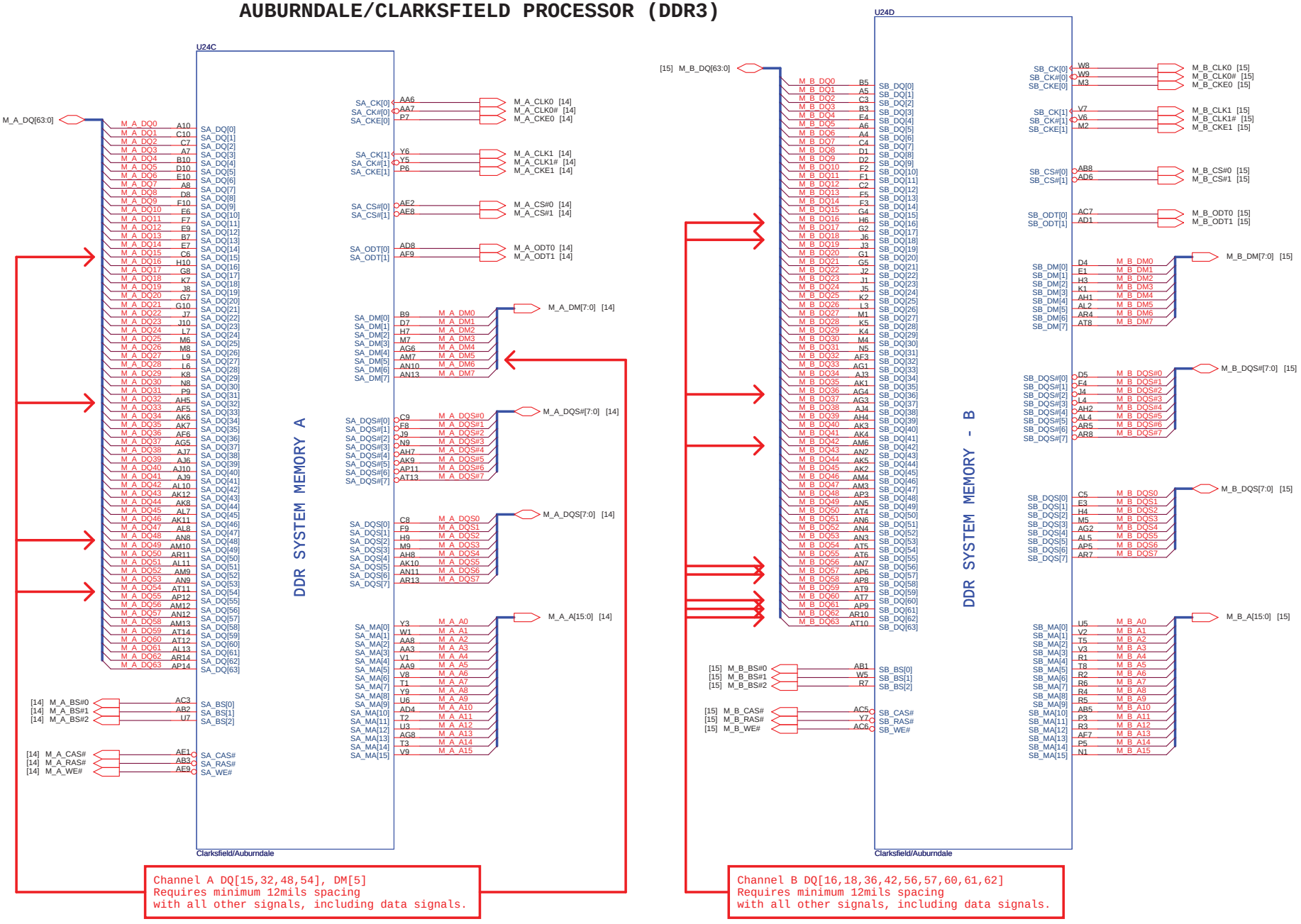
<The GFX_IMON, FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT>Note that if these signals are left as no connect, there are no functional impacts, but a small amount of power (~15 mW) maybe wasted.

Quanta Computer Inc.
PROJECT : ZRD

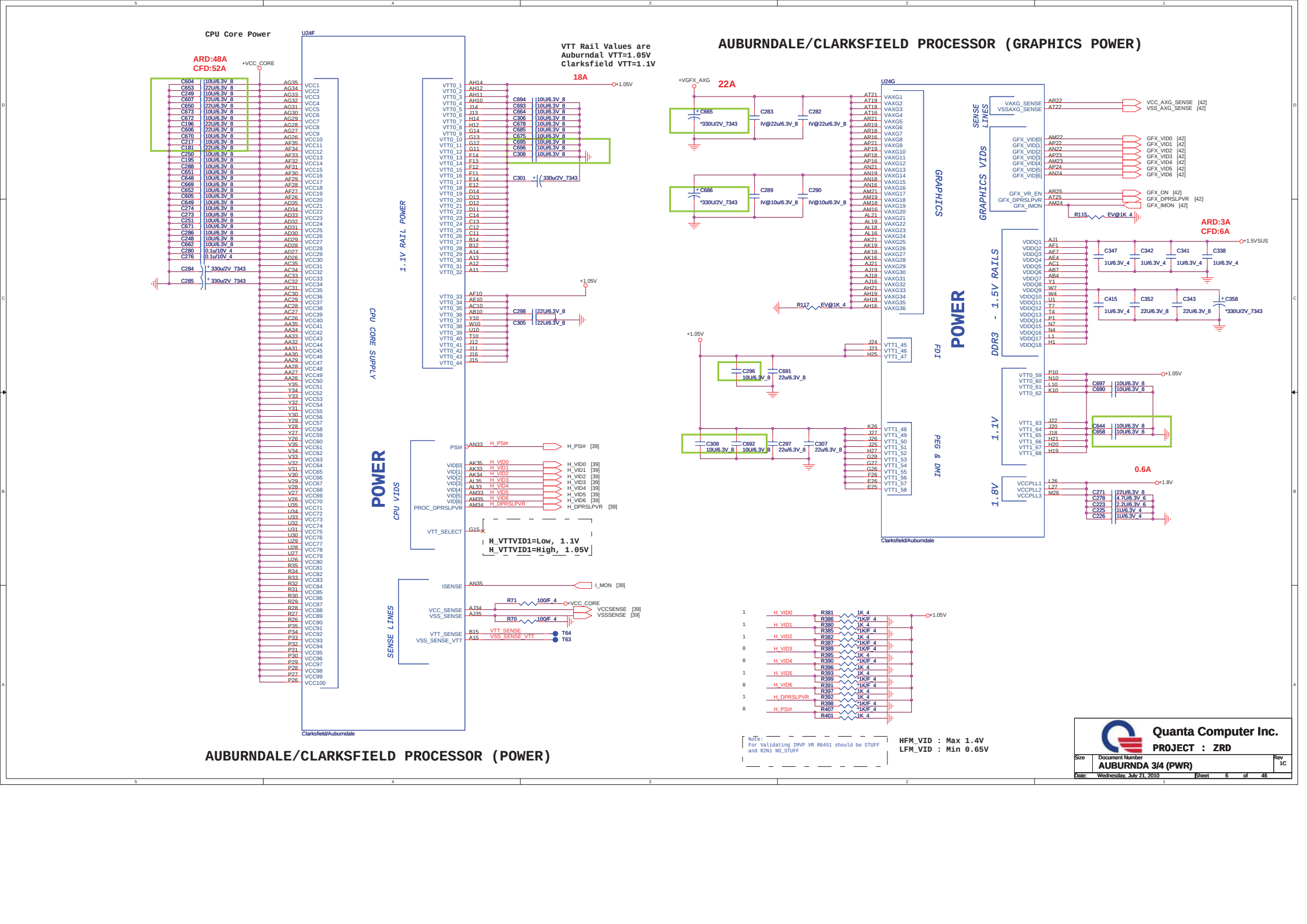
Size	Document Number	Rev
	AUBURNDA 1/4	1C

Date: Wednesday, July 21, 2010 Sheet 4 of 46

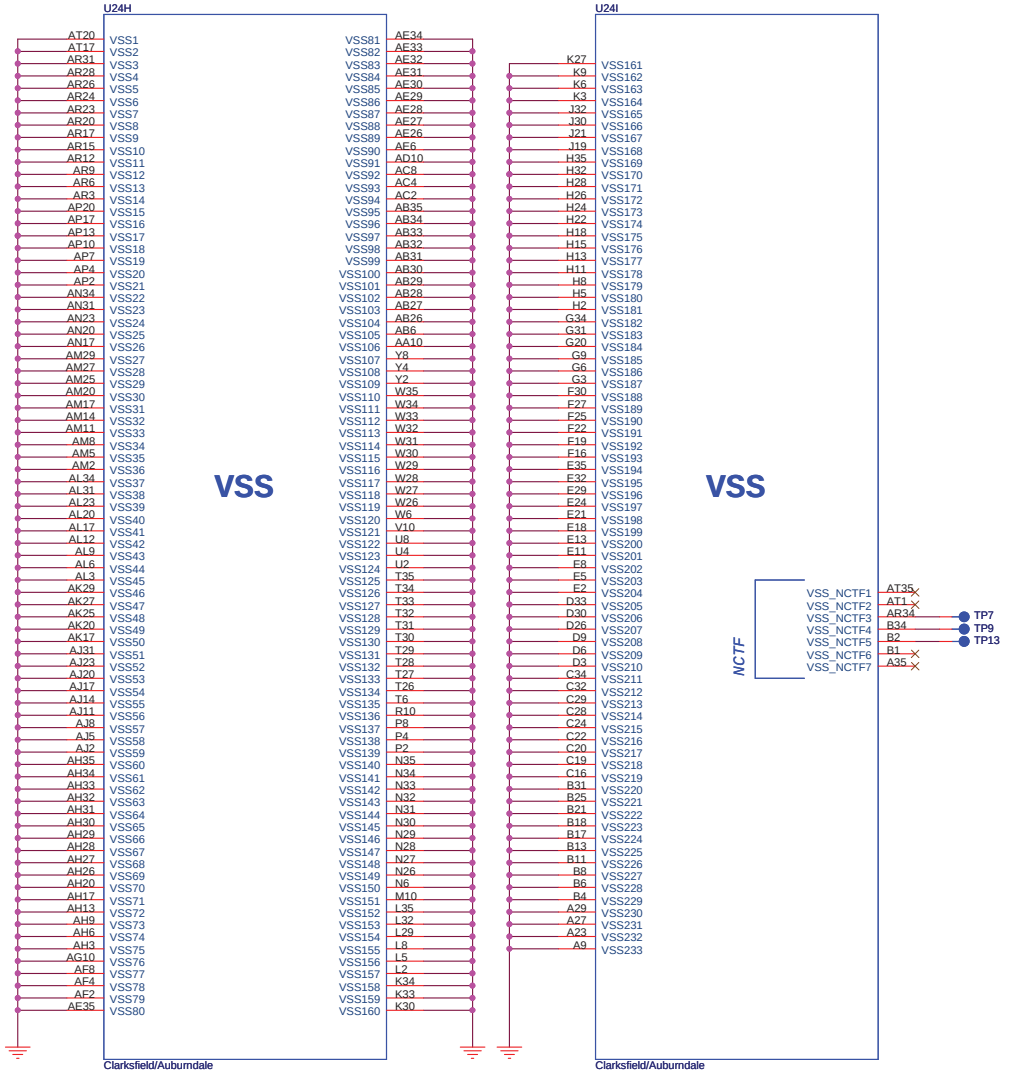
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



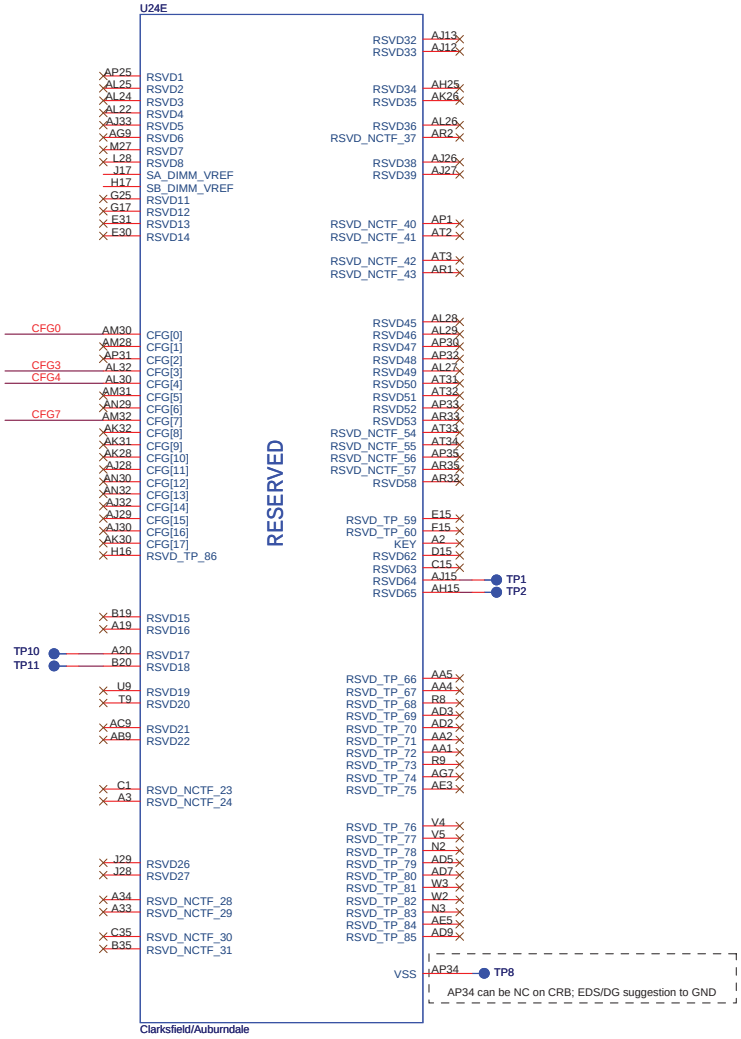
Quanta Computer Inc.			
PROJECT : ZRD			
Size	Document Number		Rev
	AUBURNDA 2/4		1C
Date: Wednesday, July 21, 2010		Sheet 5 of 46	


CPU Core Power
ARD:48A
CFD:52A
+VCC_CORE
U24F
VTT Rail Values are
Auburndal VTT=1.05V
Clarksfield VTT=1.1V
18A
1.1V RAIL POWER
CPU CORE SUPPLY
POWER
CPU VIDS
SENSE LINES
H_VTTVID1=Low, 1.1V
H_VTTVID1=High, 1.05V
Clarksfield/Auburndale
AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)
AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)
+VGFX_AXG
22A
U24G
GRAPHICS
POWER
FDI
PEG & DMI
SENSE LINES
GRAPHICS VIDs
DDR3 - 1.5V RAILS
1.1V
1.8V
ARD:3A
CFD:6A
0.6A
Clarksfield/Auburndale
HFM_VID : Max 1.4V
LFM_VID : Min 0.65V
Quanta Computer Inc.
PROJECT : ZRD
AUBURNDA 3/4 (PWR)
Wednesday, July 21, 2010
Sheet 6 of 46

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



Processor Strapping

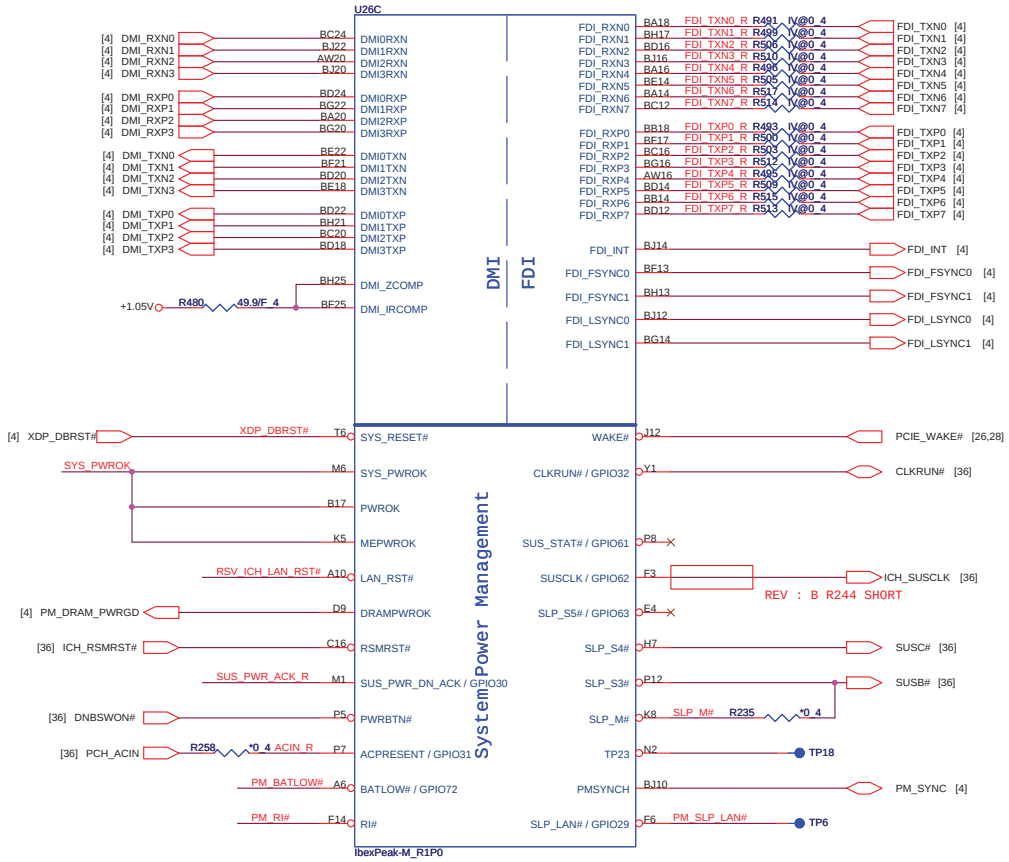
	1	0	DEFAULT	
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled	1	CFG0 R110 *3.01K_NC
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed	1	CFG3 R102 3.01K/F_4
CFG4 (Embended Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port	1	CFG4 R109 *3.01K
The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.				CFG7 R103 *3.01K/F_4

Quanta Computer Inc.
PROJECT : ZRD

Size	Document Number	Rev
	AUBURNDA 4/4	1C
Date: Wednesday, July 21, 2010	Sheet 7 of 46	

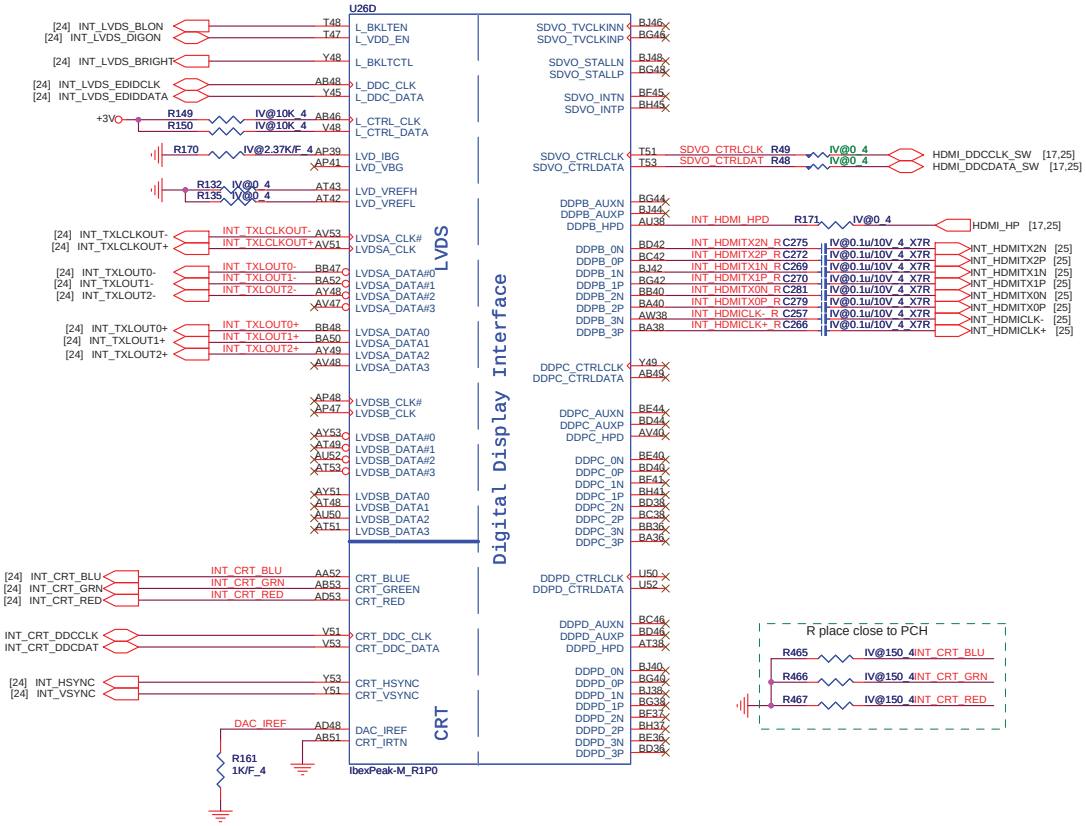
IBEX PEAK-M (DMI,FDI,GPIO)

0-ohm resistor place close to PCH

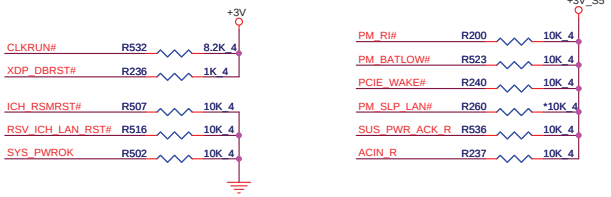


AC-coupling CAP place close to PCH

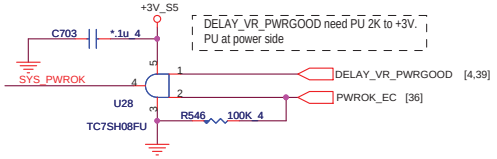
IBEX PEAK-M (LVDS,DDI)



PCH Pull-high/low



System PWR_OK



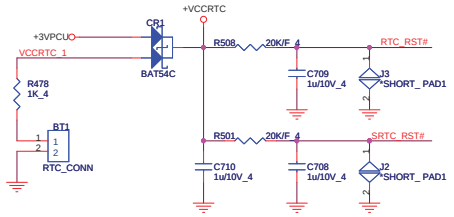
Quanta Computer Inc.

PROJECT : ZRD

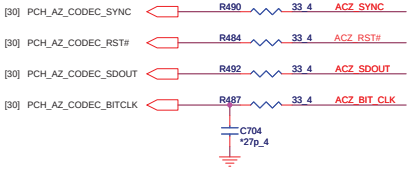
Size	Document Number	Rev
	IBEX PEAK-M 1/6	1C

Date: Wednesday, July 21, 2010 Sheet 8 of 46

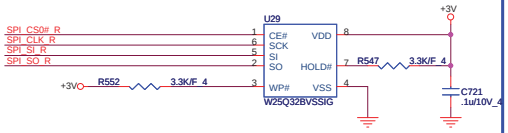
RTC Circuitry



HDA Bus

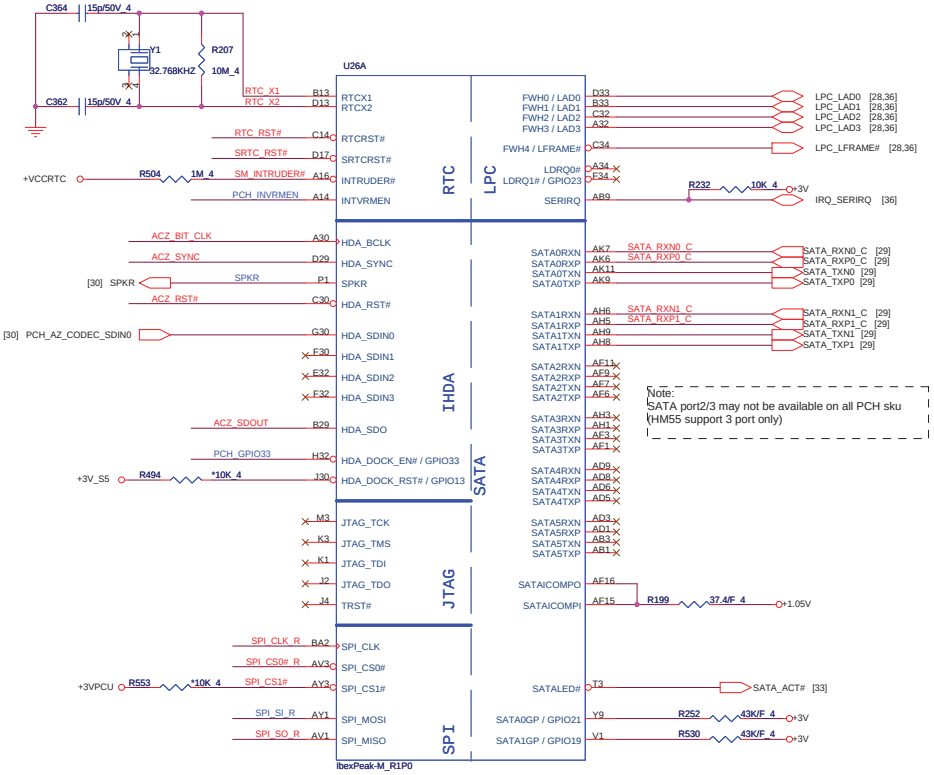


PCH SPI



HDA_SYNC (PCH strap pin)

Internal weak pull-down
VCCVRM=>+1.8V (default)
external pull-up
VCCVRM=>+1.5V



Note:
SATA port2/3 may not be available on all PCH sku (HM55 support 3 port only)

PCH Strap Pin Configuration Table-1

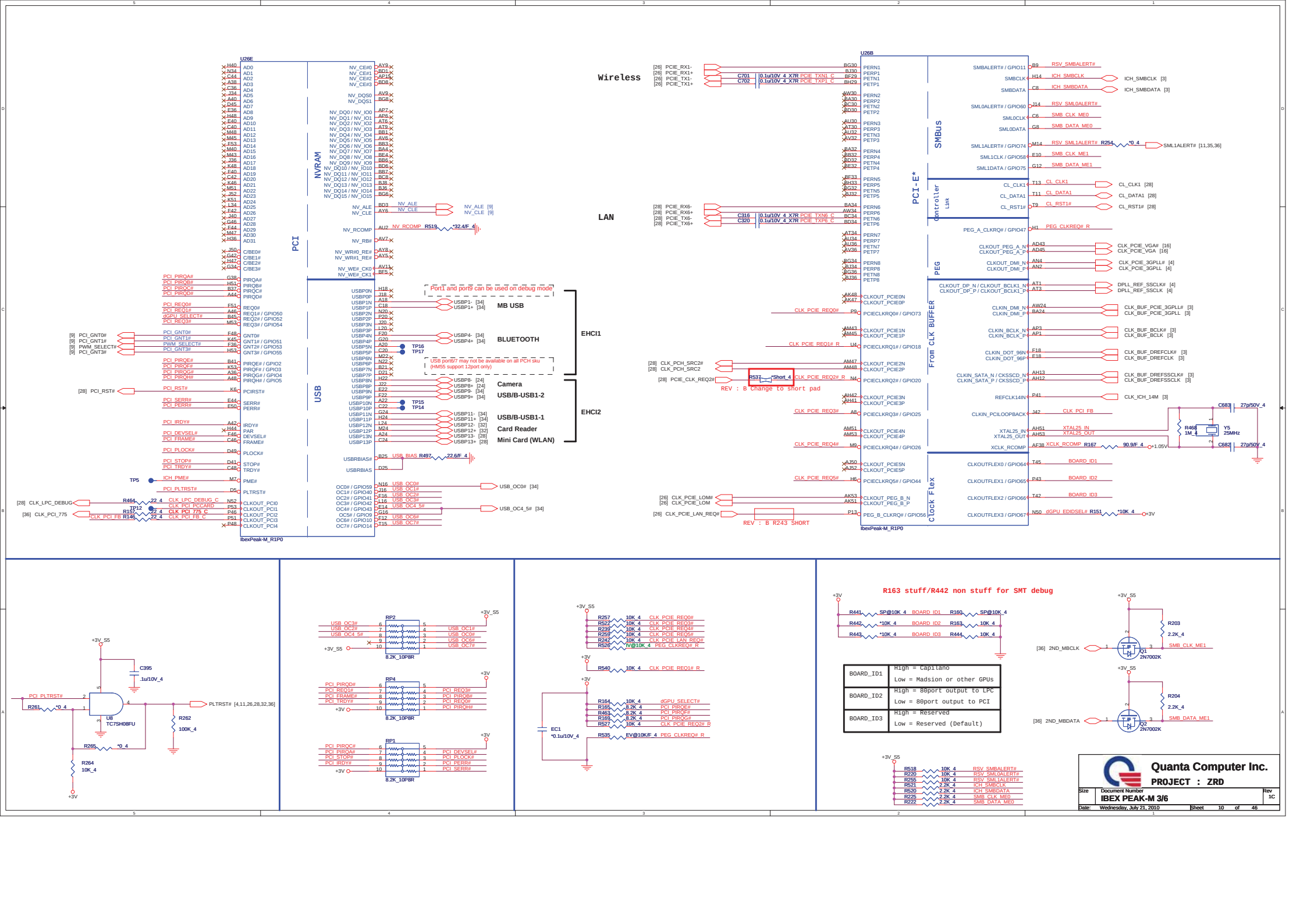
INTVRMEN	Integrated 1.05V VRM Enable / Disable	1 = Integrated VRM is enabled 0 = Integrated VRM is disabled	+VCCRTC R511 330K_6 PCH_INVRMEN
SPI_MOSI	TPM Functionality Disable	1 = Enabled 0 = Disable	+3V R551 *1K_4 SPI_SI_R
SPKR	Reboot option at power-up	0 = Default Mode (Internal weak Pull-down) 1 = No Reboot Mode with TCO Disabled	+3V R538 *1K/F_4 SPKR
HDA_DOCK_EN #/GPIO33	Flash Descriptor Security Override	0 = Flash Descriptor Security will be overridden 1 = Security measure defined in the Flash Descriptor will be enabled.	PCH_GPIO33 J1 *SHORT_PAD1
GNT0#, GNT1#	Boot BIOS Strap	(0,0) = LPC (0,1) = Reserved NAND (1,0) = PCI (1,1) = SPI	[10] PCI_GNT0# R158 1K_4 R152 1K_4 +3V [10] PCI_GNT1# R153 *1K_4 R159 *1K_4
GNT2#/ GPIO53	ESI Strap (Server Only)	ESI compatible mode is for server platforms only	[10] PWM_SELECT# R182 *1K/F_4
GNT3#/ GPIO55	Top-Block Swap Override	0 = Top Block Swap Mode 1 = Default Mode (Internal pull-up)	[10] PCI_GNT3# R462 *10K/F_4
NV_ALE	IntelR Anti-Theft Technology HDD Data Protection (Intel AT-d) Enable	1 = Enabled 0 = Disabled (Default)	[10] NV_ALE R213 *1K/F_4 +1.8V
NV_CLE	DMI Termination Voltage	DMI termination voltage. Weak internal pull-up. Do not pull low.	[10] NV_CLE R216 *1K/F_4 +1.8V

GPIO8	Reserved	This signal has a weak internal pull up. NOTE: This signal should not be pulled low	[11] RSV_GPIO8 R215 10K_4 +3V_S5 R214 *1K_4
GPIO15	Reserved	0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality	[11] CR_WAKE# R256 1K_4 +3V_S5
GPIO27	On-Die PLL Voltage Regulator <internal weak pull-up>	0 = Disables the VccVRM. 1 = Enables the internal VccVRM to have a clean supply for analog rails.	[11] PCH_GPIO27 R231 *10K_4

Quanta Computer Inc.
PROJECT : ZRD

Size	Document Number	Rev
	IBEX PEAK-M 2/6	1C

Date: Wednesday, July 21, 2010 Sheet 9 of 46


U26E
PCI
NVRAM
USB
IbexPeak-M_R1P0
Port1 and port9 can be used on debug mode
MB USB
BLUETOOTH
Camera
USB/B-USB1-2
USB/B-USB1-1
Card Reader
Mini Card (WLAN)
EHCI1
EHCI2
USB port6/7 may not be available on all PCH sku
(HM55 support 12port only)
Wireless
LAN
U26B
PCI-E*
SMBUs
Controller
Link
PEG
From CLK BUFFER
Clock Flex
REV : B Change to short pad
REV : B R243 SHORT
R163 stuff/R442 non stuff for SMT debug
BOARD_ID1 High = Capitano Low = Madsion or other GPUs
BOARD_ID2 High = 80port output to LPC Low = 80port output to PCI
BOARD_ID3 High = Reserved Low = Reserved (Default)
Quanta Computer Inc.
PROJECT : ZRD
IBEX PEAK-M 3/6
Size
Document Number
Rev 1C
Date: Wednesday, July 21, 2010
Sheet 10 of 46

IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

dGPU_PWR_EN# should be stable before dGPU_VRON enable

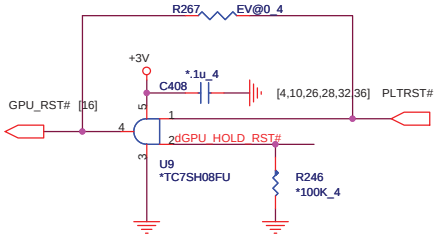
REV : B Change to short pad

[10,35,36] SML1ALERT# R533 *Short_4 SATA5GP

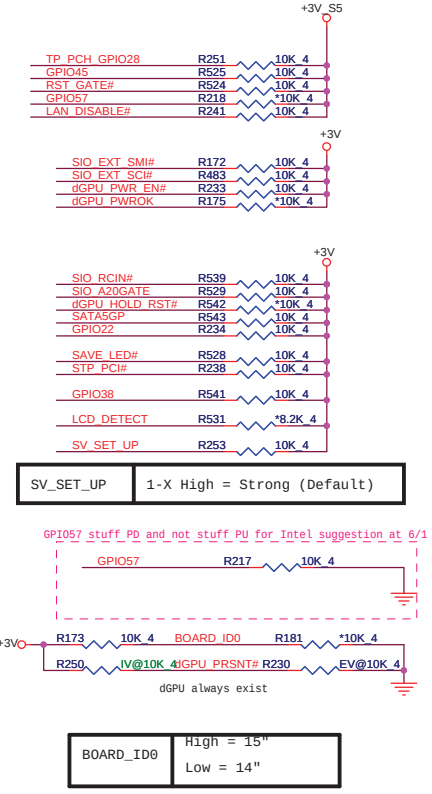
EC suggestion use GPIO49 for FAN control

SATA5GP / GPIO49 / TEMP_ALERT# is used to alert for EC when CPU or Graph/Memory controllers' temperature go out of limit. So connecting GPIO49 to EC and avoid this pin to be used for other purpose

GPU RST#



GPIO Pull-up/Pull-down



SV_SET_UP	1-X High = Strong (Default)

GPIO57 stuff PD and not stuff PU for Intel suggestion at 6/1

BOARD_ID0	High = 15" Low = 14"

Quanta Computer Inc.

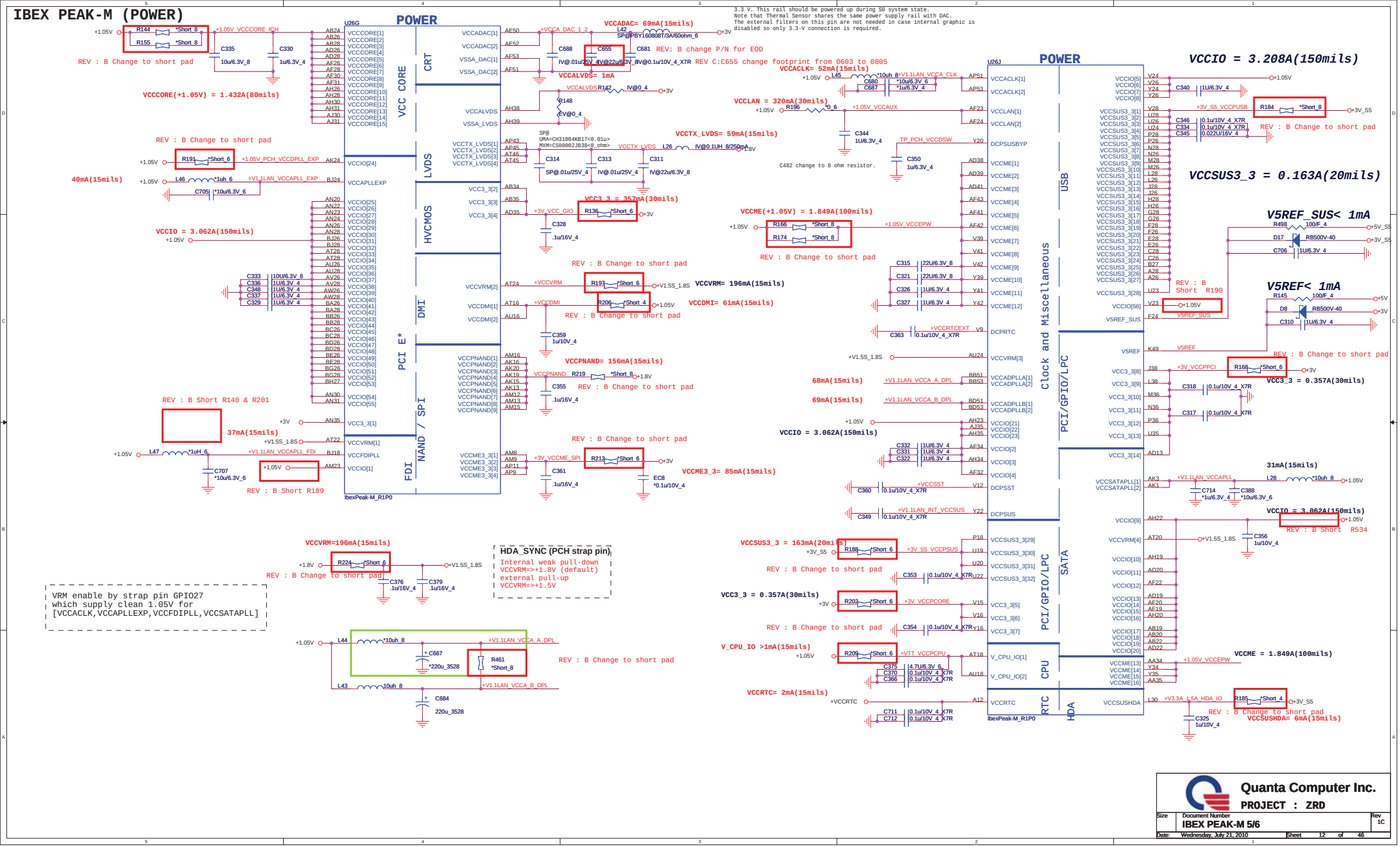
PROJECT : ZRD

Size	Document Number	Rev
	IBEX PEAK-M 4/6	1C

Date: Wednesday, July 21, 2010 Sheet 11 of 46

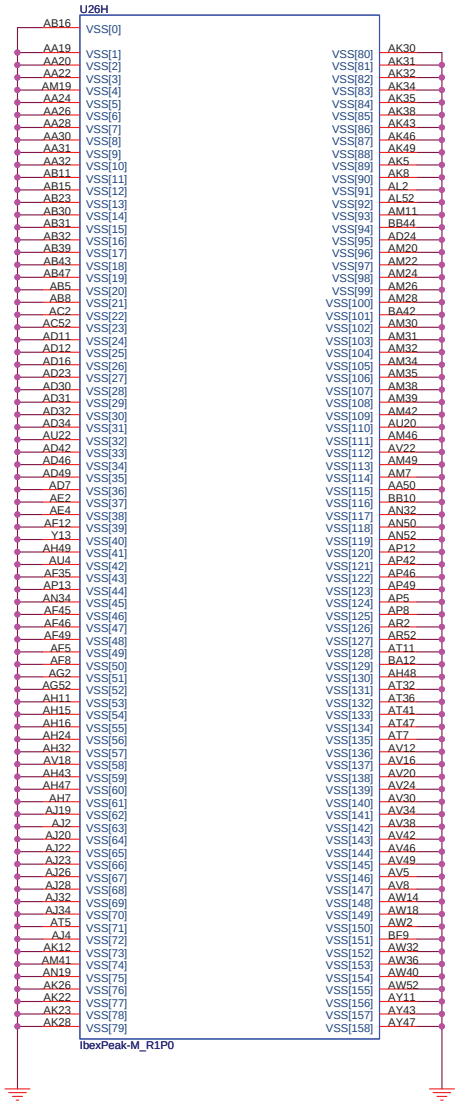
IBEX PEAK-M (POWER)

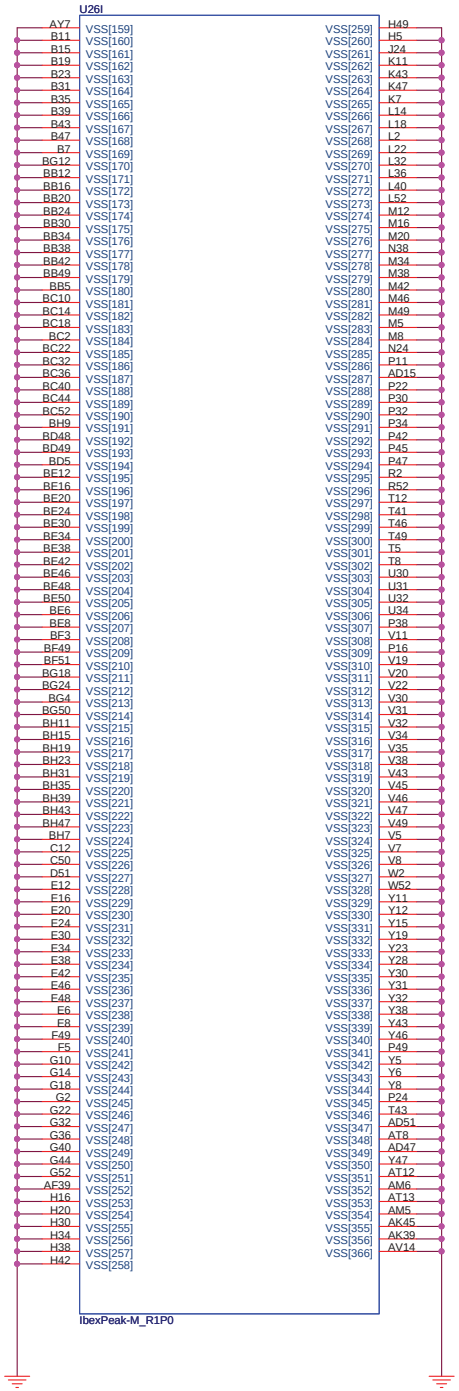
3.3 V. This rail should be powered up during S0 system state.
Note that Thermal Sensor shares the same power supply rail with DAC.
The external filters on this pin are not needed in case internal graphic is disabled so only 3.3-V connection is required.



Quanta Computer Inc.			
PROJECT : ZRD			
Size	Document Number		Rev
	IBEX PEAK-M 5/6		1C
Date: Wednesday, July 21, 2010	Sheet 12 of 46		

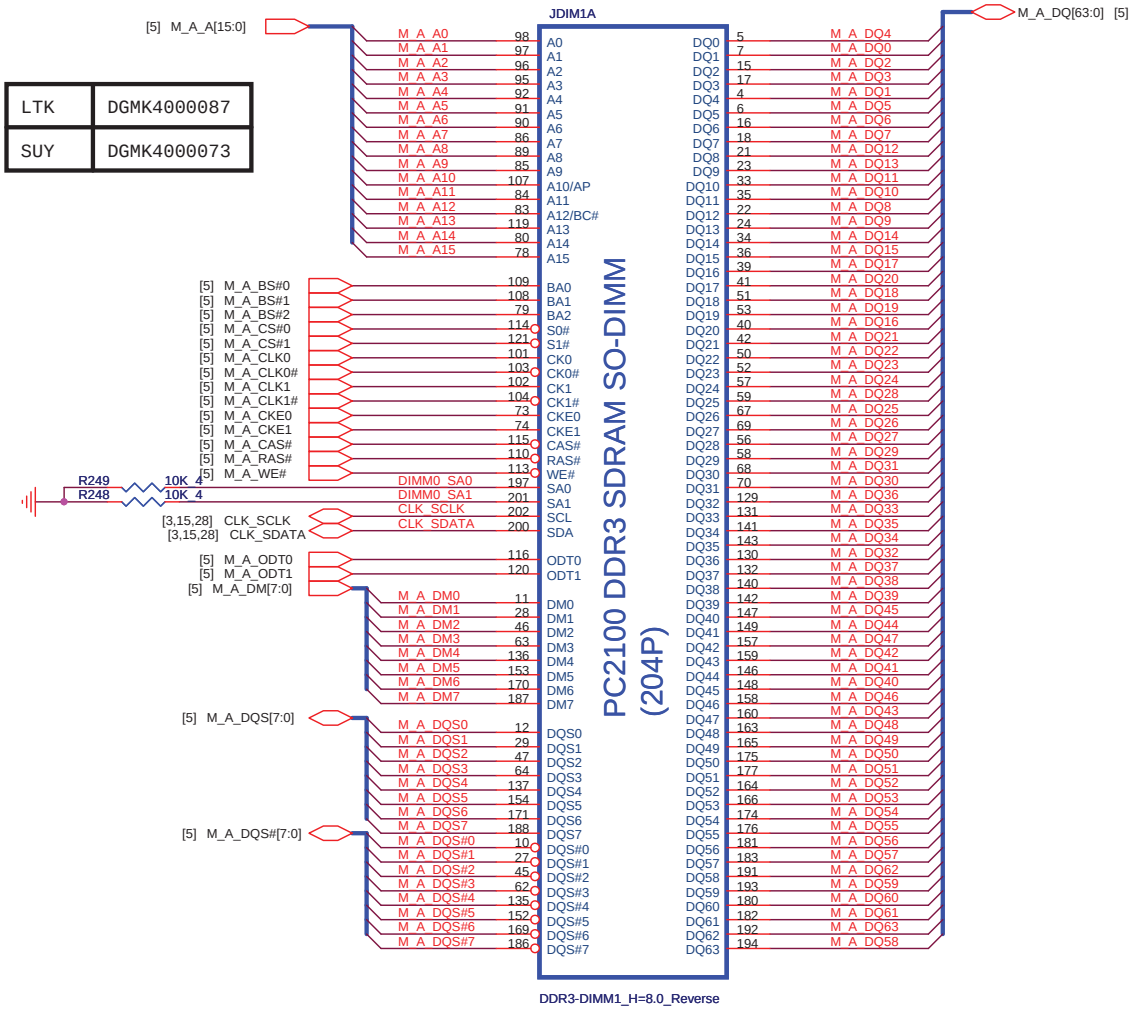
IBEX PEAK-M (GND)

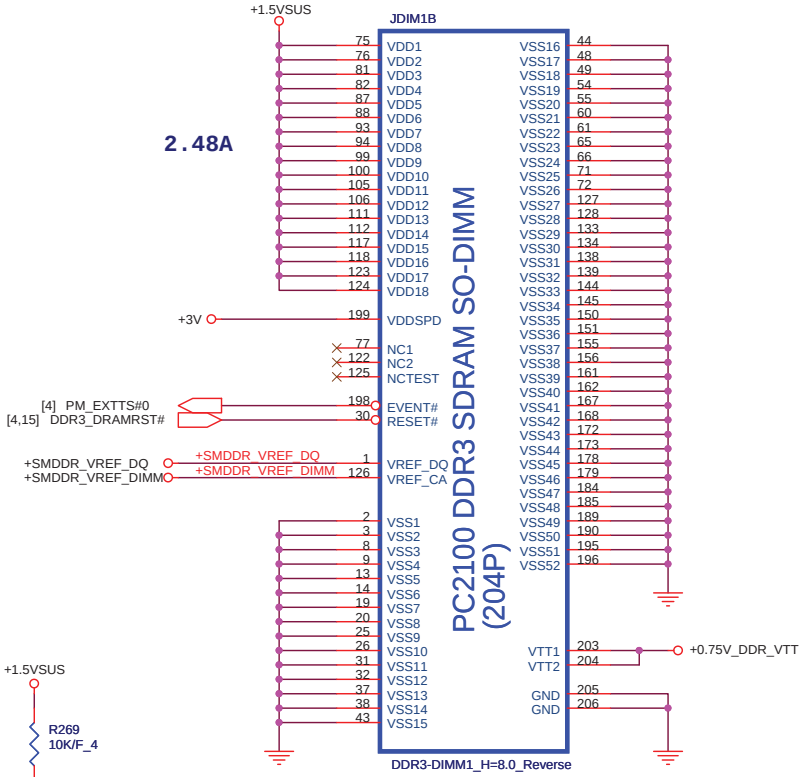


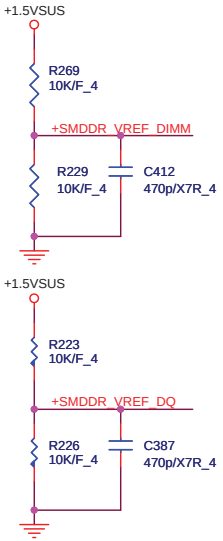


Quanta Computer Inc.		
PROJECT : ZRD		
Size	Document Number: IBEX PEAK-M 6/6	Rev: 1C
Date: Wednesday, July 21, 2010	Sheet 13 of 46	

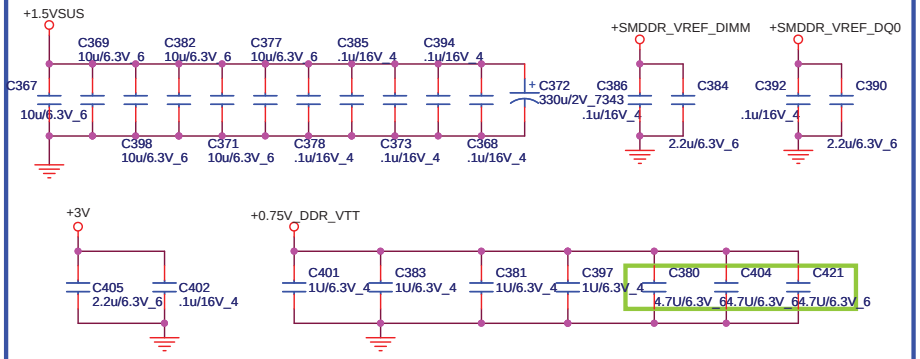
LTK	DGMK4000087
SUY	DGMK4000073







Place these Caps near So-Dimm0.

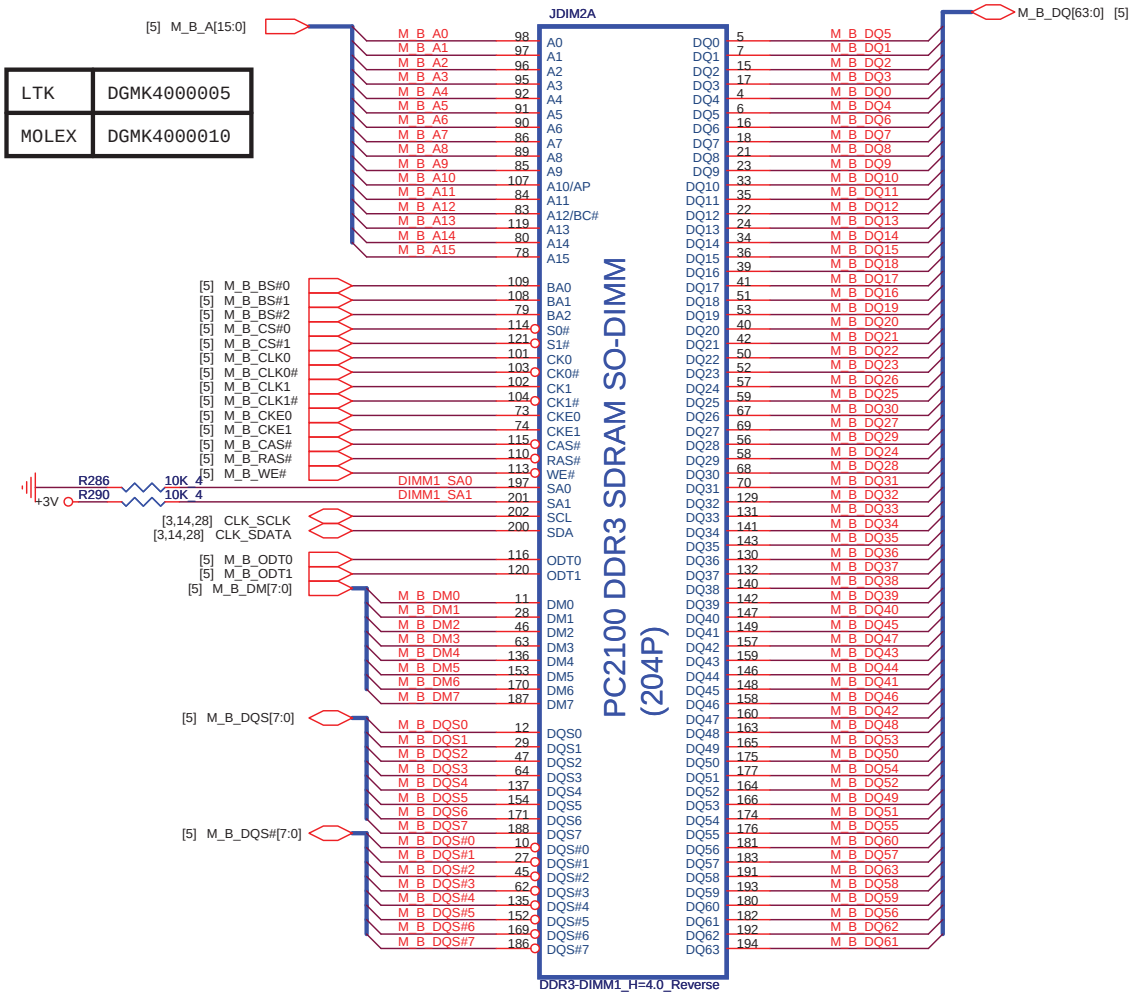


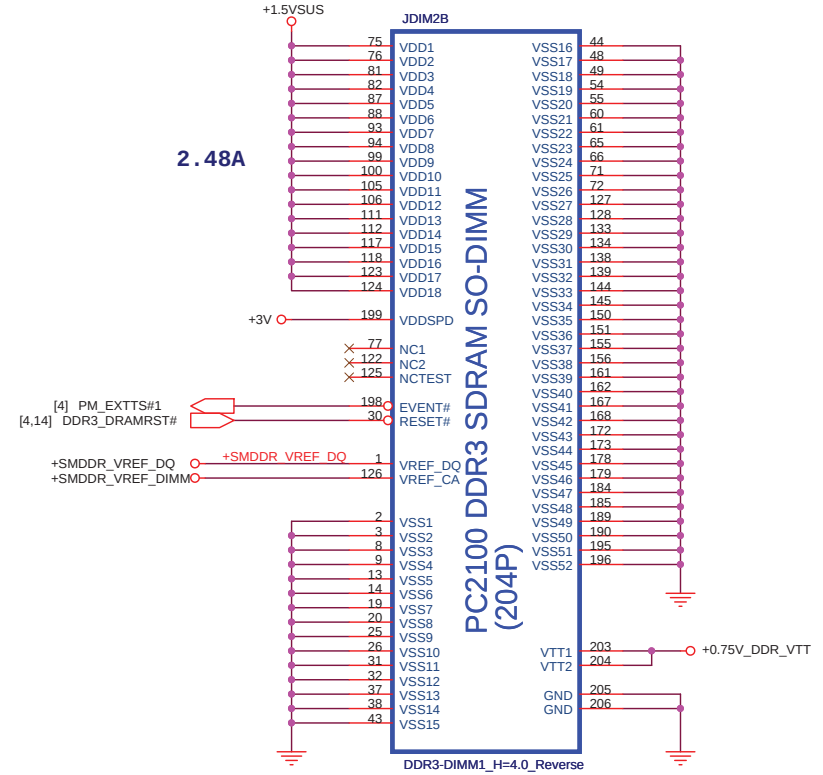
Quanta Computer Inc.

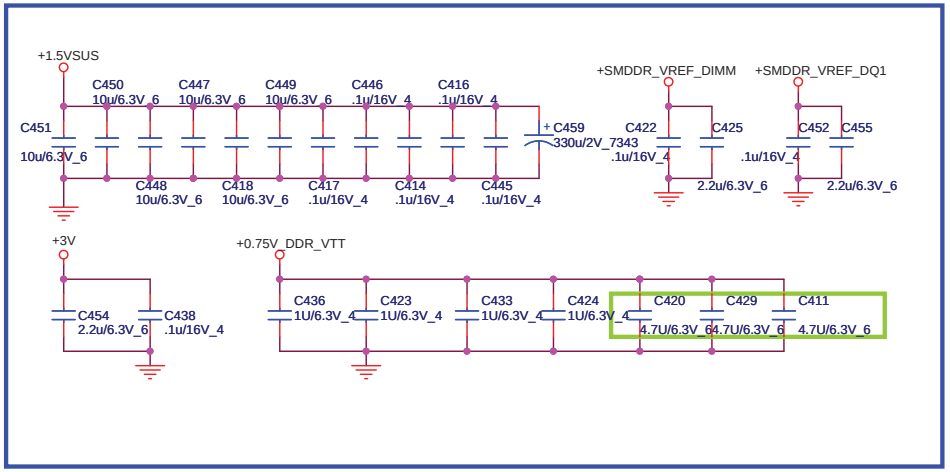
PROJECT : ZRD

Size	Document Number	Rev
	DDRIII SO-DIMM-0	1C
Date:	Wednesday, July 21, 2010	Sheet 14 of 46

LTK	DGMK4000005
MOLEX	DGMK4000010







Quanta Computer Inc.

PROJECT : ZRD

Size	Document Number	Rev
	DDRIII SO-DIMM-1	1C
Date: Wednesday, July 21, 2010	Sheet 15 of 46	

GPU_1(VGA)

[4] PEG_TXP[0..15] → PEG_TXP[0..15]
[4] PEG_TXN[0..15] → PEG_TXN[0..15]
[4] PEG_RXP[0..15] → PEG_RXP[0..15]
[4] PEG_RXN[0..15] → PEG_RXN[0..15]

0518 SWAP PCIE for VGA side

U21A

PEG_TXP15 / PEG_TXN15	AA38 / Y37	PCIE_RX0P / PCIE_RX0N	PCIE_TX0P / PCIE_TX0N	Y33 / Y32	CPEG_RXP15 C155 / CPEG_RXN15 C164	EV@0.1u/10V_4	PEG_RXP15 [4] / PEG_RXN15 [4]
PEG_TXP14 / PEG_TXN14	Y35 / W36	PCIE_RX1P / PCIE_RX1N	PCIE_TX1P / PCIE_TX1N	W33 / W32	CPEG_RXP14 C147 / CPEG_RXN14 C154	EV@0.1u/10V_4	PEG_RXP14 [4] / PEG_RXN14 [4]
PEG_TXP13 / PEG_TXN13	W38 / V37	PCIE_RX2P / PCIE_RX2N	PCIE_TX2P / PCIE_TX2N	U33 / U32	CPEG_RXP13 C141 / CPEG_RXN13 C146	EV@0.1u/10V_4	PEG_RXP13 [4] / PEG_RXN13 [4]
PEG_TXP12 / PEG_TXN12	V35 / U36	PCIE_RX3P / PCIE_RX3N	PCIE_TX3P / PCIE_TX3N	U30 / U29	CPEG_RXP12 C136 / CPEG_RXN12 C131	EV@0.1u/10V_4	PEG_RXP12 [4] / PEG_RXN12 [4]
PEG_TXP11 / PEG_TXN11	U38 / T37	PCIE_RX4P / PCIE_RX4N	PCIE_TX4P / PCIE_TX4N	T33 / T32	CPEG_RXP11 C130 / CPEG_RXN11 C116	EV@0.1u/10V_4	PEG_RXP11 [4] / PEG_RXN11 [4]
PEG_TXP10 / PEG_TXN10	T35 / R36	PCIE_RX5P / PCIE_RX5N	PCIE_TX5P / PCIE_TX5N	T30 / T29	CPEG_RXP10 C109 / CPEG_RXN10 C106	EV@0.1u/10V_4	PEG_RXP10 [4] / PEG_RXN10 [4]
PEG_TXP9 / PEG_TXN9	R38 / P37	PCIE_RX6P / PCIE_RX6N	PCIE_TX6P / PCIE_TX6N	P33 / P32	CPEG_RXP9 C105 / CPEG_RXN9 C92	EV@0.1u/10V_4	PEG_RXP9 [4] / PEG_RXN9 [4]
PEG_TXP8 / PEG_TXN8	P35 / N36	PCIE_RX7P / PCIE_RX7N	PCIE_TX7P / PCIE_TX7N	P30 / P29	CPEG_RXP8 C91 / CPEG_RXN8 C87	EV@0.1u/10V_4	PEG_RXP8 [4] / PEG_RXN8 [4]
PEG_TXP7 / PEG_TXN7	N38 / M37	PCIE_RX8P / PCIE_RX8N	PCIE_TX8P / PCIE_TX8N	N33 / N32	CPEG_RXP7 C86 / CPEG_RXN7 C80	EV@0.1u/10V_4	PEG_RXP7 [4] / PEG_RXN7 [4]
PEG_TXP6 / PEG_TXN6	M35 / L36	PCIE_RX9P / PCIE_RX9N	PCIE_TX9P / PCIE_TX9N	N30 / N29	CPEG_RXP6 C79 / CPEG_RXN6 C75	EV@0.1u/10V_4	PEG_RXP6 [4] / PEG_RXN6 [4]
PEG_TXP5 / PEG_TXN5	L38 / K37	PCIE_RX10P / PCIE_RX10N	PCIE_TX10P / PCIE_TX10N	L33 / L32	CPEG_RXP5 C72 / CPEG_RXN5 C69	EV@0.1u/10V_4	PEG_RXP5 [4] / PEG_RXN5 [4]
PEG_TXP4 / PEG_TXN4	K35 / J36	PCIE_RX11P / PCIE_RX11N	PCIE_TX11P / PCIE_TX11N	L30 / L29	CPEG_RXP4 C67 / CPEG_RXN4 C63	EV@0.1u/10V_4	PEG_RXP4 [4] / PEG_RXN4 [4]
PEG_TXP3 / PEG_TXN3	J38 / H37	PCIE_RX12P / PCIE_RX12N	PCIE_TX12P / PCIE_TX12N	K33 / K32	CPEG_RXP3 C59 / CPEG_RXN3 C61	EV@0.1u/10V_4	PEG_RXP3 [4] / PEG_RXN3 [4]
PEG_TXP2 / PEG_TXN2	H35 / G36	PCIE_RX13P / PCIE_RX13N	PCIE_TX13P / PCIE_TX13N	J33 / J32	CPEG_RXP2 C56 / CPEG_RXN2 C58	EV@0.1u/10V_4	PEG_RXP2 [4] / PEG_RXN2 [4]
PEG_TXP1 / PEG_TXN1	G38 / F37	PCIE_RX14P / PCIE_RX14N	PCIE_TX14P / PCIE_TX14N	K30 / K29	CPEG_RXP1 C50 / CPEG_RXN1 C48	EV@0.1u/10V_4	PEG_RXP1 [4] / PEG_RXN1 [4]
PEG_TXP0 / PEG_TXN0	F35 / E37	PCIE_RX15P / PCIE_RX15N	PCIE_TX15P / PCIE_TX15N	H33 / H32	CPEG_RXP0 C55 / CPEG_RXN0 C52	EV@0.1u/10V_4	PEG_RXP0 [4] / PEG_RXN0 [4]

0518 SWAP PCIE for VGA side

PCI EXPRESS INTERFACE

CLOCK

[10] CLK_PCIE_VGA → AB35 PCIE_REFCLKP
[10] CLK_PCIE_VGA# → AA36 PCIE_REFCLKN

For Broadway, Madison and Park
the PWRGOOD ball must be connecctd to ground

R67 EV@10K_4

AJ21 NC#1
AK21 NC#2
AH16 PWRGOOD

[11] GPU_RST# → AA30 PERSTB

CALIBRATION

PCIE_CALRP Y30 — R47 EV@1.27K/F_4 — +1V
PCIE_CALRN Y29 — R46 EV@2K/F_4 — +1V

+1.0V

SP@Capilano/Robson

For M97, Broadway, Madison and Park PCIE_VDDC is 1.0V

Madison	AJ007720T02
Park	AJ077400T08

Quanta Computer Inc.
PROJECT : ZRD

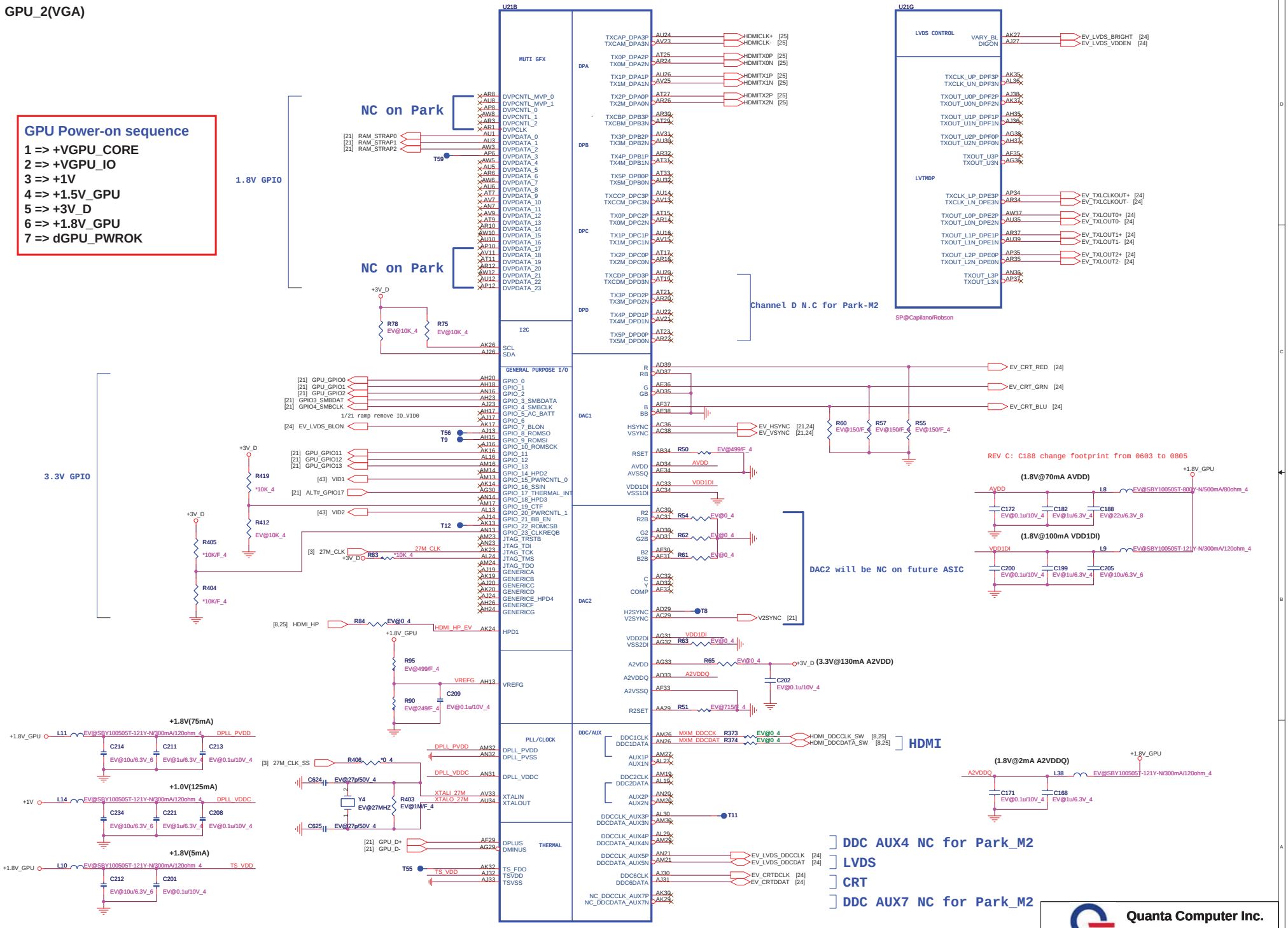
Size	Document Number	Rev
	Capilano/Robson -PCIE I/F	1C

Date: Wednesday, July 21, 2010 Sheet 16 of 46

GPU_2(VGA)

GPU Power-on sequence

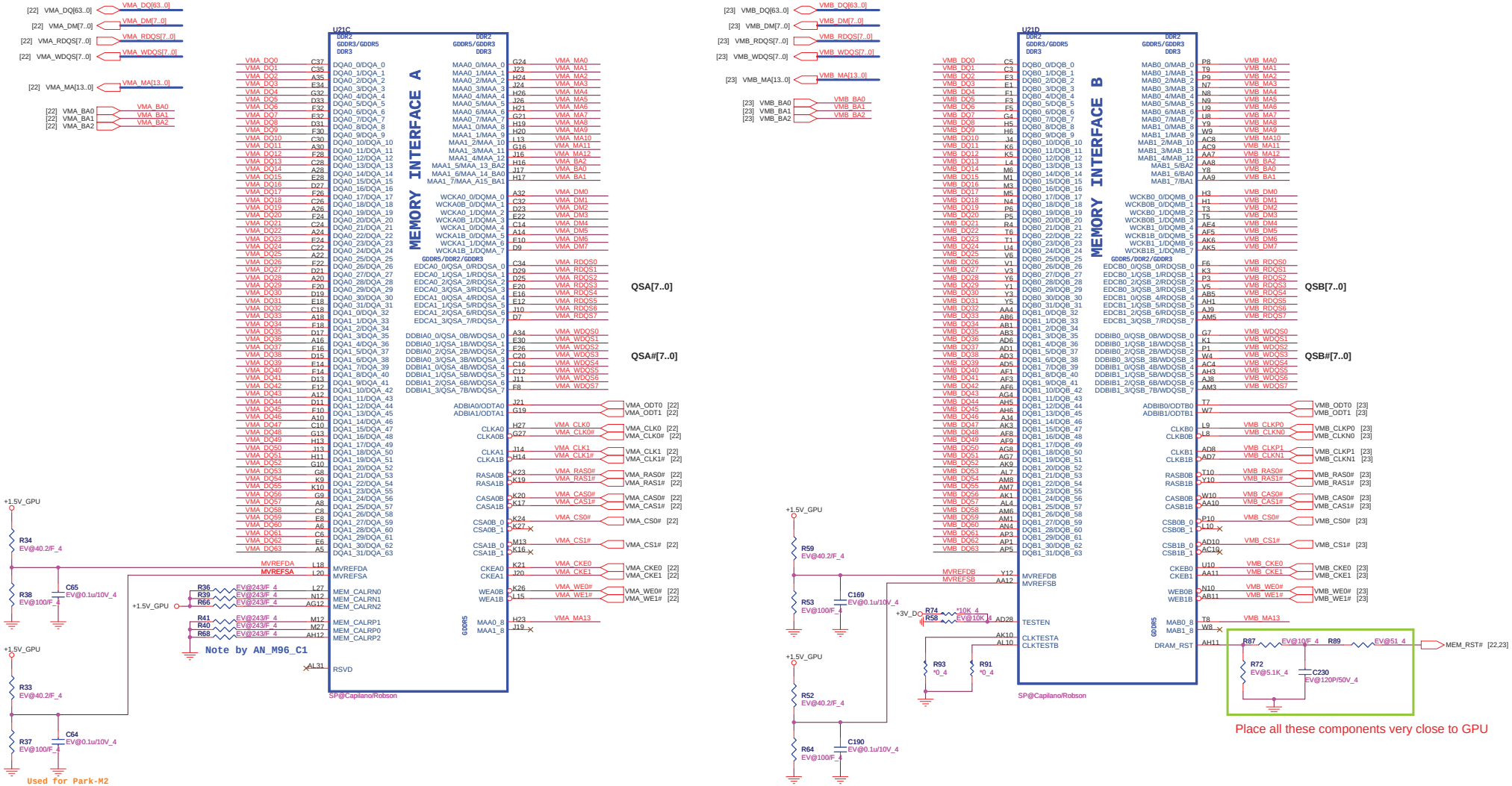
1 => +VGPU_CORE
2 => +VGPU_IO
3 => +1V
4 => +1.5V_GPU
5 => +3V_D
6 => +1.8V_GPU
7 => dGPU_PWROK



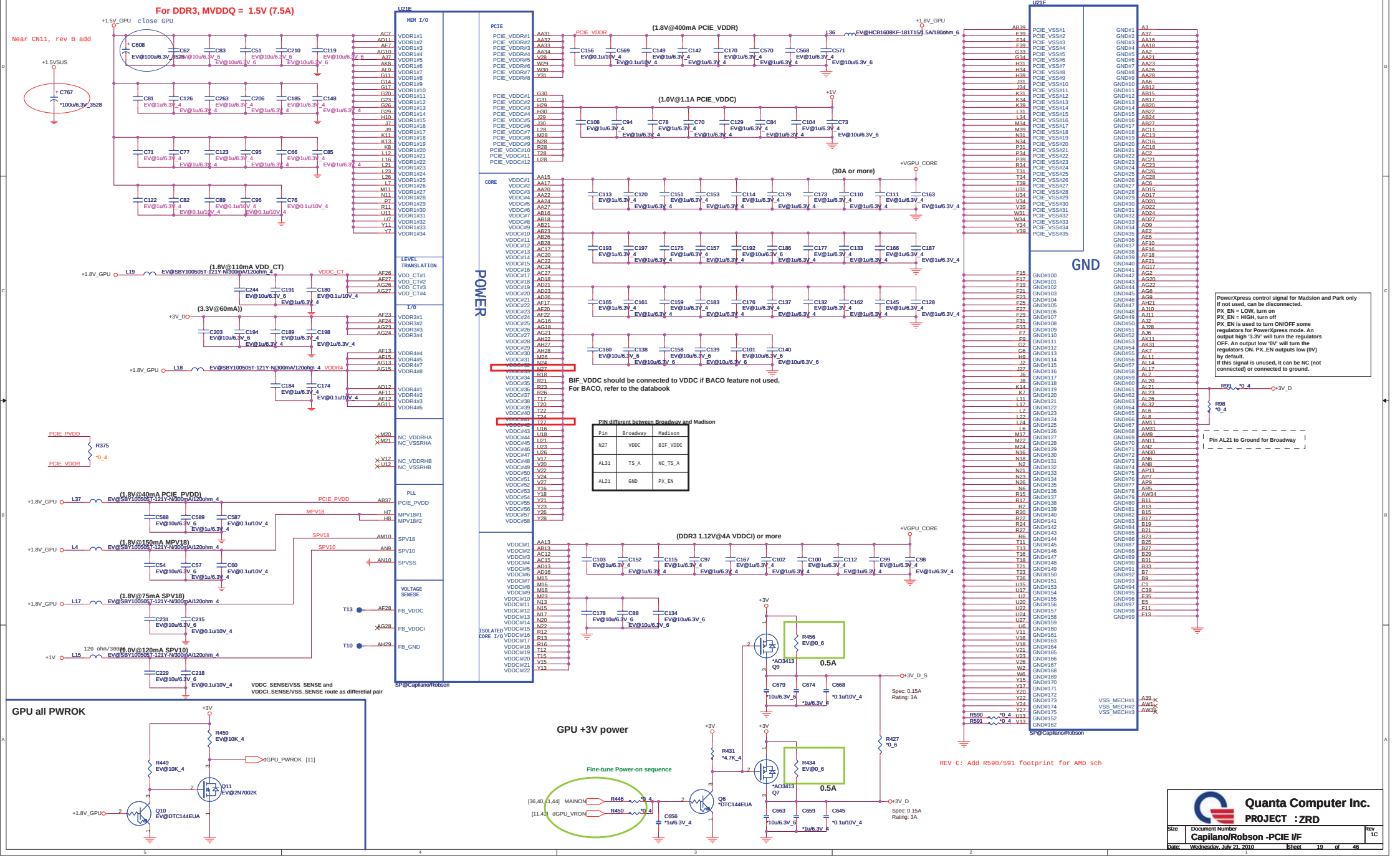
Quanta Computer Inc.			
PROJECT : ZRD			
Size	Document Number		Rev
	Capilano/Robson -PCIE I/F		1C
Date: Wednesday, July 21, 2010		Sheet 17 of 46	

GPU_3(VGA)

Park M2-channel B used(S3 package use Channel A)

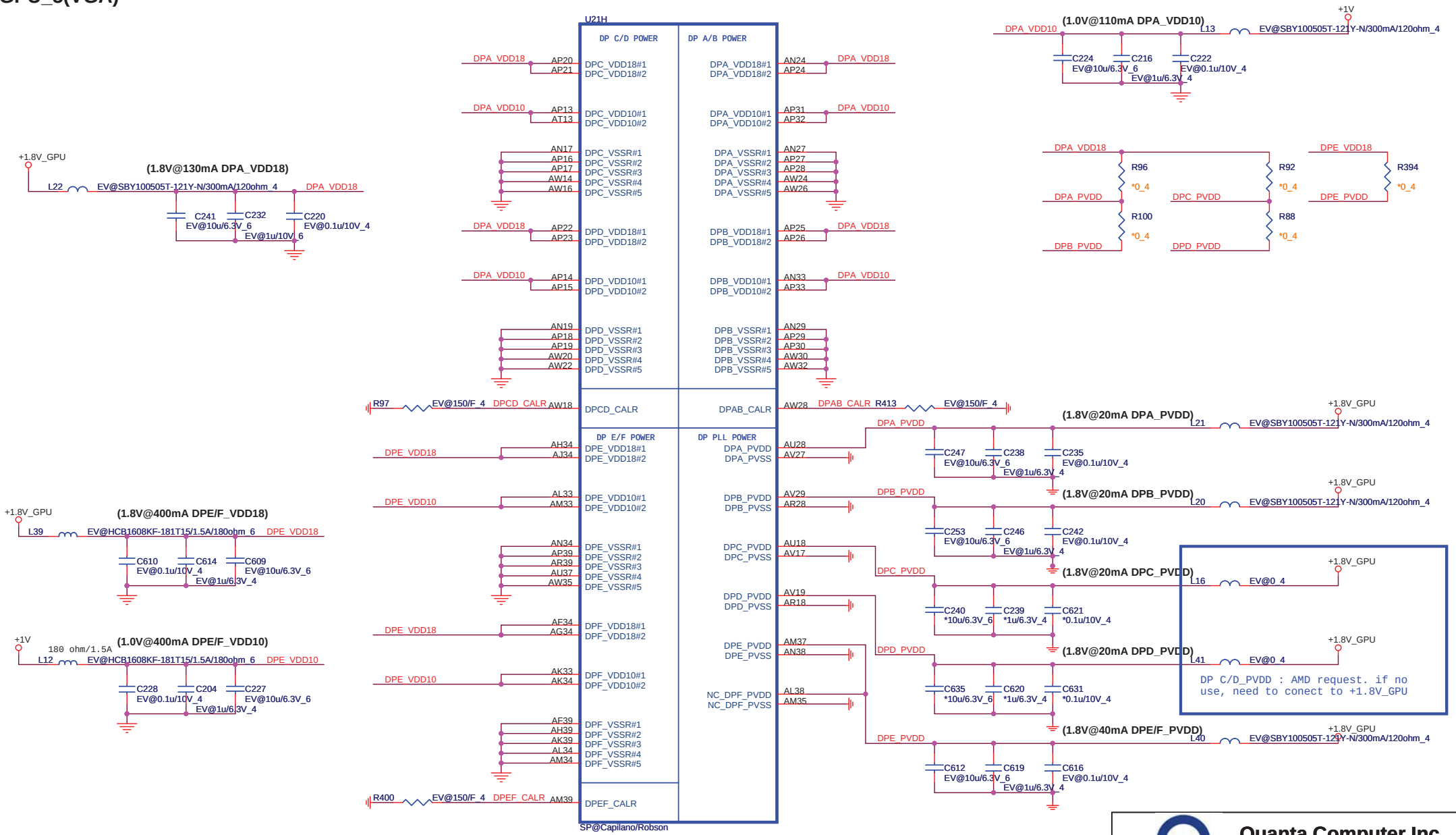


GPU_4(VGA)



Quanta Computer Inc.
PROJECT : ZRD

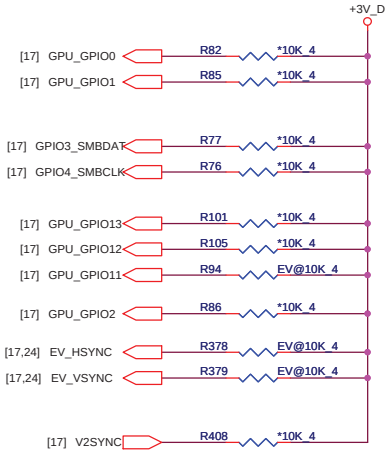
GPU_5(VGA)



Quanta Computer Inc.
PROJECT : ZRD

Size	Document Number	Rev
	Capilano/Robson -PCIE I/F	1C
Date: Wednesday, July 21, 2010	Sheet 20 of 46	

PIN STRAPS(VGA)



Size of the primary memory apertures	GPIO[13:11]
128 MB	000
256MB	001
64 MB	010
32 MB	011
More than 512 MB	Not Supported

CONFIGURATION STRAPS

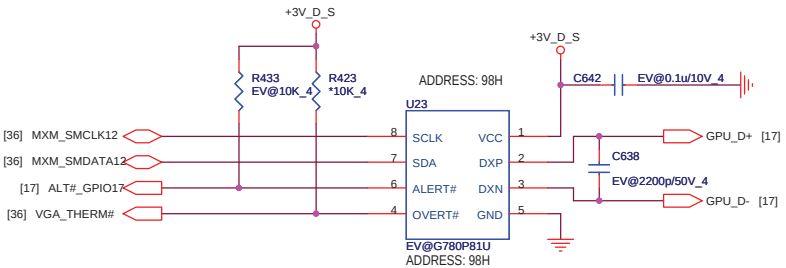
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	0	
ROMIDCFG[2:0]	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	001	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

Thermal Sensor(VGA)

Vendor	P/N
WINDBOND	AL83L771K01
GMT	AL000780000

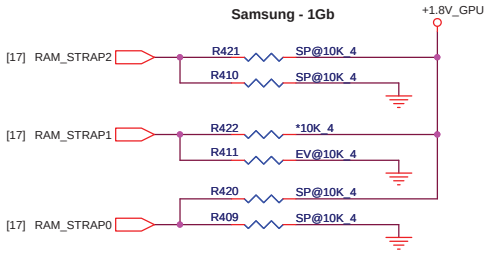
USD0.16



DDR3 Memory Aperture size(GPU)

DDR3 Memory size

Vendor	Vendor P/N	STN B/S P/N	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix			1	1	0
	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	1	0	0
	H5TQ2G63BFR-12C	AKD5MGGTW03 (128M*16)	1	0	1
Samsung					
	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	0	0	0
	K4W2G1646B-HC12	AKD5MGGT500 (128m*16)	0	0	1
AMD	23EY2387MA12-SZ	AKD5LGGT700	0	1	0

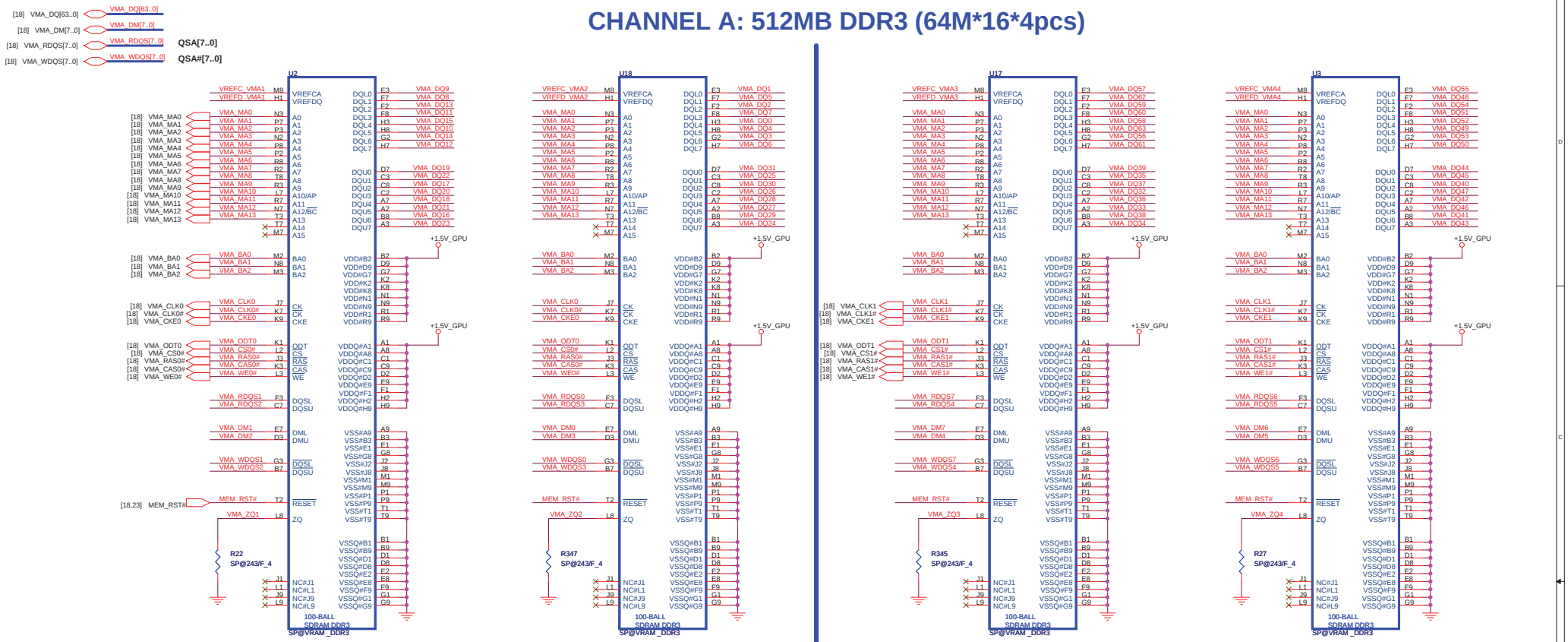


RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

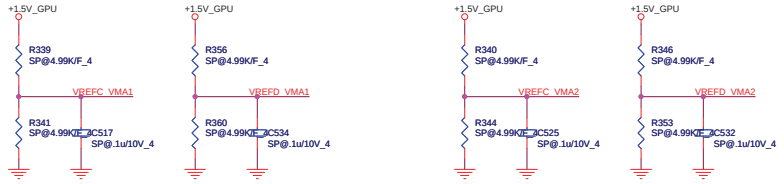
Quanta Computer Inc.
PROJECT : ZRD

Size	Document Number	Rev
	Strip/Thermal	1C
Date: Wednesday, July 21, 2010	Sheet 21 of 46	

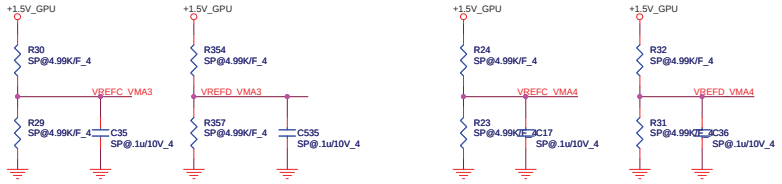
CHANNEL A: 512MB DDR3 (64M*16*4pcs)



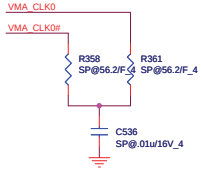
Group-A0 VREF



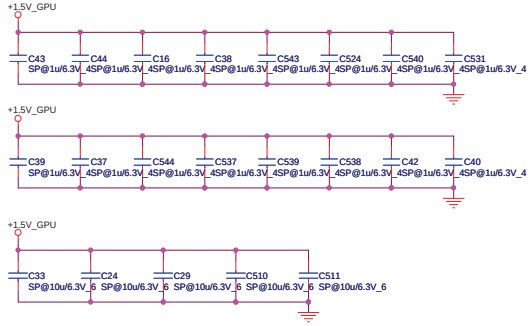
Group-A1 VREF



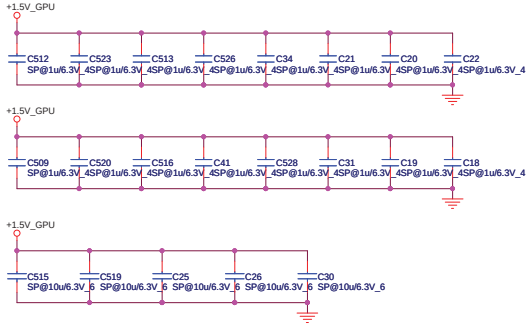
MEM_A0 CLK



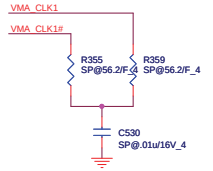
Group-A0 decoupling CAP



Group-A1 decoupling CAP



MEM_A1 CLK



Quanta Computer Inc.

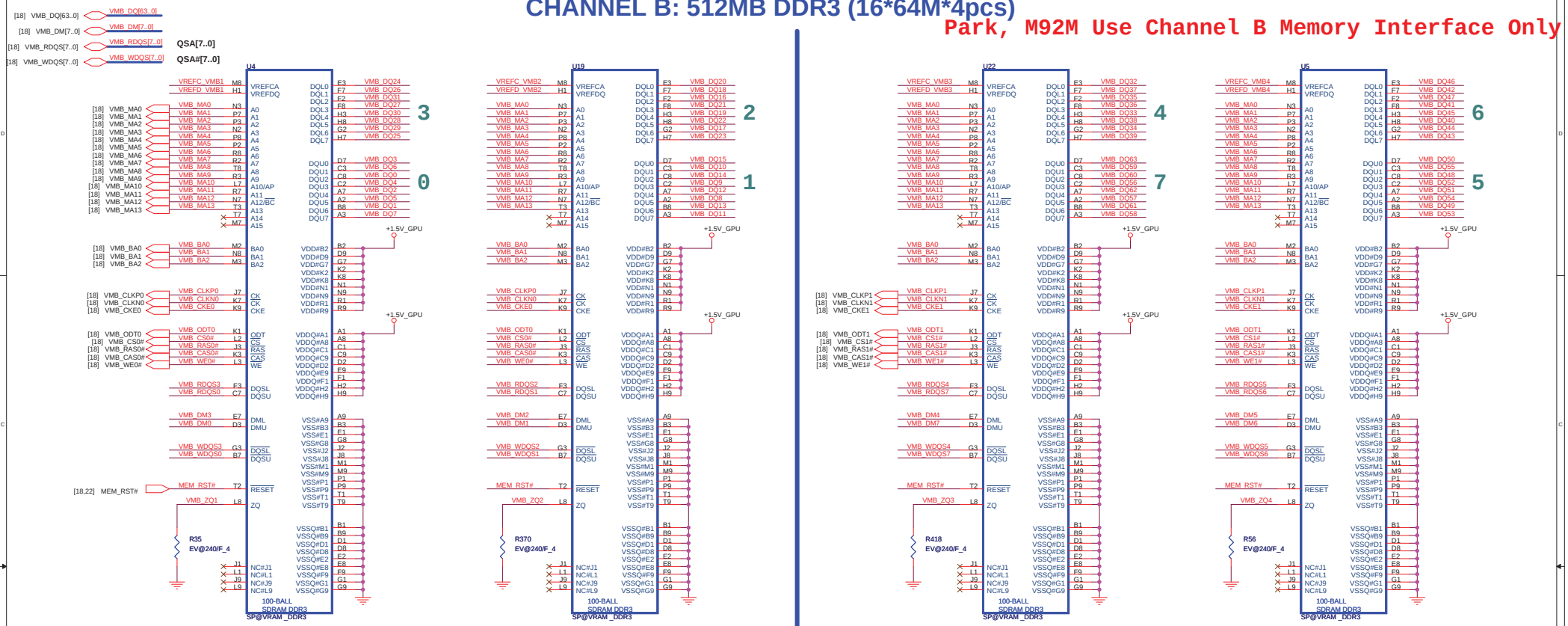
PROJECT : ZRD

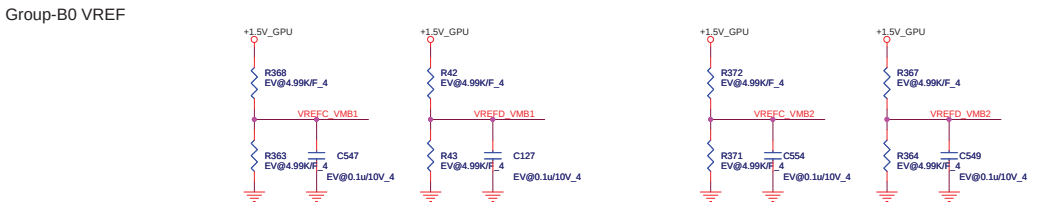
Size	Document Number	Rev
	MEMORY 1 channel A	1C

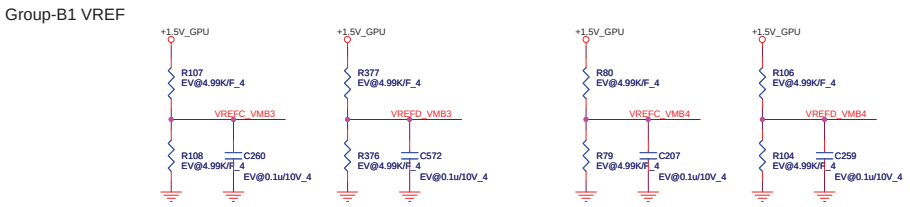
Date: Wednesday, July 21, 2010 Sheet 22 of 46

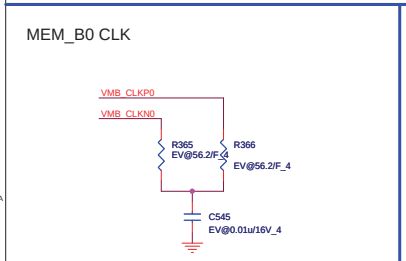
CHANNEL B: 512MB DDR3 (16*64M*4pcs)

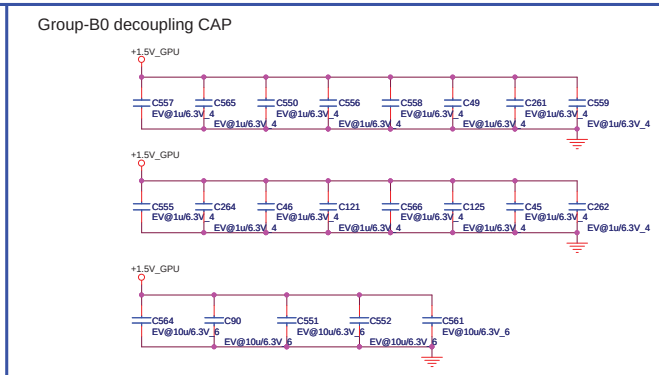
Park, M92M Use Channel B Memory Interface Only

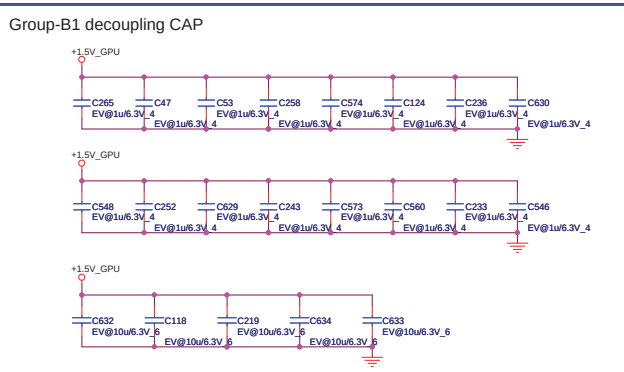


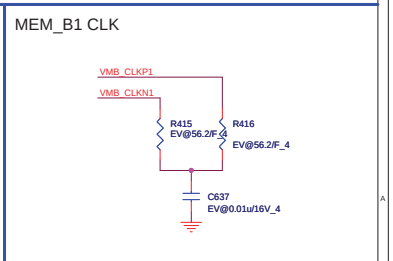












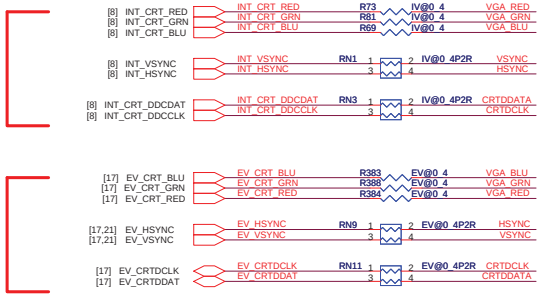
Quanta Computer Inc.

PROJECT : ZRD

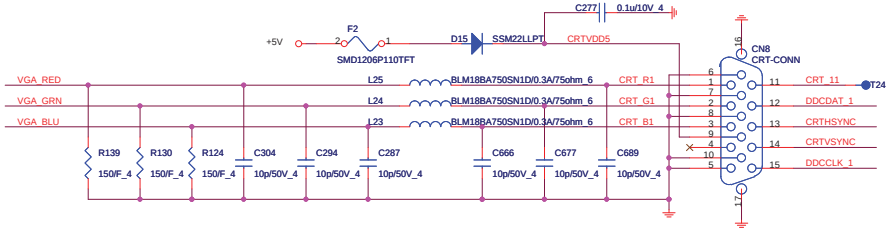
Size	Document Number	Rev
	MEMORY 2 channel B	1C
Date: Wednesday, July 21, 2010	Sheet 23 of 46	

CRT Switch

0_ohm Resistor place close to Joint-Point

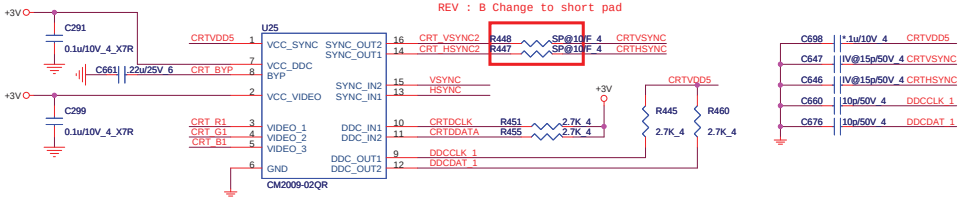


CRT



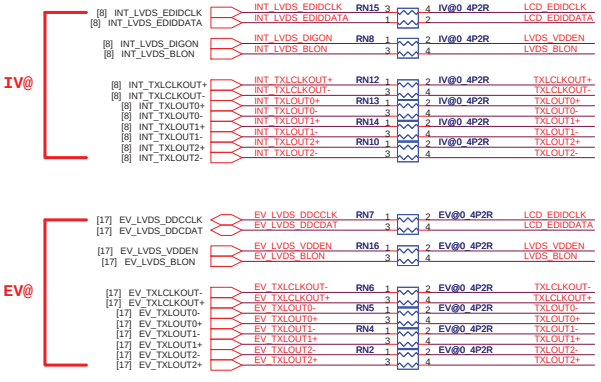
REV : C Change to 0402 R

REV : B Change to short pad



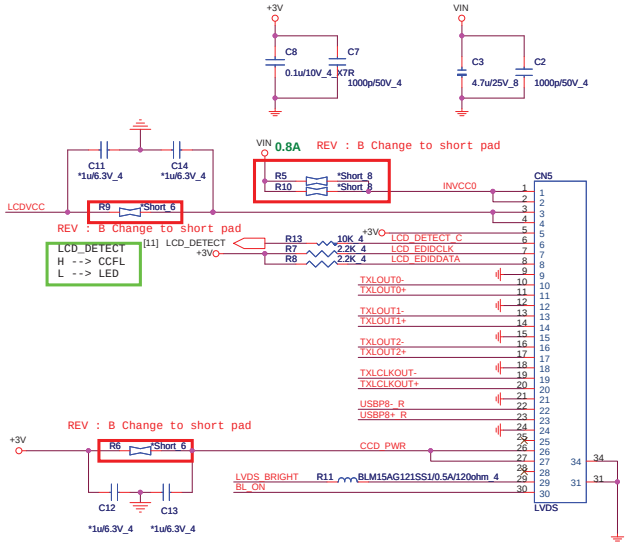
LVDS

0_ohm Resistor place close to Joint-Point

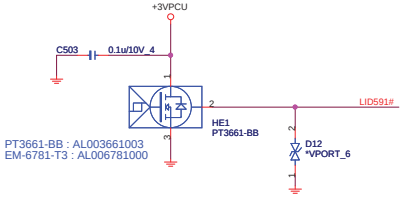


CCD +3V-current budget 0.2A

LVDS

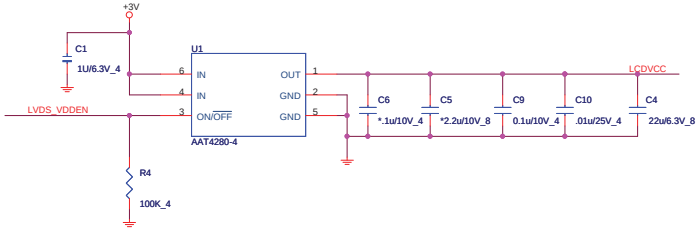


Lid Switch (Hall sensor)

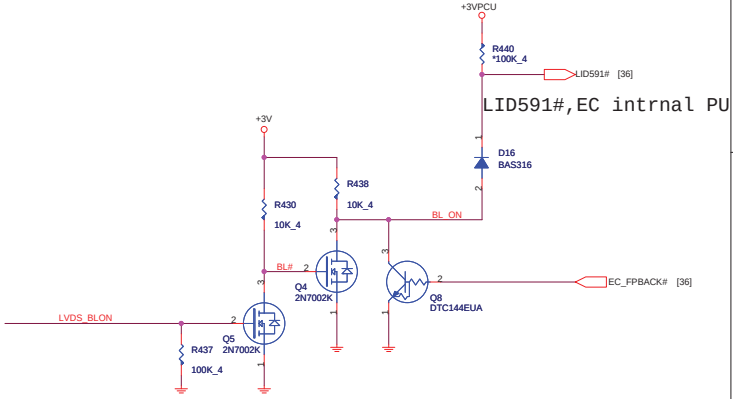


PT3661-BB : AL003661003
EM-6781-T3 : AL006781000

LCD Power



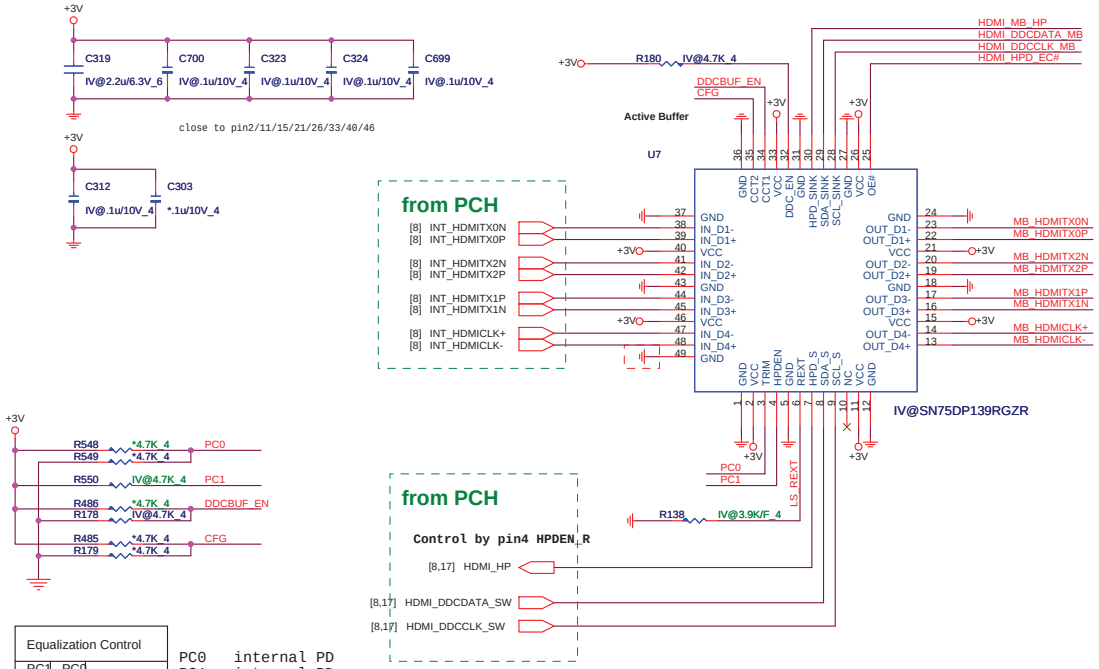
Backlight Control



Quanta Computer Inc. PROJECT : ZRD			
Size	Document Number	CRT/LVDS/CAMERA/LID	Rev 1C
Date: Wednesday, July 21, 2010	Sheet 24 of 46		

HDMI LEVEL SHIFTER

IV@

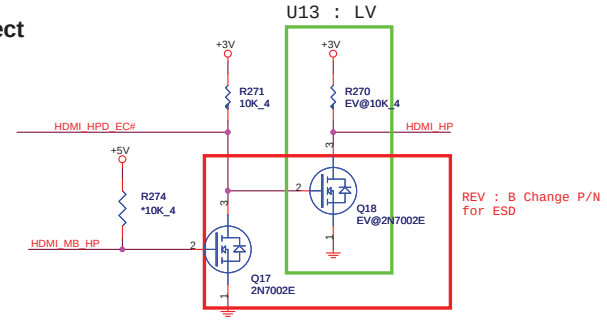


Equalization Control		
PC1 PIN4	PC0 PIN3	EQ Control
L	L	8dB
L	H	4dB
H	L	12dB
H	H	0dB

PC0 internal PD
PC1 internal PD
DDCBUF_EN internal PD
CFG internal PD
DDC_EN internal PU

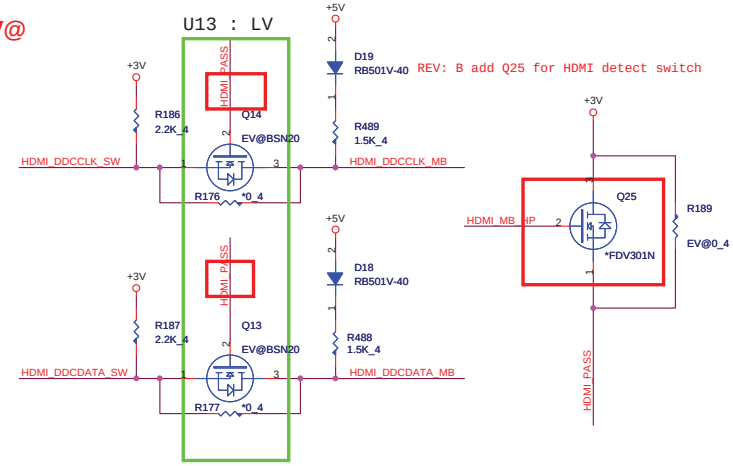
HDMI-detect

EV@



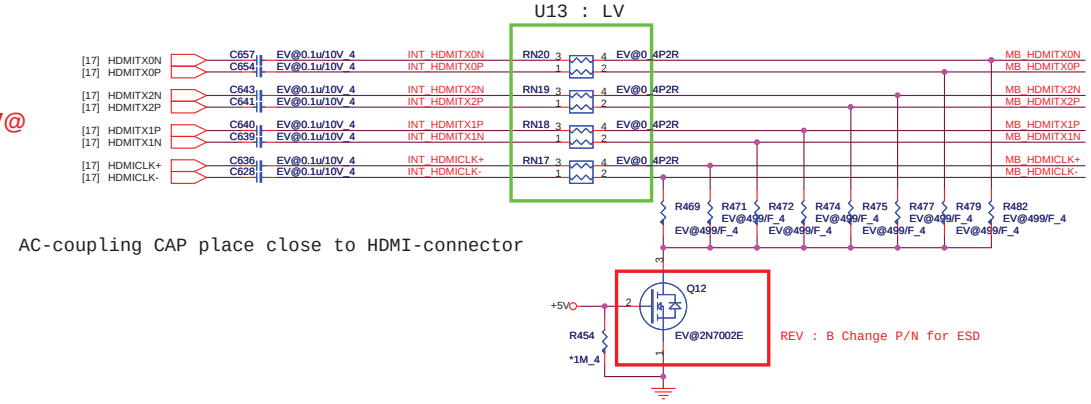
I2C

EV@



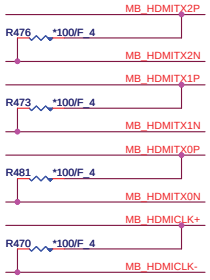
Switchable Graphic HDMI source

EV@



AC-coupling CAP place close to HDMI-connector

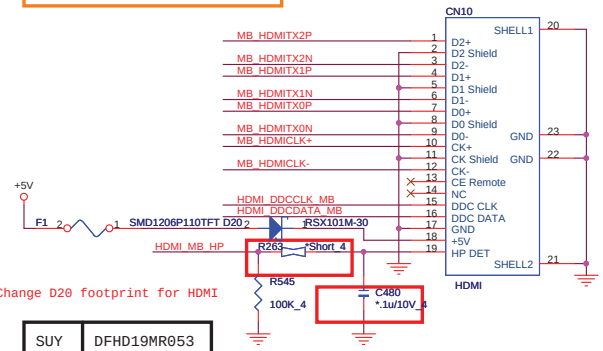
EMI



REV : C Location :D20 Change Footprint & P/N

REV C: Change D20 footprint for HDMI

HDMI connector



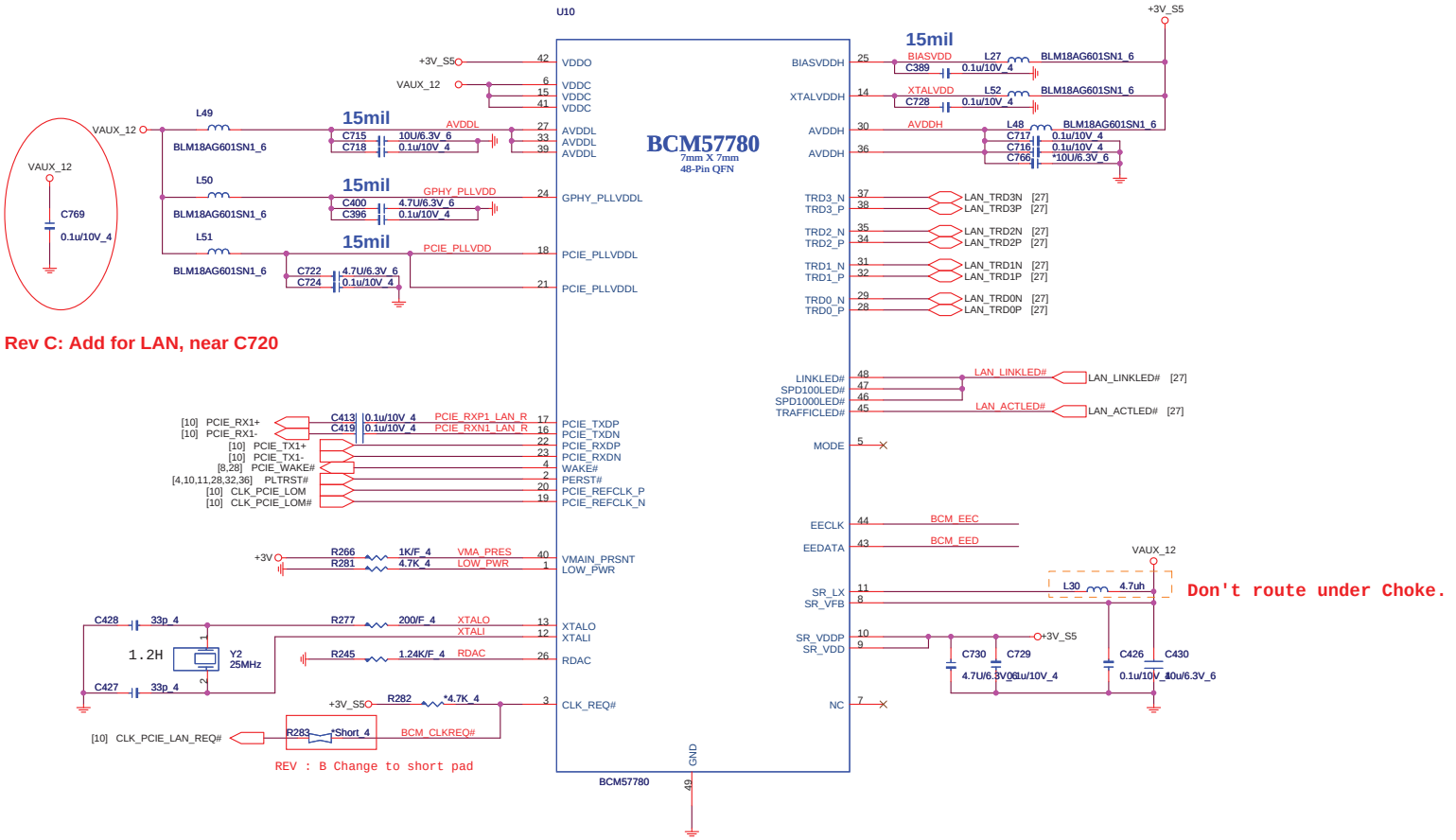
SUY	DFHD19MR053
LTS	DFHD19MR085

Quanta Computer Inc.
PROJECT : ZRD

Size	Document Number	Rev
	HDMI (PS8101)	1C

Date: Wednesday, July 21, 2010 Sheet 25 of 46

Giga-LAN BCM57780

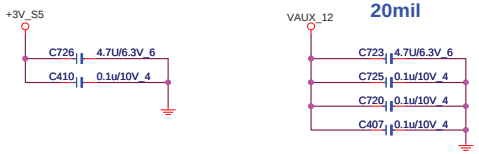


Rev C: Add for LAN, near C720

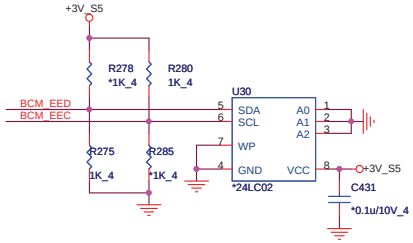
Don't route under Choke.

REV : B Change to short pad

LAN POWER



EEPROM



EEPROM Strapping

EEPROM Type	EECLK	EEDATA
24LC02	1	1
Internal	1	0

Quanta Computer Inc.

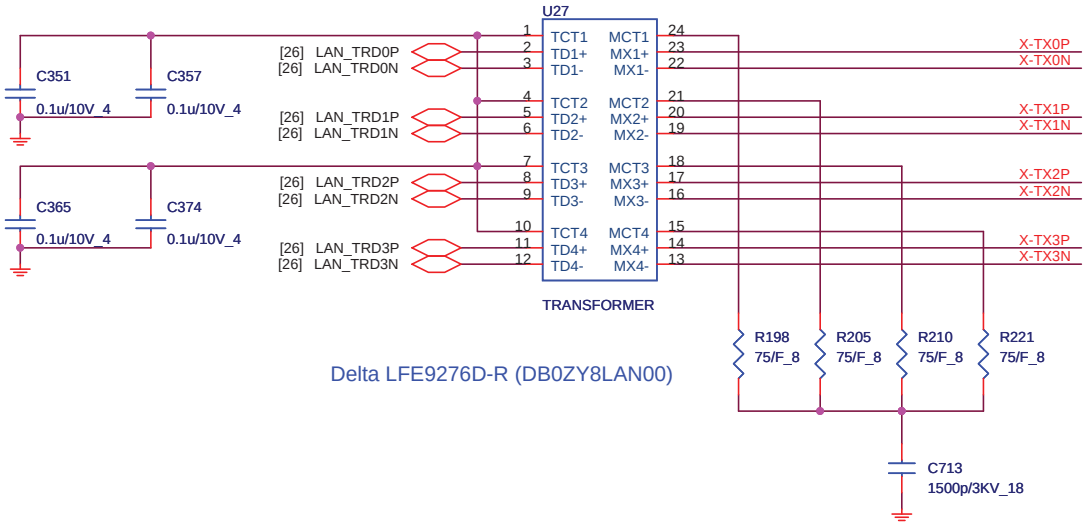
PROJECT : ZRD

Size	Document Number	Rev
	GLAN BCM57780	1C

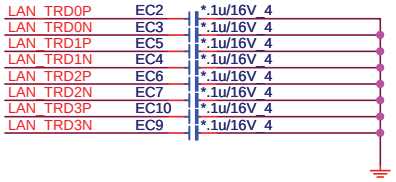
Date: Wednesday, July 21, 2010 Sheet 26 of 46

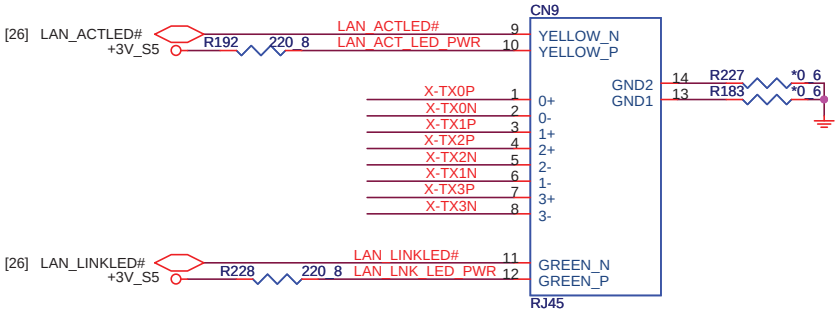
TRANSFORMER

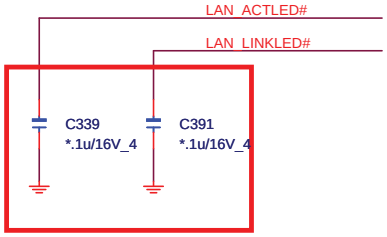
SUY	DFTJ12FR109
AEC	DFTJ12FR135



Delta LFE9276D-R (DB0ZY8LAN00)







REV : B Change to 0402 for ESD

Quanta Computer Inc.

PROJECT : ZRD

Size	Document Number	Rev
	LAN Transformer and RJ45	1C
Date: Wednesday, July 21, 2010	Sheet 27 of 46	

MINI-CARD WLAN(MPC)

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

PTI	DFHS52FR028
LTS	DFHS52FR038

REV : B Unstuff

Debug

[10] PCI_RST#
[10] CLK_LPC_DEBUG
R566 *0_4 CL_DATA1_WLAN
R294 *0_4 CL_CLK1_WLAN

H=7.0mm

CN13
LTS_AAA-PCI-046-K01

[10] CL_RST1#
[10] CL_DATA1
[10] CL_CLK1
R567 *0_4 CL_RST1#_WLAN
R565 *0_4 CL_DATA1_WLAN
R295 *0_4 CL_CLK1_WLAN

+WL_VDD

[10] PCIE_TX6+
[10] PCIE_TX6-
[10] PCIE_RX6+
[10] PCIE_RX6-
[10] CLK_PCH_SRC2
[10] CLK_PCH_SRC2#
[10] PCIE_CLK_REQ2#
PCIE_WAKE#_R

51	Reserved	+3.3V	52
49	Reserved	GND	50
47	Reserved	+1.5V	48
45	Reserved	LED_WPAN#	46
43	Reserved	LED_WLAN#	44
41	Reserved	LED_WWAN#	42
39	Reserved	GND	40
37	Reserved	USB_D+	38
35	GND	USB_D-	36
33	PETp0	GND	34
31	PETn0	SMB_DATA	32
29	GND	SMB_CLK	30
27	GND	+1.5V	28
25	PERp0	GND	26
23	PERn0	+3.3Vaux	24
21	GND	PERST#	22
19	UIM_C4	W_DISABLE#	20
17	UIM_C8	GND	18
15	GND	UIM_VPP	16
13	REFCLK+	UIM_RST	14
11	REFCLK-	UIM_CLK	12
9	GND	UIM_DATA	10
7	CLKREQ#	UIM_PWR	8
5	Reserved	+1.5V	6
3	Reserved	GND	4
1	WAKE#	+3.3V	2
53	GND	GND	54

+WL_VDD
+1.5V
RF_LED# → RF_LED# [33]
USBP13+ [10]
USBP13- [10]
CLK_SDATA [3,14,15]
CLK_SCLK [3,14,15]
PLTRST# → PLTRST# [4,10,11,26,32,36]
RF_EN [36]

Debug

A_LFRAME# R → R284 0_4 → LPC_LFRAME# [9,36]
A_LAD3_R → R279 0_4 → LPC_LAD3 [9,36]
A_LAD2_R → R276 0_4 → LPC_LAD2 [9,36]
A_LAD1_R → R273 0_4 → LPC_LAD1 [9,36]
A_LAD0_R → R272 0_4 → LPC_LAD0 [9,36]

REV B: Unstuff
REV C: stuff for SMT debug

+WL_VDD
Q3
*DTC144EUA
[8,26] PCIE_WAKE#
PCIE_WAKE#_R

+3V
R291 *Short_8 +WL_VDD
REV : B Change to short pad
C466 10u/6.3V_8
C469 0.1u/10V_4
C743 *0.1u/10V_4
C444 *0.1u/10V_4

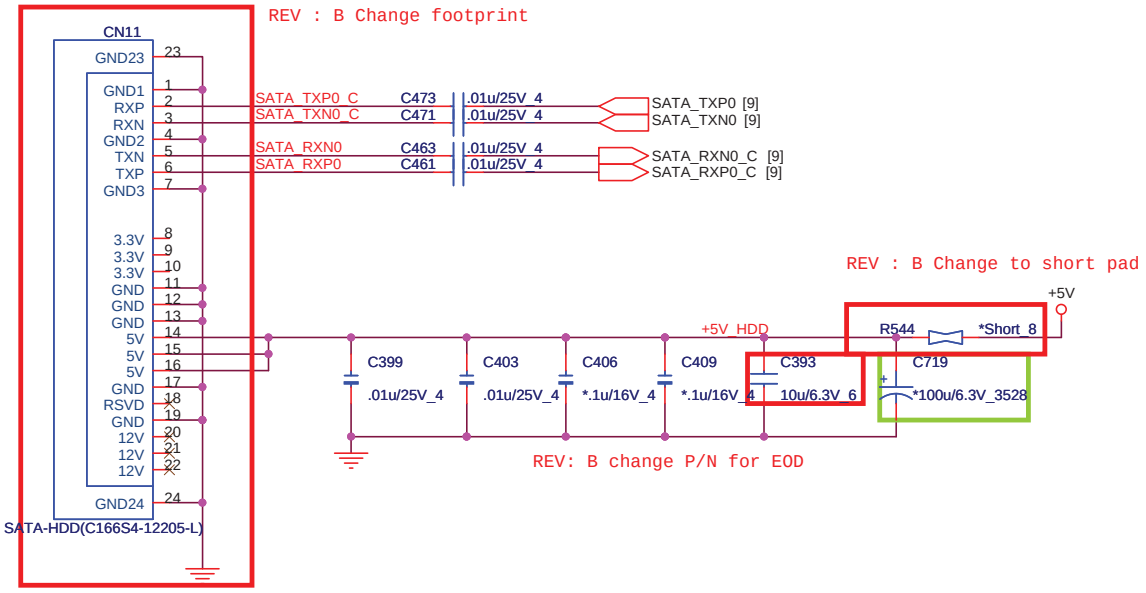
+1.5V
C742 *1000p/50V_4
C727 *0.1u/10V_4
C736 *10u/6.3V_8

Quanta Computer Inc.
PROJECT : ZRD

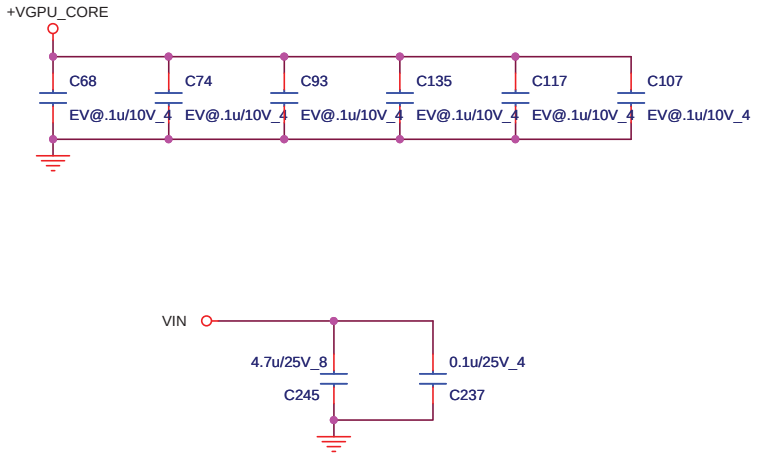
Size	Document Number	Rev
	MINI PCI-E card/TV	1C

Date: Wednesday, July 21, 2010 Sheet 28 of 46

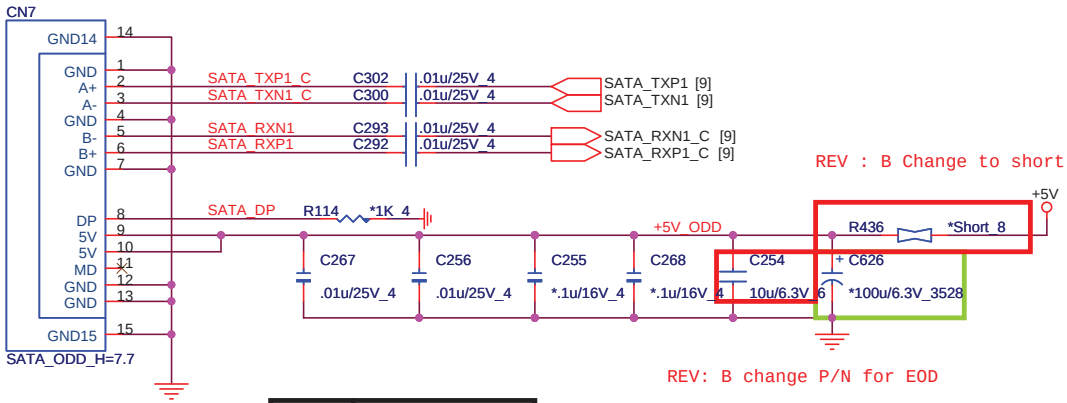
MAIN SATA HDD



EE RETURN-PATH CAPACITORS



ODD (SATA)



SUY	DFHS22FR214
AOP	DFHS22FR232
AEC	DFHS22FR216

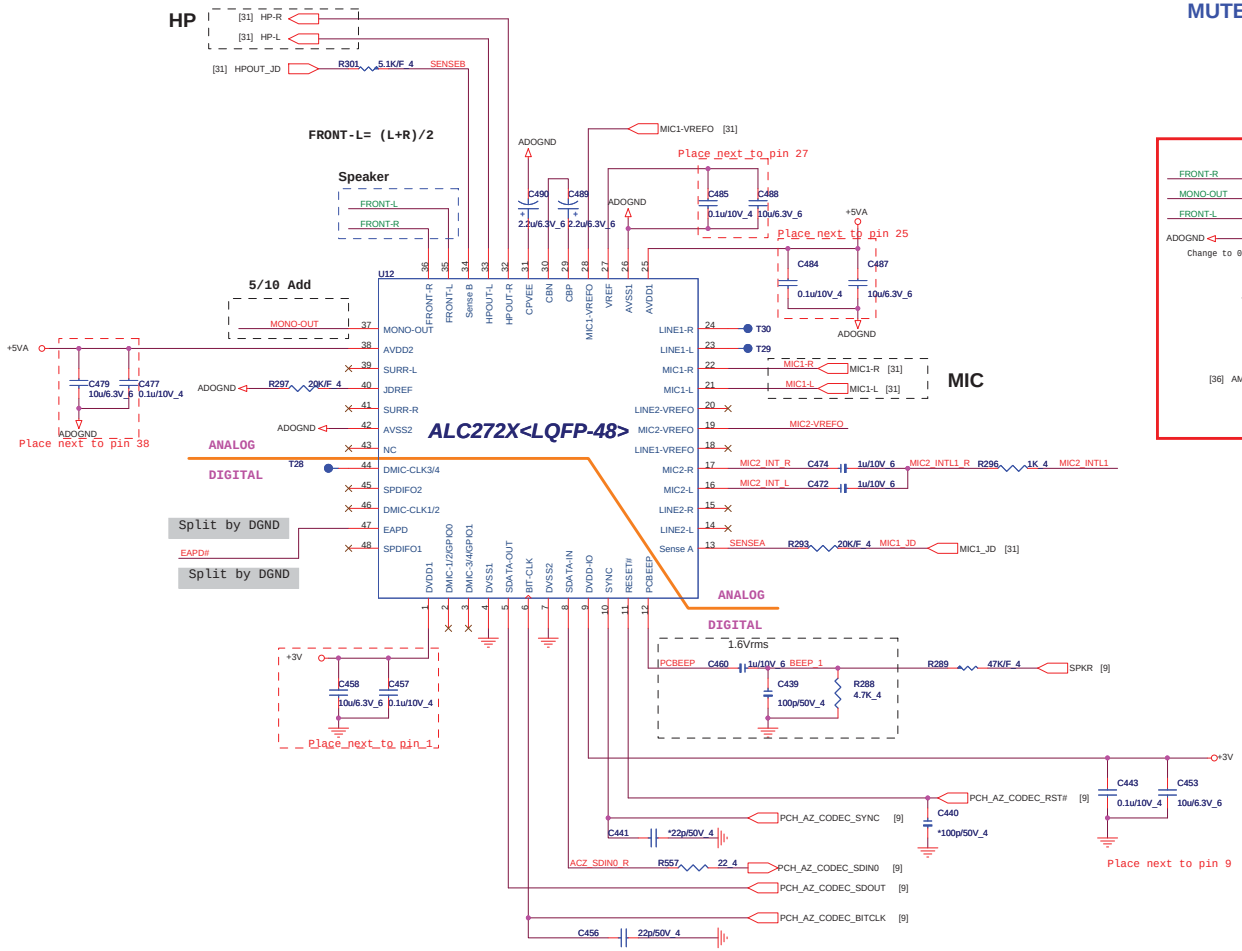
AOP	DFHS13FR011
OTK	DFHS13FR010

Quanta Computer Inc.

PROJECT : ZRD

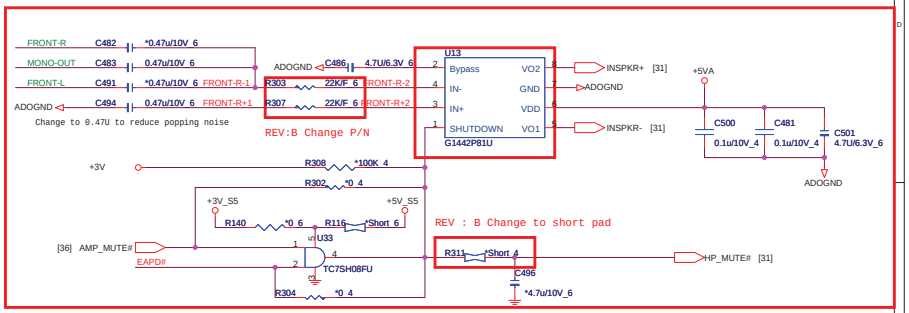
Size	Document Number	Rev
	SATA-HDD/ODD/RETURN-PATH	1C
Date: Wednesday, July 21, 2010	Sheet 29 of 46	

Codec(ADO)

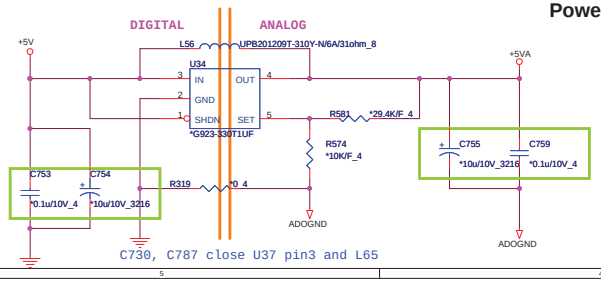


MUTE(AMP)

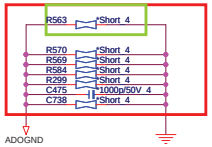
REV : B Change AMP circuit



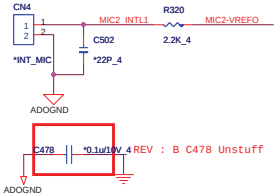
Power (ADO)



REV : B C478 Change to short pad and Stuff R563 ,R570 ,R569 ,R584 ,R299 ,C738

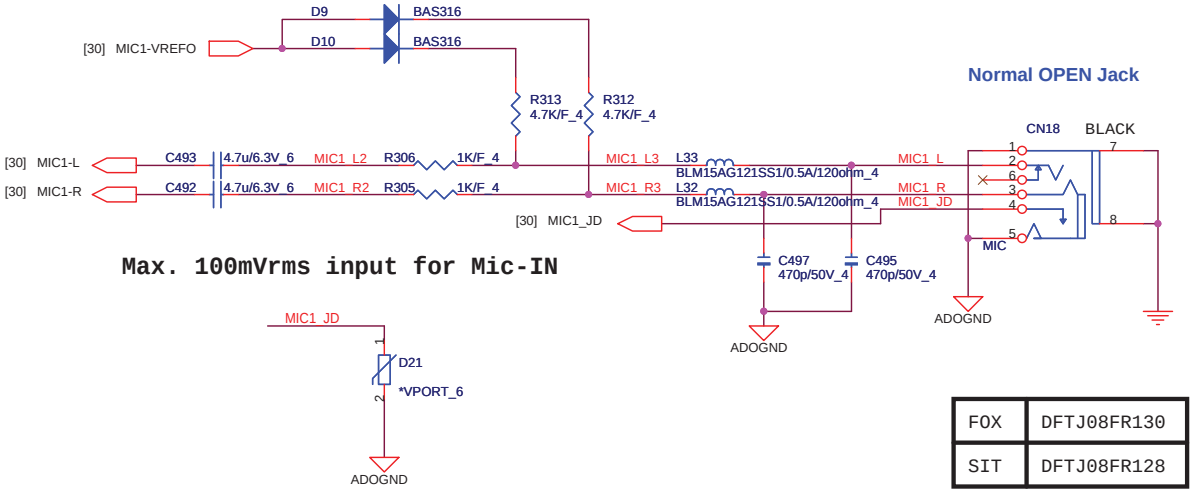


INT MIC array



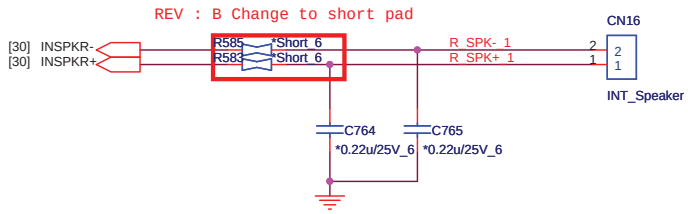
Quanta Computer Inc.		
PROJECT : ZRD		
Size	Document Number: REALTEK ALC663&888/MDC	Rev: 1C
Date: Wednesday, July 21, 2010	Sheet 30 of 46	

MIC



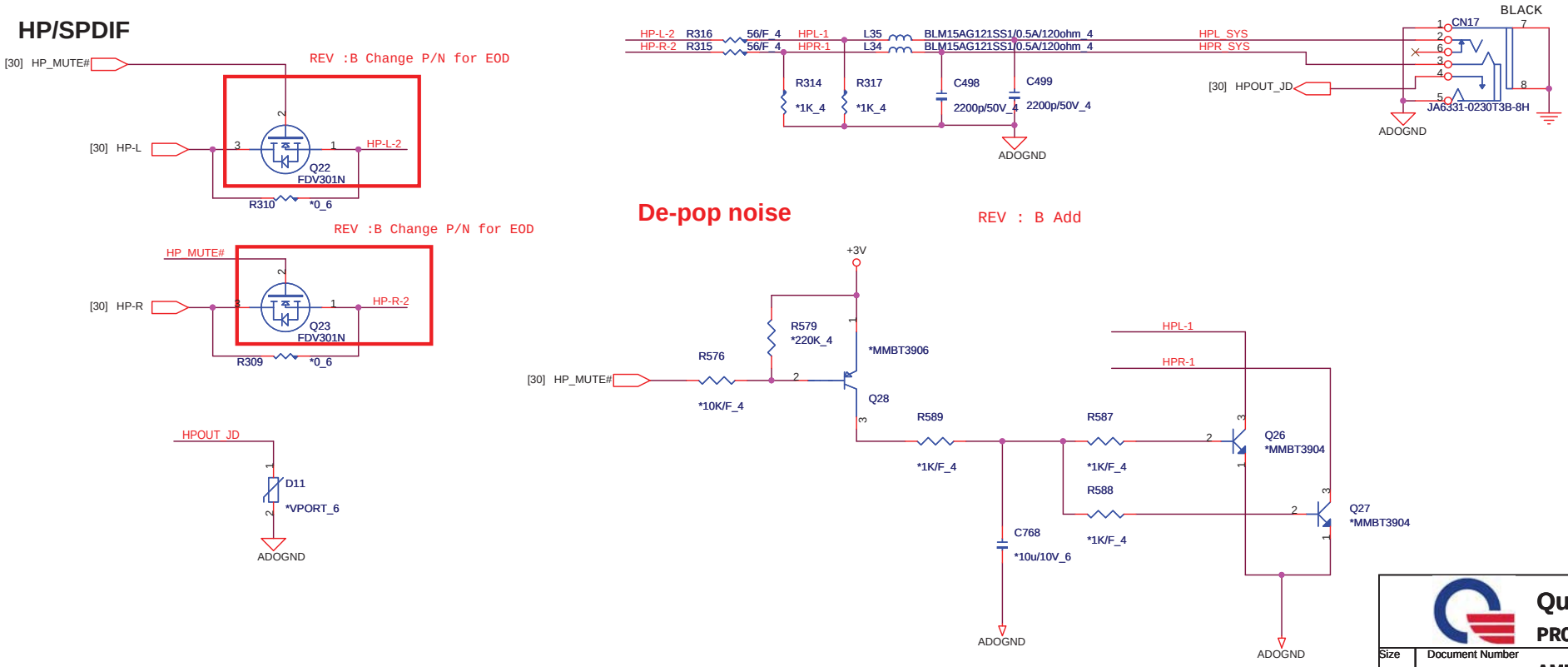
FOX	DFTJ08FR130
SIT	DFTJ08FR128

Internal Speaker



ACS	DFHD02MR311
PTI	DFHD02MR508

HP/SPDIF



Quanta Computer Inc.

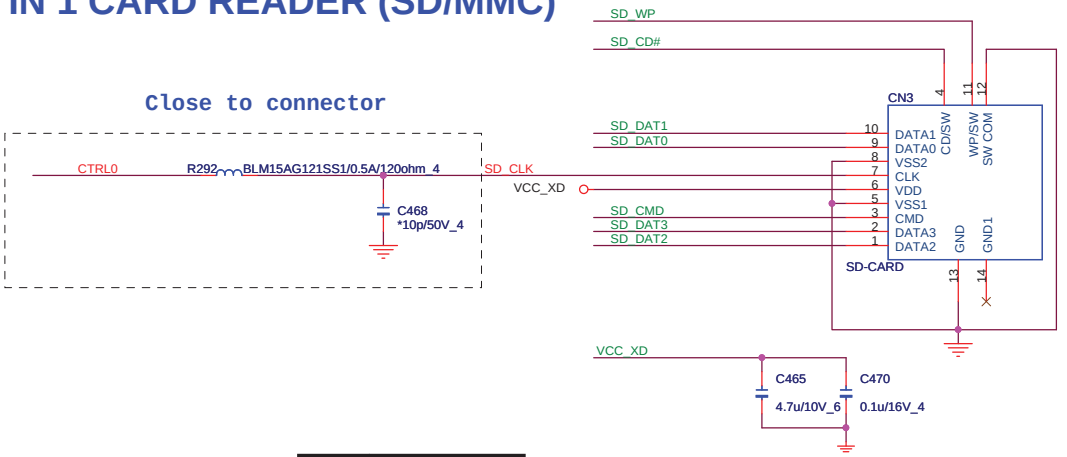
PROJECT : ZRD

Size	Document Number	Rev
	AMP /AUDIO JACK CONN	1C

Date: Wednesday, July 21, 2010 Sheet 31 of 46

CARD READER Controller

2 IN 1 CARD READER (SD/MMC)



PNT	DFHS11FR011
PLA	DFHS11FR033

Clock input selection
'1' for 48MHz input [Default,Internal PU]
'0' for 12MHz input

R571 *Short_4 XTALSEL
REV : B Change to short pad

+1.8V_VDD
+3V_VDD
C743 close PIN46, 47
C708 close PIN48, 47
C748 0.1u/16V_4
C750 0.1u/16V_4
T88
T86

R578 100K_4 +3V_VDD
[4,10,11,26,28,36] PLTRST#
R582 *0_4
C758 10u/6.3V_6
+3V
R575 *Short_6
C760 4.7u/10V_6 +3V_VDD
REV : B Change to short pad

5/10 Modify

U32
AU6437-GBL
CTRL0, CRTL 1 trace length shorter , and surround with GND.

GPON7
EXT48IN
RSTN
REXT
VD33P
DP
DM
VS33P
XI
XO
VDD
VDD

CTRL0
DATA5
CTRL2
GPI4
DATA4
DATA3
DATA2
XDWPN
GPI2
XDCEN
EEPDATA
GPI1

[10] USBP12+
[10] USBP12-
R580 330_4
C756 *5p/50V_4
C757 *5p/50V_4
XI
XO
+1.8V_VDD
8/14 C707 close PIN11, 12

crystal trace width needs at least 10 mils.
C761 18p/50V_4
C762 18p/50V_4
Y7 12MHz
R577 270K_4

8/14 pin13 output 20mils
C752 4.7u/10V_6
EEPCLK
T87
*0_4 R568

SD write protect
1:decided by SDWP[Default]
0:letting SD always write-able

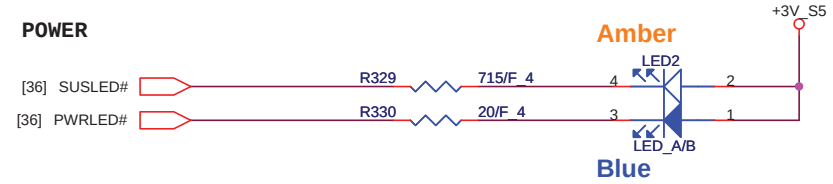
+1.8V_VDD
+3V_VDD
C745 4.7u/10V_6
C747 0.1u/16V_4

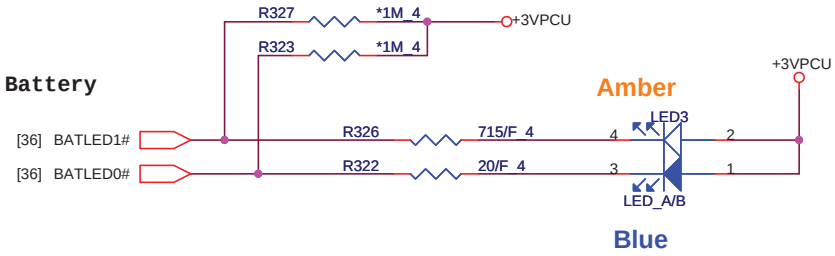
T85
T82
T83
T84

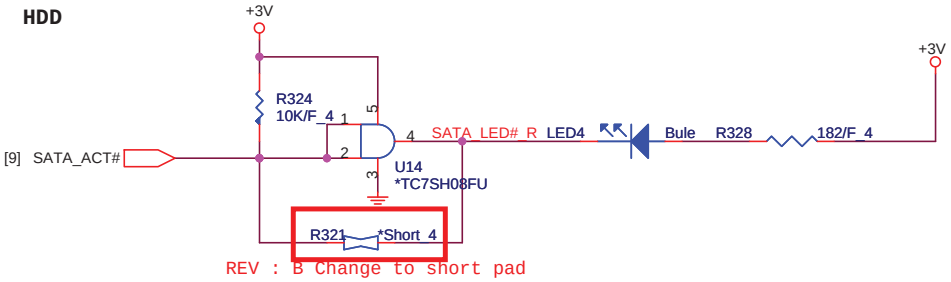
Close to CN14 pin 14 & pin23
4.7u CAP close to pin23

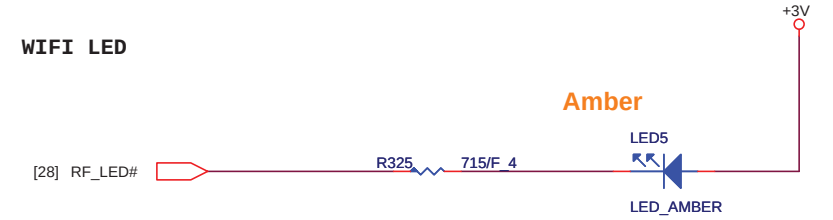
PROJECT : ZQ5 Quanta Computer Inc.			
Size	Document Number AU6433 CardReader		Rev 1C
Date:	Wednesday, July 21, 2010	Sheet 32 of 43	

LED



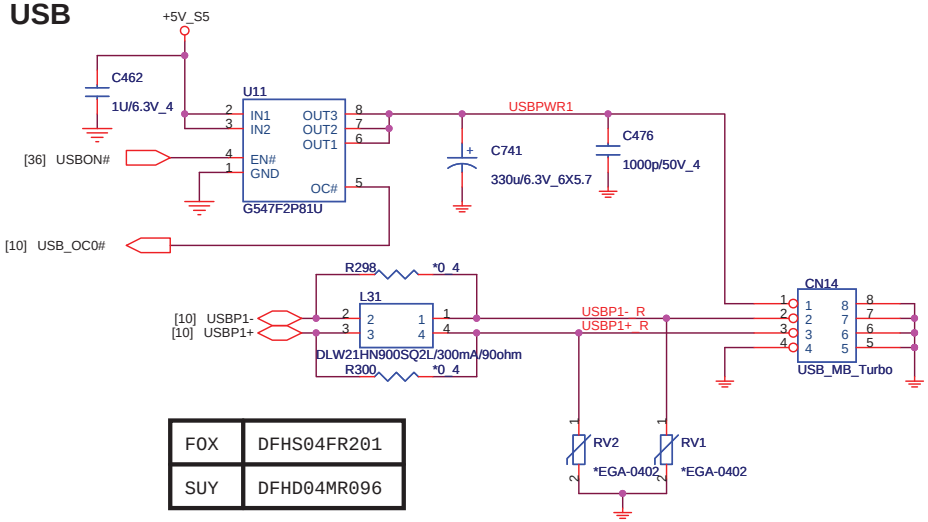






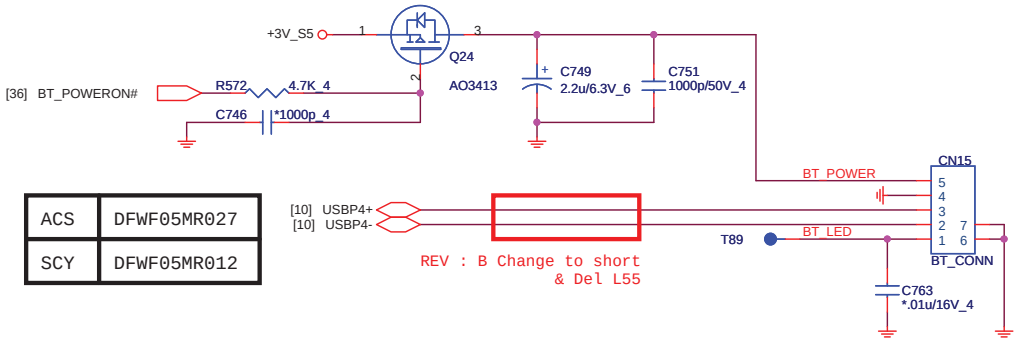
Quanta Computer Inc.		
PROJECT : ZRD		
Size	Document Number: POWER/MMB/LAUNCH/LED	Rev: 1C
Date: Wednesday, July 21, 2010	Sheet 33 of 46	

USB



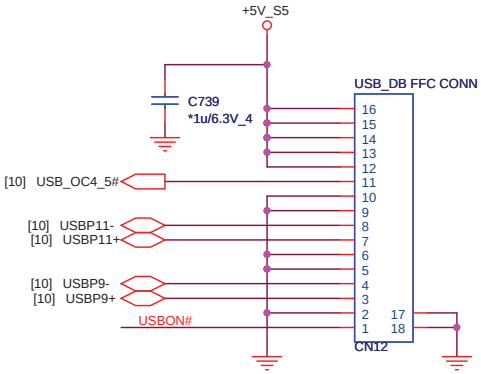
FOX	DFHS04FR201
SUY	DFHD04MR096

BLUETOOTH CONNECTOR



ACS	DFWF05MR027
SCY	DFWF05MR012

USB/B



Quanta Computer Inc.

PROJECT : ZRD

Size	Document Number	Rev
	USB/ BT	1C

Date: Wednesday, July 21, 2010 Sheet 34 of 46

K/B

PTI	DFFC26FR155
ACS	DFFC26FR014

CP1 CP2 CP6 CP5 CP4 CP3 *100p/50Vx4
C541 *100p/50V_4
C542 *100p/50V_4

CN1 KB

RP3 10K_10P8R

+3VPCU

CPU FAN

ACS	DFWF03MS091
SCY	DFWF03MS000

+5V +3V
R369 10K_4
C567 2.2U_6
U20 G995
VIN VO /FON GND VSET GND
[10,11,36] SML1ALERT#
[36] CPUFAN#
[36] FANSIG
TH_FAN_POWER
C562 2.2U_6
C563 .01U_4
C553 *.01U_4
CN6 FAN_CONN

FANPWR = 1.6*VSET

TOUCHPAD & Switch CONN.

ACS	DFFC12FR017
SCY	DFFC12FR015
PTI	DFFC12FR234

+5V
R44 10K_4
R45 10K_4
L5 *Short_6 +TPVDD
C150 0.1u/10V_4
REV : B Change to short pad
[36] TPDATA
[36] TPCLK
L6 *Short_6
L7 *Short_6
C143 *.01u/25V_4
C144 *.01u/25V_4
TPDATA_R
TPCLK_R
RIGHT#
LEFT#
CN2 Aces 88501-120N
SW3 SWITCH_1.5
SW2 SWITCH_1.5

HOLE4 H-C315i154D154P2
HOLE10 H-TC197BC122D122P2
HOLE24 *h-c315in158d118p2
HOLE5 *h-c315d118p2
HOLE7 *h-c315d118p2
HOLE31 *h-c315d118p2
HOLE26 *h-c315d118p2
HOLE30 *h-c315d118p2
HOLE11 H-TC197BC122D122P2
HOLE17 H-TC197BC122D122P2
HOLE13 *h-c315d118p2
HOLE32 *h-c315d118p2
HOLE3 *h-c315d118p2
HOLE16 *h-c315d118p2
HOLE29 *h-c315d118p2
HOLE22 *h-c315d118p2
HOLE18 h-c315d146p2
HOLE25 H-TC315BC146D146P2
HOLE14 *H-TC165BC256D165P2
HOLE21 *H-TC165BC256D165P2
HOLE20 *H-TC165BC256D165P2
HOLE27 h-c197d87p2
HOLE1 h-tc197bc79d79p2
HOLE2 h-tc197bc102d102p2
HOLE9 *h-o315x354d315x354n
HOLE19 *H-TC91BC197D91P2
HOLE15 *H-TC91BC197D91P2
HOLE23 *H-TC91BC197D91P2
HOLE28 *H-TC91BC197D91P2
+1.05V
*SPAD3
PAD3

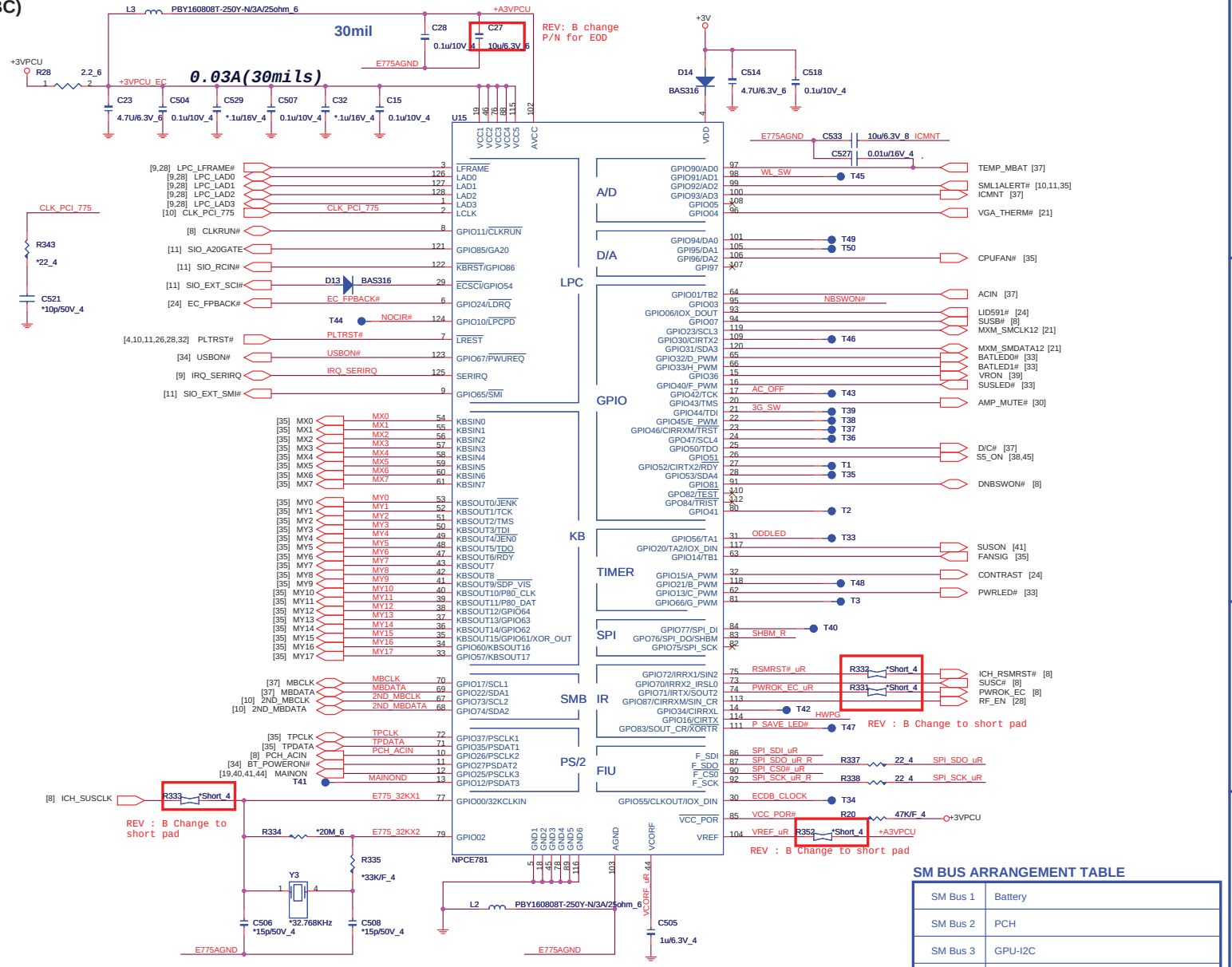
HOLE12 *h-c315d118p2
HOLE6 *h-c94d94n
HOLE8 *h-c1417d1417na1457

Quanta Computer Inc.
PROJECT : ZRD

Size	Document Number	Rev
	KB/FAN/TP+FP	1C

Date: Wednesday, July 21, 2010 Sheet 35 of 46

EC(KBC)



SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	GPU-I2C
SM Bus 4	N/A

I/O ADDRESS SETTING(KBC)

SHBM=0: Enable shared memory with host BIOS

SHBM R336 *10K_4

1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

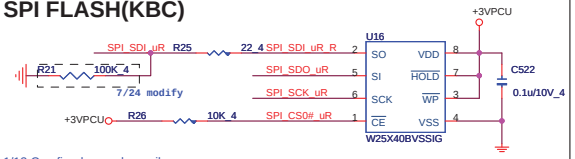
SM BUS PU(KBC)

+3VPCU
MBCLK R19 10K_4
MBDATA R18 10K_4

+3V_D_S
MXM_SMCLK12 R350 EV@2.2K_4
MXM_SMDATA12 R351 EV@2.2K_4

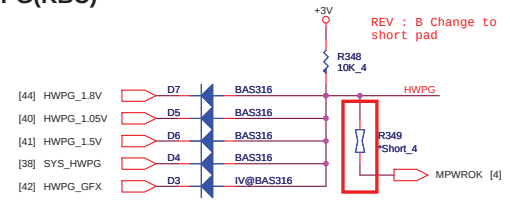
+3V
2ND_MBCLK R16 10K_4
2ND_MBDATA R17 10K_4
VGA_THERM# R342 EV@10K_4

SPI FLASH(KBC)

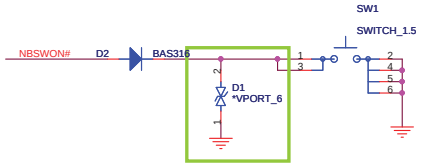


1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

HWPG(KBC)



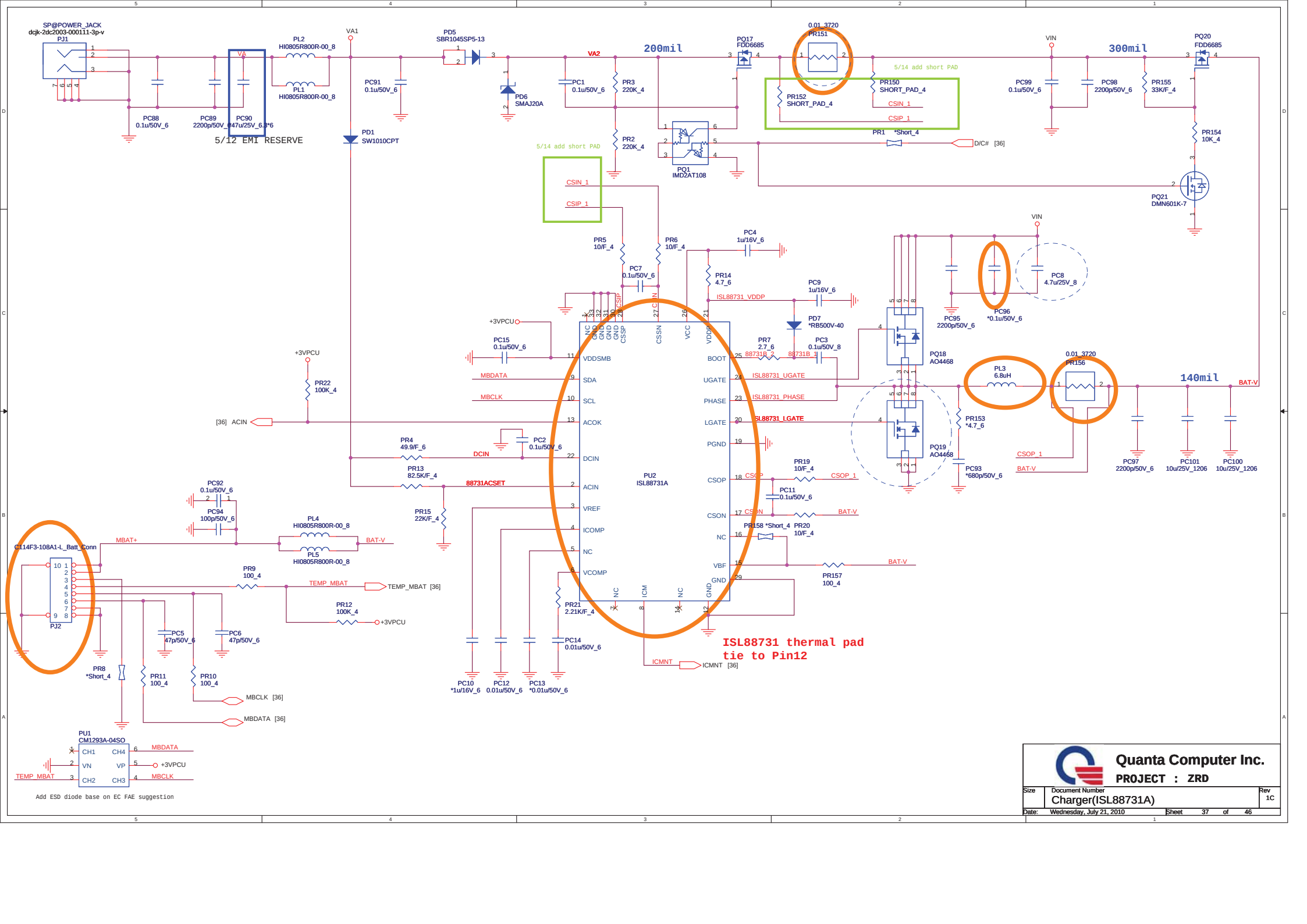
POWER-ON Switch(KBC)



INTERNAL KEYBOARD STRIP SET(KBC)

+3VPCU
MY0 R362 10K_4

Quanta Computer Inc.			
PROJECT : ZRD			
Size	Document Number		Rev
	WPCE781 & FLASH		1C
Date: Wednesday, July 21, 2010		Sheet 36 of 46	

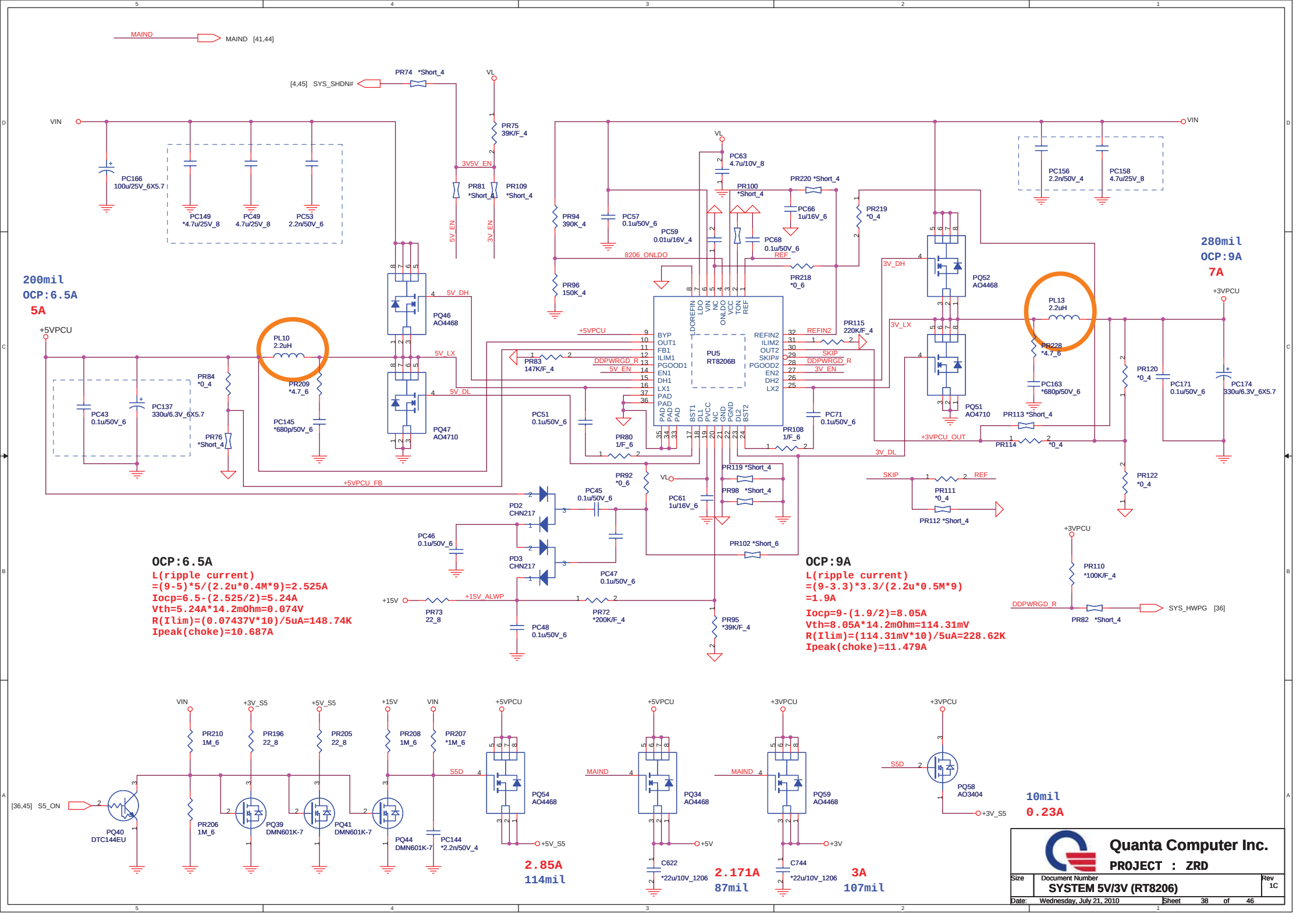


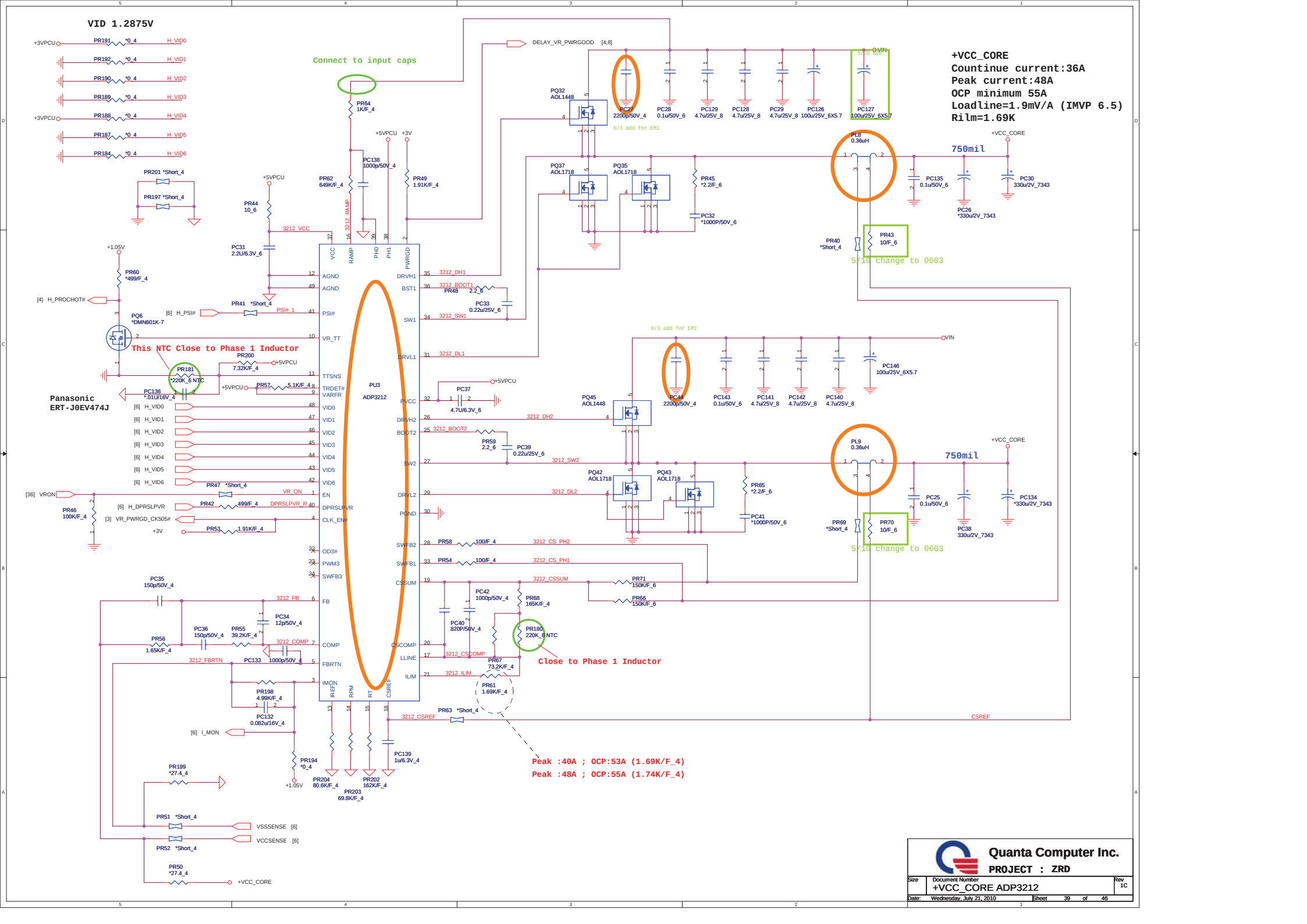
Quanta Computer Inc.

PROJECT : ZRD

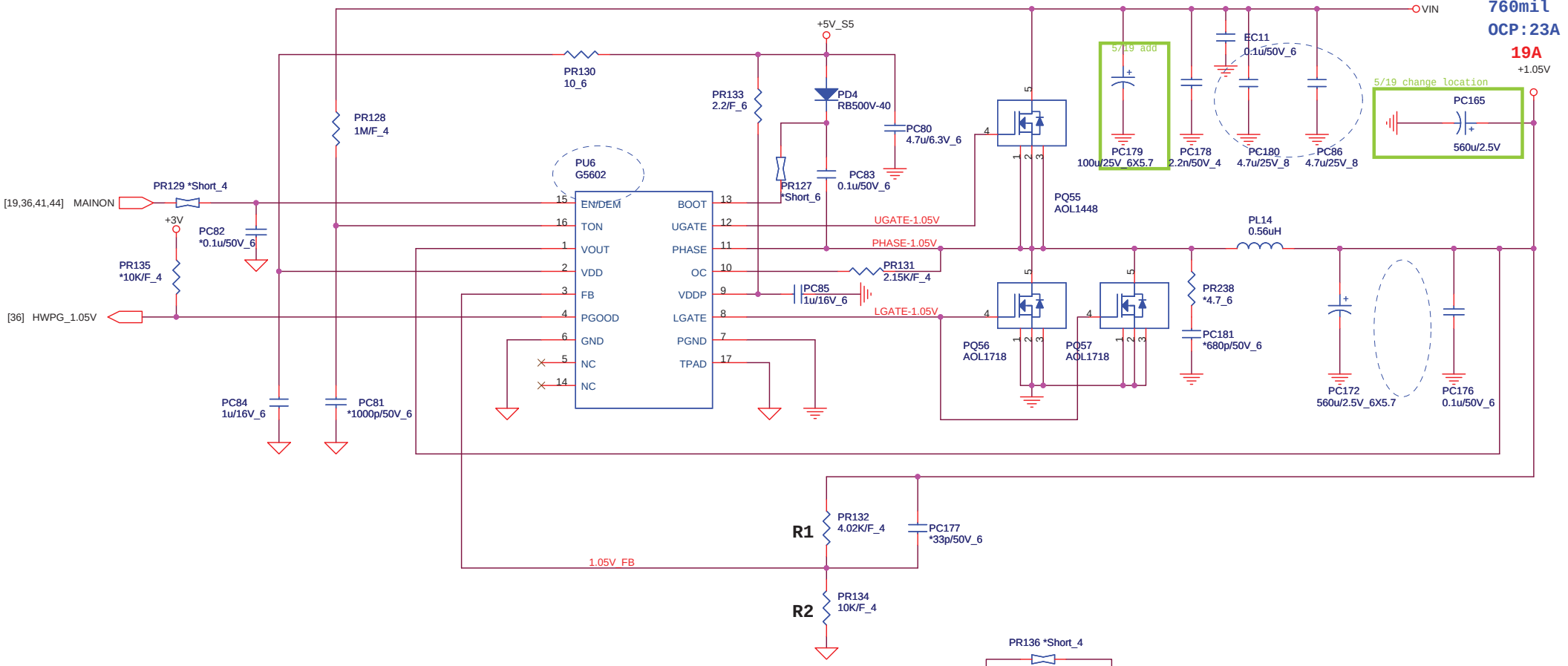
Size	Document Number	Rev
	Charger(ISL88731A)	1C

Date: Wednesday, July 21, 2010 Sheet 37 of 46


MAIND
MAIND [41,44]
[4,45] SYS_SHDN#
PR74 *Short_4
VL
PR75 39K/F_4
3V5V_EN
PR81 *Short_4
PR109 *Short_4
5V_EN
3V_EN
VIN
PC166 100u/25V_6X5.7
PC149 *4.7u/25V_8
PC49 4.7u/25V_8
PC53 2.2n/50V_6
200mil
OCP:6.5A
5A
+5VPCU
PL10 2.2uH
PR84 *0_4
PR209 *4.7_6
PC43 0.1u/50V_6
PC137 330u/6.3V_6X5.7
PC145 *680p/50V_6
PR76 *Short_4
PQ46 AO4468
PQ47 AO4710
5V_DH
5V_LX
5V_DL
+5VPCU_FB
PC63 4.7u/10V_8
PR100 *Short_4
PR220 *Short_4
PC66 1u/16V_6
PC68 0.1u/50V_6
PR94 390K_4
PC57 0.1u/50V_6
PC59 0.01u/16V_4
PR96 150K_4
8206_ONLDO
REF
PR218 *0_6
PR219 *0_4
PU5 RT8206B
LDOREFIN LDO VIN NC ONLDO VCC TON REF
BYP OUT1 FB1 ILIM1 PGOOD1 EN1 DH1 LX1 PAD PAD PAD PAD
REFIN2 ILIM2 OUT2 SKIP# PGOOD2 EN2 DH2 LX2
BST1 DL1 PVCC NC GND PGND DL2 BST2
PR83 147K/F_4
DDPWRGD_R
PR115 220K/F_4
REFIN2
SKIP
3V_EN
PC51 0.1u/50V_6
PR80 1/F_6
PC71 0.1u/50V_6
PR108 1/F_6
PR92 *0_6
PR119 *Short_4
PR98 *Short_4
PC61 1u/16V_6
PC45 0.1u/50V_6
PC46 0.1u/50V_6
PC47 0.1u/50V_6
PD2 CHN217
PD3 CHN217
PR102 *Short_6
+15V
+15V_ALWP
PR73 22_8
PR72 *200K/F_4
PC48 0.1u/50V_6
PR95 *39K/F_4
OCP:6.5A
L(ripple current)
=(9-5)*5/(2.2u*0.4M*9)=2.525A
Iocp=6.5-(2.525/2)=5.24A
Vth=5.24A*14.2mOhm=0.074V
R(Ilim)=(0.07437V*10)/5uA=148.74K
Ipeak(choke)=10.687A
280mil
OCP:9A
7A
PC156 2.2n/50V_4
PC158 4.7u/25V_8
3V_DH
3V_LX
PQ52 AO4468
PQ51 AO4710
PL13 2.2uH
PR228 *4.7_6
PC163 *680p/50V_6
PR113 *Short_4
PR114 *0_4
+3VPCU_OUT
3V_DL
PR120 *0_4
PC171 0.1u/50V_6
PC174 330u/6.3V_6X5.7
PR122 *0_4
SKIP
REF
PR111 *0_4
PR112 *Short_4
OCP:9A
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.5M*9)
=1.9A
Iocp=9-(1.9/2)=8.05A
Vth=8.05A*14.2mOhm=114.31mV
R(Ilim)=(114.31mV*10)/5uA=228.62K
Ipeak(choke)=11.479A
PR110 *100K/F_4
DDPWRGD_R
PR82 *Short_4
SYS_HWPG [36]
[36,45] S5_ON
PQ40 DTC144EU
PR210 1M_6
PR206 1M_6
PR196 22_8
PQ39 DMN601K-7
PR205 22_8
PQ41 DMN601K-7
PR208 1M_6
PQ44 DMN601K-7
PR207 *1M_6
PC144 *2.2n/50V_4
S5D
PQ54 AO4468
+5V_S5
2.85A
114mil
MAIND
PQ34 AO4468
+5V
C622 *22u/10V_1206
2.171A
87mil
PQ59 AO4468
+3V
C744 *22u/10V_1206
3A
107mil
PQ58 AO3404
+3V_S5
10mil
0.23A
Quanta Computer Inc.
PROJECT : ZRD
Size
Document Number
SYSTEM 5V/3V (RT8206)
Rev 1C
Date: Wednesday, July 21, 2010
Sheet 38 of 46


VID 1.2875V
Connect to input caps
+VCC_CORE
Countinue current:36A
Peak current:48A
OCP minimum 55A
Loadline=1.9mV/A (IMVP 6.5)
Rilm=1.69K
This NTC Close to Phase 1 Inductor
Close to Phase 1 Inductor
Panasonic
ERT-J0EV474J
PU3
ADP3212
750mil
5/19 change to 0603
6/3 add for EMI
Peak :40A ; OCP:53A (1.69K/F_4)
Peak :48A ; OCP:55A (1.74K/F_4)
Quanta Computer Inc.
PROJECT : ZRD
+VCC_CORE ADP3212
Wednesday, July 21, 2010

[PWM]



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AO1718 Rdson=3~4.3mOhm

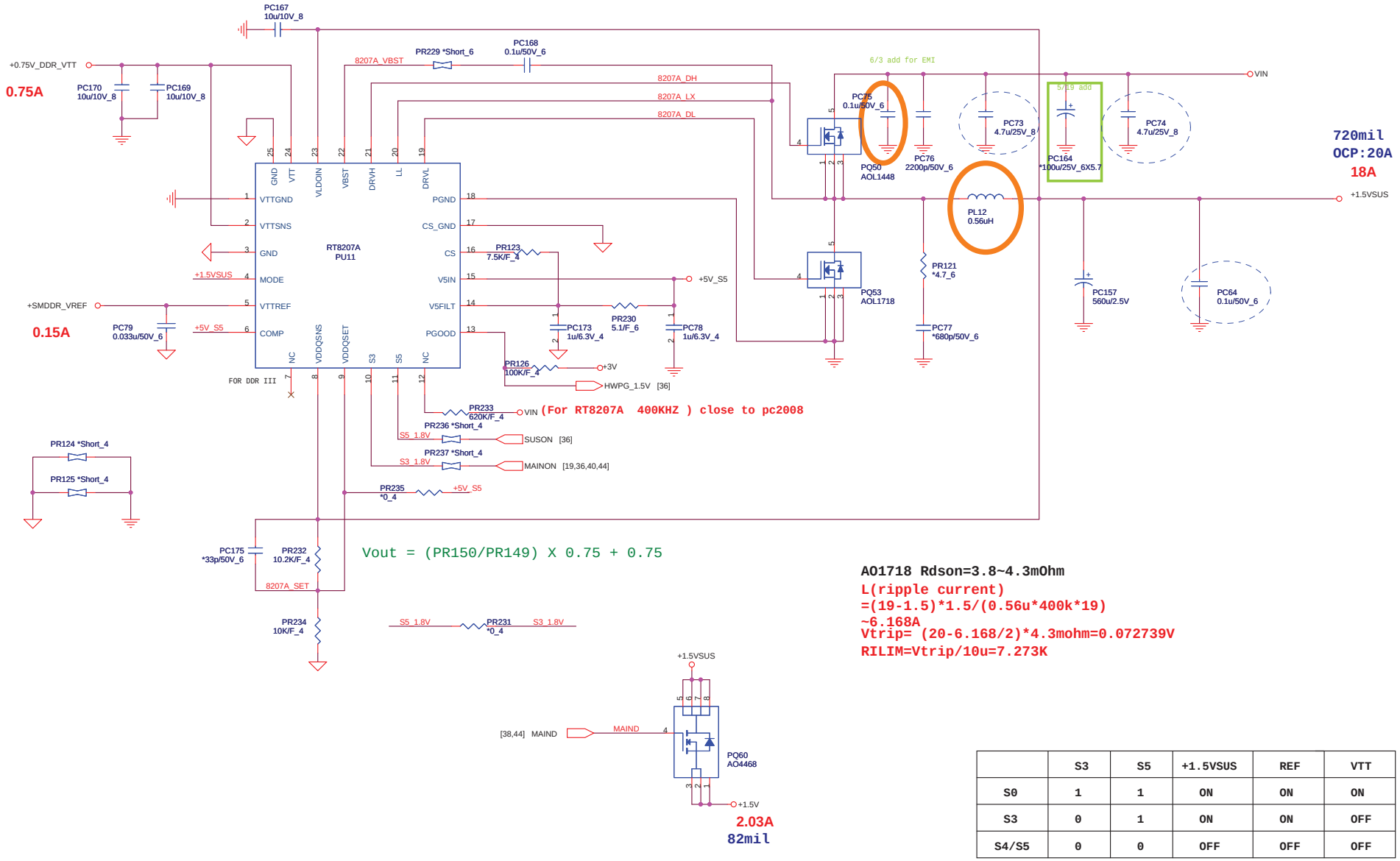
L(ripple current)
=(19-1.05)*1.05/(0.56u*272k*19)
~6.512A

RILIM=2.15mohm*23-3.256/20uA=2.122Kohm

I(choke)peak=29.512A

Quanta Computer Inc.		
PROJECT : ZRD		
Size	Document Number: +VTT (UP6111A)	Rev: 1C
Date: Wednesday, July 21, 2010	Sheet 40 of 46	

[PWM]



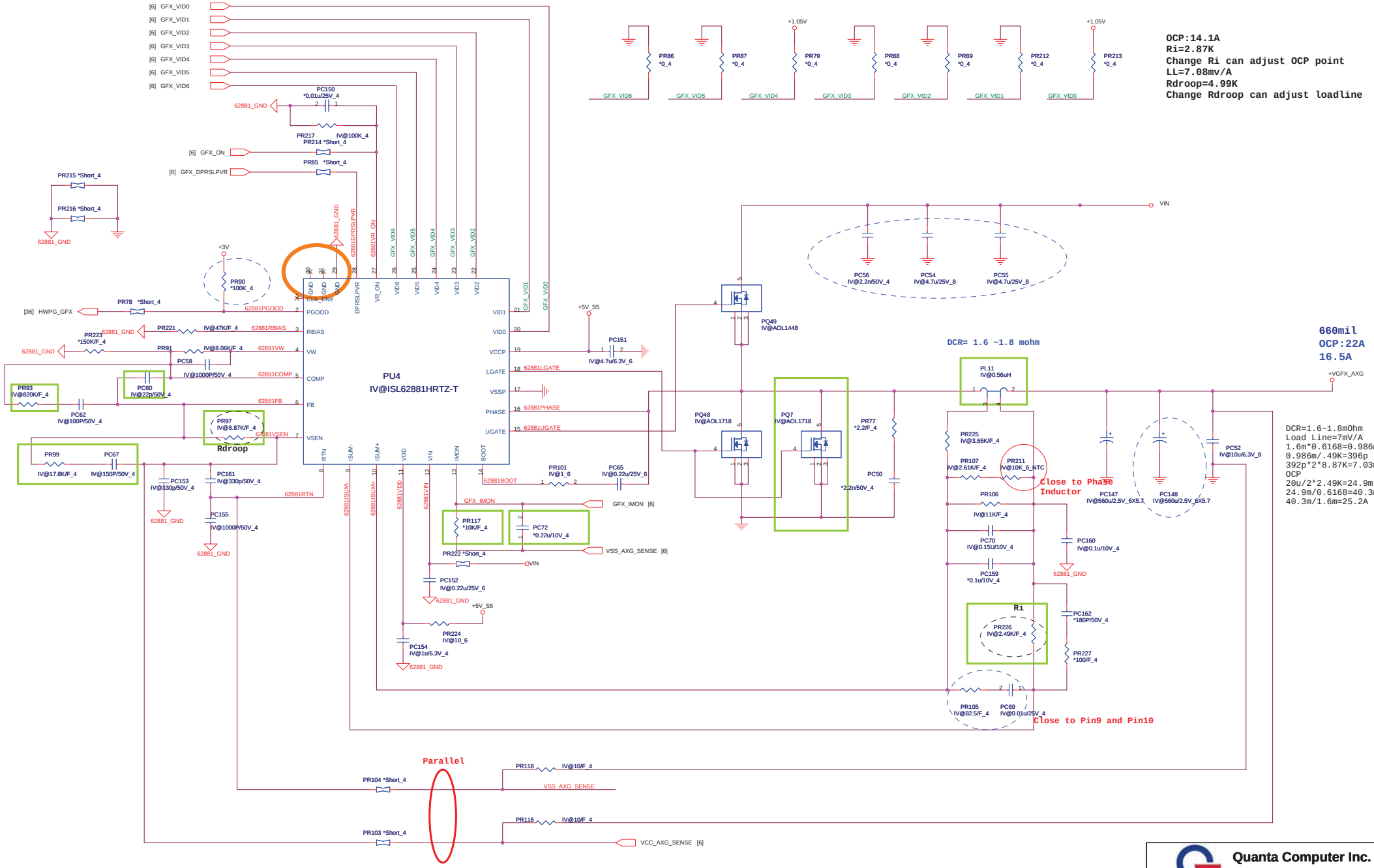
	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

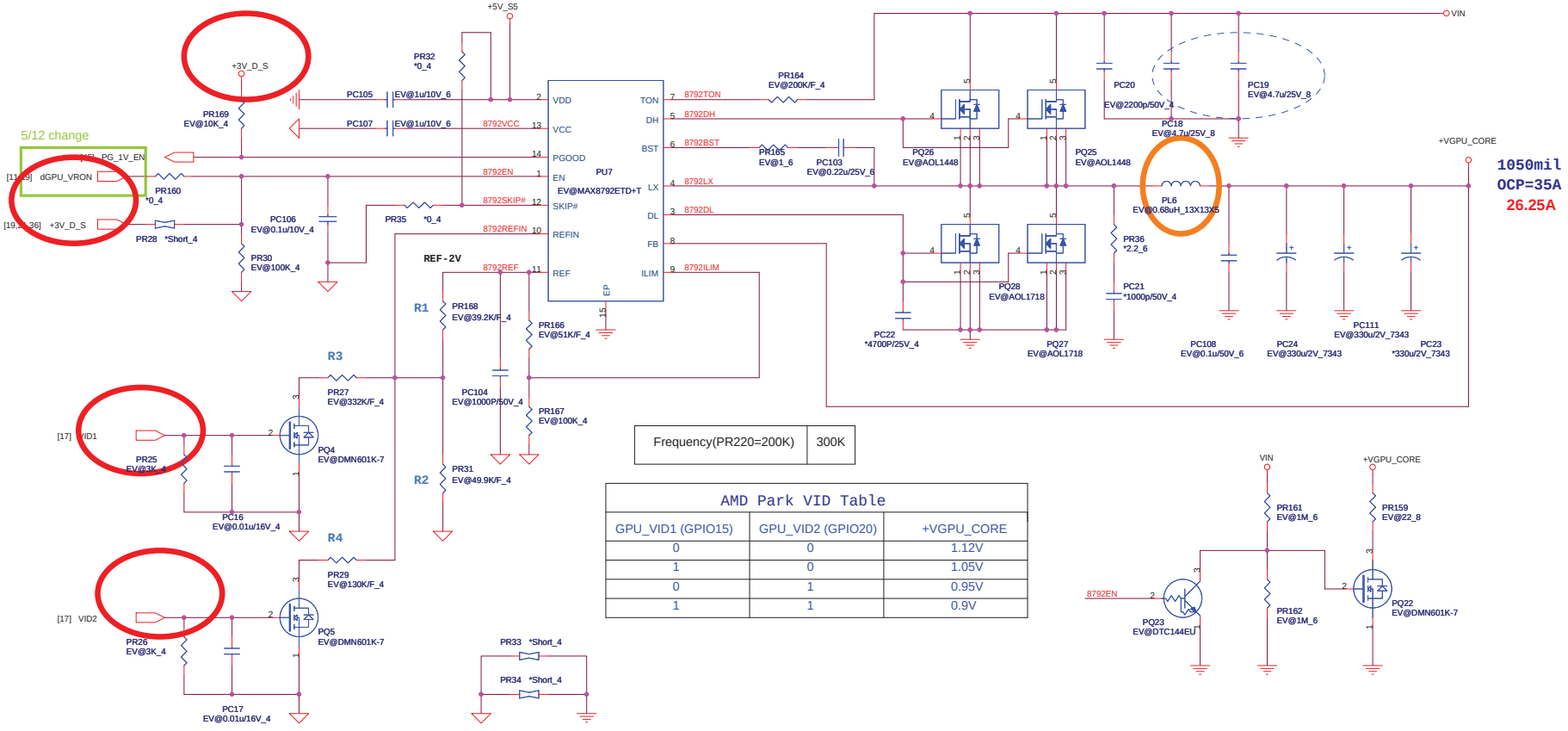
Quanta Computer Inc.
PROJECT : ZRD

Size	Document Number	Rev
	DDR 1.5V(RT8207A)	1C

Date: Wednesday, July 21, 2010 Sheet 41 of 46

Int_VGA [PWM]





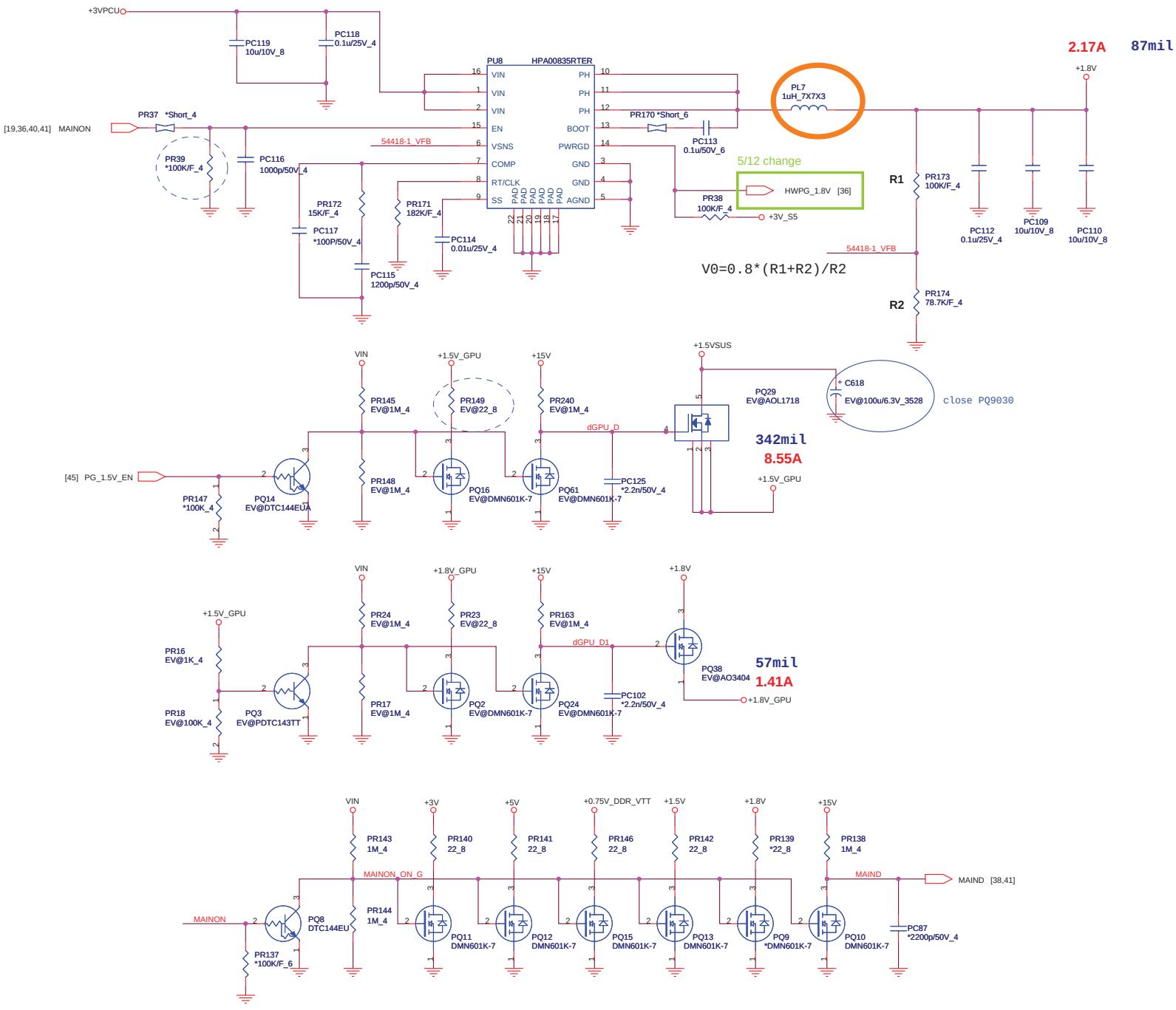
Frequency(PR220=200K)	300K

AMD Park VID Table

GPU_VID1 (GPIO15)	GPU_VID2 (GPIO20)	+VGPU_CORE
0	0	1.12V
1	0	1.05V
0	1	0.95V
1	1	0.9V

Quanta Computer Inc.
PROJECT : ZRD

Size	Document Number	Rev
	GPU CORE(MAX8792)	1C
Date: Wednesday, July 21, 2010	Sheet 43 of 9	



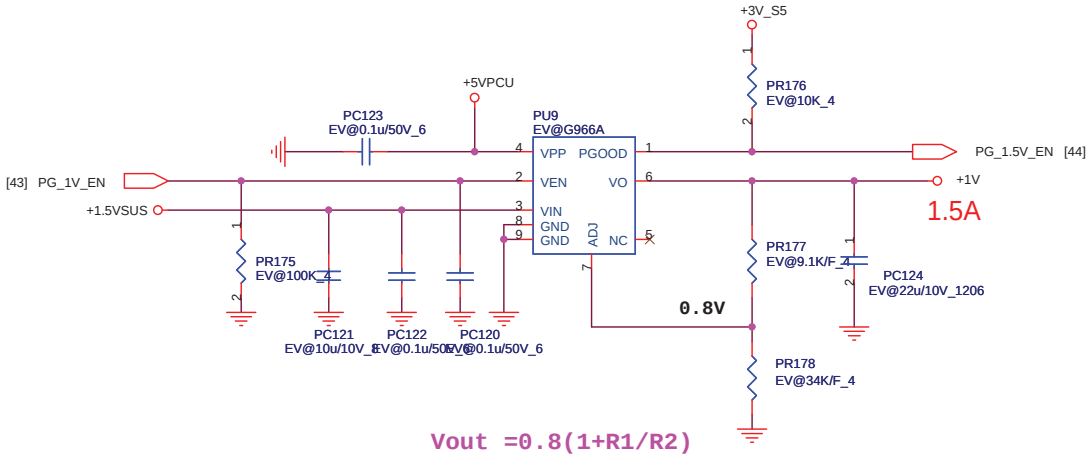
7/7 modify

Quanta Computer Inc.

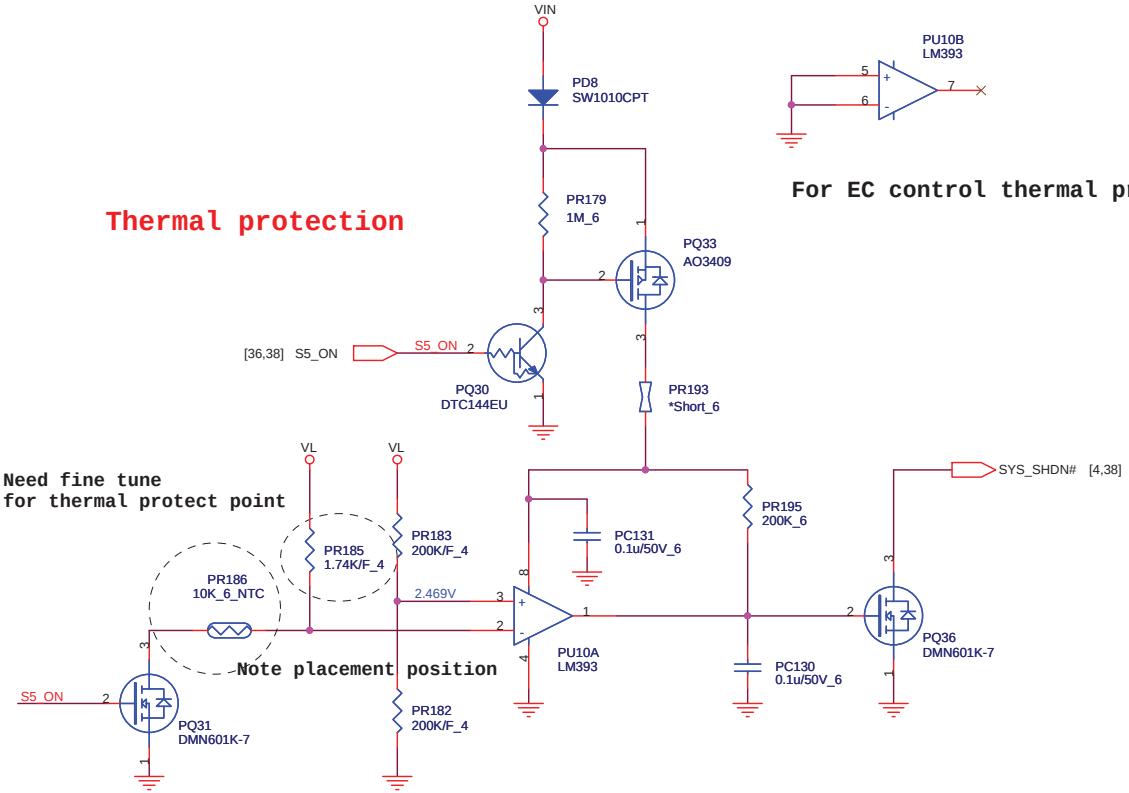
PROJECT : ZRD

Size	Document Number	Rev
	Discharge/1.8V)	1C

Date: Wednesday, July 21, 2010 Sheet 44 of 46



Vout =0.8(1+R1/R2)
=1V



Quanta Computer Inc.

PROJECT : ZRD

Size	Document Number	Rev
		1C

Date: Wednesday, July 21, 2010 Sheet 45 of 46

Model	REV	CHANGE LIST
ZRD MB	1A	FIRST RELEASED
	2A	Page 3 : Unstuff L54 & stuff R586 & change U31 P/N for 3V CLK gen and Switch CLK_BUF_DREFSSCLK and CLK_BUF_PCIE_3GPLL Page 4 : Q16 Change P/N for EOD part & short R116 (Del.) for 0 ohm Page 8 : Short R244 (Del.) for 0 ohm Page 10 :Short R243 (Del.) for 0 ohm Page 12 :Short R189 ,R190 & R534 (Del.) for 0 ohm & C655 change P/N for EOD part Page 14 :Del. R268 & R247 for M3 solution & stuff R269 ,R229 ,R223 & R226 for M1 solution,Stuff C372 for +1.5VSUS leakage Page 15 :Stuff C459 for +1.5VSUS leakage Page 25 :Q12 ,Q17 & Q18 Change P/N for ESD , CN10 Change P/N ,Q14.2 & Q13.2 Change from +5V to +3V Page 27 :C339 & C391 of footprint Change from 0805 to 0402 for ESD Page 28 :Unstuff R566 ,R294 ,R284 ,R279 ,R276 ,R273 ,R272 for disable debug card function Page 29 :C393 & C254 Change P/N for EOD , CN11 Change footprint for ME design request. Page 30 :U13 Change AMP circuit Page 31 :Q22 & Q23 Change P/N for EOD part. Page 34 :Del. L55 , CN12 Change P/N Page 36 :C27 Change P/N for EOD part Page All : Change to short pad : Location : R458 ,R452 ,R537 ,R533 ,R144 ,R155 ,R191 ,R140 ,R201 ,R224 ,R461 ,R136 ,R197 ,R206 ,R219 ,R212 ,R166 ,R174 ,R188 ,R202 ,R209 ,R184 ,R168 ,R185 ,R448 ,R447 ,R5 ,R10 ,R9 ,R6 ,R263 ,R288 ,R544 ,R436 ,R563 ,R570 ,R569 ,R584 ,R299 ,C738 ,R311 ,R585 ,R583 ,R571 ,R582 ,R575 ,R576 ,R579 ,R333 ,R352 ,R331 ,R332 & R349
	3A	
	3C	

MODEL	ZRD	
	FROM	To
	X	1A
	X	1A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B

DOC NO.	PROJECT MODEL :	ZRD	APPROVED BY:		DATE:	2010/07/21
	PART NUMBER:		DRAWING BY:		REVISON:	1C