1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
01		279015	ENGINEERING RELEASED	06/06/03	?

Q59 MLB DVT

LAST_MODIFIED=Wed Sep 17 12:11:39 2003

TABLE OF CONTENTS

POWER RAIL DEFINITIONS

	RUN	SLEEP	SHUTDOWN
+2_5V_MAIN	ON	ON	OFF
+3V_MAIN	ON	ON	OFF
+5V_MAIN	ON	ON	OFF
+5V_SLEEP	ON	OFF	OFF
+12V_MAIN	ON	ON	ON
+12V_SLEEP	ON	OFF	OFF
FW_PWR	ON	ON	OFF
+1.8V_SLEEP	ON	OFF	OFF
+MAXBUS_SLEEP	ON	OFF	OFF

SCHEMATIC AND PCB SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-6497	1	SCHEM,MLB,Q59	SCH1	CRITICAL	
820-1550	1	PCB,MLB,IMACG4	PCB1	CRITICAL	
825-2029	1	LBL,SER #,BARCODE	PCB1		
056-1158	1	DESIGN GUIDE,MCO,IMACG4	PCB1	CRITICAL	
057-0085	1	DFM,PNLZN DWG,MLB,Q59	PCB1	CRITICAL	
630-XXXX	1	630-XXXX,PCBA,H,Q59,EEE XXX	HYNIX		OMIT
630-XXXX	1	630-XXXX,PCBA,S,Q59,EEE XXX	SAMSUNG		OMIT

PCB,UL RECOGNIZED, MIN.130 DEG. C TEMP. RATING AND V-0 FLAME RATING PER UL 796 & UL 94. PCB TO BE SILK-SCREENED WITH UL/CUL RECOGNITION MARK, MANUFACTURER'S UL FILE NUMBER, UL PCB MATERIAL DESIGNATION, TEMPERATURE RATING AND FLAME RATING.

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING
THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE
SIZE D

Apple Computer Inc.

TITLE: SCHEM,MLB,Q59

DRAWING NUMBER 051-6497 REV. 13

SHT 1 OF 69

DRAWING

FW - B Connector P.36

Inverter KITCHEN P.29

LCD Panel Connector P.24

VGA/SVIDEO OUT

VGA Connector P.25

TMDS

EDID (I2C)

RGB

FW - A Connector P.36

Ethernet Connector P.35

NVIDIA NV18B 64MB P.17-27

GRAPHICS MEMORY P.20 (EXTERNAL MEM)

GRAPHICS MEMORY P.21 (EXTERNAL MEM)

FireWire PHY P.36

Ethernet PHY P.35

1394 OHCI
3.3V
8BIT TX/RX

AGP BUS
1.5V/3.3V
32BITS
66MHZ

WIRELESS P.31

32BITS

USB CONN(QTY3) P.31

FIREWIRE 400 MB/S P.34

ETHERNET 10/100 P.34

4X AGP P.16

PCI P.30

PCI BUS

USB2 CONTROL P.32

USB P.28

INTREPID

MODEM BLUETOOTH P.29

DDR MEMORY P.12

I2C P.34

MAXBUS P.9

BOOTROM P.30

BOOT ROM 1M X 8 P.30

MEMORY BUS
2.5V
167MHZ
64BITS

I2C

MAXBUS
167MHZ
32BIT ADDRESS
64BIT DATA

PMU P.44

DDR MUXES P.13

APOLLO CPU P.4-5

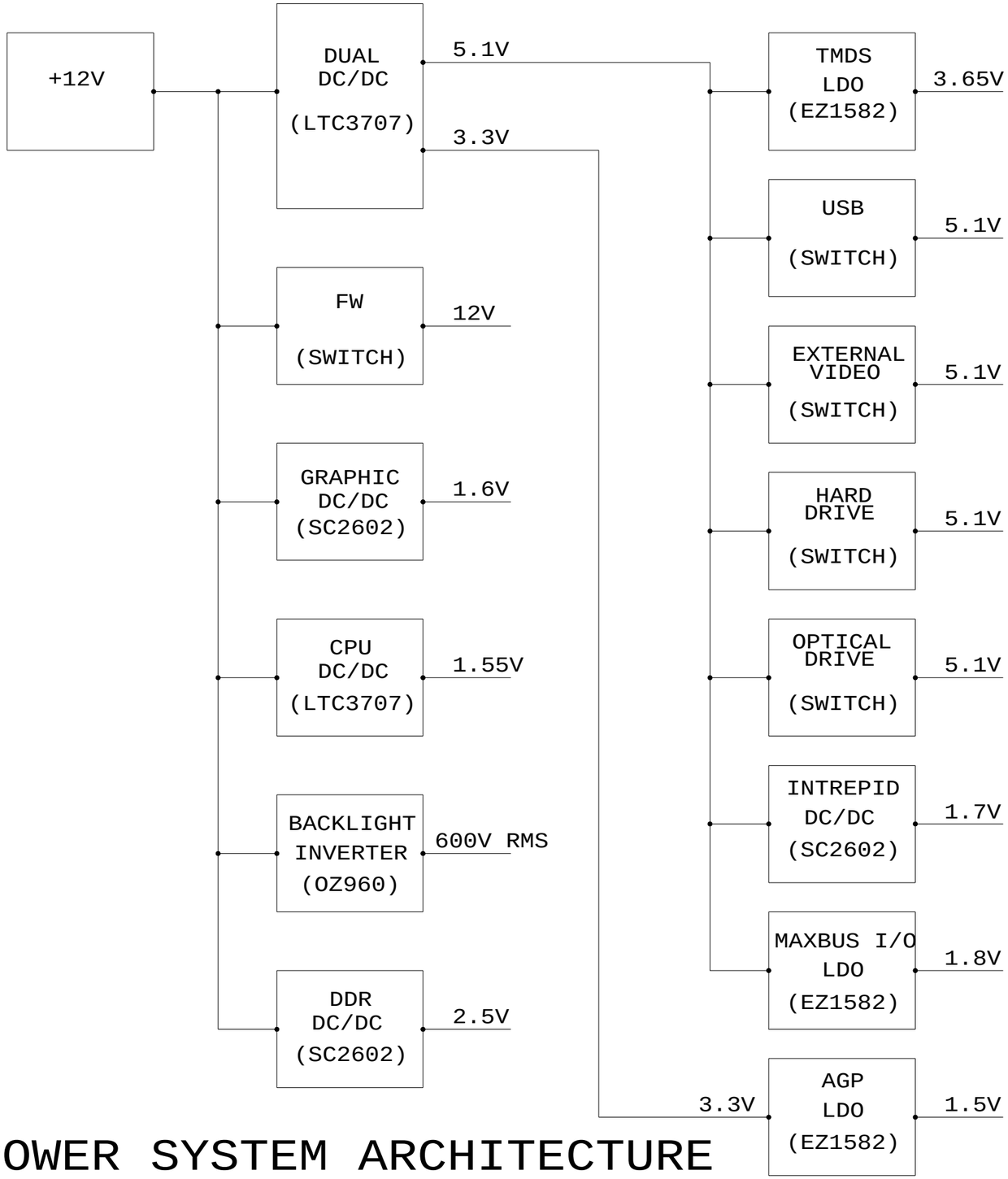
CPU PLL Config P.6

DDR SDRAM DIMM 0 P.15

DDR SDRAM DIMM 1 SO-DIMM Connector P.14

SYSTEM BLOCK

APPLE COMPUTER INC.
SIZE D | DRAWING NUMBER 051-6497 | REV. 13
SCALE NONE | SHT 2 OF 69
DRAWING



POWER SYSTEM ARCHITECTURE

LAYER	THICKNESS (MILS)	COPPER (OZ)	TRACE WIDTH (MILS)
1 - SIGNAL-TOP	0.7	0.5	4
PREPREG	3	---	
2 - GROUND1	1.4	1	---
PREPREG	3	---	
3 - SIGNAL	0.7	0.5	4
FILLER	17.4	---	
4 - POWER	2.8	2	---
PREPREG	4	---	
5 - POWER	2.8	2	---
FILLER	17.4	---	
6 - SIGNAL	0.7	0.5	4
PREPREG	3	---	
7 - GROUND2	1.4	1	---
PREPREG	3	---	
8 - SIGNAL-BOTTOM	0.7	0.5	4
TOTAL	62.0	---	---

NOSTUFF ZT39 HOLE-VIA-20R10
NOSTUFF ZT46 HOLE-VIA-20R10
NOSTUFF ZT53 HOLE-VIA-20R10
NOSTUFF ZT59 HOLE-VIA-20R10
NOSTUFF ZT64 HOLE-VIA-20R10
NOSTUFF ZT40 HOLE-VIA-20R10
NOSTUFF ZT47 HOLE-VIA-20R10
NOSTUFF ZT54 HOLE-VIA-20R10
NOSTUFF ZT60 HOLE-VIA-20R10
NOSTUFF ZT65 HOLE-VIA-20R10
NOSTUFF ZT41 HOLE-VIA-20R10
NOSTUFF ZT48 HOLE-VIA-20R10
NOSTUFF ZT55 HOLE-VIA-20R10
NOSTUFF ZT61 HOLE-VIA-20R10
NOSTUFF ZT66 HOLE-VIA-20R10
NOSTUFF ZT42 HOLE-VIA-20R10
NOSTUFF ZT49 HOLE-VIA-20R10
NOSTUFF ZT56 HOLE-VIA-20R10
NOSTUFF ZT62 HOLE-VIA-20R10
NOSTUFF ZT67 HOLE-VIA-20R10
NOSTUFF ZT43 HOLE-VIA-20R10
NOSTUFF ZT50 HOLE-VIA-20R10
NOSTUFF ZT57 HOLE-VIA-20R10
NOSTUFF ZT63 HOLE-VIA-20R10
NOSTUFF ZT68 HOLE-VIA-20R10
NOSTUFF ZT44 HOLE-VIA-20R10
NOSTUFF ZT51 HOLE-VIA-20R10
NOSTUFF ZT58 HOLE-VIA-20R10
NOSTUFF ZT45 HOLE-VIA-20R10
NOSTUFF ZT52 HOLE-VIA-20R10

PWR BLOCK,PCB INFO

APPLE COMPUTER INC.
SIZE D | DRAWING NUMBER 051-6497 | REV. 13
SCALE NONE | SHT 3 OF 69
DRAWING

CPU INTERNAL PLL FILTERING

59D8> 59B6> 52C6> 45D2<> 8C1< 8B7< 4D3< CPU_VCORE_SLEEP

R891 1 470 5% 1/16W MF 402 2

+MAXBUS_SLEEP 6C5< 6D6< 7A3< 7B3< 7C3< 7C5< 7C7< 8A3<> 8D1< 8D4< 9B7< 9D8< 44B7< 44D1< 44D2< 45D2<> 46D4< 52C6> 59C8>

CPU_VCORE_SLEEP 4D7< 8B7< 8C1< 45D2<> 52C6> 59B6> 59D8>

R901 1 10 1% 1/16W MF 603 2

52C6> CPU_AVDD

C1036 1 0.1UF 20% 10V CERM 402 2

C1035 1 2.2UF N20P80% 16V CERM 805 2

H8 H10 H12 J7 J9 J11 J13 K8 K10 K12 K14 L7 L9 L11 L13 M8 M10 M12 — VDD

B4 C2 C12 D5 E18 F2 G18 H3 J5 K2 L5 M3 N6 P2 P8 P11 R4 R13 R16 T6 T9 U2 U12 U16 V4 V7 V10 V14 — OVDD

A8 — AVDD

56D3> 9D3< 8B4<> 7C7<	CPU_BR_L	D2	BR*
56D3> 9D3<> 8B4<> 7B7<	CPU_BG_L	M1	BG*
56D3> 9D3<> 8B7<> 7C7<	CPU_TS_L	L4	TS*
7C5< 4A3<	CPU_PULLDOWN	E11	A0
		H1	A1
		C11	A2
		G3	A3
56D3> 9D3<> 8B4<>	CPU_ADDR<0>	F10	A4
56D3> 9D3<> 8B5<>	CPU_ADDR<1>	L2	A5
56D3> 9D3<> 8B4<>	CPU_ADDR<2>	D11	A6
56D3> 9D3<> 8B8<>	CPU_ADDR<3>	D1	A7
56D3> 9D3<> 8B5<>	CPU_ADDR<4>	C16	A8
56D3> 9D3<> 8B7<>	CPU_ADDR<5>	G2	A9
56D3> 9D3<> 8C4<>	CPU_ADDR<6>	D12	A10
56D3> 9D3<> 8B7<>	CPU_ADDR<7>	L3	A11
56D3> 9D3<> 8C5<>	CPU_ADDR<8>	G4	A12
56D3> 9C3<> 8B8<>	CPU_ADDR<9>	T2	A13
56D3> 9C3<> 8B8<>	CPU_ADDR<10>	F4	A14
56D3> 9C3<> 8C4<>	CPU_ADDR<11>	V1	A15
56D3> 9C3<> 8B7<>	CPU_ADDR<12>	J4	A16
56D3> 9C3<> 8B8<>	CPU_ADDR<13>	R2	A17
56D3> 9C3<> 8B7<>	CPU_ADDR<14>	K5	A18
56D3> 9C3<> 8B7<>	CPU_ADDR<15>	W2	A19
56D3> 9C3<> 8B8<>	CPU_ADDR<16>	J2	A20
56D3> 9C3<> 8B8<>	CPU_ADDR<17>	K4	A21
56D3> 9C3<> 8C8<>	CPU_ADDR<18>	N4	A22
56D3> 9C3<> 8B7<>	CPU_ADDR<19>	J3	A23
56D3> 9C3<> 8B8<>	CPU_ADDR<20>	M5	A24
56D3> 9C3<> 8C7<>	CPU_ADDR<21>	P5	A25
56D3> 9C3<> 8C7<>	CPU_ADDR<22>	N3	A26
56D3> 9C3<> 8C8<>	CPU_ADDR<23>	T1	A27
56D3> 9C3<> 8B7<>	CPU_ADDR<24>	V2	A28
56D3> 9C3<> 8B8<>	CPU_ADDR<25>	U1	A29
56D3> 9C3<> 8C8<>	CPU_ADDR<26>	N5	A30
56D3> 9C3<> 8C8<>	CPU_ADDR<27>	W1	A31
56D3> 9C3<> 8C7<>	CPU_ADDR<28>	B12	A32
56D3> 9C3<> 8C8<>	CPU_ADDR<29>	C4	A33
56D3> 9C3<> 8C7<>	CPU_ADDR<30>	G10	A34
56D3> 9C3<> 8C7<>	CPU_ADDR<31>	B11	A35

	NC_CPUAP<0>	NO_TEST C1	AP0
	NC_CPUAP<1>	NO_TEST E3	AP1
	NC_CPUAP<2>	NO_TEST H6	AP2
	NC_CPUAP<3>	NO_TEST F5	AP3
	NC_CPUAP<4>	NO_TEST G7	AP4

56D3> 9B3<> 8B4<> 7A7<	CPU_TT<0>	E5	TT0
56D3> 9B3<> 8B5<> 7A7<	CPU_TT<1>	E6	TT1
56D3> 9B3<> 8B4<> 7A7<	CPU_TT<2>	F6	TT2
56D3> 9B3<> 8B5<> 7A7<	CPU_TT<3>	E9	TT3
56D3> 9B3<> 8B4<> 7A7<	CPU_TT<4>	C5	TT4
56D3> 9B3<> 8B4<> 7B7<	CPU_TBST_L	F11	TBST*
56D3> 9B3<> 8B5<>	CPU_TSIZ<0>	G6	TSIZ0
56D3> 9B3<> 8B5<>	CPU_TSIZ<1>	F7	TSIZ1
56D3> 9B3<> 8B7<	CPU_TSIZ<2>	E7	TSIZ2
		E2	GBL*
56C3> 9B3<> 8B5<> 7A7<	CPU_WT_L	D3	WT*
56C3> 9C3<> 8C5<> 7A7<	CPU_CI_L	J1	CI*
56C3> 9B3<> 8B5<> 7B7<	CPU_AACK_L	R1	AACK*
56C3> 9B3<> 8B8<> 7C7<	CPU_ARTRY_L	N2	ARTRY*
7B5<	CPU_SHD0_L	E4	SHD0*
7B5<	CPU_SHD1_L	H5	SHD1*
56C3> 9B3< 8B8<> 7C7<	CPU_HIT_L	B2	HIT*

9C3<> 7B7< 56C3> CPU_INT_GBL_L

INT_V2 R311 0 5% 1/16W MF 402

56C3> 8B5<> CPU_GBL_L

INT_V1 R312 100 1% 1/16W MF 402

U34
800MHZ
APOLLO_MPC7445_360
BGA
(1 OF 3)
SEE_TABLE

BVSEL	B7	CPU_BUS_VSEL 7C4<
SYSCLK	A10	SYSCLK_CPU 9A4< 56C3>
CLKOUT	H2 NO_TEST	NC_CPU_CLKOUT
PLLCFG0	B8	CPU_PLL_CFG<0> 6C6< 8A8<>
PLLCFG1	C8	CPU_PLL_CFG<1> 6C6< 8A8<>
PLLCFG2	C7	CPU_PLL_CFG<2> 6C6< 8A8<>
PLLCFG3	D7	CPU_PLL_CFG<3> 6C6< 8A8<>
PLL_EXT	A7	CPU_PLL_CFGEXT 6C6< 8A8<>
DBG*	M2	CPU_DBG_L 7B7< 8B8<> 9B1<> 56C3>
DRDY*	R3	CPU_DRDY_L_UF 56C3>
DTI0	G1	CPU_EDTI 7C5<
DTI1	K1	CPU_DTI<0> 8B7<> 9A1<> 56C3>
DTI2	P1	CPU_DTI<1> 8B4<> 9A1<> 56C3>
DTI3	N1	CPU_DTI<2> 8B4<> 9A1<> 56C3>

NOSTUFF R895 1 47 5% 1/16W MF 402 2

RC GLITCH FILTER
PLACE CLOSE TO PIN

R850 1 0 5% 1/16W MF 402 2

CPU_DRDY_L 7B7< 8B5<> 9B1< 56C3>

NOSTUFF C954 1 10PF 5% 50V CERM 402 2

FILTERS A WAKE FROM SLEEP GLITCH IF NECESSARY

TDI	B9	JTAG_CPU_TDI 7A5< 8A3<> 59C8>
TDO	A4	JTAG_CPU_TDO 8A3<> 59C8>
TMS	F1	JTAG_CPU_TMS 7A5< 8A3<> 59C8>
TCK	C6	JTAG_CPU_TCK 7D5< 8A3<> 59C8>
TRST*	A5	JTAG_CPU_TRST_L 7C5< 8A3<> 59C8>
LSSDMODE*	E8	CPU_LSSD_MODE 7B5<
L1TSTCLK	G8	CPU_L1TSTCLK 7B4<
L2TSTCLK	B3	CPU_L2TSTCLK 7C4<

TA*	K6	CPU_TA_L 7C7< 8C4<> 9A1<> 56C3>
TEA*	L1	CPU_TEA_L 7B7< 8B5<> 9A1<> 56C3>

TBEN	E1	CPU_TBEN 7C5< 9A3<>
QREQ*	P4	CPU_QREQ_L 7D5< 8B7<> 9B3< 56C3>
QACK*	G5	CPU_QACK_L 8B4<> 9B3<> 56C3>
CKSTP_IN*	A3	CPU_CHKSTP_IN_L 7B5< 59C8>
CKSTP_OUT*	B1	CPU_CHKSTP_OUT_L 7B5< 8A3<> 8D5<> 59C8>

INT*	D4	MPIC_CPU_INT_L 7A5< 8D7<> 28B5>
SMI*	F9	CPU_SMI_L 7A5< 44C4<>
MCP*	C9	CPU_MCP_L 7B5<
SRESET*	A2	CPU_SRESET_L 7A5< 8A3<> 59C6>
HRESET*	D8	CPU_HRESET_L 7A3< 7A5< 7B3< 8A3<> 44C2< 44D2< 59C8>

IBORG PULLS THIS UP, SPEC SAYS TO GROUND IT FOR SW CONTROL

PMON_IN*	D9	CPU_PMONIN_L 7C5<
PMON_OUT*	A9 NO_TEST	NC_PMON_OUT_L
BMODE0*	G9	CPU_EMODE0_L 7A4<
BMODE1*	F8	CPU_EMODE1_L 7A4<
EXT_QUAL	A11	
TEST0	A12	
TEST1	B6	
TEST2	B10	
TEST3	E10	CPU_PULLUP 7A5<
TEST4	D10	CPU_PULLDOWN 4D7<> 7C5<

ZH4 275R138 ZT9P1

C352 1 0.1UF 20% 10V CERM 402 2

ZH5 TH SL-138X272-292 ZT11P1

C345 1 0.1UF 20% 10V CERM 402 2

ZH6 TH SL-138X272-292 ZT10P1

C369 1 0.1UF 20% 10V CERM 402 2

ZH7 275R138 ZT8P1

C370 1 0.1UF 20% 10V CERM 402 2

B5 C3 D6 D13 E17 F3 G17 H4 H7 H9 H11 H13 J6 J8 J10 J12 K7 K9 K11 K13 L6 L8 L10 L12 M4 M7 M9 M11 M13 N7 P3 P9 P12 R6 R14 R17 T7 T10 U3 U13 U17 V5 V8 V11 V15 — GND

INTREPID VERSION 1 PULLS GBL
ALL THE TIME. NEED TO
CUT THE TRACE AND YANK
DOWN HARD FOR SNOOPING.
FIXED IN INTREPID VERSION 2.

CPU MECHANICAL PARTS SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
875-1475	1	PAD,THERMAL,CPU,U34	U341	?	
870-1113	1	HEAT SINK,CPU,Q26,U34	U342	?	DEV
870-1114	1	CLIP,HEAT SINK,CPU,Q26.U34	U343	?	DEV
412-0042	1	SCREW,MACH,3MM W,8MM L,U34	U344	?	DEV
835-0251	1	NUT,3MM,U34	U345	?	DEV

MPC7450 MAXBUS

LAST MODIFIED=Wed Sep 17 12:15:40 2003

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6497	13

SCALE: NONE — SHT 4 OF 69

DRAWING

APOLLO_MPC7445_360

U34
800MHZ
BGA
(3 OF 3)

NC_CPUCRUD<0>	NO_TEST	F18	NC_F18
NC_CPUCRUD<1>	NO_TEST	F17	NC_F17
NC_CPUCRUD<2>	NO_TEST	F19	NC_F19
NC_CPUCRUD<3>	NO_TEST	H19	NC_H19
NC_CPUCRUD<4>	NO_TEST	H18	NC_H18
NC_CPUCRUD<5>	NO_TEST	H17	NC_H17
NC_CPUCRUD<6>	NO_TEST	H16	NC_H16
NC_CPUCRUD<7>	NO_TEST	E19	NC_E19
NC_CPUCRUD<8>	NO_TEST	D18	NC_D18
NC_CPUCRUD<9>	NO_TEST	F16	NC_F16
NC_CPUCRUD<10>	NO_TEST	G16	NC_G16
NC_CPUCRUD<11>	NO_TEST	D19	NC_D19
NC_CPUCRUD<12>	NO_TEST	F15	NC_F15
NC_CPUCRUD<13>	NO_TEST	G19	NC_G19
NC_CPUCRUD<14>	NO_TEST	E16	NC_E16
NC_CPUCRUD<15>	NO_TEST	D17	NC_D17
NC_CPUCRUD<16>	NO_TEST	D16	NC_D16
NC_CPUCRUD<17>	NO_TEST	P15	NC_P15
NC_CPUCRUD<18>	NO_TEST	L15	NC_L15
NC_CPUCRUD<19>	NO_TEST	N15	NC_N15
NC_CPUCRUD<20>	NO_TEST	P18	NC_P18
NC_CPUCRUD<21>	NO_TEST	N14	NC_N14
NC_CPUCRUD<22>	NO_TEST	M14	NC_M14
NC_CPUCRUD<23>	NO_TEST	M17	NC_M17
NC_CPUCRUD<24>	NO_TEST	N13	NC_N13
NC_CPUCRUD<25>	NO_TEST	N16	NC_N16
NC_CPUCRUD<26>	NO_TEST	M19	NC_M19
NC_CPUCRUD<27>	NO_TEST	M16	NC_M16
NC_CPUCRUD<28>	NO_TEST	P19	NC_P19
NC_CPUCRUD<29>	NO_TEST	N17	NC_N17
NC_CPUCRUD<30>	NO_TEST	M15	NC_M15
NC_CPUCRUD<31>	NO_TEST	L17	NC_L17
NC_CPUCRUD<32>	NO_TEST	L14	NC_L14
NC_CPUCRUD<33>	NO_TEST	K15	NC_K15
NC_CPUCRUD<34>	NO_TEST	J14	NC_J14
NC_CPUCRUD<35>	NO_TEST	J18	NC_J18
NC_CPUCRUD<36>	NO_TEST	J19	NC_J19
NC_CPUCRUD<37>	NO_TEST	J15	NC_J15
NC_CPUCRUD<38>	NO_TEST	K19	NC_K19
NC_CPUCRUD<39>	NO_TEST	J16	NC_J16
NC_CPUCRUD<40>	NO_TEST	H15	NC_H15
NC_CPUCRUD<41>	NO_TEST	L16	NC_L16
NC_CPUCRUD<42>	NO_TEST	P16	NC_P16
NC_CPUCRUD<43>	NO_TEST	M18	NC_M18
NC_CPUCRUD<44>	NO_TEST	L19	NC_L19
NC_CPUCRUD<45>	NO_TEST	L18	NC_L18
NC_CPUCRUD<46>	NO_TEST	K18	NC_K18
NC_CPUCRUD<47>	NO_TEST	J17	NC_J17
NC_CPUCRUD<48>	NO_TEST	K16	NC_K16
NC_CPUCRUD<49>	NO_TEST	C19	NC_C19
NC_CPUCRUD<50>	NO_TEST	D15	NC_D15
NC_CPUCRUD<51>	NO_TEST	G15	NC_G15
NC_CPUCRUD<52>	NO_TEST	C18	NC_C18
NC_CPUCRUD<53>	NO_TEST	A16	NC_A16
NC_CPUCRUD<54>	NO_TEST	B19	NC_B19
NC_CPUCRUD<55>	NO_TEST	A19	NC_A19
NC_CPUCRUD<56>	NO_TEST	D14	NC_D14
NC_CPUCRUD<57>	NO_TEST	E15	NC_E15
NC_CPUCRUD<58>	NO_TEST	B15	NC_B15
NC_CPUCRUD<59>	NO_TEST	B17	NC_B17
NC_CPUCRUD<60>	NO_TEST	C17	NC_C17
NC_CPUCRUD<61>	NO_TEST	C16	NC_C16
NC_CPUCRUD<62>	NO_TEST	G13	NC_G13
NC_CPUCRUD<63>	NO_TEST	E14	NC_E14
NC_CPUCRUD<64>	NO_TEST	H14	NC_H14
NC_CPUCRUD<65>	NO_TEST	G14	NC_G14
NC_CPUCRUD<66>	NO_TEST	C15	NC_C15
NC_CPUCRUD<67>	NO_TEST	A17	NC_A17
NC_CPUCRUD<68>	NO_TEST	G12	NC_G12
NC_CPUCRUD<69>	NO_TEST	F14	NC_F14
NC_CPUCRUD<70>	NO_TEST	F13	NC_F13
NC_CPUCRUD<71>	NO_TEST	E13	NC_E13
NC_CPUCRUD<72>	NO_TEST	B16	NC_B16
NC_CPUCRUD<73>	NO_TEST	A15	NC_A15
NC_CPUCRUD<74>	NO_TEST	C14	NC_C14
NC_CPUCRUD<75>	NO_TEST	A18	NC_A18
NC_CPUCRUD<76>	NO_TEST	A13	NC_A13
NC_CPUCRUD<77>	NO_TEST	F12	NC_F12
NC_CPUCRUD<78>	NO_TEST	A14	NC_A14
NC_CPUCRUD<79>	NO_TEST	G11	NC_G11
NC_CPUCRUD<80>	NO_TEST	C13	NC_C13
NC_CPUCRUD<81>	NO_TEST	N12	NC_N12
NC_CPUCRUD<82>	NO_TEST	N18	NC_N18
NC_CPUCRUD<83>	NO_TEST	K17	NC_K17
NC_CPUCRUD<84>	NO_TEST	N19	NC_N19
NC_CPUCRUD<85>	NO_TEST	B18	NC_B18
NC_CPUCRUD<86>	NO_TEST	E12	NC_E12
NC_CPUCRUD<87>	NO_TEST	B13	NC_B13
NC_CPUCRUD<88>	NO_TEST	B14	NC_B14
NC_CPUCRUD<89>	NO_TEST	A6	NC_A6

APOLLO_MPC7445_360

U34
800MHZ
BGA
(2 OF 3)

56D3> 9D1<> 8C4<>	CPU_DATA<0>	R15	D0
56D3> 9D1<> 8C7<>	CPU_DATA<1>	W15	D1
56D3> 9D1<> 8C8<>	CPU_DATA<2>	T14	D2
56D3> 9D1<> 8C5<>	CPU_DATA<3>	V16	D3
56D3> 9D1<> 8C7<>	CPU_DATA<4>	W16	D4
56D3> 9D1<> 8C8<>	CPU_DATA<5>	T15	D5
56D3> 9D1<> 8C4<>	CPU_DATA<6>	U15	D6
56D3> 9D1<> 8C8<>	CPU_DATA<7>	P14	D7
56D3> 9D1<> 8C5<>	CPU_DATA<8>	V13	D8
56D3> 9D1<> 8C4<>	CPU_DATA<9>	W13	D9
56D3> 9D1<> 8C7<>	CPU_DATA<10>	T13	D10
56D3> 9D1<> 8C5<>	CPU_DATA<11>	P13	D11
56D3> 9D1<> 8C5<>	CPU_DATA<12>	U14	D12
56D3> 9D1<> 8C7<>	CPU_DATA<13>	W14	D13
56D3> 9D1<> 8C8<>	CPU_DATA<14>	R12	D14
56D3> 9D1<> 8C5<>	CPU_DATA<15>	T12	D15
56D3> 9C1<> 8C4<>	CPU_DATA<16>	W12	D16
56D3> 9C1<> 8C7<>	CPU_DATA<17>	V12	D17
56D3> 9C1<> 8C4<>	CPU_DATA<18>	N11	D18
56D3> 9C1<> 8C4<>	CPU_DATA<19>	N10	D19
56D3> 9C1<> 8C4<>	CPU_DATA<20>	R11	D20
56D3> 9C1<> 8C8<>	CPU_DATA<21>	U11	D21
56D3> 9C1<> 8C7<>	CPU_DATA<22>	W11	D22
56D3> 9C1<> 8C8<>	CPU_DATA<23>	T11	D23
56D3> 9C1<> 8D4<>	CPU_DATA<24>	R10	D24
56D3> 9C1<> 8D7<>	CPU_DATA<25>	N9	D25
56D3> 9C1<> 8C5<>	CPU_DATA<26>	P10	D26
56D3> 9C1<> 8C7<>	CPU_DATA<27>	U10	D27
56D3> 9C1<> 8D8<>	CPU_DATA<28>	R9	D28
56D3> 9C1<> 8C8<>	CPU_DATA<29>	W10	D29
56D3> 9C1<> 8C5<>	CPU_DATA<30>	U9	D30
56D3> 9C1<> 8D7<>	CPU_DATA<31>	V9	D31
56D3> 9C1<> 9B7< 8D7<>	CPU_DATA<32>	W5	D32
56D3> 9C1<> 9B7< 8D8<>	CPU_DATA<33>	U6	D33
56D3> 9C1<> 9B7< 8D8<>	CPU_DATA<34>	T5	D34
56D3> 9C1<> 9B7< 8D7<>	CPU_DATA<35>	U5	D35
56D3> 9C1<> 9A7< 8D4<>	CPU_DATA<36>	W7	D36
56D3> 9C1<> 8D5<>	CPU_DATA<37>	R6	D37
56D3> 9C1<> 8D5<>	CPU_DATA<38>	P7	D38
56D3> 9C1<> 8D5<>	CPU_DATA<39>	V6	D39
56D3> 9C1<> 8D7<> 6C4<	CPU_DATA<40>	P17	D40
56D3> 9C1<> 8C4<> 6C4<	CPU_DATA<41>	R19	D41
56D3> 9B1<> 8C5<> 6C4<	CPU_DATA<42>	V18	D42
56D3> 9B1<> 8C4< 6C4<	CPU_DATA<43>	R18	D43
56D3> 9B1<> 8C8<> 6C4<	CPU_DATA<44>	V19	D44
56D3> 9B1<> 8C7<> 6C4<	CPU_DATA<45>	T19	D45
56D3> 9B1<> 8C4<> 6C4<	CPU_DATA<46>	U19	D46
56D3> 9B1<> 8C7< 6C4<	CPU_DATA<47>	W19	D47
56D3> 9D8< 9B1<> 8C5<>	CPU_DATA<48>	U18	D48
56D3> 9D8< 9B1<> 8C4<>	CPU_DATA<49>	W17	D49
56D3> 9D8< 9B1<> 8C8<>	CPU_DATA<50>	W18	D50
56D3> 9D8< 9B1<> 8C8<>	CPU_DATA<51>	T16	D51
56D3> 9C8< 9B1<> 8C5<>	CPU_DATA<52>	T18	D52
56D3> 9C8< 9B1<> 8C7<>	CPU_DATA<53>	T17	D53
56D3> 9C8< 9B1<> 8D7<>	CPU_DATA<54>	W3	D54
56D3> 9C8< 9B1<> 8C5<>	CPU_DATA<55>	V17	D55
56D3> 9B1<> 8D8<>	CPU_DATA<56>	U4	D56
56D3> 9D5< 9B1<> 8D5<>	CPU_DATA<57>	U8	D57
56D3> 9D5< 9B1<> 8D4<>	CPU_DATA<58>	U7	D58
56D3> 9D5< 9B1<> 8D8<>	CPU_DATA<59>	R7	D59
56D3> 9D5< 9B1<> 8D8<>	CPU_DATA<60>	P6	D60
56D3> 9C5< 9B1<> 8D4<>	CPU_DATA<61>	R8	D61
56D3> 9C5< 9B1<> 8D4<>	CPU_DATA<62>	W8	D62
56D3> 9C5< 9B1<> 8D5<>	CPU_DATA<63>	T8	D63
	NC_CPUDP<0> NO_TEST	T3	DP0
	NC_CPUDP<1> NO_TEST	W4	DP1
	NC_CPUDP<2> NO_TEST	T4	DP2
	NC_CPUDP<3> NO_TEST	W9	DP3
	NC_CPUDP<4> NO_TEST	M6	DP4
	NC_CPUDP<5> NO_TEST	V3	DP5
	NC_CPUDP<6> NO_TEST	N8	DP6
	NC_CPUDP<7> NO_TEST	W6	DP7

MPC7450 - 2

LAST_MODIFIED=Wed Sep 17 12:15:41 2003

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6497	13

SCALE	SHT	OF
NONE	5	69

DRAWING

BOMOPTIONS FOR UPPER-SET OF RESISTORS

1200@133&1500@167&1333@133&1667@167&1467@133&1833@167&1600@133&2000@167&1733@133&2167@167&1867@133&2333@167&2000@133&2500@167&2133@133&2667@167

667@133&833@167&733@133&917@167&800@133&1000@167&1067@133&1333@167&1333@133&1667@167&1467@133&1833@167&1600@133&2000@167&1867@133&2333@167&2133@133&2667@167

800@133&1000@167&867@133&1083@167&1067@133&1333@167&1200@133&1500@167&1733@133&2167@167&1867@133&2333@167&2133@133&2667@167

667@133&833@167&933@133&1167@167&1200@133&1500@167&1333@133&1667@167&1600@133&2000@167

667@133&833@167&733@133&917@167&800@133&1000@167&867@133&1083@167&1000@133&1250@167&1200@133&1500@167&1467@133&1833@167&1600@133&2000@167&1733@133&2167@167&2000@133&2500@167&2133@133&2667@167

+MAXBUS_SLEEP 4D5< 6C5< 7A3< 7B3< 7C3< 7C5< 7C7< 8A3<> 8D1< 8D4< 9B7< 9D8< 44B7< 44D1< 44D2< 45D2<> 46D4< 52C6> 59C8>

SPECIAL CONFIG R382 10K 1% 1/16W MF 402 — CPU_PLL_CFGEXT 4C3< 8A8<>
SPECIAL CONFIG R379 10K 1% 1/16W MF 402 — CPU_PLL_CFG<3> 4C3< 8A8<>
SPECIAL CONFIG R378 10K 1% 1/16W MF 402 — CPU_PLL_CFG<2> 4D3< 8A8<>
SPECIAL CONFIG R376 10K 1% 1/16W MF 402 — CPU_PLL_CFG<1> 4D3< 8A8<>
SPECIAL CONFIG R374 10K 1% 1/16W MF 402 — CPU_PLL_CFG<0> 4D3< 8A8<>

SPECIAL CONFIG R383 1K 1% 1/16W MF 402
SPECIAL CONFIG R381 1K 1% 1/16W MF 402
SPECIAL CONFIG R380 1K 1% 1/16W MF 402
SPECIAL CONFIG R377 1K 1% 1/16W MF 402
SPECIAL CONFIG R375 1K 1% 1/16W MF 402

CPU_PLL_STOP 44B8<

667@133&833@167&733@133&917@167&800@133&1000@167&867@133&1083@167&933@133&1167@167&1000@133&1250@167&1067@133&1333@167

867@133&1083@167&933@133&1167@167&1000@133&1250@167&1200@133&1500@167&1733@133&2167@167&2000@133&2500@167

667@133&833@167&1000@133&1250@167&1200@133&1500@167&1333@133&1667@167&1600@133&2000@167&2000@133&2500@167

733@133&917@167&800@133&1000@167&867@133&1083@167&1000@133&1250@167&1067@133&1333@167&1467@133&1833@167&1733@133&2167@167&1867@133&2333@167&2000@133&2500@167&2133@133&2667@167

933@133&1167@167&1067@133&1333@167&1333@133&1667@167&1867@133&2333@167

(STUFF FOR 133 AND 167)

833@167&917@167&1000@167&1083@167&1167@167&1250@167&1333@167&1500@167&1667@167&1833@167&2000@167&2167@167&2333@167&2500@167&2667@167

(STUFF FOR 133 AND 167)

NOSTUFF

667@133&733@133&800@133&867@133&933@133&1000@133&1067@133&1200@133&1333@133&1467@133&1600@133&1733@133&1867@133&2000@133&2133@133

+MAXBUS_SLEEP 8D1< 8A3<> 7C7< 7C5< 7C3< 7B3< 7A3< 6D6< 4D5< 46D4< 45D2<> 44D2< 44D1< 44B7< 9D8< 9B7< 8D4< 59C8> 52C6>

NOSTUFF R879 10K 1% 1/16W MF 402 — CPU_DATA<40> 5B4<> 8D7<> 9C1<> 56D3>
NOSTUFF R878 10K 1% 1/16W MF 402 — CPU_DATA<41> 5B4<> 8C4<> 9C1<> 56D3>
NOSTUFF R889 10K 1% 1/16W MF 402 — CPU_DATA<42> 5B4<> 8C5<> 9B1<> 56D3>
NOSTUFF R866 10K 1% 1/16W MF 402 — CPU_DATA<43> 5B4<> 8C4< 9B1<> 56D3>
NOSTUFF R874 10K 1% 1/16W MF 402 — CPU_DATA<44> 5B4<> 8C8<> 9B1<> 56D3>
NOSTUFF R877 10K 1% 1/16W MF 402 — CPU_DATA<45> 5B4<> 8C7<> 9B1<> 56D3>
NOSTUFF R875 10K 1% 1/16W MF 402 — CPU_DATA<46> 5B4<> 8C4<> 9B1<> 56D3>
NOSTUFF R867 10K 1% 1/16W MF 402 — CPU_DATA<47> 5B4<> 8C7< 9B1<> 56D3>

R363 4.7K 5% 1/16W MF 402
R364 4.7K 5% 1/16W MF 402
R887 4.7K 5% 1/16W MF 402
R357 4.7K 5% 1/16W MF 402
R368 4.7K 5% 1/16W MF 402
R365 4.7K 5% 1/16W MF 402
R367 4.7K 5% 1/16W MF 402
R356 4.7K 5% 1/16W MF 402

INTREPID BOOT STRAPS
BITS 40 - 47

SPARE
SPARE
PLL4MODESEL_NXT[2:0]
000: 166.4 MHZ
001: 149.76 MHZ
010: 133.12 MHZ
011: 99.84 MHZ
100: 83.20 MHZ
INTERNALSPREADEN
0:: INACTIVE
1:: ACTIVE
PCI1_SOURCE_CLOCK
0:: PLL5 (NO SPREAD)
1:: PLL4
PCI0_SOURCE_CLOCK
0:: PLL5 (NO SPREAD)
1:: PLL4

CPU FREQUENCY CONFIGURATION
(SUPPORTED CPU & BUS SPEEDS)

MULTIPLIER	CORE FREQUENCY (AT BUS FREQUENCY) 167MHZ	133MHZ	CPU_PLL_CFG
(BUS-TO-CORE)	(MHZ)		E 0123 HEX
5.0X	833	667	0 1011 0B
5.5X	917	733	0 1001 09
6.0X	1000	800	0 1101 0D
6.5X	1083	867	0 0101 05
7.0X	1167	933	0 0010 02
7.5X	1250	1000	0 0001 01
8.0X	1333	1067	0 1100 0C
9.0X	1500	1200	1 0111 17
10.0X	1667	1333	1 1010 1A
11.0X	1833	1467	1 1001 19
12.0X	2000	1600	1 1011 1B
13.0X	2167	1733	1 0101 15
14.0X	2333	1867	1 1100 1C
15.0X	2500	2000	1 0001 11
16.0X	2667	2133	1 1101 1D

CPU SPEED & BUS RATIO SUPPORT

THE CONFIGURATION RESISTORS BELOW ARE SELF CONFIGURING WHEN THE ENGINEER SELECTS THE APPROPRIATE CPU AND BUS SPEED BOM OPTION, THE APPROPRIATE RESISTORS ARE ARE AUTOMATICALLY SELECTED

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S2799	1	IC,APOLLO6,SICOH,1.0GHZ,1.5V+30/-130MV,28W,85C	U34	CRITICAL	1000@167
337S2801	1	IC,APOLLO6,SICOH,1.25GHZ,1.57V+70/-70MV,35W,85C	U34	CRITICAL	1250@167

CPU BUS RATIO BITS

APPLE COMPUTER INC.
SIZE D | DRAWING NUMBER 051-6497 | REV: 13
SCALE NONE | SHT 6 OF 69
DRAWING

<XR_PAGE_TITLE>

BMODE <0>	BMODE <1>	MSSCR0 <16:17>	Sys Bus	Vger ID	Addr Drve
L	L	1 1	???	01	yes unavail
L	!hr	1 0	Max	01	yes unavail
L	hr	1 1	???	00	yes unavail
L	H	1 0	Max	00	yes unavail
!hr	L	0 1	MB+	01	yes unavail
!hr	!hr	0 0	60x	01	yes unavail
!hr	hr	0 1	MB+	00	yes unavail
!hr	H	0 0	60x	00	yes unavail
hr	L	1 1	???	01	norm unavail
hr	!hr	1 0	Max	01	norm
hr	hr	1 1	???	00	norm unavail
HR	H	1 0	MAX	00	NORM <- DEFAULT
H	L	0 1	MB+	01	norm unavail
H	!hr	0 0	60x	01	norm
H	hr	0 1	MB+	00	norm unavail
H	H	0 0	60x	00	norm

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_H	1.5V INTERFACE
CPU_L3_VSEL	CPU_HRESET_L or L3_OVDD	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_H	1.5V INTERFACE

MAXBUS PULL-UPS

59C8> 52C6>
8D1< 8A3<> 7C5< 7C3< 7B3< 7A3< 6D6< 6C5< 4D5< +MAXBUS_SLEEP
46D4< 45D2<> 44D2< 44D1< 44B7< 9D8< 9B7< 8D4<

56D3> 9D3<> 8B7<> 4D7<> CPU_TS_L — R347 10K 1% 1/16W MF 402
56C3> 9A1<> 8C4<> 4C3< CPU_TA_L — R348 10K 1% 1/16W MF 402
56C3> 9B3<> 8B8<> 4A7<> CPU_ARTRY_L — R346 10K 1% 1/16W MF 402
56D3> 9D3< 8B4<> 4D7> CPU_BR_L — R841 10K 1% 1/16W MF 402
56C3> 9B3< 8B8<> 4A7> CPU_HIT_L — R840 10K 1% 1/16W MF 402
56C3> 9B1< 8B5<> 4C2< CPU_DRDY_L — R851 10K 1% 1/16W MF 402
56C3> 9A1<> 8B5<> 4C3< CPU_TEA_L — R845 10K 1% 1/16W MF 402
56C3> 9B3<> 8B5<> 4A7< CPU_AACK_L — R849 10K 1% 1/16W MF 402
56C3> 9B1<> 8B8<> 4C3< CPU_DBG_L — R847 10K 1% 1/16W MF 402
56D3> 9D3<> 8B4<> 4D7< CPU_BG_L — R846 10K 1% 1/16W MF 402
56D3> 9B3<> 8B4<> 4B7> CPU_TBST_L — R349 10K 1% 1/16W MF 402
56C3> 9C3<> 4B8< CPU_INT_GBL_L — R842 10K 1% 1/16W MF 402
56C3> 9C3<> 8C5<> 4A7> CPU_CI_L — R844 10K 1% 1/16W MF 402
56C3> 9B3<> 8B5<> 4B7> CPU_WT_L — RP78 10K 5% 1/16W SM1 (2-7)
56D3> 9B3<> 8B4<> 4B7<> CPU_TT<0> — RP78 10K 5% 1/16W SM1 (1-8)
56D3> 9B3<> 8B5<> 4B7<> CPU_TT<1> — RP78 10K 5% 1/16W SM1 (3-6)
56D3> 9B3<> 8B4<> 4B7<> CPU_TT<2> — R843 10K 1% 1/16W MF 402
56D3> 9B3<> 8B5<> 4B7<> CPU_TT<3> — RP78 10K 5% 1/16W SM1 (4-5)
56D3> 9B3<> 8B4<> 4B7<> CPU_TT<4> — R350 10K 1% 1/16W MF 402

56C3> 9B3< 8B7<> 4C3> CPU_QREQ_L — R848 10K 1% 1/16W MF 402
59C8> 8A3<> 4C3< JTAG_CPU_TCK — R924 10K 1% 1/16W MF 402
59C8> 8A3<> 4C3< JTAG_CPU_TRST_L — R925 200 5% 1/16W MF 402
4B3< CPU_PMONIN_L — RP79 10K 5% 1/16W SM1 (4-5)
4C3< CPU_EDTI — R858 10K 1% 1/16W MF 402
4D7<> 4A3< CPU_PULLDOWN — R859 470 5% 1/16W MF 402

MPC7450 PULL-UPS

59C8>
8D4< 8D1< 8A3<> 7C7< 7C3< 7B3< 7A3< 6D6< 6C5< 4D5< +MAXBUS_SLEEP
52C6> 46D4< 45D2<> 44D2< 44D1< 44B7< 9D8< 9B7<

9A3<> 4C3< CPU_TBEN — R856 10K 1% 1/16W MF 402
4A7<> CPU_SHD0_L — R857 10K 1% 1/16W MF 402
4A7<> CPU_SHD1_L — R860 10K 1% 1/16W MF 402
4B3< CPU_MCP_L — R910 10K 1% 1/16W MF 402
4C3< CPU_LSSD_MODE — R911 10K 1% 1/16W MF 402
59C8> 8D5<> 8A3<> 4B3> CPU_CHKSTP_OUT_L — NOSTUFF R921 1K 1% 1/16W MF 402
59C8> 4B3< CPU_CHKSTP_IN_L — R882 1K 1% 1/16W MF 402
4A3< CPU_PULLUP — R909 1K 1% 1/16W MF 402
59C8> 44D2< 44C2< 8A3<> 7B3< 7A3< 4B3< CPU_HRESET_L — R922 10K 1% 1/16W MF 402
59C6> 8A3<> 4B3< CPU_SRESET_L — RP79 10K 5% 1/16W SM1 (2-7)
28B5> 8D7<> 4B3< MPIC_CPU_INT_L — RP79 10K 5% 1/16W SM1 (3-6)
44C4<> 4B3< CPU_SMI_L — R912 10K 1% 1/16W MF 402
59C8> 8A3<> 4C3< JTAG_CPU_TDI — RP79 10K 5% 1/16W SM1 (1-8)
59C8> 8A3<> 4C3< JTAG_CPU_TMS — R923 10K 1% 1/16W MF 402

NOSTUFF R915 0 5% 1/16W MF 402 — VGER_INV_HRESET 7A3< 7B3< 44D1>
NOSTUFF R913 10K 5% 1/16W MF 402 — +MAXBUS_SLEEP 59C8> 4D5< 6C5< 6D6< 7A3< 7B3< 7C3< 7C5< 7C7< 8A3<> 8D1< 8D4< 9B7< 9D8< 44B7< 44D1< 44D2< 45D2<> 46D4< 52C6>
4D3< CPU_BUS_VSEL — R914 200 5% 1/16W MF 402

BUS MODE
0V 1.8V BUS MODE
INV_HRESET 1.5V BUS MODE
OVDD 2.5V BUS MODE

4C3< CPU_L2TSTCLK — R918 10K 1% 1/16W MF 402 — +MAXBUS_SLEEP 59C8> 4D5< 6C5< 6D6< 7A3< 7B3< 7C3< 7C5< 7C7< 8A3<> 8D1< 8D4< 9B7< 9D8< 44B7< 44D1< 44D2< 45D2<> 46D4< 52C6>
NOSTUFF R926 0 5% 1/16W MF 402 — CPU_HRESET_L 4B3< 7A3< 7A5< 7B3< 8A3<> 44C2< 44D2< 59C8>
NOSTUFF R919 0 5% 1/16W MF 402 — VGER_INV_HRESET 7A3< 7B3< 7C3< 44D1>
NOSTUFF R920 200 5% 1/16W MF 402

DO NOT USE UNLESS FIX INVERTER BUFFER

NOSTUFF R907 10K 5% 1/16W MF 402 — +MAXBUS_SLEEP 4D5< 6C5< 6D6< 7A3< 7C3< 7C5< 7C7< 8A3<> 8D1< 8D4< 9B7< 9D8< 44B7< 44D1< 44D2< 45D2<> 46D4< 52C6> 59C8>
NOSTUFF R906 0 5% 1/16W MF 402 — CPU_HRESET_L 4B3< 7A3< 7A5< 7B3< 8A3<> 44C2< 44D2< 59C8>
NOSTUFF R916 0 5% 1/16W MF 402 — VGER_INV_HRESET 7A3< 7B3< 7C3< 44D1>
4C3< CPU_L1TSTCLK — R917 200 5% 1/16W MF 402

CPUBUS_60X R904 1K 5% 1/16W MF 402 — +MAXBUS_SLEEP 59C8> 4D5< 6C5< 6D6< 7A3< 7B3< 7C3< 7C5< 7C7< 8A3<> 8D1< 8D4< 9B7< 9D8< 44B7< 44D1< 44D2< 45D2<> 46D4< 52C6>
4B3< CPU_EMODE0_L — CPUBUS_MAX R905 200 5% 1/16W MF 402 — CPU_HRESET_L 4B3< 7A5< 7B3< 8A3<> 44C2< 44D2< 59C8>
R903 1K 1% 1/16W MF 402 — +MAXBUS_SLEEP 7C5< 7C7< 8A3<> 8D1< 8D4< 9B7< 9D8< 4D5< 6C5< 6D6< 7A3< 7B3< 7C3< 44B7< 44D1< 44D2< 45D2<> 46D4< 52C6> 59C8>
4B3< CPU_EMODE1_L — NOSTUFF R902 200 5% 1/16W MF 402 — VGER_INV_HRESET 7B3< 7C3< 44D1>

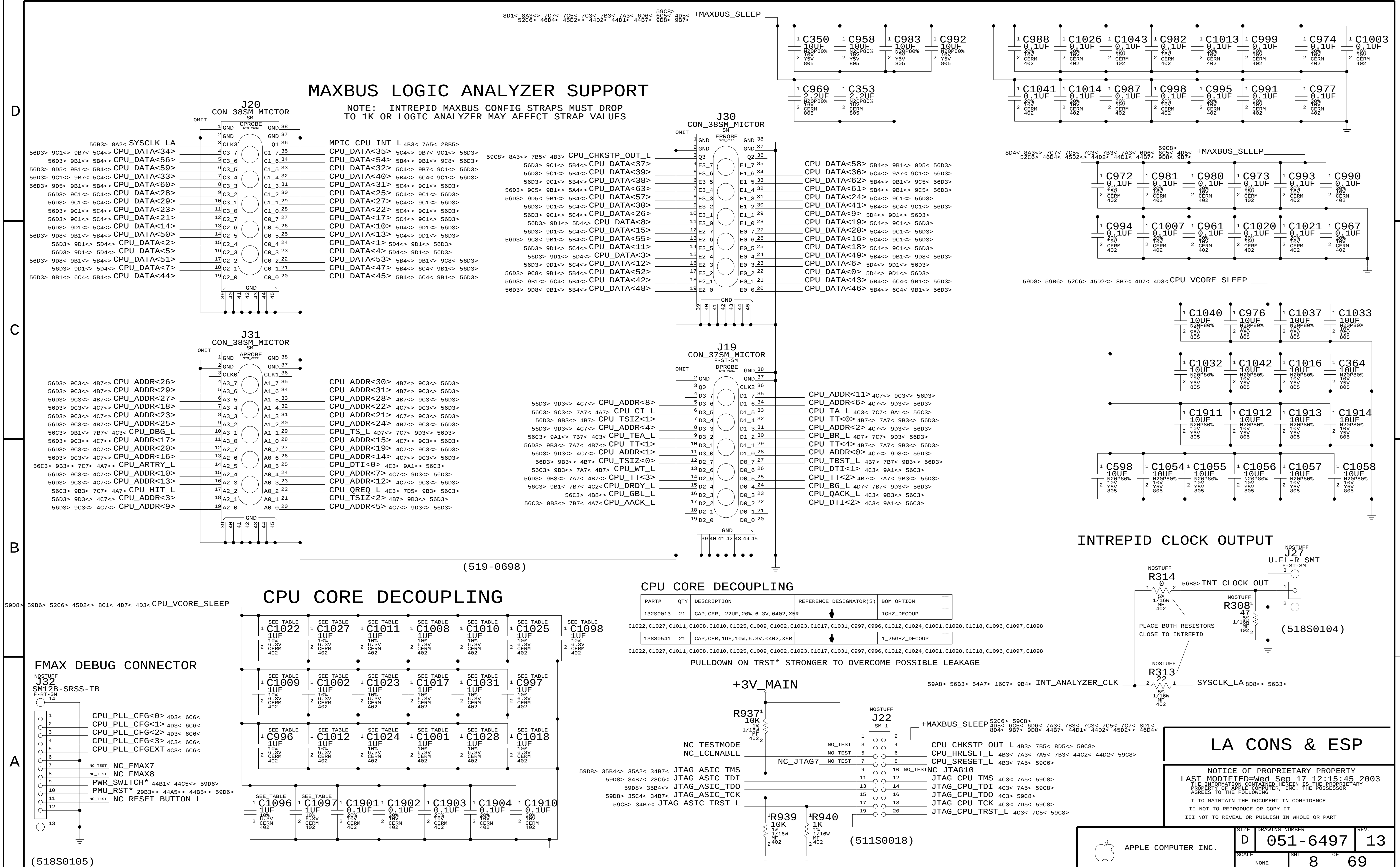
CPU CONFIG OPTIONS

LAST_MODIFIED=Wed Sep 17 12:15:43 2003

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6497	13
SCALE: NONE	SHT 7 OF 69	

DRAWING



CPU CORE DECOUPLING

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0013	21	CAP,CER,.22UF,20%,6.3V,0402,X5R	↓	1GHZ_DECOUP
138S0541	21	CAP,CER,1UF,10%,6.3V,0402,X5R	↓	1_25GHZ_DECOUP

C1022,C1027,C1011,C1008,C1010,C1025,C1009,C1002,C1023,C1017,C1031,C997,C996,C1012,C1024,C1001,C1028,C1018,C1096,C1097,C1098

C1022,C1027,C1011,C1008,C1010,C1025,C1009,C1002,C1023,C1017,C1031,C997,C996,C1012,C1024,C1001,C1028,C1018,C1096,C1097,C1098

PULLDOWN ON TRST* STRONGER TO OVERCOME POSSIBLE LEAKAGE

LA CONS & ESP

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6497	13
SCALE NONE	SHT 8	OF 69

INTREPID BOOT STRAPS

BITS 48 - 63

52C6> 46D4< 45D2<> 8D4< 8D1< 8A3<> 7A3< 6D6< 6C5< 4D5< +MAXBUS_SLEEP
7C3< 7B3< 7A3< 8D4< 6C5< 4D5<
7C7< 7C5< 7C3< 7B3<
44D2< 44D1< 44B7< 9B7<
59C8>

R890 10K	R868 10K	R892 10K	R832 10K	R863 10K	R339 10K	R340 10K	R864 10K	R876 10K	R865 10K	R885 10K	R855 10K	R869 10K	R894 4.7K	R355 4.7K	R893 4.7K
R343 4.7K	R360 4.7K	R352 4.7K	R338 4.7K	R341 4.7K	R359 4.7K	R366 4.7K	R358 4.7K	R886 4.7K	R354 4.7K	R351 4.7K	R870 4.7K				

56D3> 9B1<> 8C5<> 5B4<> CPU_DATA<48>
56D3> 9B1<> 8C4<> 5B4<> CPU_DATA<49>
56D3> 9B1<> 8C8<> 5B4<> CPU_DATA<50>
56D3> 9B1<> 8D8<> 5B4<> CPU_DATA<51>
56D3> 9B1<> 8C5<> 5B4<> CPU_DATA<52>
56D3> 9B1<> 8C7<> 5B4<> CPU_DATA<53>
56D3> 9B1<> 8D7<> 5B4<> CPU_DATA<54>
56D3> 9B1<> 8C5<> 5B4<> CPU_DATA<55>

CPU_DATA<57> 5B4<> 8D5<> 9B1<> 56D3>
CPU_DATA<58> 5B4<> 8D4<> 9B1<> 56D3>
CPU_DATA<59> 5B4<> 8D8<> 9B1<> 56D3>
CPU_DATA<60> 5B4<> 8D8<> 9B1<> 56D3>
CPU_DATA<61> 5B4<> 8D4<> 9B1<> 56D3>
CPU_DATA<62> 5B4<> 8D4<> 9B1<> 56D3>
CPU_DATA<63> 5A4<> 8D5<> 9B1<> 56D3>

0:: BUF_REF_CLK_OUTENABLE_H ACTIVE
1:: INACTIVE

1:: SEL PLL 4EXTSRC EXTERNAL SOURCE

0:: EN_PCI_ROM_P BOOTROM ON PCI1
1:: BOOTROM ON IDE/CARDSLOT

0:: TI 1394B WORKAROUND NORMAL 1394B TI PHY WORKAROUND
1:: TI 1394B WORKAROUND

MAXBUS OUTPUT IMPEDANCE
111: 28.6 OHM
011: 33.3 OHM
101: 40 OHM
001: 50 OHM
110: 66.6 OHM
010: 100 OHM
100: 200 OHM
000: 200 OHM

SPARE
SPARE
SPARE

0:: ROM_Ovrly_Rng 0-1 IDE / 2-3 PCI1
1:: 0-1 IDE / 2-3 PCI1

0:: PCI1_REQ2_L / PCI1_GNT2_L GPIOs
1:: PCI1_REQ2_L / PCI1_GNT2_L GPIOs

0:: PCI1_REQ1_L / PCI1_GNT1_L GPIOs
1:: PCI1_REQ1_L / PCI1_GNT1_L GPIOs

0:: PCI1_REQ0_L / PCI1_GNT0_L GPIOs
1:: PCI1_REQ0_L / PCI1_GNT0_L GPIOs

0:: FIREWIRE PHY INTERFACE LEGACY INTERFACE
1:: B-MODE INTERFACE

0:: PROCESSOR BUS MODE MAX BUS (G4)
1:: 60X BUS (G3)

BITS 32 - 39

45D2<> 44D2<> 44D1< 44B7<
7C3< 7B3< 7A3< 8D4< 6C5< 4D5< +MAXBUS_SLEEP
9D8< 8D4< 8D1< 8A3<> 7C7< 7C5<
59C8> 52C6> 46D4<

R833 10K	R852 10K	R862 10K	R854 10K	R853 10K	R342 4.7K	R345 4.7K	R861 4.7K	R353 4.7K	R344 4.7K

56D3> 9C1<> 8D7<> 5C4<> CPU_DATA<32>
56D3> 9C1<> 8D8<> 5C4<> CPU_DATA<33>
56D3> 9C1<> 8D8<> 5C4<> CPU_DATA<34>
56D3> 9C1<> 8D7<> 5C4<> CPU_DATA<35>
56D3> 9C1<> 8D4<> 5C4<> CPU_DATA<36>

0:: DDR_TPDMODEENABLE_H ACTIVE
1:: TDI OUTPUT(JTAG)

0:: ANALYZERCLK_EN_H ACTIVE
1:: ACTIVE

0:: DDR_TPDEN_POL ACTIVE HIGH
1:: ACTIVE LOW

0:: EXTPLL_SDWN_POL ACTIVE HIGH
1:: ACTIVE LOW

SPARE

52D3> 30D5< 28D6<> 16D6< +1_5V_INTREPID_PLL
R720 4.7 5% 1/16W MF 402
C854 0.1UF 20% 10V CERM 402
C1101 0.1UF 20% 10V CERM 402
+1_5V_INTREPID_PLL7

9A2<> INT_PLL6_GND

56D3> 8B4<> 7C7< 4D7> CPU_BR_L
56D3> 8B4<> 7B7< 4D7< CPU_BG_L
56D3> 8B7<> 7C7< 4D7<> CPU_TS_L

56D3> 8B4<> 4C7<> CPU_ADDR<0>
56D3> 8B5<> 4C7<> CPU_ADDR<1>
56D3> 8B4<> 4C7<> CPU_ADDR<2>
56D3> 8B8<> 4C7<> CPU_ADDR<3>
56D3> 8B5<> 4C7<> CPU_ADDR<4>
56D3> 8B7<> 4C7<> CPU_ADDR<5>
56D3> 8C4<> 4C7<> CPU_ADDR<6>
56D3> 8B7<> 4C7<> CPU_ADDR<7>
56D3> 8C5<> 4C7<> CPU_ADDR<8>
56D3> 8B8<> 4C7<> CPU_ADDR<9>
56D3> 8B8<> 4C7<> CPU_ADDR<10>
56D3> 8C4<> 4C7<> CPU_ADDR<11>
56D3> 8B7<> 4C7<> CPU_ADDR<12>
56D3> 8B8<> 4C7<> CPU_ADDR<13>
56D3> 8B7<> 4C7<> CPU_ADDR<14>
56D3> 8B7<> 4C7<> CPU_ADDR<15>
56D3> 8B8<> 4C7<> CPU_ADDR<16>
56D3> 8B8<> 4C7<> CPU_ADDR<17>
56D3> 8C8<> 4C7<> CPU_ADDR<18>
56D3> 8B7<> 4C7<> CPU_ADDR<19>
56D3> 8B8<> 4C7<> CPU_ADDR<20>
56D3> 8C7<> 4C7<> CPU_ADDR<21>
56D3> 8C7<> 4C7<> CPU_ADDR<22>
56D3> 8C8<> 4C7<> CPU_ADDR<23>
56D3> 8B7<> 4B7<> CPU_ADDR<24>
56D3> 8B8<> 4B7<> CPU_ADDR<25>
56D3> 8C8<> 4B7<> CPU_ADDR<26>
56D3> 8C8<> 4B7<> CPU_ADDR<27>
56D3> 8C7<> 4B7<> CPU_ADDR<28>
56D3> 8C8<> 4B7<> CPU_ADDR<29>
56D3> 8C7<> 4B7<> CPU_ADDR<30>
56D3> 8C7<> 4B7<> CPU_ADDR<31>

56C3> 8C5<> 7A7< 4A7> CPU_CI_L
56C3> 7B7< 4B8< CPU_INT_GBL_L
56D3> 8B4<> 7B7< 4B7> CPU_TBST_L
56D3> 8B5<> 4B7> CPU_TSIZ<0>
56D3> 8B5<> 4B7> CPU_TSIZ<1>
56D3> 8B7< 4B7> CPU_TSIZ<2>
56D3> 8B4<> 7A7< 4B7<> CPU_TT<0>
56D3> 8B5<> 7A7< 4B7<> CPU_TT<1>
56D3> 8B4<> 7A7< 4B7<> CPU_TT<2>
56D3> 8B5<> 7A7< 4B7<> CPU_TT<3>
56D3> 8B4<> 7A7< 4B7<> CPU_TT<4>
56C3> 8B5<> 7A7< 4B7> CPU_WT_L

56C3> 8B5<> 7B7< 4A7< CPU_AACK_L
56C3> 8B8<> 7C7< 4A7<> CPU_ARTRY_L
56C3> 8B8<> 7C7< 4A7> CPU_HIT_L

56C3> 8B7<> 7D5< 4C3> CPU_QREQ_L

56C3> 8B4<> 4C3< CPU_QACK_L
44B8<> INT_SUSPEND_REQ_L
44B5<> INT_SUSPEND_ACK_L

INTREPID V1.1 IS 133MHZ ONLY

U25 INTREPID BGA SEE_TABLE (ON PAGE 12) (1 OF 9)

BR	E29	A_0	D24
BG	E26	A_1	D25
TS	B27	A_2	A27
		A_3	E24
		A_4	G23
		A_5	B26
		A_6	A26
		A_7	D23
		A_8	A25
		A_9	E23
		A_10	J22
		A_11	B25
		A_12	H22
		A_13	G22
		A_14	D22
		A_15	B24
		A_16	B23
		A_17	E22
		A_18	J21
		A_19	G21
		A_20	E21
		A_21	A24
		A_22	D21
		A_23	A23
		A_24	H20
		A_25	B22
		A_26	H21
		A_27	A22
		A_28	E20
		A_29	B21
		A_30	D20
		A_31	A21
CI	G26		
GBL	A29		
TBST	A28		
TSIZ_0	G24		
TSIZ_1	H24		
TSIZ_2	D26		
TT_0	E25		
TT_1	G25		
TT_2	B28		
TT_3	D27		
TT_4	J25		
WT	D28		
AACK	B29		
ARTRY	H23		
HIT	B31		
QREQ	A32		
QACK	G27		
SUSPENDREQ	AK9		
SUSPENDACK	AM8		

MAXBUS INTERFACE

CPU_FB_IN	J24	D_0	D10
CPU_FB_OUT	H16	D_1	G12
ANALYZER_CLK	G8	D_2	E11
STOPCPUCLK	AH9	D_3	H11
ACS_REF	H13	D_4	B9
CPU_CLK	J15	D_5	B8
TBEN	A31	D_6	A9
		D_7	A8
		D_8	E12
		D_9	D11
		D_10	B10
		D_11	J13
		D_12	A10
		D_13	D12
		D_14	E13
		D_15	G13
		D_16	B11
		D_17	D13
		D_18	A11
		D_19	G14
		D_20	H14
		D_21	E14
		D_22	B12
		D_23	G15
		D_24	B13
		D_25	H15
		D_26	D14
		D_27	B14
		D_28	A12
		D_29	G16
		D_30	E15
		D_31	J16
		D_32	D15
		D_33	A14
		D_34	A13
		D_35	D16
		D_36	E16
		D_37	G17
		D_38	B15
		D_39	H17
		D_40	A15
		D_41	B16
		D_42	E17
		D_43	A16
		D_44	J18
		D_45	H18
		D_46	D17
		D_47	G18
		D_48	A17
		D_49	B17
		D_50	E18
		D_51	B18
		D_52	D18
		D_53	A18
		D_54	A19
		D_55	H19
		D_56	B19
		D_57	J19
		D_58	A20
		D_59	D19
		D_60	E19
		D_61	G19
		D_62	B20
		D_63	G20
DBG	A30		
DRDY	G28		
DTI_0	K25		
DTI_1	D29		
DTI_2	B30		
TA	E27		
TEA	E28		

CPU_DATA<0> 5D4<> 8C4<> 56D3>
CPU_DATA<1> 5D4<> 8C7<> 56D3>
CPU_DATA<2> 5D4<> 8C8<> 56D3>
CPU_DATA<3> 5D4<> 8C5<> 56D3>
CPU_DATA<4> 5D4<> 8C7<> 56D3>
CPU_DATA<5> 5D4<> 8C8<> 56D3>
CPU_DATA<6> 5D4<> 8C4<> 56D3>
CPU_DATA<7> 5D4<> 8C8<> 56D3>
CPU_DATA<8> 5D4<> 8C5<> 56D3>
CPU_DATA<9> 5D4<> 8C4<> 56D3>
CPU_DATA<10> 5D4<> 8C7<> 56D3>
CPU_DATA<11> 5C4<> 8C5<> 56D3>
CPU_DATA<12> 5C4<> 8C5<> 56D3>
CPU_DATA<13> 5C4<> 8C7<> 56D3>
CPU_DATA<14> 5C4<> 8C8<> 56D3>
CPU_DATA<15> 5C4<> 8C5<> 56D3>
CPU_DATA<16> 5C4<> 8C4<> 56D3>
CPU_DATA<17> 5C4<> 8C7<> 56D3>
CPU_DATA<18> 5C4<> 8C4<> 56D3>
CPU_DATA<19> 5C4<> 8C4<> 56D3>
CPU_DATA<20> 5C4<> 8C4<> 56D3>
CPU_DATA<21> 5C4<> 8C8<> 56D3>
CPU_DATA<22> 5C4<> 8C7<> 56D3>
CPU_DATA<23> 5C4<> 8C8<> 56D3>
CPU_DATA<24> 5C4<> 8D4<> 56D3>
CPU_DATA<25> 5C4<> 8D7<> 56D3>
CPU_DATA<26> 5C4<> 8C5<> 56D3>
CPU_DATA<27> 5C4<> 8C7<> 56D3>
CPU_DATA<28> 5C4<> 8D8<> 56D3>
CPU_DATA<29> 5C4<> 8C8<> 56D3>
CPU_DATA<30> 5C4<> 8C5<> 56D3>
CPU_DATA<31> 5C4<> 8D7<> 56D3>
CPU_DATA<32> 5C4<> 8D7<> 9B7< 56D3>
CPU_DATA<33> 5C4<> 8D8<> 9B7< 56D3>
CPU_DATA<34> 5C4<> 8D8<> 9B7< 56D3>
CPU_DATA<35> 5C4<> 8D7<> 9B7< 56D3>
CPU_DATA<36> 5C4<> 8D4<> 9A7< 56D3>
CPU_DATA<37> 5B4<> 8D5<> 56D3>
CPU_DATA<38> 5B4<> 8D5<> 56D3>
CPU_DATA<39> 5B4<> 8D5<> 56D3>
CPU_DATA<40> 5B4<> 6C4< 8D7<> 56D3>
CPU_DATA<41> 5B4<> 6C4< 8C4<> 56D3>
CPU_DATA<42> 5B4<> 6C4< 8C5<> 56D3>
CPU_DATA<43> 5B4<> 6C4< 8C4< 56D3>
CPU_DATA<44> 5B4<> 6C4< 8C8<> 56D3>
CPU_DATA<45> 5B4<> 6C4< 8C7<> 56D3>
CPU_DATA<46> 5B4<> 6C4< 8C4<> 56D3>
CPU_DATA<47> 5B4<> 6C4< 8C7< 56D3>
CPU_DATA<48> 5B4<> 8C5<> 9D8< 56D3>
CPU_DATA<49> 5B4<> 8C4<> 9D8< 56D3>
CPU_DATA<50> 5B4<> 8C8<> 9D8< 56D3>
CPU_DATA<51> 5B4<> 8C8<> 9D8< 56D3>
CPU_DATA<52> 5B4<> 8C7<> 9C8< 56D3>
CPU_DATA<53> 5B4<> 8C7<> 9C8< 56D3>
CPU_DATA<54> 5B4<> 8D7<> 9C8< 56D3>
CPU_DATA<55> 5B4<> 8C5<> 9C8< 56D3>
CPU_DATA<56> 5B4<> 8D8<> 56D3>
CPU_DATA<57> 5B4<> 8D5<> 9D5< 56D3>
CPU_DATA<58> 5B4<> 8D4<> 9D5< 56D3>
CPU_DATA<59> 5B4<> 8D8<> 9D5< 56D3>
CPU_DATA<60> 5B4<> 8D8<> 9D5< 56D3>
CPU_DATA<61> 5B4<> 8D4<> 9C5< 56D3>
CPU_DATA<62> 5B4<> 8D4<> 9C5< 56D3>
CPU_DATA<63> 5A4<> 8D5<> 9C5< 56D3>
CPU_DBG_L 4C3< 7B7< 8B8<> 56C3>
CPU_DRDY_L 4C2< 7B7< 8B5<> 56C3>
CPU_DTI<0> 4C3< 8B7<> 56C3>
CPU_DTI<1> 4C3< 8B4<> 56C3>
CPU_DTI<2> 4C3< 8B4<> 56C3>
CPU_TA_L 4C3< 7C7< 8C4<> 56C3>
CPU_TEA_L 4C3< 7B7< 8B5<> 56C3>

VDD15A_7 (PLL6) H26

VSSA_7 (PLL6) H25

VIN = INTREPID VCORE (1.7V)
VOUT = MAXBUS RAIL (1.8V)

59A8> 56B3> 54A7< 16C7< 8A2< INT_ANALYZER_CLK
R764 10 5% 1/16W MF 402 INT_V1
56C3> INT_CPU_FB_IN
56C3> INT_CPU_FB_OUT
INT_ANALYZER_CLKA

56C3> 4D2< SYSCLK_CPU
R713 0 5% 1/16W MF 402
56C3> SYSCLK_CPU_UF

7C5< 4C3< CPU_TBEN
R712 1K 1% 1/16W MF 402
9D3< INT_PLL6_GND NO_TEST
XW47 SM

56B3>
CPU_FB_PLUS3
ADDS 3" (0.5 NS)
R772 0 5% 1/16W MF 402
R766 0 5% 1/16W MF 402

ADDS 2" (0.35 NS)
ADDS 1" (0.17 NS)
56C3> CPU_FBI_PLUS1
R321 0 5% 1/16W MF 402
R777 0 5% 1/16W MF 402
R310 0 5% 1/16W MF 402

CPU_FB_PLUS2
56C3>
CPU_FB_MINUS3
R776 0 5% 1/16W MF 402
R757 0 5% 1/16W MF 402
R752 470 5% 1/16W MF 402

R319 0 5% 1/16W MF 402
R765 0 5% 1/16W MF 402
56C3> CPU_FBO_PLUS1

MAIN LOOP IS 3" (0.5 NS)
SHORTER THAN MAXBUS CLOCK

ALLOWS ADJUSTING FB CLOCK FROM -3" (0.5 NS)
TO +2" (0.35 NS) IN 1" (0.17 NS) INCREMENTS
PLACE ALL SERPENTINES ON INTERNAL LAYER

INTREPID MAX

APPLE COMPUTER INC.
SIZE D | DRAWING NUMBER 051-6497 | REV. 13
SCALE NONE | SHT 9 OF 69
DRAWING

INTREPID 1.1 SHOULD ALLOW MAXBUS
RAIL TO TURN OFF IN SLEEP

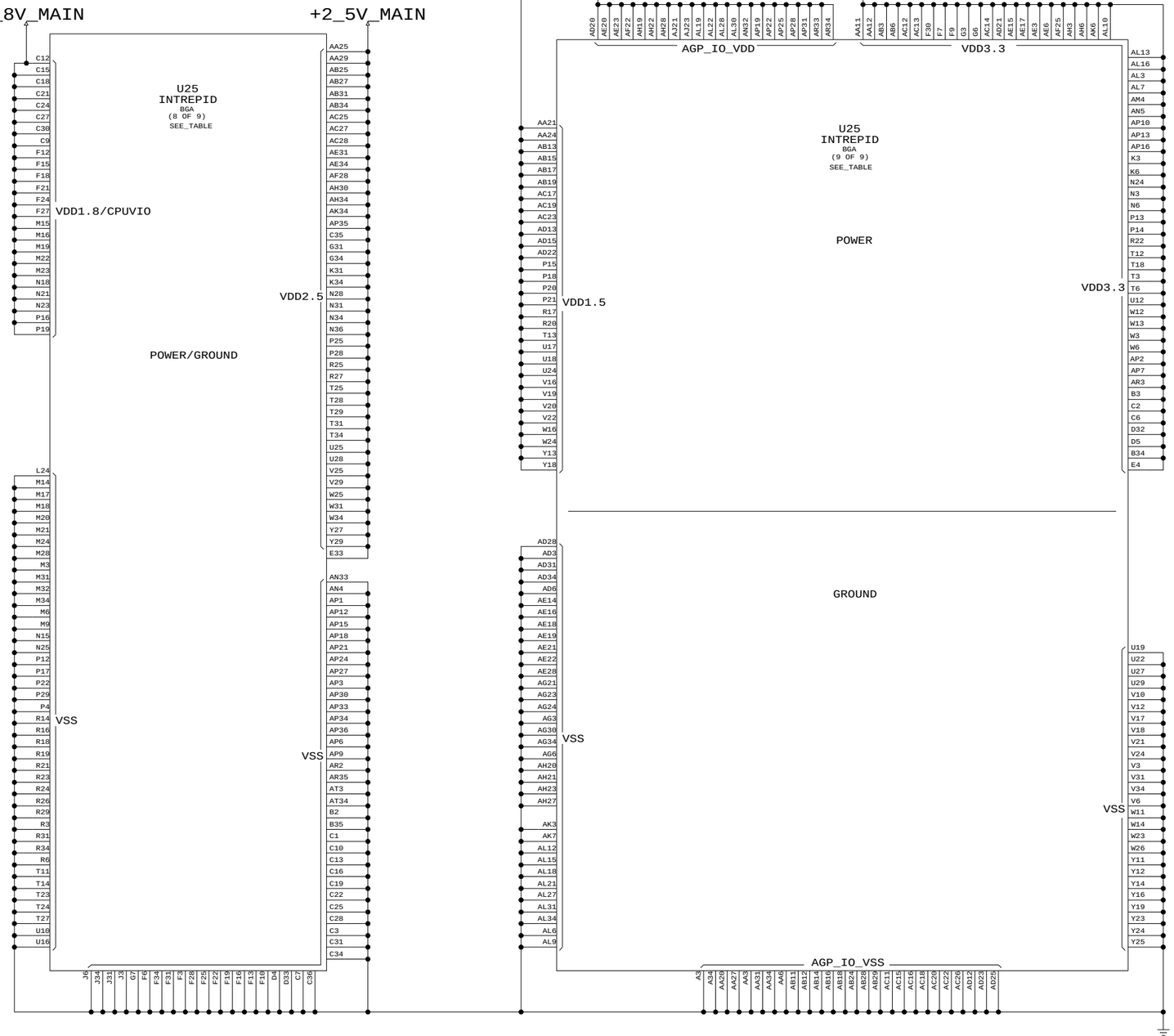
52C3> 46B4<> 17D5< 17A4< 17A3< 16D7< 16C2< 16A8< 11A6< 59C8> +1_5V_AGP

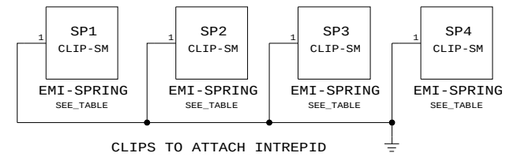
59C8> 47B2<> 46B3< 11D3< +INTREPID_CORE_MAIN

+1_8V_MAIN

+2_5V_MAIN

+3V_MAIN





CLIPS TO ATTACH INTREPID
HEATSINK TO GND AT THE
FOUR CORNERS

INTREPID EMI CLIP SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
870-1125	4	INTREPID EMI CLIP	SP1,SP2,SP3,SP4	?	

INTREPID VERSION SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
343S0198	1	IC,ASIC,INTREPID,V1.X	U25		INT_V1
343S0211	1	IC,ASIC,INTREPID,V2.1	U25	CRITICAL	INT_V2

INTREPID POWER

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6497	13

SCALE: NONE
SHT 10 OF 69

DRAWING

+1_8V_MAIN — INTREPID MAXBUS DECOUPLING

24 Balls
4 X 10UF (0805)
36 X 0.1UF (0402)

C289 10UF N20P80% 10V Y5V 805
C291 10UF N20P80% 10V Y5V 805
C288 10UF N20P80% 10V Y5V 805
C290 10UF N20P80% 10V Y5V 805
C890 0.1UF 20% 10V CERM 402
C832 0.1UF 20% 10V CERM 402
C900 0.1UF 20% 10V CERM 402
C888 0.1UF 20% 10V CERM 402
C891 0.1UF 20% 10V CERM 402
C844 0.1UF 20% 10V CERM 402
C824 0.1UF 20% 10V CERM 402
C872 0.1UF 20% 10V CERM 402
C874 0.1UF 20% 10V CERM 402
C899 0.1UF 20% 10V CERM 402
C901 0.1UF 20% 10V CERM 402
C823 0.1UF 20% 10V CERM 402
C845 0.1UF 20% 10V CERM 402
C871 0.1UF 20% 10V CERM 402
C834 0.1UF 20% 10V CERM 402
C884 0.1UF 20% 10V CERM 402
C896 0.1UF 20% 10V CERM 402
C898 0.1UF 20% 10V CERM 402
C886 0.1UF 20% 10V CERM 402
C846 0.1UF 20% 10V CERM 402
C885 0.1UF 20% 10V CERM 402
C887 0.1UF 20% 10V CERM 402
C870 0.1UF 20% 10V CERM 402
C897 0.1UF 20% 10V CERM 402
C889 0.1UF 20% 10V CERM 402
C842 0.1UF 20% 10V CERM 402
C895 0.1UF 20% 10V CERM 402
C869 0.1UF 20% 10V CERM 402
C873 0.1UF 20% 10V CERM 402
C902 0.1UF 20% 10V CERM 402
C843 0.1UF 20% 10V CERM 402
C278 0.1UF 20% 10V CERM 402
C849 0.1UF 20% 10V CERM 402
C281 0.1UF 20% 10V CERM 402
C280 0.1UF 20% 10V CERM 402
C279 0.1UF 20% 10V CERM 402

INTREPID CORE DECOUPLING

59C8> 47B2<> 46B3< 10D6< +INTREPID_CORE_MAIN

30 Balls
4 X 10UF (0805)
29 X 0.1UF (0402)

C702 10UF N20P80% 10V Y5V 805
C727 10UF N20P80% 10V Y5V 805
C292 10UF N20P80% 10V Y5V 805
C841 10UF N20P80% 10V Y5V 805
C787 0.1UF 20% 10V CERM 402
C789 0.1UF 20% 10V CERM 402
C749 0.1UF 20% 10V CERM 402
C797 0.1UF 20% 10V CERM 402
C719 0.1UF 20% 10V CERM 402
C800 0.1UF 20% 10V CERM 402
C810 0.1UF 20% 10V CERM 402
C766 0.1UF 20% 10V CERM 402
C731 0.1UF 20% 10V CERM 402
C732 0.1UF 20% 10V CERM 402
C764 0.1UF 20% 10V CERM 402
C831 0.1UF 20% 10V CERM 402
C833 0.1UF 20% 10V CERM 402
C765 0.1UF 20% 10V CERM 402
C808 0.1UF 20% 10V CERM 402
C763 0.1UF 20% 10V CERM 402
C780 0.1UF 20% 10V CERM 402
C798 0.1UF 20% 10V CERM 402
C779 0.1UF 20% 10V CERM 402
C790 0.1UF 20% 10V CERM 402
C746 0.1UF 20% 10V CERM 402
C730 0.1UF 20% 10V CERM 402
C721 0.1UF 20% 10V CERM 402
C788 0.1UF 20% 10V CERM 402
C734 0.1UF 20% 10V CERM 402
C748 0.1UF 20% 10V CERM 402
C811 0.1UF 20% 10V CERM 402
C747 0.1UF 20% 10V CERM 402
C799 0.1UF 20% 10V CERM 402

+2_5V_MAIN — INTREPID DDR DECOUPLING

44 Balls
4 X 10UF (0805)
51 X 0.1UF (0402)

C277 10UF N20P80% 10V Y5V 805
C271 10UF N20P80% 10V Y5V 805
C240 10UF N20P80% 10V Y5V 805
C641 10UF N20P80% 10V Y5V 805
C700 0.1UF 20% 10V CERM 402
C878 0.1UF 20% 10V CERM 402
C725 0.1UF 20% 10V CERM 402
C836 0.1UF 20% 10V CERM 402
C817 0.1UF 20% 10V CERM 402
C839 0.1UF 20% 10V CERM 402
C857 0.1UF 20% 10V CERM 402
C794 0.1UF 20% 10V CERM 402
C855 0.1UF 20% 10V CERM 402
C880 0.1UF 20% 10V CERM 402
C837 0.1UF 20% 10V CERM 402
C877 0.1UF 20% 10V CERM 402
C688 0.1UF 20% 10V CERM 402
C767 0.1UF 20% 10V CERM 402
C793 0.1UF 20% 10V CERM 402
C815 0.1UF 20% 10V CERM 402
C904 0.1UF 20% 10V CERM 402
C827 0.1UF 20% 10V CERM 402
C876 0.1UF 20% 10V CERM 402
C698 0.1UF 20% 10V CERM 402
C856 0.1UF 20% 10V CERM 402
C735 0.1UF 20% 10V CERM 402
C722 0.1UF 20% 10V CERM 402
C750 0.1UF 20% 10V CERM 402
C753 0.1UF 20% 10V CERM 402
C687 0.1UF 20% 10V CERM 402
C792 0.1UF 20% 10V CERM 402
C668 0.1UF 20% 10V CERM 402
C714 0.1UF 20% 10V CERM 402
C736 0.1UF 20% 10V CERM 402
C801 0.1UF 20% 10V CERM 402
C825 0.1UF 20% 10V CERM 402
C838 0.1UF 20% 10V CERM 402
C723 0.1UF 20% 10V CERM 402
C803 0.1UF 20% 10V CERM 402
C791 0.1UF 20% 10V CERM 402
C755 0.1UF 20% 10V CERM 402
C818 0.1UF 20% 10V CERM 402
C802 0.1UF 20% 10V CERM 402
C813 0.1UF 20% 10V CERM 402
C699 0.1UF 20% 10V CERM 402
C751 0.1UF 20% 10V CERM 402
C826 0.1UF 20% 10V CERM 402
C752 0.1UF 20% 10V CERM 402
C768 0.1UF 20% 10V CERM 402
C816 0.1UF 20% 10V CERM 402
C814 0.1UF 20% 10V CERM 402
C754 0.1UF 20% 10V CERM 402
C724 0.1UF 20% 10V CERM 402
C781 0.1UF 20% 10V CERM 402
C782 0.1UF 20% 10V CERM 402

+3V_MAIN — INTREPID 3.3V DECOUPLING

57 Balls
4 X 10UF (0805)
66 X 0.1UF (0402)

C655 10UF N20P80% 10V Y5V 805
C264 10UF N20P80% 10V Y5V 805
C892 10UF N20P80% 10V Y5V 805
C637 10UF N20P80% 10V Y5V 805
C745 0.1UF 20% 10V CERM 402
C830 0.1UF 20% 10V CERM 402
C775 0.1UF 20% 10V CERM 402
C717 0.1UF 20% 10V CERM 402
C829 0.1UF 20% 10V CERM 402
C806 0.1UF 20% 10V CERM 402
C691 0.1UF 20% 10V CERM 402
C762 0.1UF 20% 10V CERM 402
C777 0.1UF 20% 10V CERM 402
C796 0.1UF 20% 10V CERM 402
C867 0.1UF 20% 10V CERM 402
C866 0.1UF 20% 10V CERM 402
C863 0.1UF 20% 10V CERM 402
C868 0.1UF 20% 10V CERM 402
C812 0.1UF 20% 10V CERM 402
C821 0.1UF 20% 10V CERM 402
C822 0.1UF 20% 10V CERM 402
C893 0.1UF 20% 10V CERM 402
C720 0.1UF 20% 10V CERM 402
C728 0.1UF 20% 10V CERM 402
C809 0.1UF 20% 10V CERM 402
C680 0.1UF 20% 10V CERM 402
C894 0.1UF 20% 10V CERM 402
C643 0.1UF 20% 10V CERM 402
C656 0.1UF 20% 10V CERM 402
C689 0.1UF 20% 10V CERM 402
C774 0.1UF 20% 10V CERM 402
C828 0.1UF 20% 10V CERM 402
C850 0.1UF 20% 10V CERM 402
C743 0.1UF 20% 10V CERM 402
C761 0.1UF 20% 10V CERM 402
C707 0.1UF 20% 10V CERM 402
C883 0.1UF 20% 10V CERM 402
C807 0.1UF 20% 10V CERM 402
C776 0.1UF 20% 10V CERM 402
C744 0.1UF 20% 10V CERM 402
C718 0.1UF 20% 10V CERM 402
C712 0.1UF 20% 10V CERM 402
C835 0.1UF 20% 10V CERM 402
C729 0.1UF 20% 10V CERM 402
C881 0.1UF 20% 10V CERM 402
C676 0.1UF 20% 10V CERM 402
C716 0.1UF 20% 10V CERM 402
C805 0.1UF 20% 10V CERM 402
C644 0.1UF 20% 10V CERM 402
C645 0.1UF 20% 10V CERM 402
C865 0.1UF 20% 10V CERM 402
C882 0.1UF 20% 10V CERM 402
C708 0.1UF 20% 10V CERM 402
C681 0.1UF 20% 10V CERM 402
C678 0.1UF 20% 10V CERM 402
C682 0.1UF 20% 10V CERM 402
C879 0.1UF 20% 10V CERM 402
C903 0.1UF 20% 10V CERM 402
C673 0.1UF 20% 10V CERM 402
C679 0.1UF 20% 10V CERM 402
C677 0.1UF 20% 10V CERM 402
C660 0.1UF 20% 10V CERM 402
C657 0.1UF 20% 10V CERM 402
C851 0.1UF 20% 10V CERM 402
C875 0.1UF 20% 10V CERM 402
C659 0.1UF 20% 10V CERM 402
C690 0.1UF 20% 10V CERM 402
C658 0.1UF 20% 10V CERM 402
C852 0.1UF 20% 10V CERM 402
C646 0.1UF 20% 10V CERM 402

+1_5V_AGP — INTREPID AGP I/O DECOUPLING

52C3> 46B4<> 17D5< 17A4< 17A3< 16D7< 16C2< 16A8< 10D6< 59C8>

21 Balls
4 X 10UF (0805)
24 X 0.1UF (0402)

C231 10UF N20P80% 10V Y5V 805
C232 10UF N20P80% 10V Y5V 805
C638 10UF N20P80% 10V Y5V 805
C628 10UF N20P80% 10V Y5V 805
C697 0.1UF 20% 10V CERM 402
C693 0.1UF 20% 10V CERM 402
C684 0.1UF 20% 10V CERM 402
C686 0.1UF 20% 10V CERM 402
C709 0.1UF 20% 10V CERM 402
C649 0.1UF 20% 10V CERM 402
C667 0.1UF 20% 10V CERM 402
C694 0.1UF 20% 10V CERM 402
C695 0.1UF 20% 10V CERM 402
C664 0.1UF 20% 10V CERM 402
C733 0.1UF 20% 10V CERM 402
C650 0.1UF 20% 10V CERM 402
C647 0.1UF 20% 10V CERM 402
C710 0.1UF 20% 10V CERM 402
C685 0.1UF 20% 10V CERM 402
C683 0.1UF 20% 10V CERM 402
C665 0.1UF 20% 10V CERM 402
C696 0.1UF 20% 10V CERM 402
C666 0.1UF 20% 10V CERM 402
C651 0.1UF 20% 10V CERM 402
C662 0.1UF 20% 10V CERM 402
C661 0.1UF 20% 10V CERM 402
C648 0.1UF 20% 10V CERM 402
C674 0.1UF 20% 10V CERM 402
C711 0.1UF 20% 10V CERM 402
C663 0.1UF 20% 10V CERM 402

INTREPID BYPASS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6497	13

SCALE	SHT	OF
NONE	11	69

DRAWING

DDR MUX CONNECTIONS

0-ohm resistors to allow rewiring if necessary

SERIES RESISTORS FOR CONTROL SIGNALS

U25 INTREPID BGA (2 OF 9) SEE_TABLE (ON PAGE 12)

DDR MEMORY INTERFACE

'0'S ARE SAME POLARITY (ACTIVE LO)
'1'S ARE SAME POLARITY (ACTIVE HI)
SEL = 0; HOST=B PORT, A PORT = 100 OHMGND
SEL = 1; HOST=A PORT, B PORT = 100 OHMGND

LOCATE 2 DECOUPLING CAPS DIRECTLY AT DDR_VREF_X BALLS (U25-Y22 & T22)

LOCATE THESE RESISTORS NEAR INTREPID

INTREPID DDR CNTRL

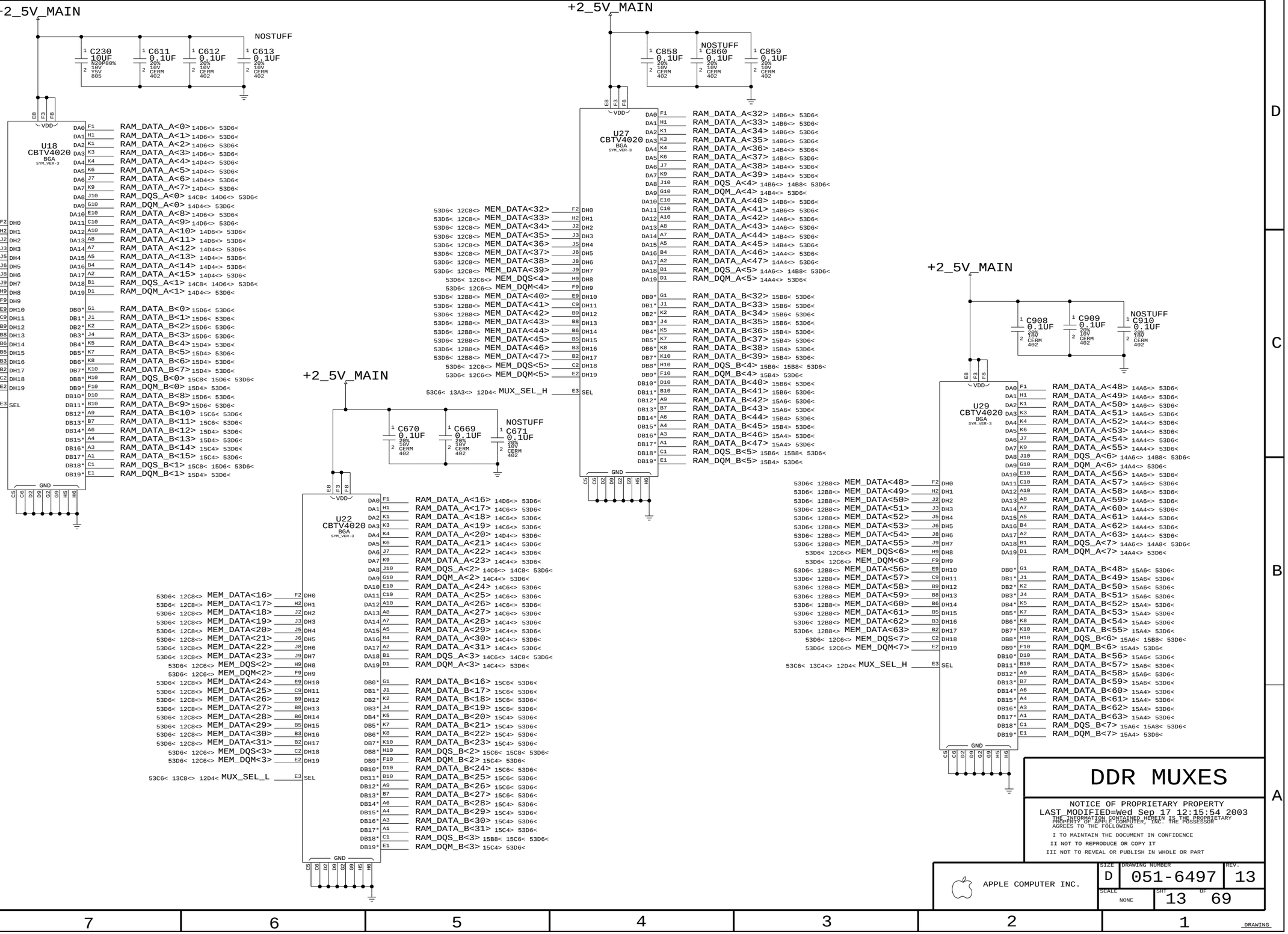
LAST_MODIFIED=Wed Sep 17 12:15:52 2003

APPLE COMPUTER INC.

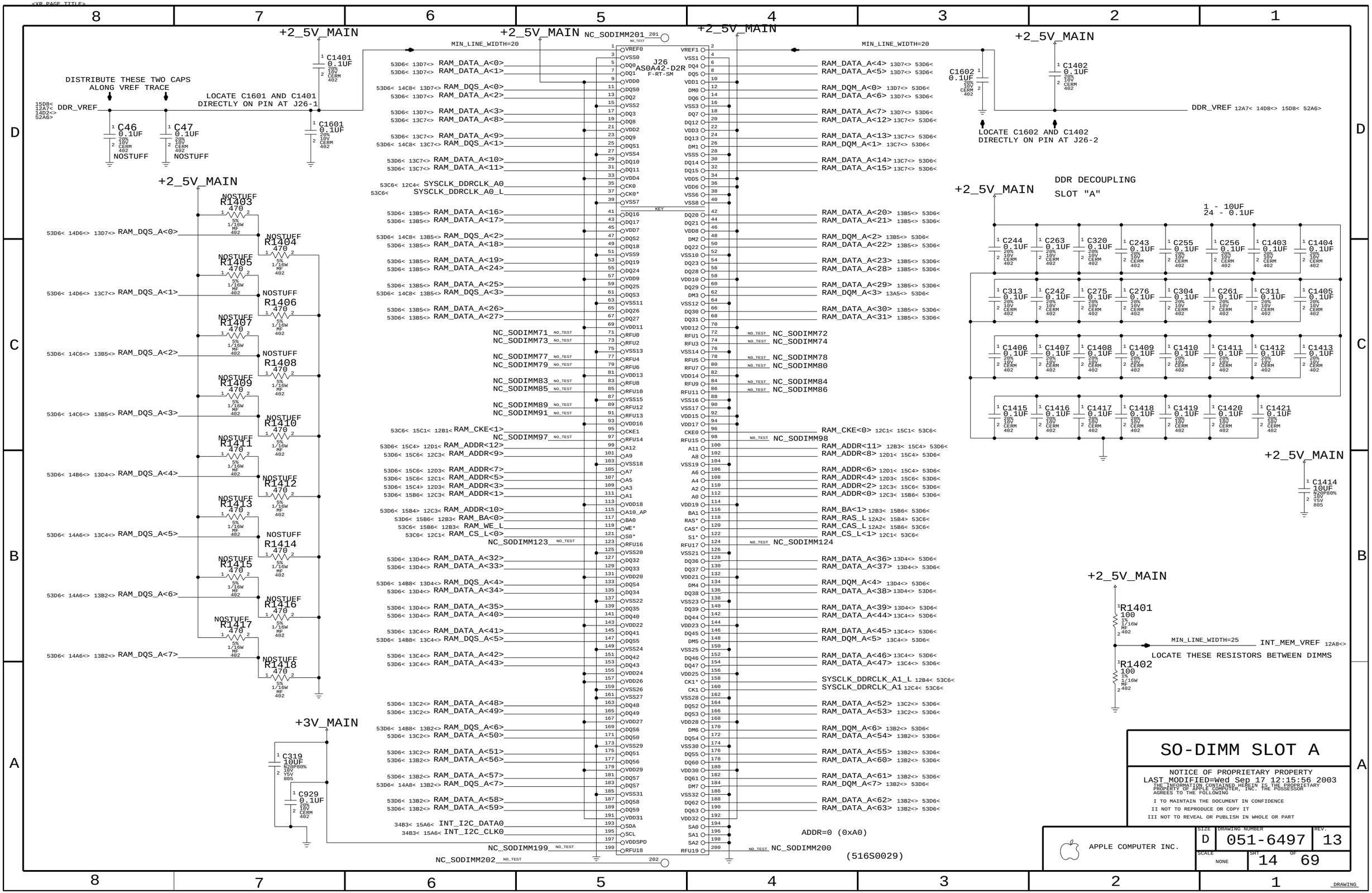
SIZE	DRAWING NUMBER	REV.
D	051-6497	13

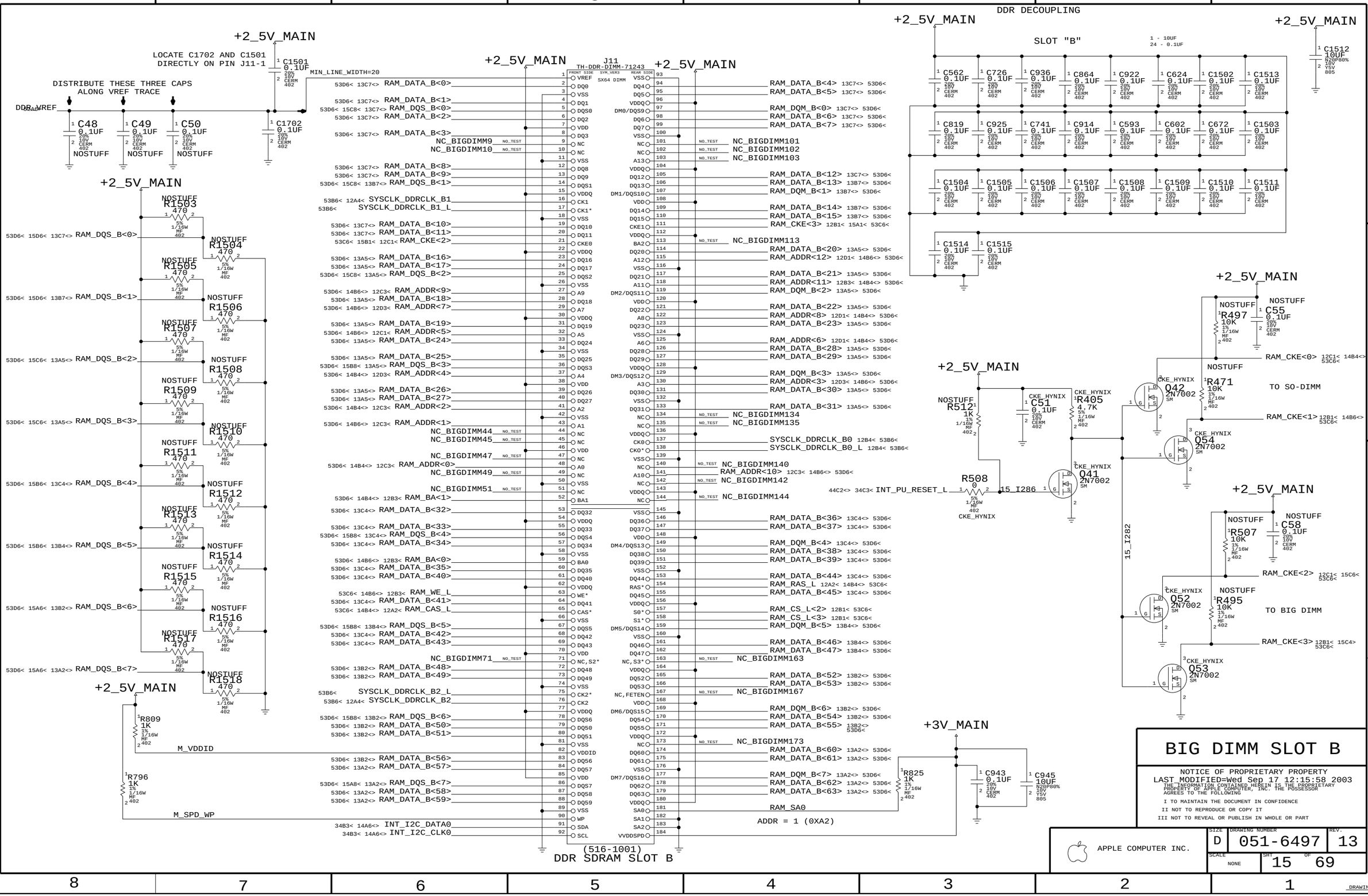
SCALE	SHT	OF
NONE	12	69

DRAWING


+2_5V_MAIN
C230 10UF N20P80% 10V 10V 805
C611 0.1UF 20% 10V CERM 402
C612 0.1UF 20% 10V CERM 402
C613 0.1UF 20% 10V CERM 402
NOSTUFF
U18 CBTV4020 BGA SYM_VER-3
RAM_DATA_A<0> 14D6<> 53D6<
RAM_DATA_A<1> 14D6<> 53D6<
RAM_DATA_A<2> 14D6<> 53D6<
RAM_DATA_A<3> 14D6<> 53D6<
RAM_DATA_A<4> 14D4<> 53D6<
RAM_DATA_A<5> 14D4<> 53D6<
RAM_DATA_A<6> 14D4<> 53D6<
RAM_DATA_A<7> 14D4<> 53D6<
RAM_DQS_A<0> 14C8< 14D6<> 53D6<
RAM_DQM_A<0> 14D4<> 53D6<
RAM_DATA_A<8> 14D6<> 53D6<
RAM_DATA_A<9> 14D6<> 53D6<
RAM_DATA_A<10> 14D6<> 53D6<
RAM_DATA_A<11> 14D6<> 53D6<
RAM_DATA_A<12> 14D4<> 53D6<
RAM_DATA_A<13> 14D4<> 53D6<
RAM_DATA_A<14> 14D4<> 53D6<
RAM_DATA_A<15> 14D4<> 53D6<
RAM_DQS_A<1> 14C8< 14D6<> 53D6<
RAM_DQM_A<1> 14D4<> 53D6<
MEM_DATA<0>
MEM_DATA<1>
MEM_DATA<2>
MEM_DATA<3>
MEM_DATA<4>
MEM_DATA<5>
MEM_DATA<6>
MEM_DATA<7>
MEM_DQS<0>
MEM_DQM<0>
MEM_DATA<8>
MEM_DATA<9>
MEM_DATA<10>
MEM_DATA<11>
MEM_DATA<12>
MEM_DATA<13>
MEM_DATA<14>
MEM_DATA<15>
MEM_DQS<1>
MEM_DQM<1>
MUX_SEL_L
RAM_DATA_B<0> 15D6< 53D6<
RAM_DATA_B<1> 15D6< 53D6<
RAM_DATA_B<2> 15D6< 53D6<
RAM_DATA_B<3> 15D6< 53D6<
RAM_DATA_B<4> 15D4> 53D6<
RAM_DATA_B<5> 15D4> 53D6<
RAM_DATA_B<6> 15D4> 53D6<
RAM_DATA_B<7> 15D4> 53D6<
RAM_DQS_B<0> 15C8< 15D6< 53D6<
RAM_DQM_B<0> 15D4> 53D6<
RAM_DATA_B<8> 15D6< 53D6<
RAM_DATA_B<9> 15D6< 53D6<
RAM_DATA_B<10> 15C6< 53D6<
RAM_DATA_B<11> 15C6< 53D6<
RAM_DATA_B<12> 15D4> 53D6<
RAM_DATA_B<13> 15D4> 53D6<
RAM_DATA_B<14> 15C4> 53D6<
RAM_DATA_B<15> 15C4> 53D6<
RAM_DQS_B<1> 15C8< 15D6< 53D6<
RAM_DQM_B<1> 15D4> 53D6<
GND
+2_5V_MAIN
C858 0.1UF 20% 10V CERM 402
NOSTUFF C860 0.1UF 20% 10V CERM 402
C859 0.1UF 20% 10V CERM 402
U27 CBTV4020 BGA SYM_VER-3
RAM_DATA_A<32> 14B6<> 53D6<
RAM_DATA_A<33> 14B6<> 53D6<
RAM_DATA_A<34> 14B6<> 53D6<
RAM_DATA_A<35> 14B6<> 53D6<
RAM_DATA_A<36> 14B4<> 53D6<
RAM_DATA_A<37> 14B4<> 53D6<
RAM_DATA_A<38> 14B4<> 53D6<
RAM_DATA_A<39> 14B4<> 53D6<
RAM_DQS_A<4> 14B6<> 14B8< 53D6<
RAM_DQM_A<4> 14B4<> 53D6<
RAM_DATA_A<40> 14B6<> 53D6<
RAM_DATA_A<41> 14B6<> 53D6<
RAM_DATA_A<42> 14A6<> 53D6<
RAM_DATA_A<43> 14A6<> 53D6<
RAM_DATA_A<44> 14B4<> 53D6<
RAM_DATA_A<45> 14B4<> 53D6<
RAM_DATA_A<46> 14A4<> 53D6<
RAM_DATA_A<47> 14A4<> 53D6<
RAM_DQS_A<5> 14A6<> 14B8< 53D6<
RAM_DQM_A<5> 14A4<> 53D6<
MEM_DATA<32>
MEM_DATA<33>
MEM_DATA<34>
MEM_DATA<35>
MEM_DATA<36>
MEM_DATA<37>
MEM_DATA<38>
MEM_DATA<39>
MEM_DQS<4>
MEM_DQM<4>
MEM_DATA<40>
MEM_DATA<41>
MEM_DATA<42>
MEM_DATA<43>
MEM_DATA<44>
MEM_DATA<45>
MEM_DATA<46>
MEM_DATA<47>
MEM_DQS<5>
MEM_DQM<5>
MUX_SEL_H
RAM_DATA_B<32> 15B6< 53D6<
RAM_DATA_B<33> 15B6< 53D6<
RAM_DATA_B<34> 15B6< 53D6<
RAM_DATA_B<35> 15B6< 53D6<
RAM_DATA_B<36> 15B4> 53D6<
RAM_DATA_B<37> 15B4> 53D6<
RAM_DATA_B<38> 15B4> 53D6<
RAM_DATA_B<39> 15B4> 53D6<
RAM_DQS_B<4> 15B6< 15B8< 53D6<
RAM_DQM_B<4> 15B4> 53D6<
RAM_DATA_B<40> 15B6< 53D6<
RAM_DATA_B<41> 15B6< 53D6<
RAM_DATA_B<42> 15A6< 53D6<
RAM_DATA_B<43> 15A6< 53D6<
RAM_DATA_B<44> 15B4> 53D6<
RAM_DATA_B<45> 15B4> 53D6<
RAM_DATA_B<46> 15A4> 53D6<
RAM_DATA_B<47> 15A4> 53D6<
RAM_DQS_B<5> 15B6< 15B8< 53D6<
RAM_DQM_B<5> 15B4> 53D6<
+2_5V_MAIN
C670 0.1UF 20% 10V CERM 402
C669 0.1UF 20% 10V CERM 402
NOSTUFF C671 0.1UF 20% 10V CERM 402
U22 CBTV4020 BGA SYM_VER-3
RAM_DATA_A<16> 14C6<> 53D6<
RAM_DATA_A<17> 14C6<> 53D6<
RAM_DATA_A<18> 14C6<> 53D6<
RAM_DATA_A<19> 14C6<> 53D6<
RAM_DATA_A<20> 14D4<> 53D6<
RAM_DATA_A<21> 14C4<> 53D6<
RAM_DATA_A<22> 14C4<> 53D6<
RAM_DATA_A<23> 14C4<> 53D6<
RAM_DQS_A<2> 14C6<> 14C8< 53D6<
RAM_DQM_A<2> 14C4<> 53D6<
RAM_DATA_A<24> 14C6<> 53D6<
RAM_DATA_A<25> 14C6<> 53D6<
RAM_DATA_A<26> 14C6<> 53D6<
RAM_DATA_A<27> 14C6<> 53D6<
RAM_DATA_A<28> 14C4<> 53D6<
RAM_DATA_A<29> 14C4<> 53D6<
RAM_DATA_A<30> 14C4<> 53D6<
RAM_DATA_A<31> 14C4<> 53D6<
RAM_DQS_A<3> 14C6<> 14C8< 53D6<
RAM_DQM_A<3> 14C4<> 53D6<
MEM_DATA<16>
MEM_DATA<17>
MEM_DATA<18>
MEM_DATA<19>
MEM_DATA<20>
MEM_DATA<21>
MEM_DATA<22>
MEM_DATA<23>
MEM_DQS<2>
MEM_DQM<2>
MEM_DATA<24>
MEM_DATA<25>
MEM_DATA<26>
MEM_DATA<27>
MEM_DATA<28>
MEM_DATA<29>
MEM_DATA<30>
MEM_DATA<31>
MEM_DQS<3>
MEM_DQM<3>
MUX_SEL_L
RAM_DATA_B<16> 15C6< 53D6<
RAM_DATA_B<17> 15C6< 53D6<
RAM_DATA_B<18> 15C6< 53D6<
RAM_DATA_B<19> 15C6< 53D6<
RAM_DATA_B<20> 15C4> 53D6<
RAM_DATA_B<21> 15C4> 53D6<
RAM_DATA_B<22> 15C4> 53D6<
RAM_DATA_B<23> 15C4> 53D6<
RAM_DQS_B<2> 15C6< 15C8< 53D6<
RAM_DQM_B<2> 15C4> 53D6<
RAM_DATA_B<24> 15C6< 53D6<
RAM_DATA_B<25> 15C6< 53D6<
RAM_DATA_B<26> 15C6< 53D6<
RAM_DATA_B<27> 15C6< 53D6<
RAM_DATA_B<28> 15C4> 53D6<
RAM_DATA_B<29> 15C4> 53D6<
RAM_DATA_B<30> 15C4> 53D6<
RAM_DATA_B<31> 15C4> 53D6<
RAM_DQS_B<3> 15B8< 15C6< 53D6<
RAM_DQM_B<3> 15C4> 53D6<
+2_5V_MAIN
C908 0.1UF 20% 10V CERM 402
C909 0.1UF 20% 10V CERM 402
NOSTUFF C910 0.1UF 20% 10V CERM 402
U29 CBTV4020 BGA SYM_VER-3
RAM_DATA_A<48> 14A6<> 53D6<
RAM_DATA_A<49> 14A6<> 53D6<
RAM_DATA_A<50> 14A6<> 53D6<
RAM_DATA_A<51> 14A6<> 53D6<
RAM_DATA_A<52> 14A4<> 53D6<
RAM_DATA_A<53> 14A4<> 53D6<
RAM_DATA_A<54> 14A4<> 53D6<
RAM_DATA_A<55> 14A4<> 53D6<
RAM_DQS_A<6> 14A6<> 14B8< 53D6<
RAM_DQM_A<6> 14A4<> 53D6<
RAM_DATA_A<56> 14A6<> 53D6<
RAM_DATA_A<57> 14A6<> 53D6<
RAM_DATA_A<58> 14A6<> 53D6<
RAM_DATA_A<59> 14A6<> 53D6<
RAM_DATA_A<60> 14A4<> 53D6<
RAM_DATA_A<61> 14A4<> 53D6<
RAM_DATA_A<62> 14A4<> 53D6<
RAM_DATA_A<63> 14A4<> 53D6<
RAM_DQS_A<7> 14A6<> 14A8< 53D6<
RAM_DQM_A<7> 14A4<> 53D6<
MEM_DATA<48>
MEM_DATA<49>
MEM_DATA<50>
MEM_DATA<51>
MEM_DATA<52>
MEM_DATA<53>
MEM_DATA<54>
MEM_DATA<55>
MEM_DQS<6>
MEM_DQM<6>
MEM_DATA<56>
MEM_DATA<57>
MEM_DATA<58>
MEM_DATA<59>
MEM_DATA<60>
MEM_DATA<61>
MEM_DATA<62>
MEM_DATA<63>
MEM_DQS<7>
MEM_DQM<7>
MUX_SEL_H
RAM_DATA_B<48> 15A6< 53D6<
RAM_DATA_B<49> 15A6< 53D6<
RAM_DATA_B<50> 15A6< 53D6<
RAM_DATA_B<51> 15A6< 53D6<
RAM_DATA_B<52> 15A4> 53D6<
RAM_DATA_B<53> 15A4> 53D6<
RAM_DATA_B<54> 15A4> 53D6<
RAM_DATA_B<55> 15A4> 53D6<
RAM_DQS_B<6> 15A6< 15B8< 53D6<
RAM_DQM_B<6> 15A4> 53D6<
RAM_DATA_B<56> 15A6< 53D6<
RAM_DATA_B<57> 15A6< 53D6<
RAM_DATA_B<58> 15A6< 53D6<
RAM_DATA_B<59> 15A6< 53D6<
RAM_DATA_B<60> 15A4> 53D6<
RAM_DATA_B<61> 15A4> 53D6<
RAM_DATA_B<62> 15A4> 53D6<
RAM_DATA_B<63> 15A4> 53D6<
RAM_DQS_B<7> 15A6< 15A8< 53D6<
RAM_DQM_B<7> 15A4> 53D6<
DDR MUXES
NOTICE OF PROPRIETARY PROPERTY
LAST_MODIFIED=Wed Sep 17 12:15:54 2003
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-6497
REV. 13
SCALE NONE
SHT 13 OF 69
DRAWING

<XR_PAGE_TITLE>




+2_5V_MAIN
LOCATE C1702 AND C1501
DIRECTLY ON PIN J11-1
C1501 0.1UF
MIN_LINE_WIDTH=20
DISTRIBUTE THESE THREE CAPS
ALONG VREF TRACE
DDR_VREF
C48 0.1UF NOSTUFF
C49 0.1UF NOSTUFF
C50 0.1UF NOSTUFF
C1702 0.1UF
+2_5V_MAIN
NOSTUFF R1503 470
NOSTUFF R1504 470
NOSTUFF R1505 470
NOSTUFF R1506 470
NOSTUFF R1507 470
NOSTUFF R1508 470
NOSTUFF R1509 470
NOSTUFF R1510 470
NOSTUFF R1511 470
NOSTUFF R1512 470
NOSTUFF R1513 470
NOSTUFF R1514 470
NOSTUFF R1515 470
NOSTUFF R1516 470
NOSTUFF R1517 470
NOSTUFF R1518 470
53D6< 15D6< 13C7< RAM_DQS_B<0>
53D6< 15D6< 13B7< RAM_DQS_B<1>
53D6< 15C6< 13A5< RAM_DQS_B<2>
53D6< 15C6< 13A5< RAM_DQS_B<3>
53D6< 15B6< 13C4< RAM_DQS_B<4>
53D6< 15B6< 13B4< RAM_DQS_B<5>
53D6< 15A6< 13B2< RAM_DQS_B<6>
53D6< 15A6< 13A2< RAM_DQS_B<7>
+2_5V_MAIN
R809 1K
M_VDDID
R796 1K
M_SPD_WP
J11
TH-DDR-DIMM-71243
SX64 DIMM
FRONT SIDE
REAR SIDE
VREF
VSS
DQ0
DQ1
DQS0
DQ2
VDD
DQ3
NC
VSS
DQ8
DQ9
DQS1
VDDQ
CK1
CK1*
VSS
DQ10
DQ11
CKE0
VDDQ
DQ16
DQ17
DQS2
VSS
A9
DQ18
A7
VDDQ
DQ19
A5
DQ24
VSS
DQ25
DQS3
A4
VDD
DQ26
DQ27
A2
VSS
A1
NC
NC
VDD
NC
NC
VSS
NC
BA1
DQ32
VDDQ
DQ33
DQS4
DQ34
VSS
BA0
DQ35
DQ40
VDDQ
WE*
DQ41
CAS*
VSS
DQS5
DQ42
DQ43
VDD
NC,S2*
DQ48
DQ49
VSS
CK2*
CK2
VDDQ
DQS6
DQ50
DQ51
VSS
VDDID
DQ56
DQ57
VDD
DQS7
DQ58
DQ59
VSS
WP
SDA
SCL
RAM_DATA_B<0>
RAM_DATA_B<1>
RAM_DQS_B<0>
RAM_DATA_B<2>
RAM_DATA_B<3>
NC_BIGDIMM9 NO_TEST
NC_BIGDIMM10 NO_TEST
RAM_DATA_B<8>
RAM_DATA_B<9>
RAM_DQS_B<1>
SYSCLK_DDRCLK_B1
SYSCLK_DDRCLK_B1_L
RAM_DATA_B<10>
RAM_DATA_B<11>
RAM_CKE<2>
RAM_DATA_B<16>
RAM_DATA_B<17>
RAM_DQS_B<2>
RAM_ADDR<9>
RAM_DATA_B<18>
RAM_ADDR<7>
RAM_DATA_B<19>
RAM_ADDR<5>
RAM_DATA_B<24>
RAM_DATA_B<25>
RAM_DQS_B<3>
RAM_ADDR<4>
RAM_DATA_B<26>
RAM_DATA_B<27>
RAM_ADDR<2>
RAM_ADDR<1>
NC_BIGDIMM44 NO_TEST
NC_BIGDIMM45 NO_TEST
NC_BIGDIMM47 NO_TEST
RAM_ADDR<0>
NC_BIGDIMM49 NO_TEST
NC_BIGDIMM51 NO_TEST
RAM_BA<1>
RAM_DATA_B<32>
RAM_DATA_B<33>
RAM_DQS_B<4>
RAM_DATA_B<34>
RAM_BA<0>
RAM_DATA_B<35>
RAM_DATA_B<40>
RAM_WE_L
RAM_DATA_B<41>
RAM_CAS_L
RAM_DQS_B<5>
RAM_DATA_B<42>
RAM_DATA_B<43>
NC_BIGDIMM71 NO_TEST
RAM_DATA_B<48>
RAM_DATA_B<49>
SYSCLK_DDRCLK_B2_L
SYSCLK_DDRCLK_B2
RAM_DQS_B<6>
RAM_DATA_B<50>
RAM_DATA_B<51>
RAM_DATA_B<56>
RAM_DATA_B<57>
RAM_DQS_B<7>
RAM_DATA_B<58>
RAM_DATA_B<59>
INT_I2C_DATA0
INT_I2C_CLK0
(516-1001)
DDR SDRAM SLOT B
+2_5V_MAIN
VSS
DQ4
DQ5
VDDQ
DM0/DQS9
DQ6
DQ7
VSS
NC
NC
A13
VDDQ
DQ12
DQ13
DM1/DQS10
VDD
DQ14
DQ15
CKE1
VDDQ
BA2
DQ20
A12
VSS
DQ21
A11
DM2/DQS11
VDD
DQ22
A8
DQ23
VSS
A6
DQ28
DQ29
VDDQ
DM3/DQS12
A3
DQ30
VSS
DQ31
NC
NC
VDDQ
CK0
CK0*
VSS
NC
A10
NC
VDDQ
NC
VSS
DQ36
DQ37
VDD
DM4/DQS13
DQ38
DQ39
VSS
DQ44
RAS*
DQ45
VDDQ
S0*
S1*
DM5/DQS14
VSS
DQ46
DQ47
NC,S3*
VDDQ
DQ52
DQ53
NC,FETEN
VDD
DM6/DQS15
DQ54
DQ55
VDDQ
NC
DQ60
DQ61
VSS
DM7/DQS16
DQ62
DQ63
VDDQ
SA0
SA1
SA2
VVDDSPD
RAM_DATA_B<4> 13C7<> 53D6<
RAM_DATA_B<5> 13C7<> 53D6<
RAM_DQM_B<0> 13C7<> 53D6<
RAM_DATA_B<6> 13C7<> 53D6<
RAM_DATA_B<7> 13C7<> 53D6<
NC_BIGDIMM101 NO_TEST
NC_BIGDIMM102 NO_TEST
NC_BIGDIMM103 NO_TEST
RAM_DATA_B<12> 13C7<> 53D6<
RAM_DATA_B<13> 13B7<> 53D6<
RAM_DQM_B<1> 13B7<> 53D6<
RAM_DATA_B<14> 13B7<> 53D6<
RAM_DATA_B<15> 13B7<> 53D6<
RAM_CKE<3> 12B1< 15A1< 53C6<
NC_BIGDIMM113 NO_TEST
RAM_DATA_B<20> 13A5<> 53D6<
RAM_ADDR<12> 12D1< 14B6<> 53D6<
RAM_DATA_B<21> 13A5<> 53D6<
RAM_ADDR<11> 12B3< 14B4<> 53D6<
RAM_DQM_B<2> 13A5<> 53D6<
RAM_DATA_B<22> 13A5<> 53D6<
RAM_ADDR<8> 12D1< 14B4<> 53D6<
RAM_DATA_B<23> 13A5<> 53D6<
RAM_ADDR<6> 12D1< 14B4<> 53D6<
RAM_DATA_B<28> 13A5<> 53D6<
RAM_DATA_B<29> 13A5<> 53D6<
RAM_DQM_B<3> 13A5<> 53D6<
RAM_ADDR<3> 12D3< 14B6<> 53D6<
RAM_DATA_B<30> 13A5<> 53D6<
RAM_DATA_B<31> 13A5<> 53D6<
NC_BIGDIMM134 NO_TEST
NC_BIGDIMM135 NO_TEST
SYSCLK_DDRCLK_B0 12B4< 53B6<
SYSCLK_DDRCLK_B0_L 12B4< 53B6<
NC_BIGDIMM140 NO_TEST
RAM_ADDR<10> 12C3< 14B6<> 53D6<
NC_BIGDIMM142 NO_TEST
NC_BIGDIMM144 NO_TEST
RAM_DATA_B<36> 13C4<> 53D6<
RAM_DATA_B<37> 13C4<> 53D6<
RAM_DQM_B<4> 13C4<> 53D6<
RAM_DATA_B<38> 13C4<> 53D6<
RAM_DATA_B<39> 13C4<> 53D6<
RAM_DATA_B<44> 13C4<> 53D6<
RAM_RAS_L 12A2< 14B4<> 53C6<
RAM_DATA_B<45> 13C4<> 53D6<
RAM_CS_L<2> 12B1< 53C6<
RAM_CS_L<3> 12B1< 53C6<
RAM_DQM_B<5> 13B4<> 53D6<
RAM_DATA_B<46> 13B4<> 53D6<
RAM_DATA_B<47> 13B4<> 53D6<
NC_BIGDIMM163 NO_TEST
RAM_DATA_B<52> 13B2<> 53D6<
RAM_DATA_B<53> 13B2<> 53D6<
NC_BIGDIMM167 NO_TEST
RAM_DQM_B<6> 13B2<> 53D6<
RAM_DATA_B<54> 13B2<> 53D6<
RAM_DATA_B<55> 13B2<> 53D6<
NC_BIGDIMM173 NO_TEST
RAM_DATA_B<60> 13A2<> 53D6<
RAM_DATA_B<61> 13A2<> 53D6<
RAM_DQM_B<7> 13A2<> 53D6<
RAM_DATA_B<62> 13A2<> 53D6<
RAM_DATA_B<63> 13A2<> 53D6<
RAM_SA0
ADDR = 1 (0XA2)
+3V_MAIN
R825 1K
C943 0.1UF
C945 10UF
DDR DECOUPLING
+2_5V_MAIN
SLOT "B"
1 - 10UF
24 - 0.1UF
C1512 10UF
C562 C726 C936 C864 C922 C624 C1502 C1513 0.1UF
C819 C925 C741 C914 C593 C602 C672 C1503 0.1UF
C1504 C1505 C1506 C1507 C1508 C1509 C1510 C1511 0.1UF
C1514 C1515 0.1UF
+2_5V_MAIN
NOSTUFF R497 10K
NOSTUFF C55 0.1UF
RAM_CKE<0> 12C1< 14B4<> 53C6<
NOSTUFF
R471 10K
TO SO-DIMM
RAM_CKE<1> 12B1< 14B6<> 53C6<
+2_5V_MAIN
NOSTUFF R507 10K
NOSTUFF C58 0.1UF
RAM_CKE<2> 12C1< 15C6< 53C6<
NOSTUFF
R495 10K
TO BIG DIMM
RAM_CKE<3> 12B1< 15C4> 53C6<
+2_5V_MAIN
NOSTUFF R512 1K
CKE_HYNIX C51 0.1UF
CKE_HYNIX R405 4.7K
R508 0
44C2<> 34C3< INT_PU_RESET_L
15_I286
15_I282
CKE_HYNIX Q42 2N7002 SM
CKE_HYNIX Q54 2N7002 SM
CKE_HYNIX Q41 2N7002 SM
CKE_HYNIX Q52 2N7002 SM
CKE_HYNIX Q53 2N7002 SM
BIG DIMM SLOT B
NOTICE OF PROPRIETARY PROPERTY
LAST_MODIFIED=Wed Sep 17 12:15:58 2003
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-6497
REV: 13
SCALE NONE
SHT 15 OF 69
DRAWING

INTREPID AGP CLK IS 1.5V OUT
NEED 3.3V SWING FOR VIDEO CHIPS
VERSION 1 WORKAROUND IS LA CLOCK
VERSION 2 WORKAROUND IS UNUSED PIN

THESE RESISTORS SHARE THE SAME PAD

2" LONGER (0.5NS SLOWER) AGP (ZERO DELAY) 2" SHORTER (0.5NS FASTER)

PLACE ALL SERPENTINES ON INTERNAL LAYER

AGP INTERFACES

VOUT = AGPIO (1.5V)
VIN = VCORE (1.5V)

AGP PULL-UPS/PULL DOWNS

GPU AGP I/O REFERENCE
(PLACE CLOSE TO GPU AGP BALLS)

INTREPID AGP

LAST MODIFIED=Wed Sep 17 12:16:00 2003

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6497	13
SCALE: NONE	SHT 16 OF 69	

U39
NV18B
BGA
(1 OF 5)

+1_5V_AGP

AGP_AD<0> AGP_AD<1> AGP_AD<2> AGP_AD<3> AGP_AD<7> AGP_AD<5> AGP_AD<6> AGP_AD<4> AGP_AD<8> AGP_AD<9> AGP_AD<10> AGP_AD<11> AGP_AD<12> AGP_AD<13> AGP_AD<14> AGP_AD<15> AGP_AD<16> AGP_AD<18> AGP_AD<17> AGP_AD<19> AGP_AD<20> AGP_AD<21> AGP_AD<22> AGP_AD<23> AGP_AD<24> AGP_AD<25> AGP_AD<26> AGP_AD<27> AGP_AD<28> AGP_AD<29> AGP_AD<30> AGP_AD<31>

RP40 22 5% 1/16W SM1
RP30 22 5% 1/16W SM1
RP32 22 5% 1/16W SM1
RP42 22 5% 1/16W SM1
RP31 22 5% 1/16W SM1
RP41 22 5% 1/16W SM1
RP44 22 5% 1/16W SM1
RP34 22 5% 1/16W SM1

GPU_AGP_AD<0> GPU_AGP_AD<1> GPU_AGP_AD<2> GPU_AGP_AD<3> GPU_AGP_AD<4> GPU_AGP_AD<5> GPU_AGP_AD<6> GPU_AGP_AD<7> GPU_AGP_AD<8> GPU_AGP_AD<9> GPU_AGP_AD<10> GPU_AGP_AD<11> GPU_AGP_AD<12> GPU_AGP_AD<13> GPU_AGP_AD<14> GPU_AGP_AD<15> GPU_AGP_AD<16> GPU_AGP_AD<17> GPU_AGP_AD<18> GPU_AGP_AD<19> GPU_AGP_AD<20> GPU_AGP_AD<21> GPU_AGP_AD<22> GPU_AGP_AD<23> GPU_AGP_AD<24> GPU_AGP_AD<25> GPU_AGP_AD<26> GPU_AGP_AD<27> GPU_AGP_AD<28> GPU_AGP_AD<29> GPU_AGP_AD<30> GPU_AGP_AD<31>

AGP_CBE<0> AGP_CBE<3> AGP_CBE<2> AGP_CBE<1>

RP43 22 5% 1/16W SM1

GPU_AGP_CBE<0> GPU_AGP_CBE<1> GPU_AGP_CBE<2> GPU_AGP_CBE<3>

R1026 0 402 5%
R1027 0 402 5%
TMDS_XMIT_SI_P

MAIN_RESET_L
AGP_RESET_L
CLK66M_GPU_AGP
NV_PCI_RST_L
AGP_GNT_L
AGP_REQ_L

AGP_TRDY_L AGP_FRAME_L AGP_IRDY_L AGP_PAR AGP_STOP_L AGP_DEVSEL_L

RP45 22 5% 1/16W SM1
RP35 22 5% 1/16W SM1

GPU_AGP_TRDY_L GPU_AGP_FRAME_L GPU_AGP_IRDY_L GPU_AGP_DEVSEL_L GPU_AGP_STOP_L GPU_AGP_PAR

AGP_INT_L
NC_GPU_INTB_L

AGP_WBF_L AGP_PIPE_L AGP_RBF_L

RP46 22 5% 1/16W SM1

GPU_AGP_RBF_L GPU_AGP_WBF_L GPU_AGP_PIPE_L NC_GPU_DBI_LO

AGP_ST<0> AGP_ST<1> AGP_ST<2>

AGP_AD_STB<0> AGP_AD_STB_L<0> AGP_AD_STB_L<1> AGP_AD_STB<1>

RP33 22 5% 1/16W SM1

GPU_AGP_AD_STB_GPUUF<0> GPU_AGP_AD_STB_L_GPUUF<0> GPU_AGP_AD_STB_GPUUF<1> GPU_AGP_AD_STB_L_GPUUF<1>

AGP_SB_STB AGP_SB_STB_L

R210 22
R558 22

GPU_AGP_SB_STB GPU_AGP_SB_STB_L

AGP_SBA<3> AGP_SBA<2> AGP_SBA<1> AGP_SBA<0> AGP_SBA<7> AGP_SBA<6> AGP_SBA<4> AGP_SBA<5>

RP47 22 5% 1/16W SM1
RP36 22 5% 1/16W SM1

GPU_AGP_SBA<0> GPU_AGP_SBA<1> GPU_AGP_SBA<2> GPU_AGP_SBA<3> GPU_AGP_SBA<4> GPU_AGP_SBA<5> GPU_AGP_SBA<6> GPU_AGP_SBA<7>

GPU_MBDET_L

AGP_BUSY_L STOP_AGP_L GPU_AGP_VREF

PCIAD0		
PCIAD1		
PCIAD2		
PCIAD3		
PCIAD4		
PCIAD5		
PCIAD6		
PCIAD7		
PCIAD8		
PCIAD9		
PCIAD10		
PCIAD11		
PCIAD12		
PCIAD13		
PCIAD14		
PCIAD15		
PCIAD16		
PCIAD17		
PCIAD18		
PCIAD19		
PCIAD20		
PCIAD21		
PCIAD22		
PCIAD23		
PCIAD24		
PCIAD25		
PCIAD26		
PCIAD27		
PCIAD28		
PCIAD29		
PCIAD30		
PCIAD31		
AGP 2X,4X	:	AGP 8X
PCIC0/BE0*	:	C0*/BE0
PCIC1/BE1*	:	C1*/BE1
PCIC2/BE2*	:	C2*/BE2
PCIC3/BE3*	:	C3*/BE3
PCICLK	:	CLK
PCIRST*	:	RST*
PCIGNT*	:	GNT
PCIREQ*	:	REQ
PCIFRAME*	:	FRAME
PCIIRDY*	:	IRDY
PCITRDY*	:	TRDY
PCIDEVSEL*	:	DEVSEL
PCISTOP*	:	STOP
PCIPAR	:	PAR
PCIINTA*	:	INTA
NC_PCIINTB*	:	INTB
AGPRBF*	:	RBF
AGPWBF*	:	WBF
AGPPIPE*	:	DBI_HI
<RESRVD>	:	DBI_LO
AGPST0	:	ST0
AGPST1	:	ST1
AGPST2	:	ST2
AGPADSTBF0	:	ADSTBF0
AGPADSTBS0*	:	ADSTBS0
AGPADSTBF1	:	ADSTBF1
AGPADSTBS1*	:	ADSTBS1
AGPSBSTBF	:	SBSTBF
AGPSBSTBS*	:	SBSTBS
AGPSBA0	:	SBA0*
AGPSBA1	:	SBA1*
AGPSBA2	:	SBA2*
AGPSBA3	:	SBA3*
AGPSBA4	:	SBA4*
AGPSBA5	:	SBA5*
AGPSBA6	:	SBA6*
AGPSBA7	:	SBA7*
<RESRVD>	:	MBDET*
AGPBUSY*	:	BUSY*
AGPSTOP*	:	STOP*
AGPVREF	:	AGPVREF

AGPVDDQ
VDD
VDD33
AGP_PLLVDD
VD50CLAMP0
VD50CLAMP1

50 OHM TO VDDQ AGPCALPD
50 OHM TO GND AGPCALPU
10K OHM TO GND TESTMODE

GPU_50PULLUP
GPU_50PULLDWN
GPU_TMODE

R177 10K 1% 1/16W MF 402
R160 49.9 1% 1/16W MF 402
R169 49.9 1% 1/16W MF 402

NC
NC_GPU<0> NC_GPU<1> NC_GPU<2> NC_GPU<3> NC_GPU<4>
ALL ARE NO_TEST

TCLK TMS TDI TDO TRST*
NVAGP_TRST_L NVAGP_TDO NVAGP_TDI NVAGP_TMS NVAGP_TCLK

R72 10K
R80 10K

R1024 10K NV34
R1025 10K NV34

+3V_MAIN

R168 10K 1% 1/16W MF 402

AGP VERSION SELECT
(LOW = AGP V3.X)
(HIGH = AGP V2.X)

OUTPUT DRIVER BYPASS

MIN_LINE_WIDTH=20

C192 0.01UF C200 0.01UF C178 0.1UF C201 0.1UF C202 0.1UF C180 0.1UF C185 0.1UF C203 0.1UF C183 0.1UF C176 0.1UF

10% 16V CERM 402

CORE BYPASS

GRAPH_CORE

C104 0.01UF C134 0.01UF C117 0.1UF C109 0.1UF C100 0.1UF C101 0.1UF C103 0.1UF C110 0.1UF C139 0.1UF C99 0.1UF C146 0.1UF

C148 0.01UF C149 0.01UF C150 0.1UF C147 0.1UF C118 0.1UF C135 0.1UF C169 0.1UF C140 0.1UF

C161 10UF N20P80% 10V Y5V 805
C93 10UF N20P80% 10V Y5V 805
C168 10UF N20P80% 10V Y5V 805
C94 10UF N20P80% 10V Y5V 805
C120 0.1UF C102 0.1UF C151 0.1UF

20% 10V CERM 402

+3V_MAIN
R198 10 1% 1/16W MF 402

C223 4.7UF N20P80% 10V CERM 805
C219 0.1UF 20% 10V CERM 402
C217 0.001UF 10% 50V CERM 402

I/O BYPASS

C177 0.01UF C111 0.01UF C129 0.1UF C136 0.1UF C116 0.1UF C87 0.1UF C184 0.1UF

C137 10UF N20P80% 10V Y5V 805
C91 0.01UF C97 0.01UF C187 0.1UF C179 0.1UF C105 0.1UF C112 0.1UF C181 0.1UF C182 0.1UF C188 0.1UF

10% 16V CERM 402

+5V_MAIN
C193 0.1UF C186 0.1UF 20% 10V CERM 402

GPU AGP I/O REFERENCE
(PLACE CLOSE TO INTREPID AGP BALLS)

+1_5V_AGP
C214 470PF 10% 50V CERM 402
R195 4.99K 1% 1/16W MF 402
R192 82.5 1% 1/16W MF 402
GPU_AGP_VREF_X

GPU_AGP_VREF
R196 4.99K 1% 1/16W MF 402
R193 82.5 1% 1/16W MF 402

C215 470PF 10% 50V CERM 402
GPU_AGP_VREF_Y

NVIDIA AGP

APPLE COMPUTER INC.
SIZE D | DRAWING NUMBER 051-6497 | REV. 13
SCALE NONE | SHT 17 OF 69
DRAWING

+2_5V_MAIN

EVENLY DISTRIBUTE 0.01UF & 0.1 UF CAPS AMONGST FBVDDQ PINS ON NV ASIC

C86 0.01UF 10% 16V CERM 402 | C84 0.1UF 10% 10V CERM 402 | C73 0.1UF 10% 10V CERM 402 | C81 0.1UF 10% 10V CERM 402 | C90 0.01UF 10% 16V CERM 402 | C72 0.1UF 10% 10V CERM 402 | C78 0.01UF 10% 16V CERM 402 | C98 0.1UF 10% 10V CERM 402 | C133 0.1UF 10% 10V CERM 402 | C167 0.1UF 10% 10V CERM 402 | C159 0.1UF 10% 10V CERM 402 | C95 10UF 20% 10V TANT 1206 | C75 0.1UF 10% 10V CERM 402 | C82 0.1UF 10% 10V CERM 402 | C79 0.1UF 10% 10V CERM 402 | C115 0.01UF 10% 16V CERM 402 | C175 0.1UF 10% 10V CERM 402 | C199 0.1UF 10% 10V CERM 402 | C83 0.01UF 10% 16V CERM 402 | C80 0.1UF 10% 10V CERM 402 | C89 0.01UF 10% 16V CERM 402 | C96 0.1UF 10% 10V CERM 402 | C145 0.1UF 10% 10V CERM 402 | C124 10UF 20% 6.3V CERM 805

+2_5V_MAIN

U39 NV18B BGA (3 OF 5)

FBVDDQ

NC_VTT

GND

FBCAL_PD_VDDQ

FBCAL_PU_GND

FBCAL_TERM_GND

FBCAL_CLK_GND

FB_DLLVDD

FBVREF

GPU_FB_VREF

ROMA14 ROMA15 ROMCS*

FBRAS* FBCAS* FBWE* FBACS0* FBACS1*

FBA0 FBA1 FBA2 FBA3 FBA4 FBA5 FBA6 FBA7 FBA8 FBA9 FBA10 FBA11 FBA12 FBABA0 FBABA1

FBCLK0 FBCLK0* FBCLK1 FBCLK1*

FBDQS0 FBDQS1 FBDQS2 FBDQS3 FBDQS4 FBDQS5 FBDQS6 FBDQS7

FBDQM0 FBDQM1 FBDQM2 FBDQM3 FBDQM4 FBDQM5 FBDQM6 FBDQM7

FBACKE

FBD<0> FBD<1> FBD<2> FBD<3> FBD<4> FBD<5> FBD<6> FBD<7> FBD<8> FBD<9> FBD<10> FBD<11> FBD<12> FBD<13> FBD<14> FBD<15> FBD<16> FBD<17> FBD<18> FBD<19> FBD<20> FBD<21> FBD<22> FBD<23> FBD<24> FBD<25> FBD<26> FBD<27> FBD<28> FBD<29> FBD<30> FBD<31> FBD<32> FBD<33> FBD<34> FBD<35> FBD<36> FBD<37> FBD<38> FBD<39> FBD<40> FBD<41> FBD<42> FBD<43> FBD<44> FBD<45> FBD<46> FBD<47> FBD<48> FBD<49> FBD<50> FBD<51> FBD<52> FBD<53> FBD<54> FBD<55> FBD<56> FBD<57> FBD<58> FBD<59> FBD<60> FBD<61> FBD<62> FBD<63>

NC_VTT<0> NC_VTT<1> NC_VTT<2> NC_VTT<3> NC_VTT<4> NC_VTT<5> NC_VTT<6> NC_VTT<7> NC_VTT<8> NC_VTT<9> NC_VTT<10> NC_VTT<11>

NC_FBDQS0* NC_FBDQS1* NC_FBDQS2* NC_FBDQS3* NC_FBDQS4* NC_FBDQS5* NC_FBDQS6* NC_FBDQS7*

NC_FBDQS_L<0> NC_FBDQS_L<1> NC_FBDQS_L<2> NC_FBDQS_L<3> NC_FBDQS_L<4> NC_FBDQS_L<5> NC_FBDQS_L<6> NC_FBDQS_L<7>

R71 49.9 1% 1/16W MF 402

C62 0.1UF 10% 10V CERM 402

U39 NV18B BGA (4 OF 5)

THERMAL GND

FBCD0 FBCD1 FBCD2 FBCD3 FBCD4 FBCD5 FBCD6 FBCD7 FBCD8 FBCD9 FBCD10 FBCD11 FBCD12 FBCD13 FBCD14 FBCD15 FBCD16 FBCD17 FBCD18 FBCD19 FBCD20 FBCD21 FBCD22 FBCD23 FBCD24 FBCD25 FBCD26 FBCD27 FBCD28 FBCD29 FBCD30 FBCD31 FBCD32 FBCD33 FBCD34 FBCD35 FBCD36 FBCD37 FBCD38 FBCD39 FBCD40 FBCD41 FBCD42 FBCD43 FBCD44 FBCD45 FBCD46 FBCD47 FBCD48 FBCD49 FBCD50 FBCD51 FBCD52 FBCD53 FBCD54 FBCD55 FBCD56 FBCD57 FBCD58 FBCD59 FBCD60 FBCD61 FBCD62 FBCD63

FBCD<64> FBCD<65> FBCD<66> FBCD<67> FBCD<68> FBCD<69> FBCD<70> FBCD<71> FBCD<72> FBCD<73> FBCD<74> FBCD<75> FBCD<76> FBCD<77> FBCD<78> FBCD<79> FBCD<80> FBCD<81> FBCD<82> FBCD<83> FBCD<84> FBCD<85> FBCD<86> FBCD<87> FBCD<88> FBCD<89> FBCD<90> FBCD<91> FBCD<92> FBCD<93> FBCD<94> FBCD<95> FBCD<96> FBCD<97> FBCD<98> FBCD<99> FBCD<100> FBCD<101> FBCD<102> FBCD<103> FBCD<104> FBCD<105> FBCD<106> FBCD<107> FBCD<108> FBCD<109> FBCD<110> FBCD<111> FBCD<112> FBCD<113> FBCD<114> FBCD<115> FBCD<116> FBCD<117> FBCD<118> FBCD<119> FBCD<120> FBCD<121> FBCD<122> FBCD<123> FBCD<124> FBCD<125> FBCD<126> FBCD<127>

FBCDQM0 FBCDQM1 FBCDQM2 FBCDQM3 FBCDQM4 FBCDQM5 FBCDQM6 FBCDQM7

FBCDQS0 FBCDQS1 FBCDQS2 FBCDQS3 FBCDQS4 FBCDQS5 FBCDQS6 FBCDQS7

FBDQS<8> FBDQS<9> FBDQS<10> FBDQS<11> FBDQS<12> FBDQS<13> FBDQS<14> FBDQS<15>

FBDQM<8> FBDQM<9> FBDQM<10> FBDQM<11> FBDQM<12> FBDQM<13> FBDQM<14> FBDQM<15>

FBCA0 FBCA1 FBCA2 FBCA3 FBCA4 FBCA5 FBCA6 FBCA7 FBCA8 FBCA9 FBCA10 FBCA11 FBCA12 FBCBA0 FBCBA1

FBCBRAS_L FBCBCAS_L FBCBWE_L FBCBCS0_L FBCBCS1_L FBCBCKE

NC_FBCDQS0* NC_FBCDQS1* NC_FBCDQS2* NC_FBCDQS3* NC_FBCDQS4* NC_FBCDQS5* NC_FBCDQS6* NC_FBCDQS7*

NC_FBDQS_L<8> NC_FBDQS_L<9> NC_FBDQS_L<10> NC_FBDQS_L<11> NC_FBDQS_L<12> NC_FBDQS_L<13> NC_FBDQS_L<14> NC_FBDQS_L<15>

C61 4.7UF 20% 6.3V TANT 805 | C70 0.1UF 10% 10V CERM 402 | C69 0.001UF 10% 16V CERM 402

R52 10 1% 1/16W MF 402

+3V_MAIN

DQM R'S CLOSE TO GPU

OTHER R'S BETWEEN GPU & MEMORY

FBDQM<0> R117 0 1/16W 5% MF 402 RFBDQM<0>
FBDQM<1> R111 0 1/16W 5% MF 402 RFBDQM<1>
FBDQM<2> R90 0 1/16W 5% MF 402 RFBDQM<2>
FBDQM<3> R84 0 1/16W 5% MF 402 RFBDQM<3>
FBDQM<4> R164 0 1/16W 5% MF 402 RFBDQM<4>
FBDQM<5> R155 0 1/16W 5% MF 402 RFBDQM<5>
FBDQM<6> R154 0 1/16W 5% MF 402 RFBDQM<6>
FBDQM<7> R143 0 1/16W 5% MF 402 RFBDQM<7>

FBACAS_L RP22 22 1/16W 5% SM1 ZT29 RFBACAS_L
FBARAS_L RP22 22 1/16W 5% SM1 ZT20 RFBARAS_L
FBACS0_L RP22 22 1/16W 5% SM1 ZT30 RFBACS0_L
FBAWE_L RP22 22 1/16W 5% SM1 ZT31 RFBAWE_L

FBA<0> RP94 22 1/16W 5% SM1 ZT22 RFBA<0>
FBA<1> RP94 22 1/16W 5% SM1 ZT23 RFBA<1>
FBA<2> RP94 22 1/16W 5% SM1 ZT34 RFBA<2>
FBA<3> RP95 22 1/16W 5% SM1 ZT24 RFBA<3>
FBA<4> RP95 22 1/16W 5% SM1 ZT25 RFBA<4>
FBA<5> RP95 22 1/16W 5% SM1 ZT37 RFBA<5>
FBA<6> RP95 22 1/16W 5% SM1 ZT26 RFBA<6>
FBA<7> RP23 22 1/16W 5% SM1 ZT27 RFBA<7>
FBA<8> RP23 22 1/16W 5% SM1 ZT38 RFBA<8>
FBA<9> RP23 22 1/16W 5% SM1 ZT36 RFBA<9>
FBA<10> RP23 22 1/16W 5% SM1 ZT33 RFBA<10>
FBA<11> RP93 22 1/16W 5% SM1 ZT35 RFBA<11>
FBA<12> RP93 22 1/16W 5% SM1 NC_RFBA<12>

FBABA<0> RP93 22 1/16W 5% SM1 ZT21 RFBABA<0>
FBABA<1> RP93 22 1/16W 5% SM1 ZT32 RFBABA<1>

WEAK PULL-DOWN RECOMMENDED BY NVIDIA

FBACKE R130 22 1/16W 5% SM1 ZT28 RFBACKE
R131 10K 5% 1/16W MF 402

FBDQM<8> R64 0 1/16W 5% MF 402 RFBDQM<8>
FBDQM<9> R66 0 1/16W 5% MF 402 RFBDQM<9>
FBDQM<10> R70 0 1/16W 5% MF 402 RFBDQM<10>
FBDQM<11> R67 0 1/16W 5% MF 402 RFBDQM<11>
FBDQM<12> R54 0 1/16W 5% MF 402 RFBDQM<12>
FBDQM<13> R56 0 1/16W 5% MF 402 RFBDQM<13>
FBDQM<14> R58 0 1/16W 5% MF 402 RFBDQM<14>
FBDQM<15> R59 0 1/16W 5% MF 402 RFBDQM<15>

FBCBCS0_L RP9 22 1/16W 5% SM1 ZT2 RFBBCS0_L
FBBWE_L RP9 22 1/16W 5% SM1 ZT5 RFBBWE_L
FBCBCAS_L RP9 22 1/16W 5% SM1 ZT1 RFBBCAS_L
FBBRAS_L RP9 22 1/16W 5% SM1 ZT3 RFBBRAS_L

FBBA<0> RP85 22 1/16W 5% SM1 ZT6 RFBBA<0>
FBBA<1> RP85 22 1/16W 5% SM1 ZT8 RFBBA<1>
FBBA<2> RP85 22 1/16W 5% SM1 ZT11 RFBBA<2>
FBBA<3> RP84 22 1/16W 5% SM1 ZT10 RFBBA<3>
FBBA<4> RP84 22 1/16W 5% SM1 ZT12 RFBBA<4>
FBBA<5> RP84 22 1/16W 5% SM1 ZT17 RFBBA<5>
FBBA<6> RP84 22 1/16W 5% SM1 ZT14 RFBBA<6>
FBBA<7> RP83 22 1/16W 5% SM1 ZT16 RFBBA<7>
FBBA<8> RP83 22 1/16W 5% SM1 ZT18 RFBBA<8>
FBBA<9> RP83 22 1/16W 5% SM1 ZT15 RFBBA<9>
FBBA<10> RP83 22 1/16W 5% SM1 ZT9 RFBBA<10>
FBBA<11> RP8 22 1/16W 5% SM1 ZT13 RFBBA<11>
FBBA<12> RP8 22 1/16W 5% SM1 NC_RFBBA<12>

FBBBA<0> RP8 22 1/16W 5% SM1 ZT4 RFBBBA<0>
FBBBA<1> RP8 22 1/16W 5% SM1 ZT7 RFBBBA<1>

WEAK PULL-DOWN RECOMMENDED BY NVIDIA

FBBCKE R62 22 1/16W 5% SM1 ZT19 RFBBCKE
R61 10K 5% 1/16W MF 402

+2_5V_MAIN

NVIDIA VREF

R36 0 1% 1/16W MF 402

MEMREFN1 MEMREFN2

R49 0 1% 1/16W MF 402 NOSTUFF

R50 0 1% 1/16W MF 402

R41 1K 1% 1/16W MF 402

R463 1K 1% 1/16W MF 402

C54 0.1UF 10% 10V CERM 402

C509 0.1UF 10% 10V CERM 402

C510 100PF 5% 25V CERM 402

U7 TLV431A SOT

FBCAL_CLK_GND FBCAL_TERM_GND FBCAL_PU_GND

R95 49.9 1% 1/16W MF 402

R83 0 1% 1/16W MF 402

R88 549 1% 1/16W MF 402

NVIDIA FRAME BUFFER

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
E	051-6497	13
SCALE	SHT	OF
NONE	18	69

DRAWING

PLACE R'S BETWEEN GPU & MEMORY

55D3> 18G8<>	FBD<0>		15	1	8	RP20	RFBD<0>	20C5<> 55D3>
55D3> 18G8<>	FBD<1>	NO_TEST	15	2	7	RP20	RFBD<1>	20C5<> 55D3>
55D3> 18G8<>	FBD<2>	NO_TEST	15	3	6	RP20	RFBD<2>	20C5<> 55D3>
55D3> 18G8<>	FBD<3>	NO_TEST	15	4	5	RP20	RFBD<3>	20C5<> 55D3>
55D3> 18G8<>	FBD<4>	NO_TEST	15	1	8	RP19	RFBD<4>	20C5<> 55D3>
55D3> 18G8<>	FBD<5>		15	2	7	RP19	RFBD<5>	20C5<> 55D3>
55D3> 18G8<>	FBD<6>	NO_TEST	15	3	6	RP19	RFBD<6>	20C5<> 55D3>
55D3> 18G8<>	FBD<7>	NO_TEST	15	4	5	RP19	RFBD<7>	20C5<> 55D3>
55D3> 18G8<>	FBD<8>	NO_TEST	15	1	8	RP21	RFBD<8>	20C5<> 55D3>
55D3> 18G8<>	FBD<9>		15	2	7	RP21	RFBD<9>	20C5<> 55D3>
55D3> 18G8<>	FBD<10>	NO_TEST	15	3	6	RP21	RFBD<10>	20C5<> 55D3>
55D3> 18G8<>	FBD<11>	NO_TEST	15	4	5	RP21	RFBD<11>	20C5<> 55D3>
55D3> 18G8<>	FBD<12>	NO_TEST	15	1	8	RP18	RFBD<12>	20C5<> 55D3>
55D3> 18G8<>	FBD<13>		15	2	7	RP18	RFBD<13>	20C5<> 55D3>
55D3> 18G8<>	FBD<14>	NO_TEST	15	3	6	RP18	RFBD<14>	20C5<> 55D3>
55D3> 18G8<>	FBD<15>	NO_TEST	15	4	5	RP18	RFBD<15>	20C5<> 55D3>
55D3> 18G8<>	FBD<16>		15	1	8	RP91	RFBD<16>	20C5<> 55D3>
55D3> 18G8<>	FBD<17>	NO_TEST	15	2	7	RP91	RFBD<17>	20C5<> 55D3>
55D3> 18G8<>	FBD<18>	NO_TEST	15	3	6	RP91	RFBD<18>	20C5<> 55D3>
55D3> 18G8<>	FBD<19>	NO_TEST	15	4	5	RP91	RFBD<19>	20C5<> 55D3>
55D3> 18G8<>	FBD<20>		15	1	8	RP90	RFBD<20>	20C5<> 55D3>
55D3> 18G8<>	FBD<21>	NO_TEST	15	2	7	RP90	RFBD<21>	20C5<> 55D3>
55D3> 18G8<>	FBD<22>	NO_TEST	15	3	6	RP90	RFBD<22>	20C5<> 55D3>
55D3> 18G8<>	FBD<23>	NO_TEST	15	4	5	RP90	RFBD<23>	20C5<> 55D3>
55D3> 18G8<>	FBD<24>		15	1	8	RP92	RFBD<24>	20C5<> 55D3>
55D3> 18F8<>	FBD<25>	NO_TEST	15	2	7	RP92	RFBD<25>	20C5<> 55D3>
55D3> 18F8<>	FBD<26>	NO_TEST	15	3	6	RP92	RFBD<26>	20B5<> 55D3>
55D3> 18F8<>	FBD<27>	NO_TEST	15	4	5	RP92	RFBD<27>	20B5<> 55D3>
55D3> 18F8<>	FBD<28>		15	1	8	RP17	RFBD<28>	20B5<> 55D3>
55D3> 18F8<>	FBD<29>	NO_TEST	15	2	7	RP17	RFBD<29>	20B5<> 55D3>
55D3> 18F8<>	FBD<30>		15	3	6	RP17	RFBD<30>	20B5<> 55D3>
55D3> 18F8<>	FBD<31>	NO_TEST	15	4	5	RP17	RFBD<31>	20B5<> 55D3>

55D3> 18F8<>	FBD<32>		15	1	8	RP29	RFBD<32>	20C1<> 55D3>
55D3> 18F8<>	FBD<33>	NO_TEST	15	2	7	RP29	RFBD<33>	20C1<> 55D3>
55D3> 18F8<>	FBD<34>	NO_TEST	15	3	6	RP29	RFBD<34>	20C1<> 55D3>
55D3> 18F8<>	FBD<35>	NO_TEST	15	4	5	RP29	RFBD<35>	20C1<> 55D3>
55D3> 18F8<>	FBD<36>		15	1	8	RP27	RFBD<36>	20C1<> 55D3>
55D3> 18F8<>	FBD<37>	NO_TEST	15	3	6	RP27	RFBD<37>	20C1<> 55D3>
55D3> 18F8<>	FBD<38>		15	2	7	RP27	RFBD<38>	20C1<> 55D3>
55D3> 18F8<>	FBD<39>	NO_TEST	15	4	5	RP27	RFBD<39>	20C1<> 55D3>
55D3> 18F8<>	FBD<40>	NO_TEST	15	1	8	RP28	RFBD<40>	20C1<> 55D3>
55D3> 18F8<>	FBD<41>		15	2	7	RP28	RFBD<41>	20C1<> 55D3>
55D3> 18F8<>	FBD<42>	NO_TEST	15	3	6	RP28	RFBD<42>	20C1<> 55D3>
55D3> 18F8<>	FBD<43>	NO_TEST	15	4	5	RP28	RFBD<43>	20C1<> 55D3>
55D3> 18F8<>	FBD<44>		15	1	8	RP97	RFBD<44>	20C1<> 55D3>
55D3> 18E8<>	FBD<45>	NO_TEST	15	2	7	RP97	RFBD<45>	20C1<> 55D3>
55D3> 18E8<>	FBD<46>	NO_TEST	15	3	6	RP97	RFBD<46>	20C1<> 55D3>
55D3> 18E8<>	FBD<47>	NO_TEST	15	4	5	RP97	RFBD<47>	20C1<> 55D3>
55D3> 18E8<>	FBD<48>		15	1	8	RP25	RFBD<48>	20C1<> 55D3>
55D3> 18E8<>	FBD<49>	NO_TEST	15	2	7	RP25	RFBD<49>	20C1<> 55D3>
55D3> 18E8<>	FBD<50>	NO_TEST	15	3	6	RP25	RFBD<50>	NO_TEST 20C1<> 55D3>
55D3> 18E8<>	FBD<51>	NO_TEST	15	4	5	RP25	RFBD<51>	20C1<> 55D3>
55D3> 18E8<>	FBD<52>	NO_TEST	15	1	8	RP96	RFBD<52>	20C1<> 55D3>
55D3> 18E8<>	FBD<53>		15	2	7	RP96	RFBD<53>	20C1<> 55D3>
55D3> 18E8<>	FBD<54>	NO_TEST	15	3	6	RP96	RFBD<54>	20C1<> 55D3>
55D3> 18E8<>	FBD<55>	NO_TEST	15	4	5	RP96	RFBD<55>	20C1<> 55D3>
55D3> 18E8<>	FBD<56>		15	1	8	RP26	RFBD<56>	20C1<> 55D3>
55D3> 18E8<>	FBD<57>	NO_TEST	15	2	7	RP26	RFBD<57>	20C1<> 55D3>
55D3> 18E8<>	FBD<58>	NO_TEST	15	3	6	RP26	RFBD<58>	20B1<> 55D3>
55D3> 18E8<>	FBD<59>	NO_TEST	15	4	5	RP26	RFBD<59>	20B1<> 55D3>
55D3> 18E8<>	FBD<60>		15	1	8	RP24	RFBD<60>	20B1<> 55D3>
55D3> 18E8<>	FBD<61>	NO_TEST	15	2	7	RP24	RFBD<61>	20B1<> 55D3>
55D3> 18E8<>	FBD<62>	NO_TEST	15	3	6	RP24	RFBD<62>	20B1<> 55D3>
55D3> 18E8<>	FBD<63>	NO_TEST	15	4	5	RP24	RFBD<63>	20B1<> 55D3>

55C3> 18G5<>	FBD<64>		15	1	8	RP10 NV34	RFBD<64>	21C5<> 55C3>
55C3> 18G5<>	FBD<65>	NO_TEST	15	2	7	RP10 NV34	RFBD<65>	21C5<> 55C3>
55C3> 18G5<>	FBD<66>	NO_TEST	15	3	6	RP10 NV34	RFBD<66>	21C5<> 55C3>
55C3> 18G5<>	FBD<67>		15	4	5	RP10 NV34	RFBD<67>	21C5<> 55C3>
55C3> 18G5<>	FBD<68>		15	1	8	RP14 NV34	RFBD<68>	21C5<> 55C3>
55C3> 18G5<>	FBD<69>	NO_TEST	15	2	7	RP14 NV34	RFBD<69>	21C5<> 55C3>
55C3> 18G5<>	FBD<70>	NO_TEST	15	3	6	RP14 NV34	RFBD<70>	21C5<> 55C3>
55C3> 18G5<>	FBD<71>	NO_TEST	15	4	5	RP14 NV34	RFBD<71>	21C5<> 55C3>
55C3> 18G5<>	FBD<72>	NO_TEST	15	4	5	RP82 NV34	RFBD<72>	21C5<> 55C3>
55C3> 18G5<>	FBD<73>	NO_TEST	15	3	6	RP82 NV34	RFBD<73>	21C5<> 55C3>
55C3> 18G5<>	FBD<74>	NO_TEST	15	2	7	RP82 NV34	RFBD<74>	21C5<> 55C3>
55C3> 18G5<>	FBD<75>		15	1	8	RP82 NV34	RFBD<75>	21C5<> 55C3>
55C3> 18G5<>	FBD<76>		15	1	8	RP12 NV34	RFBD<76>	21C5<> 55C3>
55C3> 18G5<>	FBD<77>	NO_TEST	15	2	7	RP12 NV34	RFBD<77>	21C5<> 55C3>
55C3> 18G5<>	FBD<78>	NO_TEST	15	3	6	RP12 NV34	RFBD<78>	21C5<> 55C3>
55C3> 18G5<>	FBD<79>	NO_TEST	15	4	5	RP12 NV34	RFBD<79>	21C5<> 55C3>
55C3> 18G5<>	FBD<80>		15	1	8	RP11 NV34	RFBD<80>	21C5<> 55C3>
55C3> 18G5<>	FBD<81>	NO_TEST	15	2	7	RP11 NV34	RFBD<81>	21C5<> 55C3>
55C3> 18G5<>	FBD<82>	NO_TEST	15	3	6	RP11 NV34	RFBD<82>	21C5<> 55C3>
55C3> 18G5<>	FBD<83>	NO_TEST	15	4	5	RP11 NV34	RFBD<83>	21C5<> 55C3>
55C3> 18G5<>	FBD<84>		15	4	5	RP80 NV34	RFBD<84>	21C5<> 55C3>
55C3> 18G5<>	FBD<85>	NO_TEST	15	3	6	RP80 NV34	RFBD<85>	21C5<> 55C3>
55C3> 18G5<>	FBD<86>	NO_TEST	15	2	7	RP80 NV34	RFBD<86>	21C5<> 55C3>
55C3> 18G5<>	FBD<87>	NO_TEST	15	1	8	RP80 NV34	RFBD<87>	21C5<> 55C3>
55C3> 18G5<>	FBD<88>	NO_TEST	15	4	5	RP81 NV34	RFBD<88>	21C5<> 55C3>
55C3> 18F5<>	FBD<89>		15	3	6	RP81 NV34	RFBD<89>	21C5<> 55C3>
55C3> 18F5<>	FBD<90>	NO_TEST	15	2	7	RP81 NV34	RFBD<90>	21B5<> 55C3>
55C3> 18F5<>	FBD<91>	NO_TEST	15	1	8	RP81 NV34	RFBD<91>	21B5<> 55C3>
55C3> 18F5<>	FBD<92>	NO_TEST	15	1	8	RP13 NV34	RFBD<92>	21B5<> 55C3>
55C3> 18F5<>	FBD<93>	NO_TEST	15	2	7	RP13 NV34	RFBD<93>	21B5<> 55C3>
55C3> 18F5<>	FBD<94>	NO_TEST	15	3	6	RP13 NV34	RFBD<94>	21B5<> 55C3>
55C3> 18F5<>	FBD<95>		15	4	5	RP13 NV34	RFBD<95>	21B5<> 55C3>

55C3> 18F5<>	FBD<96>		15	1	8	RP88 NV34	RFBD<96>	21C1<> 55C3>
55C3> 18F5<>	FBD<97>	NO_TEST	15	2	7	RP88 NV34	RFBD<97>	21C1<> 55C3>
55C3> 18F5<>	FBD<98>	NO_TEST	15	3	6	RP88 NV34	RFBD<98>	21C1<> 55C3>
55C3> 18F5<>	FBD<99>	NO_TEST	15	4	5	RP88 NV34	RFBD<99>	21C1<> 55C3>
55C3> 18F5<>	FBD<100>	NO_TEST	15	1	8	RP89 NV34	RFBD<100>	21C1<> 55C3>
55C3> 18F5<>	FBD<101>		15	2	7	RP89 NV34	RFBD<101>	21C1<> 55C3>
55C3> 18F5<>	FBD<102>	NO_TEST	15	3	6	RP89 NV34	RFBD<102>	21C1<> 55C3>
55C3> 18F5<>	FBD<103>	NO_TEST	15	4	5	RP89 NV34	RFBD<103>	21C1<> 55C3>
55C3> 18F5<>	FBD<104>		15	1	8	RP4 NV34	RFBD<104>	21C1<> 55C3>
55C3> 18F5<>	FBD<105>	NO_TEST	15	2	7	RP4 NV34	RFBD<105>	21C1<> 55C3>
55C3> 18F5<>	FBD<106>	NO_TEST	15	3	6	RP4 NV34	RFBD<106>	21C1<> 55C3>
55C3> 18F5<>	FBD<107>	NO_TEST	15	4	5	RP4 NV34	RFBD<107>	21C1<> 55C3>
55C3> 18F5<>	FBD<108>		15	1	8	RP86 NV34	RFBD<108>	21C1<> 55C3>
55C3> 18E5<>	FBD<109>	NO_TEST	15	2	7	RP86 NV34	RFBD<109>	21C1<> 55C3>
55C3> 18E5<>	FBD<110>	NO_TEST	15	3	6	RP86 NV34	RFBD<110>	21C1<> 55C3>
55C3> 18E5<>	FBD<111>	NO_TEST	15	4	5	RP86 NV34	RFBD<111>	21C1<> 55C3>
55C3> 18E5<>	FBD<112>		15	1	8	RP5 NV34	RFBD<112>	21C1<> 55C3>
55C3> 18E5<>	FBD<113>	NO_TEST	15	2	7	RP5 NV34	RFBD<113>	21C1<> 55C3>
55C3> 18E5<>	FBD<114>	NO_TEST	15	3	6	RP5 NV34	RFBD<114>	21C1<> 55C3>
55C3> 18E5<>	FBD<115>	NO_TEST	15	4	5	RP5 NV34	RFBD<115>	21C1<> 55C3>
55C3> 18E5<>	FBD<116>		15	1	8	RP6 NV34	RFBD<116>	21C1<> 55C3>
55C3> 18E5<>	FBD<117>	NO_TEST	15	2	7	RP6 NV34	RFBD<117>	21C1<> 55C3>
55C3> 18E5<>	FBD<118>	NO_TEST	15	3	6	RP6 NV34	RFBD<118>	21C1<> 55C3>
55C3> 18E5<>	FBD<119>	NO_TEST	15	4	5	RP6 NV34	RFBD<119>	21C1<> 55C3>
55C3> 18E5<>	FBD<120>		15	1	8	RP7 NV34	RFBD<120>	21C1<> 55C3>
55C3> 18E5<>	FBD<121>	NO_TEST	15	2	7	RP7 NV34	RFBD<121>	21C1<> 55C3>
55C3> 18E5<>	FBD<122>	NO_TEST	15	3	6	RP7 NV34	RFBD<122>	21B1<> 55C3>
55C3> 18E5<>	FBD<123>	NO_TEST	15	4	5	RP7 NV34	RFBD<123>	21B1<> 55C3>
55C3> 18E5<>	FBD<124>		15	1	8	RP87 NV34	RFBD<124>	21B1<> 55C3>
55C3> 18E5<>	FBD<125>	NO_TEST	15	2	7	RP87 NV34	RFBD<125>	21B1<> 55C3>
55C3> 18E5<>	FBD<126>	NO_TEST	15	3	6	RP87 NV34	RFBD<126>	21B1<> 55C3>
55C3> 18E5<>	FBD<127>		15	4	5	RP87 NV34	RFBD<127>	21B1<> 55C3>

PLACE R'S CLOSE TO GPU

55C3> 18D7> FBACLK1 — R123 15 1% 1/16W MF 402 — RFBACLK1 20C2< 55C3>

R158 100 1% 1/16W MF 402 — PLACE 100OHM TERM AT RAM

55C3> 18D7> FBACLK1_L — R132 15 1% 1/16W MF 402 — RFBACLK1_L 20C2< 55C3>

55C3> 18D7> FBACLK0 — R148 15 1% 1/16W MF 402 — RFBACLK0 20C6< 55C3>

R500 100 1% 1/16W MF 402 — PLACE 100OHM TERM AT RAM

55C3> 18D7> FBACLK0_L — R156 15 1% 1/16W MF 402 — RFBACLK0_L 20C6< 55C3>

55B3> 18C5<> FBBCLK1 — NV34 R106 15 1% 1/16W MF 402 — RFBBCLK1 21C2< 55B3>

NV34 R20 100 1% 1/16W MF 402 — PLACE 100OHM TERM AT RAM

55B3> 18C5<> FBBCLK1_L — NV34 R105 15 1% 1/16W MF 402 — RFBBCLK1_L 21C2< 55B3>

55B3> 18C5<> FBBCLK0 — NV34 R103 15 1% 1/16W MF 402 — RFBBCLK0 21C6< 55B3>

NV34 R403 100 1% 1/16W MF 402 — PLACE 100OHM TERM AT RAM

55B3> 18C5<> FBBCLK0_L — NV34 R104 15 1% 1/16W MF 402 — RFBBCLK0_L 21C6< 55B3>

PLACE THESE R CLOSE TO GPU / PLACE THESE R CLOSE TO SGRAM

55C3> 18C7<>	FBDQS<0>	R122 0 5% 1/16W MF 402	55C3>	NO_TEST	FBDQSTERM<0>	R483 15 1% 1/16W MF 402	RFBDQS<0>	20C6<> 55C3>
55C3> 18C7<>	FBDQS<1>	R101 0 5% 1/16W MF 402	55C3>	NO_TEST	FBDQSTERM<1>	R509 15 1% 1/16W MF 402	RFBDQS<1>	20C6<> 55C3>
55C3> 18C7<>	FBDQS<2>	R97 0 5% 1/16W MF 402	55C3>	NO_TEST	FBDQSTERM<2>	R479 15 1% 1/16W MF 402	RFBDQS<2>	20C6<> 55C3>
55C3> 18C7<>	FBDQS<3>	R81 0 5% 1/16W MF 402	55C3>	NO_TEST	FBDQSTERM<3>	R506 15 1% 1/16W MF 402	RFBDQS<3>	20C6<> 55C3>
55C3> 18C7<>	FBDQS<4>	R167 0 5% 1/16W MF 402	55C3>	NO_TEST	FBDQSTERM<4>	R187 15 1% 1/16W MF 402	RFBDQS<4>	20C2<> 55C3>
55C3> 18C7<>	FBDQS<5>	R159 0 5% 1/16W MF 402	55C3>	NO_TEST	FBDQSTERM<5>	R146 15 1% 1/16W MF 402	RFBDQS<5>	20C2<> 55C3>
55C3> 18C7<>	FBDQS<6>	R147 0 5% 1/16W MF 402	55C3>	NO_TEST	FBDQSTERM<6>	R186 15 1% 1/16W MF 402	RFBDQS<6>	20C2<> 55C3>
55C3> 18C7<>	FBDQS<7>	R140 0 5% 1/16W MF 402	55C3>	NO_TEST	FBDQSTERM<7>	R153 15 1% 1/16W MF 402	RFBDQS<7>	20C2<> 55C3>

PLACE THESE R CLOSE TO GPU / PLACE THESE R CLOSE TO SGRAM

55B3> 18D4<>	FBDQS<8>	R63 0 NV34 5% 1/16W MF 402	55B3>	NO_TEST	FBDQSTERM<8>	R428 15 NV34 1% 1/16W MF 402	RFBDQS<8>	21C6<> 55B3>
55B3> 18D4<>	FBDQS<9>	NV34 R65 0 5% 1/16W MF 402	55B3>	NO_TEST	FBDQSTERM<9>	NV34 R415 15 1% 1/16W MF 402	RFBDQS<9>	21C6<> 55B3>
55B3> 18D4<>	FBDQS<10>	R69 0 NV34 5% 1/16W MF 402	55B3>	NO_TEST	FBDQSTERM<10>	R416 15 NV34 1% 1/16W MF 402	RFBDQS<10>	21C6<> 55B3>
55B3> 18D4<>	FBDQS<11>	NV34 R68 0 5% 1/16W MF 402	55B3>	NO_TEST	FBDQSTERM<11>	NV34 R429 15 1% 1/16W MF 402	RFBDQS<11>	21C6<> 55B3>
55B3> 18D4<>	FBDQS<12>	R53 0 NV34 5% 1/16W MF 402	55B3>	NO_TEST	FBDQSTERM<12>	R31 15 NV34 1% 1/16W MF 402	RFBDQS<12>	21C2<> 55B3>
55B3> 18D4<>	FBDQS<13>	NV34 R55 0 5% 1/16W MF 402	55B3>	NO_TEST	FBDQSTERM<13>	NV34 R25 15 1% 1/16W MF 402	RFBDQS<13>	21C2<> 55B3>
55B3> 18D4<>	FBDQS<14>	R57 0 NV34 5% 1/16W MF 402	55B3>	NO_TEST	FBDQSTERM<14>	R24 15 NV34 1% 1/16W MF 402	RFBDQS<14>	21C2<> 55B3>
55B3> 18D4<>	FBDQS<15>	NV34 R60 0 5% 1/16W MF 402	55B3>	NO_TEST	FBDQSTERM<15>	NV34 R32 15 1% 1/16W MF 402	RFBDQS<15>	21C2<> 55B3>

FB TERMINATION

NOTICE OF PROPRIETARY PROPERTY

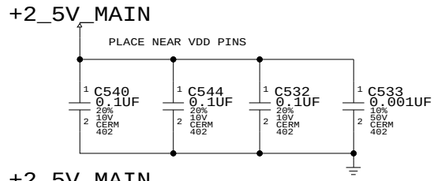
LAST MODIFIED=Wed Sep 17 12:16:10 2003

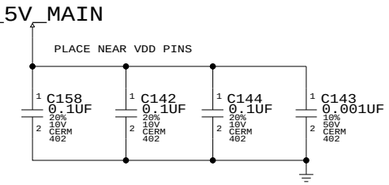
APPLE COMPUTER INC.

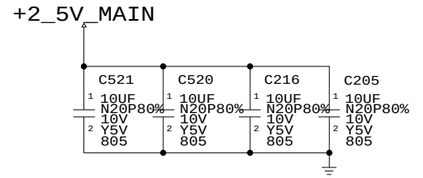
SIZE	DRAWING NUMBER	REV.
D	051-6497	13

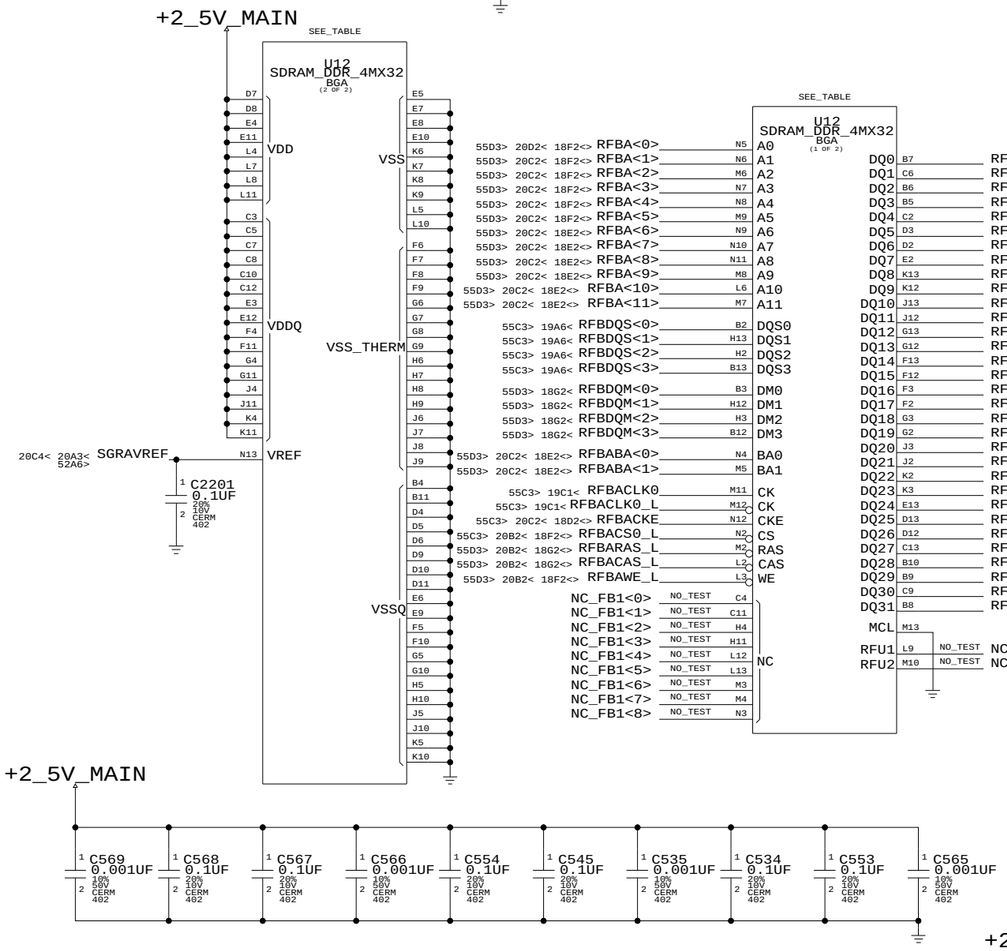
SCALE: NONE — SHT 19 OF 69

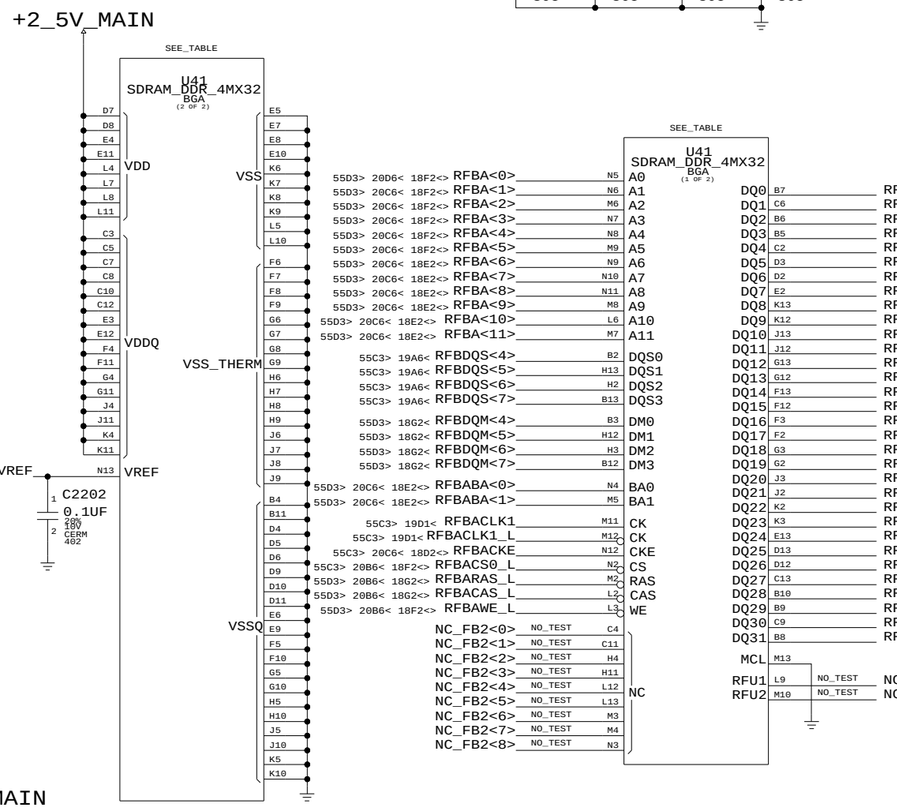
DRAWING

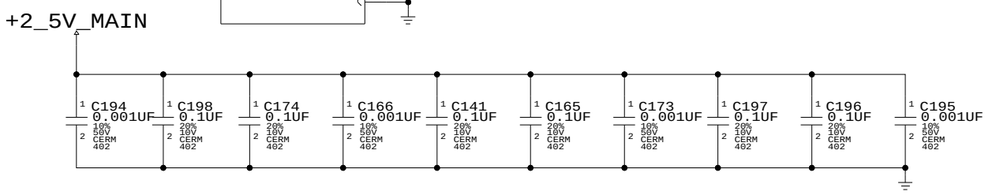










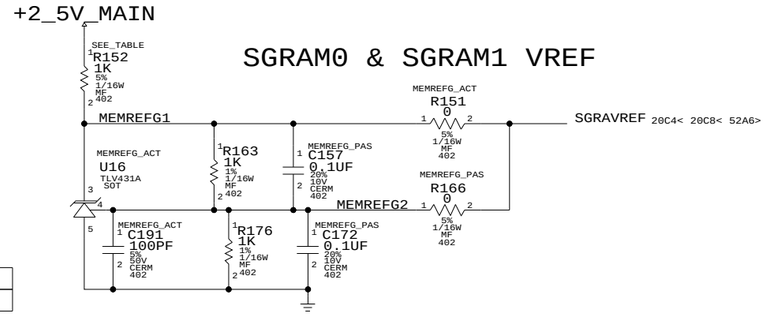


SGRAM0 & SGRAM1 MEMORY SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0249	2	SDRAM,4MX32,DDR,275MHZ	U12,U41	CRITICAL	SAMSUNG_275_32M
333S0250	2	SDRAM,4MX32,DDR,275MHZ	U12,U41	CRITICAL	HYNIX_275_32M
333S0251	2	SDRAM,4MX32,DDR,300MHZ	U12,U41	CRITICAL	SAMSUNG_300_32M
333S0252	2	SDRAM,4MX32,DDR,300MHZ	U12,U41	CRITICAL	HYNIX_300_32M

SGRAM0 & SGRAM1 DDR MEMORY REFERENCE SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S1103	1	RES,1K-OHM,5%,1/16W,0402	R152		MEMREFG_ACT
116S1000	1	RES,0-OHM,5%,1/16W,0402	R152		MEMREFG_PAS



SGRAM0 & SGRAM1 VREF

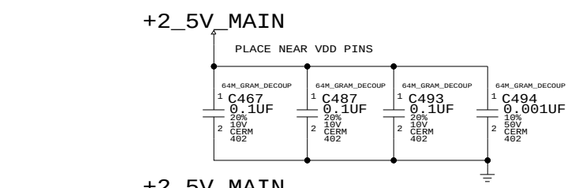
SGRAM0 & SGRAM1

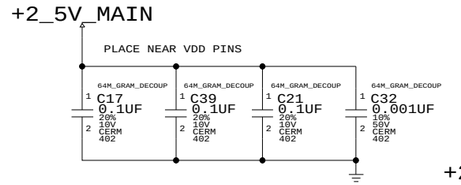
LAST_MODIFIED=Wed Sep 17 12:16:13 2003

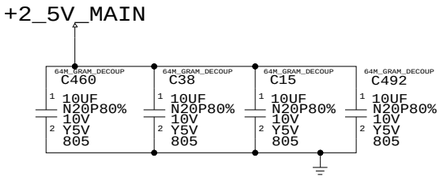
APPLE COMPUTER INC.

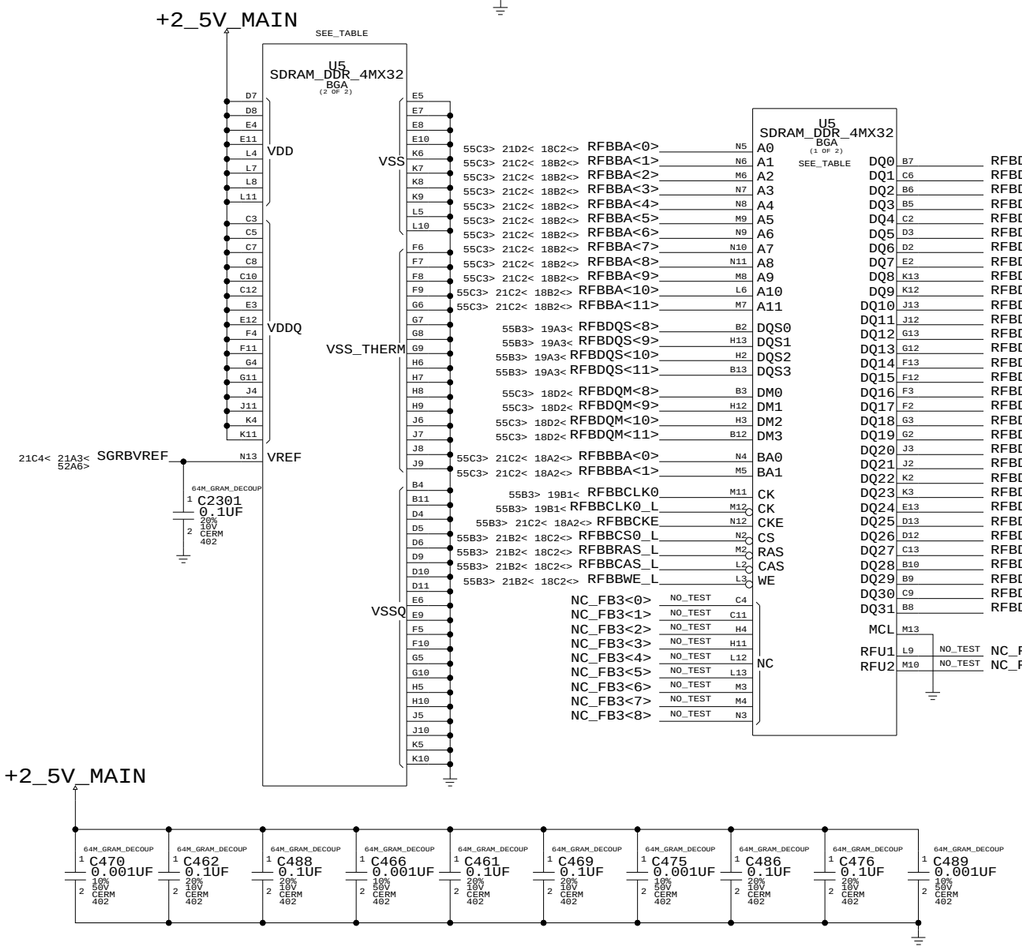
SIZE	DRAWING NUMBER	REV.
D	051-6497	13
SCALE: NONE	SHT 20 OF 69	

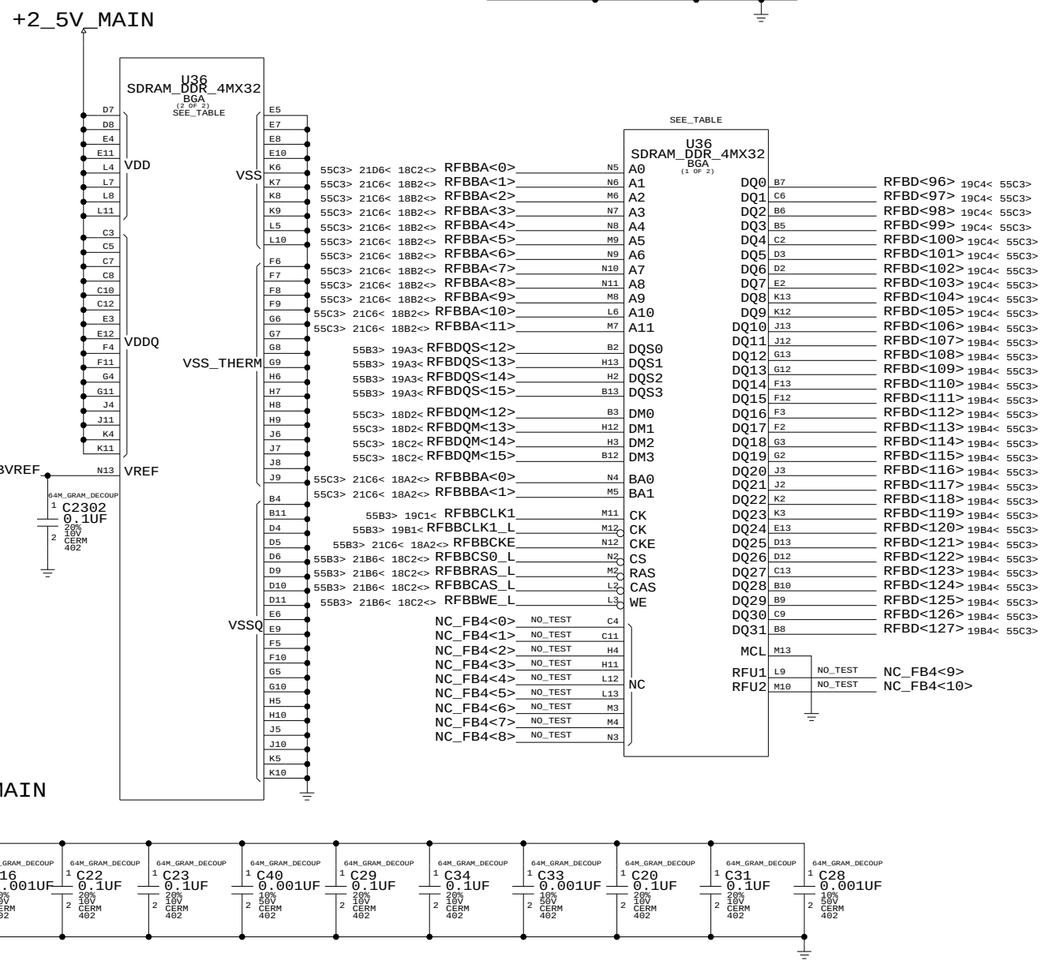
DRAWING









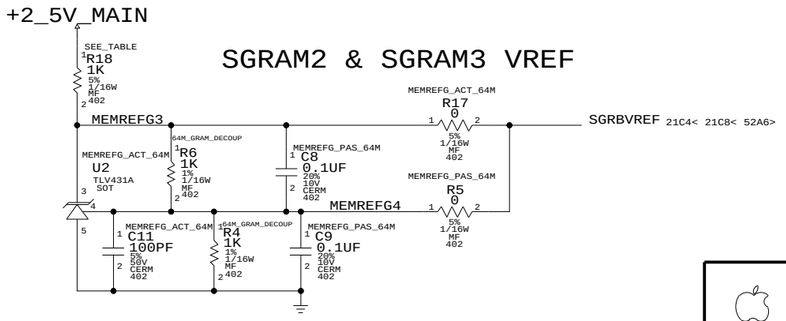


SGRAM0 & SGRAM1 MEMORY SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0249	2	SDRAM,4MX32,DDR,275MHZ	U5,U36	CRITICAL	SAMSUNG_275_64M
333S0250	2	SDRAM,4MX32,DDR,275MHZ	U5,U36	CRITICAL	HYNIX_275_64M
333S0251	2	SDRAM,4MX32,DDR,300MHZ	U5,U36	CRITICAL	SAMSUNG_300_64M
333S0252	2	SDRAM,4MX32,DDR,300MHZ	U5,U36	CRITICAL	HYNIX_300_64M

SGRAM2 & SGRAM3 DDR MEMORY REFERENCE SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S1103	1	RES,1K-OHM,5%,1/16W,0402	R18		MEMREFG_ACT_64M
116S1000	1	RES,0-OHM,5%,1/16W,0402	R18		MEMREFG_PAS_64M



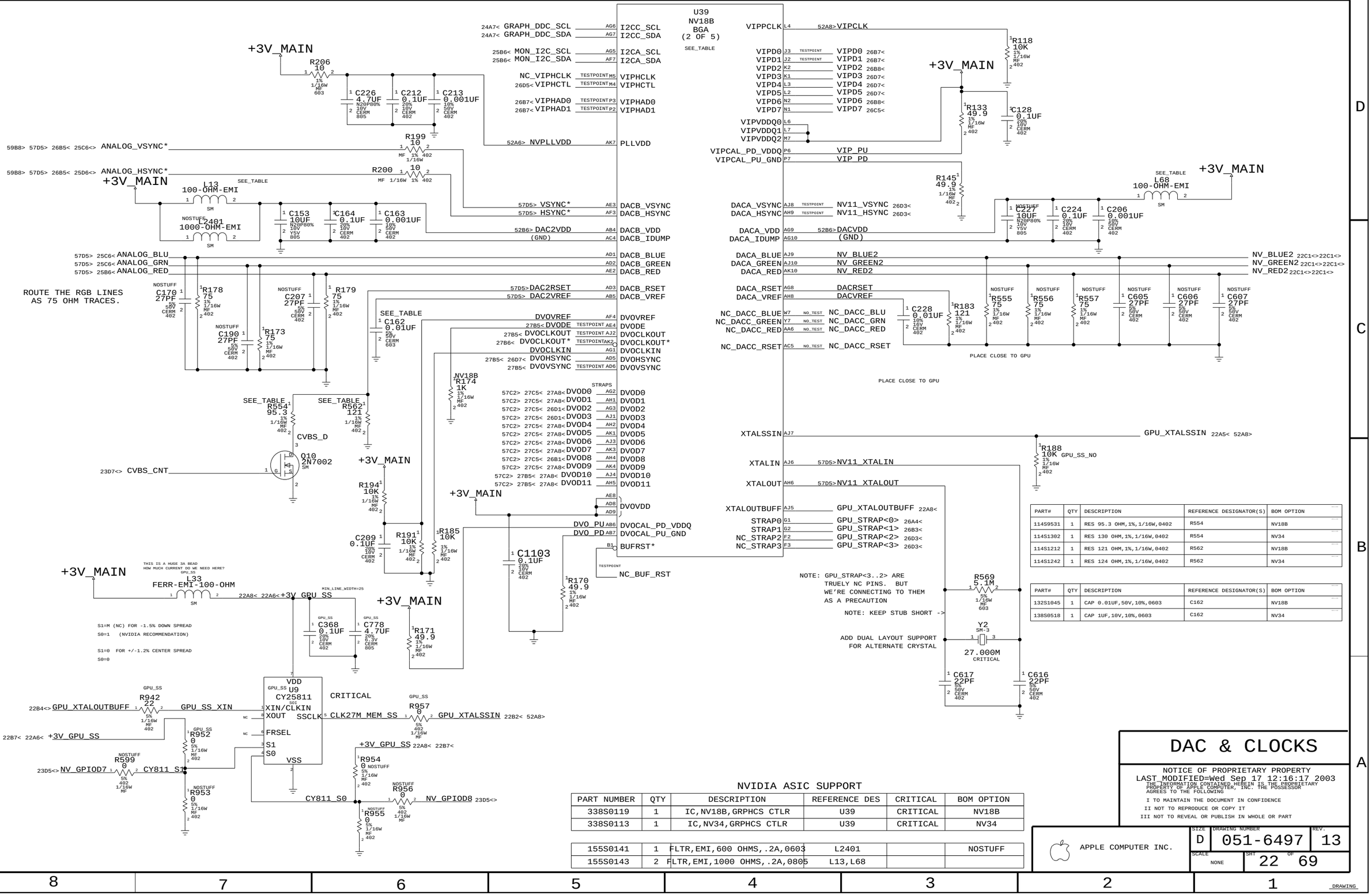
SGRAM2 & SGRAM3

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6497	13
SCALE: NONE	SHT 21 OF 69	

DRAWING

<XR_PAGE_TITLE>



NVIDIA ASIC SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0119	1	IC,NV18B,GRPHCS CTLR	U39	CRITICAL	NV18B
338S0113	1	IC,NV34,GRPHCS CTLR	U39	CRITICAL	NV34

155S0141	1	FLTR,EMI,600 OHMS,.2A,0603	L2401		NOSTUFF
155S0143	2	FLTR,EMI,1000 OHMS,.2A,0805	L13,L68		

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S9531	1	RES 95.3 OHM,1%,1/16W,0402	R554	NV18B
114S1302	1	RES 130 OHM,1%,1/16W,0402	R554	NV34
114S1212	1	RES 121 OHM,1%,1/16W,0402	R562	NV18B
114S1242	1	RES 124 OHM,1%,1/16W,0402	R562	NV34

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S1045	1	CAP 0.01UF,50V,10%,0603	C162	NV18B
138S0518	1	CAP 1UF,10V,10%,0603	C162	NV34

DAC & CLOCKS

LAST_MODIFIED=Wed Sep 17 12:16:17 2003

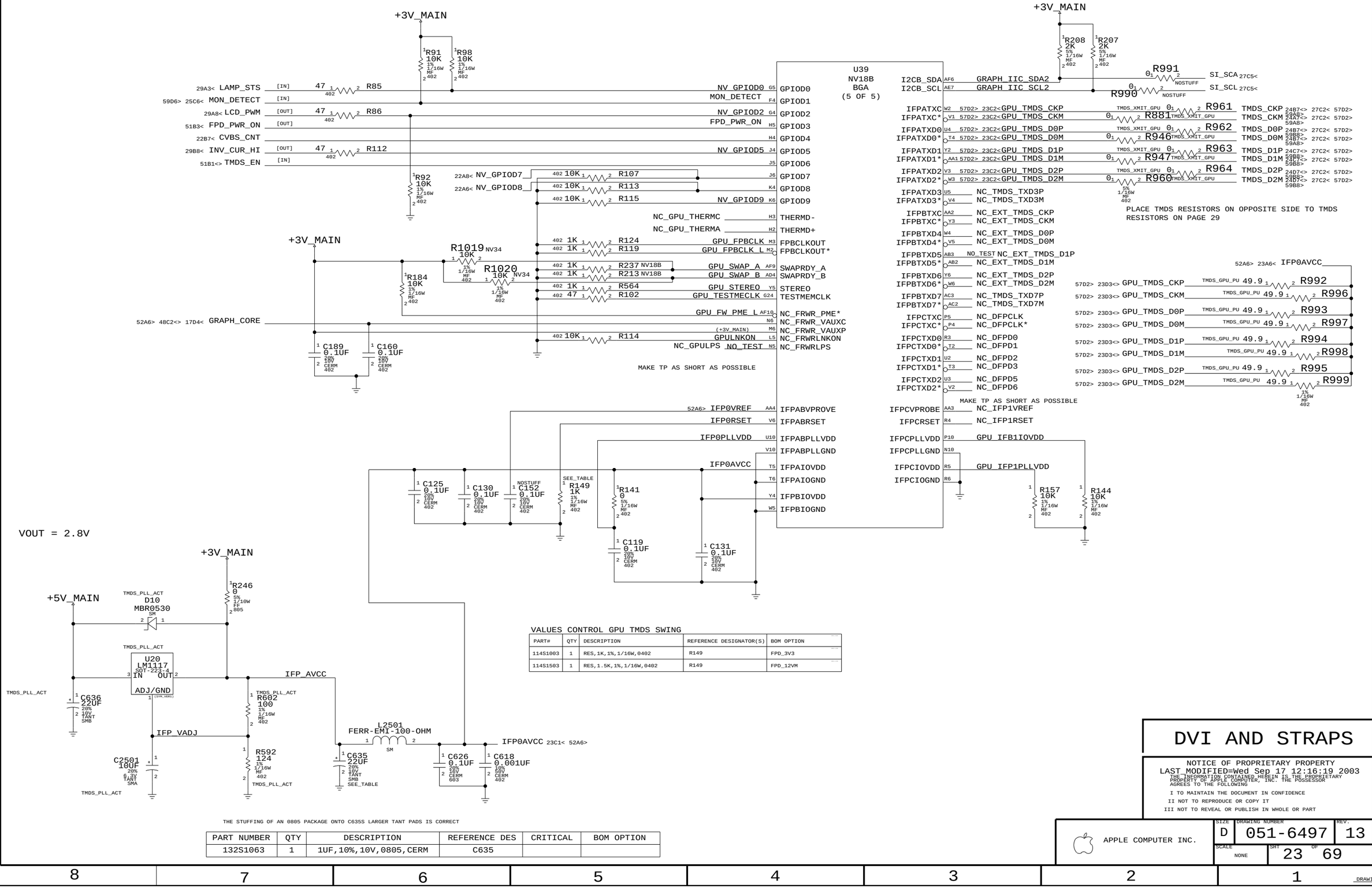
APPLE COMPUTER INC.

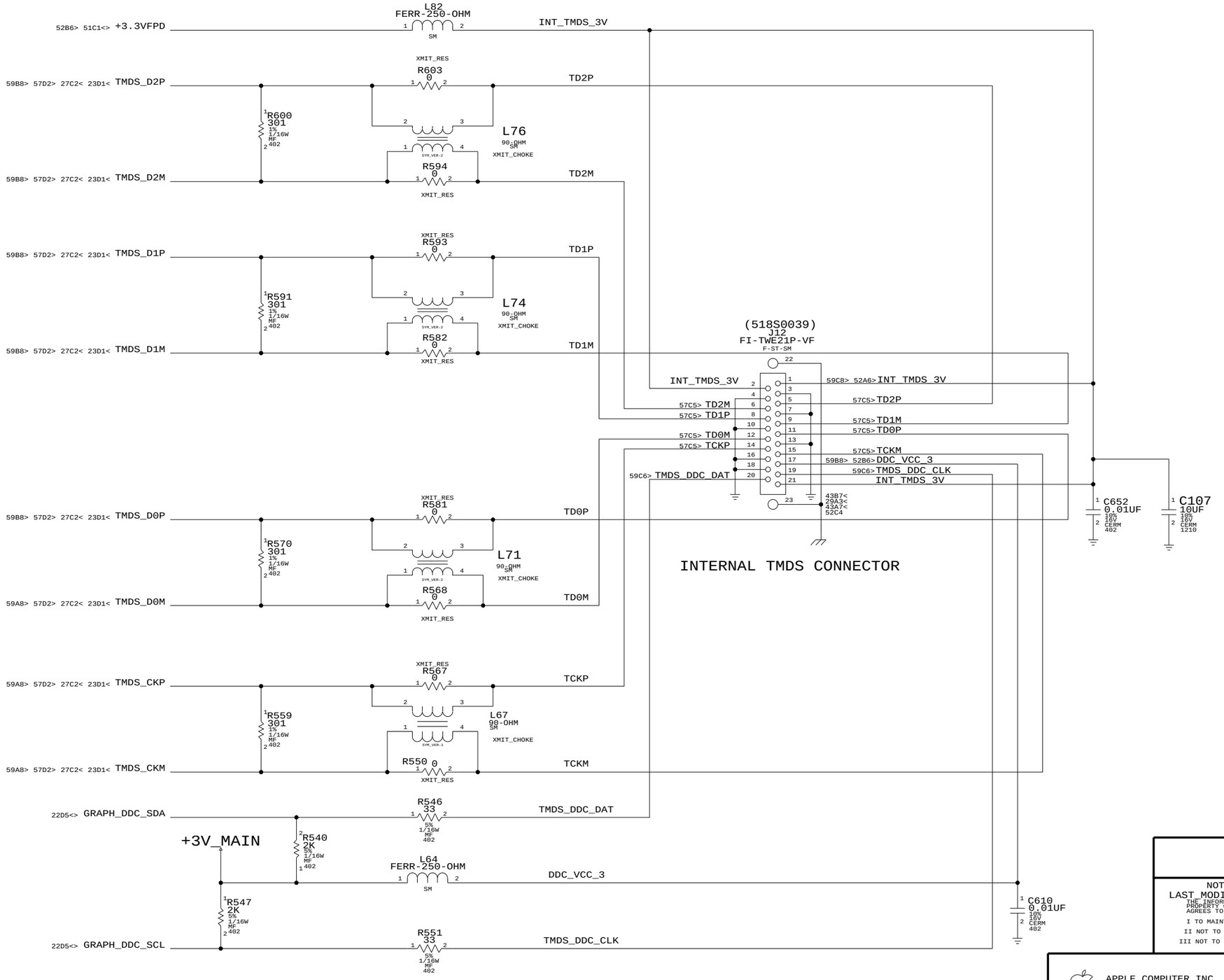
SIZE	DRAWING NUMBER	REV.
D	051-6497	13

SCALE: NONE

SHT 22 OF 69

<XR_PAGE_TITLE>



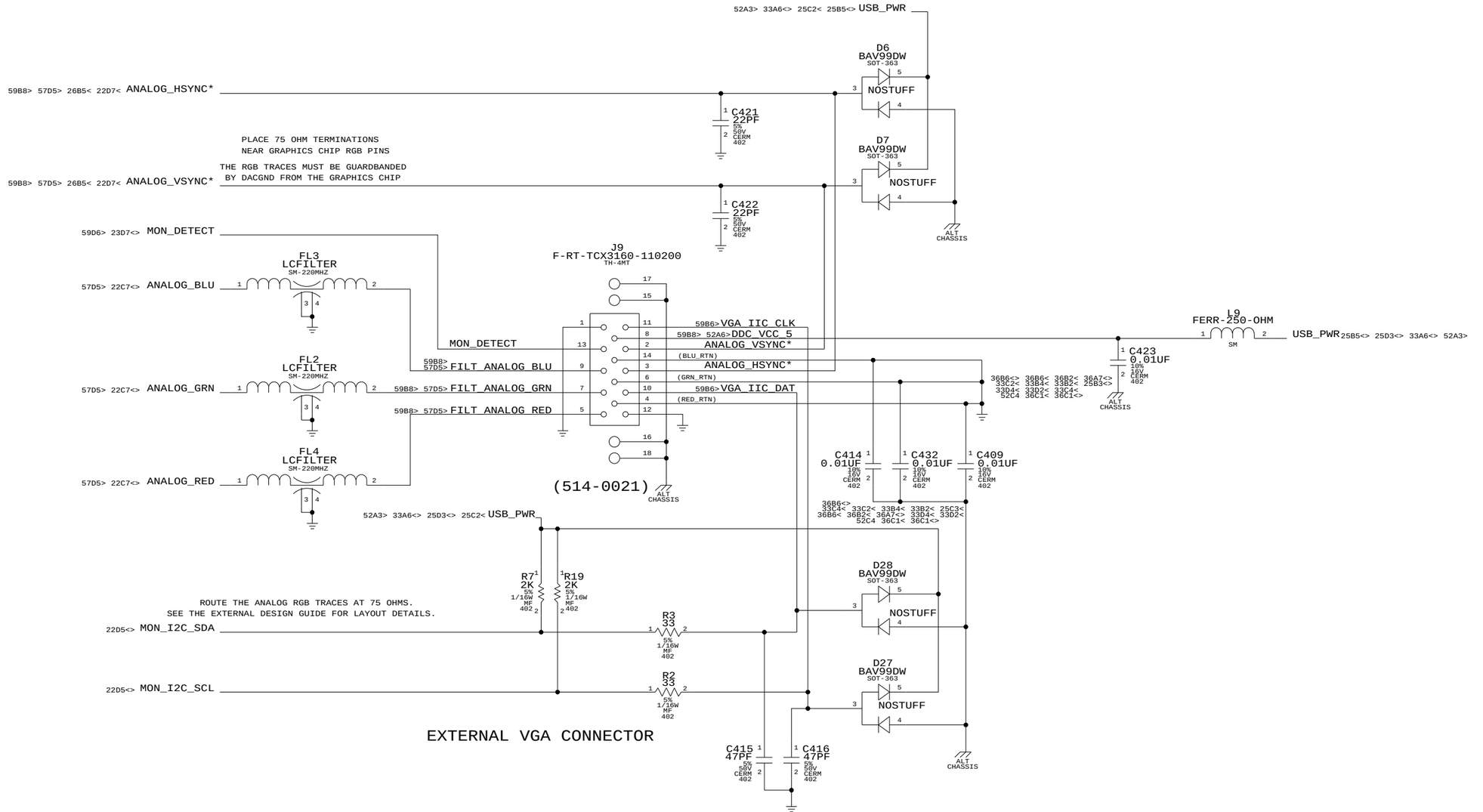


TMDS/LVDS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6497	13
SCALE: NONE	SHT 24 OF 69	

DRAWING

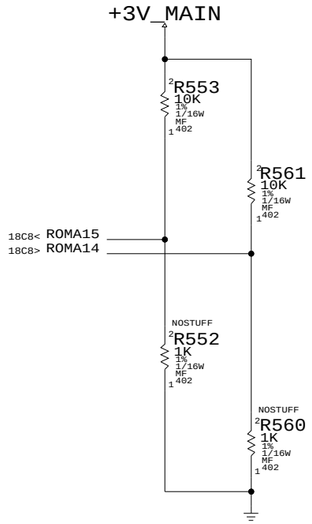


EXTERNAL VGA

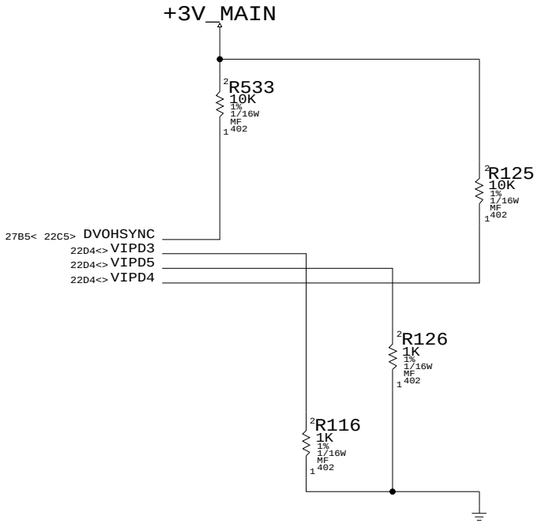
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6497	13
SCALE: NONE	SHT 25 OF 69	

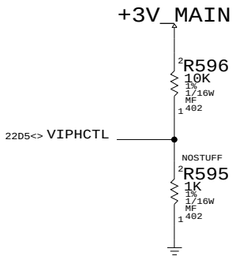
DRAWING



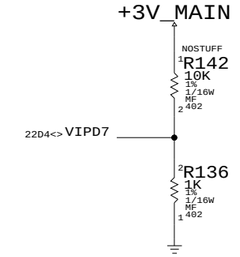
(1) ROM TYPE (OVERRIDDEN IF STRAP1 = 0)
[1..0] = [ROMA15,ROMA14]
00 = PARALLEL
01 = SERIAL AT25F
10 = SERIAL SST45VF
* 11 = SERIAL FUTURE



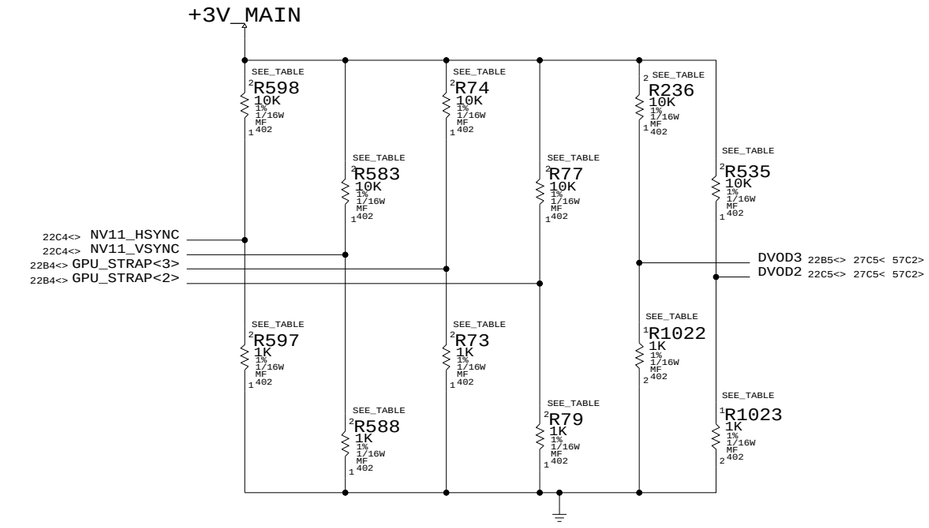
(3) PCI DEVICE ID
[3..0] = [DVOHSYNC,VIPD3,VIPD5,VIPD4]
0010 = 0X112 GEFORCE2 GO
0011 = 0X113 QUADRO2 GO
0100 = 0X114 NV17M
0000 = 0X110 GEFORCE2GO MX (NV11B)
* 1001 = NV18B,NV31,NV34



(5) HOST MODE
[0] = [VIPHCTL]
0 = PCI MODE
* 1 = AGP MODE



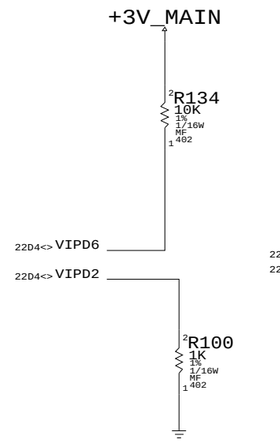
(6) AGP SIDEBAND
[0] = [VIPD7]
* 0 = ENABLE AGP SIDEBAND
1 = DISABLE AGP SIDEBAND



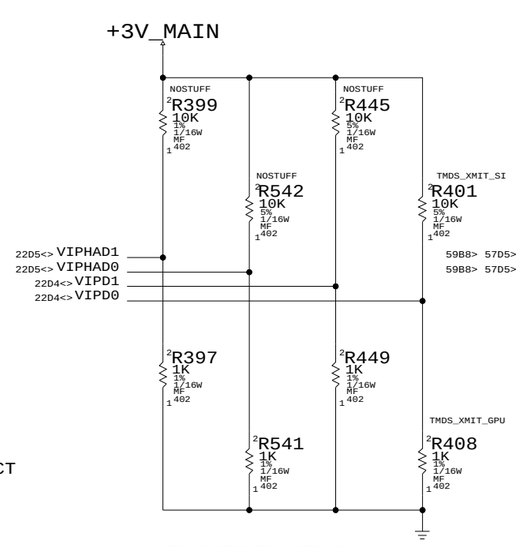
(8) FRAME BUFFER MEMORY TYPE
[3..0] = [NV11_HSYNC,NV11_VSYNC,GPU_STRAP<3>,GPU_STRAP<2>]
1111 = 222MHZ
1101 = 275MHZ SAMSUNG
1100 = 275MHZ HYNIX

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S1004	5	RES,10KOHM,1%,0402	R598,R583,R77,R236,R535		SAMSUNG_NV18B_270
114S1003	1	RES,1KOHM,1%,0402	R73		SAMSUNG_NV18B_270
114S1004	4	RES,10KOHM,1%,0402	R598,R583,R236,R535		HYNIX_NV18B_270
114S1003	2	RES,1KOHM,1%,0402	R73,R79		HYNIX_NV18B_270

114S1004	5	RES,10KOHM,1%,0402	R598,R583,R535,R74,R77		SAMSUNG_NV34_270
114S1003	1	RES,1KOHM,1%,0402	R1022		SAMSUNG_NV34_270
114S1004	4	RES,10KOHM,1%,0402	R583,R74,R77,R535		HYNIX_NV34_270
114S1003	2	RES,1KOHM,1%,0402	R597,R1022		HYNIX_NV34_270

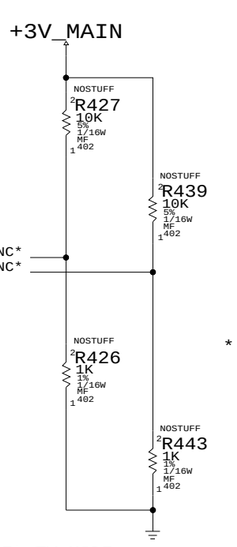


(2) CRYSTAL FREQUENCY SELECT
[1..0] = [VIPD6,VIPD2]
00 = 13.5MHZ
01 = 14.38MHZ
* 10 = 27MHZ
11 = {UNDEFINED}

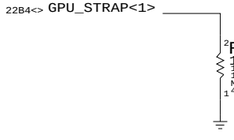


(4) USER DEFINED STRAPS
[3..0] = [VIPHAD1,VIPHAD0,VIPD1,VIPD0]

THESE BITS ARE UNDEFINED BUT THEY
MUST BE KEPT LOW DURING RESET

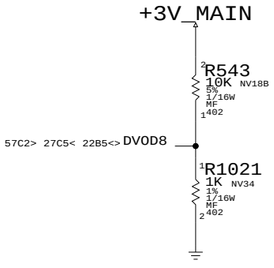


(7) TV MODE
[1..0] = [ANALOG_HSYNC*,ANALOG_VSYNC*]
00 = SECAM
01 = NTSC
10 = PAL
* 11 = DISABLED
(THESE RESISTORS ARE ALL NOSTUFF)



(9) SUB-VENDOR
[0] = [GPU_STRAP<1>]
0 = SYSTEM BIOS (VENDOR & SUBSYSTEM ID=0X0000)
1 = ADAPTER CARD VGA BIOS (VENDOR & SUBSYSTEM ID=0X54-0X57)

(10) PCI ADDRESS BUS
[0] = [GPU_STRAP<0>]
0 = REVERSED
* 1 = NORMAL



FASTWR
0 = ENABLE
1 = DISABLE

NVIDIA STRAPS 1

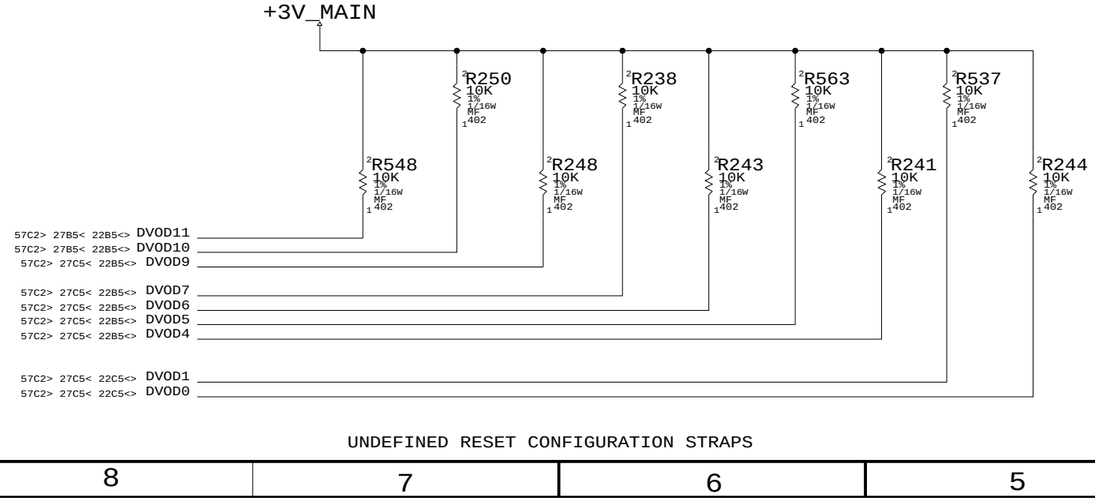
LAST_MODIFIED=Wed Sep 17 12:16:22 2003

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6497	13
SCALE: NONE	SHT 26 OF 69	

DRAWING

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S1003	1	RES,1K,1%,1/16W,0402	R1003	SI_SWING_LO
116S1000	1	RES,0 OHM,1%,1/16W,0402	R1003	SI_SWING_HI



NVIDIA STRAPS 2

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6497	13
SCALE: NONE	SHT 27 OF 69	

+2_5V_MAIN
+1_8V_MAIN
R571 0 1/16W MF 603
R572 0 1/16W MF 603
LT1962_INT_VIN
NC_UT6P7
NC_UT6P6
C234 1UF 10% 10V X5R 603
U19 LT1962-ADJ MSOP
IN OUT ADJ BYP GND SHDN NC NC
LT1962 INT ADJ
LT1962 INT BYP
C623 0.01UF 10% 16V CERM 402
R586 15.8K 1% 1/16W MF 402
C233 10UF 20% 6.3V CERM 805
52D3> 30D5< 16D6< 9D4< +1_5V_INTREPID_PLL

R630 4.7 5% 1/16W MF 402
C713 0.1UF 20% 10V CERM 402
C3005 0.1UF 20% 10V CERM 402
+1_5V_INTREPID_PLL8 52D3>
R629 4.7 5% 1/16W MF 402
INT_PLL9_GND 28A4<>
+1_5V_INTREPID_PLL4 52D3>
C704 0.1UF 20% 10V CERM 402
C3004 0.1UF 20% 10V CERM 402
INT_PLL7_GND 28A4<>
R628 4.7 5% 1/16W MF 402
+1_5V_INTREPID_PLL3 52D3>
C703 0.1UF 20% 10V CERM 402
C3003 0.1UF 20% 10V CERM 402
INT_PLL3_GND 28A4<>
R620 4.7 5% 1/16W MF 402
+1_5V_INTREPID_PLL2 52D3>
C692 0.1UF 20% 10V CERM 402
C3002 0.1UF 20% 10V CERM 402
INT_PLL2_GND 28A5<>
R565 4.7 5% 1/16W MF 402
+1_5V_INTREPID_PLL1 52D3>
C229 0.1UF 20% 10V CERM 402
C3001 0.1UF 20% 10V CERM 402
INT_PLL1_GND 28A5<>

+3V_MAIN
INTREPID DEBUG HOOKS
PLL TEST FUNCTION
HWPLL_TESTMUXSEL[0:5]
R231 R678 R289 R292 R291 R274 R228 R232 1K 1% 1/16W MF 402 NOSTUFF
INT_MOD_BITCLK 28A3<> 28A8<
INT_MOD_CLKOUT 28A3> 28A8<
INT_MOD_DTO 28A3> 28A8<
INT_MOD_SYNC 28A3<> 28A8< (INTREPID JTAG TDO)
INT_MOD_DTI 28A3< 28A8<
JTAG_INTRP_TDO 34B7> 35B3<
JTAG_ASIC_TDI 8A4<> 34B7< 59D8>
INT_TST_PLLEN_PD 34B7<
R574 R276 R708 R735 R727 R661 R577 R573 1K 1% 1/16W MF 402 NOSTUFF

TOO MANY MODS TO LIST, SEE INTREPID ERS
CONFIGURED FOR INTREPID VERSION 1
VIEW AGP CLOCK OUT LA CLOCK PIN

+3V_MAIN
GPIO & INTERRUPT PULL-UPS
R746 10K 1% 1/16W MF 402 AGP_INT_L 17B6<> 28B5<>
R749 10K 1% 1/16W MF 402 33SLOTB_INT_L
R750 10K 1% 1/16W MF 402 28B5<> UNUSED_EXTINT7 SPARE
R306 10K 1% 1/16W MF 402 28B5<> UNUSED_EXTINT8 SPARE
RP113 10K 5% 1/16W SM1
INT_GPIO9_PU 28B5<>
INT_EXTINT12_PU 28B5<>
INT_EXTINT17_PU 28B5<> 32B6>
INT_EXTINT3_PU 28B5<>
RP74 10K 5% 1/16W SM1 NO_TEST
COMM_RING_DET_L 28B5<> 29C5<>
INT_EXTINT13_PU 28B5<> 59D6>
NC_RPT77P6
PMU_INT_L 28B5<> 44B5<>
RP100 10K 5% 1/16W SM1 NO_TEST
NC_CBUS_INT_L
PMU_INT_NMI 28B5<> 44C4<>
PMU_REQ_L 28C3> 44C2<
EXTINT14 28B5<>
RP110 10K 5% 1/16W SM1 NO_TEST
NC_RP2848
INT_GPIO12_PU 28B5<>
INT_GPIO1_PD 28C5<>
SND_HW_RESET_L 28B5<> 39B4<
R589 10K 1% 1/16W MF 402
USB2_CRUN_L_INT 28B5<> 32A8<
R680 10K 1% 1/16W MF 402 INT_MOD_DTI 28A3< 28C6<
RP66 10K 5% 1/16W SM1 NOSTUFF
INT_MOD_CLKOUT 28A3> 28C6<
INT_MOD_DTO 28A3> 28C6<
INT_MOD_BITCLK 28A3<> 28C6<
INT_MOD_SYNC 28A3<> 28C6<

36B5<> 34C5<> FW_C_LKON
R747 0 5% 1/16W MF 402 NOSTUFF
33SLOTB_INT_L 28B7<> 31C2<> 59A6> 59A6>
(USB2.0 IRQ)

(518S0104)
J23 U.FL-R_SMT F-ST-SM
CLK18M_INT_EXT 59A6> 44B2<> 32A8< 31C2<
R666 0 5% 1/16W MF 402 NOSTUFF
R611 51 5% 1/16W MF 402 NOSTUFF
CLK18M_INT_XIN
CLK18M_INT_XOUT
44C4<> SYSTEM_CLK_EN
R672 10M 5% 1/16W MF 402 NOSTUFF
44C5<> INT_WATCHDOG_L
R711 0 5% 1/16W MF 402
NC_BRCLKO
Y5 18.432M CRITICAL 8X4.5MM-SM
CLK18M_INT_XO
C784 27PF 5% 50V CERM 402
C840 27PF 5% 50V CERM 402
R710 10K 1% 1/16W MF 402
53A6< INT_REF_CLK_IN_PD

U25 INTREPID BGA (6 OF 9) SEE_TABLE (ON PAGE 12)
GENERAL PURPOSE I/O'S
28D3< SNF_FSEL GPIO0
28A8< INT_GPIO1_PD GPIO1
59D6> 29D7<> 28D1< COMM_SHUTDOWN GPIO2
59A8> 29D5<> COMM_RESET_L GPIO3
36C8< FWPHYRST GPIO4
41A7< SND_HP_MUTE_L GPIO5
43C8< SND_AMP_MUTE_L GPIO6
28B8< INT_GPIO9_PU GPIO9
39B4< 28A8< SND_HW_RESET_L GPIO11
28A8< INT_GPIO12_PU GPIO12
59A6> 28C1< UNUSED_GPIO15 GPIO15
35B8< 28D1< INT_ENET_RST_L GPIO16

INTERRUPTS
59D6> 44C5> 29C5> 28B8< COMM_RING_DET_L EXTINT0
44B5<> 28B8< PMU_INT_L EXTINT1
28B8< 17B6<> AGP_INT_L EXTINT2
28B8< INT_EXTINT3_PU EXTINT3
59B6> 40D4< SND_LIN_SENSE_L EXTINT4
35B4> 28C1< ENET_ENERGY_DET EXTINT5
33SLOTB_INT_L EXTINT6
28B8<> UNUSED_EXTINT7 EXTINT7
28B8<> UNUSED_EXTINT8 EXTINT8
44C4<> 28A8< PMU_INT_NMI EXTINT9
28D3< VCORE_VGATE EXTINT10
32A8< USB2_CRUN_L_INT EXTINT11
28B8< INT_EXTINT12_PU EXTINT12
28B8< INT_EXTINT13_PU EXTINT13
28A8< EXTINT14 EXTINT14
59B8> 41A5< SND_HP_SENSE_L EXTINT15
42B8< SND_SPKR_ID EXTINT16
32B6> 28B8< INT_EXTINT17_PU EXTINT17
8D7<> 7A5< 4B3< MPIC_CPU_INT_L CPU_INT

PCIPME
PROCSLEEPREQ 44B4<> INT_PROC_SLEEP_REQ_L
PENDPROCINT 44B4<> INT_PEND_PROC_INT

CLOCKS
XTAL_IN
XTAL_OUT
STOPXTAL
WATCHDOG
BUF_REF_CLK_OUT
SS_REF_CLK_IN

USB
USB_VD0_P USB_VD0_N 58B5> 28A3< USB_DAP USB_DAN 402 24 R724 USB1 USB_DAP_F 33B7< 58B5>
R718 USB1 USB_DAN_F 33B7< 58B5>
USB_VD1_P USB_VD1_N 58B5> 28A3< USB_DBP USB_DBN 402 24 R736 USB1 USB_DBP_F 33C7< 58B5>
R742 USB1 USB_DBN_F 33C7< 58B5>
USB_PRTPWR0 USB_PWRFLT0 J4 K4 USB_PWREN_AB_L 28C2< USB_PWR_FLT* 28C1< 32B1< 33A7>
USB_VD2_P USB_VD2_N H2 H1 58B5> 28A3< USB_DCP USB_DCN 402 24 R723 USB1 USB_DCP_F 33D7< 58B5>
R728 USB1 USB_DCN_F 33D7< 58B5>
USB_VD3_P USB_VD3_N M7 M8 USB_DDP USB_DDN 402 24 R694 R691 USB_DDP_F_TERM USB_DDN_F_TERM
USB_PRTPWR1 USB_PWRFLT1 J2 J1 USB_PWREN_CD_L 28C2<
USB_VD4_P USB_VD4_N K5 L5 58B5> USB_DEP USB_DEN 402 22 R762 R763 BT_USB_DP 29D3<> 58B5> 59B6> BT_USB_DM 29D3<> 58A5> 59B6>
USB_VD5_P USB_VD5_N P8 N8 58A5> USB_DFP USB_DFN 402 22 R271 R272 MODEM_USB_DP 29C5<> 58A5> 59B6> MODEM_USB_DM 29C5<> 58A5> 59B6>
USB_PRTPWR2 USB_PWRFLT2 M5 N7 USB_PWREN_EF_L 28C2< USB_OC_EF_L 28C2<

AUDIO/I2S
AUD_DTO R4 INT_SND_TO_AUDIO 47 4 RP108 SND_TO_AUDIO 39C4<
AUD_DTI R7 AUDIO_TO_SND AUDIO_TO_SND 39C1<
AUD_SYNC T5 INT_SND_SYNC 47 2 RP108 SND_SYNC 39C1<>
AUD_BITCLK P2 INT_SND_SCLK 47 3 RP108 SND_SCLK 39B1<>
AUD_CLKOUT R5 INT_SND_CLKOUT 47 1 RP108 SND_CLKOUT 39B4<
MOD_DTO R2 INT_MOD_DTO 28A8< 28C6<
MOD_DTI T4 INT_MOD_DTI 28A8< 28C6<
MOD_SYNC R1 INT_MOD_SYNC 28A8< 28C6<
MOD_BITCLK V8 INT_MOD_BITCLK 28A8< 28C6<
MOD_CLKOUT P1 INT_MOD_CLKOUT 28A8< 28C6<
R3001 R3002 R650 R651 R660 15K 1% 1/16W MF 402
R683 10K 1% 1/16W MF 402

IIC
IICCLK_2 AL4 INT_I2C_CLK2 28D1< 29C7<> 34B5< 39B1<> 59A8>
IICDATA_2 AH8 INT_I2C_DATA2 28D1< 29C7<> 34B5< 39B1<> 59A8>

VIA
SPI MISO REQ* MOSI ACK* SCK
SCCTXDA SCCRTSA SCCDTRA SCCRXDA SCCGPIOA SCCTRXCA SCCTXDB SCCRTSB SCCRXDB SCCGPIOB SCCTRXCB
COMM_TXD_L 29C7<> 59C6>
COMM_RTS_L 29D5<> 59C6>
COMM_DTR_L 29C7<> 59C6>
COMM_RXD 29C5<> 59C6>
COMM_GPIO_L 28D3< 29C5<> 59C6>
COMM_TRXC 28D3< 29C7<> 59C6>
PMU_FROM_INT 44C4<>
PMU_REQ_L 28A8< 44C2<
PMU_TO_INT 44C4<>
PMU_ACK_L 44C4<>
PMU_CLK 44C4<>

+3V_MAIN
NC_RPT48P1 RP39 10K 5% 1/16W SM1 NO_TEST
59C6> 29C5<> 28C3<> COMM_GPIO_L
NC_RP3319 NO_TEST
59C6> 29C7<> 28C3<> COMM_TRXC
28C5<> SNF_FSEL
R755 1K 1% 1/16W MF 402
28B5<> VCORE_VGATE
R756 10K 1% 1/16W MF 402

+3V_INTREPID_USB 52A3>
L16 FERR-EMI-100-OHM SM
C785 0.01UF 20% 10V CERM 402
C795 0.1UF 20% 10V CERM 402
C820 4.7UF N20P80% 10V CERM 805

I2C 2 PULL-UPS
+3V_MAIN
59A8> 39B1<> 34B5< 29C7<> 28A3<> INT_I2C_CLK2 R264 4.7K 5% 1/16W MF 402
39B1<> 34B5< 29C7<> 28A3<> 59A8> INT_I2C_DATA2 R641 4.7K 5% 1/16W MF 402
59D6> 29D7<> 28C5<> COMM_SHUTDOWN RP117 10K 5% 1/16W SM1
35B8< 28B5<> INT_ENET_RST_L RP117 10K 5% 1/16W SM1
35B4> 28B5<> ENET_ENERGY_DET RP117 10K 5% 1/16W SM1
NC_RP3324_2 NO_TEST RP117 10K 5% 1/16W SM1
33A7> 32B1< 28B3< USB_PWR_FLT* R1005 10K 1% 1/16W MF 402

USB PULL-UPS
+3V_MAIN
RP60 10K 5% 1/16W SM1
28B3< USB_OC_EF_L
28B3<> USB_PWREN_CD_L
28B3<> USB_PWREN_AB_L
28B3<> USB_PWREN_EF_L

+3V_MAIN
59A6> 28B5<> UNUSED_GPIO15
R294 10K 1% 1/16W MF 402
NOSTUFF R267 10K 1% 1/16W MF 402

58B5> 28B3<> USB_DAP 402 15K R305 USB2
58B5> 28B3<> USB_DAN 402 15K R396 USB2
58B5> 28B3<> USB_DBP 402 15K R247 USB2
58B5> 28B3<> USB_DBN 402 15K R398 USB2
58B5> 28B3<> USB_DCP 402 15K R333 USB2
58B5> 28B3<> USB_DCN 402 15K R493 USB2

VSSA1 (PLL1) VSSA2 (PLL2) VSSA3 (PLL3) VSSA4 (PLL7) VSSA_8 (PLL9) VSSU_1 VSSU_2
AA15 AJ13 AJ16 AK18 AH20 R9 R8
XW42 XW43 XW44 XW45 XW46 SM
28C4< INT_PLL1_GND NO_TEST
28D4< INT_PLL2_GND NO_TEST
NO_TEST INT_PLL9_GND 28D4<
NO_TEST INT_PLL7_GND 28D4<
NO_TEST INT_PLL3_GND 28D4<

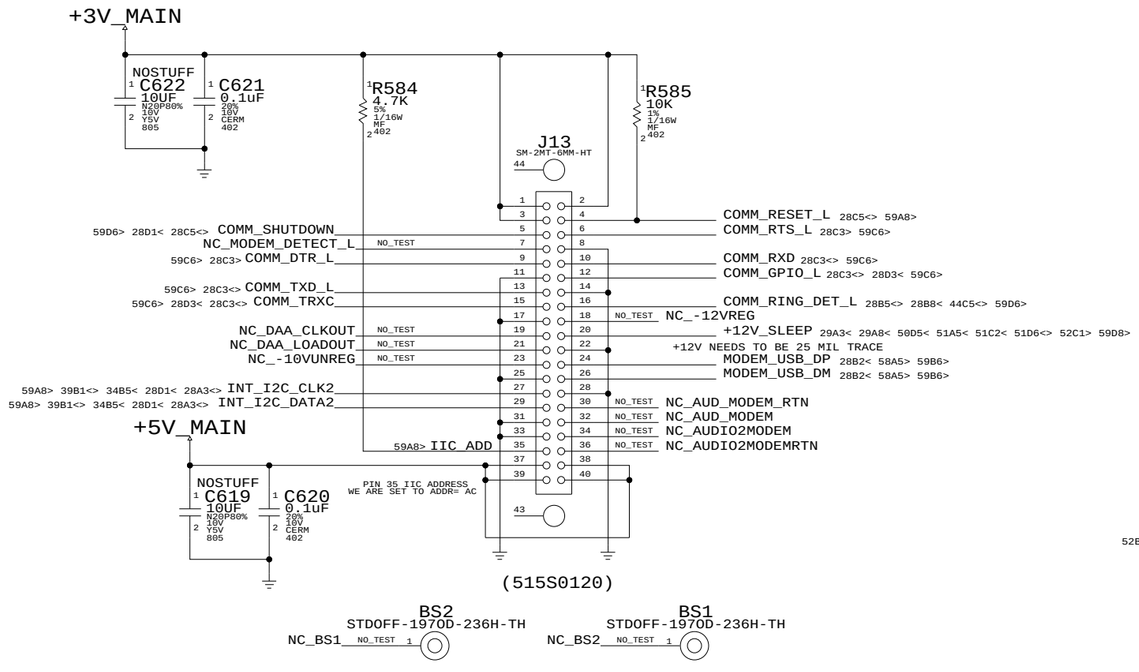
INTREPID GPIO/ SCC/USB/I2S

NOTICE OF PROPRIETARY PROPERTY
LAST_MODIFIED=Wed Sep 17 12:16:27 2003
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.
SIZE D | DRAWING NUMBER 051-6497 | REV: 13
SCALE NONE | SHT 28 OF 69
DRAWING

MODEM BOARD CONNECTOR

(DASH II)



(515S0120)

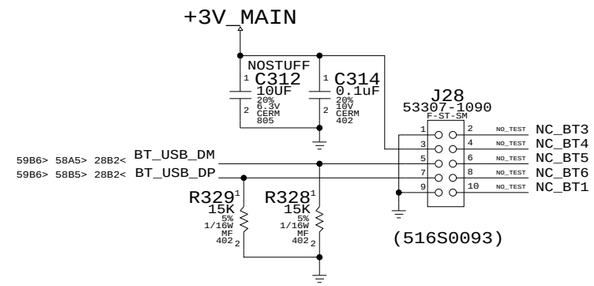
BS2 STDOFF-1970D-236H-TH NC_BS1 NO_TEST

BS1 STDOFF-1970D-236H-TH NC_BS2 NO_TEST

MODEM STANDOFF SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
860-1034	2	STDOFF-19709-236H-TH	BS1,BS2		

BLUETOOTH CONNECTOR



BS3 STDOFF-1970D-236H-TH NC_BS3 NO_TEST

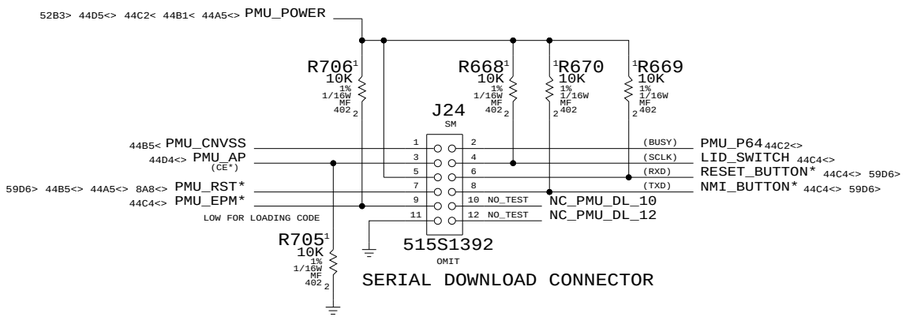
BS4 STDOFF-1970D-236H-TH NC_BS4 NO_TEST

BS4 SHORTEST STANDOFF
FURTHEST FROM J28

BLUETOOTH CARD MOUNTING HARDWARE SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
860-0170	1	STDOFF,BLUETOOTH,SHORT	BS4		
860-0171	1	STDOFF,BLUETOOTH,LONG	BS3		

SERIAL DOWNLOAD INTERFACE

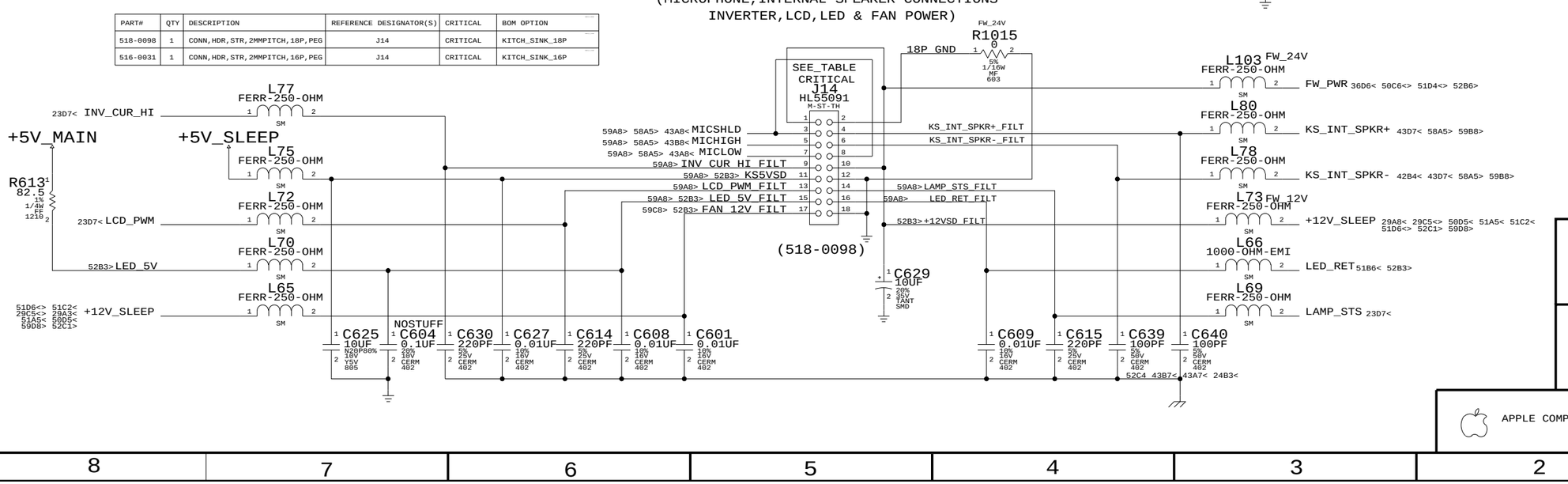


SERIAL DOWNLOAD CONNECTOR

'KITCHEN SINK' CONNECTOR

(MICROPHONE,INTERNAL SPEAKER CONNECTIONS
INVERTER,LCD,LED & FAN POWER)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
518-0098	1	CONN,HDR,STR,2MMPITCH,18P,PEG	J14	CRITICAL	KITCH_SINK_18P
516-0031	1	CONN,HDR,STR,2MMPITCH,16P,PEG	J14	CRITICAL	KITCH_SINK_16P



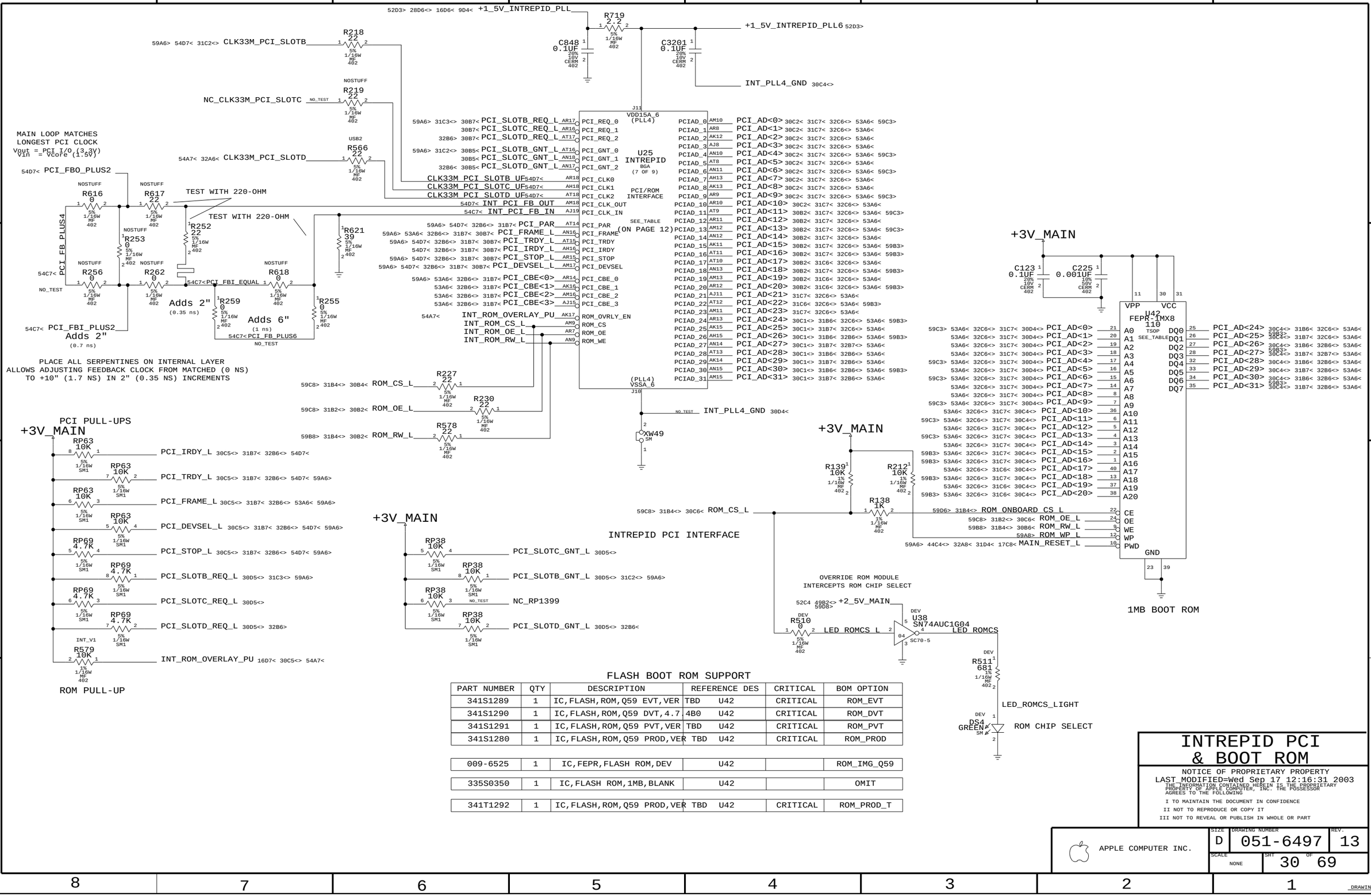
MODEM, BLUETOOTH, KITCHEN SINK & SERIAL DOWNLOAD

LAST_MODIFIED=Wed Sep 17 12:16:29 2003

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6497	13
SCALE: NONE	SHT 29 OF 69	

DRAWING



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S1289	1	IC,FLASH,ROM,Q59 EVT,VER	TBD U42	CRITICAL	ROM_EVT
341S1290	1	IC,FLASH,ROM,Q59 DVT,4.7	4B0 U42	CRITICAL	ROM_DVT
341S1291	1	IC,FLASH,ROM,Q59 PVT,VER	TBD U42	CRITICAL	ROM_PVT
341S1280	1	IC,FLASH,ROM,Q59 PROD,VER	TBD U42	CRITICAL	ROM_PROD
009-6525	1	IC,FEPR,FLASH ROM,DEV	U42		ROM_IMG_Q59
335S0350	1	IC,FLASH ROM,1MB,BLANK	U42		OMIT
341T1292	1	IC,FLASH,ROM,Q59 PROD,VER	TBD U42	CRITICAL	ROM_PROD_T

INTREPID PCI & BOOT ROM

LAST_MODIFIED=Wed Sep 17 12:16:31 2003

APPLE COMPUTER INC.

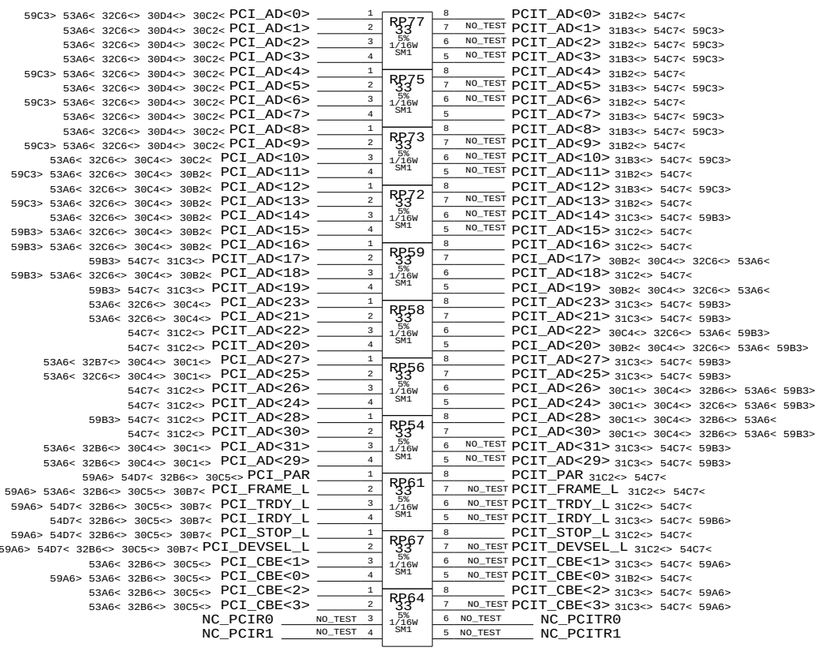
SIZE	DRAWING NUMBER	REV.
D	051-6497	13

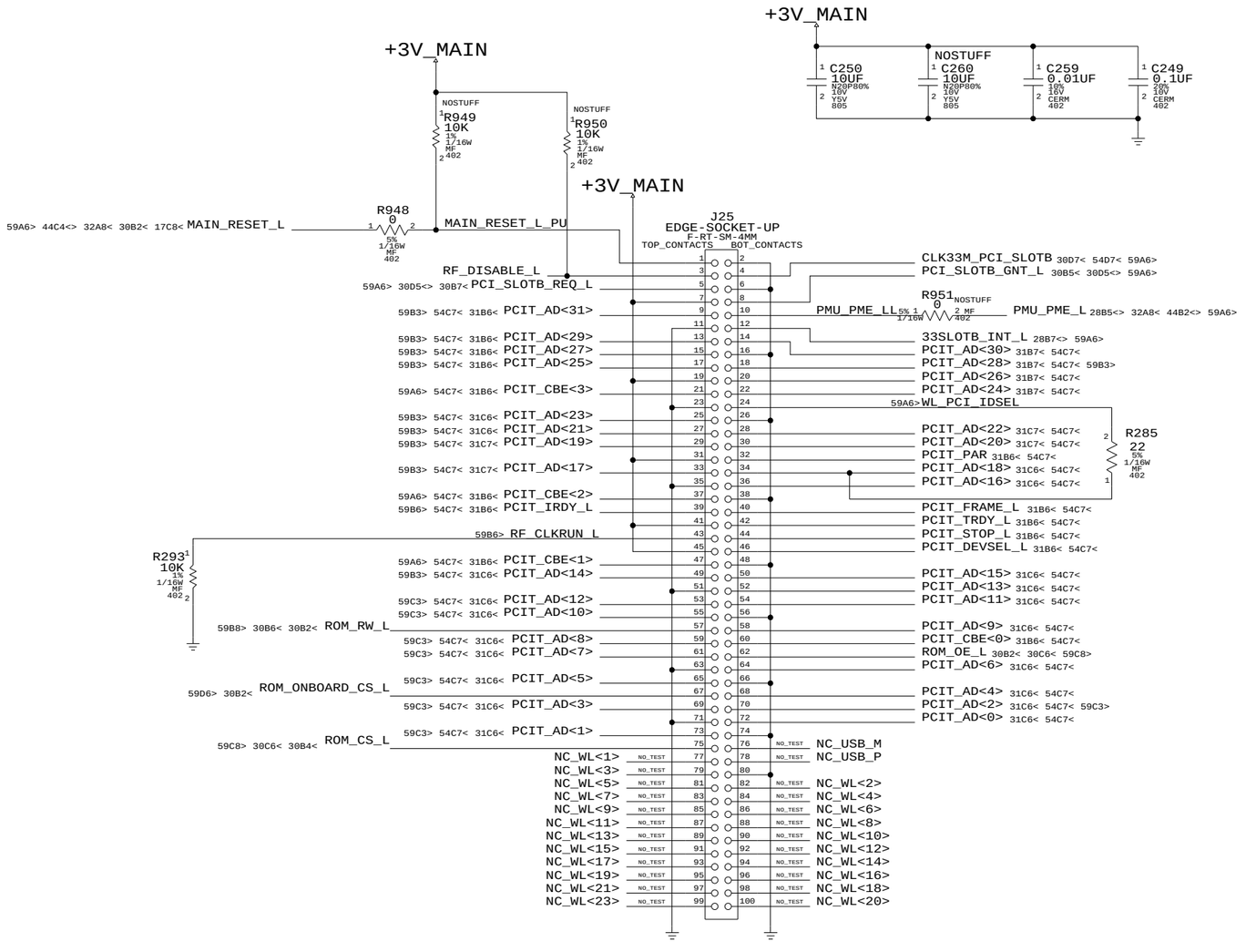
SCALE: NONE

SHT 30 OF 69

DRAWING

PLACE RP'S NEAR WIRELESS CONNECTOR





(516S0046)

WIRELESS CARD MOUNTING HARDWARE SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
815-7245	1	WIRELESS CARD GUIDE,J25	J251		
452-0411	2	NUT,HEX,M2 X 1.5H, J25	J252,J253		
452-0412	2	SCREW,M2 X 0.4 X 6.0 L,J25	J254,J255		

WIRELESS PCI

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6497	13
SCALE: NONE	SHT 31 OF 69	

DRAWING

+3V_MAIN

USB2 C519 0.1UF 20% 10V CERM 402
USB2 C522 0.1UF 20% 10V CERM 402
USB2 C527 0.1UF 20% 10V CERM 402
USB2 C547 0.1UF 20% 10V CERM 402
USB2 C523 0.1UF 20% 10V CERM 402
USB2 C541 0.1UF 20% 10V CERM 402
USB2 C548 0.1UF 20% 10V CERM 402
USB2 C555 0.1UF 20% 10V CERM 402
USB2 C559 0.1UF 20% 10V CERM 402
USB2 C546 0.1UF 20% 10V CERM 402
USB2 C516 0.1UF 20% 10V CERM 402
USB2 C537 0.1UF 20% 10V CERM 402
USB2 C536 0.1UF 20% 10V CERM 402
USB2 C515 0.1UF 20% 10V CERM 402
USB2 C570 0.1UF 20% 10V CERM 402
USB2 C530 0.1UF 20% 10V CERM 402
NOSTUFF C517 10UF N20P80% 10V Y5V 805
USB2 C573 10UF N20P80% 10V Y5V 805
NOSTUFF C574 10UF N20P80% 10V Y5V 805
USB2 C531 10UF N20P80% 10V Y5V 805

+3V_MAIN

USB2 L58 100-OHM-EMI SM

USB2 C526 0.1UF 20% 10V CERM 402
USB2 C529 0.1UF 20% 10V CERM 402
USB2 C511 10UF N20P80% 10V Y5V 805

52A3> NEC_AVDD

NOSTUFF R89 100K 1% 1/16W MF 402

NEC_XT2_B

Y7 30.0000M CRITICAL 8X4.5MM-SM USB2

USB2 C77 10PF 5% 50V CERM 402
USB2 C114 10PF 5% 50V CERM 402

USB2 R129 100 1% 1/16W MF 402

USB2

H3 M4 C8 P2 P3 P12 A13 A12 A3 E2 N8 L13 J13 H13 F13 D13 G12 H4 D7 — VDD
N10 N12 — AVDD

VDD_PCI

U11
NEC_UPD720101_USB2
FBGA

CRITICAL

59C3> 53A6< 31C7< 30D4<> 30C2<	PCI_AD<0>	M5	AD0			
53A6< 31C7< 30D4<> 30C2<	PCI_AD<1>	P5	AD1			
53A6< 31C7< 30D4<> 30C2<	PCI_AD<2>	N5	AD2			
53A6< 31C7< 30D4<> 30C2<	PCI_AD<3>	P4	AD3			
59C3> 53A6< 31C7< 30D4<> 30C2<	PCI_AD<4>	N4	AD4			
53A6< 31C7< 30D4<> 30C2<	PCI_AD<5>	M3	AD5			
59C3> 53A6< 31C7< 30D4<> 30C2<	PCI_AD<6>	N3	AD6			
53A6< 31C7< 30D4<> 30C2<	PCI_AD<7>	M1	AD7			
53A6< 31C7< 30D4<> 30C2<	PCI_AD<8>	L2	AD8			
59C3> 53A6< 31C7< 30D4<> 30C2<	PCI_AD<9>	L1	AD9			
53A6< 31C7< 30C4<> 30C2<	PCI_AD<10>	K2	AD10			
59C3> 53A6< 31C7< 30C4<> 30B2<	PCI_AD<11>	L3	AD11			
53A6< 31C7< 30C4<> 30B2<	PCI_AD<12>	K1	AD12			
59C3> 53A6< 31C7< 30C4<> 30B2<	PCI_AD<13>	K3	AD13			
53A6< 31C7< 30C4<> 30B2<	PCI_AD<14>	J2	AD14			
59B3> 53A6< 31C7< 30C4<> 30B2<	PCI_AD<15>	J1	AD15			
59B3> 53A6< 31C7< 30C4<> 30B2<	PCI_AD<16>	F2	AD16			
53A6< 31C6< 30C4<> 30B2<	PCI_AD<17>	E3	AD17			
59B3> 53A6< 31C7< 30C4<> 30B2<	PCI_AD<18>	E1	AD18			
53A6< 31C6< 30C4<> 30B2<	PCI_AD<19>	D3	AD19			
59B3> 53A6< 31C6< 30C4<> 30B2<	PCI_AD<20>	D1	AD20			
53A6< 31C7< 30C4<>	PCI_AD<21>	D2	AD21			
59B3> 53A6< 31C6< 30C4<>	PCI_AD<22>	C2	AD22			
53A6< 31C7< 30C4<>	PCI_AD<23>	C1	AD23			
59B3> 53A6< 31B6< 30C4<> 30C1<>	PCI_AD<24>	B4	AD24			
53A6< 31B7< 30C4<> 30C1<>	PCI_AD<25>	A4	AD25			
59B3> 53A6< 31B6< 30C4<> 30C1<>	PCI_AD<26>	B5	AD26			
53A6< 31B7< 30C4<> 30C1<> PCI_AD<27>		C4	AD27			
53A6< 31B6< 30C4<> 30C1<>	PCI_AD<28>	A5	AD28			
53A6< 31B7< 30C4<> 30C1<>	PCI_AD<29>	C5	AD29			
59B3> 53A6< 31B6< 30C4<> 30C1<>	PCI_AD<30>	B6	AD30			
53A6< 31B7< 30C4<> 30C1<>	PCI_AD<31>	A6	AD31			
59A6> 53A6< 31B7< 30C5<>	PCI_CBE<0>	M2	CBE0			
53A6< 31B7< 30C5<>	PCI_CBE<1>	J3	CBE1			
53A6< 31B7< 30C5<>	PCI_CBE<2>	F1	CBE2			
53A6< 31B7< 30C5<>	PCI_CBE<3>	C3	CBE3			
59A6> 54D7< 31B7< 30C5<>	PCI_PAR	J4	PAR			
59A6> 53A6< 31B7< 30C5<> 30B7<	PCI_FRAME_L	F3	FRAME			
54D7< 31B7< 30C5<> 30B7<	PCI_IRDY_L	F4	IRDY			
59A6> 54D7< 31B7< 30C5<> 30B7<	PCI_TRDY_L	G1	TRDY			
59A6> 54D7< 31B7< 30C5<> 30B7<	PCI_STOP_L	G3	STOP			
	USB2_IDSEL	B3	IDSEL			
59A6> 54D7< 31B7< 30C5<> 30B7<	PCI_DEVSEL_L	G2	DEVSEL			
30D5<> 30B7<	PCI_SLOTD_REQ_L	C6	REQ			
30D5<> 30B5<	PCI_SLOTD_GNT_L	D6	GNT			
	PCI_SLOTD_PERR_L	H2	PERR			
	33PCI_SLOTD_SERR_L	OD H1	SERR			
28B8< 28B5<>	INT_EXTINT17_PU	OD C7	INTA			
		OD B7	INTB			
		OD A7	INTC			
54A7< 30D7<	CLK33M_PCI_SLOTD	A8	PCLK			
59A8> 44D3< 44B8<> 35B8<	IO_RESET_L	B8	VBBRST	STARTUP & RESTARTS		
	USB2_CRUN_L	N6	CRUN			
	USB2_PME_L	OD D9	PME			
		C9	VCCRST	STARTUP, RESTARTS, WAKEUP		
	NC_USB2_SMI_L	OD L6	SMI			
		L7	LEGC			

VSS — B1 N1 P10 N14 H14 B14 A2 B2 N2 M13 B13 M11 L12 H12 D12 G4 J11 F11 D8

XT1/SCLK	L9	56B3>	USB2_XT1	
XT2	P8	56B3>	USB2_XT2	
RSDM1	M14	56B3>	USB2_RSDAM	R464 35.7 → USB2_DAN_F 33B7< 56B3>
DM1	M13		USB2_DAN_F	
DP1	L14		USB2_DAP_F	R465 35.7 → USB2_DAP_F 33B7< 56B3>
RSDP1	K13	56B3>	USB2_RSDAP	
RSDM2	K14	56B3>	USB2_RSDBM	R466 35.7 → USB2_DBN_F 33C7< 56B3>
DM2	K12		USB2_DBN_F	
DP2	J14		USB2_DBP_F	R467 35.7 → USB2_DBP_F 33C7< 56B3>
RSDP2	J12	56B3>	USB2_RSDBP	
RSDM3	H11	56B3>	USB2_RSDCM	R468 35.7 → USB2_DCN_F 33D7< 56B3>
DM3	G11		USB2_DCN_F	
DP3	G13		USB2_DCP_F	R469 35.7 → USB2_DCP_F 33D7< 56B3>
RSDP3	G14	56B3>	USB2_RSDCP	
RSDM4	F12		NC_USB2_RSDEM	
DM4	F14			
DP4	E12			
RSDP4	E14		NC_USB2_RSDEP	
RSDM5	E13		NC_USB2_RSDFM	
DM5	D14			
DP5	C13			
RSDP5	C14		NC_USB2_RSDFP	
56B3> RREF	P11		USB2_RREF	R476 9.09K 1% 1/16W MF 402 TIED TO BALL N11
OCI1	B12		USB_PWR_FLT*	→ USB_PWR_FLT* 28B3< 28C1< 33A7>
OCI2	B11			
OCI3	B10			
OCI4	A10		U_USB_PWR_FLT*	
OCI5	B9			
PPON1	C12		NC_USB2_PPON1	
PPON2	A11		NC_USB2_PPON2	
PPON3	C11		NC_USB2_PPON3	
PPON4	C10		NC_USB2_PPON4	
PPON5	A9		NC_USB2_PPON5	
NC1	P6		USB2_NC1	
NC2	M6		USB2_NC2	
NTEST1	M8		NC_USB2_NTEST1	
SMC	M7		NC_USB2_SMC	
TEB	N7		NC_USB2_TEB	
AMC	P7		NC_USB2_AMC	
TEST	L8		NC_USB2_TEST	
NANDTEST	M10		NC_USB2_NANDTEST	
SRCLK	M9		NC_USB2_SRCLK	
SRDTA	N9		NC_USB2_SRDTA	
SRMOD	P9		NC_USB2_SRMOD	
AVSS				

AVSS(R) — N11 P13 M12

OVERLAP STUFFING OF 35.7OHMS HERE WITH 0OHMS ON SH31 TO MINIMIZE STUBS

+3V_MAIN

USB2 R480 4.7K 5% 1/16W MF 402

+3V_MAIN

USB2 R470 2.2K 5% 1/16W MF 402
USB2 R490 2.2K 5% 1/16W MF 402

+3V_MAIN

USB2 R127 4.7K 5% 1/16W MF 402
USB2 R128 4.7K 5% 1/16W MF 402
USB2 R494 22 5% 1/16W MF 402

USB2 R484 0 5% 1/16W 402
44B2<> 31C2< 28B5<> 59A6> PMU_PME_L

NOSTUFF R373 0 5% 1/16W 402
28B5<> 28A8< USB2_CRUN_L_INT

R78 1K 1% 1/16W MF 402

+3V_MAIN

R1029 4.7K 5% 1/16W MF 402 D3_HOT

D3_COLD R1028 0 5% 1/16W MF 402
44C4<> 31D4< 30B2< 17C8< 59A6> MAIN_RESET_L

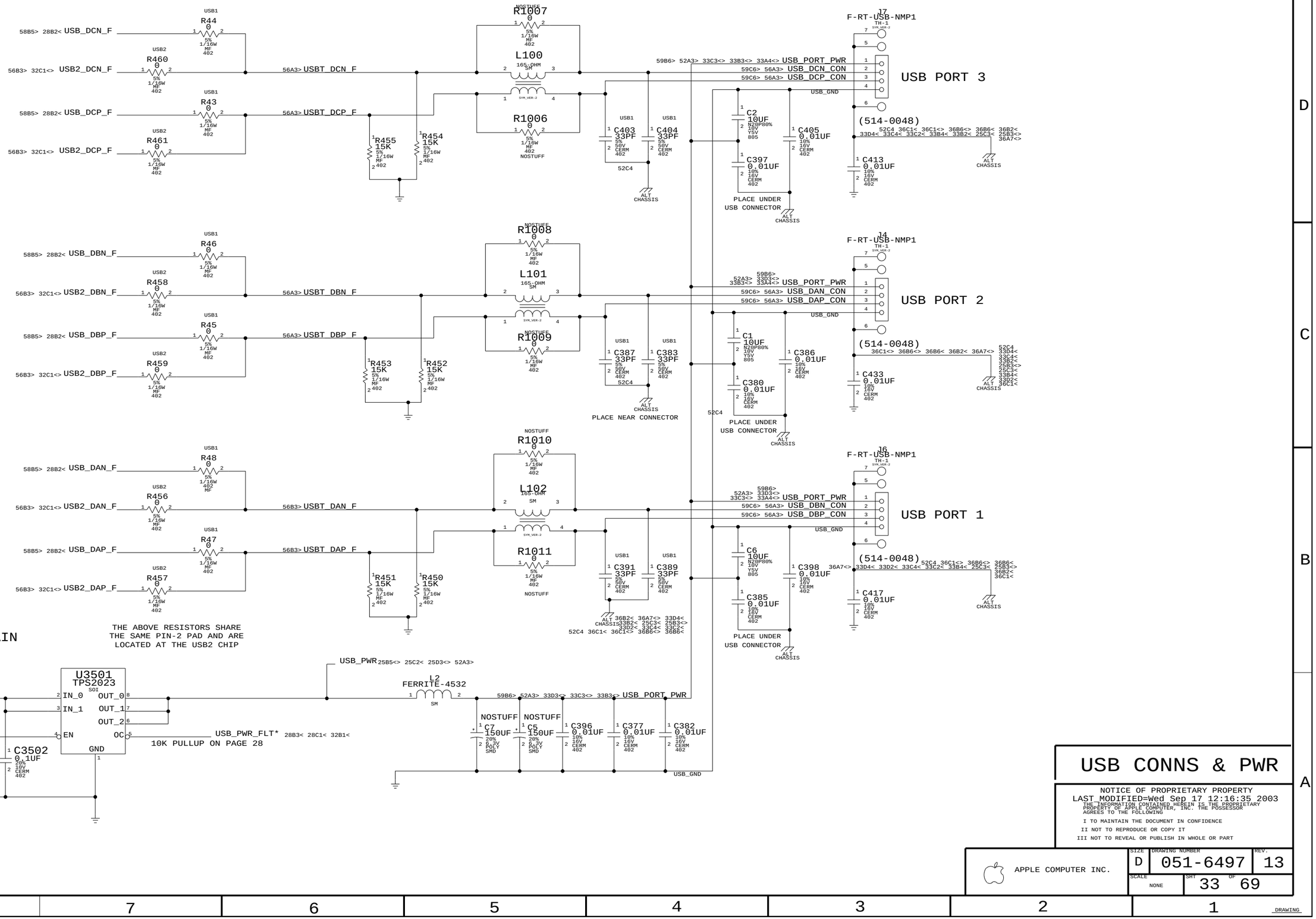
USB2_VCCRST

USB2 CONTROLLER

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6497	13
SCALE: NONE	SHT 32 OF 69	

DRAWING



USB CONNS & PWR

APPLE COMPUTER INC.
SIZE D | DRAWING NUMBER 051-6497 | REV: 13
SCALE NONE | SHT 33 OF 69
DRAWING

CLKENET_LINK_TX
R307 33 5% 1/16W MF 402
ENET_PHY_TX_EN → ENET_LINK_TX_EN
R303 33 5% 1/16W MF 402
ENET_PHY_TX_ER → ENET_LINK_TX_ER
RP70 33 1/16W 5% SM1
ENET_PHY_TXD<0> → ENET_LINK_TXD<0>
ENET_PHY_TXD<1> → ENET_LINK_TXD<1>
ENET_PHY_TXD<2> → ENET_LINK_TXD<2>
ENET_PHY_TXD<3> → ENET_LINK_TXD<3>
NC_ENET_LINK_TXD<4>
NC_ENET_LINK_TXD<5>
NC_ENET_LINK_TXD<6>
NC_ENET_LINK_TXD<7>
CLKENET_LINK_RX
ENET_RX_DV
ENET_RX_ER
ENET_LINK_RXD<0>
ENET_LINK_RXD<1>
ENET_LINK_RXD<2>
ENET_LINK_RXD<3>
RP76 33 1/16W 5% SM1
ENET_LINK_RXD<4>
ENET_LINK_RXD<5>
ENET_LINK_RXD<6>
ENET_LINK_RXD<7>
CLKENET_LINK_GBE_REF
NC_CLKENET_LINK_GTX
ENET_CRS
ENET_COL
ENET_MDIO
ENET_MDC
JTAG_ASIC_TDI
JTAG_INTRP_TDO
JTAG_ASIC_TCK
JTAG_ASIC_TMS
JTAG_ASIC_TRST_L
INT_JTAG_TEI
INT_TST_MONIN_PD
NC_INT_TST_MONOUT_TP
INT_TST_PLLEN_PD
R714 1K 1% 1/16W MF 402
NOSTUFF C92 47PF 5% 50V CERM 402

U25 INTREPID BGA (4 OF 9)
SEE_TABLE (ON PAGE 12)

GB ETHERNET: TX_CLK, TX_EN, TX_ER, TXD_0..TXD_7, RX_CLK, RX_DV, RX_ER, RXD_0..RXD_7, GBE_REFCLK, GTX_CLK, CRS, COL, MDIO, MDC
MISC: RESET (U5) ← RINT_RESET_L; PURESET (T2) ← RINT_PU_RESET_L
FIREWIRE: PHY_DATA0..PHY_DATA7, PHY_LPS, PHY_CTL0, PHY_CTL1, PHY_LREQ, FWR_PCLK, FWR_LCLK, FW_LINKON, FW_PINT
TEST: TDI, TDO, TCK, TMS, TRSTN, TEI, TST_MONIN, TST_MONOUT, TST_PLLEN
IICCLK_0, IICDATA_0, IICCLK_1, IICDATA_1

R707 47 5% 1/16W MF 402 → INT_RESET_L 35B8< 41A7< 43C7< 44D2<>
R275 47 5% 1/16W MF 402 → INT_PU_RESET_L 15B3< 44C2<>
FW_LINK_DATA<0>..<7> → RP112 22 5% 1/16W SM1 / RP65 22 5% 1/16W SM1 → FW_D<0>..FW_D<7> 36C8< 57A5>
FW_LPS 36C8<
FW_LINK_CNTL<0> → R269 22 5% 1/16W MF 402 → FW_CNTL0 36C8< 57A5>
FW_LINK_CNTL<1> → R709 22 5% 1/16W MF 402 → FW_CNTL1 36C8< 57A5>
FW_LINK_LREQ → R702 22 5% 1/16W MF 402 → FW_LREQ 36C8< 57A5>
FW_SCLK 36C8< 57A5>
CLKFW_LINK_LCLK
FW_C_LKON 28B6< 36B5<>
FW_PINT 34C1<
R673 1K 1% 1/16W MF 402

INT_I2C_CLK0R
INT_I2C_DATA0R
INT_I2C_CLK1
INT_I2C_DATA1
INT_I2C_CLK2
INT_I2C_DATA2

INT_V2 R257 0 MF 5% 1/16W 402 → INT_I2C_CLK0 14A6<> 15A6<
INT_V2 R254 0 MF 5% 1/16W 402 → INT_I2C_DATA0 14A6<> 15A6<
INT_V1 R637 0 MF 5% 1/16W 402
INT_V1 R647 0 MF 5% 1/16W 402

+3V_MAIN
NOSTUFF J18 M-ST-LK TH
(515-1560)
I2C DEBUG HEADER

INTREPID VERSION 1 HAS AN I2C BUS PROBLEM
USE KEY LARGO'S I2C INSTEAD.
FIXED IN INTREPID VERSION 2

INT_I2C_CLK1 34B1<
INT_I2C_DATA1 34B1<

TEST PULL-DOWNS
INT_JTAG_TEI → R575 1K 1% 1/16W MF 402
INT_TST_MONIN_PD → R576 1K 1% 1/16W MF 402
FW_PINT → R684 10K 1% 1/16W MF 402

I2C 3.3V PULL-UPS
+3V_MAIN
INT_I2C_CLK0R → RP119 4.7K 5% 1/16W SM1
INT_I2C_DATA0R → RP119 4.7K 5% 1/16W SM1
INT_I2C_CLK1 → RP101 4.7K 5% 1/16W SM1
INT_I2C_DATA1 → RP101 4.7K 5% 1/16W SM1

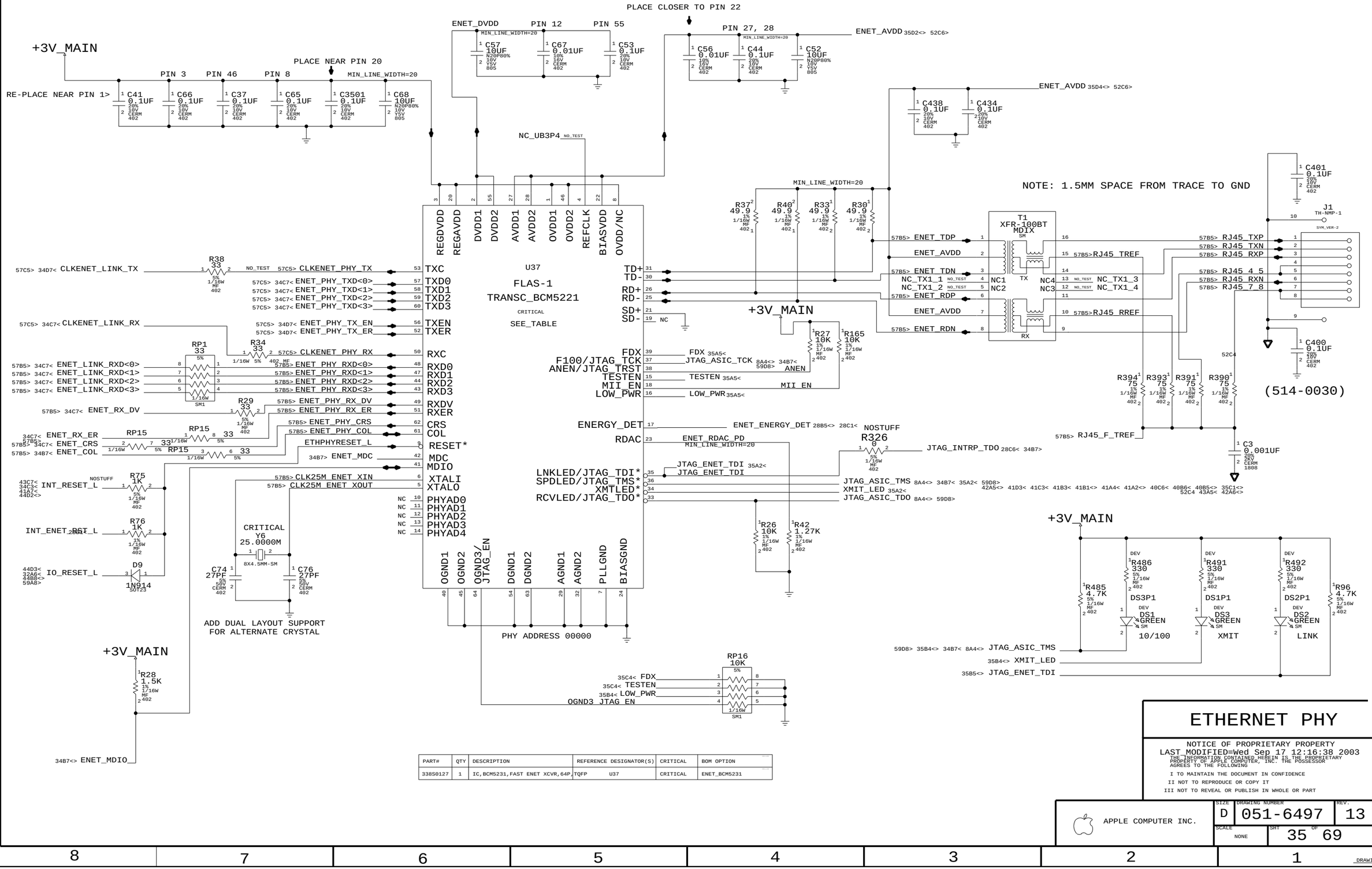
INTREPID ENET & FW

LAST_MODIFIED=Wed Sep 17 12:16:36 2003

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6497	13

SCALE: NONE
SHT 34 OF 69



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0127	1	IC,BCM5231,FAST ENET XCVR,64P,TQFP	U37	CRITICAL	ENET_BCM5231

ETHERNET PHY

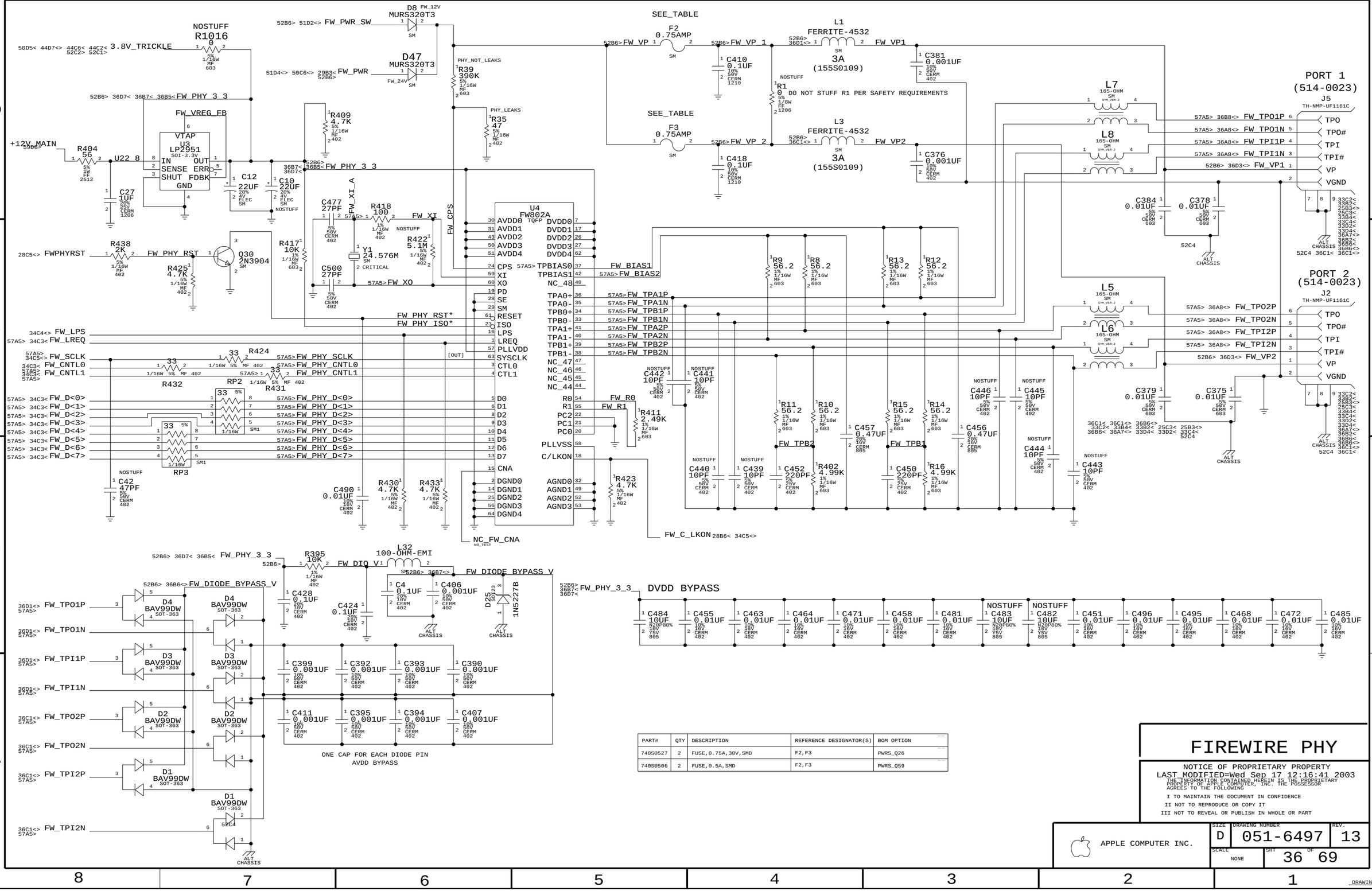
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6497	13

SCALE	SHT OF
NONE	35 OF 69

DRAWING

<XR_PAGE_TITLE>



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
740S0527	2	FUSE,0.75A,30V,SMD	F2,F3	PWRS_Q26
740S0506	2	FUSE,0.5A,SMD	F2,F3	PWRS_Q59

FIREWIRE PHY

LAST MODIFIED=Wed Sep 17 12:16:41 2003

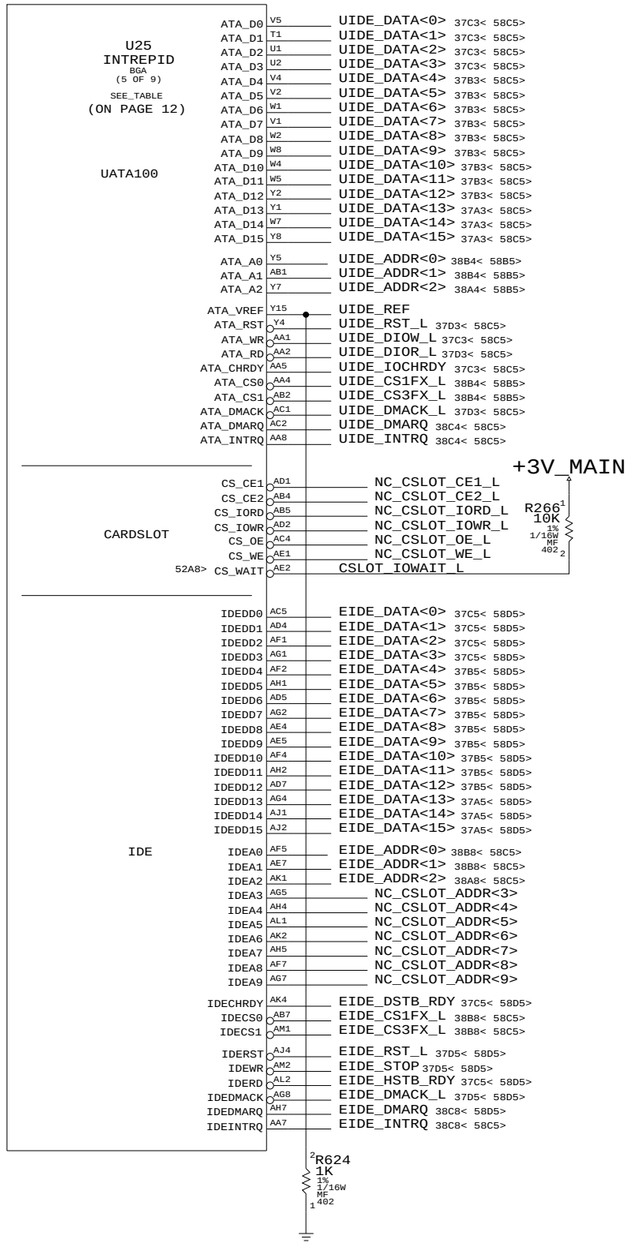
APPLE COMPUTER INC.

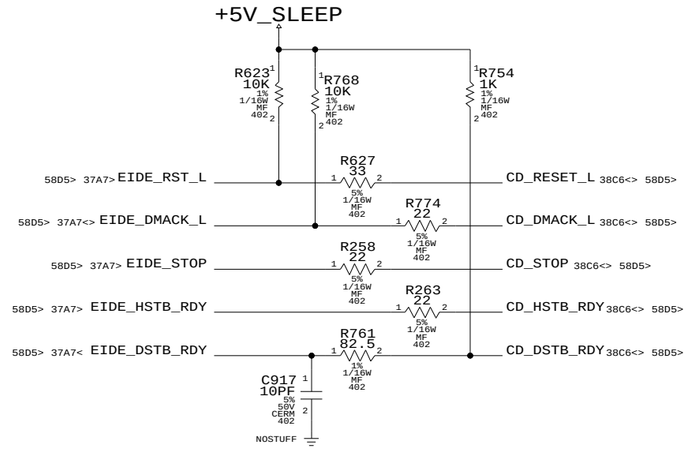
SIZE	DRAWING NUMBER	REV.
D	051-6497	13

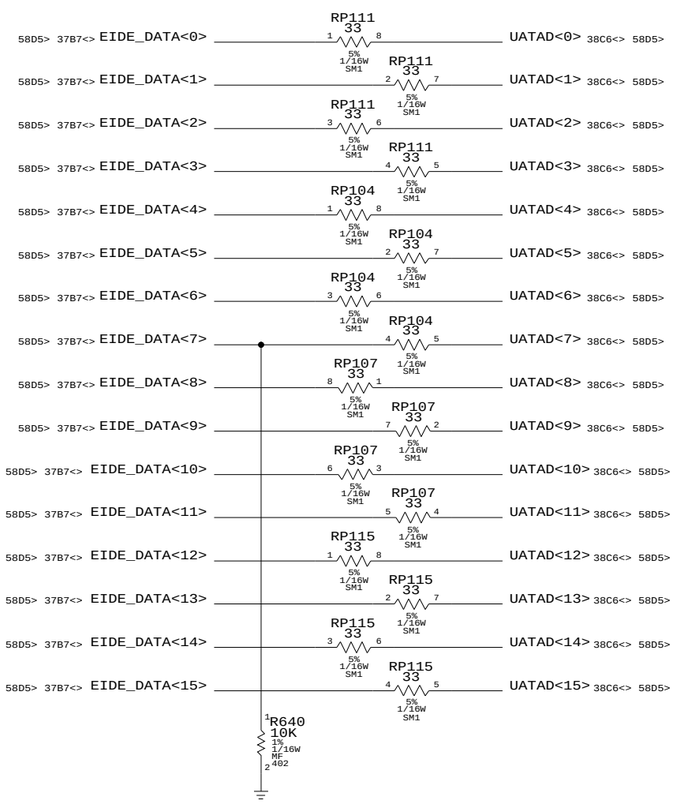
SCALE: NONE

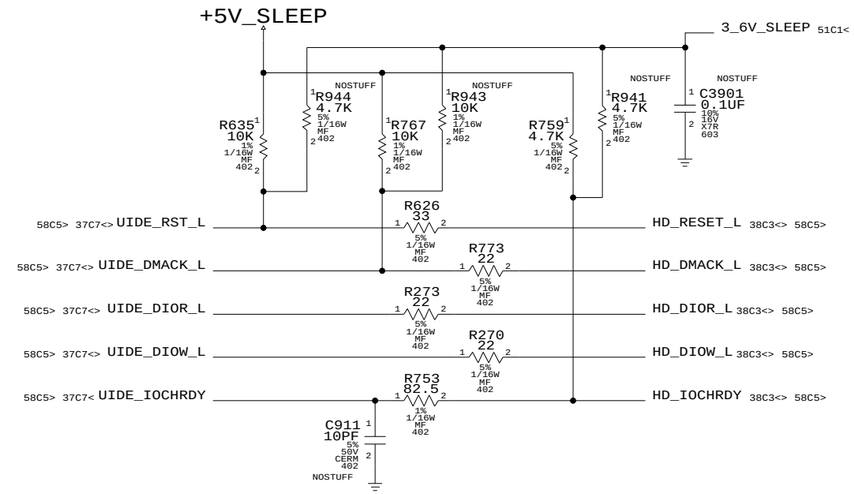
SHT 36 OF 69

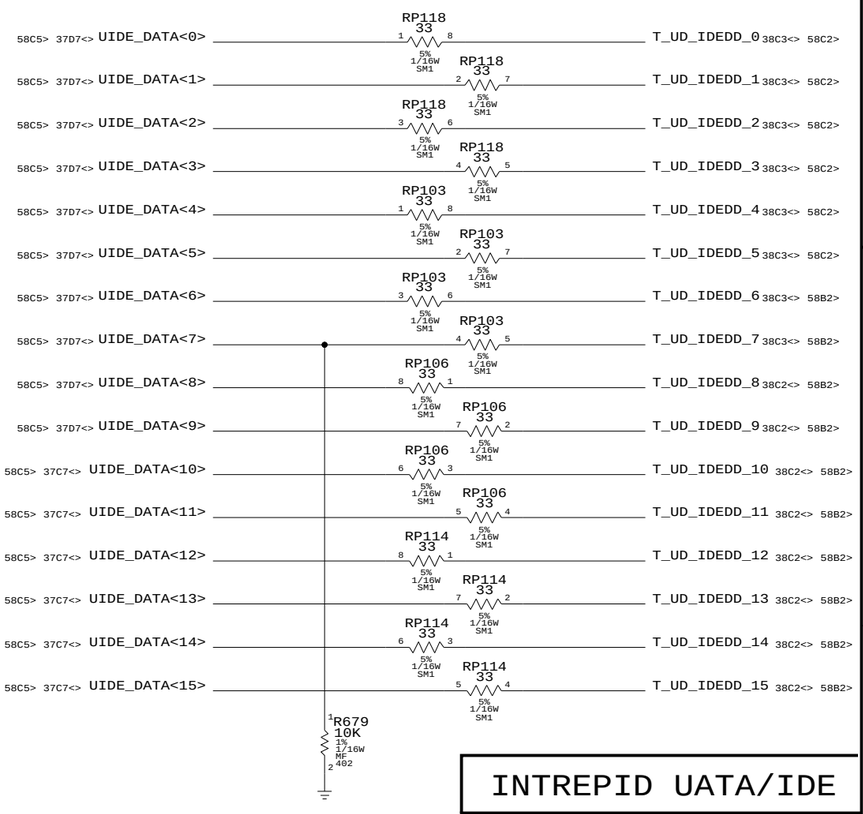
DRAWING











INTREPID UATA/IDE

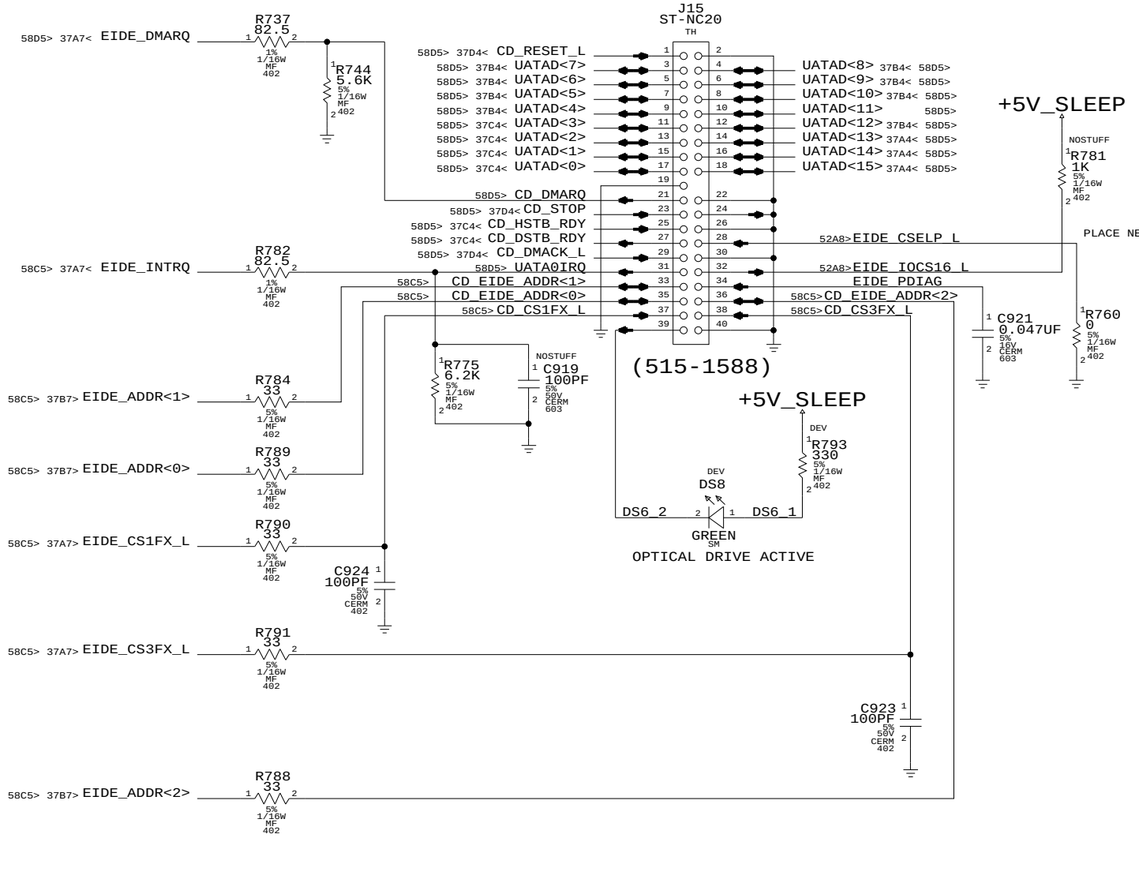
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6497	13
SCALE: NONE	SHT 37 OF 69	

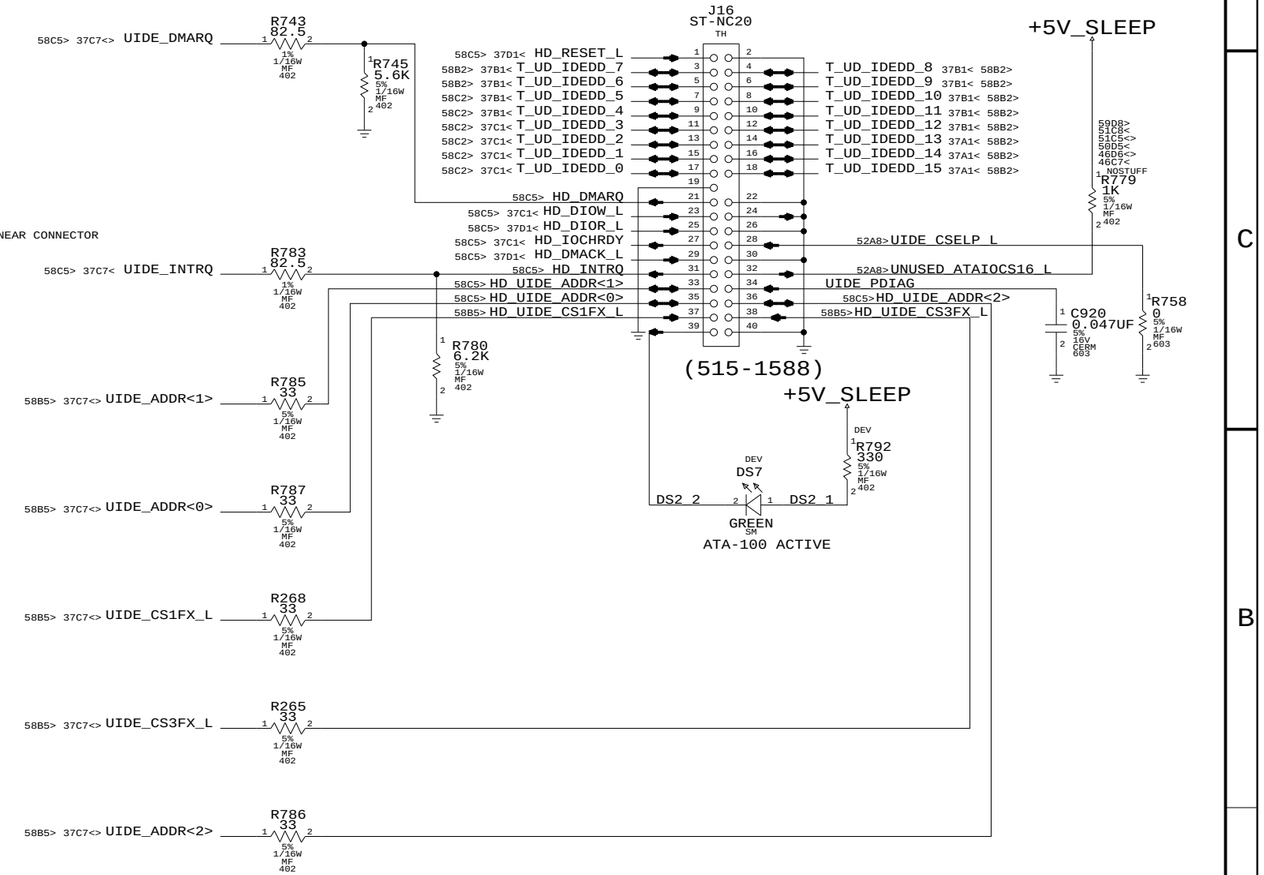
DRAWING

<XR_PAGE_TITLE>

OPTICAL DRIVE INTERFACE



ATA-100 INTERFACE

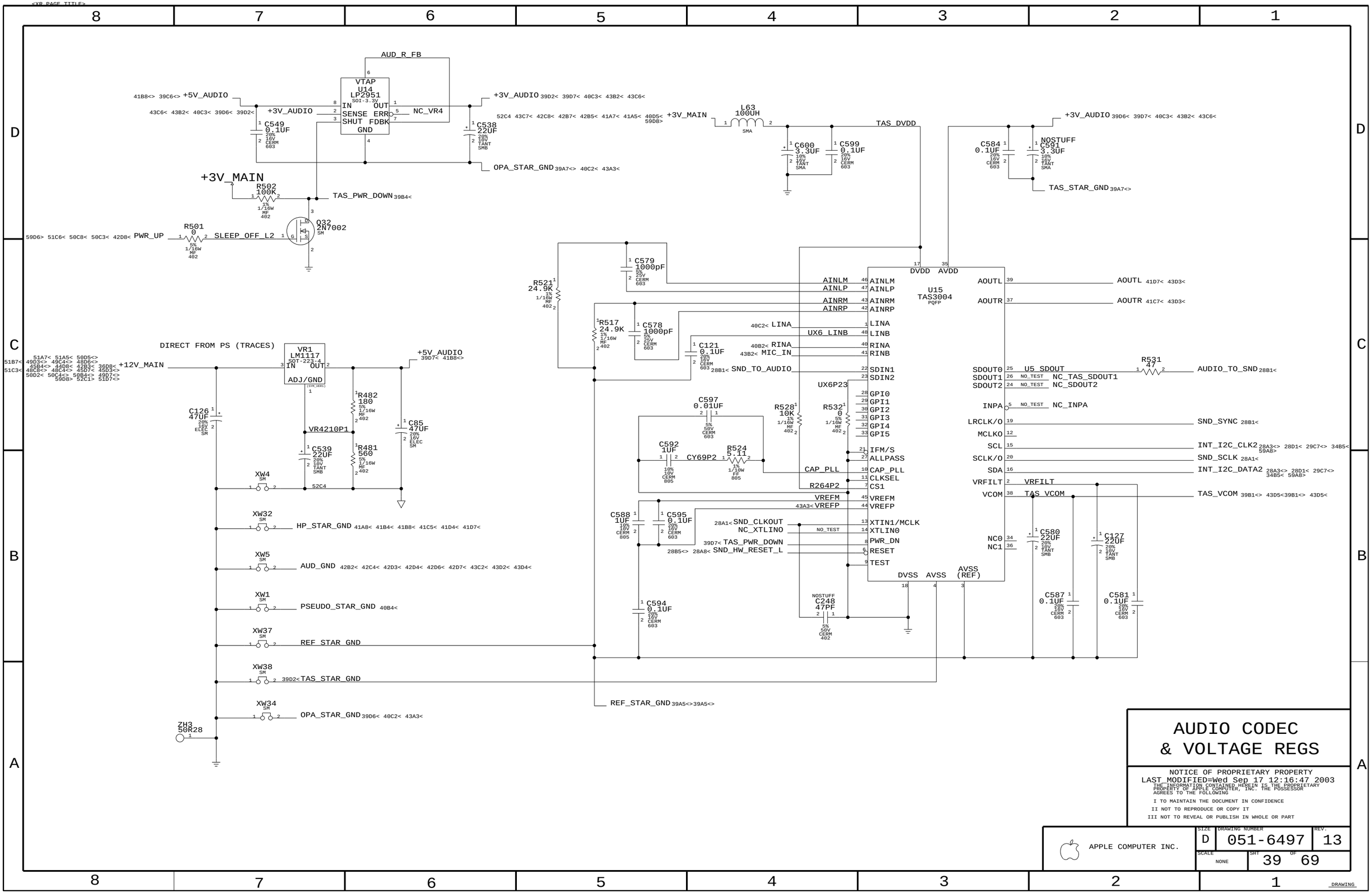


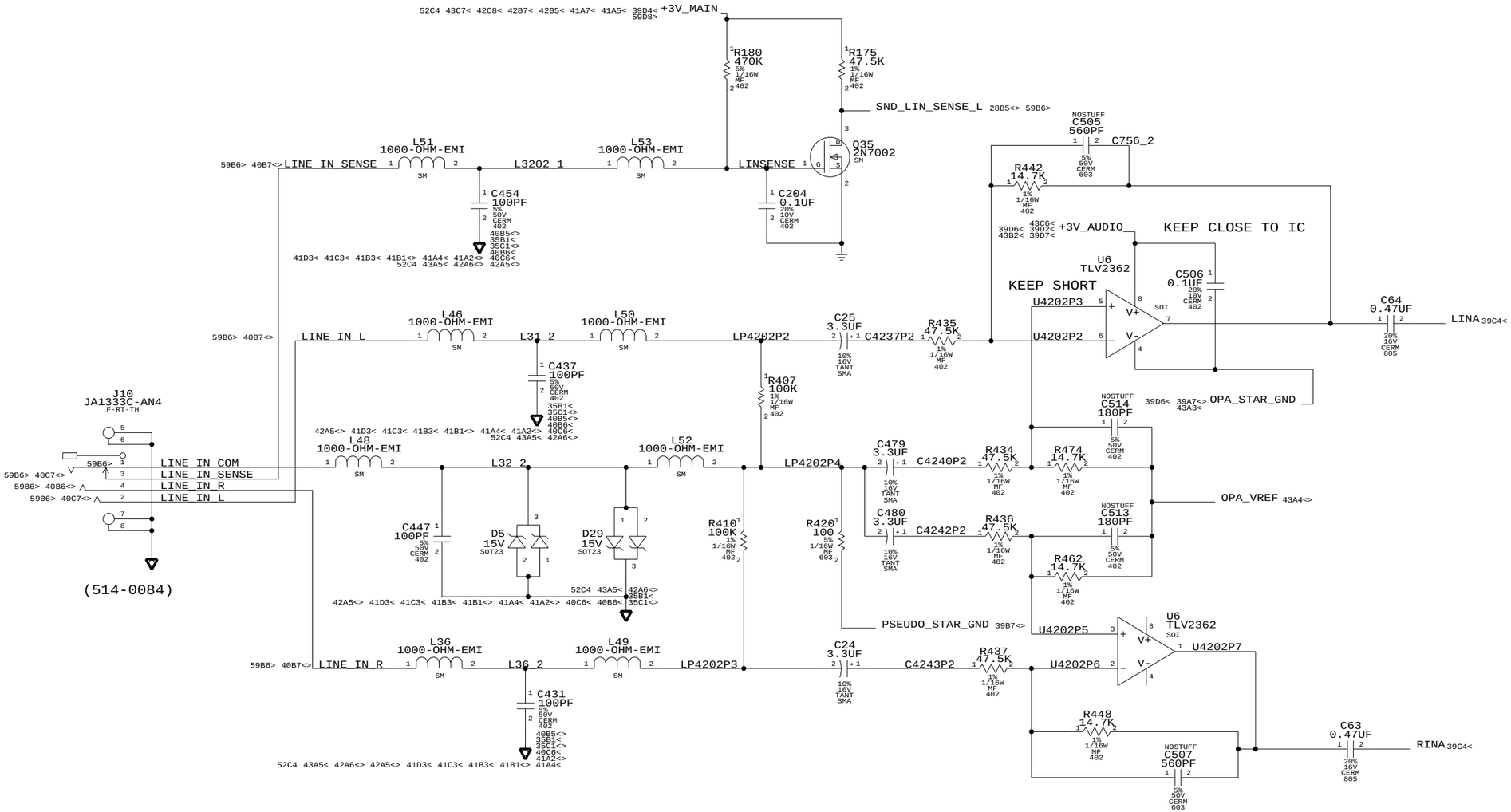
CD/HD CONS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6497	13
SCALE: NONE	SHT 38 OF 69	

DRAWING


AUD_R_FB
VTAP
U14
LP2951
SOI-3.3V
IN
OUT
SENSE
ERR
SHUT
FDBK
GND
NC_VR4
41B8<> 39C6<> +5V_AUDIO
43C6< 43B2< 40C3< 39D6< 39D2<
+3V_AUDIO
C549 0.1UF
C538 22UF
+3V_AUDIO 39D2< 39D7< 40C3< 43B2< 43C6<
52C4 43C7< 42C8< 42B7< 42B5< 41A7< 41A5< 40D5< 59D8>
OPA_STAR_GND 39A7<> 40C2< 43A3<
+3V_MAIN
R502 100K
TAS_PWR_DOWN 39B4<
Q32 2N7002 SM
R501 0
59D6> 51C6< 50C8< 50C3< 42D8< PWR_UP
SLEEP_OFF_L2
L63 100UH SMA
+3V_MAIN
C600 3.3UF
C599 0.1UF
TAS_DVDD
+3V_AUDIO 39D6< 39D7< 40C3< 43B2< 43C6<
C584 0.1UF
NOSTUFF C591 3.3UF
TAS_STAR_GND 39A7<>
DIRECT FROM PS (TRACES)
VR1
LM1117
SOT-223-4
ADJ/GND
51B7< 51A7< 51A5< 50D5<>
49D3<> 49C4<> 48D6<>
45B4<> 44D8< 42B3< 36D8< +12V_MAIN
51C3< 48C8<> 48C4<> 45D7< 45D3<>
50D2< 50C4<> 50B4<> 49D7<>
59D8> 52C1> 51D7<>
+5V_AUDIO 39D7< 41B8<>
C126 47UF
R482 180
VR4210P1
C85 47UF
C539 22UF
R481 560
XW4 SM
52C4
XW32 SM
HP_STAR_GND 41A8< 41B4< 41B8< 41C5< 41D4< 41D7<
XW5 SM
AUD_GND 42B2< 42C4< 42D3< 42D4< 42D6< 42D7< 43C2< 43D2< 43D4<
XW1 SM
PSEUDO_STAR_GND 40B4<
XW37 SM
REF_STAR_GND
XW38 SM
39D2< TAS_STAR_GND
XW34 SM
OPA_STAR_GND 39D6< 40C2< 43A3<
ZH3
50R28
C579 1000pF
R521 24.9K
R517 24.9K
C578 1000pF
C121 0.1UF
SND_TO_AUDIO 28B1<
C597 0.01UF
C592 1UF
CY69P2
R524 5.11
R528 10K
R532 0
R264P2
C588 1UF
C595 0.1UF
C594 0.1UF
C248 47PF
NOSTUFF
U15
TAS3004
PQFP
DVDD
AVDD
DVSS
AVSS
AVSS (REF)
AINLM
AINLP
AINRM
AINRP
LINA
LINB
RINA
RINB
SDIN1
SDIN2
GPI0
GPI1
GPI2
GPI3
GPI4
GPI5
IFM/S
ALLPASS
CAP_PLL
CLKSEL
CS1
VREFM
VREFP
XTIN1/MCLK
XTLIN0
PWR_DN
RESET
TEST
40C2< LINA
UX6_LINB
40B2< RINA
43B2< MIC_IN
UX6P23
28A1< SND_CLKOUT
NC_XTLINO
NO_TEST
39D7< TAS_PWR_DOWN
28B5<> 28A8< SND_HW_RESET_L
AOUTL
AOUTR
SDOUT0
SDOUT1
SDOUT2
INPA
LRCLK/O
MCLKO
SCL
SCLK/O
SDA
VRFILT
VCOM
NC0
NC1
U5_SDOUT
NC_TAS_SDOUT1
NC_SDOUT2
NC_INPA
R531 47
AUDIO_TO_SND 28B1<
SND_SYNC 28B1<
INT_I2C_CLK2 28A3<> 28D1< 29C7<> 34B5< 59A8>
SND_SCLK 28A1<
INT_I2C_DATA2 28A3<> 28D1< 29C7<> 34B5< 59A8>
VRFILT
TAS_VCOM 39B1<> 43D5<39B1<> 43D5<
C500 22UF
C587 0.1UF
C127 22UF
C581 0.1UF
REF_STAR_GND 39A5<>39A5<>
AUDIO CODEC
& VOLTAGE REGS
NOTICE OF PROPRIETARY PROPERTY
LAST_MODIFIED=Wed Sep 17 12:16:47 2003
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-6497
REV. 13
SCALE NONE
SHT 39 OF 69
DRAWING



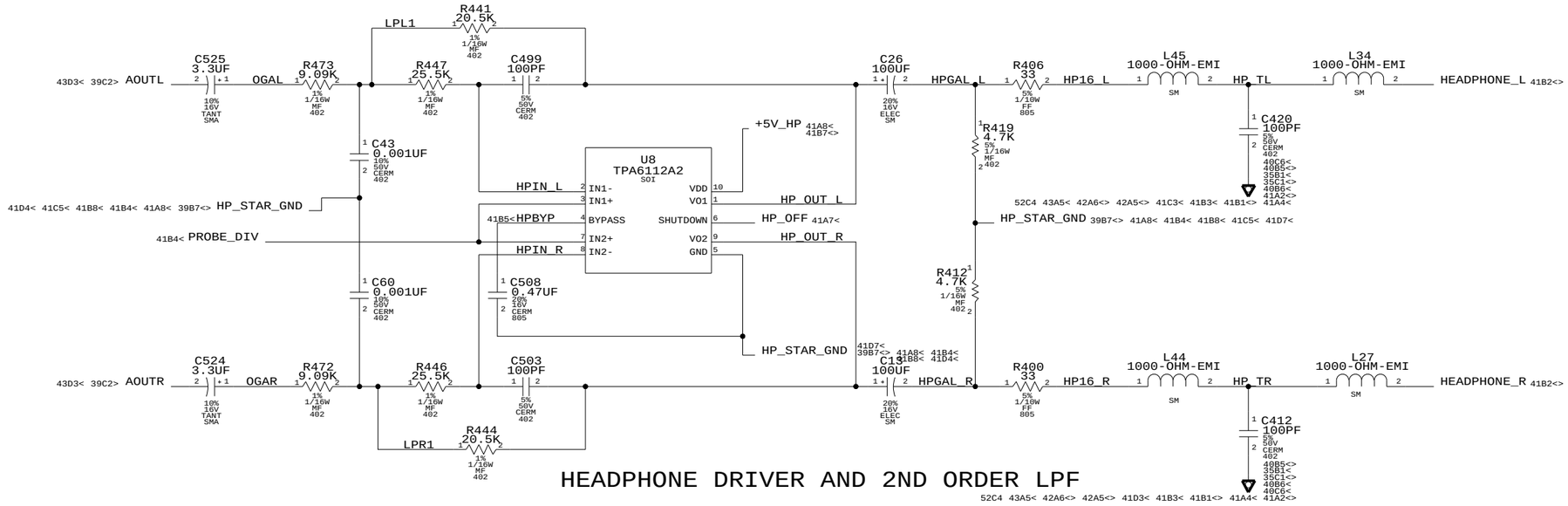
LINE IN BUFFER

APPLE COMPUTER INC.

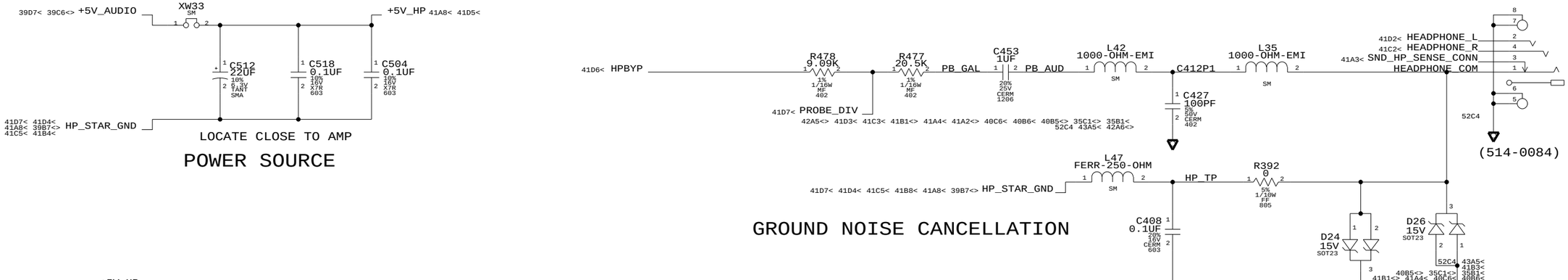
SIZE	DRAWING NUMBER	REV.
D	051-6497	13

SCALE	SHT	OF
NONE	40	69

DRAWING

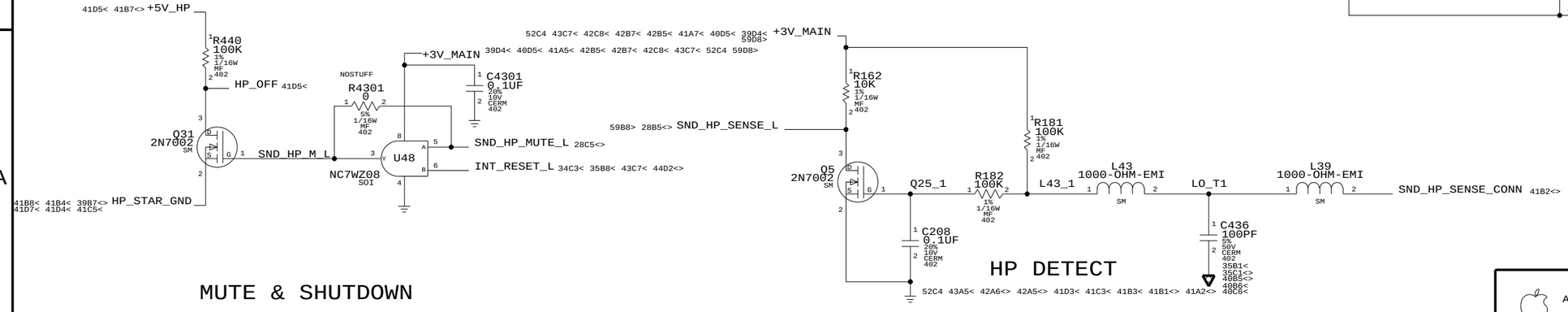


HEADPHONE DRIVER AND 2ND ORDER LPF



POWER SOURCE

GROUND NOISE CANCELLATION



MUTE & SHUTDOWN

HP DETECT

HEADPHONE OUT AMP

LAST MODIFIED=Wed Sep 17 12:16:50 2003

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6497	13

SCALE	SHT	OF
NONE	41	69

DRAWING

<XR_PAGE_TITLE>

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
155S0148	4	FILTR,EMI,160OHM,6A,1206	L90,L91,L93,L96	

TPA_5V IS NOT USED IN THIS SCHEMATIC

SPEAKER AMP

NOTICE OF PROPRIETARY PROPERTY
LAST MODIFIED=Wed Sep 17 12:16:53 2003
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6497	13
SCALE: NONE	SHT 42 OF 69	

DRAWING

L97
TB321611B130
42A6<> INT_SPKR+ 1 1206 2 KS_INT_SPKR+ 29A3< 58A5> 59B8>

L98
TB321611B130
42A6<> INT_SPKR- 1 1206 2 KS_INT_SPKR- 29A3< 42B4< 58A5> 59B8>

R4401
0
NOSTUFF 1/16W 5% MF 402
+3V_MAIN 39D4< 40D5< 41A5< 41A7< 42B5< 42B7< 42C8< 52C4 59D8>
28C5<> SND_AMP_MUTE_L
44D2<> 41A7< 35B8< 34C3< INT_RESET_L
U48 NC7WZ08 SOI
SND_AMP_M_L 42D3<

C1076 1UF 10% 10V CERM 805
R986 200 5% 1/16W MF 402
VCOML AUDIO
LINP 42C5<
NET_PHYSICAL_TYPE=AUDIO
C1078 0.047UF 10% 16V CERM 402
39B1<> TAS_VCOM
NET_PHYSICAL_TYPE=AUDIO
AUD_GND 39B7<> 42B2< 42C4< 42D3< 42D4< 42D6< 42D7< 43C2< 43D2<
C1079 0.047UF 10% 16V CERM 402
C1077 1UF 10% 10V CERM 805
R987 200 5% 1/16W MF 402
VCOMR AUDIO
RINP 42C4<
NET_PHYSICAL_TYPE=AUDIO

41D7< 39C2> AOUTL
C1088 1UF 10% 16V CERM 805
R989 200 5% 1/16W MF 402
LINN1
LINN 42C5<
C1095 0.047UF 10% 16V CERM 402
AUD_GND 39B7<> 42B2< 42C4< 42D3< 42D4< 42D6< 42D7< 43C2< 43D4<
41C7< 39C2> AOUTR
C1087 1UF 10% 10V CERM 805
R988 200 5% 1/16W MF 402
RINN1
RINN 42C4<
C1094 0.047UF 10% 16V CERM 402
AUD_GND 39B7<> 42B2< 42C4< 42D3< 42D4< 42D6< 42D7< 43D2< 43D4<

R4507 330 1/16W 5% MF 402
43B2< 40C3< 39D7< 39D6< 39D2< +3V_AUDIO
MIC_FIX

518S0008

J4501 DF13B-4P-1.25V F-ST-SM NOSTUFF
J4502 DF13B-4P-1.25V F-ST-SM NOSTUFF
43A6<> M1S
43B6<> M1H
43A6<> M1L

NEEDED FOR MIC NOISE
C4502 22UF 20% 10V TANT SMB
R421 2.2K 5% 1/16W MF 402

C542 100PF 5% 50V CERM 402
C556 0.1UF 20% 16V CERM 603
MIC_IN 39C4<
+3V_AUDIO 39D2< 39D6< 39D7< 40C3< 43C6<

L79 1000-OHM-EMI SM
59A8> 58A5> 29A5<> MICHIGH M1FH
C642 47PF 5% 50V CERM 402
24B3< 29A3< 52C4 43A7<
R4501 0 5% 1/16W MF 402
43B6<> JAZ NO_TEST
R4504 0 5% 1/16W MF 402
M1H
L60 1000-OHM-EMI SM
M1HFILT
R414 330 5% 1/16W MF 402
MIC1
C35 2.2UF 20% 10V CERM 805
MIC2
R488 2.2K 5% 1/16W MF 402
MIC3
R489 121K 1% 1/16W MF 402
MIC4
C478 470PF 10% 50V CERM 402
R413 47.5K 1% 1/16W MF 402

L81 1000-OHM-EMI SM
59A8> 58A5> 29A5<> MICLOW M1FL
C675 47PF 5% 50V CERM 402
24B3< 29A3< 52C4 43B7<
R4502 0 5% 1/16W MF 402
43B6<> ASH NO_TEST
R4505 0 5% 1/16W MF 402
M1L
L59 1000-OHM-EMI SM

U13 TLV2362 SOI
U13 TLV2362 SOI
39B4< VREFP
Q33 2N3904 SM
MIC5
C551 0.1UF 20% 16V CERM 603
C550 1UF 10% 10V X5R 603
R498 47.5K 1% 1/16W MF 402
40B3< OPA_VREF
39D6< 39A7<> 40C2< OPA_STAR_GND

L83 1000-OHM-EMI SM
59A8> 58A5> 29A5<> MICSHLD MIC1S1
R4503 0 5% 1/16W MF 402
43B6<> KAVAN NO_TEST
R4506 0 5% 1/16W MF 402
M1S
52C4 42A6<> 42A5<> 41D3< 41C3< 41B3< 41B1<> 41A4< 41A2<> 40C6< 40B6< 40B5<> 35B1< 35C1<>
R487 0 5% 1/16W MF 402

PLACE R4501, R4502 AND R4503 NEAR AUDIO
PLACE R4504, R4505 AND R4506 NEAR KITCHENSINK

MIC PREAMP

LAST MODIFIED=Wed Sep 17 12:16:55 2003

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6497	13
SCALE: NONE	SHT 43 OF 69	

DRAWING

<XR_PAGE_TITLE>

PMU SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S1008	1	PMU,M16C62,64KB,PRMGD	U26		
525-0057	1	CONN,BATTERY HOLDER	BT1		

AGP_RESET_L IS USED AS MAIN_RESET_L FOR SIL1162
THROUGH R1027 AND IS NOT USED IN ANY OTHER DEVICE

IIC BUS PULLUPS

PMU NOT RATED STRONG ENOUGH FOR 1K
MAIN RAIL, TO PREVENT LEAKAGE INTO UNPOWERED DEVICES

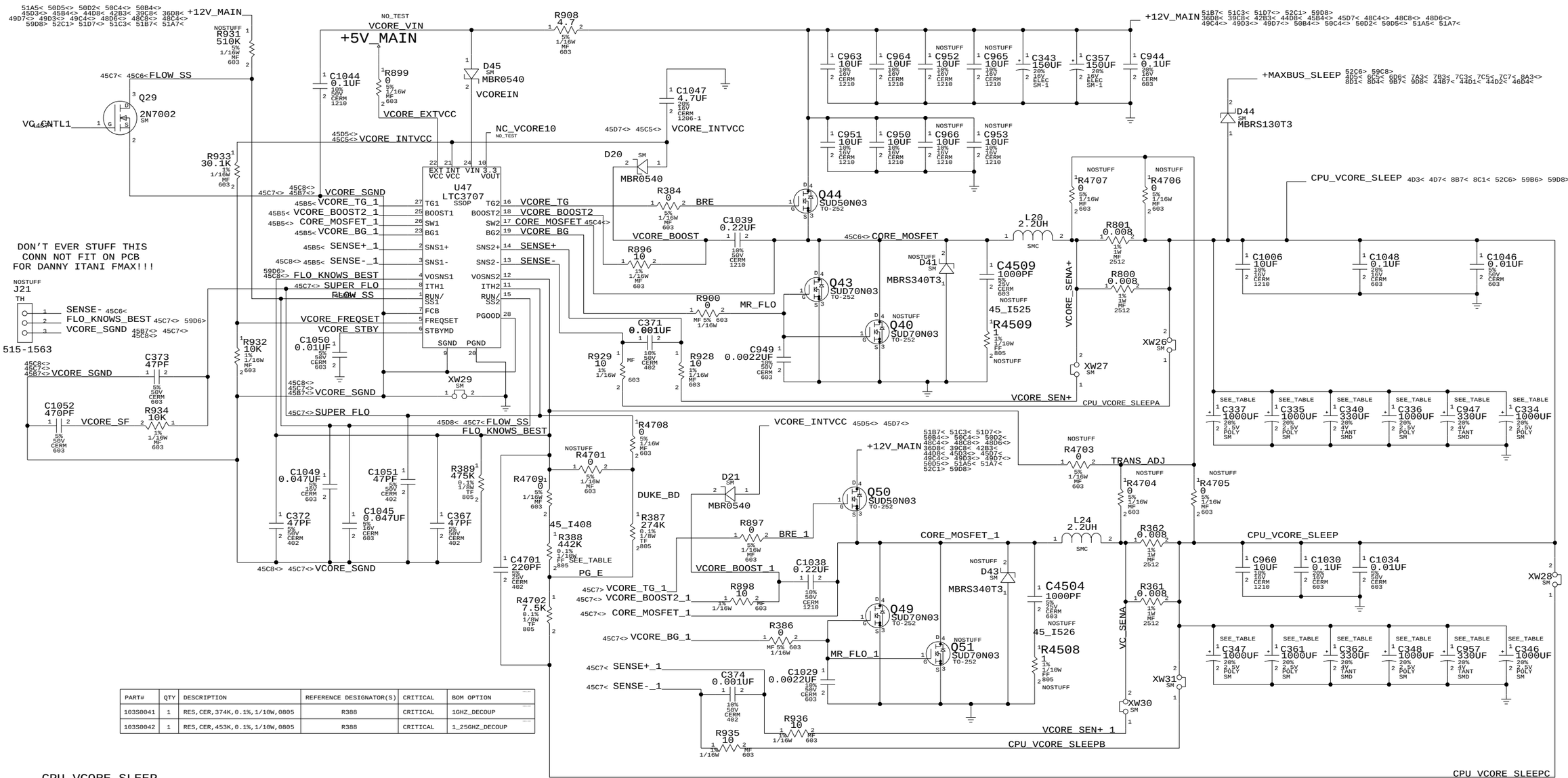
LOCATE NEAR TO PMU

PMU POWER MGR

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6497	13
SCALE: NONE	SHT 44 OF 69	

DRAWING



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
103S0041	1	RES,CER,374K,0.1%,1/10W,0805	R388	CRITICAL	1GHZ_DECOUP
103S0042	1	RES,CER,453K,0.1%,1/10W,0805	R388	CRITICAL	1_25GHZ_DECOUP

CPU_VCORE_SLEEP
1.0GHZ,1.5V+30/-130MV,35W
1.25GHZ,1.57V+70/-70MV,35W

KUMA SERVER(1):HARDWARE:KUMA DESIGNS:KUMA POWER SUPPLIES:VCORE WITH AVP TABLES

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
128S0012	4	CAP,TANT,POLY,330UF,4.0V,D4	C340,C947,C362,C957	1_25GHZ_DECOUP
128S0410	8	CAP,TANT,POLY,1000UF,2.5V,D4	C337,C335,C336,C334,C347,C361,C348,C346	1_25GHZ_DECOUP
128S0022	12	CAP,EL,POLY,220UF,20%,2V	C337,C335,C336,C334,C347,C361,C348,C346,C340,C947,C362,C957	1GHZ_DECOUP

CPU & AGP VREGS

LAST_MODIFIED=Wed Sep 17 12:17:00 2003

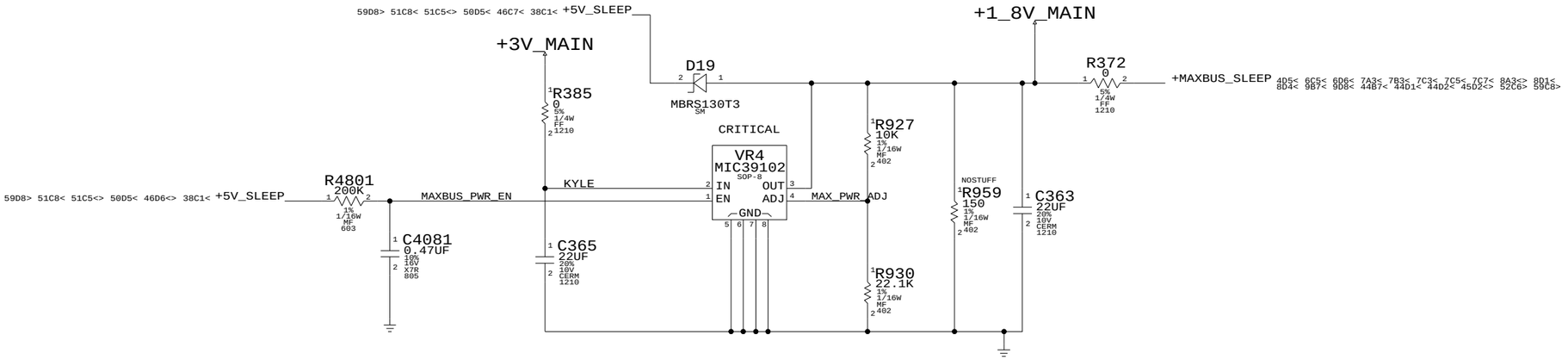
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6497	13
SCALE: NONE	SHT 45 OF 69	

INTREPID MAXBUS & CPU OVDD POWER CONVERTER

(OFF DURING SLEEP)

+MAXBUS_SLEEP 1.8V,+/-2%,.606W

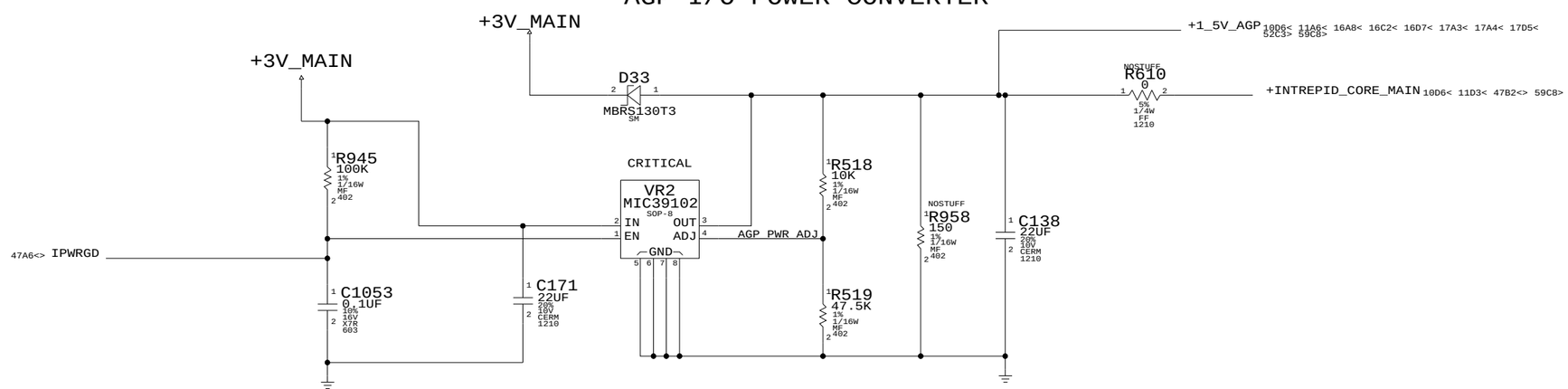


MAXBUS I/O SUPPLY SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S4754	1	RES,FF,47.5K-OHM,1%	R930		MAXIO_1'50V
114S3014	1	RES,FF,30.1K-OHM,1%	R930		MAXIO_1'65V
114S2674	1	RES,FF,26.7K-OHM,1%	R930		MAXIO_1'70V
114S2214	1	RES,FF,22.1K-OHM,1%	R930		MAXIO_1'80V *

+1_5V_AGP 1.5V,+/-5%,.6W

AGP I/O POWER CONVERTER



AGP I/O SUPPLY SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S4754	1	RES,FF,47.5K-OHM,1%	R519		AGPIO_1'50V *
114S3014	1	RES,FF,30.1K-OHM,1%	R519		AGPIO_1'65V
114S2674	1	RES,FF,26.7K-OHM,1%	R519		AGPIO_1'70V
114S2214	1	RES,FF,22.1K-OHM,1%	R519		AGPIO_1'80V

CPU & AGP VREGS

LAST_MODIFIED=Wed Sep 17 12:17:01 2003

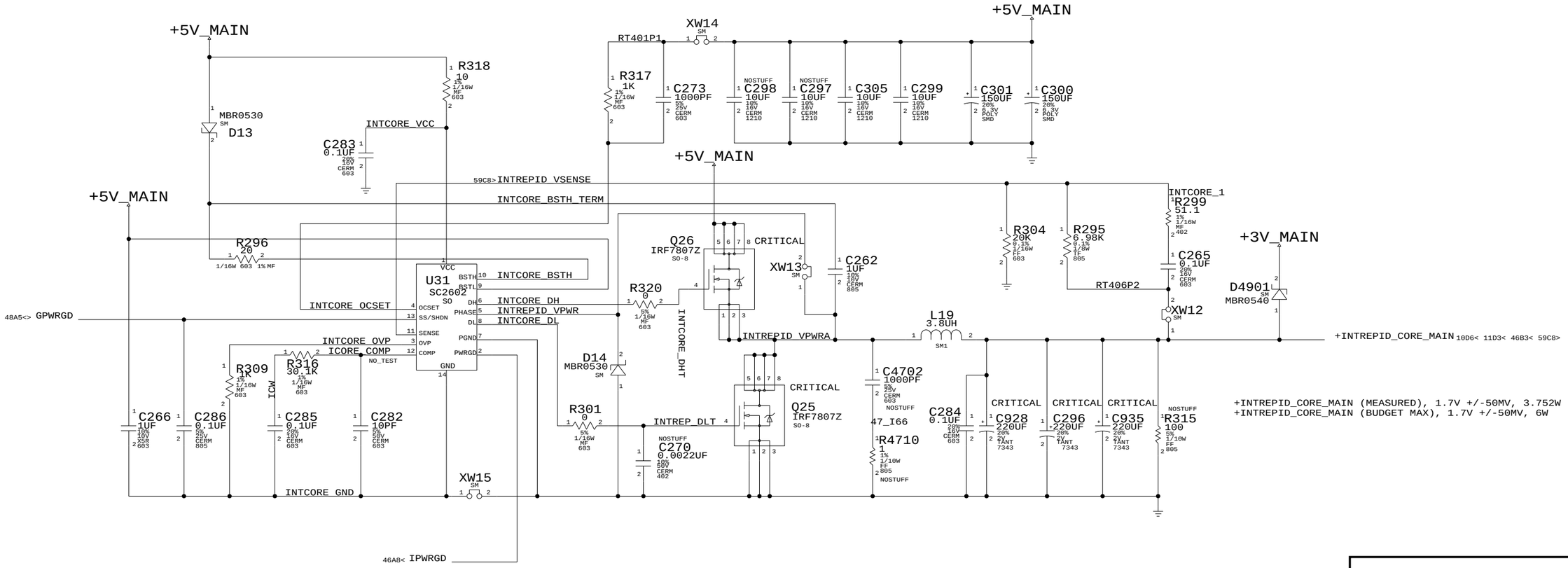
APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6497 | REV. 13

SCALE NONE | SHT 46 OF 69

DRAWING

<XR_PAGE_TITLE>



TABLES FOR INTREPID CORE RESISTOR VALUES TO VOLTAGES ARE LOCATED AT
KUMA SERVER(1):HARDWARE:KUMA DESIGNS;KUMA POWER SUPPLIES;ICORE R TOLERANCE

INTREPID CORE

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6497	13

SCALE	SHT	OF
NONE	47	69

DRAWING

<XR_PAGE_TITLE>

GRAPH_CORE (NV18B), 1.6V +/-100MV, 12W
GRAPH_CORE (NV34), 1.45V +/-100MV, 16W

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
110S5233	1	RES,5.23K OHMS,1%,1/16W,0603	R499	NV18B
110S2943	1	RES,2.94K OHMS,1%,1/16W,0603	R499	NV34

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
128S0410	3	CAP,TANT,POLY,1000UF,2.5V,D4	C106,C132,C88	1_25GHZ_DECOUP
128S0410	3	CAP,TANT,POLY,1000UF,2.5V,D4	C106,C132,C88	1GHZ_DECOUP

GRAPHICS CORE

LAST_MODIFIED=Wed Sep 17 12:17:04 2003

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6497	13
SCALE: NONE	SHT 48 OF 69	

DRAWING

<XR_PAGE_TITLE>

MAIN MEMORY DDR AND FRAME BUFFER POWER CONVERTER (2.50VDC)

+12V_MAIN

R888 10 1% 1/16W MF 603

25V_VCC

C1019 0.1UF 20% 16V CERM 603

MBR0530 SM D18

XW25 SM

RB227P1

R884 1K 1% 1/16W MF 603

C1005 470PF 10% 50V CERM 402

C959 10UF 10% 16V CERM 1210

C968 10UF 10% 16V CERM 1210

C975 10UF 10% 16V CERM 1210

C989 10UF 10% 16V CERM 1210

NOSTUFF C342 150UF 20% 16V ELEC SM-1

C351 150UF 20% 16V ELEC SM-1

25V_OCSET

25V_BSTH_TERM

25V_VSENSE NO_TEST

49B5<> 25V_VPWR

R369 20 1% 1/16W MF 603

25V_BSTH

U45 SC2602 SO

VCC BSTH BSTL DH PHASE DL PGND PWRGD GND OCSET SS/SHDN SENSE OVP COMP

25V_DH

25V_VPWR 49C4<>

25V_DL

R873 0 5% 1/16W MF 603

25V_DHT

Q28 SUD50N03 TO-252

25V_VPWRA

XW24 SM

C358 0.1UF 20% 25V CERM 603

R880 20K 1% 1/16W MF 603

R871 22.1K 1% 1/16W MF 603

R872 51.1 1% 1/16W MF 402

25_CORE_1 NO_TEST

C962 0.1UF 20% 16V CERM 603

RB213P2

XW23 SM

+2_5V_MAIN

L21 4.0UH SM1

D46 SM MBRS130T3

+3V_MAIN

50A6> 49B7<50A6> 49B7< PGOOD

PGOOD

R883 4.75K 1% 1/16W MF 603

25V_OVP

25V_COMP

NO_TEST

25V_COMP_DWN

D42 SM MBR0530

R827 0 5% 1/16W MF 603

25V_DLT

Q27 SUD70N03 TO-252

C4901 1000PF 5% 25V CERM 603

NOSTUFF D15 SM MBRS340T3

49_I70

R4901 1 1% 1/10W FF 805

NOSTUFF

C1015 0.1UF 20% 25V CERM 805

C359 0.1UF 20% 16V CERM 603

R371 1K 1% 1/16W MF 603

C1004 0.1UF 20% 16V CERM 603

C1000 10PF 5% 50V CERM 603

NOSTUFF C948 0.0022UF 10% 50V CERM 402

XW41 SM

25V_GND

MPWRGD 48B7<

C218 330UF 20% 6.3V POLY SMD

C330 330UF 20% 6.3V POLY SMD

NOSTUFF C323 330UF 20% 6.3V POLY SMD

C332 330UF 20% 6.3V POLY SMD

R334 100 5% 1/10W FF 805

NOSTUFF C329 0.1UF 20% 16V CERM 603

NOSTUFF C324 330UF 20% 6.3V POLY SMD

C235 330UF 20% 6.3V POLY SMD

C331 330UF 20% 6.3V POLY SMD

+2_5V_MAIN, 1.61V +/-50MV, 12.908W

MEMORY PS

APPLE COMPUTER INC.

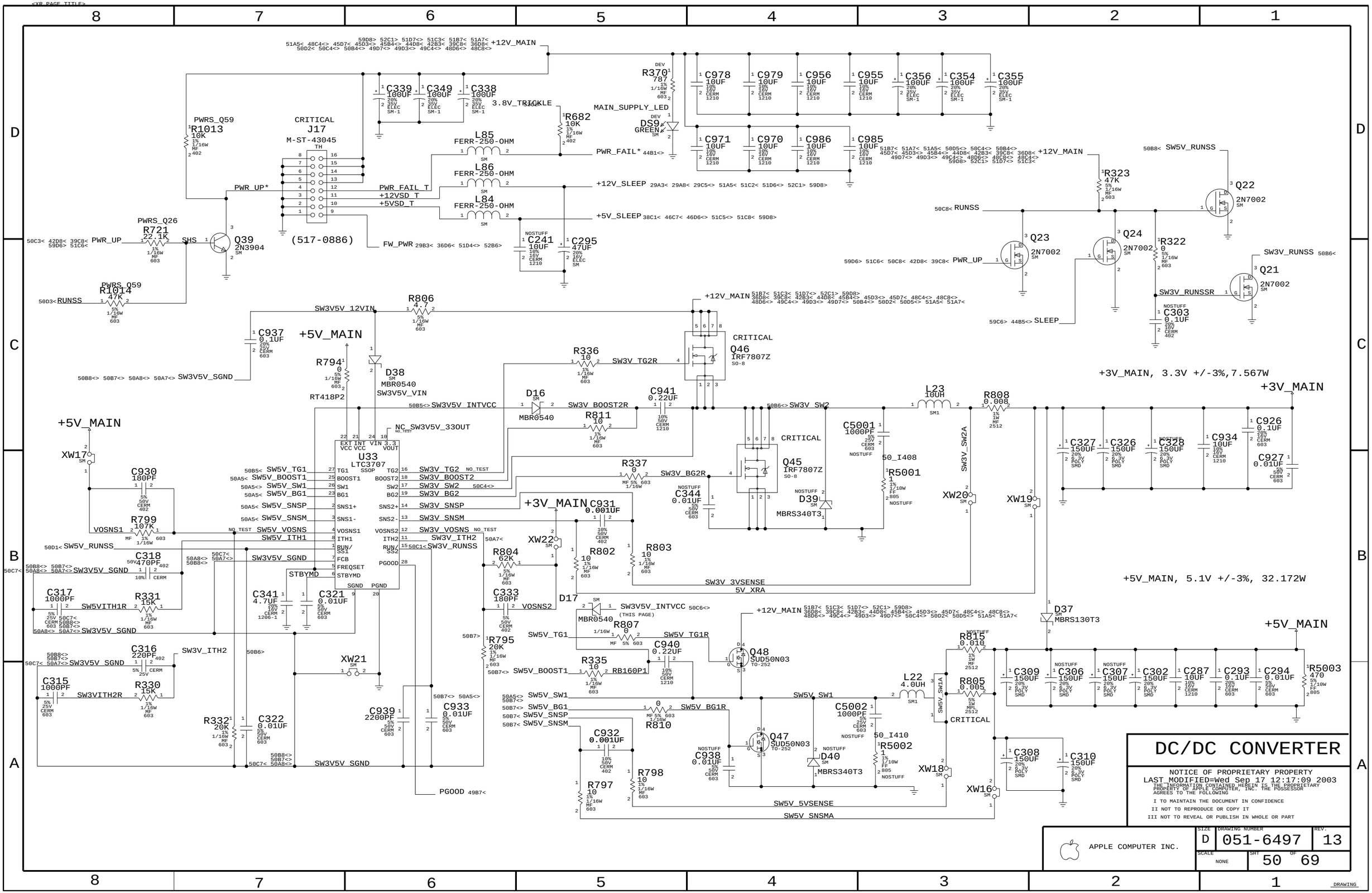
SIZE	DRAWING NUMBER	REV.
D	051-6497	13

SCALE NONE

SHT 49 OF 69

DRAWING

<XR_PAGE_TITLE>



DC/DC CONVERTER

NOTICE OF PROPRIETARY PROPERTY

LAST_MODIFIED=Wed Sep 17 12:17:09 2003

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6497	13

SCALE	SHT	OF
NONE	50	69

DRAWING

<XR_PAGE_TITLE>

+12V MAIN POWER SWITCH
(OFF DURING SLEEP)

50B4<> 49D7<> 49D3<> 49C4<> 51B7< 45B4<> 44D8< 42B3< 39C8< 36D8< 48D6<> 48C8<> 48C4<> 45D7< 45D3<> 51A7< 51A5< 50D5<> 50D2< 50C4<> 59D8> 52C1> 51C3< +12V_MAIN

R769 470K 5% 1/16W MF 402

Q20 FDC602P SOT-6

+12V_SLEEP 29A3< 29A8< 29C5<> 50D5< 51A5< 51C2< 52C1> 59D8>

C269 47UF 20% 16V ELEC SM

C915 0.01UF CERM 10% 16V 402

SW12V_SLEEP

C918 0.0022UF 10% 50V CERM 402

R770 100K 1% 1/16W MF 402

SW12V_SL

51B6< SLEEP_OFF_L

Q14 2N7002 SM

R739 0 5% 1/16W MF 402

PWR_UP 39C8< 42D8< 50C3< 50C8< 59D6>

+5V POWER SWITCH
(OFF DURING SLEEP)

+5V_MAIN

Q37 FDC602P SOT-6

+5V_SLEEP 38C1< 46C7< 46D6<> 50D5< 51C8< 59D8>

C742 0.01UF CERM 10% 16V 402

SWITCH5V_4

C773 0.0022UF 10% 50V CERM 402

C238 150UF 20% 6.3V POLY SMD

R645 470K 5% 1/16W MF 402

R664 100K 1% 1/16W MF 402

SWITCH5V_3

R685 0 5% 1/16W MF 402

51C7< SLEEP_OFF_L

Q38 2N7002 SM

46D6<> 46C7< 38C1< +5V_SLEEP 59D8> 51C5<> 50D5<

R300 330 5% 1/16W MF 402

RUNLED1

DS5 GREEN SM

+5V POWER LED

FIREWIRE POWER SWITCH
EVALUATE CIRCUIT FOR SURGE PROTECTION FOR Q59C

FW_12V U35 SI4435DY SOI

52B6> 50C6<> 36D6< 29B3< FW_PWR

FW_PWR_SW 36D6< 52B6>

C19 47UF 20% 25V ELEC SM

C18 0.01UF CERM 5% 50V 603

C473 0.0022UF 10% 50V CERM 402

Q42P4

R23 470K 5% 1/10W MF 603

R21 100K 5% 1/16W MF 603

+5V_MAIN

R22 10K 1% 1/16W MF 603

Q1P3

Q1P1

Q1 2N7002 SM

TMDS POWER CONVERTER & SWITCH
(OFF DURING SLEEP)

VOLTAGE TO SUPPORT 3.3V AT PANEL
VOLTAGE HERE WILL EXCEED 3.3V

+3.3VFPD (3_6V_SLEEP), 3.6V +/-50MV, 3.32W

59D8> 52C1> 51D7<> 51B7< 51A7< 51A5< 48C8<> 48C4<> 45D7< 45D3<> 45B4<> 44D8< 42B3< 39C8< 36D8< 50D5<> 50D2< 50C4<> 50B4<> 49D7<> 49D3<> 49C4<> 48D6<> +12V_MAIN

FPD_12VM R1017 0 5% 1/8W FF 1206

+12V_SLEEP 29A3< 29A8< 29C5<> 50D5< 51A5< 51D6<> 52C1> 59D8>

FPD_12VS R1018 0 5% 1/8W FF 1206

FPD_3V3&FPD_12VM Q11 FDC602P SOT-6

+3.3VFPD 24D7< 52B6>

R5301 0 5% 1/16W MF 402 NOSTUFF

3_6V_SLEEP 37D1<

C254 10UF 10% 16V CERM 1210

+5V_MAIN

3_5 HONKER

+5V_MAIN

FPD_3V3

SENSE VR3 EZ1582 SM

VPWR VOUT VCTRL VOUT ADJ TAB

52C4 51B4<> 59D8>

59D8> 52C4 51B4<>

R251 102 1% 1/16W MF 402

HONK_ADJ

C246 150UF 20% 6.3V POLY SMD

FPD_3V3&FPD_12VM C257 0.01UF 402 10% 16V CERM

SWITCH5V_6

FPD_3V3&FPD_12VM C252 0.0022UF 10% 50V CERM 402

R278 100K 1% 1/16W MF 402 FPD_3V3&FPD_12VM

R277 10K 1% 1/16W MF 402 FPD_3V3&FPD_12VM

R279 10K 1% 1/16W MF 402

NOSTUFF C258 0.01UF 20% 16V CERM 402

TMDS_EN 23D7<>

FPD_12VS&FPD_12VM DZ1 1N5227B SOT23

FPD_3V3 C654 10UF 10% 16V CERM 1210

FPD_3V3 C653 10UF 10% 16V CERM 1210

FPD_3V3 C236 0.022UF 10% 50V CERM 805

FPD_3V3 R601 182 1% 1/16W MF 402

SWITCH5V_5

R1012 100K 1% 1/16W MF 402 SEE_TABLE

CHOC_BROWNIE

FPD_3V3&FPD_12VM R283 0 5% 1/16W MF 402

FPD_PWR_ON

FPD_PWR_ON_T

Q13 2N7002 SM

R284 100K 1% 1/16W MF 402 FPD_3V3&FPD_12VM

+5V POWER, SLEEP & TESTPOINT LEDS
(TESTPOINT LED IS USED TO FOR SERVICE AND
IF NOT ILLUMINATED, TELLS USER ITS OK TO ADD MEMORY)

50C4<> 50B4<> 49D7<> 49D3<> 52C1> 45D3<> 45B4<> 44D8< 42B3< 39C8< 36D8< 49C4<> 48D6<> 48C8<> 48C4<> 45D7< 51D7<> 51C3< 51B7< 51A5< 50D5<> 50D2< 59D8> +12V_MAIN

R740 10K 1% 1/16W MF 402

SLEEP2

R751 0 5% 1/16W MF 402

CPU_STATE_LED* SLEEP1

Q18 2N7002 SM

51C3< 51A7< 51A5< 50D5<> 49D3<> 49C4<> 48D6<> 45B4<> 44D8< 42B3< 39C8< 36D8< 48C8<> 48C4<> 45D7< 50D2< 50C4<> 50B4<> 49D7<> 59D8> 52C1> 51D7<> +12V_MAIN

R738 4.7K 5% 1/16W MF 402

59D6> 44C7<> POWER_UP*

Q16 2N7002 SM

Q15 2N7002 SM

CPU_SLEEPIN

LED_RET 29A3< 52B3>

Q17 2N7002 SM

R741 47.5K 1% 1/16W MF 402

+3V_MAIN

R302 330 5% 1/16W MF 402

SLEEPLED_TERM

DS6 GREEN SM

SLEEP_LED_BD

Q19 2N7002 SM

SLEEP LED

44D6<> BT1

TESTPOINT

NOSTUFF R615 0 5% 1/16W MF 402

R607 0 5% 1/16W MF 402

NOSTUFF R609 0 5% 1/16W MF 402

NOSTUFF R608 0 5% 1/16W MF 402

+5V_MAIN

+12V_MAIN

+12V_SLEEP

51B7< 51C3< 51D7<> 52C1> 59D8> 36D8< 39C8< 42B3< 44D8< 45B4<> 45D3<> 45D7< 48C4<> 48C8<> 48D6<> 49C4<> 49D3<> 49D7<> 50B4<> 50C4<> 50D2< 50D5<> 51A7<

RT373P1

R612 787 1% 1/16W MF 603

PWR_LED

NOSTUFF R614 470 5% 1/16W MF 402

BT1_LED

DS10 RED SM

JAZ1 A TH-TP50

GENERAL POWER LED
(NOT ILLUMINATED = OK TO ADD MEMORY)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S1005	1	RES,100K OHM,1%,1/16W,0402,SMD	R1012	FPD_12VM
116S1000	1	RES,0 OHM,5%,1/16W,0402,SMD	R1012	FPD_3V3

+5V/+12V, AUDIO FW & TMDS PWR

LAST_MODIFIED=Wed Sep 17 12:17:11 2003

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6497	13
SCALE: NONE	SHT 51 OF 69	

DRAWING

CPU POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
+MAXBUS_SLEEP	10	1.8	20
CPU_AVDD	10	1.85	20
CPU_VCORE_SLEEP	10	1.85	20

4D5< 6C5< 6D6< 7A3< 7B3< 7C3< 7C5< 7C7< 8A3<> 8D1< 8D4< 9B7< 9D8< 44B7<
4D1< 44D2< 45D2<> 46D4< 59C8>
4D3<
4D3< 4D7< 8B7< 8C1< 45D2<> 59B6> 59D8>

ETHERNET POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
ENET_AVDD	10	2.5	20

35D2<> 35D4<>

FIREWIRE POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
FW_DIO_V	10	3.3	20
FW_DIODE_BYPASS_V	10	3.3	20
FW_PWR	10	24	20
FW_PWR_SW	10	24	20
FW_PHY_3_3	10	3.3	20
FW_VGND	10	0	20
FW_VP	10	12	20
FW_VP1	10	12	20
FW_VP2	10	12	20
FW_VP_1	10	12	20
FW_VP_2	10	12	20

36B6<
36B6<> 36B7<>
29B3< 36D6< 50C6<> 51D4<>
36D6< 51D2<>
36B5< 36B7< 36D7<

36D5<
36D1<> 36D3<>
36C1<> 36D3<>
36D4<
36D4<

GRAPHICS POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
+3.3VFPD	10	3.6	20
DAC2VDD	10	3.3	20
DACVDD	10	3.3	20
DDC_VCC_3	10	3.3	20
DDC_VCC_5	10	5	20
DDR_VREF	10	1.25	20
IFP0AVCC	10	3.8	20
IFP0VREF	10	3.8	20
INT_TMDS_3V	10	3.6	20
GPU_AGP_VREF	10	0.75	20
GPU_FB_VREF	10	1.25	20
GRAPH_CORE	10	1.6	20
NVPLLVDD	10	3.3	20
SGRAVREF	10	1.25	20
SGRBVREF	10	1.25	20

24D7< 51C1<>
22C5<
22C4<
24B3<> 59B8>
25C4< 59B8>
12A7< 14D2<> 14D8<> 15D8<
23A6< 23C1<
23B4<>
24C3<> 59C8>
17A2< 17A8<
18C8<
17D4< 23C7<> 48C2<>
22D5<
20A3< 20C4< 20C8<
21A3< 21C4< 21C8<

17B5<>	GPU_50PULLUP	1.5	
17A5<>	GPU_50PULLDWN	0	
17A5<	GPU_TMODE	0	
22B2< 22A5<	GPU_XTALSSIN	0	
22D4<	VIPCLK	0	
37B7<	CSLOT_IOWAIT_L	3.3	
38C6<>	EIDE_CSELP_L	0	
38C6<>	EIDE_IOCS16_L	5	
38C2<>	UIDE_CSELP_L	0	
38C2<>	UNUSED_ATAIOCS16_L	5	

INTREPID POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
+1_5V_INTREPID_PLL	10	1.5	20
+1_5V_INTREPID_PLL1	10	1.5	20
+1_5V_INTREPID_PLL2	10	1.5	20
+1_5V_INTREPID_PLL3	10	1.5	20
+1_5V_INTREPID_PLL4	10	1.5	20
+1_5V_INTREPID_PLL5	10	1.5	20
+1_5V_INTREPID_PLL6	10	1.5	20
+1_5V_INTREPID_PLL7	10	1.5	20
+1_5V_INTREPID_PLL8	10	1.5	20
+1_5V_AGP	10	1.5	20
INT_AGP_VREF	10	0.75	20

9D4< 16D6< 28D6<> 30D5<
28C4<
28D4<
28D4<
28D4<
16D5<
30D4<
9D2<
28D4<
10D6< 11A6< 16A8< 16C2< 16D7< 17A3< 17A4< 17D5< 46B4<> 59C8>
16A7< 16C6<>

MAIN POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
+1_8V_MAIN	10	1.8	20
+2_5V_MAIN	10	2.5	20
+3V_MAIN	10	3.3	20
3.8V_TRICKLE	10	3.8	20
+5V_MAIN	10	5	20
+12V_MAIN	10	12	20
+12V_SLEEP	10	12	20
GND	10	0	20
AGND	10	0	20
ANALOGGND	10	0	20
ALTCHGND	10	0	20
CHGND	10	0	20

59D8>
59D8> 49B2<> 30B3<
43C7< 42C8< 42B7< 42B5< 41A7< 41A5< 40D5< 39D4<
59D8>
59D8> 51B4<>

41B3< 41B1<> 41A4< 41A2<> 40C6< 40B6< 40B5<> 35C1<> 35B1<
43A5< 42A6<> 42A5<> 41D3< 41C3<
36B2< 36A7<> 33D4< 33D2< 33C4< 33C2< 33B4< 33B2< 29C3< 25B3<>
36C1<> 36C1<> 36B6<> 36B6<
43B7< 43A7< 29A3< 24B3<

+1_8V_MAIN
+2_5V_MAIN
+3V_MAIN
3.8V_TRICKLE
+5V_MAIN
+12V_MAIN
+12V_SLEEP
ALT CHASSIS

36D8< 44C2< 44C6< 44D7<> 50D5< 52C2>
59D8< 44C2< 44C6< 44D7<> 50D5< 52C1>
59D8>
59D8>
59D8

SIG_NAME	RATSNEST_SCHEDULE RELATIVE_PROPAGATION_DELAY	MAX_VIAS	PROPAGATION_DELAY	STUB_LENGTH	MIN_NECK_WIDTH NET_SPACING_TYPE	MAX_EXPOSED_LENGTH	NO_TEST	FUNC_TEST	PULSE_PARAM
MEM_DATA<0..63>	MEM_GROUP0:G:L:S:0:150	8	L:S::1300		3				167 MHZ
RAM_DATA_A<0..63>	RAM_GROUP0_A:G:L:S:0:180	8	L:S::1800		3				167 MHZ
RAM_DATA_B<0..63>	RAM_GROUP0_B:G:L:S:0:180	2	L:S::2400		3				167 MHZ
MEM_DQS<0..7>	MEM_GROUP0:G:L:S:0:180	3	L:S::1300		3				167 MHZ
RAM_DQS_A<0..7>	RAM_GROUP0_A:G:L:S:0:180	3	L:S::1700		3				167 MHZ
RAM_DQS_B<0..7>	RAM_GROUP0_B:G:L:S:0:180	2	L:S::2400		3				167 MHZ
MEM_DQM<0..7>	MEM_GROUP0:G:L:S:0:180	3	L:S::1300		3				167 MHZ
RAM_DQM_A<0..7>	RAM_GROUP0_A:G:L:S:0:180	3	L:S::1800		3				167 MHZ
RAM_DQM_B<0..7>	RAM_GROUP0_B:G:L:S:0:180	2	L:S::2400		3				167 MHZ
MEM_ADDR<0..12>	MEM_ADDR:G:L:S:0:200	3	L:S::600						
RAM_ADDR<0..12>	RAM_ADDR:G:L:S:0:1300	4	L:S::3500	200					
MEM_BA<0..1>	MEM_ADDR:G:L:S:0:1300	3	L:S::600						
RAM_BA<0..1>	RAM_ADDR:G:L:S:0:1300	4	L:S::4000	200					
MEM_CS_L<0..3>	MEM_ADDR:G:L:S:0:200	3	L:S::600		10 MIL SPACING				
RAM_CS_L<0..1>	RAM_CS_GROUP0:G:L:S:0:400	3	L:S:2000:3500		10 MIL SPACING				
RAM_CS_L<2..3>	RAM_CS_GROUP1:G:L:S:0:350	2	L:S:2000:3500		10 MIL SPACING				
MEM_RAS_L	MEM_ADDR:G:L:S:0 MIL:200 MIL	3	L:S::600 MIL						
MEM_CAS_L	MEM_ADDR:G:L:S:0 MIL:200 MIL	3	L:S::600 MIL						
MEM_WE_L	MEM_ADDR:G:L:S:0 MIL:280 MIL	3	L:S::600 MIL						
RAM_CAS_L	RAM_ADDR:G:L:S:0 MIL:2000 MIL	4	L:S::4000 MIL	200					
RAM_RAS_L	RAM_ADDR:G:L:S:0 MIL:2000 MIL	4	L:S::4000 MIL	200					
RAM_WE_L	RAM_ADDR:G:L:S:0 MIL:2000 MIL	4	L:S::4000 MIL	200					
MEM_CKE<0..3>	MEM_ADDR:G:L:S:0:200	3	L:S::600		10 MIL SPACING				
RAM_CKE<0..1>	RAM_CS_GROUP0:G:L:S:0:400	3	L:S::2500		10 MIL SPACING				
RAM_CKE<2..3>	RAM_CS_GROUP1:G:L:S:0:350	2	L:S::2500		10 MIL SPACING				
MEM_MUXSEL_H<0..1>		3	L:S::1000						
MEM_MUXSEL_L<0..1>		3	L:S::1000						167 MHZ
MUX_SEL_H		4	L:S::2000 MIL	200					167 MHZ
MUX_SEL_L		4	L:S::2000 MIL	200					167 MHZ
SYSCLK_DDRCLK_A0_UF		L3	S:500 MIL:850 MIL		8 MIL SPACING	270			167 MHZ
SYSCLK_DDRCLK_A0_UF		L3	S:500 MIL:850 MIL		8 MIL SPACING	270			167 MHZ
SYSCLK_DDRCLK_A0	SYSCLK_DDRCLKA0:G:L:S:0 MIL:100 MIL	3	L:S::2600 MIL	200	8 MIL SPACING	270			167 MHZ
SYSCLK_DDRCLK_A0_L	SYSCLK_DDRCLKA0:G:L:S:0 MIL:100 MIL	3	L:S::2600 MIL	200	8 MIL SPACING	270			167 MHZ
SYSCLK_DDRCLK_A1_UF		L3	S:500 MIL:850 MIL		8 MIL SPACING	270			167 MHZ
SYSCLK_DDRCLK_A1_UF		L3	S:500 MIL:850 MIL		8 MIL SPACING	270			167 MHZ
SYSCLK_DDRCLK_A1	SYSCLK_DDRCLKA1:G:L:S:0 MIL:100 MIL	3	L:S::2600 MIL	200	8 MIL SPACING	270			167 MHZ
SYSCLK_DDRCLK_A1_L	SYSCLK_DDRCLKA1:G:L:S:0 MIL:100 MIL	3	L:S::2600 MIL	200	8 MIL SPACING	270			167 MHZ
SYSCLK_DDRCLK_A2_UF		L3	S:500 MIL:850 MIL		8 MIL SPACING	270			167 MHZ
SYSCLK_DDRCLK_A2_UF		L3	S:500 MIL:850 MIL		8 MIL SPACING	270			167 MHZ
SYSCLK_DDRCLK_A2_L		3	L:S::750 MIL		8 MIL SPACING	270			167 MHZ
SYSCLK_DDRCLK_B0_UF		L3	S:500 MIL:850 MIL		8 MIL SPACING	270			167 MHZ
SYSCLK_DDRCLK_B0_UF		L3	S:500 MIL:850 MIL		8 MIL SPACING	270			167 MHZ
SYSCLK_DDRCLK_B0	SYSCLK_DDRCLKB0:G:L:S:0 MIL:100 MIL	3	L:S::3500 MIL	200	8 MIL SPACING	270			167 MHZ
SYSCLK_DDRCLK_B0_L	SYSCLK_DDRCLKB0:G:L:S:0 MIL:100 MIL	3	L:S::3500 MIL	200	8 MIL SPACING	270			167 MHZ
SYSCLK_DDRCLK_B1_UF		L3	S:500 MIL:850 MIL		8 MIL SPACING	270			167 MHZ
SYSCLK_DDRCLK_B1_UF		L3	S:500 MIL:850 MIL		8 MIL SPACING	270			167 MHZ
SYSCLK_DDRCLK_B1	SYSCLK_DDRCLKB1:G:L:S:0 MIL:100 MIL	3	L:S::3500 MIL	200	8 MIL SPACING	270			167 MHZ
SYSCLK_DDRCLK_B1_L	SYSCLK_DDRCLKB1:G:L:S:0 MIL:100 MIL	3	L:S::3200 MIL	200	8 MIL SPACING	270			167 MHZ
SYSCLK_DDRCLK_B2_UF		L3	S:500 MIL:850 MIL		8 MIL SPACING	270			167 MHZ
SYSCLK_DDRCLK_B2_UF		L3	S:500 MIL:850 MIL		8 MIL SPACING	270			167 MHZ
SYSCLK_DDRCLK_B2	SYSCLK_DDRCLKB2:G:L:S:0 MIL:100 MIL	3	L:S::3500 MIL	200	8 MIL SPACING	270			167 MHZ
SYSCLK_DDRCLK_B2_L	SYSCLK_DDRCLKB2:G:L:S:0 MIL:100 MIL	3	L:S::3500 MIL	200	8 MIL SPACING	270			167 MHZ
INT_REF_CLK_IN_PD		8	L:S::2500 MIL		10 MIL SPACING	270			66.56 MHZ
PCI_AD<31..0>	MIN_DAISY_CHAIN	6	L:S:6000:8000	500					33 MHZ
PCI_CBE<3..0>	MIN_DAISY_CHAIN	6	L:S:6000:8000	500					33 MHZ
PCI_FRAME_L	MIN_DAISY_CHAIN	L7	S:6000 MIL:8000 MIL	500					33 MHZ

DIGITAL SIGNAL CONSTRAINTS

SIGNAL CONSTRAINTS

APPLE COMPUTER INC.
SIZE D | DRAWING NUMBER 051-6497 | REV. 13
SCALE NONE | SHT 53 OF 69
DRAWING

SIG_NAME	RATSNEST_SCHEDULE RELATIVE_PROPAGATION_DELAY	MAX_VIAS	PROPAGATION_DELAY	STUB_LENGTH	NET_SPACING_TYPE	MAX_EXPOSED_LENGTH	DIFFERENTIAL_PAIR	FUNC_TEST	PULSE_PARAM
32B6<> 31B7< 30C5<> 30B7<PCI_IRDY_L	MIN_DAISY_CHAIN	6	S:6000 MIL:8000 MIL	50					33 MHZ
59A6> 32B6<> 31B7< 30C5<> 30B7<PCI_TRDY_L	MIN_DAISY_CHAIN	6	S:6000 MIL:8000 MIL	50					33 MHZ
59A6> 32B6<> 31B7< 30C5<> 30B7<PCI_DEVSEL_L	MIN_DAISY_CHAIN	6	S:6000 MIL:8000 MIL	50					33 MHZ
59A6> 32B6<> 31B7< 30C5<> 30B7<PCI_STOP_L	MIN_DAISY_CHAIN	6	S:6000 MIL:8000 MIL	50					33 MHZ
59A6> 32B6<> 31B7< 30C5<>PCI_PAR	MIN_DAISY_CHAIN	6	S:6000 MIL:8000 MIL	50					33 MHZ
30D5<>CLK33M_PCI_SLOTB_UF		B	S:600 MIL:1000 MIL	200		450			33 MHZ
30D5<>CLK33M_PCI_SLOTC_UF		B	S:600 MIL:1200 MIL	200		450			33 MHZ
30D5<>CLK33M_PCI_SLOTD_UF		B	S:600 MIL:1000 MIL	200		450			33 MHZ
59A6> 31C2<> 30D7<CLK33M_PCI_SLOTB		5	S:3000 MIL:4000 MIL	200	10 MIL SPACING	450			33 MHZ
30C5<>INT_PCI_FB_OUT		4	L:S::1000 MIL	200		450			33 MHZ
30D8<PCI_FBO_PLUS2		4	L:S::200 MIL	200		450			33 MHZ
30C8<PCI_FB_PLUS4		4	S:1900 MIL:2000 MIL			450			33 MHZ
30C8<PCI_FBI_PLUS2		4	S:1900 MIL:2000 MIL	200		450			33 MHZ
30C7<PCI_FBI_EQUAL		4	S:2600 MIL:3000 MIL	200		450			33 MHZ
30C7<PCI_FB_PLUS6		4	S:5900 MIL:6000 MIL			450			33 MHZ
30C5<>INT_PCI_FB_IN		4	L:S::1080 MIL	200		450			33 MHZ
31C6< 31C3<> 31C2<> 31B7< 31B6<> 31B3<> 31B2<>PCIT_AD<31..0>		3	L:S::1000						33 MHZ
59C3> 59B3> 31C7<> 59A6> 31C3<> 31B6< 31B2<>PCIT_CBE<31..0>		3	L:S::1000						33 MHZ
31C2<> 31B6<PCIT_FRAME_L		3	L:S::1000 MIL						33 MHZ
59B6> 31C3<> 31B6<PCIT_IRDY_L		3	L:S::1000 MIL						33 MHZ
31C2<> 31B6<PCIT_TRDY_L		3	L:S::1000 MIL						33 MHZ
31C2<> 31B6<PCIT_DEVSEL_L		3	L:S::1000 MIL						33 MHZ
31C2<> 31B6<PCIT_STOP_L		3	L:S::1000 MIL						33 MHZ
31C2<> 31B6<PCIT_PAR		3	L:S::1000 MIL						33 MHZ
17D8< 17C8< 16C4<>AGP_AD<0..15>	AGP_GROUP0:G:L:S:0:280	5	L:S::4500						266 MHZ
17C8< 16B4<>AGP_CBE<0..1>	AGP_GROUP0:G:L:S:0:330	5	L:S::4500						266 MHZ
17B8< 16B3< 16A4<>AGP_AD_STB<0>	AGP_GROUP0:G:L:S:0 MIL:330 MIL	4	L:S::4400 MIL	200	8 MIL SPACING	500	AGP_ADSTBDP0		133 MHZ
17B8< 16D1< 16A4<>AGP_AD_STB_L<0>	AGP_GROUP0:G:L:S:0 MIL:330 MIL	4	L:S::4400 MIL	200	8 MIL SPACING	500	AGP_ADSTBDP0		133 MHZ
17C8< 16C4<> 16B4<>AGP_AD<16..31>	AGP_GROUP0:G:L:S:0:280	5	L:S::4500						266 MHZ
17C8< 16B4<>AGP_CBE<2..3>	AGP_GROUP0:G:L:S:0:280	5	L:S::4500						266 MHZ
17B8< 16B3< 16A4<>AGP_AD_STB<1>	AGP_GROUP0:G:L:S:0 MIL:280 MIL	4	L:S::4400 MIL	200	8 MIL SPACING	500	AGP_ADSTBDP1		133 MHZ
17B8< 16D1< 16A4<>AGP_AD_STB_L<1>	AGP_GROUP0:G:L:S:0 MIL:330 MIL	4	L:S::4400 MIL	200	8 MIL SPACING	500	AGP_ADSTBDP1		133 MHZ
17B8< 16C3< 16B4<>AGP_FRAME_L		5	S:4000 MIL:4500 MIL						66 MHZ
17B8< 16C3< 16B4<>AGP_IRDY_L		5	S:4000 MIL:4500 MIL						66 MHZ
17B8< 16B4<> 16B3<AGP_TRDY_L		5	S:4000 MIL:4500 MIL						66 MHZ
17B8< 16C3< 16B4<>AGP_DEVSEL_L		5	S:4000 MIL:4500 MIL						66 MHZ
17B8< 16B4<> 16B3<AGP_STOP_L		5	S:4000 MIL:4500 MIL						66 MHZ
17B8< 16B4<>AGP_PAR		5	S:4000 MIL:4500 MIL						66 MHZ
17A8< 16C1< 16B4< 16B4<> 16B1< 16A4<>AGP_SBA<0..7>		5	L:S:4000:4500						
17B8< 16B3< 16A4<>AGP_SB_STB	AGP_GROUP99:G:L:S:0 MIL:200 MIL	3	L:S::4500 MIL				AGP_SBSTBB		
17A8< 16D1< 16A4<>AGP_SB_STB_L	AGP_GROUP99:G:L:S:0 MIL:200 MIL	3	L:S::4500 MIL				AGP_SBSTBB		
17B6< 16B1< 16A4<>AGP_ST<0..2>		5	L:S:4500:5000						
17B8< 16B3< 16A4<>AGP_PIPE_L		5	S:4000 MIL:4500 MIL						
17B8< 16B3< 16A4<>AGP_RBF_L		5	S:4000 MIL:4500 MIL						
17B7<> 16C4<> 16C3<AGP_REQ_L		5	S:4500 MIL:5000 MIL						
17B7< 16C4<> 16C3<AGP_GNT_L		5	S:4500 MIL:5000 MIL						
17B8< 16B1< 16A6<>AGP_WBF_L		5	S:4000 MIL:4500 MIL						
17A8> 16D3< 16D1< 16C6<>AGP_BUSY_L		5	S:4500 MIL:5000 MIL						
17A8< 16D3< 16C6<>STOP_AGP_L		5	S:4500 MIL:5000 MIL						
17D7<> 17D6<> 17C6<>GPU_AGP_AD<0..15>	GPU_AGP_GROUP0:G:L:S:0:100	3	L:S::600						266 MHZ
17C6<>GPU_AGP_CBE<0..1>	GPU_AGP_GROUP0:G:L:S:0:100	3	L:S::600						266 MHZ
AGP_AD_STB_GPU_UF<0>	GPU_AGP_STB0:G:L:S:0 MIL:50 MIL	3	L:S::450 MIL		8 MIL SPACING	500	GPU_ADSTBDP0		133 MHZ
AGP_AD_STB_L_GPU_UF<0>	GPU_AGP_STB0:G:L:S:0 MIL:50 MIL	3	L:S::800 MIL		8 MIL SPACING	500	GPU_ADSTBDP0		133 MHZ
17C6<> GPU_AGP_AD<16..31>	GPU_AGP_GROUP1:G:L:S:0:100	3	L:S::600						266 MHZ
17C6<>GPU_AGP_CBE<2..3>	GPU_AGP_GROUP1:G:L:S:0:100	3	L:S::600						266 MHZ
AGP_AD_STB_GPU_UF<1>	GPU_AGP_STB1:G:L:S:0 MIL:50 MIL	3	L:S::800 MIL		8 MIL SPACING	500	GPU_ADSTBDP1		133 MHZ
AGP_AD_STB_L_GPU_UF<1>	GPU_AGP_STB1:G:L:S:0 MIL:50 MIL	3	L:S::800 MIL		8 MIL SPACING	500	GPU_ADSTBDP1		133 MHZ
17B6<>GPU_AGP_FRAME_L		3	S:300 MIL:600 MIL						66 MHZ
17B6<>GPU_AGP_IRDY_L		3	S:300 MIL:600 MIL						66 MHZ
17B6<>GPU_AGP_TRDY_L		3	S:300 MIL:600 MIL						66 MHZ
17B6<>GPU_AGP_DEVSEL_L		3	S:300 MIL:600 MIL						66 MHZ
17B6<>GPU_AGP_STOP_L		3	S:300 MIL:600 MIL						66 MHZ
17B6<>GPU_AGP_PAR		3	S:300 MIL:600 MIL						66 MHZ
17A6<>GPU_AGP_SBA<0..7>		3	L:S:300:600						
17B6<>GPU_AGP_SB_STB	GPU_AGP_SBSTB:G:L:S:0 MIL:50 MIL	3	L:S:300 MIL:600 MIL				GPU_SBSTBB		
17A6<>GPU_AGP_SB_STB_L	GPU_AGP_SBSTB:G:L:S:0 MIL:50 MIL	3	L:S:300 MIL:600 MIL				GPU_SBSTBB		
17B6<>GPU_AGP_PIPE_L		3	S:300 MIL:600 MIL						
17B6<>GPU_AGP_RBF_L		3	S:300 MIL:600 MIL						
16C6<>CLK66M_GPU_UF		3	S:1000 MIL:1100 MIL		10 MIL SPACING	250			66 MHZ
17C7< 16D8<CLK66M_GPU_AGP		4	S:3700 MIL:3900 MIL	200	10 MIL SPACING	250			66 MHZ
16C6<>INT_AGP_FB_OUT		4	S:1400 MIL:1500 MIL	200		250			66 MHZ
16B7<AGP_FBO_EQUAL		4	S:900 MIL:1080 MIL	200		250			66 MHZ
16B8<AGP_FB_PLUS2		4	S:1900 MIL:2000 MIL			250			66 MHZ
16C7<AGP_FBI_EQUAL		4	L:S::200 MIL	200		250			66 MHZ
16C6<INT_AGP_FB_IN		4	L:S::1200 MIL	200		250			66 MHZ
30C5<> 30A7< 16D7<INT_ROM_OVERLAY_PU		3	S:600 MIL:800 MIL		10 MIL SPACING	250			66 MHZ
59A8> 56B3> 16C7> 9B4< 8A2<INT_ANALYZER_CLK		3	L:S::2800 MIL		8 MIL SPACING	250			166 MHZ
32A6< 30D7<CLK33M_PCI_SLOTD		4	S:3000 MIL:3500 MIL	200	8 MIL SPACING	250			33 MHZ

SIGNAL CONSTRAINTS

APPLE COMPUTER INC.
SIZE D | DRAWING NUMBER 051-6497 | REV. 13
SCALE NONE | SHT 54 OF 69
DRAWING

DIGITAL SIGNALS

RATSNEST_SCHEDULE

GROUP	SIG_NAME	RELATIVE_PROPAGATION_DELAY	MAX VIAS	PROPAGATION_DELAY	STUB_LENGTH	NET_SPACING_TYPE	MAX EXPOSED LENGTH	PULSE PARAM	
	FBD<0..63>	GPU_FBDATA_A:G:L:S:0:225	2	L:S::800				300 MHZ	18E8<> 18F8<> 18G8<> 19C5< 19C8< 19D5< 19D8<
	RFBD<0..63>	RAM_FBDATA_A:G:L:S:0:300	2	L:S::1000				300 MHZ	19C4< 19C7< 19D4< 19D7< 20B1<> 20B5<> 20C1<> 20C5<>
	FBDQM<0..7>	GPU_FBDQM_A:G:L:S:0:200	2	L:S::800				300 MHZ	18D8> 18G3<
	RFBDQM<0..7>	RAM_FBDQM_A:G:L:S:0:200	2	L:S::1000				300 MHZ	18G2< 20C2< 20C6<
	FBA<0..12>	GPU_FBADDR_A:G:L:S:0:200	2	L:S::700				300 MHZ	18C8> 18D8> 18E3< 18F3<
	RFBA<0..11>	RAM_FBADDR_A:G:L:S:0:330	2	L:S::2400	2350			300 MHZ	18E2<> 18F2<> 20C2< 20C6< 20D2< 20D6<
	FBABA<0..1>	GPU_FBADDR_A:G:L:S:0:200	2	L:S::600				300 MHZ	18C8<> 18E3<
	RFBABA<0..1>	RAM_FBADDR_A:G:L:S:0:330	2	L:S::2400	50			300 MHZ	18E2<> 20C2< 20C6<
	FBARAS_L	GPU_FBCNTL_A:G:L:S:0 MIL:200 MIL	1	L:S::400 MIL				300 MHZ	18C8> 18G3<
	FBACAS_L	GPU_FBCNTL_A:G:L:S:0 MIL:200 MIL	1	L:S::400 MIL				300 MHZ	18C8> 18G3<
	FBAWE_L	GPU_FBCNTL_A:G:L:S:0 MIL:200 MIL	1	L:S::400 MIL				300 MHZ	18C8> 18F3<
	FBACS0_L	GPU_FBCNTL_A:G:L:S:0 MIL:200 MIL	1	L:S::400 MIL				300 MHZ	18C8> 18F3<
	FBACKE	GPU_FBCNTL_A:G:L:S:0 MIL:200 MIL	1	L:S::400 MIL	100			300 MHZ	18D3< 18D7<>
	RFBARAS_L	RAM_FBCNTL_A:G:L:S:0 MIL:350 MIL	2	L:S::2700 MIL	50			300 MHZ	18G2<> 20B2< 20B6<
	RFBACAS_L	RAM_FBCNTL_A:G:L:S:0 MIL:500 MIL	2	L:S::2700 MIL	50			300 MHZ	18G2<> 20B2< 20B6<
	RFBAWE_L	RAM_FBCNTL_A:G:L:S:0 MIL:500 MIL	2	L:S::2700 MIL	50			300 MHZ	18F2<> 20B2< 20B6<
	RFBACS0_L	RAM_FBCNTL_A:G:L:S:0 MIL:350 MIL	2	L:S::2700 MIL	50			300 MHZ	18F2<> 20B2< 20B6<
	RFBACKE	RAM_FBCNTL_A:G:L:S:0 MIL:500 MIL	2	L:S::2700 MIL	50			300 MHZ	18D2<> 20C2< 20C6<
	FBDQS<0..7>	GPU_FBDQS_A:G:L:S:0:100	0	L:S::350				300 MHZ	18C7<> 19A8<
	FBDQSTERM<0..7>	FB_DQSTERM_A:G:L:S:0:80	0	L:S::1500		10 MIL SPACING		300 MHZ	19A7<
	RFBDQS<0..7>	RAM_FBDQS_A:G:L:S:0:55	0	L:S::150		10 MIL SPACING		300 MHZ	19A6< 20C2<> 20C6<>
	FBACLK0	GPU_FBCLK_A:G:L:S:0 MIL:50 MIL	1	L:S::150 MIL			200	300 MHZ	18D7> 19C3<
	FBACLK0_L	GPU_FBCLK_A:G:L:S:0 MIL:50 MIL	1	L:S::150 MIL			200	300 MHZ	18D7> 19C3<
	FBACLK1	GPU_FBCLK_A:G:L:S:0 MIL:50 MIL	1	L:S::150 MIL			200	300 MHZ	18D7> 19D3<
	FBACLK1_L	GPU_FBCLK_A:G:L:S:0 MIL:50 MIL	1	L:S::150 MIL			200	300 MHZ	18D7> 19D3<
	RFBACLK1	RAM_FBCLK_A:G:L:S:0 MIL:80 MIL	1	L:S::2500 MIL			200	300 MHZ	19D1< 20C2<
	RFBACLK1_L	RAM_FBCLK_A:G:L:S:0 MIL:80 MIL	1	L:S::2500 MIL			200	300 MHZ	19D1< 20C2<
	RFBACLK0	RAM_FBCLK_A:G:L:S:0 MIL:70 MIL	1	L:S::2500 MIL			200	300 MHZ	19C1< 20C6<
	RFBACLK0_L	RAM_FBCLK_A:G:L:S:0 MIL:70 MIL	1	L:S::2500 MIL			200	300 MHZ	19C1< 20C6<
	FBD<64..127>	GPU_FBDATA_B:G:L:S:0:225	2	L:S::800				300 MHZ	18E5<> 18F5<> 18G5<> 19B5< 19B8< 19C5< 19C8<
	RFBD<64..127>	RAM_FBDATA_B:G:L:S:0:325	2	L:S::1000				300 MHZ	19B4< 19B7< 19C4< 19C7< 21B1<> 21B5<> 21C1<> 21C5<>
	FBDQM<8..15>	GPU_FBDQM_B:G:L:S:0:120	1	L:S::800				300 MHZ	18C3< 18D3< 18D5>
	RFBDQM<8..15>	RAM_FBDQM_B:G:L:S:0:120	1	L:S::1000				300 MHZ	18C2< 18D2< 21C2< 21C6<
	FBBA<0..12>	GPU_FBADDR_B:G:L:S:0:120	1	L:S::600				300 MHZ	18A3< 18B3< 18C3< 18C5<> 18D5<>
	RFBBA<0..11>	RAM_FBADDR_B:G:L:S:0:370	1	L:S::2400	50			300 MHZ	18B2<> 18C2<> 21C2< 21C6< 21D2< 21D6<
	FBBBA<0..1>	GPU_FBADDR_B:G:L:S:0:120	1	L:S::600				300 MHZ	18A3< 18C5<>
	RFBBBA<0..1>	RAM_FBADDR_B:G:L:S:0:370	1	L:S::2400	50			300 MHZ	18A2<> 21C2< 21C6<
	FBBRAS_L	GPU_FBCNTL_B:G:L:S:0 MIL:120 MIL	1	L:S::400 MIL				300 MHZ	18C3< 18D4<>
	FBBCAS_L	GPU_FBCNTL_B:G:L:S:0 MIL:120 MIL	1	L:S::400 MIL				300 MHZ	18C3< 18D4<>
	FBBWE_L	GPU_FBCNTL_B:G:L:S:0 MIL:120 MIL	1	L:S::400 MIL				300 MHZ	18C3< 18D4<>
	FBBCS0_L	GPU_FBCNTL_B:G:L:S:0 MIL:120 MIL	1	L:S::400 MIL				300 MHZ	18C3< 18C4<>
	FBBCKE	GPU_FBCNTL_B:G:L:S:0 MIL:120 MIL	1	L:S::400 MIL	100			300 MHZ	18A3< 18C4<>
	RFBBRAS_L	RAM_FBCNTL_B:G:L:S:0 MIL:2000 MIL	3	L:S::3500 MIL	3550			300 MHZ	18C2<> 21B2< 21B6<
	RFBBCAS_L	RAM_FBCNTL_B:G:L:S:0 MIL:2000 MIL	3	L:S::3500 MIL	3550			300 MHZ	18C2<> 21B2< 21B6<
	RFBBWE_L	RAM_FBCNTL_B:G:L:S:0 MIL:2000 MIL	3	L:S::3500 MIL	3550			300 MHZ	18C2<> 21B2< 21B6<
	RFBBCS0_L	RAM_FBCNTL_B:G:L:S:0 MIL:2000 MIL	3	L:S::3500 MIL	3550			300 MHZ	18C2<> 21B2< 21B6<
	RFBBCKE	RAM_FBCNTL_B:G:L:S:0 MIL:2000 MIL	3	L:S::3500 MIL	3550			300 MHZ	18A2<> 21C2< 21C6<
	FBDQS<8..15>	GPU_FBDQS_B:G:L:S:0:100	0	L:S::350		10 MIL SPACING		300 MHZ	18D4<> 19A5<
	FBDQSTERM<8..15>	FB_FBDQSTERM_B:G:L:S:0:60	0	L:S::1500		10 MIL SPACING		300 MHZ	19A4<
	RFBDQS<8..15>	RAM_FBDQS_B:G:L:S:0:50	0	L:S::150		10 MIL SPACING		300 MHZ	19A3< 21C2<> 21C6<>
	FBBCLK0	GPU_FBCLK_B:G:L:S:0 MIL:50 MIL	1	L:S::150 MIL			200	300 MHZ	18C5<> 19B3<
	FBBCLK0_L	GPU_FBCLK_B:G:L:S:0 MIL:50 MIL	1	L:S::150 MIL			200	300 MHZ	18C5> 19B3<
	FBBCLK1	GPU_FBCLK_B:G:L:S:0 MIL:50 MIL	1	L:S::150 MIL			200	300 MHZ	18C5> 19C3<
	FBBCLK1_L	GPU_FBCLK_B:G:L:S:0 MIL:50 MIL	1	L:S::150 MIL			200	300 MHZ	18C5> 19B3<
	RFBBCLK1	RAM_FBCLK_B:G:L:S:0 MIL:90 MIL	1	L:S::2500 MIL			200	300 MHZ	19C1< 21C2<
	RFBBCLK1_L	RAM_FBCLK_B:G:L:S:0 MIL:90 MIL	1	L:S::2500 MIL			200	300 MHZ	19B1< 21C2<
	RFBBCLK0	RAM_FBCLK_B:G:L:S:0 MIL:90 MIL	1	L:S::2500 MIL			200	300 MHZ	19B1< 21C6<
	RFBBCLK0_L	RAM_FBCLK_B:G:L:S:0 MIL:90 MIL	1	L:S::2500 MIL			200	300 MHZ	19B1< 21C6<

SIGNAL CONSTRAINTS

NOTICE OF PROPRIETARY PROPERTY

LAST_MODIFIED=Wed Sep 17 12:12:38 2003

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6497	13

SCALE: NONE

SHT 55 OF 69

DRAWING

<XR_PAGE_TITLE>

DIGITAL SIGNALS

GROUP	SIG_NAME	RELATIVE_PROPAGATION_DELAY	VIAS	PROPAGATION_DELAY	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	MAX_EXPOSED_LENGTH	
MAXBUS	CPU_ADDR<0..31>	CPU_ADDR_GROUP:G:L:S:0 MIL:60 MIL	7	:::5000	250			166 MHZ		4B7<> 4C7<> 8B4<> 8B5<> 8B7<> 8B8<> 8C4<> 8C5<> 8C7<> 8C8<>
	CPU_DATA<0..63>	CPU_DATA_GROUP:G:L:S:0 MIL:60 MIL	7	:::1400	1550			166 MHZ		9C3<> 9D3<> 9D5<> 9D8<>
	CPU_BR_L	CPU_CNTL_GROUP:G:L:S:0 MIL:60 MIL	7	:::5000	250	10 MIL SPACING		166 MHZ		9A3<> 9B4<> 9C4<> 9C4< 9D4<> 9C6<> 8C4<> 8C4< 8C5<> 8C7<> 8C7< 8C8<> 9D4<> 8D5<> 8D7<> 8D8<> 9A7< 9B1<> 9B7< 9C1<> 9C5< 9C8< 9D1<>
	CPU_BG_L	CPU_CNTL_GROUP:G:L:S:0 MIL:60 MIL	7	:::5000	250	10 MIL SPACING		166 MHZ		4D7> 7C7< 8B4<> 9D3<
	CPU_BG_L	CPU_CNTL_GROUP:G:L:S:0 MIL:60 MIL	7	:::5000	250	10 MIL SPACING		166 MHZ		4D7< 7B7< 8B4<> 9D3<>
	CPU_TS_L	CPU_CNTL_GROUP:G:L:S:0 MIL:60 MIL	7	:::5000	250	10 MIL SPACING		166 MHZ		4D7<> 7C7< 8B7<> 9D3<>
	CPU_TT<0..4>	CPU_CNTL_GROUP:G:L:S:0 MIL:60 MIL	7	:::1350	250	10 MIL SPACING		166 MHZ		4B7<> 7A7< 8B4<> 8B5<> 9B3<>
	CPU_TBST_L	CPU_CNTL_GROUP:G:L:S:0 MIL:60 MIL	7	:::5000	250	10 MIL SPACING		166 MHZ		4B7> 7B7< 8B4<> 9B3<>
	CPU_TSIZ<0..2>	CPU_CNTL_GROUP:G:L:S:0 MIL:60 MIL	7	:::1250	250	10 MIL SPACING		166 MHZ		4B7> 8B5<> 8B7< 9B3<>
	CPU_ARTRY_L	CPU_CNTL_GROUP:G:L:S:0 MIL:60 MIL	7	:::5000	250	10 MIL SPACING		166 MHZ		4A7<> 7C7< 8B8<> 9B3<>
	CPU_AACK_L	CPU_CNTL_GROUP:G:L:S:0 MIL:60 MIL	7	:::5000	250	10 MIL SPACING		166 MHZ		4A7< 7B7< 8B5<> 9B3<>
	CPU_GBL_L	CPU_CNTL_GROUP:G:L:S:0 MIL:60 MIL	7	:::1000	250	10 MIL SPACING		166 MHZ		4B8<> 8B5<>
	CPU_INT_GBL_L	CPU_CNTL_GROUP:G:L:S:0 MIL:60 MIL	6	:::3500	250	10 MIL SPACING		166 MHZ		4B8< 7B7< 9C3<>
	CPU_CI_L	CPU_CNTL_GROUP:G:L:S:0 MIL:60 MIL	7	:::5000	250	10 MIL SPACING		166 MHZ		4A7> 7A7< 8C5<> 9C3<>
	CPU_HIT_L	CPU_CNTL_GROUP:G:L:S:0 MIL:60 MIL	7	:::5000	250	10 MIL SPACING		166 MHZ		4A7> 7C7< 8B8<> 9B3<
	CPU_DBG_L	CPU_CNTL_GROUP:G:L:S:0 MIL:60 MIL	6	:::3500	250	10 MIL SPACING		166 MHZ		4C3< 7B7< 8B8<> 9B1<>
	CPU_DRDY_L	CPU_CNTL_GROUP:G:L:S:0 MIL:60 MIL	6	:::1500	250	10 MIL SPACING		166 MHZ		4C2< 7B7< 8B5<> 9B1<
	CPU_WT_L	CPU_CNTL_GROUP:G:L:S:0 MIL:60 MIL	7	:::5000	250	10 MIL SPACING		166 MHZ		4B7> 7A7< 8B5<> 9B3<>
	CPU_DRDY_L_UF		2	:::5000	250	10 MIL SPACING		166 MHZ		4C3<>
	CPU_DTI<0..2>	CPU_CNTL_GROUP:G:L:S:0 MIL:60 MIL	7	:::1250	250	10 MIL SPACING		166 MHZ		4C3< 8B4<> 8B7<> 9A1<>
	CPU_TA_L	CPU_CNTL_GROUP:G:L:S:0 MIL:60 MIL	7	:::5000	250	10 MIL SPACING		166 MHZ		4C3< 7C7< 8C4<> 9A1<>
	CPU_TEA_L	CPU_CNTL_GROUP:G:L:S:0 MIL:60 MIL	7	:::5000	250	10 MIL SPACING		166 MHZ		4C3< 7B7< 8B5<> 9A1<>
	CPU_QREQ_L	CPU_CNTL_GROUP:G:L:S:0 MIL:60 MIL	7	:::1000	250	10 MIL SPACING		166 MHZ		4C3> 7D5< 8B7<> 9B3<
	CPU_QACK_L	CPU_CNTL_GROUP:G:L:S:0 MIL:60 MIL	7	:::4000	250	10 MIL SPACING		166 MHZ		4C3< 8B4<> 9B3<>
	SYSCLK_CPU_UF		2	:::150		10 MIL SPACING		166 MHZ	315	9A3<>
	SYSCLK_CPU		4	::2200:2400	200	10 MIL SPACING		166 MHZ	315	4D2< 9A4<
	INT_CPU_FB_OUT		3	:::1000	200			166 MHZ	315	9B3<>
	CPU_FBO_PLUS1		3	:::200	200			166 MHZ	315	9A5<
	CPU_FBI_PLUS1		3	::1400:1500	200			166 MHZ	315	9A5<
	CPU_FB_MINUS3		4	::900:1000	200			166 MHZ	315	9A4<
	INT_CPU_FB_IN		4	:::1000	200			166 MHZ	315	9B3<
	CPU_FB_PLUS2		3	::900:1000				166 MHZ	315	9A5<
	CPU_FB_PLUS3		3	::2900:3000				166 MHZ	315	9A4<
	INT_ANALYZER_CLK		3	:::300				166 MHZ		8A2< 9B4< 16C7< 54A7< 59A8>
	SYSCLK_LA		2	:::2000				166 MHZ		8A2< 8D8<>
	INT_CLOCK_OUT		3	:::3000				166 MHZ		8B2<>

					MIN_LINE_WIDTH	DIFFERENTIAL_PAIR			
USB2_XT1		3	:::1000	100	10 MIL SPACING		30 MHZ		32C4<
USB2_XT2_B		3	:::1000	100	10 MIL SPACING		30 MHZ		
USB2_XT2		3	:::100	100	10 MIL SPACING		30 MHZ		32C4<>
USB2_RREF		2	:::100						32B4<>
USB2_RSDAM	USB2_RSDA:G:L:S:02MIL:20 MIL	6	:::600		8 MIL SPACING 3.5		480 MHZ		32C4<>
USB2_RSDAP	USB2_RSDA:G:L:S:02MIL:20 MIL	6	:::600		8 MIL SPACING 3.5		480 MHZ		32C4<>
USB2_RSDBM	USB2_RSDB:G:L:S:02MIL:20 MIL	6	:::600		8 MIL SPACING 3.5		480 MHZ		32C4<>
USB2_RSDBP	USB2_RSDB:G:L:S:02MIL:20 MIL	6	:::600		8 MIL SPACING 3.5		480 MHZ		32C4<>
USB2_RSDCM	USB2_RSDC:G:L:S:02MIL:20 MIL	6	:::600		8 MIL SPACING 3.5		480 MHZ		32C4<> RATSNEST_SCEDULE
USB2_RSDCP	USB2_RSDC:G:L:S:02MIL:20 MIL	6	:::600		8 MIL SPACING 3.5		480 MHZ		32C4<>
USB2_DAN_F	USB2_DMA:G:L:S:0 MIL:30 MIL	5	:::1500	50	8 MIL SPACING 3.5	USB2_DMA_DP	480 MHZ	MIN_DAISY_CHAIN	32C1<> 33B7<
USB2_DAP_F	USB2_DMA:G:L:S:0 MIL:30 MIL	5	:::1500	50	8 MIL SPACING 3.5	USB2_DMA_DP	480 MHZ	MIN_DAISY_CHAIN	32C1<> 33B7<
USB2_DBN_F	USB2_DMB:G:L:S:0 MIL:20 MIL	5	:::1500	50	8 MIL SPACING 3.5	USB2_DMB_DP	480 MHZ	MIN_DAISY_CHAIN	32C1<> 33C7<
USB2_DBP_F	USB2_DMB:G:L:S:0 MIL:20 MIL	5	:::1500	50	8 MIL SPACING 3.5	USB2_DMB_DP	480 MHZ	MIN_DAISY_CHAIN	32C1<> 33C7<
USB2_DCN_F	USB2_DMC:G:L:S:0 MIL:20 MIL	5	:::1500	50	8 MIL SPACING 3.5	USB2_DMC_DP	480 MHZ	MIN_DAISY_CHAIN	32C1<> 33D7<
USB2_DCP_F	USB2_DMC:G:L:S:0 MIL:20 MIL	5	:::1500	50	8 MIL SPACING 3.5	USB2_DMC_DP	480 MHZ	MIN_DAISY_CHAIN	32C1<> 33D7<
USBT_DAN_F	USB2_DMAT:G:L:S:04MIL:60 MIL	6	:::4000	2000	8 MIL SPACING 3.5	USB2_DMAT_DP	480 MHZ	MIN_DAISY_CHAIN	33B6<>
USBT_DAP_F	USB2_DMAT:G:L:S:04MIL:60 MIL	6	:::4000	2000	8 MIL SPACING 3.5	USB2_DMAT_DP	480 MHZ	MIN_DAISY_CHAIN	33B6<>
USBT_DBN_F	USB2_DMBT:G:L:S:04MIL:60 MIL	6	:::4000	2000	8 MIL SPACING 3.5	USB2_DMBT_DP	480 MHZ	MIN_DAISY_CHAIN	33C6<>
USBT_DBP_F	USB2_DMBT:G:L:S:04MIL:60 MIL	6	:::4000	2000	8 MIL SPACING 3.5	USB2_DMBT_DP	480 MHZ	MIN_DAISY_CHAIN	33C6<>
USBT_DCN_F	USB2_DMCT:G:L:S:04MIL:60 MIL	6	:::4000	2000	8 MIL SPACING 3.5	USB2_DMCT_DP	480 MHZ	MIN_DAISY_CHAIN	33D6<>
USBT_DCP_F	USB2_DMCT:G:L:S:04MIL:60 MIL	6	:::4000	2000	8 MIL SPACING 3.5	USB2_DMCT_DP	480 MHZ	MIN_DAISY_CHAIN	33D6<>
USB_DAN_CON	USB2_CONA:G:L:S:02MIL:30 MIL	5	:::750	50	8 MIL SPACING 3.5	USB2_CONA_DP	480 MHZ	MIN_DAISY_CHAIN	33C3<> 59C6>
USB_DAP_CON	USB2_CONA:G:L:S:02MIL:30 MIL	5	:::750	50	8 MIL SPACING 3.5	USB2_CONA_DP	480 MHZ	MIN_DAISY_CHAIN	33C3<> 59C6>
USB_DBN_CON	USB2_CONB:G:L:S:02MIL:30 MIL	5	:::750	50	8 MIL SPACING 3.5	USB2_CONB_DP	480 MHZ	MIN_DAISY_CHAIN	33B3<> 59C6>
USB_DBP_CON	USB2_CONB:G:L:S:02MIL:30 MIL	5	:::750	50	8 MIL SPACING 3.5	USB2_CONB_DP	480 MHZ	MIN_DAISY_CHAIN	33B3<> 59C6>
USB_DCN_CON	USB2_CONC:G:L:S:02MIL:30 MIL	5	:::750	50	8 MIL SPACING 3.5	USB2_CONC_DP	480 MHZ	MIN_DAISY_CHAIN	33D3<> 59C6>
USB_DCP_CON	USB2_CONC:G:L:S:0 MIL:30 MIL	5	:::750	50	8 MIL SPACING 3.5	USB2_CONC_DP	480 MHZ	MIN_DAISY_CHAIN	33D3<> 59C6>

SIGNAL CONSTRAINTS

LAST_MODIFIED=Wed Sep 17 12:12:39 2003

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6497	13

SCALE	SHT	OF
NONE	56	69

DRAWING

DIGITAL SIGNALS

GROUP	SIG_NAME	RELATIVE_PROPAGATION_DELAY	MAX_VIAS	PROPAGATION_DELAY	STUB_LENGTH	NET_SPACING_TYPE	MIN_LINE_WIDTH MAX_EXPOSED_LENGTH	PULSE_PARAM	
NEW STUFF HERE	VSYNC*		3	L:S::1000 MIL					22C5<>
	ANALOG_VSYNC*		4	L:S::3500 MIL					22D7< 25C6<> 26B5< 59B8>
	HSYNC*		3	L:S::1000 MIL					22C5<>
	ANALOG_HSYNC*		5	L:S::3500 MIL					22D7< 25D6<> 26B5< 59B8>
	ANALOG_BLU		4	L:S::4000 MIL	2200	10 MIL SPACING	5.8		22C7<> 25C6<
	ANALOG_GRN		4	L:S::4000 MIL	2200	10 MIL SPACING	5.8		22C7<> 25C6<
	ANALOG_RED		4	L:S::4000 MIL	2200	10 MIL SPACING	5.8		22C7<> 25B6<
	FILT_ANALOG_RED		2	L:S::500 MIL		10 MIL SPACING	5.8		25C5< 59B8>
	FILT_ANALOG_GRN		2	L:S::500 MIL		10 MIL SPACING	5.8		25C5< 59B8>
	FILT_ANALOG_BLU		2	L:S::500 MIL		10 MIL SPACING	5.8		25C5< 59B8>
	DAC2RSET			L:S::1000 MIL		10 MIL SPACING			22C5<>
	DAC2VREF			L:S::1000 MIL		10 MIL SPACING			22C5<>
	NV11_XTALIN		4	L:S::1000 MIL	100	8 MIL SPACING		27 MHZ	22B4<>
	NV11_XTALOUT		4	L:S::1000 MIL	100	8 MIL SPACING		27 MHZ	22B4<>
	TCKP	TMDSFILT:G:L:S:0 MIL:110 MIL			110	8 MIL SPACING	TMDSFILT_CLK		24C4<>
	TCKM	TMDSFILT:G:L:S:0 MIL:110 MIL			110	8 MIL SPACING	TMDSFILT_CLK		24C3<>
	TD0P	TMDSFILT:G:L:S:0 MIL:110 MIL			110	8 MIL SPACING	TMDSFILT_D0		24C3<>
	TD0M	TMDSFILT:G:L:S:0 MIL:110 MIL			110	8 MIL SPACING	TMDSFILT_D0		24C4<>
	TD1P	TMDSFILT:G:L:S:0 MIL:110 MIL			110	8 MIL SPACING	TMDSFILT_D1		24C4<>
	TD1M	TMDSFILT:G:L:S:0 MIL:110 MIL			110	8 MIL SPACING	TMDSFILT_D1		24C3<>
	TD2P	TMDSFILT:G:L:S:0 MIL:110 MIL			110	8 MIL SPACING	TMDSFILT_D2		24C3<>
	TD2M	TMDSFILT:G:L:S:0 MIL:110 MIL			110	8 MIL SPACING	TMDSFILT_D2		24C4<>
	ENET_LINK_TX_EN		4	L:S::1000 MIL				25 MHZ	34D6<>
	ENET_LINK_TX_ER		4	L:S::1000 MIL				25 MHZ	34D6<>
	ENET_LINK_TXD<0..3>		4	L:S::1000				25 MHZ	34C6<>
	ENET_PHY_TX_EN		4	L:S::5600 MIL				25 MHZ	34D7< 35C6<
	ENET_PHY_TX_ER		4	L:S::5600 MIL				25 MHZ	34D7< 35C6<
	ENET_PHY_TXD<0..3>		4	L:S:4600:5600				25 MHZ	34C7< 35C6<>
	CLKENET_LINK_TX		4	L:S:4600 MIL:5600 MIL				25 MHZ	34D7< 35C8<
	CLKENET_PHY_TX		4	L:S::1000 MIL				25 MHZ	35C6<>
	CLKENET_LINK_RX		4	L:S:4600 MIL:5600 MIL				25 MHZ	34C7< 35C8<
	CLKENET_PHY_RX		4	L:S::1000 MIL				25 MHZ	35C6<>
	ENET_PHY_RXD<0..3>		4	L:S::1000				25 MHZ	35B6<> 35C6<>
	ENET_PHY_RX_DV		4	L:S::1000 MIL				25 MHZ	35B6<>
	ENET_PHY_RX_ER		4	L:S::1000 MIL				25 MHZ	35B6<>
	ENET_PHY_CRS		4	L:S::1000 MIL				25 MHZ	35B6<>
	ENET_PHY_COL		4	L:S::1000 MIL				25 MHZ	35B6<>
	ENET_LINK_RXD<0..3>		4	L:S:4600:5600				25 MHZ	34C7< 35B8< 35C8<
	ENET_CRS		4	L:S:4600 MIL:5600 MIL				25 MHZ	34C7< 35B8<
	ENET_COL		4	L:S:4600 MIL:5600 MIL				25 MHZ	34B7< 35B8<
	ENET_RX_DV		4	L:S:4600 MIL:5600 MIL				25 MHZ	34C7< 35B8<
	ENET_RX_ER		4	L:S:4600 MIL:5600 MIL				25 MHZ	34C7< 35B8<
	CLK25M_ENET_XIN		3	L:S::1000 MIL	400	8 MIL SPACING		25 MHZ	35B6<
	CLK25M_ENET_XOUT		3	L:S::1000 MIL	400	8 MIL SPACING		25 MHZ	35B6<>
	ENET_TDP	ETHTD:G:L:S:0 MIL:70 MIL		L:S::4000 MIL	3150	10 MIL SPACING	ETH_TXD	100 MHZ	35C3<>
	ENET_TDN	ETHTD:G:L:S:0 MIL:70 MIL		L:S::4000 MIL	3150	10 MIL SPACING	ETH_TXD	100 MHZ	35C3<>
	ENET_RDP	ETHRD:G:L:S:0 MIL:70 MIL		L:S::4000 MIL	3150	10 MIL SPACING	ETH_RXD	100 MHZ	35C3<>
	ENET_RDN	ETHRD:G:L:S:0 MIL:70 MIL		L:S::4000 MIL	3150	10 MIL SPACING	ETH_RXD	100 MHZ	35C3<>
	RJ45_TXP	RJTXD:G:L:S:0 MIL:70 MIL		L:S::750 MIL		2KV_ISO	RJ45_TXD	100 MHZ	35C1<>
	RJ45_TXN	RJTXD:G:L:S:0 MIL:70 MIL		L:S::750 MIL		2KV_ISO	RJ45_TXD	100 MHZ	35C1<>
	RJ45_RXP	RJRXD:G:L:S:0 MIL:70 MIL		L:S::750 MIL		2KV_ISO	RJ45_RXD	100 MHZ	35C1<>
	RJ45_RXN	RJRXD:G:L:S:0 MIL:70 MIL		L:S::750 MIL		2KV_ISO	RJ45_RXD	100 MHZ	35C1<>
	RJ45_TREF					2KV_ISO			35C2<>
	RJ45_RREF					2KV_ISO			35C2<>
	RJ45_4_5					2KV_ISO			35C1<>
	RJ45_7_8					2KV_ISO			35C1<>
	RJ45_F_TREF					2KV_ISO			35B2<
	FW_LINK_DATA<0..7>		4	L:S::1000					34C4<>
	FW_LINK_CNTL<0..1>		4	L:S::1000				49.152 MHZ	34C4<>
	FW_LINK_LREQ		4	L:S::1000 MIL				49.152 MHZ	34C4<>
	FW_SCLK		4	L:S:3500 MIL:4500 MIL				49.152 MHZ	34C5<> 36C8<
	FW_D<0..7>		4	L:S:3700:4700				49.152 MHZ	34C3< 36B8< 36C8<
	FW_CNTL0		4	L:S:3700 MIL:4700 MIL				49.152 MHZ	34C3< 36C8<
	FW_CNTL1		4	L:S:3700 MIL:4700 MIL				49.152 MHZ	34C3< 36C8<
	FW_LREQ		4	L:S:3700 MIL:4700 MIL				49.152 MHZ	34C3< 36C8<
	FW_PHY_SCLK		4	L:S::500 MIL				49.152 MHZ	36C7<>
	FW_PHY_CNTL0		4	L:S::1000 MIL				49.152 MHZ	36C7<>
	FW_PHY_CNTL1		4	L:S::1000 MIL				49.152 MHZ	36C7<>
	FW_PHY_D<0..7>		4	L:S::1000				49.152 MHZ	36B7<> 36C7<>
	FW_XI		3	L:S::1000 MIL	100	8 MIL SPACING		24.576 MHZ	36C6<
	FW_XO		3	L:S::1000 MIL	100	8 MIL SPACING		24.576 MHZ	36C6<>
	FW_BIAS1								36C5<>
	FW_BIAS2								36C5<>
	FW_TPA1P	FWTPA1:G:L:S:0 MIL:50 MIL		L:S::1220 MIL	5000		FW_TPA1	400 MHZ	36C5<>
	FW_TPA1N	FWTPA1:G:L:S:0 MIL:50 MIL		L:S::1220 MIL	5000		FW_TPA1	400 MHZ	36C5<>
	FW_TPB1P	FWTPB1:G:L:S:0 MIL:50 MIL		L:S::1220 MIL	5000		FW_TPB1	400 MHZ	36C5<>
	FW_TPB1N	FWTPB1:G:L:S:0 MIL:50 MIL		L:S::1220 MIL	5000		FW_TPB1	400 MHZ	36C5<>
	FW_TPA2P	FWTPA2:G:L:S:0 MIL:50 MIL		L:S::1220 MIL	5000		FW_TPA2	400 MHZ	36C5<>
	FW_TPA2N	FWTPA2:G:L:S:0 MIL:50 MIL		L:S::1220 MIL	5000		FW_TPA2	400 MHZ	36C5<>
	FW_TPB2P	FWTPB2:G:L:S:0 MIL:50 MIL		L:S::1220 MIL	5000		FW_TPB2	400 MHZ	36C5<>
	FW_TPB2N	FWTPB2:G:L:S:0 MIL:50 MIL		L:S::1220 MIL	5000		FW_TPB2	400 MHZ	36C5<>
	FW_TPO1P	FWTPO1:G:L:S:0 MIL:50 MIL		L:S::1220 MIL	5000		FW_TPO1	400 MHZ	36B8<> 36D1<>
	FW_TPO1N	FWTPO1:G:L:S:0 MIL:50 MIL		L:S::1220 MIL	5000		FW_TPO1	400 MHZ	36A8<> 36D1<>
	FW_TPI1P	FWTPL1:G:L:S:0 MIL:50 MIL		L:S::1220 MIL	5000		FW_TPL1	400 MHZ	36A8<> 36D1<>
	FW_TPI1N	FWTPL1:G:L:S:0 MIL:50 MIL		L:S::1220 MIL	5000		FW_TPL1	400 MHZ	36A8<> 36D1<>
	FW_TPO2P	FWTPO2:G:L:S:0 MIL:50 MIL		L:S::1220 MIL	5000		FW_TPO2	400 MHZ	36A8<> 36C1<>
	FW_TPO2N	FWTPO2:G:L:S:0 MIL:50 MIL		L:S::1220 MIL	5000		FW_TPO2	400 MHZ	36A8<> 36C1<>
	FW_TPI2P	FWTPL2:G:L:S:0 MIL:50 MIL		L:S::1220 MIL	5000		FW_TPL2	400 MHZ	36A8<> 36C1<>
	FW_TPI2N	FWTPL2:G:L:S:0 MIL:50 MIL		L:S::1220 MIL	5000		FW_TPL2	400 MHZ	36A8<> 36C1<>

DIGITAL SIGNALS

GROUP	SIG_NAME	RELATIVE_PROPAGATION_DELAY	MAX_VIAS	STUB_LENGTH	NET_SPACING_TYPE	MIN_LINE_WIDTH MAX_EXPOSED_LENGTH	PULSE_PARAM	
NEW STUFF HERE	TMDS_CKP	TMDS:G:L:S:0 MIL:120 MIL	3	70	8 MIL SPACING	TMDS_CLK		23D1< 24B7<> 27C2< 59A8>
	TMDS_CKM	TMDS:G:L:S:0 MIL:120 MIL	3	70	8 MIL SPACING	TMDS_CLK		23D1< 24A7<> 27C2< 59A8>
	TMDS_D0P	TMDS:G:L:S:0 MIL:120 MIL	3	70	8 MIL SPACING	TMDS_D0		23D1< 24B7<> 27C2< 59B8>
	TMDS_D0M	TMDS:G:L:S:0 MIL:120 MIL	3	70	8 MIL SPACING	TMDS_D0		23D1< 24B7<> 27C2< 59A8>
	TMDS_D1P	TMDS:G:L:S:0 MIL:120 MIL	3	70	8 MIL SPACING	TMDS_D1		23D1< 24C7<> 27C2< 59B8>
	TMDS_D1M	TMDS:G:L:S:0 MIL:120 MIL	3	70	8 MIL SPACING	TMDS_D1		23D1< 24C7<> 27C2< 59B8>
	TMDS_D2P	TMDS:G:L:S:0 MIL:120 MIL	3	70	8 MIL SPACING	TMDS_D2		23D1< 24D7<> 27C2< 59B8>
	TMDS_D2M	TMDS:G:L:S:0 MIL:120 MIL	3	70	8 MIL SPACING	TMDS_D2		23D1< 24D7<> 27C2< 59B8>
	GPU_TMDS_CKP	GTMDS:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING	G_TMDS_CLK		23C2< 23D3<>
	GPU_TMDS_CKM	GTMDS:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING	G_TMDS_CLK		23C2< 23D3<>
	GPU_TMDS_D0P	GTMDS:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING	G_TMDS_D0		23C2< 23D3<>
	GPU_TMDS_D0M	GTMDS:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING	G_TMDS_D0		23C2< 23D3<>
	GPU_TMDS_D1P	GTMDS:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING	G_TMDS_D1		23C2< 23D3<>
	GPU_TMDS_D1M	GTMDS:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING	G_TMDS_D1		23C2< 23D3<>
	GPU_TMDS_D2P	GTMDS:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING	G_TMDS_D2		23C2< 23D3<>
	GPU_TMDS_D2M	GTMDS:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING	G_TMDS_D2		23C2< 23D3<>
	SI_TMDS_CKP	STMDS:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING	S_TMDS_CLK		27C3<>
	SI_TMDS_CKM	STMDS:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING	S_TMDS_CLK		27C3<>
	SI_TMDS_D0P	STMDS:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING	S_TMDS_D0		27C3<>
	SI_TMDS_D0M	STMDS:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING	S_TMDS_D0		27C3<>
	SI_TMDS_D1P	STMDS:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING	S_TMDS_D1		27C3<>
	SI_TMDS_D1M	STMDS:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING	S_TMDS_D1		27C3<>
	SI_TMDS_D2P	STMDS:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING	S_TMDS_D2		27C3<>
	SI_TMDS_D2M	STMDS:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING	S_TMDS_D2		27C3<>
	DVOD0	TMDS_XMIT:G:L:S:0 MIL:400 MIL		200			165MHZ	22C5<> 27A8< 27C5<
	DVOD1	TMDS_XMIT:G:L:S:0 MIL:400 MIL		200			165MHZ	22C5<> 27A8< 27C5<
	DVOD2	TMDS_XMIT:G:L:S:0 MIL:400 MIL		200			165MHZ	22C5<> 26D1< 27C5<
	DVOD3	TMDS_XMIT:G:L:S:0 MIL:400 MIL		200			165MHZ	22B5<> 26D1< 27C5<
	DVOD4	TMDS_XMIT:G:L:S:0 MIL:400 MIL		200			165MHZ	22B5<> 27A8< 27C5<
	DVOD5	TMDS_XMIT:G:L:S:0 MIL:400 MIL		200			165MHZ	22B5<> 27A8< 27C5<
	DVOD6	TMDS_XMIT:G:L:S:0 MIL:400 MIL		200			165MHZ	22B5<> 27A8< 27C5<
	DVOD7	TMDS_XMIT:G:L:S:0 MIL:400 MIL		200			165MHZ	22B5<> 27A8< 27C5<
	DVOD8	TMDS_XMIT:G:L:S:0 MIL:400 MIL		200			165MHZ	22B5<> 26B1< 27C5<
	DVOD9	TMDS_XMIT:G:L:S:0 MIL:400 MIL		200			165MHZ	22B5<> 27A8< 27C5<
	DVOD10	TMDS_XMIT:G:L:S:0 MIL:400 MIL		200			165MHZ	22B5<> 27A8< 27B5<
	DVOD11	TMDS_XMIT:G:L:S:0 MIL:400 MIL		200			165MHZ	22B5<> 27A8< 27B5<

SIGNAL CONSTRAINTS

NOTICE OF PROPRIETARY PROPERTY

LAST_MODIFIED=Wed Sep 17 12:12:40 2003

DIGITAL SIGNALS (CONT'D)

	GROUP	SIG_NAME	RELATIVE_PROPAGATION	MAX_VIAS	PROPAGATION_DELAY	STUB_LENGTH	NET_SPACING_TYPE	MAX_EXPOSED_LENGTH	PULSE_PARAM	
	CD DRIVE BUS	EIDE_RST_L			L:S:3500 MIL:5500 MIL				33 MHZ	37A7> 37D5<
B17		EIDE_DMACK_L			L:S:3500 MIL:5500 MIL				33 MHZ	37A7<> 37D5<
B18		EIDE_STOP			L:S::5500 MIL				33 MHZ	37A7> 37D5<
B19		EIDE_HSTB_RDY			L:S::5500 MIL				33 MHZ	37A7> 37C5<
B20		EIDE_DSTB_RDY			L:S:3500 MIL:5500 MIL				33 MHZ	37A7< 37C5<
B21		EIDE_DATA<0..15>			L:S:3500:5500				33 MHZ	37A5< 37B5< 37B7<> 37C5<
B22		CD_RESET_L			L:S::1000 MIL				33 MHZ	37D4< 38C6<>
B23		CD_DMACK_L			L:S::4000 MIL				33 MHZ	37D4< 38C6<>
B24		CD_STOP			L:S::5000 MIL				33 MHZ	37D4< 38C6<>
B25		CD_HSTB_RDY			L:S::5000 MIL				33 MHZ	37C4< 38C6<>
B26		CD_DSTB_RDY			L:S::1000 MIL				33 MHZ	37C4< 38C6<>
B27		UATAD<0..15>			L:S::1000				33 MHZ	37A4< 37B4< 37C4< 38C6<>
B28		CD_DMARQ			L:S::1000 MIL				33 MHZ	38C6<>
B29		EIDE_DMARQ			L:S:3500 MIL:5500 MIL				33 MHZ	37A7< 38C8<
B30		UATA0IRQ			L:S::1000 MIL				33 MHZ	38C6<>
B31		EIDE_INTRQ			L:S:3500 MIL:5500 MIL				33 MHZ	37A7< 38C8<
B32		CD_EIDE_ADDR<0..2>			L:S::1000				33 MHZ	38C6<>
B33		EIDE_ADDR<0..2>			L:S:3500:5500				33 MHZ	37B7> 38A8< 38B8<
B34		CD_CS1FX_L			L:S::1000 MIL				33 MHZ	38C6<>
B35		EIDE_CS1FX_L			L:S:3500 MIL:5500 MIL				33 MHZ	37A7> 38B8<
B36		CD_CS3FX_L			L:S::1000 MIL				33 MHZ	38C6<>
B37		EIDE_CS3FX_L			L:S:3500 MIL:5500 MIL				33 MHZ	37A7> 38B8<
B38										
	HD DRIVE BUS									
B39		UIDE_RST_L	HD_DATA:G:L:S:0 MIL:5500 MIL		L:S:100 MIL:6000 MIL				100 MHZ	37C7<> 37D3<
B40		UIDE_DMACK_L	HD_DATA:G:L:S:0 MIL:5500 MIL		L:S:100 MIL:6000 MIL				100 MHZ	37C7<> 37D3<
B41		UIDE_DIOR_L	HD_DATA:G:L:S:0 MIL:5500 MIL		L:S:100 MIL:6000 MIL				100 MHZ	37C7<> 37D3<
B42		UIDE_DIOW_L	HD_DATA:G:L:S:0 MIL:5500 MIL		L:S::55000 MIL				100 MHZ	37C3< 37C7<>
B43		UIDE_IOCHRDY	HD_DATA:G:L:S:0 MIL:5500 MIL		L:S:100 MIL:6000 MIL				100 MHZ	37C3< 37C7<
B44		UIDE_DATA<0..15>	HD_DATA:G:L:S:0:5500		L:S:100:6000				100 MHZ	37A3< 37B3< 37C3< 37C7<> 37D7<>
B45		HD_RESET_L			L:S::1000 MIL				100 MHZ	37D1< 38C3<>
B46		HD_DMACK_L			L:S::1000 MIL				100 MHZ	37D1< 38C3<>
B47		HD_DIOR_L			L:S::55000 MIL				100 MHZ	37D1< 38C3<>
B48		HD_DIOW_L			L:S::55000 MIL				100 MHZ	37C1< 38C3<>
B49		HD_IOCHRDY			L:S::1000 MIL				100 MHZ	37C1< 38C3<>
		HD_DMARQ			L:S::1000 MIL				100 MHZ	38C3<>
B50		UIDE_DMARQ	HD_DATA:G:L:S:0 MIL:5500 MIL		L:S:100 MIL:6000 MIL				100 MHZ	37C7<> 38C4<
B51		HD_INTRQ			L:S::1000 MIL				100 MHZ	38C3<>
B52		UIDE_INTRQ	HD_DATA:G:L:S:0 MIL:5500 MIL		L:S:100 MIL:6000 MIL				100 MHZ	37C7< 38C4<
B53		HD_UIDE_ADDR<0..2>			L:S::1000				100 MHZ	38C2<> 38C3<>
B54		UIDE_ADDR<0..2>	HD_DATA:G:L:S:0:5500		L:S:100:6000				100 MHZ	37C7<> 38A4< 38B4<
B55		HD_UIDE_CS1FX_L			L:S::6000 MIL				100 MHZ	38C3<>
B56		UIDE_CS1FX_L	HD_DATA:G:L:S:0 MIL:5500 MIL		L:S:100 MIL:6000 MIL				100 MHZ	37C7<> 38B4<
B57		HD_UIDE_CS3FX_L			L:S::6000 MIL				100 MHZ	38C2<>
B58		UIDE_CS3FX_L	HD_DATA:G:L:S:0 MIL:5500 MIL		L:S:100 MIL:6000 MIL				100 MHZ	37C7<> 38B4<
B59										
B60		CLK_18M_INT_XOUT	3		L:S::1000	100	8 MIL SPACING		18.432 MHZ	58B5>
B61		CLK_18M_INT_XOUT	3		L:S::1000	100	8 MIL SPACING		18.432 MHZ	58B5>
B62		CLK_18M_INT_XOUT	3		L:S::200	50	8 MIL SPACING		18.432 MHZ	58B5>
B63		USB_DAP	USBA:G:L:S:0 MIL:500 MIL							28A3< 28B3<>
B64		USB_DAN	USBA:G:L:S:0 MIL:500 MIL							28A3< 28B3<>
B65		USB_DAP_F	USBA_F:G:L:S:0 MIL:500 MIL			100				28B2< 33B7<
B66		USB_DAN_F	USBA_F:G:L:S:0 MIL:500 MIL			100				28B2< 33B7<
B67		USB_DBP	USBB:G:L:S:0 MIL:500 MIL							28A3< 28B3<>
B68		USB_DBN	USBB:G:L:S:0 MIL:500 MIL							28A3< 28B3<>
B69		USB_DBP_F	USBB_F:G:L:S:0 MIL:500 MIL			100				28B2< 33C7<
B70		USB_DBN_F	USBB_F:G:L:S:0 MIL:500 MIL			100				28B2< 33C7<
B71		USB_DCP	USBC:G:L:S:0 MIL:500 MIL							28A3< 28B3<>
B72		USB_DCN	USBC:G:L:S:0 MIL:500 MIL							28A3< 28B3<>
B73		USB_DCP_F	USBC_F:G:L:S:0 MIL:500 MIL			100				28B2< 33D7<
B74		USB_DCN_F	USBC_F:G:L:S:0 MIL:500 MIL			100				28B2< 33D7<
B75		USB_DEP	USBE:G:L:S:0 MIL:500 MIL							28B3<>
B76		USB_DEN	USBE:G:L:S:0 MIL:500 MIL							28B3<>
B77		BT_USB_DP	USBE_F:G:L:S:0 MIL:500 MIL			100				28B2< 29D3<> 59B6>
B78		BT_USB_DM	USBE_F:G:L:S:0 MIL:500 MIL			100				28B2< 29D3<> 59B6>
B79		USB_DFP	USBF:G:L:S:0 MIL:500 MIL							28B3<>
B80		USB_DFN	USBF:G:L:S:0 MIL:500 MIL							28B3<>
B81		MODEM_USB_DP	USBF_F:G:L:S:0 MIL:500 MIL			100				28B2< 29C5<> 59B6>
B82		MODEM_USB_DM	USFE_F:G:L:S:0 MIL:500 MIL			100				28B2< 29C5<> 59B6>
B83										
B84		PMU_XO		3	L:S::1000 MIL	100	8 MIL SPACING		10 MHZ	44B5<
B85		PMU_XI		3	L:S::1000 MIL	100	8 MIL SPACING		10 MHZ	44B5<
B86		PMU_XT		3	L:S::300 MIL	50	8 MIL SPACING		10 MHZ	44A6<
B87		PMU_CLKOUT		3	L:S::1000 MIL	100	8 MIL SPACING		32.768 MHZ	44B4<>
B88		PMU_CLKIN		3	L:S::1000 MIL	100	8 MIL SPACING		32.768 MHZ	44B4<>
B84		PMU_CLKT		3	L:S::300 MIL	50	8 MIL SPACING		32.768 MHZ	44B2<>
B89		MICSHLD					10 MIL SPACING			29A5<> 43A8< 59A8>
B90		MICHIGH					10 MIL SPACING			29A5<> 43B8< 59A8>
B91		MICLOW					10 MIL SPACING			29A5<> 43A8< 59A8>
B92		KS_INT_SPKR+					10 MIL SPACING			29A3< 43D7< 59B8>
B93		KS_INT_SPKR-					10 MIL SPACING			29A3< 42B4< 43D7< 59B8>

	SIG_NAME	PROPAGATION_DELAY	PULSE_PARAM	
E1	T_UD_IDEDD_0	L:S::1000 MIL	100 MHZ	37C1< 38C3<>
E2	T_UD_IDEDD_1	L:S::1000 MIL	100 MHZ	37C1< 38C3<>
E3	T_UD_IDEDD_2	L:S::1000 MIL	100 MHZ	37C1< 38C3<>
E4	T_UD_IDEDD_3	L:S::1000 MIL	100 MHZ	37C1< 38C3<>
E5	T_UD_IDEDD_4	L:S::1000 MIL	100 MHZ	37B1< 38C3<>
E6	T_UD_IDEDD_5	L:S::1000 MIL	100 MHZ	37B1< 38C3<>
E7	T_UD_IDEDD_6	L:S::1000 MIL	100 MHZ	37B1< 38C3<>
E8	T_UD_IDEDD_7	L:S::1000 MIL	100 MHZ	37B1< 38C3<>
E9	T_UD_IDEDD_8	L:S::1000 MIL	100 MHZ	37B1< 38C2<>
E10	T_UD_IDEDD_9	L:S::1000 MIL	100 MHZ	37B1< 38C2<>
E11	T_UD_IDEDD_10	L:S::1000 MIL	100 MHZ	37B1< 38C2<>
E12	T_UD_IDEDD_11	L:S::1000 MIL	100 MHZ	37B1< 38C2<>
E13	T_UD_IDEDD_12	L:S::1000 MIL	100 MHZ	37B1< 38C2<>
E14	T_UD_IDEDD_13	L:S::1000 MIL	100 MHZ	37A1< 38C2<>
E15	T_UD_IDEDD_14	L:S::1000 MIL	100 MHZ	37A1< 38C2<>
E16	T_UD_IDEDD_15	L:S::1000 MIL	100 MHZ	37A1< 38C2<>

SIGNAL CONSTRAINTS

APPLE COMPUTER INC.
SIZE D | DRAWING NUMBER 051-6497 | REV. 13
SCALE NONE | SHT 58 OF 69
DRAWING

FUNC_TEST

+1_8V_MAIN
+12V_MAIN
+12V_SLEEP
+12V_SLEEPA
+5V_MAIN
+5V_SLEEP
+2_5V_MAIN
+3V_MAIN
CPU_VCORE_SLEEP
JTAG_ASIC_TCK
JTAG_ASIC_TDI
JTAG_ASIC_TDO
JTAG_ASIC_TMS
JTAG_ASIC_TRST_L
INT_TMDS_3V
+1_5V_AGP
FAN_12V_FILT
+INTREPID_CORE_MAIN
INTREPID_VSENSE
OVDD_ADJ
CPU_CHKSTP_OUT_L
CPU_CHKSTP_IN_L
CPU_HRESET_L
JTAG_CPU_TCK
JTAG_CPU_TDI
JTAG_CPU_TDO
JTAG_CPU_TMS
JTAG_CPU_TRST_L
+MAXBUS_SLEEP
ROM_CS_L
ROM_OE_L
ROM_RW_L
DDC_VCC_3
DDC_VCC_5
SND_HP_SENSE_L
ANALOG_HSYNC*
ANALOG_VSYNC*
FILT_ANALOG_BLU
FILT_ANALOG_RED
FILT_ANALOG_GRN
GND
KS_INT_SPKR+
KS_INT_SPKR-
TMDS_D2P
TMDS_D2M
TMDS_D1P
TMDS_D1M
TMDS_D0P
TMDS_D0M
TMDS_CKP
TMDS_CKM
INV_CUR_HI_FILT
IO_RESET_L
KS5VSD
INT_I2C_CLK2
INT_I2C_DATA2
INT_ANALYZER_CLK
LAMP_STS_FILT
LCD_PWM_FILT
LED_5V_FILT
LED_RET_FILT
MICSHLD
MICHIGH
MICLOW
COMM_RESET_L
IIC_ADD
ROM_WP_L

FUNC_TEST

COMM_SHUTDOWN
MON_DETECT
FLO_KNOWS_BEST
NMI_BUTTON*
PWR_SWITCH*
PMU_RST*
PMURESETBUTTON*
PWR_SWITCH*
PWR_UP
POWER_UP*
RESET_BUTTON*
COMM_RING_DET_L
ROM_ONBOARD_CS_L
COMM_DTR_L
COMM_TXD_L
COMM_TRXC
COMM_RTS_L
COMM_RXD
COMM_GPIO_L
SLEEP
CPU_SRESET_L
PMU_AVCC
TMDS_DDC_CLK
TMDS_DDC_DAT
USB_DCN_CON
USB_DCP_CON
USB_DBN_CON
USB_DBP_CON
USB_DAN_CON
USB_DAP_CON
BT_USB_DP
BT_USB_DM
MODEM_USB_DP
MODEM_USB_DM
USB_PORT_PWR
VGA_IIC_CLK
VGA_IIC_DAT
CPU_VCORE_SLEEP
LINE_IN_COM
LINE_IN_R
LINE_IN_SENSE
LINE_IN_L
SND_LIN_SENSE_L
OUT_R FUNC_TEST
LINEOUT_COMM2 FUNC_TEST
LINE_OUT_L FUNC_TEST
PCIT_IRDY_L
RF_CLKRUN_L
NC_RF_DISABLE_L FUNC_TEST
PCI_DEVSEL_L
PCI_STOP_L
PCI_TRDY_L
PCI_FRAME_L
PCI_PAR
WL_PCI_IDSEL
33SLOTB_INT_L
PMU_PME_L
PCI_SLOTB_GNT_L
CLK33M_PCI_SLOTB
PCI_SLOTB_REQ_L
MAIN_RESET_L
PCI_CBE<0>
PCIT_CBE<1>
PCIT_CBE<2>
PCIT_CBE<3>
UNUSED_GPIO15

FUNC_TEST

PCI_AD<0>
PCIT_AD<1>
PCIT_AD<2>
PCIT_AD<3>
PCI_AD<4>
PCIT_AD<5>
PCI_AD<6>
PCIT_AD<7>
PCIT_AD<8>
PCI_AD<9>
PCIT_AD<10>
PCI_AD<11>
PCIT_AD<12>
PCI_AD<13>
PCIT_AD<14>
PCI_AD<15>
PCI_AD<16>
PCIT_AD<17>
PCI_AD<18>
PCIT_AD<19>
PCI_AD<20>
PCIT_AD<21>
PCI_AD<22>
PCIT_AD<23>
PCI_AD<24>
PCIT_AD<25>
PCI_AD<26>
PCIT_AD<27>
PCIT_AD<28>
PCIT_AD<29>
PCI_AD<30>
PCIT_AD<31>

CONSTRINT TABLES

LAST_MODIFIED=Wed Sep 17 12:12:42 2003

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6497	13
SCALE: NONE	SHT 59 OF 69	

DRAWING

```
*** Signal Cross-Reference for the entire design ***

+1_5V_AGP        10D6< 11A6< 16A8< 16C2< 16D7<
                 17A3< 17A4< 17D5< 46B4<> 52C3> 59C8>


+1_5V_INTREPID_PLL  9D4< 16D6< 28D6<> 30D5< 52D3>
+1_5V_INTREPID_PLL1  28C4< 52D3>
+1_5V_INTREPID_PLL2  28D4< 52D3>
+1_5V_INTREPID_PLL3  28D4< 52D3>
+1_5V_INTREPID_PLL4  28D4< 52D3>
+1_5V_INTREPID_PLL5  16D5< 52D3>
+1_5V_INTREPID_PLL6  30D4< 52D3>
+1_5V_INTREPID_PLL7  9D2< 52D3>
+1_5V_INTREPID_PLL8  28D4< 52D3>
+1_8V_MAIN        52C4 59D8>
+2_5V_MAIN        30B3< 49B2<> 52C4 59D8>
+3.3VFPD          24D7< 51C1<> 52B6>
+3V_AUDIO         39D2< 39D6< 39D7< 40C3< 43B2<
                 43C6<
+3V_GPU_SS        22A6< 22A8< 22B7<
+3V_INTREPID_USB  28C4< 52A3>
+3V_MAIN          39D4< 40D5< 41A5< 41A7< 42B5<
                 42B7< 42C8< 43C7< 52C4 59D8>
+5VSD_T           50D6<>
+5V_AUDIO         39C6<> 39D7< 41B6<>
+5V_HP            41A8< 41B7<> 41D5<
+5V_MAIN          51B4<> 51B4<> 52C4 59D8>
+5V_SLEEP         38C1< 46C7< 46D6<> 50D5< 51C5<>
                 51C8< 59D8>
+12VSD_FILT       29A5<> 52B3>
+12VSD_T          50D6<>
+12V_DROPPED      44D8<
+12V_MAIN         36D8< 39C8< 42B3< 44D8< 45B4<>
                 45D3<> 45D7< 48C4<> 48C8<> 48D6<>
                 49C4<> 49D3<> 49D7<> 50B4<> 50C4<>
                 50D2< 50D5<> 51A5< 51A7< 51B7< 51C3<
                 51D7<> 52C1> 52C1> 59D8>
+12V_SLEEP        29A3< 29A8< 29C5<> 50D5< 51A5<
                 51C2< 51D6<> 52C1> 52C1> 59D8>
+12V_SLEEPA      59D8>
+12V_TPA         42B2< 42B7< 42C4< 42C5< 42D5<
+INTREPID_CORE_MAIN  10D6< 11D3< 46B3< 47B2<> 59C8>


+MAXBUS_SLEEP    4D5< 6C5< 6D6< 7A3< 7A3< 7B3< 7C3<
                 7C3< 7C5< 7C7< 8A3<> 8D1< 8D4< 9B7<
                 9D8< 44B7< 44D1< 44D2< 45D2<> 46D4<
                 52C6> 59C8>
3.8VH_TRICKLE    44C1< 44D7<> 52B3>
3.8V_TRICKLE     36D8< 44C2< 44C6< 44D7<> 50D5<
                 52C1> 52C2>
3V_SI_AVCC       27D4<
3V_SI_PLLVCC     27D4<
3V_SI_VCC        27B2< 27D3<
3_5_HONKER       51C4<>
3_6V_SLEEP       37D1< 51C1<
5V_XRA           50B4<>
15_I282          15B2<
15_I286          15B3<
18P_GND          29B5<>
25V_BSTH         49C5<>
25V_BSTH_TERM    49C5<>
25V_COMP         49B6<
25V_COMP_DWN     49B6<
25V_DH           49B5<>
25V_DHT          49B5<>
25V_DL           49B5<>
25V_DLT          49B4<>
25V_GND          49B6<>
25V_OCSET        49C5<>
25V_OVP          49B6<>
25V_VCC          49C6<
25V_VPWR         49B5<> 49C4<>
25V_VPWRA        49B4<>
25V_VSENSE       49C4<>
25_CORE_1        49C3<
33PCI_SLOTD_SERR_L  32B6<>
33SLOTB_INT_L    28B7<> 28B7<> 28B7<> 31C2<> 59A6>
42_I291          42B6<
42_I295          42B5<
45_I408          45B6<
45_I525          45C4<
45_I526          45B3<
47_I66           47B4<
48_I10           48C3<
48_I99           48B4<
49_I70           49B4<
50_I408          50B3<
50_I410          50A3<
AGND             39B7<> 52C4
AGP_AD<0>        16C4<> 17D8<
AGP_AD<0..15>    54C7<
AGP_AD<1>        16C4<> 17D8<
AGP_AD<2>        16C4<> 17D8<
AGP_AD<3>        16C4<> 17D8<
AGP_AD<4>        16C4<> 17D8<
AGP_AD<5>        16C4<> 17D8<
AGP_AD<6>        16C4<> 17D8<
AGP_AD<7>        16C4<> 17D8<
AGP_AD<8>        16C4<> 17D8<
AGP_AD<9>        16C4<> 17D8<
AGP_AD<10>       16C4<> 17D8<
AGP_AD<11>       16C4<> 17D8<
AGP_AD<12>       16C4<> 17D8<
AGP_AD<13>       16C4<> 17D8<
AGP_AD<14>       16C4<> 17D8<
AGP_AD<15>       16C4<> 17C8<
AGP_AD<16>       16C4<> 17C8<
AGP_AD<16..31>   54C7<
AGP_AD<17>       16C4<> 17C8<
AGP_AD<18>       16C4<> 17C8<

AGP_AD<19>       16C4<> 17C8<
AGP_AD<20>       16C4<> 17C8<
AGP_AD<21>       16C4<> 17C8<
AGP_AD<22>       16C4<> 17C8<
AGP_AD<23>       16C4<> 17C8<
AGP_AD<24>       16B4<> 17C8<
AGP_AD<25>       16B4<> 17C8<
AGP_AD<26>       16B4<> 17C8<
AGP_AD<27>       16B4<> 17C8<
AGP_AD<28>       16B4<> 17C8<
AGP_AD<29>       16B4<> 17C8<
AGP_AD<30>       16B4<> 17C8<
AGP_AD<31>       16B4<> 17C8<
AGP_AD_STB<0>    16A4<> 16B3< 17B8< 54C7<
AGP_AD_STB<1>    16A4<> 16B3< 17B8< 54C7<
AGP_AD_STB_GPUUF<0>  17B6< 54B7<
AGP_AD_STB_GPUUF<1>  17B6< 54B7<
AGP_AD_STB_L<0>  16A4<> 16D1< 17B8< 54C7<
AGP_AD_STB_L<1>  16A4<> 16D1< 17B8< 54C7<
AGP_AD_STB_L_GPUUF<0>  17B6< 54B7<
AGP_AD_STB_L_GPUUF<1>  17B6< 54B7<
AGP_BUSY_L       16C6<> 16D1< 16D3< 17A8> 54B7<
AGP_CBE<0>       16B4<> 17C8<
AGP_CBE<0..1>    54C7<
AGP_CBE<1>       16B4<> 17C8<
AGP_CBE<2>       16B4<> 17C8<
AGP_CBE<2..3>    54C7<
AGP_CBE<3>       16B4<> 17C8<
AGP_DEVSEL_L     16B4<> 16C3< 17B8< 54C7<
AGP_FBI_EQUAL    16C7< 54A7<
AGP_FBO_EQUAL    16B7< 54A7<
AGP_FB_PLUS2     16B8< 54A7<
AGP_FRAME_L      16B4<> 16C3< 17B8< 54C7<
AGP_GNT_L        16C3< 16C4<> 17B7< 54B7<
AGP_INT_L        17B6<> 28B5<> 28B8<
AGP_IRDY_L       16B4<> 16C3< 17B8< 54C7<
AGP_PAR          16B4<> 17B8< 54B7<
AGP_PIPE_L       16A4<> 16B3< 17B8< 54B7<
AGP_PLLVDD       17C5<
AGP_PWR_ADJ      46A5<>
AGP_RBF_L        16A4<> 16B3< 17B8< 54B7<
AGP_REQ_L        16C3< 16C4<> 17B7<> 54B7<
AGP_RESET_L      17B8< 27C5< 44D3<
AGP_SBA<0>       16B4< 16C1< 17A8<
AGP_SBA<0..7>    54B7<
AGP_SBA<1>       16B4<> 16C1< 17A8<
AGP_SBA<2>       16B1< 16B4<> 17A8<
AGP_SBA<3>       16B4<> 16C1< 17A8<
AGP_SBA<4>       16B4<> 16C1< 17A8<
AGP_SBA<5>       16B4<> 16C1< 17A8<
AGP_SBA<6>       16A4<> 16B1< 17A8<
AGP_SBA<7>       16A4<> 16B1< 17A8<
AGP_SB_STB       16A4<> 16B3< 17B8< 54B7<
AGP_SB_STB_L     16A4<> 16D1< 17A8< 54B7<
AGP_ST<0>        16A4<> 16B1< 17B6<
AGP_ST<0..2>     54B7<
AGP_ST<1>        16A4<> 16B1< 17B6<
AGP_ST<2>        16A4<> 16B1< 17B6<
AGP_STOP_L       16B3< 16B4<> 17B8< 54C7<
AGP_TRDY_L       16B3< 16B4<> 17B8< 54C7<
AGP_WBF_L        16A6<> 16B1< 17B8< 54B7<
AINLM            39C4<
AINLP            39C4<
AINRM            39C4<
AINRP            39C4<
ALTCHGND         25B3<> 25C3< 33B2< 33B4< 33C2<
                 33C4< 33C4< 33D2< 33D4< 36A7<> 36B2<
                 36B6< 36B6<> 36C1<> 36C1<> 36C1<
                 52C4
ANALOGGND          35B1< 35C1<> 40B5<> 40B6< 40C6<
                 40C6< 41A2<> 41A4< 41B1<> 41B3<
                 41C3< 41D3< 42A5<> 42A6<> 43A5< 52C4


ANALOG_BLU       22C7<> 25C6< 57D5>
ANALOG_GRN       22C7<> 25C6< 57D5>
ANALOG_HSYNC*    22D7< 25D6<> 26B5< 57D5> 59B8>
ANALOG_RED       22C7<> 25B6< 57D5>
ANALOG_VSYNC*    22D7< 25C6<> 26B5< 57D5> 59B8>
ANEN             35C4<
AOUTL            39C2> 41D7< 43D3<
AOUTR            39C2> 41C7< 43D3<
ASH              43A6<
AUDIO_TO_SND     28B1< 39C1<
AUD_GND          39B7<> 42B2< 42C4< 42D3< 42D4<
                 42D6< 42D7< 43C2< 43D2< 43D4<
AUD_R_FB         39D6<
BRE              45C5<>
BRE_1            45B5<>
BT1              44D6<> 51A6<
BT1_LED          51A6<
BT_USB_DM        28B2< 29D3<> 58A5> 59B6>
BT_USB_DP        28B2< 29D3<> 58B5> 59B6>
C412P1           41B3<
C756_2           40D3<>
C4237P2          40C4<
C4240P2          40C4<
C4242P2          40B4<
C4243P2          40B4<
CAP_PLL          39B4<
CD_CS1FX_L       38C6<> 58C5>
CD_CS3FX_L       38C6<> 58C5>
CD_DMACK_L       37D4< 38C6<> 58D5>
CD_DMARQ         38C6<> 58D5>
CD_DSTB_RDY      37C4< 38C6<> 58D5>
CD_EIDE_ADDR<0>  38C6<>
CD_EIDE_ADDR<0..2>  58C5>
CD_EIDE_ADDR<1>  38C6<>
CD_EIDE_ADDR<2>  38C6<>
CD_HSTB_RDY      37C4< 38C6<> 58D5>
CD_RESET_L       37D4< 38C6<> 58D5>

CD_STOP          37D4< 38C6<> 58D5>
CHGND            24B3< 29A3< 43A7< 43B7< 52C4
CHOC_BROWNIE     51B2<
CLK18M_INT_EXT   28B6<>
CLK18M_INT_XIN   28A5<
CLK18M_INT_XO    28A6<
CLK18M_INT_XOUT  28A5<>
CLK25M_ENET_XIN  35B6< 57B5>
CLK25M_ENET_XOUT  35B6<> 57B5>
CLK27M_MEM_SS    22A6<>
CLK33M_PCI_SLOTB  30D7  31C2<> 54D7< 59A6>
CLK33M_PCI_SLOTB_UF  30D5<> 54D7<
CLK33M_PCI_SLOTC_UF  30D5<> 54D7<
CLK33M_PCI_SLOTD  30D7< 32A6< 54A7<
CLK33M_PCI_SLOTD_UF  30D5<> 54D7<
CLK66M_GPU_AGP   16D8< 17C7< 54A7<
CLK66M_GPU_UF    16C6<> 54A7<
CLKENET_LINK_GBE_REF  34C6<
CLKENET_LINK_RX  34C7< 35C8< 57C5>
CLKENET_LINK_TX  34D7< 35C8< 57C5>
CLKENET_PHY_RX   35C6<> 57C5>
CLKENET_PHY_TX   35C6<> 57C5>
CLKFW_LINK_LCLK  34C5<>
CLK_18M_INT_XOUT  58B5> 58B5> 58B5>
COMM_DTR_L       28C3<> 29C7<> 59C6>
COMM_GPIO_L      28C3<> 28D3< 29C5<> 59C6>
COMM_RESET_L     28C5<> 29D5<> 59A8>
COMM_RING_DET_L  28B5<> 28B8< 29C5<> 44C5<> 59D6>
COMM_RTS_L       28C3> 29D5<> 59C6>
COMM_RXD         28C3<> 29C5<> 59C6>
COMM_SHUTDOWN    28C5<> 28D1< 29D7<> 59D6>
COMM_TRXC        28C3<> 28D3< 29C7<> 59C6>
COMM_TXD_L       28C3<> 29C7<> 59C6>
CORE_MOSFET      45C4<> 45C6<>
CORE_MOSFET_1    45B5<> 45C7<>
CPU_AACK_L       4A7< 7B7< 8B5<> 9B3<> 56C3>
CPU_ADDR<0>      4C7<> 8B4<> 9D3<>
CPU_ADDR<0..31>  56D3>
CPU_ADDR<1>      4C7<> 8B5<> 9D3<>
CPU_ADDR<2>      4C7<> 8B4<> 9D3<>
CPU_ADDR<3>      4C7<> 8B8<> 9D3<>
CPU_ADDR<4>      4C7<> 8B5<> 9D3<>
CPU_ADDR<5>      4C7<> 8B7<> 9D3<>
CPU_ADDR<6>      4C7<> 8C4<> 9D3<>
CPU_ADDR<7>      4C7<> 8B7<> 9D3<>
CPU_ADDR<8>      4C7<> 8C5<> 9D3<>
CPU_ADDR<9>      4C7<> 8B8<> 9C3<>
CPU_ADDR<10>     4C7<> 8B8<> 9C3<>
CPU_ADDR<11>     4C7<> 8C4<> 9C3<>
CPU_ADDR<12>     4C7<> 8B7<> 9C3<>
CPU_ADDR<13>     4C7<> 8B8<> 9C3<>
CPU_ADDR<14>     4C7<> 8B7<> 9C3<>
CPU_ADDR<15>     4C7<> 8B7<> 9C3<>
CPU_ADDR<16>     4C7<> 8B8<> 9C3<>
CPU_ADDR<17>     4C7<> 8B8<> 9C3<>
CPU_ADDR<18>     4C7<> 8C8<> 9C3<>
CPU_ADDR<19>     4C7<> 8B7<> 9C3<>
CPU_ADDR<20>     4C7<> 8B8<> 9C3<>
CPU_ADDR<21>     4C7<> 8C7<> 9C3<>
CPU_ADDR<22>     4C7<> 8C7<> 9C3<>
CPU_ADDR<23>     4C7<> 8C8<> 9C3<>
CPU_ADDR<24>     4B7<> 8B7<> 9C3<>
CPU_ADDR<25>     4B7<> 8B8<> 9C3<>
CPU_ADDR<26>     4B7<> 8C8<> 9C3<>
CPU_ADDR<27>     4B7<> 8C8<> 9C3<>
CPU_ADDR<28>     4B7<> 8C7<> 9C3<>
CPU_ADDR<29>     4B7<> 8C8<> 9C3<>
CPU_ADDR<30>     4B7<> 8C7<> 9C3<>
CPU_ADDR<31>     4B7<> 8C7<> 9C3<>
CPU_ARTRY_L      4A7<> 7C7< 8B8<> 9B3<> 56C3>
CPU_AVDD         4D3< 52C6>
CPU_BG_L         4D7< 7B7< 8B4<> 9D3<> 56D3>
CPU_BR_L         4D7> 7C7< 8B4<> 9D3< 56D3>
CPU_BUS_VSEL     4D3< 7C4<
CPU_CHKSTP_IN_L  4B3< 7B5< 59C8>
CPU_CHKSTP_OUT_L  4B3> 7B5< 8A3<> 8D5<> 59C8>
CPU_CI_L         4A7> 7A7< 8C5<> 9C3<> 56C3>
CPU_CLK_EN       9A3< 44C4<>
CPU_DATA<0>      5D4<> 8C4<> 9D1<>
CPU_DATA<0..63>  56D3>
CPU_DATA<1>      5D4<> 8C7<> 9D1<>
CPU_DATA<2>      5D4<> 8C8<> 9D1<>
CPU_DATA<3>      5D4<> 8C5<> 9D1<>
CPU_DATA<4>      5D4<> 8C7<> 9D1<>
CPU_DATA<5>      5D4<> 8C8<> 9D1<>
CPU_DATA<6>      5D4<> 8C4<> 9D1<>
CPU_DATA<7>      5D4<> 8C8<> 9D1<>
CPU_DATA<8>      5D4<> 8C5<> 9D1<>
CPU_DATA<9>      5D4<> 8C4<> 9D1<>
CPU_DATA<10>     5D4<> 8C7<> 9D1<>
CPU_DATA<11>     5C4<> 8C5<> 9D1<>
CPU_DATA<12>     5C4<> 8C5<> 9D1<>
CPU_DATA<13>     5C4<> 8C7<> 9D1<>
CPU_DATA<14>     5C4<> 8C8<> 9D1<>
CPU_DATA<15>     5C4<> 8C5<> 9D1<>
CPU_DATA<16>     5C4<> 8C4<> 9C1<>
CPU_DATA<17>     5C4<> 8C7<> 9C1<>
CPU_DATA<18>     5C4<> 8C4<> 9C1<>
CPU_DATA<19>     5C4<> 8C4<> 9C1<>
CPU_DATA<20>     5C4<> 8C4<> 9C1<>
CPU_DATA<21>     5C4<> 8C8<> 9C1<>
CPU_DATA<22>     5C4<> 8C7<> 9C1<>
CPU_DATA<23>     5C4<> 8C8<> 9C1<>
CPU_DATA<24>     5C4<> 8D4<> 9C1<>
CPU_DATA<25>     5C4<> 8D7<> 9C1<>
CPU_DATA<26>     5C4<> 8C5<> 9C1<>
CPU_DATA<27>     5C4<> 8C7<> 9C1<>
CPU_DATA<28>     5C4<> 8D8<> 9C1<>
CPU_DATA<29>     5C4<> 8C8<> 9C1<>
CPU_DATA<30>     5C4<> 8C5<> 9C1<>

CPU_DATA<31>     5C4<> 8D7<> 9C1<>
CPU_DATA<32>     5C4<> 8D7<> 9B7< 9C1<>
CPU_DATA<33>     5C4<> 8D8<> 9B7< 9C1<>
CPU_DATA<34>     5C4<> 8D8<> 9B7< 9C1<>
CPU_DATA<35>     5C4<> 8D7<> 9B7< 9C1<>
CPU_DATA<36>     5C4<> 8D4<> 9A7< 9C1<>
CPU_DATA<37>     5B4<> 8D5<> 9C1<>
CPU_DATA<38>     5B4<> 8D5<> 9C1<>
CPU_DATA<39>     5B4<> 8D5<> 9C1<>
CPU_DATA<40>     5B4<> 6C4< 8D7<> 9C1<>
CPU_DATA<41>     5B4<> 6C4< 8C4<> 9C1<>
CPU_DATA<42>     5B4<> 6C4< 8C5<> 9B1<>
CPU_DATA<43>     5B4<> 6C4< 8C4< 9B1<>
CPU_DATA<44>     5B4<> 6C4< 8C8<> 9B1<>
CPU_DATA<45>     5B4<> 6C4< 8C7<> 9B1<>
CPU_DATA<46>     5B4<> 6C4< 8C4<> 9B1<>
CPU_DATA<47>     5B4<> 6C4< 8C7< 9B1<>
CPU_DATA<48>     5B4<> 8C5<> 9B1<> 9D8<
CPU_DATA<49>     5B4<> 8C4<> 9B1<> 9D8<
CPU_DATA<50>     5B4<> 8C8<> 9B1<> 9D8<
CPU_DATA<51>     5B4<> 8C8<> 9B1<> 9D8<
CPU_DATA<52>     5B4<> 8C5<> 9B1<> 9C8<
CPU_DATA<53>     5B4<> 8C7<> 9B1<> 9C8<
CPU_DATA<54>     5B4<> 8D7<> 9B1<> 9C8<
CPU_DATA<55>     5B4<> 8C5<> 9B1<> 9C8<
CPU_DATA<56>     5B4<> 8D8<> 9B1<>
CPU_DATA<57>     5B4<> 8D5<> 9B1<> 9D5<
CPU_DATA<58>     5B4<> 8D4<> 9B1<> 9D5<
CPU_DATA<59>     5B4<> 8D8<> 9B1<> 9D5<
CPU_DATA<60>     5B4<> 8D8<> 9B1<> 9D5<
CPU_DATA<61>     5B4<> 8D4<> 9B1<> 9C5<
CPU_DATA<62>     5B4<> 8D4<> 9B1<> 9C5<
CPU_DATA<63>     5A4<> 8D5<> 9B1<> 9C5<
CPU_DBG_L        4C3< 7B7< 8B8<> 9B1<> 56C3>
CPU_DRDY_L       4C2< 7B7< 8B5<> 9B1< 56C3>
CPU_DRDY_L_UF    4C3<> 56C3>
CPU_DTI<0>       4C3< 8B7<> 9A1<>
CPU_DTI<0..2>    56C3>
CPU_DTI<1>       4C3< 8B4<> 9A1<>
CPU_DTI<2>       4C3< 8B4<> 9A1<>
CPU_EDTI         4C3< 7C5<
CPU_EMODE0_L     4B3< 7A4<
CPU_EMODE1_L     4B3< 7A4<
CPU_FBI_PLUS1    9A5< 56C3>
CPU_FBO_PLUS1    9A5< 56C3>
CPU_FB_MINUS3    9A4< 56C3>
CPU_FB_PLUS2     9A5< 56C3>
CPU_FB_PLUS3     9A4< 56B3>
CPU_GBL_L        4B8<> 8B5<> 56C3>
CPU_HDRST_L      44C4<>
CPU_HIT_L        4A7> 7C7< 8B8<> 9B3< 56C3>
CPU_HRESET_L     4B3< 7A3< 7A5< 7B3< 7B3< 8A3<>
                44C2< 44D2< 59C8>
CPU_INT_GBL_L    4B8< 7B7< 9C3<> 56C3>
CPU_L1TSTCLK     4C3< 7B4<
CPU_L2TSTCLK     4C3< 7C4<
CPU_LSSD_MODE    4C3< 7B5<
CPU_MCP_L        4B3< 7B5<
CPU_PLL_CFG<0>   4D3< 6C6< 8A8<>
CPU_PLL_CFG<1>   4D3< 6C6< 8A8<>
CPU_PLL_CFG<2>   4D3< 6C6< 8A8<>
CPU_PLL_CFG<3>   4C3< 6C6< 8A8<>
CPU_PLL_CFGEXT   4C3< 6C6< 8A8<>
CPU_PLL_STOP     6B8< 44B8<
CPU_PMONIN_L     4B3< 7C5<
CPU_PULLDOWN     4A3< 4D7<> 7C5<
CPU_PULLUP       4A3< 7A5<
CPU_QACK_L       4C3< 8B4<> 9B3<> 56C3>
CPU_QREQ_L       4C3> 7D5< 8B7<> 9B3< 56C3>
CPU_SHD0_L       4A7<> 7B5<
CPU_SHD1_L       4A7<> 7B5<
CPU_SLEEPIN      51B7<
CPU_SMI_L        4B3< 7A5< 44C4<>
CPU_SRESET_L     4B3< 7A5< 8A3<> 59C6>
CPU_STATE_LED*   44C4<> 51A8<
CPU_TA_L         4C3< 7C7< 8C4<> 9A1<> 56C3>
CPU_TBEN         4C3< 7C5< 9A3<>
CPU_TBST_L       4B7> 7B7< 8B4<> 9B3<> 56D3>
CPU_TEA_L        4C3< 7B7< 8B5<> 9A1<> 56C3>
CPU_TSIZ<0>      4B7> 8B5<> 9B3<>
CPU_TSIZ<0..2>   56D3>
CPU_TSIZ<1>      4B7> 8B5<> 9B3<>
CPU_TSIZ<2>      4B7> 8B7< 9B3<>
CPU_TS_L         4D7<> 7C7< 8B7<> 9D3<> 56D3>
CPU_TT<0>        4B7<> 7A7< 8B4<> 9B3<>
CPU_TT<0..4>     56D3>
CPU_TT<1>        4B7<> 7A7< 8B5<> 9B3<>
CPU_TT<2>        4B7<> 7A7< 8B4<> 9B3<>
CPU_TT<3>        4B7<> 7A7< 8B5<> 9B3<>
CPU_TT<4>        4B7<> 7A7< 8B4<> 9B3<>
CPU_VCORE_SLEEP  4D3< 4D7< 8B7< 8C1< 45D2<> 52C6>
                 59B6> 59D8>
CPU_VCORE_SLEEPA  45C3<>
CPU_VCORE_SLEEPB  45A4<>
CPU_VCORE_SLEEPC  45A1<>
CPU_WT_L         4B7> 7A7< 8B5<> 9B3<> 56C3>
CSLOT_IOWAIT_L   37B7< 52A8>
CVBS_CNT         22B7< 23D7<>
CVBS_D           22B7<
CY69P2           39B5<
CY811_S0         22A7<
CY811_S1         22A7<
DAC2RSET         22C5<> 57D5>
DAC2VDD          22C5< 52B6>
DAC2VREF         22C5<> 57D5>
DACRSET          22C4<
DACVDD           22C4< 52B6>
DACVREF          22C4<
DDC_VCC_3        24B3<> 52B6> 59B8>
DDC_VCC_5        25C4< 52A6> 59B8>

DDR_VREF         12A7< 14D2<> 14D8<> 15D8< 52A6>
DS1P1            35B2<
DS2P1            35B1<
DS2_1            38B2<
DS2_2            38B2<>
DS3P1            35B2<
DS6_1            38B6<
DS6_2            38B6<>
DUKE_BD          45B5<
DVOCLKIN         22C5<
DVOCLKOUT        22C5> 27B5<
DVOCLKOUT*       22C5<> 27B6<
DVOD0            22C5<> 27A8< 27C5< 57C2>
DVOD1            22C5<> 27A8< 27C5< 57C2>
DVOD2            22C5<> 26D1< 27C5< 57C2>
DVOD3            22B5<> 26D1< 27C5< 57C2>
DVOD4            22B5<> 27A8< 27C5< 57C2>
DVOD5            22B5<> 27A8< 27C5< 57C2>
DVOD6            22B5<> 27A8< 27C5< 57C2>
DVOD7            22B5<> 27A8< 27C5< 57C2>
DVOD8            22B5<> 26B1< 27C5< 57C2>
DVOD9            22B5<> 27A8< 27C5< 57C2>
DVOD10           22B5<> 27A8< 27B5< 57C2>
DVOD11           22B5<> 27A8< 27B5< 57C2>
DVODE            22C5<> 27B5<
DVOHSYNC         22C5> 26D7< 27B5<
DVOVREF          22C5<>
DVOVSYNC         22C5> 27B5<
DVO_PD           22B5<
DVO_PU           22B5<
EIDE_ADDR<0>     37B7> 38B8<
EIDE_ADDR<0..2>  58C5>
EIDE_ADDR<1>     37B7> 38B8<
EIDE_ADDR<2>     37B7> 38A8<
EIDE_CS1FX_L     37A7> 38B8< 58C5>
EIDE_CS3FX_L     37A7> 38B8< 58C5>
EIDE_CSELP_L     38C6<> 52A8>
EIDE_DATA<0>     37B7<> 37C5<
EIDE_DATA<0..15>  58D5>
EIDE_DATA<1>     37B7<> 37C5<
EIDE_DATA<2>     37B7<> 37C5<
EIDE_DATA<3>     37B7<> 37C5<
EIDE_DATA<4>     37B5< 37B7<>
EIDE_DATA<5>     37B5< 37B7<>
EIDE_DATA<6>     37B5< 37B7<>
EIDE_DATA<7>     37B5< 37B7<>
EIDE_DATA<8>     37B5< 37B7<>
EIDE_DATA<9>     37B5< 37B7<>
EIDE_DATA<10>    37B5< 37B7<>
EIDE_DATA<11>    37B5< 37B7<>
EIDE_DATA<12>    37B5< 37B7<>
EIDE_DATA<13>    37A5< 37B7<>
EIDE_DATA<14>    37A5< 37B7<>
EIDE_DATA<15>    37A5< 37B7<>
EIDE_DMACK_L     37A7<> 37C5< 58D5>
EIDE_DMARQ       37A7< 38C8< 58D5>
EIDE_DSTB_RDY    37A7< 37C5< 58D5>
EIDE_HSTB_RDY    37A7> 37C5< 58D5>
EIDE_INTRQ       37A7< 38C8< 58C5>
EIDE_IOCS16_L    38C6<> 52A8>
EIDE_PDIAG       38C6<>
EIDE_RST_L       37A7> 37D5< 58D5>
EIDE_STOP        37A7> 37D5< 58D5>
ENET_AVDD        35D2<> 35D4<> 52C6>
ENET_COL         34B7< 35B8< 57B5>
ENET_CRS         34C7< 35B8< 57B5>
ENET_DVDD        35D6<>
ENET_ENERGY_DET  28B5<> 28C1< 35B4>
ENET_LINK_RXD<0>  34C7< 35C8<
ENET_LINK_RXD<0..3>  57B5>
ENET_LINK_RXD<1>  34C7< 35C8<
ENET_LINK_RXD<2>  34C7< 35C8<
ENET_LINK_RXD<3>  34C7< 35B8<
ENET_LINK_RXD<4>  34C6<
ENET_LINK_RXD<5>  34C6<
ENET_LINK_RXD<6>  34C6<
ENET_LINK_RXD<7>  34C6<
ENET_LINK_TXD<0>  34C6<>
ENET_LINK_TXD<0..3>  57C5>
ENET_LINK_TXD<1>  34C6<>
ENET_LINK_TXD<2>  34C6<>
ENET_LINK_TXD<3>  34C6<>
ENET_LINK_TX_EN  34D6<> 57C5>
ENET_LINK_TX_ER  34D6<> 57C5>
ENET_MDC         34B7> 35B6<
ENET_MDIO        34B7<> 35A8<>
ENET_PHY_COL     35B6<> 57B5>
ENET_PHY_CRS     35B6<> 57B5>
ENET_PHY_RXD<0>  35C6<>
ENET_PHY_RXD<0..3>  57B5>
ENET_PHY_RXD<1>  35C6<>
ENET_PHY_RXD<2>  35C6<>
ENET_PHY_RXD<3>  35B6<>
ENET_PHY_RX_DV   35B6<> 57B5>
ENET_PHY_RX_ER   35B6<> 57B5>
ENET_PHY_TXD<0>  34C7< 35C6<>
ENET_PHY_TXD<0..3>  57C5>
ENET_PHY_TXD<1>  34C7< 35C6<>
ENET_PHY_TXD<2>  34C7< 35C6<>
ENET_PHY_TXD<3>  34C7< 35C6<>
ENET_PHY_TX_EN   34D7< 35C6< 57C5>
ENET_PHY_TX_ER   34D7< 35C6< 57C5>
ENET_RDAC_PD     35B5<>
ENET_RDN         35C3<> 57B5>
ENET_RDP         35C3<> 57B5>
ENET_RX_DV       34C7< 35B8< 57B5>
ENET_RX_ER       34C7< 35B8< 57B5>
ENET_TDN         35C3<> 57B5>
ENET_TDP         35C3<> 57B5>
ETHPHYRESET_L    35B6<

EXTINT14         28A8< 28B5<>
FAN_12V_FILT     29A5<> 52B3> 59C8>
FBA<0>           18D8> 18F3<
FBA<0..12>       55D3>
FBA<1>           18D8> 18F3<
FBA<2>           18D8> 18F3<
FBA<3>           18D8> 18F3<
FBA<4>           18D8> 18F3<
FBA<5>           18D8> 18F3<
FBA<6>           18D8> 18E3<
FBA<7>           18D8> 18E3<
FBA<8>           18D8> 18E3<
FBA<9>           18D8> 18E3<
FBA<10>          18D8> 18E3<
FBA<11>          18C8> 18E3<
FBA<12>          18C8> 18E3<
FBABA<0>         18C8<> 18E3<
FBABA<0..1>      55D3>
FBABA<1>         18C8<> 18E3<
FBACAS_L         18C8> 18G3< 55D3>
FBACKE           18D3< 18D7<> 55D3>
FBACLK0          18D7> 19C3< 55C3>
FBACLK0_L        18D7> 19C3< 55C3>
FBACLK1          18D7> 19D3< 55C3>
FBACLK1_L        18D7> 19D3< 55C3>
FBACS0_L         18C8> 18F3< 55D3>
FBARAS_L         18C8> 18G3< 55D3>
FBAWE_L          18C8> 18F3< 55D3>
FBBA<0>          18C3< 18D5<>
FBBA<0..12>      55C3>
FBBA<1>          18B3< 18D5<>
FBBA<2>          18B3< 18D5<>
FBBA<3>          18B3< 18D5<>
FBBA<4>          18B3< 18D5<>
FBBA<5>          18B3< 18D5<>
FBBA<6>          18B3< 18D5<>
FBBA<7>          18B3< 18D5<>
FBBA<8>          18B3< 18D5<>
FBBA<9>          18B3< 18D5<>
FBBA<10>         18B3< 18D5<>
FBBA<11>         18B3< 18C5<>
FBBA<12>         18A3< 18C5<>
FBBBA<0>         18A3< 18C5<>
FBBBA<0..1>      55C3>
FBBBA<1>         18A3< 18C5<>
FBBCAS_L         18C3< 18D4<> 55C3>
FBBCKE           18A3< 18C4<> 55B3>
FBBCLK0          18C5<> 19B3< 55B3>
FBBCLK0_L        18C5<> 19B3< 55B3>
FBBCLK1          18C5<> 19C3< 55B3>
FBBCLK1_L        18C5<> 19B3< 55B3>
FBBCS0_L         18C3< 18C4<> 55C3>
FBBRAS_L         18C3< 18D4<> 55C3>
FBBWE_L          18C3< 18D4<> 55C3>
FBCAL_CLK_GND    18A5< 18D7<
FBCAL_PD_VDDQ    18D7<
FBCAL_PU_GND     18A5< 18D7<
FBCAL_TERM_GND   18A5< 18D7<
FBD<0>           18G8<> 19D8<
FBD<0..63>       55D3>
FBD<1>           18G8<> 19D8<
FBD<2>           18G8<> 19D8<
FBD<3>           18G8<> 19D8<
FBD<4>           18G8<> 19D8<
FBD<5>           18G8<> 18E3<
FBD<6>           18G8<> 19D8<
FBD<7>           18G8<> 19D8<
FBD<8>           18G8<> 19D8<
FBD<9>           18G8<> 19D8<
FBD<10>          18G8<> 19D8<
FBD<11>          18G8<> 19D8<
FBD<12>          18G8<> 19D8<
FBD<13>          18G8<> 19D8<
FBD<14>          18G8<> 19D8<
FBD<15>          18G8<> 19D8<
FBD<16>          18G8<> 19D8<
FBD<17>          18G8<> 19D8<
FBD<18>          18G8<> 19D8<
FBD<19>          18G8<> 19C8<
FBD<20>          18G8<> 19C8<
FBD<21>          18G8<> 19C8<
FBD<22>          18G8<> 19C8<
FBD<23>          18G8<> 19C8<
FBD<24>          18G8<> 19C8<
FBD<25>          18F8<> 19C8<
FBD<26>          18F8<> 19C8<
FBD<27>          18F8<> 19C8<
FBD<28>          18F8<> 19C8<
FBD<29>          18F8<> 19C8<
FBD<30>          18F8<> 19C8<
FBD<31>          18F8<> 19C8<
FBD<32>          18F8<> 19D5<
FBD<33>          18F8<> 19D5<
FBD<34>          18F8<> 19D5<
FBD<35>          18F8<> 19D5<
FBD<36>          18F8<> 19D5<
FBD<37>          18F8<> 19D5<
FBD<38>          18F8<> 19D5<
FBD<39>          18F8<> 19D5<
FBD<40>          18F8<> 19D5<
FBD<41>          18F8<> 19D5<
FBD<42>          18F8<> 19D5<
FBD<43>          18F8<> 19D5<
FBD<44>          18F8<> 19D5<
FBD<45>          18E8<> 19D5<
FBD<46>          18E8<> 19D5<
FBD<47>          18E8<> 19D5<
FBD<48>          18E8<> 19D5<
FBD<49>          18E8<> 19D5<
FBD<50>          18E8<> 19D5<
```

8	7	6	5	4	3	2	1

```
FBD<51>          18E8<> 19C5<
FBD<52>          18E8<> 19C5<
FBD<53>          18E8<> 19C5<
FBD<54>          18E8<> 19C5<
FBD<55>          18E8<> 19C5<
FBD<56>          18E8<> 19C5<
FBD<57>          18E8<> 19C5<
FBD<58>          18E8<> 19C5<
FBD<59>          18E8<> 19C5<
FBD<60>          18E8<> 19C5<
FBD<61>          18E8<> 19C5<
FBD<62>          18E8<> 19C5<
FBD<63>          18E8<> 19C5<
FBD<64>          18G5<> 19C8<
FBD<64..127>     55C3>
FBD<65>          18G5<> 19C8<
FBD<66>          18G5<> 19C8<
FBD<67>          18G5<> 19C8<
FBD<68>          18G5<> 19C8<
FBD<69>          18G5<> 19C8<
FBD<70>          18G5<> 19C8<
FBD<71>          18G5<> 19C8<
FBD<72>          18G5<> 19C8<
FBD<73>          18G5<> 19C8<
FBD<74>          18G5<> 19B8<
FBD<75>          18G5<> 19B8<
FBD<76>          18G5<> 19B8<
FBD<77>          18G5<> 19B8<
FBD<78>          18G5<> 19B8<
FBD<79>          18G5<> 19B8<
FBD<80>          18G5<> 19B8<
FBD<81>          18G5<> 19B8<
FBD<82>          18G5<> 19B8<
FBD<83>          18G5<> 19B8<
FBD<84>          18G5<> 19B8<
FBD<85>          18G5<> 19B8<
FBD<86>          18G5<> 19B8<
FBD<87>          18G5<> 19B8<
FBD<88>          18G5<> 19B8<
FBD<89>          18F5<> 19B8<
FBD<90>          18F5<> 19B8<
FBD<91>          18F5<> 19B8<
FBD<92>          18F5<> 19B8<
FBD<93>          18F5<> 19B8<
FBD<94>          18F5<> 19B8<
FBD<95>          18F5<> 19B8<
FBD<96>          18F5<> 19C5<
FBD<97>          18F5<> 19C5<
FBD<98>          18F5<> 19C5<
FBD<99>          18F5<> 19C5<
FBD<100>         18F5<> 19C5<
FBD<101>         18F5<> 19C5<
FBD<102>         18F5<> 19C5<
FBD<103>         18F5<> 19C5<
FBD<104>         18F5<> 19C5<
FBD<105>         18F5<> 19C5<
FBD<106>         18F5<> 19B5<
FBD<107>         18F5<> 19B5<
FBD<108>         18F5<> 19B5<
FBD<109>         18E5<> 19B5<
FBD<110>         18E5<> 19B5<
FBD<111>         18E5<> 19B5<
FBD<112>         18E5<> 19B5<
FBD<113>         18E5<> 19B5<
FBD<114>         18E5<> 19B5<
FBD<115>         18E5<> 19B5<
FBD<116>         18E5<> 19B5<
FBD<117>         18E5<> 19B5<
FBD<118>         18E5<> 19B5<
FBD<119>         18E5<> 19B5<
FBD<120>         18E5<> 19B5<
FBD<121>         18E5<> 19B5<
FBD<122>         18E5<> 19B5<
FBD<123>         18E5<> 19B5<
FBD<124>         18E5<> 19B5<
FBD<125>         18E5<> 19B5<
FBD<126>         18E5<> 19B5<
FBD<127>         18E5<> 19B5<
FBDQM<0>         18D8> 18G3<
FBDQM<0..7>      55D3>
FBDQM<1>         18D8> 18G3<
FBDQM<2>         18D8> 18G3<
FBDQM<3>         18D8> 18G3<
FBDQM<4>         18D8> 18G3<
FBDQM<5>         18D8> 18G3<
FBDQM<6>         18D8> 18G3<
FBDQM<7>         18D8> 18G3<
FBDQM<8>         18D3< 18D5>
FBDQM<8..15>     55C3>
FBDQM<9>         18D3< 18D5>
FBDQM<10>        18D3< 18D5>
FBDQM<11>        18D3< 18D5>
FBDQM<12>        18D3< 18D5>
FBDQM<13>        18D3< 18D5>
FBDQM<14>        18C3< 18D5>
FBDQM<15>        18C3< 18D5>
FBDQS<0>         18C7<> 19A8<
FBDQS<0..7>      55C3>
FBDQS<1>         18C7<> 19A8<
FBDQS<2>         18C7<> 19A8<
FBDQS<3>         18C7<> 19A8<
FBDQS<4>         18C7<> 19A8<
FBDQS<5>         18C7<> 19A8<
FBDQS<6>         18C7<> 19A8<
FBDQS<7>         18C7<> 19A8<
FBDQS<8>         18D4<> 19A5<
FBDQS<8..15>     55B3>
FBDQS<9>         18D4<> 19A5<
FBDQS<10>        18D4<> 19A5<
FBDQS<11>        18D4<> 19A5<
```

```
FBDQS<12>        18D4<> 19A5<
FBDQS<13>        18D4<> 19A5<
FBDQS<14>        18D4<> 19A5<
FBDQS<15>        18D4<> 19A5<
FBDQSTERM<0>     19A7<
FBDQSTERM<0..7>  55C3>
FBDQSTERM<1>     19A7<
FBDQSTERM<2>     19A7<
FBDQSTERM<3>     19A7<
FBDQSTERM<4>     19A7<
FBDQSTERM<5>     19A7<
FBDQSTERM<6>     19A7<
FBDQSTERM<7>     19A7<
FBDQSTERM<8>     19A4<
FBDQSTERM<8..15>  55B3>
FBDQSTERM<9>     19A4<
FBDQSTERM<10>    19A4<
FBDQSTERM<11>    19A4<
FBDQSTERM<12>    19A4<
FBDQSTERM<13>    19A4<
FBDQSTERM<14>    19A4<
FBDQSTERM<15>    19A4<
FB_DLLVDD        18C6< 18D7<
FDX              35A5< 35C4<
FILT_ANALOG_BLU  25C5< 57D5> 59B8>
FILT_ANALOG_GRN  25C5< 57D5> 59B8>
FILT_ANALOG_RED  25C5< 57D5> 59B8>
FLOW_SS          45C6< 45C7< 45D8<
FLO_KNOWS_BEST   45C7<> 45C8<> 59D6>
FPD_PWR_ON       23D7<> 51B3<
FPD_PWR_ON_T     51B3<
FWPHYRST         28C5<> 36C8<
FW_BIAS1         36C5<> 57A5>
FW_BIAS2         36C5<> 57A5>
FW_CNTL0         34C3< 36C8< 57A5>
FW_CNTL1         34C3< 36C8< 57A5>
FW_CPS           36C6<
FW_C_LKON        28B6< 34C5<> 36B5<>
FW_D<0>          34C3< 36C8<
FW_D<0..7>       57A5>
FW_D<1>          34C3< 36C8<
FW_D<2>          34C3< 36B8<
FW_D<3>          34C3< 36B8<
FW_D<4>          34C3< 36B8<
FW_D<5>          34C3< 36B8<
FW_D<6>          34C3< 36B8<
FW_D<7>          34C3< 36B8<
FW_DIODE_BYPASS_V  36B6<> 36B7<> 52B6>
FW_DIO_V         36B6< 52B6>
FW_LINK_CNTL<0>  34C4<>
FW_LINK_CNTL<0..1>  57A5>
FW_LINK_CNTL<1>  34C4<>
FW_LINK_DATA<0>  34C4<>
FW_LINK_DATA<0..7>  57A5>
FW_LINK_DATA<1>  34C4<>
FW_LINK_DATA<2>  34C4<>
FW_LINK_DATA<3>  34C4<>
FW_LINK_DATA<4>  34C4<>
FW_LINK_DATA<5>  34C4<>
FW_LINK_DATA<6>  34C4<>
FW_LINK_DATA<7>  34C4<>
FW_LINK_LREQ     34C4<> 57A5>
FW_LPS           34C4<> 36C8<
FW_LREQ          34C3< 36C8< 57A5>
FW_PHY_3_3       36B5< 36B7< 36D7< 36D7< 52B6>
FW_PHY_CNTL0     36C7<> 57A5>
FW_PHY_CNTL1     36C7<> 57A5>
FW_PHY_D<0>      36C7<>
FW_PHY_D<0..7>   57A5>
FW_PHY_D<1>      36C7<>
FW_PHY_D<2>      36B7<>
FW_PHY_D<3>      36B7<>
FW_PHY_D<4>      36B7<>
FW_PHY_D<5>      36B7<>
FW_PHY_D<6>      36B7<>
FW_PHY_D<7>      36B7<>
FW_PHY_ISO*      36C6<
FW_PHY_RST       36C8<
FW_PHY_RST*      36C6<
FW_PHY_SCLK      36C7<> 57A5>
FW_PINT          34B5<> 34C1<
FW_PWR           29B3< 36D6< 50C6<> 51D4<> 52B6>
FW_PWR_SW        36D6< 51D2<> 52B6>
FW_R0            36C5<>
FW_R1            36C5<>
FW_SCLK          34C5<> 36C8< 57A5>
FW_TPA1N         36C5<> 57A5>
FW_TPA1P         36C5<> 57A5>
FW_TPA2N         36C5<> 57A5>
FW_TPA2P         36C5<> 57A5>
FW_TPB1          36B3<
FW_TPB1N         36C5<> 57A5>
FW_TPB1P         36C5<> 57A5>
FW_TPB2          36B4<
FW_TPB2N         36C5<> 57A5>
FW_TPB2P         36C5<> 57A5>
FW_TPI1N         36A8<> 36D1<> 57A5>
FW_TPI1P         36A8<> 36D1<> 57A5>
FW_TPI2N         36A8<> 36C1<> 57A5>
FW_TPI2P         36A8<> 36C1<> 57A5>
FW_TPO1N         36A8<> 36D1<> 57A5>
FW_TPO1P         36B8<> 36D1<> 57A5>
FW_TPO2N         36A8<> 36C1<> 57A5>
FW_TPO2P         36A8<> 36C1<> 57A5>
FW_VGND          52B6>
FW_VP            36D5< 52B6>
FW_VP1           36D1<> 36D3<> 52B6>
FW_VP2           36C1<> 36D3<> 52B6>
FW_VP_1          36D4< 52B6>
FW_VP_2          36D4< 52B6>
```

```
FW_VREG_FB       36D7<
FW_XI            36C6< 57A5>
FW_XI_A          36C6<
FW_XO            36C6<> 57A5>
GCORE_1          48C2<
GCORE_BSTH       48C5<>
GCORE_BSTH_TERM  48C3<>
GCORE_COMP       48B6<
GCORE_DH         48B5<>
GCORE_DL         48B5<>
GCORE_GND        48B5<>
GCORE_OCSET      48B6<>
GCORE_OVP        48B6<>
GCORE_VCC        48C6<
GCORE_VSENSE     48B6<> 48C4<>
GPULNKON         23C4<>
GPU_50PULLDWN    17A5<> 52A8>
GPU_50PULLUP     17B5<> 52A8>
GPU_AGP_AD<0>    17D6<>
GPU_AGP_AD<0..15>  54B7<
GPU_AGP_AD<1>    17D6<>
GPU_AGP_AD<2>    17D6<>
GPU_AGP_AD<3>    17D6<>
GPU_AGP_AD<4>    17D7<>
GPU_AGP_AD<5>    17D7<>
GPU_AGP_AD<6>    17D7<>
GPU_AGP_AD<7>    17D7<>
GPU_AGP_AD<8>    17D6<>
GPU_AGP_AD<9>    17D6<>
GPU_AGP_AD<10>   17D6<>
GPU_AGP_AD<11>   17D6<>
GPU_AGP_AD<12>   17D6<>
GPU_AGP_AD<13>   17D6<>
GPU_AGP_AD<14>   17D6<>
GPU_AGP_AD<15>   17C6<>
GPU_AGP_AD<16>   17C6<>
GPU_AGP_AD<16..31>  54B7<
GPU_AGP_AD<17>   17C6<>
GPU_AGP_AD<18>   17C6<>
GPU_AGP_AD<19>   17C6<>
GPU_AGP_AD<20>   17C6<>
GPU_AGP_AD<21>   17C6<>
GPU_AGP_AD<22>   17C6<>
GPU_AGP_AD<23>   17C6<>
GPU_AGP_AD<24>   17C6<>
GPU_AGP_AD<25>   17C6<>
GPU_AGP_AD<26>   17C6<>
GPU_AGP_AD<27>   17C6<>
GPU_AGP_AD<28>   17C6<>
GPU_AGP_AD<29>   17C6<>
GPU_AGP_AD<30>   17C6<>
GPU_AGP_AD<31>   17C6<>
GPU_AGP_CBE<0>   17C6<>
GPU_AGP_CBE<0..1>  54B7<
GPU_AGP_CBE<1>   17C6<>
GPU_AGP_CBE<2>   17C6<>
GPU_AGP_CBE<2..3>  54B7<
GPU_AGP_CBE<3>   17C6<>
GPU_AGP_DEVSEL_L  17B6<> 54B7<
GPU_AGP_FRAME_L  17B6<> 54B7<
GPU_AGP_IRDY_L   17B6<> 54B7<
GPU_AGP_PAR      17B6<> 54B7<
GPU_AGP_PIPE_L   17B6<> 54A7<
GPU_AGP_RBF_L    17B6<> 54A7<
GPU_AGP_SBA<0>   17A6<>
GPU_AGP_SBA<0..7>  54A7<
GPU_AGP_SBA<1>   17A6<>
GPU_AGP_SBA<2>   17A6<>
GPU_AGP_SBA<3>   17A6<>
GPU_AGP_SBA<4>   17A6<>
GPU_AGP_SBA<5>   17A6<>
GPU_AGP_SBA<6>   17A6<>
GPU_AGP_SBA<7>   17A6<>
GPU_AGP_SB_STB   17B6<> 54A7<
GPU_AGP_SB_STB_L  17A6<> 54A7<
GPU_AGP_STOP_L   17B6<> 54B7<
GPU_AGP_TRDY_L   17B6<> 54B7<
GPU_AGP_VREF     17A2< 17A8< 52A6>
GPU_AGP_VREF_H   16A7<
GPU_AGP_VREF_L   16A7<
GPU_AGP_VREF_X   17A2<
GPU_AGP_VREF_Y   17A2<
GPU_AGP_WBF_L    17B6<>
GPU_FB_VREF      18C8< 52A6>
GPU_FPBCLK       23C4<>
GPU_FPBCLK_L     23C4<>
GPU_FW_PME_L     23C4<>
GPU_IFB1OVDD     23B3<
GPU_IFP1PLLVDD   23B3<
GPU_MBDET_L      17A6<>
GPU_SS_XIN       22A7<
GPU_STEREO       23C4<>
GPU_STRAP<0>     22B4<> 26A4<
GPU_STRAP<1>     22B4<> 26B3<
GPU_STRAP<2>     22B4<> 26D3<
GPU_STRAP<3>     22B4<> 26D3<
GPU_SWAP_A       23C4<>
GPU_SWAP_B       23C4<>
GPU_TESTMECLK    23C4<>
GPU_TMDS_CKM     23C2< 23D3<> 57D2>
GPU_TMDS_CKP     23C2< 23D3<> 57D2>
GPU_TMDS_D0M     23C2< 23D3<> 57D2>
GPU_TMDS_D0P     23C2< 23D3<> 57D2>
GPU_TMDS_D1M     23C2< 23D3<> 57D2>
GPU_TMDS_D1P     23C2< 23D3<> 57D2>
GPU_TMDS_D2M     23C2< 23D3<> 57D2>
GPU_TMDS_D2P     23C2< 23D3<> 57D2>
GPU_TMODE        17A5< 52A8>
GPU_XTALOUTBUFF  22A8< 22B4<>
GPU_XTALSSIN     22A5< 22B2< 52A8>
```

```
GPWRGD           47B8< 48A5<>
GRAPHICS_VPWR    48B5<>
GRAPH_CORE       17D4< 23C7<> 48C2<> 52A6>
GRAPH_DDC_SCL    22D5<> 24A7<
GRAPH_DDC_SDA    22D5<> 24A7<
GRAPH_IIC_SCL2   23D3<>
GRAPH_IIC_SDA2   23D3<>
HD_DIOR_L        37D1< 38C3<> 58C5>
HD_DIOW_L        37C1< 38C3<> 58C5>
HD_DMACK_L       37D1< 38C3<> 58C5>
HD_DMARQ         38C3<> 58C5>
HD_INTRQ         38C3<> 58C5>
HD_IOCHRDY       37C1< 38C3<> 58C5>
HD_RESET_L       37D1< 38C3<> 58C5>
HD_UIDE_ADDR<0>  38C3<>
HD_UIDE_ADDR<0..2>  58C5>
HD_UIDE_ADDR<1>  38C3<>
HD_UIDE_ADDR<2>  38C2<>
HD_UIDE_CS1FX_L  38C3<> 58B5>
HD_UIDE_CS3FX_L  38C2<> 58B5>
HEADPHONE_COM    41B2<>
HEADPHONE_L      41B2<> 41D2<
HEADPHONE_R      41B2<> 41C2<
HONK_ADJ         51B4<>
HP16_L           41D4<
HP16_R           41C4<
HPBYP            41B5< 41D6<
HPGAL_L          41D4<
HPGAL_R          41C4<
HPIN_L           41D6<
HPIN_R           41D6<
HP_OFF           41A7< 41D5<
HP_OUT_L         41D5<>
HP_OUT_R         41D5<>
HP_STAR_GND      39B7<> 41A8< 41B4< 41B8< 41C5<
                 41D4< 41D7<
HP_TL            41D3<
HP_TP            41B3<
HP_TR            41C3<
HSYNC*           22C5<> 57D5>
ICORE_COMP       47B6<
ICW              47B7<
IFP0AVCC         23A6< 23C1< 52A6>
IFP0PLLVDD       23B4<
IFP0RSET         23B4<>
IFP0VREF         23B4<> 52A6>
IFP_AVCC         23A7<>
IFP_VADJ         23A8<
IIC_ADD          29C6<> 59A8>
INTCORE_1        47B3<
INTCORE_BSTH     47B6<>
INTCORE_BSTH_TERM  47B6<>
INTCORE_DH       47B6<>
INTCORE_DHT      47B5<>
INTCORE_DL       47B6<>
INTCORE_GND      47A7<>
INTCORE_OCSET    47B6<>
INTCORE_OVP      47B6<>
INTCORE_VCC      47C7<
INTREPID_ACS_REF  9A3<
INTREPID_VPWR    47B6<>
INTREPID_VPWRA   47B4<>
INTREPID_VSENSE  47C6<> 59C8>
INTREP_DLT       47B5<>
INT_AGPPVT       16C6<>
INT_AGP_FB_IN    16C6< 54A7<
INT_AGP_FB_OUT   16C6<> 54A7<
INT_AGP_VREF     16A7< 16C6<> 52C3>
INT_ANALYZER_CLK  8A2< 9B4< 16C7< 54A7< 56B3> 59A8>

INT_ANALYZER_CLKA  9B3<>
INT_CLOCK_OUT    8B2<> 56B3>
INT_CPU_FB_IN    9B3< 56C3>
INT_CPU_FB_OUT   9B3<> 56C3>
INT_ENET_RST_L   28B5<> 28D1< 35B8<
INT_EXTINT3_PU   28B5<> 28B8<
INT_EXTINT12_PU  28B5<> 28B8<
INT_EXTINT13_PU  28B5<> 28B8<
INT_EXTINT17_PU  28B5<> 28B8< 32B6>
INT_GPIO1_PD     28A8< 28C5<>
INT_GPIO9_PU     28B5<> 28B8<
INT_GPIO12_PU    28A8< 28B5<>
INT_I2C_CLK0     14A6<> 15A6< 34B3<
INT_I2C_CLK0R    34B5<> 34C1<
INT_I2C_CLK1     34A3<> 34B1<
INT_I2C_CLK2     28A3<> 28D1< 29C7<> 34B5< 39B1<>
                 59A8>
INT_I2C_DATA0    14A6<> 15A6< 34B3<
INT_I2C_DATA0R   34B5<> 34C1<
INT_I2C_DATA1    34A3<> 34B1<
INT_I2C_DATA2    28A3<> 28D1< 29C7<> 34B5< 39B1<>
                 59A8>
INT_JTAG_TEI     34B7< 34C1<
INT_MEM_REF      12B6<
INT_MEM_VREF     12A8<> 14A1<
INT_MOD_BITCLK   28A3<> 28A8< 28C6<
INT_MOD_CLKOUT   28A3> 28A8< 28C6<
INT_MOD_DTI      28A3< 28A8< 28C6<
INT_MOD_DTO      28A3> 28A8< 28C6<
INT_MOD_SYNC     28A3<> 28A8< 28C6<
INT_PCI_FB_IN    30C5< 54C7<
INT_PCI_FB_OUT   30C5<> 54D7<
INT_PEND_PROC_INT  28A5> 44B4<>
INT_PLL1_GND     28A5<> 28C4<
INT_PLL2_GND     28A5<> 28D4<
INT_PLL3_GND     28A4<> 28D4<
INT_PLL4_GND     30C4<> 30D4<
INT_PLL5_GND     16A5<> 16D5<
INT_PLL6_GND     9A2<> 9D3<
INT_PLL7_GND     28A4<> 28D4<
```

```
INT_PLL9_GND     28A4<> 28D4<
INT_PROC_SLEEP_REQ_L  28A5< 44B4<>
INT_PU_RESET_L   15B3< 34C3< 44C2<> 44C2<>
INT_REF_CLK_IN_PD  28A6< 53A6<
INT_RESET_L      34C3< 35B8< 41A7< 43C7< 44D2<>
INT_ROM_CS_L     30C5<>
INT_ROM_OE_L     30C5<>
INT_ROM_OVERLAY_PU  16D7< 30A7< 30C5<> 54A7<
INT_ROM_RW_L     30C5<>
INT_SND_CLKOUT   28A3<>
INT_SND_SCLK     28A3<>
INT_SND_SYNC     28B3<>
INT_SND_TO_AUDIO  28B3<>
INT_SPKR+        42A6<> 43D8<
INT_SPKR-        42A6<> 43D8<
INT_SUSPEND_ACK_L  9B3> 44B5<>
INT_SUSPEND_REQ_L  9B3< 44B8<>
INT_TMDS_3V      24C3<> 52A6> 59C8>
INT_TST_MONIN_PD  34B7< 34C1<
INT_TST_PLLEN_PD  28C6< 34B7<
INT_WATCHDOG_L   28A5> 44C5<>
INV_CUR_HI       23D7< 29B8<
INV_CUR_HI_FILT  29A5<> 59A8>
IO_RESET_L       32A6< 35B8< 44B8<> 44D3< 59A8>
IPWRGD           46A8< 47A6<>
JAZ              43B6<
JTAG_ASIC_TCK    8A4<> 34B7< 35C4< 59D8>
JTAG_ASIC_TDI    8A4<> 28C6< 34B7< 59D8>
JTAG_ASIC_TDO    8A4<> 35B4<> 59D8>
JTAG_ASIC_TMS    8A4<> 34B7< 35A2< 35B4<> 59D8>
JTAG_ASIC_TRST_L  8A4<> 34B7< 59C8>
JTAG_CPU_TCK     4C3< 7D5< 8A3<> 59C8>
JTAG_CPU_TDI     4C3< 7A5< 8A3<> 59C8>
JTAG_CPU_TDO     4C3> 8A3<> 59C8>
JTAG_CPU_TMS     4C3< 7A5< 8A3<> 59C8>
JTAG_CPU_TRST_L  4C3< 7C5< 8A3<> 59C8>
JTAG_ENET_TDI    35A2< 35B5<>
JTAG_INTRP_TDO   28C6< 34B7> 35B3<
KAVAN            43A6<
KS5VSD           29A5<> 52B3> 59A8>
KS_INT_SPKR+     29A3< 43D7< 58A5> 59B8>
KS_INT_SPKR+_FILT  29A5<>
KS_INT_SPKR-     29A3< 42B4< 43D7< 58A5> 59B8>
KS_INT_SPKR-_FILT  29A5<>
KYLE             46C6<
L31_2            40C6<
L32_2            40B6<>
L36_2            40B6<
L41_FILT         42B7<>
L43_1            41A4<
L3202_1          40C6<
LAMP_STS         23D7< 29A3<
LAMP_STS_FILT    29A5<> 59A8>
LCD_PWM          23D7< 29A8<
LCD_PWM_FILT     29A5<> 59A8>
LED_5V           29A8< 52B3>
LED_5V_FILT      29A5<> 52B3> 59A8>
LED_RET          29A3< 51B6< 52B3>
LED_RET_FILT     29A5<> 52A3> 59A8>
LED_ROMCS        30B3<>
LED_ROMCS_L      30B4<
LED_ROMCS_LIGHT  30A3<
LID_SWITCH       29B2<> 44C4<>
LINA             39C4< 40C2<
LINEOUT_COMM2    59B6>
LINE_IN_COM      40B7<> 59B6>
LINE_IN_L        40B7<> 40C7<> 59B6>
LINE_IN_R        40B6<> 40B7<> 59B6>
LINE_IN_SENSE    40B7<> 40C7<> 59B6>
LINE_OUT_L       59B6>
LINN             42C5< 43D2<
LINN1            43D2<
LINP             42C5< 43D4<
LINSENSE         40C5<
LOW_PWR          35A5< 35B4<
LO_T1            41A4<
LP4202P2         40C5<
LP4202P3         40B5<
LP4202P4         40B5<
LPL1             41D6<
LPR1             41C6<
LT1962_INT_ADJ   28D7<
LT1962_INT_BYP   28D7<>
LT1962_INT_VIN   28D7<>
M1FH             43B7<>
M1FL             43A7<>
M1H              43B6<> 43B6<>
M1HFILT          43B5<
M1L              43A6<> 43B6<>
M1S              43A6<> 43B6<>
MAIN_RESET_L     17C8< 30B2< 31D4< 32A8< 44C4<>
                 59A6>
MAIN_RESET_L_PU  31D3<>
MAIN_SUPPLY_LED  50D5<
MAXBUS_PWR_EN    46C7<
MAX_PWR_ADJ      46C5<>
MEMREFG1         20A5<>
MEMREFG2         20A4<>
MEMREFG3         21A4<>
MEMREFG4         21A4<>
MEMREFN1         18B8<>
MEMREFN2         18B7<>
MEM_ADDR<0>      12C3< 12D6<>
MEM_ADDR<0..12>  53D6<
MEM_ADDR<1>      12C3< 12D6<>
MEM_ADDR<2>      12C3< 12D6<>
MEM_ADDR<3>      12D3< 12D6<>
MEM_ADDR<4>      12D3< 12D6<>
MEM_ADDR<5>      12C2< 12D6<>
MEM_ADDR<6>      12D2< 12D6<>
```

```
MEM_ADDR<7>      12D3< 12D6<>
MEM_ADDR<8>      12D2< 12D6<>
MEM_ADDR<9>      12C3< 12D6<>
MEM_ADDR<10>     12C3< 12D6<>
MEM_ADDR<11>     12B3< 12D6<>
MEM_ADDR<12>     12D2< 12D6<>
MEM_BA<0>        12B3< 12D6<>
MEM_BA<0..1>     53D6<
MEM_BA<1>        12B3< 12D6<>
MEM_CAS_L        12A3< 12C6<> 53C6<
MEM_CKE<0>       12C2< 12C6<>
MEM_CKE<0..3>    53C6<
MEM_CKE<1>       12B2< 12B6<>
MEM_CKE<2>       12B6<> 12C2<
MEM_CKE<3>       12B2< 12B6<>
MEM_CS_L<0>      12C2< 12C6<>
MEM_CS_L<0..3>   53C6<
MEM_CS_L<1>      12C2< 12C6<>
MEM_CS_L<2>      12B2< 12B6<>
MEM_CS_L<3>      12B2< 12C6<>
MEM_DATA<0>      12D8<> 13C8<>
MEM_DATA<0..63>  53D6<
MEM_DATA<1>      12D8<> 13C8<>
MEM_DATA<2>      12D8<> 13C8<>
MEM_DATA<3>      12D8<> 13C8<>
MEM_DATA<4>      12D8<> 13C8<>
MEM_DATA<5>      12D8<> 13C8<>
MEM_DATA<6>      12D8<> 13C8<>
MEM_DATA<7>      12D8<> 13C8<>
MEM_DATA<8>      12D8<> 13C8<>
MEM_DATA<9>      12D8<> 13C8<>
MEM_DATA<10>     12D8<> 13C8<>
MEM_DATA<11>     12D8<> 13C8<>
MEM_DATA<12>     12D8<> 13C8<>
MEM_DATA<13>     12D8<> 13C8<>
MEM_DATA<14>     12C8<> 13C8<>
MEM_DATA<15>     12C8<> 13C8<>
MEM_DATA<16>     12C8<> 13B6<>
MEM_DATA<17>     12C8<> 13B6<>
MEM_DATA<18>     12C8<> 13B6<>
MEM_DATA<19>     12C8<> 13B6<>
MEM_DATA<20>     12C8<> 13B6<>
MEM_DATA<21>     12C8<> 13B6<>
MEM_DATA<22>     12C8<> 13B6<>
MEM_DATA<23>     12C8<> 13B6<>
MEM_DATA<24>     12C8<> 13A6<>
MEM_DATA<25>     12C8<> 13A6<>
MEM_DATA<26>     12C8<> 13A6<>
MEM_DATA<27>     12C8<> 13A6<>
MEM_DATA<28>     12C8<> 13A6<>
MEM_DATA<29>     12C8<> 13A6<>
MEM_DATA<30>     12C8<> 13A6<>
MEM_DATA<31>     12C8<> 13A6<>
MEM_DATA<32>     12C8<> 13C4<>
MEM_DATA<33>     12C8<> 13C4<>
MEM_DATA<34>     12C8<> 13C4<>
MEM_DATA<35>     12C8<> 13C4<>
MEM_DATA<36>     12C8<> 13C4<>
MEM_DATA<37>     12C8<> 13C4<>
MEM_DATA<38>     12C8<> 13C4<>
MEM_DATA<39>     12C8<> 13C4<>
MEM_DATA<40>     12B8<> 13C4<>
MEM_DATA<41>     12B8<> 13C4<>
MEM_DATA<42>     12B8<> 13C4<>
MEM_DATA<43>     12B8<> 13C4<>
MEM_DATA<44>     12B8<> 13C4<>
MEM_DATA<45>     12B8<> 13C4<>
MEM_DATA<46>     12B8<> 13C4<>
MEM_DATA<47>     12B8<> 13C4<>
MEM_DATA<48>     12B8<> 13B3<>
MEM_DATA<49>     12B8<> 13B3<>
MEM_DATA<50>     12B8<> 13B3<>
MEM_DATA<51>     12B8<> 13B3<>
MEM_DATA<52>     12B8<> 13B3<>
MEM_DATA<53>     12B8<> 13B3<>
MEM_DATA<54>     12B8<> 13B3<>
MEM_DATA<55>     12B8<> 13B3<>
MEM_DATA<56>     12B8<> 13B3<>
MEM_DATA<57>     12B8<> 13B3<>
MEM_DATA<58>     12B8<> 13B3<>
MEM_DATA<59>     12B8<> 13B3<>
MEM_DATA<60>     12B8<> 13B3<>
MEM_DATA<61>     12B8<> 13B3<>
MEM_DATA<62>     12B8<> 13B3<>
MEM_DATA<63>     12B8<> 13B3<>
MEM_DQM<0>       12C6<> 13C8<>
MEM_DQM<0..7>    53D6<
MEM_DQM<1>       12C6<> 13C8<>
MEM_DQM<2>       12C6<> 13A6<>
MEM_DQM<3>       12C6<> 13A6<>
MEM_DQM<4>       12C6<> 13C4<>
MEM_DQM<5>       12C6<> 13C4<>
MEM_DQM<6>       12C6<> 13B3<>
MEM_DQM<7>       12C6<> 13B3<>
MEM_DQS<0>       12C6<> 13C8<>
MEM_DQS<0..7>    53D6<
MEM_DQS<1>       12C6<> 13C8<>
MEM_DQS<2>       12C6<> 13A6<>
MEM_DQS<3>       12C6<> 13A6<>
MEM_DQS<4>       12C6<> 13C4<>
MEM_DQS<5>       12C6<> 13C4<>
MEM_DQS<6>       12C6<> 13B3<>
MEM_DQS<7>       12C6<> 13B3<>
MEM_MUXSEL_H<0..1>  53C6<
MEM_MUXSEL_H<1>  12B6<>
MEM_MUXSEL_L<0..1>  53C6<
MEM_MUXSEL_L<1>  12B6<>
MEM_RAS_L        12A3< 12C6<> 53C6<
MEM_WE_L         12B3< 12C6<> 53C6<
MIC1             43B5<
```

```
MIC1S1          43A7<>
MIC2            43B4<
MIC3            43B4<
MIC4            43B3<>
MIC5            43A3<
MICHIGH         29A5<> 43B8< 58A5> 59A8>
MICLOW          29A5<> 43A8< 58A5> 59A8>
MICSHLD         29A5<> 43A8< 58A5> 59A8>
MIC_FIX         43C5<
MIC_IN          39C4< 43B2<
MII_EN          35C4<
MODEM_USB_DM    28B2< 29C5<> 58A5> 59B6>
MODEM_USB_DP    28B2< 29C5<> 58A5> 59B6>
MON_DETECT      23D7<> 25C6< 59D6>
MON_I2C_SCL     22D5<> 25B6<
MON_I2C_SDA     22D5<> 25B6<
MPIC_CPU_INT_L  4B3< 7A5< 8D7<> 28B5>
MPWRGD          48B7< 48B7< 49B5<>
MR_FLO          45C5<>
MR_FLO_1        45B4<>
MUX_SEL_H       12D4< 13A3<> 13C4<> 53C6<
MUX_SEL_L       12D4< 13A6<> 13C8<> 53C6<
M_SPD_WP        15A7<
M_VDDID         15A7<
NC_-10VINREG    29C7<>
NC_-12VREG      29C6<>
NC_AUDIO2MODEM  29C6<>
NC_AUDIO2MODEMRTN  29C6<>
NC_AUD_MODEM    29C6<>
NC_AUD_MODEM_RTN  29C6<>
NC_BIGDIMM9     15D6<
NC_BIGDIMM10    15D6<
NC_BIGDIMM44    15B6<
NC_BIGDIMM45    15B6<
NC_BIGDIMM47    15B6<
NC_BIGDIMM49    15B6<
NC_BIGDIMM51    15B6<
NC_BIGDIMM71    15A6<
NC_BIGDIMM101   15D4>
NC_BIGDIMM102   15D4>
NC_BIGDIMM103   15D4>
NC_BIGDIMM113   15C4>
NC_BIGDIMM134   15C4>
NC_BIGDIMM135   15B4>
NC_BIGDIMM140   15B4>
NC_BIGDIMM142   15B4>
NC_BIGDIMM144   15B4>
NC_BIGDIMM163   15A4>
NC_BIGDIMM167   15A4>
NC_BIGDIMM173   15A4>
NC_BRCLKO       28A5>
NC_BS1          29B7<>
NC_BS2          29B6<>
NC_BS3          29D1<>
NC_BS4          29D1<>
NC_BT1          29D2<>
NC_BT3          29D2<>
NC_BT4          29D2<>
NC_BT5          29D2<>
NC_BT6          29D2<>
NC_BUF_RST      22B5>
NC_CBUS_INT_L   28A8<
NC_CLK33M_PCI_SLOTC  30D7<
NC_CLKENET_LINK_GTX  34C6>
NC_CPUAP<0>     4B7<>
NC_CPUAP<1>     4B7<>
NC_CPUAP<2>     4B7<>
NC_CPUAP<3>     4B7<>
NC_CPUAP<4>     4B7<>
NC_CPUCRUD<0>   5D7<>
NC_CPUCRUD<1>   5D7<>
NC_CPUCRUD<2>   5D7<>
NC_CPUCRUD<3>   5D7<>
NC_CPUCRUD<4>   5D7<>
NC_CPUCRUD<5>   5D7<>
NC_CPUCRUD<6>   5D7<>
NC_CPUCRUD<7>   5D7<>
NC_CPUCRUD<8>   5D7<>
NC_CPUCRUD<9>   5D7<>
NC_CPUCRUD<10>  5D7<>
NC_CPUCRUD<11>  5D7<>
NC_CPUCRUD<12>  5D7<>
NC_CPUCRUD<13>  5D7<>
NC_CPUCRUD<14>  5D7<>
NC_CPUCRUD<15>  5D7<>
NC_CPUCRUD<16>  5D7<>
NC_CPUCRUD<17>  5C7<>
NC_CPUCRUD<18>  5C7<>
NC_CPUCRUD<19>  5C7<>
NC_CPUCRUD<20>  5C7<>
NC_CPUCRUD<21>  5C7<>
NC_CPUCRUD<22>  5C7<>
NC_CPUCRUD<23>  5C7<>
NC_CPUCRUD<24>  5C7<>
NC_CPUCRUD<25>  5C7<>
NC_CPUCRUD<26>  5C7<>
NC_CPUCRUD<27>  5C7<>
NC_CPUCRUD<28>  5C7<>
NC_CPUCRUD<29>  5C7<>
NC_CPUCRUD<30>  5C7<>
NC_CPUCRUD<31>  5C7<>
NC_CPUCRUD<32>  5C7<>
NC_CPUCRUD<33>  5C7<>
NC_CPUCRUD<34>  5C7<>
NC_CPUCRUD<35>  5C7<>
NC_CPUCRUD<36>  5C7<>
NC_CPUCRUD<37>  5C7<>
NC_CPUCRUD<38>  5C7<>
NC_CPUCRUD<39>  5C7<>
NC_CPUCRUD<40>  5C7<>
```

```
NC_CPUCRUD<41>  5B7<>
NC_CPUCRUD<42>  5B7<>
NC_CPUCRUD<43>  5B7<>
NC_CPUCRUD<44>  5B7<>
NC_CPUCRUD<45>  5B7<>
NC_CPUCRUD<46>  5B7<>
NC_CPUCRUD<47>  5B7<>
NC_CPUCRUD<48>  5B7<>
NC_CPUCRUD<49>  5B7<>
NC_CPUCRUD<50>  5B7<>
NC_CPUCRUD<51>  5B7<>
NC_CPUCRUD<52>  5B7<>
NC_CPUCRUD<53>  5B7<>
NC_CPUCRUD<54>  5B7<>
NC_CPUCRUD<55>  5B7<>
NC_CPUCRUD<56>  5B7<>
NC_CPUCRUD<57>  5B7<>
NC_CPUCRUD<58>  5B7<>
NC_CPUCRUD<59>  5B7<>
NC_CPUCRUD<60>  5B7<>
NC_CPUCRUD<61>  5B7<>
NC_CPUCRUD<62>  5B7<>
NC_CPUCRUD<63>  5B7<>
NC_CPUCRUD<64>  5B7<>
NC_CPUCRUD<65>  5B7<>
NC_CPUCRUD<66>  5B7<>
NC_CPUCRUD<67>  5A7<>
NC_CPUCRUD<68>  5A7<>
NC_CPUCRUD<69>  5A7<>
NC_CPUCRUD<70>  5A7<>
NC_CPUCRUD<71>  5A7<>
NC_CPUCRUD<72>  5A7<>
NC_CPUCRUD<73>  5A7<>
NC_CPUCRUD<74>  5A7<>
NC_CPUCRUD<75>  5A7<>
NC_CPUCRUD<76>  5A7<>
NC_CPUCRUD<77>  5A7<>
NC_CPUCRUD<78>  5A7<>
NC_CPUCRUD<79>  5A7<>
NC_CPUCRUD<80>  5A7<>
NC_CPUCRUD<81>  5A7<>
NC_CPUCRUD<82>  5A7<>
NC_CPUCRUD<83>  5A7<>
NC_CPUCRUD<84>  5A7<>
NC_CPUCRUD<85>  5A7<>
NC_CPUCRUD<86>  5A7<>
NC_CPUCRUD<87>  5A7<>
NC_CPUCRUD<88>  5A7<>
NC_CPUCRUD<89>  5A7<>
NC_CPUDP<0>     5A4<>
NC_CPUDP<1>     5A4<>
NC_CPUDP<2>     5A4<>
NC_CPUDP<3>     5A4<>
NC_CPUDP<4>     5A4<>
NC_CPUDP<5>     5A4<>
NC_CPUDP<6>     5A4<>
NC_CPUDP<7>     5A4<>
NC_CPU_CLKOUT   4D3>
NC_CSLOT_ADDR<3>  37B7>
NC_CSLOT_ADDR<4>  37A7>
NC_CSLOT_ADDR<5>  37A7>
NC_CSLOT_ADDR<6>  37A7>
NC_CSLOT_ADDR<7>  37A7>
NC_CSLOT_ADDR<8>  37A7>
NC_CSLOT_ADDR<9>  37A7>
NC_CSLOT_CE1_L  37C7>
NC_CSLOT_CE2_L  37C7>
NC_CSLOT_IORD_L  37C7>
NC_CSLOT_IOWR_L  37C7>
NC_CSLOT_OE_L   37B7>
NC_CSLOT_WE_L   37B7>
NC_DAA_CLKOUT   29C7<>
NC_DAA_LOADOUT  29C7<>
NC_DACC_BLU     22C4>
NC_DACC_GRN     22C4>
NC_DACC_RED     22C4>
NC_DACC_RSET    22C4>
NC_DFPCLK       23C3>
NC_DFPCLK*      23C3>
NC_DFPD0        23C3>
NC_DFPD1        23C3>
NC_DFPD2        23C3>
NC_DFPD3        23C3>
NC_DFPD5        23C3>
NC_DFPD6        23C3>
NC_ENET_LINK_TXD<4>  34C6>
NC_ENET_LINK_TXD<5>  34C6>
NC_ENET_LINK_TXD<6>  34C6>
NC_ENET_LINK_TXD<7>  34C6>
NC_EXT_TMDS_CKM  23C3>
NC_EXT_TMDS_CKP  23C3>
NC_EXT_TMDS_D0M  23C3>
NC_EXT_TMDS_D0P  23C3>
NC_EXT_TMDS_D1M  23C3>
NC_EXT_TMDS_D1P  23C3>
NC_EXT_TMDS_D2M  23C3>
NC_EXT_TMDS_D2P  23C3>
NC_FB1<0>       20B6<>
NC_FB1<1>       20B6<>
NC_FB1<2>       20B6<>
NC_FB1<3>       20B6<>
NC_FB1<4>       20B6<>
NC_FB1<5>       20B6<>
NC_FB1<6>       20B6<>
NC_FB1<7>       20B6<>
NC_FB1<8>       20B6<>
NC_FB1<9>       20B5<>
NC_FB1<10>      20B5<>
NC_FB2<0>       20B2<>
NC_FB2<1>       20B2<>
```

```
NC_FB2<2>       20B2<>
NC_FB2<3>       20B2<>
NC_FB2<4>       20B2<>
NC_FB2<5>       20B2<>
NC_FB2<6>       20B2<>
NC_FB2<7>       20B2<>
NC_FB2<8>       20B2<>
NC_FB2<9>       20B1<>
NC_FB2<10>      20B1<>
NC_FB3<0>       21B6<>
NC_FB3<1>       21B6<>
NC_FB3<2>       21B6<>
NC_FB3<3>       21B6<>
NC_FB3<4>       21B6<>
NC_FB3<5>       21B6<>
NC_FB3<6>       21B6<>
NC_FB3<7>       21B6<>
NC_FB3<8>       21B6<>
NC_FB3<9>       21B5<>
NC_FB3<10>      21B5<>
NC_FB4<0>       21B2<>
NC_FB4<1>       21B2<>
NC_FB4<2>       21B2<>
NC_FB4<3>       21B2<>
NC_FB4<4>       21B2<>
NC_FB4<5>       21B2<>
NC_FB4<6>       21B2<>
NC_FB4<7>       21B2<>
NC_FB4<8>       21B2<>
NC_FB4<9>       21B1<>
NC_FB4<10>      21B1<>
NC_FBACS1_L     18C8>
NC_FBBCS1_L     18C4<>
NC_FBDQS_L<0>   18C7<>
NC_FBDQS_L<1>   18C7<>
NC_FBDQS_L<2>   18C7<>
NC_FBDQS_L<3>   18C7<>
NC_FBDQS_L<4>   18C7<>
NC_FBDQS_L<5>   18C7<>
NC_FBDQS_L<6>   18C7<>
NC_FBDQS_L<7>   18C7<>
NC_FBDQS_L<8>   18D4<>
NC_FBDQS_L<9>   18D4<>
NC_FBDQS_L<10>  18D4<>
NC_FBDQS_L<11>  18D4<>
NC_FBDQS_L<12>  18D4<>
NC_FBDQS_L<13>  18D4<>
NC_FBDQS_L<14>  18D4<>
NC_FBDQS_L<15>  18D4<>
NC_FMAX7        8A8<>
NC_FMAX8        8A8<>
NC_FW_CNA       36B6>
NC_GPU<0>       17A6<>
NC_GPU<1>       17A6<>
NC_GPU<2>       17A6<>
NC_GPU<3>       17A6<>
NC_GPU<4>       17A6<>
NC_GPULPS       23C4<>
NC_GPU_DBI_LO   17B6<>
NC_GPU_INTB_L   17B6<>
NC_GPU_THERMA   23C4<>
NC_GPU_THERMC   23C4<>
NC_IFP1RSET     23B3<>
NC_IFP1VREF     23B3<>
NC_INPA         39C2>
NC_INT_TST_MONOUT_TP  34B6>
NC_JTAG7        8A4<>
NC_JTAG10       8A3<>
NC_LCENABLE     8A4<>
NC_MEM_MUXSEL_H<0>  12B6<>
NC_MEM_MUXSEL_L<0>  12B6<>
NC_MODEM_DETECT_L  29C7<>
NC_NVAGP_TDO    17A5<>
NC_P00_D0       44D5<>
NC_P01_D1       44D5<>
NC_P02_D2       44C5<>
NC_P03_D3       44C5<>
NC_P04_D4       44C5<>
NC_P05_D5       44C5<>
NC_P06_D6       44C5<>
NC_P07_D7       44C5<>
NC_P10_D8       44C5<>
NC_P11_D9       44C5<>
NC_P14_D12      44C5<>
NC_P20_A0_D0    44C5<>
NC_P21_A1_D1_D0  44C5<>
NC_P22_A2_D2_D1  44C5<>
NC_P23_A3_D3_D2  44C5<>
NC_P24_A4_D4_D3  44C5<>
NC_P25_A5_D5_D4  44C5<>
NC_P26_A6_D6_D5  44C5<>
NC_P27_A7_D7_D6  44C5<>
NC_P33_A11      44B5<>
NC_P34_A12      44B5<>
NC_P35_A13      44B5<>
NC_P36_A14      44B5<>
NC_P37_A15      44B5<>
NC_P43_A19      44B5<>
NC_P45_CS1_L    44B5<>
NC_P74_TA2OUT_W  44C4<>
NC_P75_TA2IN_W  44C4<>
NC_P76_TA3OUT   44C4<>
NC_P77_TA3IN    44C4<>
NC_P92_TB2IN_SOUT3  44B4<>
NC_P93_DA0_TB3IN  44B4<>
NC_P96_ANEX0_CLK4  44B4<>
NC_P103_AN3     44B4<>
NC_PCIR0        31B7<
NC_PCIR1        31B7<
NC_PCITR0       31B6<
```

```
NC_PCITR1       31B6<
NC_PMON_OUT_L   4B3>
NC_PMU_DL_10    29B2<>
NC_PMU_DL_12    29B2<>
NC_PPL*         44C6<
NC_RESET_BUTTON_L  8A8<>
NC_RFBA<12>     18E2<
NC_RFBBA<12>    18A2<
NC_RF_DISABLE_L  59A6>
NC_ROMCS_L      16C8>
NC_RP1PIN4      16B3<
NC_RP1399       30B5<
NC_RP2848       28A8<
NC_RP3319       28D3<
NC_RP3324_2     28C1<
NC_RPT48P1      28D3<
NC_RPT77P6      28B8<
NC_SDOUT2       39C2>
NC_SODIMM71     14C5<>
NC_SODIMM72     14C4<>
NC_SODIMM73     14C5<>
NC_SODIMM74     14C4<>
NC_SODIMM77     14C5<>
NC_SODIMM78     14C4<>
NC_SODIMM79     14C5<>
NC_SODIMM80     14C4<>
NC_SODIMM83     14C5<>
NC_SODIMM84     14C4<>
NC_SODIMM85     14C5<>
NC_SODIMM86     14C4<>
NC_SODIMM89     14C5<>
NC_SODIMM91     14C5<>
NC_SODIMM97     14B5<>
NC_SODIMM98     14B4<>
NC_SODIMM123    14B5<>
NC_SODIMM124    14B4<>
NC_SODIMM199    14A5<>
NC_SODIMM200    14A4<>
NC_SODIMM201    14D5<>
NC_SODIMM202    14A6<>
NC_SW3V5V_33OUT  50C6<
NC_SYSCLK_DDRCLK_A2  12B4<
NC_SYSCLK_DDRCLK_A2_L  12B4<
NC_TAS_SDOUT1   39C2>
NC_TESTMODE     8A4<>
NC_TMDS_TXD3M   23C3>
NC_TMDS_TXD3P   23C3>
NC_TMDS_TXD7M   23C3>
NC_TMDS_TXD7P   23C3>
NC_TX1_1        35C3<
NC_TX1_2        35C3<
NC_TX1_3        35C2<
NC_TX1_4        35C2<
NC_UB3P4        35D5<>
NC_USB2_AMC     32A4<
NC_USB2_NANDTEST  32A4<
NC_USB2_NTEST1  32A4<
NC_USB2_PPON1   32B4>
NC_USB2_PPON2   32B4>
NC_USB2_PPON3   32B4>
NC_USB2_PPON4   32B4>
NC_USB2_PPON5   32B4>
NC_USB2_RSDEM   32C4>
NC_USB2_RSDEP   32C4>
NC_USB2_RSDFM   32C4>
NC_USB2_RSDFP   32B4>
NC_USB2_SMC     32A4<
NC_USB2_SMI_L   32A6>
NC_USB2_SRCLK   32A4>
NC_USB2_SRDTA   32A4<>
NC_USB2_SRMOD   32A4<
NC_USB2_TEB     32A4<
NC_USB2_TEST    32A4<
NC_USB_M        31B2<>
NC_USB_P        31B2<>
NC_UT6P6        28D8<>
NC_UT6P7        28D8<>
NC_UT164        44D7<>
NC_UT165        44D7<>
NC_VCORE10      45D6<
NC_VIPHCLK      22D5>
NC_VR4          39D6<
NC_VTT<0>       18G7<
NC_VTT<1>       18G7<
NC_VTT<2>       18G7<
NC_VTT<3>       18G7<
NC_VTT<4>       18G7<
NC_VTT<5>       18G7<
NC_VTT<6>       18G7<
NC_VTT<7>       18G7<
NC_VTT<8>       18G7<
NC_VTT<9>       18F7<
NC_VTT<10>      18F7<
NC_VTT<11>      18F7<
NC_WL<1>        31B3<>
NC_WL<2>        31B2<>
NC_WL<3>        31B3<>
NC_WL<4>        31B2<>
NC_WL<5>        31B3<>
NC_WL<6>        31B2<>
NC_WL<7>        31B3<>
NC_WL<8>        31B2<>
NC_WL<9>        31B3<>
NC_WL<10>       31B2<>
NC_WL<11>       31B3<>
NC_WL<12>       31B2<>
NC_WL<13>       31B3<>
NC_WL<14>       31B2<>
NC_WL<15>       31B3<>
NC_WL<16>       31B2<>
```

```
NC_WL<17>       31B3<>
NC_WL<18>       31B2<>
NC_WL<19>       31B3<>
NC_WL<20>       31B2<>
NC_WL<21>       31B3<>
NC_WL<23>       31B3<>
NC_XTLINO       39B4<
NEC_AVDD        32D5< 52A3>
NEC_XT2_B       32D3<
NET18           44D6<>
NET19           44D6<>
NET22           44D8<>
NET24           44D8<>
NET32           42A5<
NET32_B         42A5<>
NET40           44B4<>
NMI_BUTTON*     29B2<> 44C4<> 59D6>
NV11_HSYNC      22C4<> 26D3<
NV11_VSYNC      22C4<> 26D3<
NV11_XTALIN     22B4<> 57D5>
NV11_XTALOUT    22B4<> 57D5>
NVAGP_TCLK      17A5<>
NVAGP_TDI       17A5<>
NVAGP_TMS       17A5<>
NVAGP_TRST_L    17A5<>
NVPLLVDD        22D5< 52A6>
NV_BLUE2        22C1<> 22C1<>
NV_GPIOD0       23D4<>
NV_GPIOD2       23D4<>
NV_GPIOD5       23D4<>
NV_GPIOD7       22A8< 23D5<>
NV_GPIOD8       22A6< 23D5<>
NV_GPIOD9       23C4<>
NV_GREEN2       22C1<> 22C1<>
NV_PCI_RST_L    17C7<
NV_RED2         22C1<> 22C1<>
OGAL            41D7<
OGAR            41C7<
OGND3_JTAG_EN   35A5<>
OPA_STAR_GND    39A7<> 39D6< 40C2< 43A3<
OPA_VREF        40B3< 43A4<>
OUT_R           59B6>
OVDD_ADJ        59C8>
PB_AUD          41B4<
PB_GAL          41B4<
PCIT_AD<0>      31B2<> 31C6<
PCIT_AD<31..0>  54C7<
PCIT_AD<1>      31B3<> 31C6< 59C3>
PCIT_AD<2>      31B2<> 31C6< 59C3>
PCIT_AD<3>      31B3<> 31C6< 59C3>
PCIT_AD<4>      31B2<> 31C6<
PCIT_AD<5>      31B3<> 31C6< 59C3>
PCIT_AD<6>      31B2<> 31C6<
PCIT_AD<7>      31B3<> 31C6< 59C3>
PCIT_AD<8>      31B2<> 31C6<
PCIT_AD<9>      31B3<> 31C6< 59C3>
PCIT_AD<10>     31B2<> 31C6<
PCIT_AD<11>     31B2<> 31C6< 59C3>
PCIT_AD<12>     31B3<> 31C6< 59C3>
PCIT_AD<13>     31B2<> 31C6<
PCIT_AD<14>     31C3<> 31C6< 59B3>
PCIT_AD<15>     31C2<> 31C6<
PCIT_AD<16>     31C2<> 31C6<
PCIT_AD<17>     31C3<> 31C7< 59B3>
PCIT_AD<18>     31C2<> 31C6<
PCIT_AD<19>     31C3<> 31C7< 59B3>
PCIT_AD<20>     31C2<> 31C7<
PCIT_AD<21>     31C3<> 31C6< 59B3>
PCIT_AD<22>     31C2<> 31C7<
PCIT_AD<23>     31C3<> 31C6< 59B3>
PCIT_AD<24>     31B7< 31C2<>
PCIT_AD<25>     31B6< 31C3<> 59B3>
PCIT_AD<26>     31B7< 31C2<>
PCIT_AD<27>     31B6< 31C3<> 59B3>
PCIT_AD<28>     31B7< 31C2<> 59B3>
PCIT_AD<29>     31B6< 31C3<> 59B3>
PCIT_AD<30>     31B7< 31C2<>
PCIT_AD<31>     31B6< 31C3<> 59B3>
PCIT_CBE<0>     31B2<> 31B6<
PCIT_CBE<31..0>  54C7<
PCIT_CBE<1>     31B6< 31C3<> 59A6>
PCIT_CBE<2>     31B6< 31C3<> 59A6>
PCIT_CBE<3>     31B6< 31C3<> 59A6>
PCIT_DEVSEL_L   31B6< 31C2<> 54C7<
PCIT_FRAME_L    31B6< 31C2<> 54C7<
PCIT_IRDY_L     31B6< 31C3<> 54C7< 59B6>
PCIT_PAR        31B6< 31C2<> 54C7<
PCIT_STOP_L     31B6< 31C2<> 54C7<
PCIT_TRDY_L     31B6< 31C2<> 54C7<
PCI_AD<0>       30C2< 30D4<> 31C7< 32C6<> 59C3>
PCI_AD<31..0>   53A6<
PCI_AD<1>       30C2< 30D4<> 31C7< 32C6<>
PCI_AD<2>       30C2< 30D4<> 31C7< 32C6<>
PCI_AD<3>       30C2< 30D4<> 31C7< 32C6<>
PCI_AD<4>       30C2< 30D4<> 31C7< 32C6<> 59C3>
PCI_AD<5>       30C2< 30D4<> 31C7< 32C6<>
PCI_AD<6>       30C2< 30D4<> 31C7< 32C6<> 59C3>
PCI_AD<7>       30C2< 30D4<> 31C7< 32C6<>
PCI_AD<8>       30C2< 30D4<> 31C7< 32C6<>
PCI_AD<9>       30C2< 30D4<> 31C7< 32C6<> 59C3>
PCI_AD<10>      30C2< 30C4<> 31C7< 32C6<>
PCI_AD<11>      30B2< 30C4<> 31C7< 32C6<> 59C3>
PCI_AD<12>      30B2< 30C4<> 31C7< 32C6<>
PCI_AD<13>      30B2< 30C4<> 31C7< 32C6<> 59C3>
PCI_AD<14>      30B2< 30C4<> 31C7< 32C6<>
PCI_AD<15>      30B2< 30C4<> 31C7< 32C6<> 59B3>
PCI_AD<16>      30B2< 30C4<> 31C7< 32C6<> 59B3>
PCI_AD<17>      30B2< 30C4<> 31C6< 32C6<>
PCI_AD<18>      30B2< 30C4<> 31C7< 32C6<> 59B3>
PCI_AD<19>      30B2< 30C4<> 31C6< 32C6<>
```

```
PCI_AD<20>      30B2< 30C4<> 31C6< 32C6<> 59B3>
PCI_AD<21>      30C4<> 31C7< 32C6<>
PCI_AD<22>      30C4<> 31C6< 32C6<> 59B3>
PCI_AD<23>      30C4<> 31C7< 32C6<>
PCI_AD<24>      30C1<> 30C4<> 31B6< 32C6<> 59B3>
PCI_AD<25>      30C1<> 30C4<> 31B7< 32C6<>
PCI_AD<26>      30C1<> 30C4<> 31B6< 32B6<> 59B3>
PCI_AD<27>      30C1<> 30C4<> 31B7< 32B7<>
PCI_AD<28>      30C1<> 30C4<> 31B6< 32B6<>
PCI_AD<29>      30C1<> 30C4<> 31B7< 32B6<>
PCI_AD<30>      30C1<> 30C4<> 31B6< 32B6<> 59B3>
PCI_AD<31>      30C1<> 30C4<> 31B7< 32B6<>
PCI_CBE<0>      30C5<> 31B7< 32B6<> 59A6>
PCI_CBE<3..0>   53A6<
PCI_CBE<1>      30C5<> 31B7< 32B6<>
PCI_CBE<2>      30C5<> 31B7< 32B6<>
PCI_CBE<3>      30C5<> 31B7< 32B6<>
PCI_DEVSEL_L    30B7< 30C5<> 31B7< 32B6<> 54D7<
                59A6>
PCI_FBI_EQUAL   30C7< 54C7<
PCI_FBI_PLUS2   30C8< 54C7<
PCI_FBO_PLUS2   30D8< 54D7<
PCI_FB_PLUS4    30C8< 54C7<
PCI_FB_PLUS6    30C7< 54C7<
PCI_FRAME_L     30B7< 30C5<> 31B7< 32B6<> 53A6<
                59A6>
PCI_IRDY_L      30B7< 30C5<> 31B7< 32B6<> 54D7<
PCI_PAR         30C5<> 31B7< 32B6<> 54D7< 59A6>
PCI_SLOTB_GNT_L  30B5< 30D5<> 31C2<> 59A6>
PCI_SLOTB_REQ_L  30B7< 30D5<> 31C3<> 59A6>
PCI_SLOTC_GNT_L  30B5< 30D5<>
PCI_SLOTC_REQ_L  30B7< 30D5<>
PCI_SLOTD_GNT_L  30B5< 30D5<> 32B6<
PCI_SLOTD_PERR_L  32B6<>
PCI_SLOTD_REQ_L  30B7< 30D5<> 32B6>
PCI_STOP_L      30B7< 30C5<> 31B7< 32B6<> 54D7<
                59A6>
PCI_TRDY_L      30B7< 30C5<> 31B7< 32B6<> 54D7<
                59A6>
PGOOD           49B7< 49B7< 50A6>
PG_E            45B6<
PMURESETBUTTON*  44A4< 44A4< 59D6>
PMU_5V_SCL      44C3<>
PMU_5V_SDA      44C3<>
PMU_ACK_L       28C3< 44C4<>
PMU_AGP_RESET   44C4<>
PMU_AP          29B3<> 44D4<>
PMU_AVCC        44B5< 44D4<> 52B3> 59C6>
PMU_BYTE        44B5<
PMU_CLK         28C3<> 44C4<>
PMU_CLKIN       44B4<> 58A5>
PMU_CLKOUT      44B4<> 58A5>
PMU_CLKT        44B2<> 58A5>
PMU_CNVSS       29B3<> 44B5<
PMU_EPM*        29B3<> 44C4<>
PMU_FROM_INT    28C3<> 44C4<>
PMU_IIC_CLK     44A8< 44B4<>
PMU_IIC_DAT     44A8< 44B4<>
PMU_INT_L       28B5<> 28B8< 44B5<>
PMU_INT_NMI     28A8< 28B5<> 44C4<>
PMU_LOW_DSKTP   44B5<>
PMU_NMI         44B4<>
PMU_P64         29B2<> 44C2<>
PMU_PME_L       28B5<> 31C2< 32A8< 44B2<> 59A6>
PMU_PME_LL      31C2<>
PMU_POWER       29C3<> 44A5<> 44B1< 44C2< 44D5<>
                52B3>
PMU_PRE_PLLSTOP  44B5<>
PMU_PWR_LED*    44C5<>
PMU_REQ_L       28A8< 28C3> 44C2<
PMU_RST*        8A8<> 29B3<> 44A5<> 44B5<> 59D6>
PMU_SMB_SCK     44A3<>
PMU_SMB_SDA     44A3<>
PMU_STRAP1      44C5<>
PMU_TO_INT      28C3<> 44C4<>
PMU_XI          44B5< 58A5>
PMU_XO          44B5< 58A5>
PMU_XT          44A6< 58A5>
POWERUP_OK      44B4<>
POWER_UP*       44C7<> 51A8< 59D6>
PRESPK_LOUTN    42C7<
PRESPK_LOUTP    42C7<
PRESPK_ROUTN    42C3<
PRESPK_ROUTP    42C3<
PROBE_DIV       41B4< 41D7<
PSEUDO_STAR_GND  39B7<> 40B4<
PWR_FAIL*       44B1<> 50D5<
PWR_FAILPMU*    44B4<>
PWR_FAIL_T      50D6<>
PWR_LED         51A4<
PWR_SWITCH*     8A8<> 44B1< 44C5<> 59D6> 59D6>
PWR_UP          39C8< 42D8< 50C3< 50C8< 51C6<
                59D6>
PWR_UP*         50D7<>
Q1P1            51C3<
Q1P3            51D3<
Q2_GATE         42D7<
Q25_1           41A5<
Q42P4           51D3<>
QT1P1           48A4<>
QT2P1           48B4<>
QT2P3           48B4<>
R264P2          39B4<
RAM_ADDR<0>     12C3< 14B4<> 15B6<
RAM_ADDR<0..12>  53D6<
RAM_ADDR<1>     12C3< 14B6<> 15B6<
RAM_ADDR<2>     12C3< 14B4<> 15C6<
RAM_ADDR<3>     12D3< 14B6<> 15C4>
RAM_ADDR<4>     12D3< 14B4<> 15C6<
RAM_ADDR<5>     12C1< 14B6<> 15C6<
```

	8	7	6	5	4	3	2	1	
D	RAM_ADDR<6> 12D1< 14B4<> 15C4> RAM_ADDR<7> 12D3< 14B6<> 15C6> RAM_ADDR<8> 12D1< 14B4<> 15C4> RAM_ADDR<9> 12C3< 14B6<> 15C6> RAM_ADDR<10> 12C3< 14B6<> 15B4> RAM_ADDR<11> 12B3< 14B4<> 15C4> RAM_ADDR<12> 12D1< 14B6<> 15C4> RAM_BA<0> 12B3< 14B6<> 15B6> RAM_BA<0..1> 53D6 RAM_BA<1> 12B3< 14B4<> 15B6> RAM_CAS_L 12A2< 14B4<> 15B6< 53C6> RAM_CKE<0> 12C1< 14B4<> 15C1 RAM_CKE<0..1> 53C6 RAM_CKE<1> 12B1< 14B6<> 15C1 RAM_CKE<2> 12C1< 15B1< 15C6 RAM_CKE<2..3> 53C6 RAM_CKE<3> 12B1< 15A1< 15C4> RAM_CS_L<0> 12C1< 14B6 RAM_CS_L<0..1> 53C6 RAM_CS_L<1> 12C1< 14B4 RAM_CS_L<2> 12B1< 15B4> RAM_CS_L<2..3> 53C6 RAM_CS_L<3> 12B1< 15B4> RAM_DATA_A<0> 13D7<> 14D6 RAM_DATA_A<0..63> 53D6 RAM_DATA_A<1> 13D7<> 14D6 RAM_DATA_A<2> 13D7<> 14D6 RAM_DATA_A<3> 13D7<> 14D6 RAM_DATA_A<4> 13D7<> 14D4 RAM_DATA_A<5> 13D7<> 14D4 RAM_DATA_A<6> 13D7<> 14D4 RAM_DATA_A<7> 13D7<> 14D4 RAM_DATA_A<8> 13C7<> 14D6 RAM_DATA_A<9> 13C7<> 14D6 RAM_DATA_A<10> 13C7<> 14D6 RAM_DATA_A<11> 13C7<> 14D6 RAM_DATA_A<12> 13C7<> 14D4 RAM_DATA_A<13> 13C7<> 14D4 RAM_DATA_A<14> 13C7<> 14D4 RAM_DATA_A<15> 13C7<> 14D4 RAM_DATA_A<16> 13B5<> 14D6 RAM_DATA_A<17> 13B5<> 14C6 RAM_DATA_A<18> 13B5<> 14C6 RAM_DATA_A<19> 13B5<> 14C6 RAM_DATA_A<20> 13B5<> 14D4 RAM_DATA_A<21> 13B5<> 14C4 RAM_DATA_A<22> 13B5<> 14C4 RAM_DATA_A<23> 13B5<> 14C4 RAM_DATA_A<24> 13B5<> 14C6 RAM_DATA_A<25> 13B5<> 14C6 RAM_DATA_A<26> 13B5<> 14C6 RAM_DATA_A<27> 13B5<> 14C6 RAM_DATA_A<28> 13B5<> 14C4 RAM_DATA_A<29> 13B5<> 14C4 RAM_DATA_A<30> 13B5<> 14C4 RAM_DATA_A<31> 13B5<> 14C4 RAM_DATA_A<32> 13D4<> 14B6 RAM_DATA_A<33> 13D4<> 14B6 RAM_DATA_A<34> 13D4<> 14B6 RAM_DATA_A<35> 13D4<> 14B6 RAM_DATA_A<36> 13D4<> 14B4 RAM_DATA_A<37> 13D4<> 14B4 RAM_DATA_A<38> 13D4<> 14B4 RAM_DATA_A<39> 13D4<> 14B4 RAM_DATA_A<40> 13D4<> 14B6 RAM_DATA_A<41> 13C4<> 14B6 RAM_DATA_A<42> 13C4<> 14A6 RAM_DATA_A<43> 13C4<> 14A6 RAM_DATA_A<44> 13C4<> 14B4 RAM_DATA_A<45> 13C4<> 14B4 RAM_DATA_A<46> 13C4<> 14A4 RAM_DATA_A<47> 13C4<> 14A4 RAM_DATA_A<48> 13C2<> 14A6 RAM_DATA_A<49> 13C2<> 14A6 RAM_DATA_A<50> 13C2<> 14A6 RAM_DATA_A<51> 13C2<> 14A6 RAM_DATA_A<52> 13C2<> 14A4 RAM_DATA_A<53> 13C2<> 14A4 RAM_DATA_A<54> 13B2<> 14A4 RAM_DATA_A<55> 13B2<> 14A4 RAM_DATA_A<56> 13B2<> 14A6 RAM_DATA_A<57> 13B2<> 14A6 RAM_DATA_A<58> 13B2<> 14A6 RAM_DATA_A<59> 13B2<> 14A6 RAM_DATA_A<60> 13B2<> 14A4 RAM_DATA_A<61> 13B2<> 14A4 RAM_DATA_A<62> 13B2<> 14A4 RAM_DATA_A<63> 13B2<> 14A4 RAM_DATA_B<0> 13C7<> 15D6 RAM_DATA_B<0..63> 53D6 RAM_DATA_B<1> 13C7<> 15D6 RAM_DATA_B<2> 13C7<> 15D6 RAM_DATA_B<3> 13C7<> 15D6 RAM_DATA_B<4> 13C7<> 15D4> RAM_DATA_B<5> 13C7<> 15D4> RAM_DATA_B<6> 13C7<> 15D4> RAM_DATA_B<7> 13C7<> 15D4> RAM_DATA_B<8> 13C7<> 15D6 RAM_DATA_B<9> 13C7<> 15D6 RAM_DATA_B<10> 13C7<> 15C6 RAM_DATA_B<11> 13C7<> 15C6 RAM_DATA_B<12> 13C7<> 15D4> RAM_DATA_B<13> 13B7<> 15D4> RAM_DATA_B<14> 13B7<> 15C4> RAM_DATA_B<15> 13B7<> 15C4> RAM_DATA_B<16> 13A5<> 15C6> RAM_DATA_B<17> 13A5<> 15C6> RAM_DATA_B<18> 13A5<> 15C6> RAM_DATA_B<19> 13A5<> 15C6> RAM_DATA_B<20> 13A5<> 15C4>	RAM_DATA_B<21> 13A5<> 15C4> RAM_DATA_B<22> 13A5<> 15C4> RAM_DATA_B<23> 13A5<> 15C4> RAM_DATA_B<24> 13A5<> 15C6> RAM_DATA_B<25> 13A5<> 15C6> RAM_DATA_B<26> 13A5<> 15C6> RAM_DATA_B<27> 13A5<> 15C6> RAM_DATA_B<28> 13A5<> 15C4> RAM_DATA_B<29> 13A5<> 15C4> RAM_DATA_B<30> 13A5<> 15C4> RAM_DATA_B<31> 13A5<> 15C4> RAM_DATA_B<32> 13C4<> 15B6> RAM_DATA_B<33> 13C4<> 15B6> RAM_DATA_B<34> 13C4<> 15B6> RAM_DATA_B<35> 13C4<> 15B6> RAM_DATA_B<36> 13C4<> 15B4> RAM_DATA_B<37> 13C4<> 15B4> RAM_DATA_B<38> 13C4<> 15B4> RAM_DATA_B<39> 13C4<> 15B4> RAM_DATA_B<40> 13C4<> 15B6> RAM_DATA_B<41> 13C4<> 15B6> RAM_DATA_B<42> 13C4<> 15A6> RAM_DATA_B<43> 13C4<> 15A6> RAM_DATA_B<44> 13C4<> 15B4> RAM_DATA_B<45> 13C4<> 15B4> RAM_DATA_B<46> 13B4<> 15A4> RAM_DATA_B<47> 13B4<> 15A4> RAM_DATA_B<48> 13B2<> 15A6> RAM_DATA_B<49> 13B2<> 15A6> RAM_DATA_B<50> 13B2<> 15A6> RAM_DATA_B<51> 13B2<> 15A6> RAM_DATA_B<52> 13B2<> 15A4> RAM_DATA_B<53> 13B2<> 15A4> RAM_DATA_B<54> 13B2<> 15A4> RAM_DATA_B<55> 13B2<> 15A4> RAM_DATA_B<56> 13B2<> 15A6> RAM_DATA_B<57> 13A2<> 15A6> RAM_DATA_B<58> 13A2<> 15A6> RAM_DATA_B<59> 13A2<> 15A6> RAM_DATA_B<60> 13A2<> 15A4> RAM_DATA_B<61> 13A2<> 15A4> RAM_DATA_B<62> 13A2<> 15A4> RAM_DATA_B<63> 13A2<> 15A4> RAM_DQM_A<0> 13D7<> 14D4> RAM_DQM_A<0..7> 53D6 RAM_DQM_A<1> 13C7<> 14D4> RAM_DQM_A<2> 13B5<> 14C4> RAM_DQM_A<3> 13A5<> 14C4> RAM_DQM_A<4> 13D4<> 14B4> RAM_DQM_A<5> 13C4<> 14A4> RAM_DQM_A<6> 13B2<> 14A4> RAM_DQM_A<7> 13B2<> 14A4> RAM_DQM_B<0> 13C7<> 15D4> RAM_DQM_B<0..7> 53D6 RAM_DQM_B<1> 13B7<> 15D4> RAM_DQM_B<2> 13A5<> 15C4> RAM_DQM_B<3> 13A5<> 15C4> RAM_DQM_B<4> 13C4<> 15B4> RAM_DQM_B<5> 13B4<> 15B4> RAM_DQM_B<6> 13B2<> 15A4> RAM_DQM_B<7> 13A2<> 15A4> RAM_DQS_A<0> 13D7<> 14C8< 14D6> RAM_DQS_A<0..7> 53D6 RAM_DQS_A<1> 13C7<> 14C8< 14D6> RAM_DQS_A<2> 13B5<> 14C6<> 14C8 RAM_DQS_A<3> 13B5<> 14C6<> 14C8 RAM_DQS_A<4> 13D4<> 14B6<> 14B8 RAM_DQS_A<5> 13C4<> 14A6<> 14B8 RAM_DQS_A<6> 13B2<> 14A6<> 14B8 RAM_DQS_A<7> 13B2<> 14A6<> 14A8 RAM_DQS_B<0> 13C7<> 15C8< 15D6 RAM_DQS_B<0..7> 53D6 RAM_DQS_B<1> 13B7<> 15C8< 15D6 RAM_DQS_B<2> 13A5<> 15C6< 15C8 RAM_DQS_B<3> 13A5<> 15B8< 15C6 RAM_DQS_B<4> 13C4<> 15B6< 15B8 RAM_DQS_B<5> 13B4<> 15B6< 15B8 RAM_DQS_B<6> 13B2<> 15A6< 15B8 RAM_DQS_B<7> 13A2<> 15A6< 15A8 RAM_RAS_L 12A2< 14B4<> 15B4> 53C6 RAM_SA0 15A4 RAM_WE_L 12B3< 14B6<> 15B6< 53C6 RB22P2 48B3 RB27-1 48B6 RB37P1 48C6 RB160P1 50A5 RB213P2 49C3 RB227P1 49C5 REF_STAR_GND 39A5<> 39A5 RESET_BUTTON* 29B2<> 44C4<> 59D6> RFBA<0> 18F2<> 20D2< 20D6 RFBA<0..11> 55D3> RFBA<1> 18F2<> 20C2< 20C6 RFBA<2> 18F2<> 20C2< 20C6 RFBA<3> 18F2<> 20C2< 20C6 RFBA<4> 18F2<> 20C2< 20C6 RFBA<5> 18F2<> 20C2< 20C6 RFBA<6> 18E2<> 20C2< 20C6 RFBA<7> 18E2<> 20C2< 20C6 RFBA<8> 18E2<> 20C2< 20C6 RFBA<9> 18E2<> 20C2< 20C6 RFBA<10> 18E2<> 20C2< 20C6 RFBA<11> 18E2<> 20C2< 20C6 RFBABA<0> 18E2<> 20C2< 20C6 RFBABA<0..1> 55D3> RFBABA<1> 18E2<> 20C2< 20D6 RFBACAS_L 18G2<> 20B2< 20B6< 55D3> RFBACKE 18D2<> 20C2< 20C6< 55C3> RFBACLK0 19C1< 20C6< 55C3> RFBACLK0_L 19C1< 20C6< 55C3>	RFBACLK1 19D1< 20C2< 55C3> RFBACLK1_L 19D1< 20C2< 55C3> RFBACS0_L 18F2<> 20B2< 20B6< 55C3> RFBARAS_L 18G2<> 20B2< 20B6< 55D3> RFBAWE_L 18F2<> 20B2< 20B6< 55D3> RFBBA<0> 18C2<> 21D2< 21D6 RFBBA<0..11> 55C3> RFBBA<1> 18B2<> 21C2< 21C6 RFBBA<2> 18B2<> 21C2< 21C6 RFBBA<3> 18B2<> 21C2< 21C6 RFBBA<4> 18B2<> 21C2< 21C6 RFBBA<5> 18B2<> 21C2< 21C6 RFBBA<6> 18B2<> 21C2< 21C6 RFBBA<7> 18B2<> 21C2< 21C6 RFBBA<8> 18B2<> 21C2< 21C6 RFBBA<9> 18B2<> 21C2< 21C6 RFBBA<10> 18B2<> 21C2< 21C6 RFBBA<11> 18B2<> 21C2< 21C6 RFBBBA<0> 18A2<> 21C2< 21C6 RFBBBA<0..1> 55C3> RFBBBA<1> 18A2<> 21C2< 21C6 RFBBCAS_L 18C2<> 21B2< 21B6< 55B3> RFBBCKE 18A2<> 21C2< 21C6< 55B3> RFBBCLK0 19B1< 21C6< 55B3> RFBBCLK0_L 19B1< 21C6< 55B3> RFBBCLK1 19C1< 21C2< 55B3> RFBBCLK1_L 19B1< 21C2< 55B3> RFBBCS0_L 18C2<> 21B2< 21B6< 55B3> RFBBRAS_L 18C2<> 21B2< 21B6< 55B3> RFBBWE_L 18C2<> 21B2< 21B6< 55B3> RFBD<0> 19D7< 20C5> RFBD<0..63> 55D3> RFBD<1> 19D7< 20C5> RFBD<2> 19D7< 20C5> RFBD<3> 19D7< 20C5> RFBD<4> 19D7< 20C5> RFBD<5> 19D7< 20C5> RFBD<6> 19D7< 20C5> RFBD<7> 19D7< 20C5> RFBD<8> 19D7< 20C5> RFBD<9> 19D7< 20C5> RFBD<10> 19D7< 20C5> RFBD<11> 19D7< 20C5> RFBD<12> 19D7< 20C5> RFBD<13> 19D7< 20C5> RFBD<14> 19D7< 20C5> RFBD<15> 19D7< 20C5> RFBD<16> 19D7< 20C5> RFBD<17> 19D7< 20C5> RFBD<18> 19D7< 20C5> RFBD<19> 19C7< 20C5> RFBD<20> 19C7< 20C5> RFBD<21> 19C7< 20C5> RFBD<22> 19C7< 20C5> RFBD<23> 19C7< 20C5> RFBD<24> 19C7< 20C5> RFBD<25> 19C7< 20C5> RFBD<26> 19C7< 20B5> RFBD<27> 19C7< 20B5> RFBD<28> 19C7< 20B5> RFBD<29> 19C7< 20B5> RFBD<30> 19C7< 20B5> RFBD<31> 19C7< 20B5> RFBD<32> 19D4< 20C1> RFBD<33> 19D4< 20C1> RFBD<34> 19D4< 20C1> RFBD<35> 19D4< 20C1> RFBD<36> 19D4< 20C1> RFBD<37> 19D4< 20C1> RFBD<38> 19D4< 20C1> RFBD<39> 19D4< 20C1> RFBD<40> 19D4< 20C1> RFBD<41> 19D4< 20C1> RFBD<42> 19D4< 20C1> RFBD<43> 19D4< 20C1> RFBD<44> 19D4< 20C1> RFBD<45> 19D4< 20C1> RFBD<46> 19D4< 20C1> RFBD<47> 19D4< 20C1> RFBD<48> 19D4< 20C1> RFBD<49> 19D4< 20C1> RFBD<50> 19D4< 20C1> RFBD<51> 19C4< 20C1> RFBD<52> 19C4< 20C1> RFBD<53> 19C4< 20C1> RFBD<54> 19C4< 20C1> RFBD<55> 19C4< 20C1> RFBD<56> 19C4< 20C1> RFBD<57> 19C4< 20C1> RFBD<58> 19C4< 20B1> RFBD<59> 19C4< 20B1> RFBD<60> 19C4< 20B1> RFBD<61> 19C4< 20B1> RFBD<62> 19C4< 20B1> RFBD<63> 19C4< 20B1> RFBD<64> 19C7< 21C5> RFBD<64..127> 55C3> RFBD<65> 19C7< 21C5> RFBD<66> 19C7< 21C5> RFBD<67> 19C7< 21C5> RFBD<68> 19C7< 21C5> RFBD<69> 19C7< 21C5> RFBD<70> 19C7< 21C5> RFBD<71> 19C7< 21C5> RFBD<72> 19C7< 21C5> RFBD<73> 19C7< 21C5> RFBD<74> 19B7< 21C5> RFBD<75> 19B7< 21C5> RFBD<76> 19B7< 21C5> RFBD<77> 19B7< 21C5>	RFBD<78> 19B7< 21C5> RFBD<79> 19B7< 21C5> RFBD<80> 19B7< 21C5> RFBD<81> 19B7< 21C5> RFBD<82> 19B7< 21C5> RFBD<83> 19B7< 21C5> RFBD<84> 19B7< 21C5> RFBD<85> 19B7< 21C5> RFBD<86> 19B7< 21C5> RFBD<87> 19B7< 21C5> RFBD<88> 19B7< 21C5> RFBD<89> 19B7< 21C5> RFBD<90> 19B7< 21B5> RFBD<91> 19B7< 21B5> RFBD<92> 19B7< 21B5> RFBD<93> 19B7< 21B5> RFBD<94> 19B7< 21B5> RFBD<95> 19B7< 21B5> RFBD<96> 19C4< 21C1> RFBD<97> 19C4< 21C1> RFBD<98> 19C4< 21C1> RFBD<99> 19C4< 21C1> RFBD<100> 19C4< 21C1> RFBD<101> 19C4< 21C1> RFBD<102> 19C4< 21C1> RFBD<103> 19C4< 21C1> RFBD<104> 19C4< 21C1> RFBD<105> 19C4< 21C1> RFBD<106> 19B4< 21C1> RFBD<107> 19B4< 21C1> RFBD<108> 19B4< 21C1> RFBD<109> 19B4< 21C1> RFBD<110> 19B4< 21C1> RFBD<111> 19B4< 21C1> RFBD<112> 19B4< 21C1> RFBD<113> 19B4< 21C1> RFBD<114> 19B4< 21C1> RFBD<115> 19B4< 21C1> RFBD<116> 19B4< 21C1> RFBD<117> 19B4< 21C1> RFBD<118> 19B4< 21C1> RFBD<119> 19B4< 21C1> RFBD<120> 19B4< 21C1> RFBD<121> 19B4< 21C1> RFBD<122> 19B4< 21B1> RFBD<123> 19B4< 21B1> RFBD<124> 19B4< 21B1> RFBD<125> 19B4< 21B1> RFBD<126> 19B4< 21B1> RFBD<127> 19B4< 21B1> RFBDQM<0> 18G2< 20C6> RFBDQM<0..7> 55D3> RFBDQM<1> 18G2< 20C6> RFBDQM<2> 18G2< 20C6> RFBDQM<3> 18G2< 20C6> RFBDQM<4> 18G2< 20C2> RFBDQM<5> 18G2< 20C2> RFBDQM<6> 18G2< 20C2> RFBDQM<7> 18G2< 20C2> RFBDQM<8> 18D2< 21C6> RFBDQM<8..15> 55C3> RFBDQM<9> 18D2< 21C6> RFBDQM<10> 18D2< 21C6> RFBDQM<11> 18D2< 21C6> RFBDQM<12> 18D2< 21C2> RFBDQM<13> 18D2< 21C2> RFBDQM<14> 18C2< 21C2> RFBDQM<15> 18C2< 21C2> RFBDQS<0> 19A6< 20C6> RFBDQS<0..7> 55C3> RFBDQS<1> 19A6< 20C6> RFBDQS<2> 19A6< 20C6> RFBDQS<3> 19A6< 20C6> RFBDQS<4> 19A6< 20C2> RFBDQS<5> 19A6< 20C2> RFBDQS<6> 19A6< 20C2> RFBDQS<7> 19A6< 20C2> RFBDQS<8> 19A3< 21C6> RFBDQS<8..15> 55B3> RFBDQS<9> 19A3< 21C6> RFBDQS<10> 19A3< 21C6> RFBDQS<11> 19A3< 21C6> RFBDQS<12> 19A3< 21C2> RFBDQS<13> 19A3< 21C2> RFBDQS<14> 19A3< 21C2> RFBDQS<15> 19A3< 21C2> RF_CLKRUN_L 31C3<> 59B6> RF_DISABLE_L 31C3> RINA 39C4< 40B2 RINN 42C4< 43C2 RINN1 43C2 RINP 42C4< 43D4 RINT_PU_RESET_L 34C5 RINT_RESET_L 34C5 RJ45_4_5 35C1<> 57B5> RJ45_7_8 35C1<> 57B5> RJ45_F_TREF 35B2< 57B5> RJ45_RREF 35C2<> 57B5> RJ45_RXN 35C1<> 57B5> RJ45_RXP 35C1<> 57B5> RJ45_TREF 35C2<> 57B5> RJ45_TXN 35C1<> 57B5> RJ45_TXP 35C1<> 57B5> ROMA14 18C8> 26D8 ROMA15 18C8< 26D8 ROM_CS_L 30B4< 30C6< 31B4<> 59C8> ROM_OE_L 30B2< 30C6< 31B2<> 59C8> ROM_ONBOARD_CS_L 30B2< 31B4<> 59D6> ROM_RW_L 30B2< 30B6< 31B4<> 59B8> ROM_WP_L 30B2< 59A8>	RT373P1 51A5 RT401P1 47C5<> RT406P2 47B3<> RT418P2 50C7< RUNLED1 51C8< RUNSS 50C8< 50D3< S3700P1 44A1<> S3700P2 44A1<> SB1P1 44A3< SENSE+ 45C6< SENSE+_1 45B5< 45C7< SENSE- 45C6< 45C8<> SENSE-_1 45B5< 45C7< SGRAVREF 20A3< 20C4< 20C8< 52A6> SGRBVREF 21A3< 21C4< 21C8< 52A6> SHS 50C7< SI_EDGE 27C5< SI_EXT_SWING_SET 27B3<> SI_I2C_OFF 27C5< SI_IDCK_M 27B5< SI_SCA 23D2< 27C5< SI_SCL 23D2< 27C5< SI_TMDS_CKM 27C3<> 57C2> SI_TMDS_CKP 27C3<> 57C2> SI_TMDS_D0M 27C3<> 57C2> SI_TMDS_D0P 27C3<> 57C2> SI_TMDS_D1M 27C3<> 57C2> SI_TMDS_D1P 27C3<> 57C2> SI_TMDS_D2M 27C3<> 57C2> SI_TMDS_D2P 27C3<> 57C2> SI_VREF 27B3< SLEEP 44B5<> 50C2< 59C6> SLEEP1 51A8< SLEEP2 51A7< SLEEPLED_TERM 51A6< SLEEP_LED_BD 51A6< SLEEP_OFF_L 51B6< 51C7< SLEEP_OFF_L2 39C7< SND_AMP_MUTE_L 28C5<> 43C8< SND_AMP_M_L 42D3< 43C7<> SND_CLKOUT 28A1< 39B4< SND_HP_MUTE_L 28C5<> 41A7< SND_HP_M_L 41A7<> SND_HP_SENSE_CONN 41A3< 41B2> SND_HP_SENSE_L 28B5<> 41A5< 59B8> SND_HW_RESET_L 28A8< 28B5<> 39B4< SND_LIN_SENSE_L 28B5<> 40D4< 59B6> SND_SCLK 28A1< 39B1<> SND_SPKR_ID 28B5<> 42B8< SND_SPKR_ID_U10 42B8< SND_SYNC 28B1< 39C1<> SND_TO_AUDIO 28B1< 39C4< SNF_FSEL 28C5<> 28D3< SPDA 42B7< SPKROUT_L_N 42A8< 42C8< SPKROUT_L_P 42A8< 42C8< SPKROUT_R_N 42A8< 42C1< SPKROUT_R_P 42A8< 42C1< SPKR_JACK_DALLAS 42A5> SPKR_LM 42A5> SPKR_LP 42A5> SPKR_RM 42A5> SPKR_RMS 42C8< SPKR_RP 42A5> STBYMD 50B7<> STOP_AGP_L 16C6<> 16D3< 17A8< 54B7< SUPER_FLO 45C7<> 45C7<> SW3V5V_12VIN 50C7<> SW3V5V_INTVCC 50B5<> 50C6> SW3V5V_SGND 50A7<> 50A8<> 50B7<> 50B8<> 50B8<> 50C7< SW3V5V_VIN 50C6> SW3VITH2R 50A8< SW3V_3VSENSE 50B4<> SW3V_BG2 50B6> SW3V_BG2R 50B5> SW3V_BOOST2 50B6> SW3V_BOOST2R 50C5> SW3V_ITH2 50A7< 50B6> SW3V_RUNSS 50B6< 50C1< SW3V_RUNSSR 50C2< SW3V_SNSM 50B6< SW3V_SNSP 50B6< SW3V_SW2 50B6<> 50C4> SW3V_SW2A 50B3> SW3V_TG2 50B6> SW3V_TG2R 50C5> SW3V_VOSNS 50B6> SW5VITH1R 50B8< SW5V_5VSENSE 50A4> SW5V_BG1 50A5< 50B7> SW5V_BG1R 50A5> SW5V_BOOST1 50A5< 50B7> SW5V_ITH1 50B7> SW5V_RUNSS 50B8< 50D1< SW5V_SNSM 50A5< 50B7< SW5V_SNSMA 50A4> SW5V_SNSP 50A5< 50B7< SW5V_SW1 50A5<> 50A5<> 50B7<> SW5V_SW1A 50A3> SW5V_TG1 50B5< 50B7> SW5V_TG1R 50B4> SW5V_VOSNS 50B7> SW12V_SL 51C7< SW12V_SLEEP 51D7<> SWITCH5V_3 51B6< SWITCH5V_4 51B6<> SWITCH5V_5 51B3< SWITCH5V_6 51B2> SYSCLK_CPU 4D2< 9A4< 56C3>	SYSCLK_CPU_UF 9A3<> 56C3> SYSCLK_DDRCLK_A0 12C4< 14D6<> 53C6< SYSCLK_DDRCLK_A0_L 12C4< 14D6<> 53C6< SYSCLK_DDRCLK_A0_L_UF 12B6<> 53C6< SYSCLK_DDRCLK_A0_UF 12B6<> 53C6< SYSCLK_DDRCLK_A1 12C4< 14A4<> 53C6< SYSCLK_DDRCLK_A1_L 12B4< 14A4<> 53C6< SYSCLK_DDRCLK_A1_L_UF 12B6<> 53C6< SYSCLK_DDRCLK_A1_UF 12B6<> 53C6< SYSCLK_DDRCLK_A2_L 53B6< SYSCLK_DDRCLK_A2_L_UF 12B6<> 53B6< SYSCLK_DDRCLK_A2_UF 12B6<> 53C6< SYSCLK_DDRCLK_B0 12B4< 15B4> 53B6< SYSCLK_DDRCLK_B0_L 12B4< 15B3> 53B6< SYSCLK_DDRCLK_B0_L_UF 12B6<> 53B6< SYSCLK_DDRCLK_B0_UF 12B6<> 53B6< SYSCLK_DDRCLK_B1 12A4< 15D6< 53B6< SYSCLK_DDRCLK_B1_L 12A4< 15C6< 53B6< SYSCLK_DDRCLK_B1_L_UF 12B6<> 53B6< SYSCLK_DDRCLK_B1_UF 12B6<> 53B6< SYSCLK_DDRCLK_B2 12A4< 15A6< 53B6< SYSCLK_DDRCLK_B2_L 12A4< 15A6< 53B6< SYSCLK_DDRCLK_B2_L_UF 12B6<> 53B6< SYSCLK_DDRCLK_B2_UF 12B6<> 53B6< SYSCLK_LA 8A2< 8D8<> 56B3> SYSTEM_CLK_EN 28A5< 44C4> TAS_DVDD 39D3< TAS_PWR_DOWN 39B4< 39D7< TAS_STAR_GND 39A7<> 39D2< TAS_VCOM 39B1<> 39B1<> 43D5< TCKM 24C3<> 57C5> TCKP 24C4<> 57C5> TD0M 24C4<> 57C5> TD0P 24C3<> 57C5> TD1M 24C3<> 57C5> TD1P 24C4<> 57C5> TD2M 24C4<> 57C5> TD2P 24C3<> 57C5> TESTEN 35A5< 35C4< TI_MODE_OUT 42D4> TI_MODE_OUT_2 42C7< TI_SD* 42D5< TMDS_CKM 23D1< 24A7<> 27C2< 57D2> 59A8> TMDS_CKP 23D1< 24B7<> 27C2< 57D2> 59A8> TMDS_D0M 23D1< 24B7<> 27C2< 57D2> 59A8> TMDS_D0P 23D1< 24B7<> 27C2< 57D2> 59B8> TMDS_D1M 23D1< 24C7<> 27C2< 57D2> 59B8> TMDS_D1P 23D1< 24C7<> 27C2< 57D2> 59B8> TMDS_D2M 23D1< 24D7<> 27C2< 57D2> 59B8> TMDS_D2P 23D1< 24D7<> 27C2< 57D2> 59B8> TMDS_DDC_CLK 24B3<> 59C6> TMDS_DDC_DAT 24B4<> 59C6> TMDS_EN 23D7<> 51B1> TPA_5V 42D4< TPA_AVDD_REF 42D4< TPA_BSLN 42D5> TPA_BSLP 42D5> TPA_BSRN 42D4> TPA_BSRP 42D4> TPA_COSC 42C4> TPA_LOUTN 42C5> TPA_LOUTP 42C5> TPA_MODE 42D4< TPA_ROSC 42C4> TPA_ROUTN 42C4> TPA_ROUTP 42C4> TPA_V2P5 42D5< TPA_VCLAMPL 42C5< TPA_VCLAMPR 42C4< TPA_VOL 42D5< TRANS_ADJ 45B3< T_UD_IDEDD_0 37C1< 38C3<> 58C2> T_UD_IDEDD_1 37C1< 38C3<> 58C2> T_UD_IDEDD_2 37C1< 38C3<> 58C2> T_UD_IDEDD_3 37C1< 38C3<> 58C2> T_UD_IDEDD_4 37B1< 38C3<> 58C2> T_UD_IDEDD_5 37B1< 38C3<> 58C2> T_UD_IDEDD_6 37B1< 38C3<> 58B2> T_UD_IDEDD_7 37B1< 38C3<> 58B2> T_UD_IDEDD_8 37B1< 38C2<> 58B2> T_UD_IDEDD_9 37B1< 38C2<> 58B2> T_UD_IDEDD_10 37B1< 38C2<> 58B2> T_UD_IDEDD_11 37B1< 38C2<> 58B2> T_UD_IDEDD_12 37B1< 38C2<> 58B2> T_UD_IDEDD_13 37A1< 38C2<> 58B2> T_UD_IDEDD_14 37A1< 38C2<> 58B2> T_UD_IDEDD_15 37A1< 38C2<> 58B2> U5_SDOUT 39C3<> U10_A 42C7< U10_OUT 42C7> 42D8< U22_8 36D8< U4202P2 40C3< U4202P3 40C3< U4202P5 40B3< U4202P6 40B3< U4202P7 40B3<> UATA0IRQ 38C6<> 58D5> UATAD<0> 37C4< 38C6> UATAD<0..15> 58D5> UATAD<1> 37C4< 38C6> UATAD<2> 37C4< 38C6> UATAD<3> 37C4< 38C6> UATAD<4> 37B4< 38C6> UATAD<5> 37B4< 38C6> UATAD<6> 37B4< 38C6> UATAD<7> 37B4< 38C6> UATAD<8> 37B4< 38C6> UATAD<9> 37B4< 38C6> UATAD<10> 37B4< 38C6> UATAD<11> 37B4< 38C6>	D
C									C
B									B
A									A
	8	7	6	5	4	3	2	1	

UATAD<12>	37B4< 38C6<>
UATAD<13>	37A4< 38C6<>
UATAD<14>	37A4< 38C6<>
UATAD<15>	37A4< 38C6<>
UIDE_ADDR<0>	37C7<> 38B4<
UIDE_ADDR<0..2>	58B5>
UIDE_ADDR<1>	37C7<> 38B4<
UIDE_ADDR<2>	37C7<> 38A4<
UIDE_CS1FX_L	37C7<> 38B4< 58B5>
UIDE_CS3FX_L	37C7<> 38B4< 58B5>
UIDE_CSELP_L	38C2<> 52A8>
UIDE_DATA<0>	37C3< 37D7<>
UIDE_DATA<0..15>	58C5>
UIDE_DATA<1>	37C3< 37D7<>
UIDE_DATA<2>	37C3< 37D7<>
UIDE_DATA<3>	37C3< 37D7<>
UIDE_DATA<4>	37B3< 37D7<>
UIDE_DATA<5>	37B3< 37D7<>
UIDE_DATA<6>	37B3< 37D7<>
UIDE_DATA<7>	37B3< 37D7<>
UIDE_DATA<8>	37B3< 37D7<>
UIDE_DATA<9>	37B3< 37D7<>
UIDE_DATA<10>	37B3< 37C7<>
UIDE_DATA<11>	37B3< 37C7<>
UIDE_DATA<12>	37B3< 37C7<>
UIDE_DATA<13>	37A3< 37C7<>
UIDE_DATA<14>	37A3< 37C7<>
UIDE_DATA<15>	37A3< 37C7<>
UIDE_DIOR_L	37C7<> 37D3< 58C5>
UIDE_DIOW_L	37C3< 37C7<> 58C5>
UIDE_DMACK_L	37C7<> 37D3< 58C5>
UIDE_DMARQ	37C7<> 38C4< 58C5>
UIDE_INTRQ	37C7< 38C4< 58C5>
UIDE_IOCHRDY	37C3< 37C7< 58C5>
UIDE_PDIAG	38C2<>
UIDE_REF	37C7<>
UIDE_RST_L	37C7<> 37D3< 58C5>
UNUSED_ATAIOCS16_L	38C2<> 52A8>
UNUSED_EXTINT7	28B5<> 28B8<>
UNUSED_EXTINT8	28B5<> 28B8<>
UNUSED_GPIO15	28B5<> 28C1< 59A6>
USB2_CRUN_L	32A6<>
USB2_CRUN_L_INT	28A8< 28B5<> 32A8<
USB2_DAN_F	32C1<> 33B7< 56B3>
USB2_DAP_F	32C1<> 33B7< 56B3>
USB2_DBN_F	32C1<> 33C7< 56B3>
USB2_DBP_F	32C1<> 33C7< 56B3>
USB2_DCN_F	32C1<> 33D7< 56B3>
USB2_DCP_F	32C1<> 33D7< 56B3>
USB2_IDSEL	32B6<
USB2_NC1	32B4<>
USB2_NC2	32B4<>
USB2_PME_L	32A6<>
USB2_RREF	32B4<> 56B3>
USB2_RSDAM	32C4<> 56B3>
USB2_RSDAP	32C4<> 56B3>
USB2_RSDBM	32C4<> 56B3>
USB2_RSDBP	32C4<> 56B3>
USB2_RSDCM	32C4<> 56B3>
USB2_RSDCP	32C4<> 56B3>
USB2_VCCRST	32A6<
USB2_XT1	32C4< 56B3>
USB2_XT2	32C4<> 56B3>
USB2_XT2_B	56B3>
USBT_DAN_F	33B6<> 56B3>
USBT_DAP_F	33B6<> 56B3>
USBT_DBN_F	33C6<> 56A3>
USBT_DBP_F	33C6<> 56A3>
USBT_DCN_F	33D6<> 56A3>
USBT_DCP_F	33D6<> 56A3>
USB_DAN	28A3< 28B3<> 58B5>
USB_DAN_CON	33C3<> 56A3> 59C6>
USB_DAN_F	28B2< 33B7< 58B5>
USB_DAP	28A3< 28B3<> 58B5>
USB_DAP_CON	33C3<> 56A3> 59C6>
USB_DAP_F	28B2< 33B7< 58B5>
USB_DBN	28A3< 28B3<> 58B5>
USB_DBN_CON	33B3<> 56A3> 59C6>
USB_DBN_F	28B2< 33C7< 58B5>
USB_DBP	28A3< 28B3<> 58B5>
USB_DBP_CON	33B3<> 56A3> 59C6>
USB_DBP_F	28B2< 33C7< 58B5>
USB_DCN	28A3< 28B3<> 58B5>
USB_DCN_CON	33D3<> 56A3> 59C6>
USB_DCN_F	28B2< 33D7< 58B5>
USB_DCP	28A3< 28B3<> 58B5>
USB_DCP_CON	33D3<> 56A3> 59C6>
USB_DCP_F	28B2< 33D7< 58B5>
USB_DDN	28B3<>
USB_DDN_F_TERM	28B2<
USB_DDP	28B3<>
USB_DDP_F_TERM	28B2<
USB_DEN	28B3<> 58B5>
USB_DEP	28B3<> 58B5>
USB_DFN	28B3<> 58A5>
USB_DFP	28B3<> 58A5>
USB_GND	52A3>
USB_OC_EF_L	28B3< 28C2<
USB_PORT_PWR	33A4<> 33B3<> 33C3<> 33D3<> 52A3> 59B6>
USB_PWR	25B5<> 25C2< 25D3<> 33A6<> 52A3>
USB_PWREN_AB_L	28B3<> 28C2<
USB_PWREN_CD_L	28B3<> 28C2<
USB_PWREN_EF_L	28B3<> 28C2<
USB_PWR_EN	33A8<>
USB_PWR_FLT*	28B3< 28C1< 32B1< 33A7>
UX6P23	39C4<
UX6_LINB	39C4<
U_USB_PWR_FLT*	32B4<
VCOML	43D5<

VCOMR	43D5<
VCOREIN	45D6<>
VCORE_BG	45C6<>
VCORE_BG_1	45B5< 45C7<>
VCORE_BOOST	45C5<>
VCORE_BOOST2	45C6<>
VCORE_BOOST2_1	45B5< 45C7<>
VCORE_BOOST_1	45B5<>
VCORE_EXTVCC	45D7<
VCORE_FREQSET	45C7<
VCORE_INTVCC	45C5<> 45D5<> 45D7<>
VCORE_SEN+	45C3<>
VCORE_SEN+_1	45A3<>
VCORE_SENA+	45C3<>
VCORE_SF	45C8<
VCORE_SGND	45B7<> 45C7<> 45C7<> 45C8<> 45C8<>
VCORE_STBY	45C7<>
VCORE_TG	45C6<>
VCORE_TG_1	45B5< 45C7>
VCORE_VGATE	28B5<> 28D3<
VCORE_VIN	45D7<>
VC_CNTL1	44C7< 45D8<
VC_SENA	45B3<>
VGA_IIC_CLK	25C4<> 59B6>
VGA_IIC_DAT	25C4<> 59B6>
VGER_INV_HRESET	7A3< 7B3< 7B3< 7C3< 44D1>
VIPCLK	22D4< 52A8>
VIPD0	22D4<> 26B7<
VIPD1	22D4<> 26B7<
VIPD2	22D4<> 26B8<
VIPD3	22D4<> 26D7<
VIPD4	22D4<> 26D7<
VIPD5	22D4<> 26D7<
VIPD6	22D4<> 26B8<
VIPD7	22D4<> 26C5<
VIPHAD0	22D5<> 26B7<
VIPHAD1	22D5<> 26B7<
VIPHCTL	22D5<> 26D5<
VIP_PD	22D4<
VIP_PU	22D4<
VOSNS1	50B8<>
VOSNS2	50B5<>
VR4210P1	39B7<
VREFM	39B4<
VREFP	39B4< 43A3<
VRFILT	39B3<>
VSYNC*	22C5<> 57D5>
WL_PCI_IDSEL	31C2<> 59A6>
XMIT_LED	35A2< 35B4<>
ZT8P1	4A1<>
ZT9P1	4B2<>
ZT10P1	4A2<>
ZT11P1	4B1<>

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6497 | REV. 13

SCALE NONE | SHT 64 OF 69

*** Part Cross-Reference for the entire design ***

BS1	PCB_STANDOFF	29B5
BS2	PCB_STANDOFF	29B6
BS3	PCB_STANDOFF	29D1
BS4	PCB_STANDOFF	29D1
BT1	BATTERY	44D6
C1	CAP	33C4
C2	CAP	33D4
C3	CAP	35B1
C4	CAP	36B6
C5	CAP_P	33A5
C6	CAP	33B4
C7	CAP_P	33A5
C8	CAP	21A4
C9	CAP	21A4
C10	CAP_P	36D7
C11	CAP	21A4
C12	CAP_P	36D7
C13	CAP_P	41C4
C14	CAP	12A7
C15	CAP	21D2
C16	CAP	21B4
C17	CAP	21D5
C18	CAP	51D3
C19	CAP_P	51D4
C20	CAP	21B2
C21	CAP	21D5
C22	CAP	21B4
C23	CAP	21B4
C24	CAP_P	40B4
C25	CAP_P	40C4
C26	CAP_P	41D4
C27	CAP	36D8
C28	CAP	21B1
C29	CAP	21B3
C30	CAP	12A6
C31	CAP	21B2
C32	CAP	21D4
C33	CAP	21B2
C34	CAP	21B3
C35	CAP	43B5
C36	CAP	42D7
C37	CAP	35D7
C38	CAP	21D2
C39	CAP	21D5
C40	CAP	21B3
C41	CAP	35D8
C42	CAP	36B8
C43	CAP	41D6
C44	CAP	35D4
C45	CAP	42B8
C46	CAP	14D8
C47	CAP	14D8
C48	CAP	15D8
C49	CAP	15D8
C50	CAP	15D7
C51	CAP	15C3
C52	CAP	35D4
C53	CAP	35D5
C54	CAP	18B8
C55	CAP	15C1
C56	CAP	35D4
C57	CAP	35D6
C58	CAP	15B1
C59	CAP_P	48B2
C60	CAP	41C6
C61	CAP	18B6
C62	CAP	18D6
C63	CAP	40B2
C64	CAP	40C2
C65	CAP	35D7
C66	CAP	35D7
C67	CAP	35D5
C68	CAP	35D6
C69	CAP	18B5
C70	CAP	18B6
C71	CAP_P	48B1
C72	CAP	18H7
C73	CAP	18H7
C74	CAP	35B7
C75	CAP	18H5
C76	CAP	35B7
C77	CAP	32D3
C78	CAP	18H6
C79	CAP	18H4
C80	CAP	18H2
C81	CAP	18H7
C82	CAP	18H4
C83	CAP	18H3
C84	CAP	18H8
C85	CAP_P	39C6
C86	CAP	18H8
C87	CAP	17B2
C88	CAP_P	48B1
C89	CAP	18H2
C90	CAP	18H7
C91	CAP	17B3
C92	CAP	34B6
C93	CAP	17C3
C94	CAP	17C3
C95	CAP	18H5
C96	CAP	18H2
C97	CAP	17B3
C98	CAP	18H6
C99	CAP	17D1
C100	CAP	17D3
C101	CAP	17D2
C102	CAP	17C2
C103	CAP	17D2
C104	CAP	17D4
C105	CAP	17B2
C106	CAP_P	48B2
C107	CAP	24B2
C108	CAP	42B7
C109	CAP	17D3
C110	CAP	17D2
C111	CAP	17B3
C112	CAP	17B2
C113	CAP	27D5
C114	CAP	32D3
C115	CAP	18H3
C116	CAP	17B3
C117	CAP	17D3
C118	CAP	17C3
C119	CAP	23B5
C120	CAP	17C3
C121	CAP	39C4
C123	CAP	30C3
C124	CAP	18H1
C125	CAP	23B6
C126	CAP_P	39C7
C127	CAP_P	39B2
C128	CAP	22D3
C129	CAP	17B3
C130	CAP	23B6
C131	CAP	23B4
C132	CAP_P	48B2
C133	CAP	18H6
C134	CAP	17D3
C135	CAP	17C2
C136	CAP	17B3
C137	CAP	17B4
C138	CAP	46B4
C139	CAP	17D1
C140	CAP	17C2
C141	CAP	20B3
C142	CAP	20D5
C143	CAP	20D5
C144	CAP	20D5
C145	CAP	18H2
C146	CAP	17D1
C147	CAP	17C3
C148	CAP	17C4
C149	CAP	17C3
C150	CAP	17C3
C151	CAP	17C2
C152	CAP	23B5
C153	CAP	22C7
C157	CAP	20A4
C158	CAP	20D5
C159	CAP	18H5
C160	CAP	23C6
C161	CAP	17C4
C162	CAP	22C6
C163	CAP	22C6
C164	CAP	22C6
C165	CAP	20B3
C166	CAP	20B3
C167	CAP	18H5
C168	CAP	17C3
C169	CAP	17C2
C170	CAP	22C7
C171	CAP	46A6
C172	CAP	20A4
C173	CAP	20B2
C174	CAP	20B4
C175	CAP	18H3
C176	CAP	17D2
C177	CAP	17B4
C178	CAP	17D4
C179	CAP	17B3
C180	CAP	17D3
C181	CAP	17B2
C182	CAP	17B1
C183	CAP	17D2
C184	CAP	17B2
C185	CAP	17D3
C186	CAP	17B4
C187	CAP	17B3
C188	CAP	17B1
C189	CAP	23C7
C190	CAP	22C7
C191	CAP	20A5
C192	CAP	17D4
C193	CAP	17B5
C194	CAP	20B4
C195	CAP	20B1
C196	CAP	20B2
C197	CAP	20B2
C198	CAP	20B4
C199	CAP	18H3
C200	CAP	17D4
C201	CAP	17D4
C202	CAP	17D3
C203	CAP	17D2
C204	CAP	40C5
C205	CAP	20D2
C206	CAP	22C2
C207	CAP	22C7
C208	CAP	41A5
C209	CAP	22B6
C212	CAP	22D6
C213	CAP	22D6
C214	CAP	17B3
C215	CAP	17A3
C216	CAP	20D2
C217	CAP	17C1
C218	CAP_P	49B3
C219	CAP	17C2
C220	CAP_P	48C8
C222	CAP	16A8
C223	CAP	17C2
C224	CAP	22C2
C225	CAP	30C2
C226	CAP	22D6
C227	CAP	22C3
C228	CAP	22C3
C229	CAP	28C6
C230	CAP	13D7
C231	CAP	11A6
C232	CAP	11A6
C233	CAP	28D6
C234	CAP	28D7
C235	CAP_P	49B2
C236	CAP	51B3
C238	CAP_P	51C5
C239	CAP	44A4
C240	CAP	11C8
C241	CAP	50C5
C242	CAP	14C2
C243	CAP	14C2
C244	CAP	14C3
C245	CAP_P	44D5
C246	CAP_P	51B3
C248	CAP	39B4
C249	CAP	31D1
C250	CAP	31D2
C252	CAP	51B2
C254	CAP	51B1
C255	CAP	14C2
C256	CAP	14C1
C257	CAP	51B2
C258	CAP	51B2
C259	CAP	31D1
C260	CAP	31D2
C261	CAP	14C1
C262	CAP	47B4
C263	CAP	14C2
C264	CAP	11C4
C265	CAP	47B3
C266	CAP	47B8
C267	CAP	44D6
C269	CAP_P	51D6
C270	CAP	47A5
C271	CAP	11C8
C272	CAP	27D4
C273	CAP	47C5
C275	CAP	14C2
C276	CAP	14C2
C277	CAP	11C8
C278	CAP	11C6
C279	CAP	11C5
C280	CAP	11C6
C281	CAP	11C6
C282	CAP	47B6
C283	CAP	47C7
C284	CAP	47B4
C285	CAP	47B7
C286	CAP	47B7
C287	CAP	50A2
C288	CAP	11D8
C289	CAP	11D8
C290	CAP	11D8
C291	CAP	11D8
C292	CAP	11D4
C293	CAP	50A1
C294	CAP	50A1
C295	CAP_P	50C5
C296	CAP_P	47B3
C297	CAP	47C4
C298	CAP	47C5
C299	CAP	47C4
C300	CAP_P	47C3
C301	CAP_P	47C4
C302	CAP_P	50A2
C303	CAP	50C2
C304	CAP	14C2
C305	CAP	47C4
C306	CAP_P	50A2
C307	CAP_P	50A2
C308	CAP_P	50A3
C309	CAP_P	50A3
C310	CAP_P	50A2
C311	CAP	14C1
C312	CAP	29D3
C313	CAP	14C3
C314	CAP	29D3
C315	CAP	50A8
C316	CAP	50A8
C317	CAP	50B8
C318	CAP	50B8
C319	CAP	14A7
C320	CAP	14C2
C321	CAP	50B7
C322	CAP	50A7
C323	CAP_P	49B2
C324	CAP_P	49B2
C325	CAP	27D4
C326	CAP_P	50B2
C327	CAP_P	50B2
C328	CAP_P	50B2
C329	CAP	49B3
C330	CAP_P	49B2
C331	CAP_P	49B2
C332	CAP_P	49B2
C333	CAP	50B6
C334	CAP_P	45C1
C335	CAP_P	45C2
C336	CAP_P	45C2
C337	CAP_P	45C2
C338	CAP_P	50D6
C339	CAP_P	50D6
C340	CAP_P	45C2
C341	CAP	50B7
C342	CAP_P	49C3
C343	CAP_P	45D3
C344	CAP	50B4
C345	CAP	4B1
C346	CAP_P	45B1
C347	CAP_P	45B2
C348	CAP_P	45B2
C349	CAP_P	50D6
C350	CAP	8D4
C351	CAP_P	49C3
C352	CAP	4B1
C353	CAP	8D4
C354	CAP_P	50D3
C355	CAP_P	50D3
C356	CAP_P	50D3
C357	CAP_P	45D3
C358	CAP	49C4
C359	CAP	49B7
C360	CAP	27D4
C361	CAP_P	45B2
C362	CAP_P	45B2
C363	CAP	46C4
C364	CAP	8C1
C365	CAP	46C6
C366	CAP	27D4
C367	CAP	45B6
C368	CAP	22B6
C369	CAP	4A1
C370	CAP	4A1
C371	CAP	45C5
C372	CAP	45B7
C373	CAP	45C8
C374	CAP	45B5
C375	CAP	36C1
C376	CAP	36D3
C377	CAP	33A4
C378	CAP	36C1
C379	CAP	36C2
C380	CAP	33C4
C381	CAP	36D3
C382	CAP	33A4
C383	CAP	33C4
C384	CAP	36C2
C385	CAP	33B4
C386	CAP	33C3
C387	CAP	33C4
C388	CAP	42A5
C389	CAP	33B4
C390	CAP	36A6
C391	CAP	33B4
C392	CAP	36A6
C393	CAP	36A6
C394	CAP	36A6
C395	CAP	36A6
C396	CAP	33A5
C397	CAP	33D4
C398	CAP	33B3
C399	CAP	36A7
C400	CAP	35C1
C401	CAP	35D1
C403	CAP	33D4
C404	CAP	33D4
C405	CAP	33D3
C406	CAP	36B6
C407	CAP	36A6
C408	CAP	41B3
C409	CAP	25B3
C410	CAP	36D4
C411	CAP	36A7
C412	CAP	41C3
C413	CAP	33D3
C414	CAP	25B4
C415	CAP	25A4
C416	CAP	25A4
C417	CAP	33B3
C418	CAP	36D4
C420	CAP	41D3
C421	CAP	25D4
C422	CAP	25C4
C423	CAP	25C3
C424	CAP	36B6
C427	CAP	41B3
C428	CAP	36B7
C431	CAP	40B6
C432	CAP	25B3
C433	CAP	33C3
C434	CAP	35D3
C436	CAP	41A4
C437	CAP	40C6
C438	CAP	35D3
C439	CAP	36B4
C440	CAP	36B4
C441	CAP	36C4
C442	CAP	36C5
C443	CAP	36B2
C444	CAP	36B2
C445	CAP	36C3
C446	CAP	36C3
C447	CAP	40B6
C449	CAP	27D4
C450	CAP	36B3
C451	CAP	36B2
C452	CAP	36B4
C453	CAP	41B4
C454	CAP	40C6
C455	CAP	36B4
C456	CAP	36B3
C457	CAP	36B4
C458	CAP	36B3
C460	CAP	21D2
C461	CAP	21B7
C462	CAP	21B8
C463	CAP	36B4
C464	CAP	36B4
C466	CAP	21B7
C467	CAP	21D8
C468	CAP	36B1
C469	CAP	21B7
C470	CAP	21B8
C471	CAP	36B4
C472	CAP	36B1
C473	CAP	51D2
C475	CAP	21B6
C476	CAP	21B6
C477	CAP	36C7
C478	CAP	43A5
C479	CAP_P	40C4
C480	CAP_P	40B4
C481	CAP	36B3
C482	CAP	36B3
C483	CAP	36B3
C484	CAP	36B5
C485	CAP	36B1
C486	CAP	21B6
C487	CAP	21D7
C488	CAP	21B7
C489	CAP	21B5
C490	CAP	36B6
C492	CAP	21D1
C493	CAP	21D7
C494	CAP	21D7
C495	CAP	36B2
C496	CAP	36B2
C499	CAP	41D6
C500	CAP	36C7
C503	CAP	41C6
C504	CAP	41B7
C505	CAP	40D3
C506	CAP	40C3
C507	CAP	40B3
C508	CAP	41C6
C509	CAP	18B8
C510	CAP	18B8
C511	CAP	32D5
C512	CAP_P	41B7
C513	CAP	40B3
C514	CAP	40C3
C515	CAP	32C8
C516	CAP	32D8
C517	CAP	32C8
C518	CAP	41B7
C519	CAP	32D8
C520	CAP	20D2
C521	CAP	20D2
C522	CAP	32D8
C523	CAP	32D8
C524	CAP_P	41C7
C525	CAP_P	41D7
C526	CAP	32D5
C527	CAP	32D8
C528	CAP_P	48B3
C529	CAP	32D5
C530	CAP	32C7
C531	CAP	32C7
C532	CAP	20D7
C533	CAP	20D7
C534	CAP	20B6
C535	CAP	20B6
C536	CAP	32C8
C537	CAP	32D7
C538	CAP_P	39D6
C539	CAP_P	39B7
C540	CAP	20D8
C541	CAP	32D8
C542	CAP	43B4
C543	CAP	48B3
C544	CAP	20D7
C545	CAP	20B7
C546	CAP	32D8
C547	CAP	32D7
C548	CAP	32D8
C549	CAP	39D7
C550	CAP	43A3
C551	CAP	43B3
C552	CAP	48B6
C553	CAP	20B6
C554	CAP	20B7
C555	CAP	32D7
C556	CAP	43B3
C557	CAP	27D4
C558	CAP_P	48B2
C559	CAP	32D8
C562	CAP	15D3
C563	CAP	48B6
C564	CAP	48C2
C565	CAP	20B5
C566	CAP	20B7
C567	CAP	20B7
C568	CAP	20B8
C569	CAP	20B8
C570	CAP	32C8
C572	CAP	48B7
C573	CAP	32C8
C574	CAP	32C8
C576	CAP	48C3
C578	CAP	39C5
C579	CAP	39C5
C580	CAP_P	39B2
C581	CAP	39B2
C582	CAP	42B7
C583	CAP	27D3
C584	CAP	39D3
C585	CAP	48B5
C586	CAP	48A4
C587	CAP	39B2
C588	CAP	39B5
C589	CAP	48C5
C591	CAP_P	39D2
C592	CAP	39B5
C593	CAP	15D2
C594	CAP	39B5
C595	CAP	39B5
C596	CAP	48C6
C597	CAP	39C4
C598	CAP	8B2
C599	CAP	39D4
C600	CAP_P	39D4
C601	CAP	29A5
C602	CAP	15D2
C603	CAP	16A8
C604	CAP	29A7
C605	CAP	22C2
C606	CAP	22C2
C607	CAP	22C1
C608	CAP	29A6
C609	CAP	29A4
C610	CAP	24A3
C611	CAP	13D7
C612	CAP	13D6
C613	CAP	13D6
C614	CAP	29A6
C615	CAP	29A4
C616	CAP	22A2
C617	CAP	22A3
C618	CAP	23A6
C619	CAP	29C7
C620	CAP	29C7
C621	CAP	29D7
C622	CAP	29D7
C623	CAP	28D7
C624	CAP	15D2
C625	CAP	29A7
C626	CAP	23A6
C627	CAP	29A6
C628	CAP	11A6
C629	CAP_P	29A5
C630	CAP	29A6
C631	CAP	48C7
C632	CAP	48C7
C633	CAP	48C7
C634	CAP	48C7
C635	CAP_P	23A6
C636	CAP_P	23A8
C637	CAP	11C4
C638	CAP	11A6
C639	CAP	29A4
C640	CAP	29A3
C641	CAP	11C8
C642	CAP	43B7
C643	CAP	11C2
C644	CAP	11B2
C645	CAP	11B1
C646	CAP	11B1
C647	CAP	11A5
C648	CAP	11A5
C649	CAP	11A4
C650	CAP	11A6
C651	CAP	11A3
C652	CAP	24B2
C653	CAP	51B4
C654	CAP	51B4
C655	CAP	11C4
C656	CAP	11C2
C657	CAP	11B3
C658	CAP	11B2
C659	CAP	11B3
C660	CAP	11B1
C661	CAP	11A6
C662	CAP	11A6
C663	CAP	11A4
C664	CAP	11A3
C665	CAP	11A4
C666	CAP	11A4
C667	CAP	11A4
C668	CAP	11B5
C669	CAP	13C5
C670	CAP	13C5
C671	CAP	13C5
C672	CAP	15D1
C673	CAP	11B2
C674	CAP	11A5
C675	CAP	43A7
C676	CAP	11B3
C677	CAP	11B1
C678	CAP	11B3
C679	CAP	11B1
C680	CAP	11C3
C681	CAP	11B3
C682	CAP	11B3
C683	CAP	11A4
C684	CAP	11A5
C685	CAP	11A5
C686	CAP	11A5
C687	CAP	11B6
C688	CAP	11C7

C689	CAP	11C1	
C690	CAP	11B2	
C691	CAP	11C2	
C692	CAP	28D6	
C693	CAP	11A6	
C694	CAP	11A4	
C695	CAP	11A4	
C696	CAP	11A4	
C697	CAP	11A6	
C698	CAP	11C5	
C699	CAP	11B7	
C700	CAP	11C7	
C701	CAP	44B2	
C702	CAP	11D4	
C703	CAP	28D6	
C704	CAP	28D5	
C705	CAP	44A6	
C706	CAP	44A6	
C707	CAP	11B3	
C708	CAP	11B3	
C709	CAP	11A5	
C710	CAP	11A5	
C711	CAP	11A5	
C712	CAP	11B1	
C713	CAP	28D5	
C714	CAP	11B5	
C715	CAP	44B2	
C716	CAP	11B2	
C717	CAP	11C3	
C718	CAP	11B1	
C719	CAP	11D2	
C720	CAP	11C3	
C721	CAP	11D3	
C722	CAP	11B7	
C723	CAP	11B6	
C724	CAP	11B5	
C725	CAP	11C7	
C726	CAP	15D3	
C727	CAP	11D4	
C728	CAP	11C3	
C729	CAP	11B3	
C730	CAP	11D3	
C731	CAP	11D1	
C732	CAP	11D1	
C733	CAP	11A6	
C734	CAP	11D2	
C735	CAP	11B7	
C736	CAP	11B5	
C741	CAP	15D3	
C742	CAP	51C6	
C743	CAP	11B3	
C744	CAP	11B1	
C745	CAP	11C3	
C746	CAP	11D3	
C747	CAP	11D1	
C748	CAP	11D2	
C749	CAP	11D3	
C750	CAP	11B6	
C751	CAP	11B7	
C752	CAP	11B6	
C753	CAP	11B6	
C754	CAP	11B5	
C755	CAP	11B6	
C759	CAP	44D5	
C760	CAP	16D6	
C761	CAP	11B3	
C762	CAP	11C1	
C763	CAP	11D2	
C764	CAP	11D3	
C765	CAP	11D3	
C766	CAP	11D1	
C767	CAP	11C6	
C768	CAP	11B6	
C773	CAP	51C6	
C774	CAP	11C1	
C775	CAP	11C3	
C776	CAP	11B2	
C777	CAP	11C1	
C778	CAP	22B6	
C779	CAP	11D1	
C780	CAP	11D2	
C781	CAP	11B5	
C782	CAP	11B7	
C783	CAP	44D5	
C784	CAP	28A6	
C785	CAP	28C3	
C786	CAP	27D3	
C787	CAP	11D3	
C788	CAP	11D3	
C789	CAP	11D3	
C790	CAP	11D1	
C791	CAP	11B6	
C792	CAP	11B6	
C793	CAP	11C6	
C794	CAP	11C5	
C795	CAP	28C3	
C796	CAP	11C3	
C797	CAP	11D3	
C798	CAP	11D1	
C799	CAP	11D1	
C800	CAP	11D2	
C801	CAP	11B7	
C802	CAP	11B5	
C803	CAP	11B6	
C805	CAP	11B2	
C806	CAP	11C2	
C807	CAP	11B2	
C808	CAP	11D2	
C809	CAP	11C3	
C810	CAP	11D2	

C811	CAP	11D2	
C812	CAP	11C2	
C813	CAP	11B5	
C814	CAP	11B6	
C815	CAP	11C6	
C816	CAP	11B6	
C817	CAP	11C6	
C818	CAP	11B5	
C819	CAP	15D3	
C820	CAP	28C3	
C821	CAP	11C1	
C822	CAP	11C1	
C823	CAP	11D7	
C824	CAP	11D6	
C825	CAP	11B7	
C826	CAP	11B7	
C827	CAP	11C5	
C828	CAP	11C1	
C829	CAP	11C2	
C830	CAP	11C3	
C831	CAP	11D3	
C832	CAP	11D7	
C833	CAP	11D3	
C834	CAP	11D6	
C835	CAP	11B3	
C836	CAP	11C6	
C837	CAP	11C7	
C838	CAP	11B7	
C839	CAP	11C6	
C840	CAP	28A6	
C841	CAP	11D4	
C842	CAP	11D6	
C843	CAP	11C7	
C844	CAP	11D6	
C845	CAP	11D6	
C846	CAP	11D7	
C848	CAP	30D5	
C849	CAP	11C6	
C850	CAP	11B3	
C851	CAP	11B3	
C852	CAP	11B2	
C854	CAP	9D3	
C855	CAP	11C5	
C856	CAP	11B7	
C857	CAP	11C6	
C858	CAP	13D4	
C859	CAP	13D3	
C860	CAP	13D4	
C861	CAP	44A1	
C862	CAP	44B7	
C863	CAP	11C2	
C864	CAP	15D2	
C865	CAP	11B1	
C866	CAP	11C3	
C867	CAP	11C3	
C868	CAP	11C2	
C869	CAP	11D5	
C870	CAP	11D6	
C871	CAP	11D6	
C872	CAP	11D5	
C873	CAP	11D5	
C874	CAP	11D5	
C875	CAP	11B3	
C876	CAP	11C5	
C877	CAP	11C7	
C878	CAP	11C7	
C879	CAP	11B2	
C880	CAP	11C5	
C881	CAP	11B3	
C882	CAP	11B1	
C883	CAP	11B2	
C884	CAP	11D6	
C885	CAP	11D7	
C886	CAP	11D5	
C887	CAP	11D7	
C888	CAP	11D6	
C889	CAP	11D6	
C890	CAP	11D7	
C891	CAP	11D6	
C892	CAP	11C4	
C893	CAP	11C1	
C894	CAP	11C2	
C895	CAP	11D5	
C896	CAP	11D5	
C897	CAP	11D6	
C898	CAP	11D5	
C899	CAP	11D5	
C900	CAP	11D7	
C901	CAP	11D7	
C902	CAP	11C7	
C903	CAP	11B2	
C904	CAP	11C6	
C908	CAP	13C2	
C909	CAP	13C2	
C910	CAP	13C1	
C911	CAP	37C2	
C914	CAP	15D2	
C915	CAP	51D7	
C917	CAP	37C5	
C918	CAP	51D6	
C919	CAP	38C7	
C920	CAP	38C1	
C921	CAP	38C5	
C922	CAP	15D2	
C923	CAP	38B5	
C924	CAP	38B7	
C925	CAP	15D3	
C926	CAP	50C1	
C927	CAP	50B1	
C928	CAP_P	47B4	

C929	CAP	14A7	
C930	CAP	50B8	
C931	CAP	50B5	
C932	CAP	50A5	
C933	CAP	50A6	
C934	CAP	50B1	
C935	CAP_P	47B3	
C936	CAP	15D3	
C937	CAP	50C7	
C938	CAP	50A4	
C939	CAP	50A6	
C940	CAP	50A5	
C941	CAP	50C5	
C943	CAP	15A3	
C944	CAP	45D3	
C945	CAP	15A2	
C947	CAP_P	45C1	
C948	CAP	49B4	
C949	CAP	45C5	
C950	CAP	45D4	
C951	CAP	45D4	
C952	CAP	45D4	
C953	CAP	45D4	
C954	CAP	4C2	
C955	CAP	50D3	
C956	CAP	50D4	
C957	CAP_P	45B1	
C958	CAP	8D4	
C959	CAP	49C4	
C960	CAP	45B2	
C961	CAP	8C2	
C962	CAP	49C3	
C963	CAP	45D4	
C964	CAP	45D4	
C965	CAP	45D4	
C966	CAP	45D4	
C967	CAP	8C1	
C968	CAP	49C4	
C969	CAP	8D4	
C970	CAP	50D4	
C971	CAP	50D4	
C972	CAP	8D2	
C973	CAP	8D1	
C974	CAP	8D1	
C975	CAP	49C4	
C976	CAP	8C1	
C977	CAP	8D1	
C978	CAP	50D4	
C979	CAP	50D4	
C980	CAP	8D2	
C981	CAP	8D2	
C982	CAP	8D2	
C983	CAP	8D3	
C984	CAP	27D3	
C985	CAP	50D3	
C986	CAP	50D4	
C987	CAP	8D2	
C988	CAP	8D3	
C989	CAP	49C3	
C990	CAP	8D1	
C991	CAP	8D1	
C992	CAP	8D3	
C993	CAP	8D1	
C994	CAP	8C2	
C995	CAP	8D2	
C996	CAP	8A7	
C997	CAP	8A6	
C998	CAP	8D2	
C999	CAP	8D1	
C1000	CAP	49B6	
C1001	CAP	8A6	
C1002	CAP	8A7	
C1003	CAP	8D1	
C1004	CAP	49B6	
C1005	CAP	49C4	
C1006	CAP	45C2	
C1007	CAP	8C2	
C1008	CAP	8B6	
C1009	CAP	8A7	
C1010	CAP	8B6	
C1011	CAP	8B6	
C1012	CAP	8A7	
C1013	CAP	8D2	
C1014	CAP	8D2	
C1015	CAP	49B7	
C1016	CAP	8C1	
C1017	CAP	8A6	
C1018	CAP	8A6	
C1019	CAP	49C6	
C1020	CAP	8C1	
C1021	CAP	8C1	
C1022	CAP	8B7	
C1023	CAP	8A6	
C1024	CAP	8A6	
C1025	CAP	8B6	
C1026	CAP	8D2	
C1027	CAP	8B7	
C1028	CAP	8A6	
C1029	CAP	45B4	
C1030	CAP	45B2	
C1031	CAP	8A6	
C1032	CAP	8C2	
C1033	CAP	8C1	
C1034	CAP	45B2	
C1035	CAP	4D3	
C1036	CAP	4D3	
C1037	CAP	8C1	
C1038	CAP	45B4	
C1039	CAP	45C5	
C1040	CAP	8C2	

C1041	CAP	8D3	
C1042	CAP	8C1	
C1043	CAP	8D2	
C1044	CAP	45D7	
C1045	CAP	45B7	
C1046	CAP	45C1	
C1047	CAP	45D5	
C1048	CAP	45C2	
C1049	CAP	45B7	
C1050	CAP	45C7	
C1051	CAP	45B6	
C1052	CAP	45C8	
C1053	CAP	46A7	
C1054	CAP	8B2	
C1055	CAP	8B2	
C1056	CAP	8B1	
C1057	CAP	8B1	
C1058	CAP	8B1	
C1059	CAP	42C7	
C1060	CAP	42C6	
C1061	CAP	42A7	
C1062	CAP	42A7	
C1063	CAP	42C6	
C1064	CAP	42C6	
C1065	CAP	42A7	
C1066	CAP	42C6	
C1067	CAP	42A7	
C1068	CAP	42D6	
C1069	CAP	42D4	
C1070	CAP	42C4	
C1071	CAP	42C4	
C1072	CAP	42C3	
C1073	CAP	42C3	
C1074	CAP	42C3	
C1075	CAP	42C2	
C1076	CAP	43D5	
C1077	CAP	43D5	
C1078	CAP	43D5	
C1079	CAP	43D5	
C1080	CAP_P	42B3	
C1081	CAP_P	42A3	
C1082	CAP	42B2	
C1083	CAP	42B2	
C1084	CAP	42B2	
C1085	CAP	42B2	
C1086	CAP	42A2	
C1087	CAP	43D2	
C1088	CAP	43D2	
C1089	CAP	42B2	
C1090	CAP	42B2	
C1091	CAP	42B2	
C1092	CAP	42B2	
C1093	CAP	42A2	
C1094	CAP	43C2	
C1095	CAP	43D2	
C1096	CAP	8A7	
C1097	CAP	8A7	
C1098	CAP	8B5	
C1099	CAP	42C8	
C1100	CAP	42C2	
C1101	CAP	9D3	
C1102	CAP_P	42B3	
C1103	CAP	22B5	
C1401	CAP	14D7	
C1402	CAP	14D2	
C1403	CAP	14C1	
C1404	CAP	14C1	
C1405	CAP	14C1	
C1406	CAP	14C3	
C1407	CAP	14C2	
C1408	CAP	14C2	
C1409	CAP	14C2	
C1410	CAP	14C2	
C1411	CAP	14C1	
C1412	CAP	14C1	
C1413	CAP	14C1	
C1414	CAP	14B1	
C1415	CAP	14C3	
C1416	CAP	14C2	
C1417	CAP	14C2	
C1418	CAP	14C2	
C1419	CAP	14C2	
C1420	CAP	14C1	
C1421	CAP	14C1	
C1501	CAP	15D7	
C1502	CAP	15D1	
C1503	CAP	15D1	
C1504	CAP	15D3	
C1505	CAP	15D3	
C1506	CAP	15D3	
C1507	CAP	15D2	
C1508	CAP	15D2	
C1509	CAP	15D2	
C1510	CAP	15D1	
C1511	CAP	15D1	
C1512	CAP	15D1	
C1513	CAP	15D1	
C1514	CAP	15C3	
C1515	CAP	15C3	
C1601	CAP	14D7	
C1602	CAP	14D3	
C1702	CAP	15D7	
C1801	CAP	16D5	
C1802	CAP	16A7	
C1901	CAP	8A7	
C1902	CAP	8A6	
C1903	CAP	8A6	
C1904	CAP	8A6	
C1910	CAP	8A6	
C1911	CAP	8C2	

C1912	CAP	8C1	
C1913	CAP	8C1	
C1914	CAP	8C1	
C2201	CAP	20C8	
C2202	CAP	20C4	
C2301	CAP	21C8	
C2302	CAP	21C4	
C2501	CAP_P	23A8	
C3001	CAP	28C5	
C3002	CAP	28D5	
C3003	CAP	28D5	
C3004	CAP	28D4	
C3005	CAP	28D4	
C3201	CAP	30D4	
C3501	CAP	35D6	
C3502	CAP	33A8	
C3901	CAP	37D1	
C4081	CAP	46C7	
C4201	CAP	42B6	
C4301	CAP	41A6	
C4502	CAP_P	43B5	
C4504	CAP	45B3	
C4509	CAP	45C4	
C4701	CAP	45B6	
C4702	CAP	47B4	
C4801	CAP	48B4	
C4901	CAP	49B4	
C5001	CAP	50C3	
C5002	CAP	50A3	
D1	DIODE_DUAL_6P	36A7	
D2	DIODE_DUAL_6P	36A7	
D3	DIODE_DUAL_6P	36A7	
D4	DIODE_DUAL_6P	36B7	
D5	ZENER_MMBZ15VDLT1	40B6	
D6	DIODE_DUAL_6P	25D4	
D7	DIODE_DUAL_6P	25D4	
D8	DIODE	36D6	
D9	DIODE	35B8	
D10	DIODE_SCHOT	23B8	
D11	DIODE_SCHOT	44D7	
D12	DIODE_SCHOT	44D7	
D13	DIODE_SCHOT	47C7	
D14	DIODE_SCHOT	47B5	
D15	DIODE_SCHOT	49B3	
D16	DIODE_SCHOT	50C5	
D17	DIODE_SCHOT	50B5	
D18	DIODE_SCHOT	49C6	
D19	DIODE_SCHOT	46D6	
D20	DIODE_SCHOT	45D5	
D21	DIODE_SCHOT	45B5	
D23	DIODE_SCHOT_3P	42A6	
D24	ZENER_MMBZ15VDLT1	41B2	
D25	ZENER	36B6	
D26	ZENER_MMBZ15VDLT1	41B2	
D27	DIODE_DUAL_6P	25B4	
D28	DIODE_DUAL_6P	25B4	
D29	ZENER_MMBZ15VDLT1	40B5	
D30	DIODE_SCHOT	48C5	
D31	DIODE_SCHOT	48B3	
D32	DIODE_SCHOT	48B5	
D33	DIODE_SCHOT	46B6	
D34	DIODE_SCHOT	48B2	
D35	DIODE_SCHOT	44D6	
D36	DIODE_SCHOT	44D6	
D37	DIODE_SCHOT	50B2	
D38	DIODE_SCHOT	50C6	
D39	DIODE_SCHOT	50B4	
D40	DIODE_SCHOT	50A4	
D41	DIODE_SCHOT	45C4	
D42	DIODE_SCHOT	49B5	
D43	DIODE_SCHOT	45B4	
D44	DIODE_SCHOT	45D2	
D45	DIODE_SCHOT	45D6	
D46	DIODE_SCHOT	49B1	
D47	DIODE	36D6	
D48	DIODE_DUAL_SWI	42B6	
D4901	DIODE_SCHOT	47B2	
DS1	LED	35A2	
DS2	LED	35A1	
DS3	LED	35A1	
DS4	LED	30A3	
DS5	LED	51C8	
DS6	LED	51A6	
DS7	LED	38B2	
DS8	LED	38B6	
DS9	LED	50D5	
DS10	LED	51A4	
DZ1	ZENER	51B1	
F2	FUSE	36D5	
F3	FUSE	36D5	
FL2	FILTER_LC	25C6	
FL3	FILTER_LC	25C6	
FL4	FILTER_LC	25B6	
J1	CON_RJ45	35C1	
J2	CON_FWVERT_SKT	36C1	
J3	CON_F8RT_S_TH1	42B5	
J4	CON_F4RT_USB_UPRIGHT	33C3	
J5	CON_FWVERT_SKT	36D1	
J6	CON_F4RT_USB_UPRIGHT	33B3	
J7	CON_F4RT_USB_UPRIGHT	33D3	
J8	CON_F4RT_S4MT_TH1	41C1	
J9	CON_F14RT_D4MT_TH1	25C5	
J10	CON_F4RT_S4MT_TH1	40C7	
J11	CON_F184ST_DDRDIMM	15D5	
J12	CON_F21ST_D2MT_SM	24C4	
J13	CON_M40SM_635	29D6	
J14	CON_M18ST_D_TH	29B5	
J15	CON_M40ST_NC20	38D6	
J16	CON_M40ST_NC20	38D2	
J17	CON_M16ST_MICROFIT	50D7	

J18	CON_M4ST_LCK	34B4	
J19	CON_37SM_MTOR	8C4	
J20	CON_38SM_MTOR	8D7	
J21	CON_M3ST_LCK	45C8	
J22	CON_F20SM_KX	8A4	
J23	CON_F1ST_S2MT_SM	28B7	
J24	CON_M12ST_SM	29B3	
J25	CON_F100RT_LP_SM	31D3	
J26	CON_F200RT_DDRDIMM_SM2	14D5	
J27	CON_F1ST_S2MT_SM	8B1	
J28	CON_F10ST_D_SMA	29D2	
J30	CON_38SM_MTOR	8D4	
J31	CON_38SM_MTOR	8C7	
J32	CON_F12RT_S2MT_SM	8A8	
J4501	CON_F4ST_S2MT_SM	43B6	
J4502	CON_F4ST_S2MT_SM	43B6	
JAZ1	TP	51A5	
L1	IND	36D4	
L2	IND	33A5	
L3	IND	36D4	
L4	IND	27D5	
L5	FILTER_4P	36C2	
L6	FILTER_4P	36C2	
L7	FILTER_4P	36D2	
L8	FILTER_4P	36D2	
L9	IND	25C2	
L12	IND	48B3	
L13	IND	22D7	
L16	IND	28C3	
L19	IND	47B4	
L20	IND	45C3	
L21	IND_3P	49B3	
L22	IND_3P	50A3	
L23	IND	50C3	
L24	IND	45B3	
L26	IND	42A6	
L27	IND	41C3	
L32	IND	36B6	
L33	IND	22B7	
L34	IND	41D3	
L35	IND	41B3	
L36	IND	40B6	
L39	IND	41A3	
L40	IND	42A5	
L41	IND	42B7	
L42	IND	41B3	
L43	IND	41A4	
L44	IND	41C3	
L45	IND	41D3	
L46	IND	40C6	
L47	IND	41B3	
L48	IND	40C6	
L49	IND	40B5	
L50	IND	40C5	
L51	IND	40D6	
L52	IND	40C5	
L53	IND	40D5	
L56	IND	44A1	
L57	IND	44A1	
L58	IND	32D6	
L59	IND	43A5	
L60	IND	43B5	
L63	IND	39D4	
L64	IND	24A5	
L65	IND	29A7	
L66	IND	29A3	
L67	FILTER_4P	24B5	
L68	IND	22D2	
L69	IND	29A3	
L70	IND	29A7	
L71	FILTER_4P	24B5	
L72	IND	29A7	
L73	IND	29A3	
L74	FILTER_4P	24C5	
L75	IND	29A7	
L76	FILTER_4P	24D5	
L77	IND	29B7	
L78	IND	29A3	
L79	IND	43B7	
L80	IND	29B3	
L81	IND	43A7	
L82	IND	24D5	
L83	IND	43A7	
L84	IND	50D6	
L85	IND	50D6	
L86	IND	50D6	
L87	IND	27D5	
L88	IND	27D2	
L89	IND	42C7	
L90	IND	42C6	
L91	IND	42C6	
L92	IND	42C7	
L93	IND	42C3	
L94	IND	42C2	
L95	IND	42C2	
L96	IND	42C3	
L97	IND	43D7	
L98	IND	43D7	
L99	IND	42B3	
L100	FILTER_4P	33D5	
L101	FILTER_4P	33C5	
L102	FILTER_4P	33B5	
L103	IND	29B3	
L2401	IND	22C7	
L2501	IND	23A6	
LP1	LPAK4P	42A8	
Q1	TRA_2N7002	51C3	
Q2	TRA_2N7002	42D7	
Q3	TRA_2N7002	42C7	
Q4	TRA_2N7002	42B8	

Q5	TRA_2N7002	41A5	
Q6	TRA_2N7002	42B6	
Q7	TRA_SUD70N03	48B4	
Q8	TRA_SUD50N03	48B4	
Q9	TRA_SUD50N03	48C4	
Q10	TRA_2N7002	22B7	
Q11	TRA_FDC602P	51C2	
Q12	TRA_2N3904	44D7	
Q13	TRA_2N7002	51B2	
Q14	TRA_2N7002	51C7	
Q15	TRA_2N7002	51B7	
Q16	TRA_2N7002	51A7	
Q17	TRA_2N7002	51B6	
Q18	TRA_2N7002	51A7	
Q19	TRA_2N7002	51A6	
Q20	TRA_FDC602P	51D7	
Q21	TRA_2N7002	50C1	
Q22	TRA_2N7002	50D1	
Q23	TRA_2N7002	50C2	
Q24	TRA_2N7002	50C2	
Q25	TRA_IRF7807Z	47B5	
Q26	TRA_IRF7807Z	47B5	
Q27	TRA_SUD70N03	49B4	
Q28	TRA_SUD50N03	49B4	
Q29	TRA_2N7002	45D8	
Q30	TRA_2N3904	36C7	
Q31	TRA_2N7002	41A8	
Q32	TRA_2N7002	39C7	
Q33	TRA_2N3904	43A2	
Q34	TRA_SUD70N03	48B4	
Q35	TRA_2N7002	40D4	
Q36	TRA_2N7002	42D3	
Q37	TRA_FDC602P	51C6	
Q38	TRA_2N7002	51B6	
Q39	TRA_2N3904	50C7	
Q40	TRA_SUD70N03	45C4	
Q41	TRA_2N7002	15B2	
Q42	TRA_2N7002	15C2	
Q43	TRA_SUD70N03	45C4	
Q44	TRA_SUD50N03	45C4	
Q45	TRA_IRF7807Z	50B4	
Q46	TRA_IRF7807Z	50C4	
Q47	TRA_SUD50N03	50A4	
Q48	TRA_SUD50N03	50A4	
Q49	TRA_SUD70N03	45B4	
Q50	TRA_SUD50N03	45B4	
Q51	TRA_SUD70N03	45B4	
Q52	TRA_2N7002	15B2	
Q53	TRA_2N7002	15A2	
Q54	TRA_2N7002	15B2	
R1	RES	36D4	
R2	RES	25B4	
R3	RES	25B4	
R4	RES	21A4	
R5	RES	21A3	
R6	RES	21A4	
R7	RES	25B5	
R8	RES	36C4	
R9	RES	36C4	
R10	RES	36C4	
R11	RES	36C4	
R12	RES	36C3	
R13	RES	36C3	
R14	RES	36C3	
R15	RES	36C3	
R16	RES	36B3	
R17	RES	21A3	
R18	RES	21A4	
R19	RES	25B5	
R20	RES	19C2	
R21	RES	51D3	
R22	RES	51C4	
R23	RES	51D3	
R24	RES	19A3	
R25	RES	19A3	
R26	RES	35B4	
R27	RES	35C4	
R28	RES	35A8	
R29	RES	35B7	
R30	RES	35C3	
R31	RES	19A3	
R32	RES	19A3	
R33	RES	35C4	
R34	RES	35C7	
R35	RES	36D6	
R36	RES	18B8	
R37	RES	35C4	
R38	RES	35C7	
R39	RES	36D6	
R40	RES	35C4	
R41	RES	18B8	
R42	RES	35B4	
R43	RES	33D7	
R44	RES	33D7	
R45	RES	33C7	
R46	RES	33C7	
R47	RES	33B7	
R48	RES	33B7	
R49	RES	18B7	
R50	RES	18B7	
R51	RES	42B7	
R52	RES	18C5	
R53	RES	19A4	
R54	RES	18D3	
R55	RES	19A4	
R56	RES	18D2	
R57	RES	19A4	
R58	RES	18D3	
R59	RES	18C2	
R60	RES	19A4	
R61	RES	18A3	
R62	RES	18A2	
R63	RES	19A4	
R64	RES	18D3	
R65	RES	19A4	
R66	RES	18D2	
R67	RES	18D2	
R68	RES	19A4	
R69	RES	19A4	
R70	RES	18D3	
R71	RES	18D6	
R72	RES	17A5	
R73	RES	26C2	
R74	RES	26D2	
R75	RES	35B8	
R76	RES	35B8	
R77	RES	26D2	
R78	RES	32A7	
R79	RES	26C2	
R80	RES	17A5	
R81	RES	19A7	
R82	RES	12A8	
R83	RES	18A5	
R84	RES	18G2	
R85	RES	23D6	
R86	RES	23D6	
R87	RES	26B3	
R88	RES	18A5	
R89	RES	32D3	
R90	RES	18G3	
R91	RES	23D6	
R92	RES	23D6	
R93	RES	12A8	
R94	RES	26A3	
R95	RES	18A5	
R96	RES	35B1	
R97	RES	19A7	
R98	RES	23D6	
R99	RES	42D8	
R100	RES	26A8	
R101	RES	19A7	
R102	RES	23C5	
R103	RES	19B2	
R104	RES	19B2	
R105	RES	19C2	
R106	RES	19C2	
R107	RES	23D5	
R108	RES	42D7	
R109	RES	42D6	
R110	RES	42C8	
R111	RES	18G2	
R112	RES	23D6	
R113	RES	23D5	
R114	RES	23C5	
R115	RES	23C5	
R116	RES	26C6	
R117	RES	18G3	
R118	RES	22D3	
R119	RES	23C5	
R120	RES	42B8	
R121	RES	42C8	
R122	RES	19A7	
R123	RES	19D2	
R124	RES	23C5	
R125	RES	26D5	
R126	RES	26C6	
R127	RES	32B8	
R128	RES	32B8	
R129	RES	32D3	
R130	RES	18D2	
R131	RES	18D3	
R132	RES	19D2	
R133	RES	22D3	
R134	RES	26B8	
R135	RES	42D7	
R136	RES	26C5	
R137	RES	12B1	
R138	RES	30B3	
R139	RES	30B4	
R140	RES	19A7	
R141	RES	23B5	
R142	RES	26C5	
R143	RES	18G2	
R144	RES	23B2	
R145	RES	22D3	
R146	RES	19A7	
R147	RES	19A7	
R148	RES	19C2	
R149	RES	23B5	
R150	RES	48C5	
R151	RES	20A4	
R152	RES	20A5	
R153	RES	19A7	
R154	RES	18G3	
R155	RES	18G2	
R156	RES	19C2	
R157	RES	23B3	
R158	RES	19D2	
R159	RES	19A7	
R160	RES	17A5	
R161	RES	16D1	
R162	RES	41A5	
R163	RES	20A4	
R164	RES	18G3	
R165	RES	35C4	
R166	RES	20A4	
R167	RES	19A7	
R168	RES	17A7	
R169	RES	17A4	
R170	RES	22B5	
R171	RES	22B6	
R172	RES	12A1	
R173	RES	22C7	
R174	RES	22C6	
R175	RES	40D4	
R176	RES	20A4	
R177	RES	17A5	
R178	RES	22C7	
R179	RES	22C6	
R180	RES	40D5	
R181	RES	41A4	
R182	RES	41A4	
R183	RES	22C3	
R184	RES	23C6	
R185	RES	22B6	
R186	RES	19A6	
R187	RES	19A6	
R188	RES	22B2	
R191	RES	22B6	
R192	RES	17A2	
R193	RES	17A2	
R194	RES	22B6	
R195	RES	17A3	
R196	RES	17A3	
R197	RES	16A7	
R198	RES	17C1	
R199	RES	22D6	
R200	RES	22D6	
R203	RES	16C8	
R204	RES	16B8	
R205	RES	16A8	
R206	RES	22D6	
R207	RES	23D2	
R208	RES	23D2	
R210	RES	17B7	
R211	RES	16C7	
R212	RES	30B3	
R213	RES	23C5	
R214	RES	12B1	
R215	RES	16C7	
R216	RES	16B7	
R217	RES	16D3	
R218	RES	30D6	
R219	RES	30D6	
R220	RES	16C7	
R221	RES	16D1	
R222	RES	16D3	
R223	RES	16D1	
R224	RES	16C7	
R225	RES	16D7	
R226	RES	16C7	
R227	RES	30C6	
R228	RES	28C7	
R230	RES	30C6	
R231	RES	28C8	
R232	RES	28C6	
R233	RES	16B3	
R234	RES	16D1	
R235	RES	12A1	
R236	RES	26D2	
R237	RES	23C5	
R238	RES	27A6	
R239	RES	42B7	
R240	RES	42B6	
R241	RES	27A5	
R242	RES	42B5	
R243	RES	27A6	
R244	RES	27A5	
R245	RES	42B5	
R246	RES	23B7	
R247	RES	28A2	
R248	RES	27A7	
R249	RES	42B5	
R250	RES	27A7	
R251	RES	51B3	
R252	RES	30C7	
R253	RES	30C8	
R254	RES	34B4	
R255	RES	30C7	
R256	RES	30C8	
R257	RES	34B3	
R258	RES	37D5	
R259	RES	30C7	
R261	RES	12D5	
R262	RES	30C8	
R263	RES	37D4	
R264	RES	28D1	
R265	RES	38B4	
R266	RES	37C6	
R267	RES	28B1	
R268	RES	38B4	
R269	RES	34C4	
R270	RES	37D2	
R271	RES	28B3	
R272	RES	28B3	
R273	RES	37D2	
R274	RES	28C7	
R275	RES	34C4	
R276	RES	28C8	
R277	RES	51B2	
R278	RES	51B3	
R279	RES	51B2	
R280	RES	44D8	
R281	RES	44D7	
R282	RES	44D7	
R283	RES	51B3	
R284	RES	51A3	
R285	RES	31C1	
R286	RES	12A3	
R287	RES	44D5	
R288	RES	12D5	
R289	RES	28C8	
R290	RES	44D8	
R291	RES	28C7	
R292	RES	28C7	
R293	RES	31C5	
R294	RES	28C1	
R295	RES	47B3	
R296	RES	47B7	
R297	RES	44D6	
R298	RES	44B1	
R299	RES	47B3	
R300	RES	51C8	
R301	RES	47B5	
R302	RES	51A6	
R303	RES	34D7	
R304	RES	47B3	
R305	RES	28A2	
R306	RES	28B8	
R307	RES	34D7	
R308	RES	8B1	
R309	RES	47B7	
R310	RES	9A4	
R311	RES	4B8	
R312	RES	4A8	
R313	RES	8A2	
R314	RES	8B2	
R315	RES	47B3	
R316	RES	47B7	
R317	RES	47C5	
R318	RES	47C6	
R319	RES	9A5	
R320	RES	47B5	
R321	RES	9A5	
R322	RES	50C2	
R323	RES	50D2	
R324	RES	42B5	
R326	RES	35B3	
R328	RES	29D3	
R329	RES	29D3	
R330	RES	50A8	
R331	RES	50B8	
R332	RES	50A7	
R333	RES	28A2	
R334	RES	49B1	
R335	RES	50A5	
R336	RES	50C5	
R337	RES	50B5	
R338	RES	9C5	
R339	RES	9D5	
R340	RES	9D5	
R341	RES	9C5	
R342	RES	9A7	
R343	RES	9C6	
R344	RES	9A7	
R345	RES	9A7	
R346	RES	7C7	
R347	RES	7C7	
R348	RES	7C7	
R349	RES	7B7	
R350	RES	7A7	
R351	RES	9C5	
R352	RES	9C6	
R353	RES	9A7	
R354	RES	9C6	
R355	RES	9C7	
R356	RES	6C4	
R357	RES	6C4	
R358	RES	9C6	
R359	RES	9C7	
R360	RES	9C6	
R361	RES	45B3	
R362	RES	45B3	
R363	RES	6C5	
R364	RES	6C5	
R365	RES	6C4	
R366	RES	9C7	
R367	RES	6C4	
R368	RES	6C4	
R369	RES	49C6	
R370	RES	50D5	
R371	RES	49B6	
R372	RES	46D4	
R373	RES	32A7	
R374	RES	6C6	
R375	RES	6C6	
R376	RES	6C7	
R377	RES	6C7	
R378	RES	6C7	
R379	RES	6C8	
R380	RES	6C7	
R381	RES	6C8	
R382	RES	6C8	
R383	RES	6C8	
R384	RES	45C5	
R385	RES	46D6	
R386	RES	45B5	
R387	RES	45B5	
R388	RES	45B6	
R389	RES	45B6	
R390	RES	35C1	
R391	RES	35C2	
R392	RES	41B3	
R393	RES	35C2	
R394	RES	35C2	
R395	RES	36B7	
R396	RES	28A2	
R397	RES	26A7	
R398	RES	28A2	
R399	RES	26B7	
R400	RES	41C4	
R401	RES	26B6	
R402	RES	36B4	
R403	RES	19B2	
R404	RES	36D8	
R405	RES	15C2	
R406	RES	41D4	
R407	RES	40C5	
R408	RES	26A6	
R409	RES	36D7	
R410	RES	40B5	
R411	RES	36C5	
R412	RES	41C4	
R413	RES	43B5	
R414	RES	43B5	
R415	RES	19A3	
R416	RES	19A3	
R417	RES	36C7	
R418	RES	36C6	
R419	RES	41D4	
R420	RES	40B4	
R421	RES	43B5	
R422	RES	36C6	
R423	RES	36B5	
R424	RES	36C7	
R425	RES	36C7	
R426	RES	26A5	
R427	RES	26B5	
R428	RES	19A3	
R429	RES	19A3	
R430	RES	36B6	
R431	RES	36C7	
R432	RES	36C7	
R433	RES	36B6	
R434	RES	40C4	
R435	RES	40C4	
R436	RES	40B4	
R437	RES	40B4	
R438	RES	36C8	
R439	RES	26B4	
R440	RES	41A8	
R441	RES	41D6	
R442	RES	40C4	
R443	RES	26A4	
R444	RES	41C6	
R445	RES	26B6	
R446	RES	41C6	
R447	RES	41D6	
R448	RES	40B3	
R449	RES	26A6	
R450	RES	33B5	
R451	RES	33B6	
R452	RES	33C5	
R453	RES	33C6	
R454	RES	33D5	
R455	RES	33D6	
R456	RES	33B7	
R457	RES	33B7	
R458	RES	33C7	
R459	RES	33C7	
R460	RES	33D7	
R461	RES	33D7	
R462	RES	40B3	
R463	RES	18B8	
R464	RES	32C3	
R465	RES	32C3	
R466	RES	32C2	
R467	RES	32C2	
R468	RES	32C3	
R469	RES	32C3	
R470	RES	32B3	
R471	RES	15C1	
R472	RES	41C7	
R473	RES	41D7	
R474	RES	40C3	
R475	RES	48B1	
R476	RES	32B3	
R477	RES	41B4	
R478	RES	41B5	
R479	RES	19A6	
R480	RES	32B2	
R481	RES	39B6	
R482	RES	39C6	
R483	RES	19A6	
R484	RES	32A7	
R485	RES	35B2	
R486	RES	35B2	
R487	RES	43A6	
R488	RES	43B4	
R489	RES	43B4	
R490	RES	32B3	
R491	RES	35B2	
R492	RES	35B1	
R493	RES	28A2	
R494	RES	32B7	
R495	RES	15B1	
R496	RES	48C2	
R497	RES	15C1	
R498	RES	43A2	
R499	RES	48C3	
R500	RES	19C2	
R501	RES	39C7	
R502	RES	39D7	
R503	RES	48B6	
R504	RES	48C3	
R505	RES	48C5	
R506	RES	19A7	
R507	RES	15B1	
R508	RES	15B3	
R509	RES	19A7	
R510	RES	30B4	
R511	RES	30A3	
R512	RES	15C3	
R515	RES	48B5	
R517	RES	39C5	
R518	RES	46B5	
R519	RES	46A5	
R521	RES	39C5	
R522	RES	42B8	
R523	RES	48C6	
R524	RES	39B4	
R525	RES	42B7	
R526	RES	42B7	
R527	RES	48B7	
R528	RES	39C4	
R529	RES	48C6	
R531	RES	39C2	
R532	RES	39C4	
R533	RES	26D6	
R535	RES	26D1	
R537	RES	27A5	
R540	RES	24A6	
R541	RES	26A6	
R542	RES	26B6	
R543	RES	26B1	
R545	RES	16A7	
R546	RES	24A5	
R547	RES	24A6	
R548	RES	27A7	
R549	RES	16A8	
R550	RES	24A5	
R551	RES	24A5	
R552	RES	26C8	
R553	RES	26D8	
R554	RES	22C7	
R555	RES	22C3	
R556	RES	22C2	
R557	RES	22C2	
R558	RES	17B7	
R559	RES	24B6	
R560	RES	26C7	
R561	RES	26D7	
R562	RES	22C6	
R563	RES	27A6	
R564	RES	23C5	
R565	RES	28D5	
R566	RES	30D6	
R567	RES	24B5	
R568	RES	24B5	
R569	RES	22B3	
R570	RES	24B6	
R571	RES	28D8	
R572	RES	28D8	
R573	RES	28C6	
R574	RES	28C8	
R575	RES	34C1	
R576	RES	34C1	
R577	RES	28C7	
R578	RES	30B6	
R579	RES	30A8	
R580	RES	16B3	
R581	RES	24B5	
R582	RES	24C5	
R583	RES	26D3	
R584	RES	29D7	
R585	RES	29D6	
R586	RES	28D6	
R587	RES	16B3	
R588	RES	26C3	
R589	RES	28A8	
R590	RES	28D6	
R591	RES	24C6	
R592	RES	23A7	
R593	RES	24C5	
R594	RES	24D5	
R595	RES	26D5	
R596	RES	26D5	
R597	RES	26C3	
R598	RES	26D3	
R599	RES	22A8	
R600	RES	24D6	
R601	RES	51B3	
R602	RES	23A7	
R603	RES	24D5	
R604	RES	44A3	
R605	RES	44A5	
R606	RES	44A5	
R607	RES	51A5	
R608	RES	51A5	
R609	RES	51A5	
R610	RES	46B4	
R611	RES	28A6	
R612	RES	51A5	
R613	RES	29A8	
R614	RES	51A5	
R615	RES	51A6	
R616	RES	30D8	
R617	RES	30D8	
R618	RES	30C7	
R619	RES	16D6	
R620	RES	28D5	
R621	RES	30C6	
R622	RES	16C6	
R623	RES	37D5	
R624	RES	37A7	
R625	RES	12B6	
R626	RES	37D2	
R627	RES	37D5	
R628	RES	28D5	
R629	RES	28D5	

| | | |

ZT14	HOLE_VIA	18B2	
ZT15	HOLE_VIA	18B2	
ZT16	HOLE_VIA	18B2	
ZT17	HOLE_VIA	18B2	
ZT18	HOLE_VIA	18B2	
ZT19	HOLE_VIA	18A2	
ZT20	HOLE_VIA	18G2	
ZT21	HOLE_VIA	18E2	
ZT22	HOLE_VIA	18F2	
ZT23	HOLE_VIA	18F2	
ZT24	HOLE_VIA	18F2	
ZT25	HOLE_VIA	18F2	
ZT26	HOLE_VIA	18F2	
ZT27	HOLE_VIA	18E2	
ZT28	HOLE_VIA	18D2	
ZT29	HOLE_VIA	18G2	
ZT30	HOLE_VIA	18F2	
ZT31	HOLE_VIA	18F2	
ZT32	HOLE_VIA	18E2	
ZT33	HOLE_VIA	18E2	
ZT34	HOLE_VIA	18F2	
ZT35	HOLE_VIA	18E2	
ZT36	HOLE_VIA	18E2	
ZT37	HOLE_VIA	18F2	
ZT38	HOLE_VIA	18E2	
ZT39	HOLE_VIA	3B3	
ZT40	HOLE_VIA	3B3	
ZT41	HOLE_VIA	3B3	
ZT42	HOLE_VIA	3B3	
ZT43	HOLE_VIA	3A3	
ZT44	HOLE_VIA	3A3	
ZT45	HOLE_VIA	3A3	
ZT46	HOLE_VIA	3B3	
ZT47	HOLE_VIA	3B3	
ZT48	HOLE_VIA	3B3	
ZT49	HOLE_VIA	3B3	
ZT50	HOLE_VIA	3A3	
ZT51	HOLE_VIA	3A3	
ZT52	HOLE_VIA	3A3	
ZT53	HOLE_VIA	3B2	
ZT54	HOLE_VIA	3B2	
ZT55	HOLE_VIA	3B2	
ZT56	HOLE_VIA	3B2	
ZT57	HOLE_VIA	3A2	
ZT58	HOLE_VIA	3A2	
ZT59	HOLE_VIA	3B2	
ZT60	HOLE_VIA	3B2	
ZT61	HOLE_VIA	3B2	
ZT62	HOLE_VIA	3B2	
ZT63	HOLE_VIA	3A2	
ZT64	HOLE_VIA	3B1	
ZT65	HOLE_VIA	3B1	
ZT66	HOLE_VIA	3B1	
ZT67	HOLE_VIA	3B1	
ZT68	HOLE_VIA	3A1	

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6497	13

SCALE: NONE

SHT 69 OF 69