1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
E		303550	PRODUCTION RELEASED	11/11/03	?

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING
THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE
SIZE D

Apple Computer Inc.

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TITLE
SCHEM,PBG4,MLB,P88

DRAWING NUMBER 051-6403 REV. E

SHT 1 OF 46

J21
Inverter Connector P.31

J17
LCD Panel Connector P.31

J1
S-Video Connector P.31

J4
DVI-I Connector P.31

LVDS
EDID (I2C)
S-VIDEO
COMPOSITE
TMDS
RGB
(DDC TOO)

J7
FireWire Connector P.29

J2
Ethernet Connector P.28

U4
ATI Mobility M7_M9
P.19-21

MEMORY CH. A
(INTERNAL MEM)
MEMORY CH. B

U2/U7
16MB DDR SDRAM P.22

VMEM BUS
2.5V
64BITS
183 MHZ

2 DATA PAIRS @ 200MHz
4 DATA PAIRS

U5
FireWire PHY P.29

U8
Ethernet PHY P.28

1394 OHCI
3.3V
8BIT TX/RX
50MHZ

G/MII
3.3V
8BIT TX
8BIT RX
125MHZ

AGP BUS
1.5V/3.3V
32BITS
66MHZ

J11
CardBus Connector P.18

J5/J6
USB Connector P.30

33MHZ
16/32 BITS
3.3V/5V

Port 3
Port 4

U52
TI PCI1410A CardBus Controller P.18

U51
NEC USB 2.0 Host Controller P.17

32BITS
32BITS

U9
FIREWIRE 400 MB/S P.10
ETHERNET 10/100/1000 P.10
4X AGP P.8
PCI 64BITS 33/66MHZ P.9
Upper 32 bits pulled up
UNI-N 1.5
MEMORY P.7
I2C P.10
MAXBUS P.6
BOOTROM P.7

PCI BUS
64BITS
33MHZ
3.3V

U53
Key Largo (Expanded View P.3)

32BITS

U23
BOOT ROM 1M X 8 P.23

MEMORY BUS
3.3V
133MHZ
64BITS

I2C

MAXBUS
1.8V
133MHZ
32BIT ADDRESS
64BIT DATA

U22
IMI C5005 System Clock P.23

I2C

U47
PMU P.34

Power Supply & Charger P.35-39

SMBUS
3.3V

Battery P.35

J16
SDRAM DIMM 0
SDRAM DIMM 1 SO-DIMM Connector P.7

Fan Circuit P.24

U10
Apollo CPU (XPC7455) P.13-14

CPU PLL Config P.12

SERIAL
5V

J28
Trackpad Connector P.33

J14
Keyboard Connector P.33

L3 BUS
1.5V
200 MHZ
18BIT ADDRESS
64BIT DATA

U11/U42
L3 Cache P.15

SYSTEM BLOCK DIAGRAM

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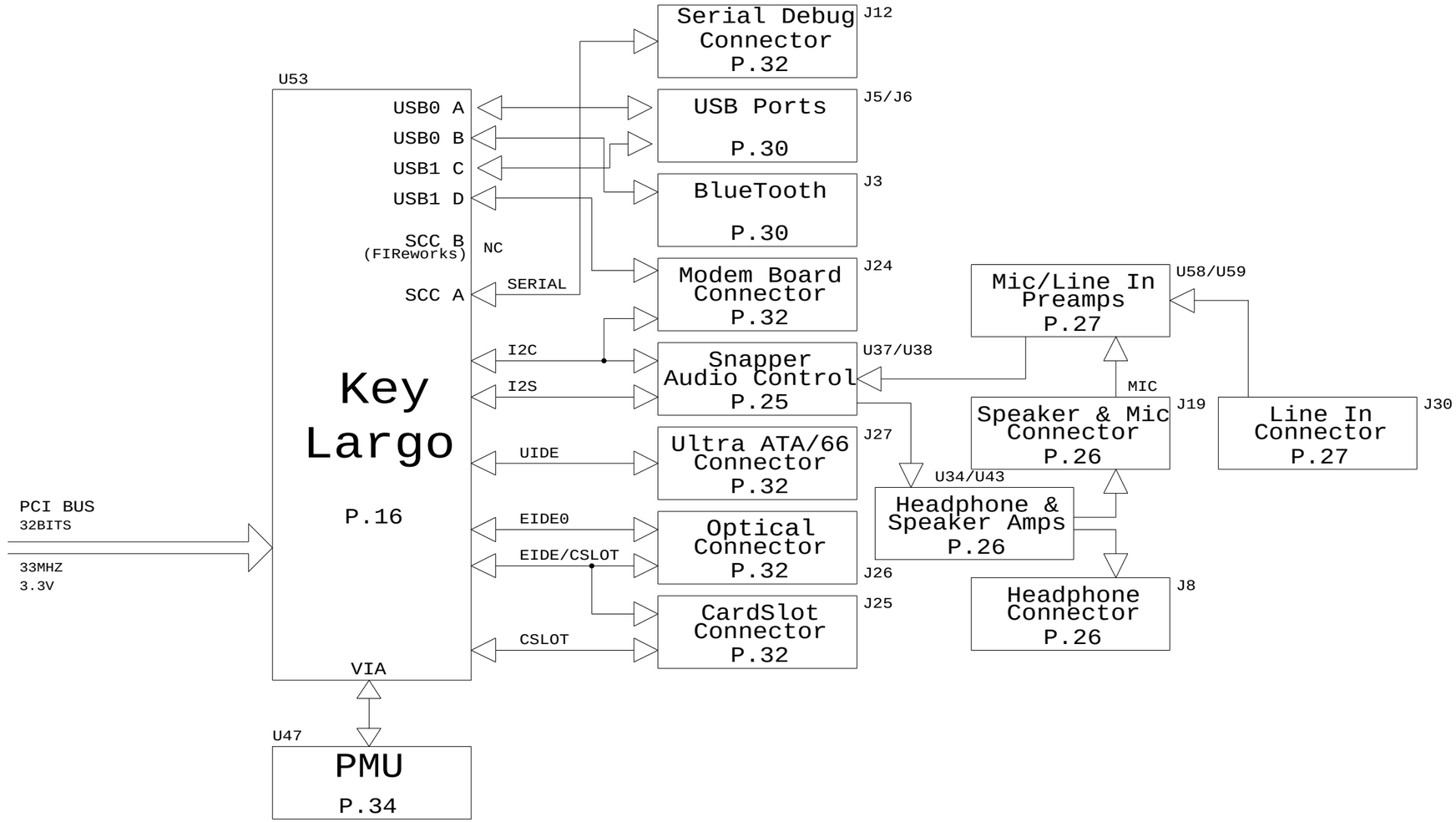
SIZE	DRAWING NUMBER	REV.
D	051-6403	E

SCALE	SHT	OF
NONE	2	46



SYSTEM BLOCK DIAGRAM

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APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6403 | REV. E

SCALE NONE | SHT 3 OF 46

POWER SYSTEM ARCHITECTURE

AC ADAPTER IN

INPUT14_24V

BUCK REGULATOR CHARGER (LTC1625)

PBUS

BACKLIGHT INVERTER

DCDC_EN

$\overline{SD}$
ON3
ON5

MAIN 3V/5V DC/DC CONVERTER (MAX785)

+5V

+3.3V

+1.8V

LDO (LT1962)

+1.41V L3 I/O

CPU_VCORE (+1.15V/+1.3V)

DC/DC (MAX1717)

$\overline{SHDN}$

DCDC_EN SLEEP

+5V

DC/DC (LTC1773)

+1.25V ATI M7_M9 CORE

BACKUP BATTERY CIRCUIT CHARGES OFF PBUS AND PREVENTS PBUS FROM DROPPING BELOW 6V (UNTIL DRAINED)

BACKUP BATTERY

CHARGER INPUT & BOOST OUTPUT

+5V

DC/DC (MAX1644)

$\overline{SHDN}$

+2.5V ATI M7_M9 DDR CORE AND I/O
L3 CORE

DCDC_EN

+3.3V

DC/DC (MAX1644)

$\overline{SHDN}$

+1.8V MAX BUS INTERFACE
CPU I/O

DCDC_EN

4S 2P LITHIUM ION

POWER BLOCK DIAGRAM

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APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6403 | REV. E

SCALE NONE | SHT 4 OF 46

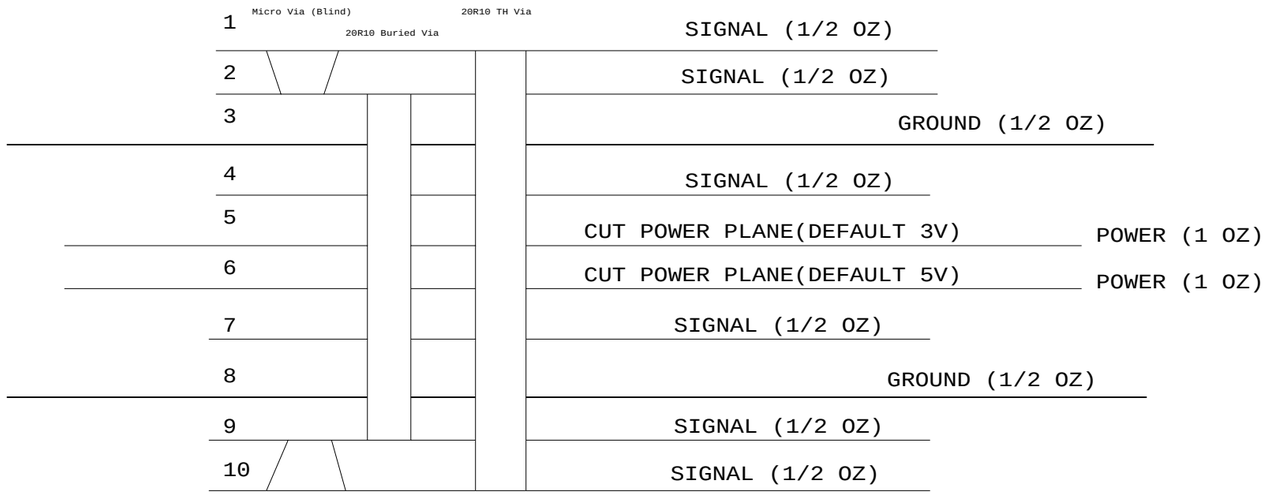
PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

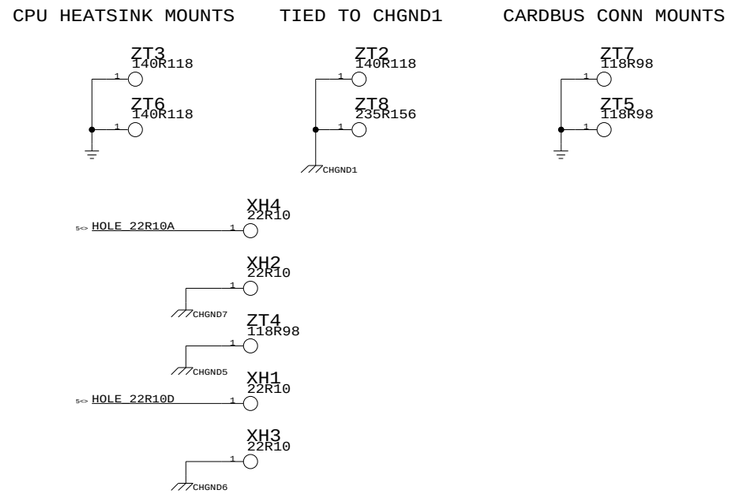
IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 10
SIGNAL TRACE WIDTH: 4 MILS
PREPREG THICKNESS: 3 - 6 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

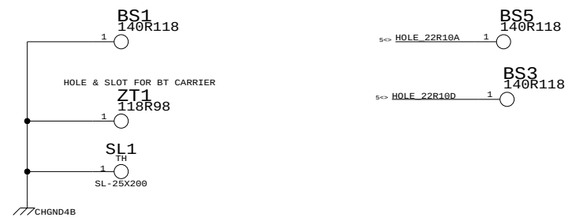
BOARD STACK-UP AND CONSTRUCTION



BOARD HOLES



PCB BOARD STANDOFFS



BOARD INFORMATION

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SIZE	DRAWING NUMBER	REV.
D	051-6403	E

SCALE	SHT	OF
NONE	5	46

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
343S1303	343S0347		U9	

+3V_MAIN

R481 22 5% 1/16W MF 402

+3V_UNIN_MAXPLL_MAIN 43<>

C662 4.7uF N20P80% 10V CERM 805

C637 0.01uF 20% 16V CERM 402

43<> +1_8V_UNIN_MAXPLL_MAIN

C638 0.01uF 20% 16V CERM 402

C607 4.7uF N20P80% 10V CERM 805

+1_8V_MAIN

R440 22 5% 1/16W MF 402

AE8 AF5 AE6

MAX_CLKIN_VDD3 MAXPLLAVD MAXPLLDVD

CRITICAL

U9
UNI-N-1.5
(1 OF 5)
PBGA-UNIN-1.5.1

MAXBUS INTERFACE

40<> SYSCLK_UNIN	AH2	MAXCLK	
13> CPU_BR_L	AJ12	BR_0	
6< 40<> 13> CPU_BG_L	AF17	BG_0	
UNIN_BR_1_L_PU	AF14	BR_1	
NC	AF15	BG_1	
6< 40<> 13> CPU_TS_L	AD15	TS	
40<> 13<> CPU_ADDR<0>	AK4	A_0	
40<> 13<> CPU_ADDR<1>	AH4	A_1	
40<> 13<> CPU_ADDR<2>	AH3	A_2	
40<> 13<> CPU_ADDR<3>	AF6	A_3	
40<> 13<> CPU_ADDR<4>	AH5	A_4	
40<> 13<> CPU_ADDR<5>	AJ2	A_5	
40<> 13<> CPU_ADDR<6>	AJ4	A_6	
40<> 13<> CPU_ADDR<7>	AJ3	A_7	
40<> 13<> CPU_ADDR<8>	AD9	A_8	
40<> 13<> CPU_ADDR<9>	AK3	A_9	
40<> 13<> CPU_ADDR<10>	AH10	A_10	
40<> 13<> CPU_ADDR<11>	AJ8	A_11	
40<> 13<> CPU_ADDR<12>	AH9	A_12	
40<> 13<> CPU_ADDR<13>	AE9	A_13	
40<> 13<> CPU_ADDR<14>	AH7	A_14	
40<> 13<> CPU_ADDR<15>	AE10	A_15	
40<> 13<> CPU_ADDR<16>	AK8	A_16	
40<> 13<> CPU_ADDR<17>	AE11	A_17	
40<> 13<> CPU_ADDR<18>	AJ7	A_18	
40<> 13<> CPU_ADDR<19>	AH8	A_19	
40<> 13<> CPU_ADDR<20>	AJ9	A_20	
40<> 13<> CPU_ADDR<21>	AF8	A_21	
40<> 13<> CPU_ADDR<22>	AJ6	A_22	
40<> 13<> CPU_ADDR<23>	AD11	A_23	
40<> 13<> CPU_ADDR<24>	AF11	A_24	
40<> 13<> CPU_ADDR<25>	AF9	A_25	
40<> 13<> CPU_ADDR<26>	AH6	A_26	
40<> 13<> CPU_ADDR<27>	AF7	A_27	
40<> 13<> CPU_ADDR<28>	AF10	A_28	
40<> 13<> CPU_ADDR<29>	AJ5	A_29	
40<> 13<> CPU_ADDR<30>	AD10	A_30	
40<> 13<> CPU_ADDR<31>	AK5	A_31	
40<> 13> CPU_CI_L	AE16	CI	
40<> 13<> CPU_GBL_L	AJ14	GBL	
40<> 13> CPU_TBST_L	AK9	TBST	
40<> 13> CPU_TSIZ<0>	AJ10	TSIZ_0	
40<> 13> CPU_TSIZ<1>	AK10	TSIZ_1	
40<> 13> CPU_TSIZ<2>	AF12	TSIZ_2	
40<> 13<> CPU_TT<0>	AE12	TT_0	
40<> 13<> CPU_TT<1>	AF13	TT_1	
40<> 13<> CPU_TT<2>	AJ11	TT_2	
40<> 13<> CPU_TT<3>	AE13	TT_3	
40<> 13<> CPU_TT<4>	AH11	TT_4	
40<> 13> CPU_WT_L	AJ16	WT	
13< 6< 40<> CPU_AACK_L	AK14	AACK	
6< 40<> 13<> CPU_ARTRY_L	AJ12	ARTRY	
13> CPU_HIT_0_L	AK13	HIT_0	
UNIN_HIT_1_L_PU	AH12	HIT_1	
13> CPU_QREQ_L	AH14	QREQ_0	
UNIN_QREQ_1_L_PD	AE15	QREQ_1	
13< 40<> CPU_QACK_L	AF16	QACK	
34<> UNIN_SUSPEND_REQ_L	AB20	SUSPENDREQ	
34<> UNIN_SUSPEND_ACK_L	Y26	SUSPENDACK	
UNIN_MAXBUS_REF	AJ17	MAXREF	
UNIN_SPARE_AB6	R7	SPARE1	

+1_8V_MAIN

R430 49.9 1% 1/16W MF 402

D_0	AJ28	CPU_DATA<0>	14<> 40<>
D_1	AB25	CPU_DATA<1>	14<> 40<>
D_2	AE28	CPU_DATA<2>	14<> 40<>
D_3	AH28	CPU_DATA<3>	14<> 40<>
D_4	AH30	CPU_DATA<4>	14<> 40<>
D_5	AC24	CPU_DATA<5>	14<> 40<>
D_6	AD25	CPU_DATA<6>	14<> 40<>
D_7	AH21	CPU_DATA<7>	14<> 40<>
D_8	AJ21	CPU_DATA<8>	14<> 40<>
D_9	AJ23	CPU_DATA<9>	14<> 40<>
D_10	AG29	CPU_DATA<10>	14<> 40<>
D_11	AE21	CPU_DATA<11>	14<> 40<>
D_12	AE29	CPU_DATA<12>	14<> 40<>
D_13	AF23	CPU_DATA<13>	14<> 40<>
D_14	AH29	CPU_DATA<14>	14<> 40<>
D_15	AE26	CPU_DATA<15>	14<> 40<>
D_16	AE25	CPU_DATA<16>	14<> 40<>
D_17	AC25	CPU_DATA<17>	14<> 40<>
D_18	AJ30	CPU_DATA<18>	14<> 40<>
D_19	AH25	CPU_DATA<19>	14<> 40<>
D_20	AH27	CPU_DATA<20>	14<> 40<>
D_21	AH23	CPU_DATA<21>	14<> 40<>
D_22	AH26	CPU_DATA<22>	14<> 40<>
D_23	AD22	CPU_DATA<23>	14<> 40<>
D_24	AD21	CPU_DATA<24>	14<> 40<>
D_25	AF25	CPU_DATA<25>	14<> 40<>
D_26	AJ25	CPU_DATA<26>	14<> 40<>
D_27	AJ27	CPU_DATA<27>	14<> 40<>
D_28	AE22	CPU_DATA<28>	14<> 40<>
D_29	AK27	CPU_DATA<29>	14<> 40<>
D_30	AJ29	CPU_DATA<30>	14<> 40<>
D_31	AF21	CPU_DATA<31>	14<> 40<>
D_32	AF18	CPU_DATA<32>	14<> 40<>
D_33	AH20	CPU_DATA<33>	14<> 40<>
D_34	AH22	CPU_DATA<34>	14<> 40<>
D_35	AF20	CPU_DATA<35>	14<> 40<>
D_36	AJ24	CPU_DATA<36>	14<> 40<>
D_37	AH19	CPU_DATA<37>	14<> 40<>
D_38	AD19	CPU_DATA<38>	14<> 40<>
D_39	AK21	CPU_DATA<39>	14<> 40<>
D_40	AE20	CPU_DATA<40>	14<> 40<>
D_41	AK23	CPU_DATA<41>	14<> 40<>
D_42	AK22	CPU_DATA<42>	14<> 40<>
D_43	AF24	CPU_DATA<43>	14<> 40<>
D_44	AK26	CPU_DATA<44>	14<> 40<>
D_45	AJ22	CPU_DATA<45>	14<> 40<>
D_46	AJ26	CPU_DATA<46>	14<> 40<>
D_47	AG28	CPU_DATA<47>	14<> 40<>
D_48	AF26	CPU_DATA<48>	14<> 40<>
D_49	AF29	CPU_DATA<49>	14<> 40<>
D_50	AB24	CPU_DATA<50>	14<> 40<>
D_51	AF22	CPU_DATA<51>	14<> 40<>
D_52	AD26	CPU_DATA<52>	14<> 40<>
D_53	AK28	CPU_DATA<53>	14<> 40<>
D_54	AF28	CPU_DATA<54>	14<> 40<>
D_55	AK18	CPU_DATA<55>	14<> 40<>
D_56	AE19	CPU_DATA<56>	14<> 40<>
D_57	AJ19	CPU_DATA<57>	14<> 40<>
D_58	AJ18	CPU_DATA<58>	14<> 40<>
D_59	AH17	CPU_DATA<59>	14<> 40<>
D_60	AH18	CPU_DATA<60>	14<> 40<>
D_61	AH24	CPU_DATA<61>	14<> 40<>
D_62	AF19	CPU_DATA<62>	14<> 40<>
D_63	AJ20	CPU_DATA<63>	14<> 40<> 12<
DBG_0	AJ15	CPU_DBG_L	40<> 6< 13<
DBG_1	AD16	NC	
DRDY_0	AH13	CPU_DRDY_0_L	
DRDY_1	AE14	UNIN_DRDY_1_L_PU	
DTI_0	AH15	CPU_DTI<0>	40<> 13<
DTI_1	AK17	CPU_DTI<1>	40<> 13<
DTI_2	AH16	CPU_DTI<2>	40<> 13<
TA	AE18	CPU_TA_L	40<> 6< 13<
TEA	AE17	CPU_TEA_L	40<> 6< 13<

MAXPLLAVS

AE7

MAXBUS PULL-UPS

+1_8V_SLEEP

RP3 1K 5% 1/16W SM1
40<> 13> 6< CPU_TS_L

RP2 10K 5% 1/16W SM1
40<> 6> CPU_TA_L

RP2 10K 5% 1/16W SM1
40<> 6> CPU_TEA_L

RP4 10K 5% 1/16W SM1
40<> 13> 6< CPU_ARTRY_L

RP4 10K 5% 1/16W SM1
13> CPU_BR_L

RP4 10K 5% 1/16W SM1
13> CPU_HIT_0_L

RP3 1K 5% 1/16W SM1
CPU_DRDY_0_L

R429 10K 5% 1/16W MF 402
40<> 6> CPU_AACK_L

R415 10K 5% 1/16W MF 402
40<> 13> 6> CPU_BG_L

R439 10K 5% 1/16W MF 402
40<> 6> CPU_DBG_L

R401 10K 5% 1/16W MF 402
13> CPU_QREQ_L

UNI-N SECONDARY PROCESSOR SUPPORT

+1_8V_SLEEP

RP4 10K 5% 1/16W SM1
UNIN_HIT_1_L_PU

RP3 1K 5% 1/16W SM1
UNIN_DRDY_1_L_PU

RP3 1K 5% 1/16W SM1
UNIN_BR_1_L_PU

R366 10K 5% 1/16W MF 402
UNIN_QREQ_1_L_PD

UNI-N MAXBUS

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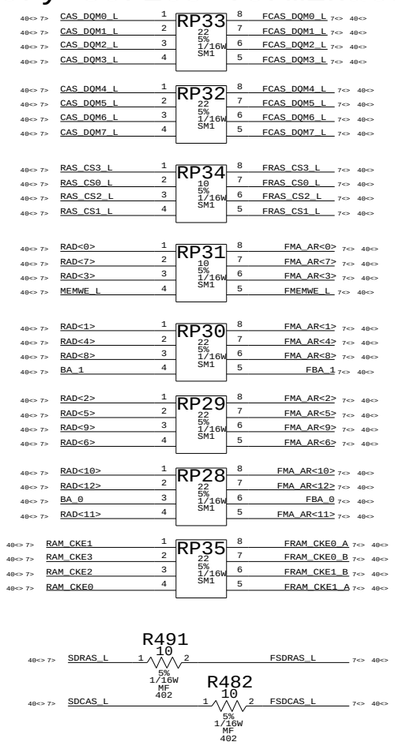
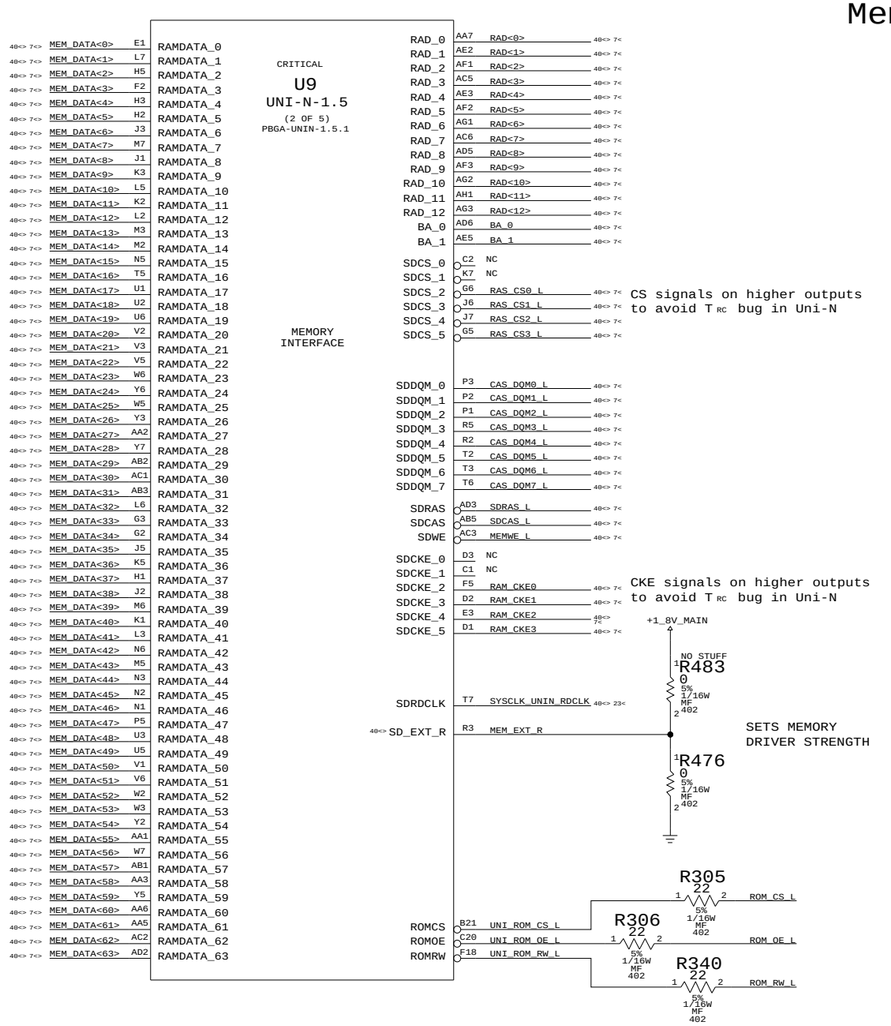
SIZE D | DRAWING NUMBER 051-6403 | REV. E

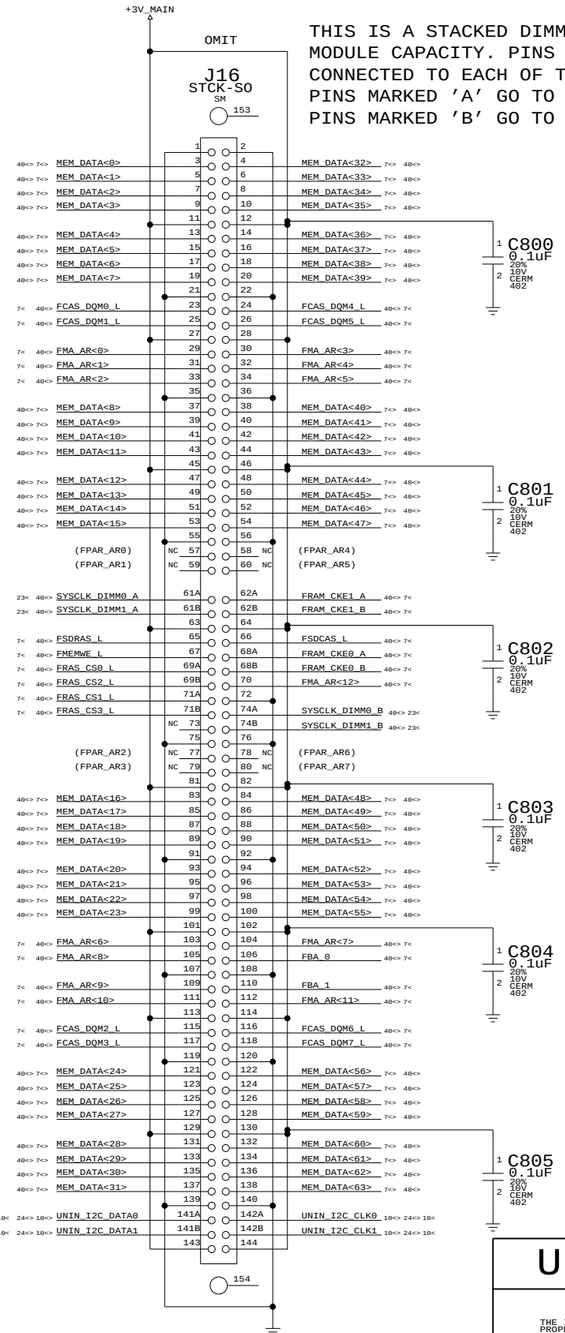
SCALE NONE | SHT 6 OF 46

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516S0062	1	CONN,SODIMM,DUAL STACK,TOP IMPROVED	J16	CRITICAL	?

Memory Series Terminators







THIS IS A STACKED DIMM CONNECTOR WITH A 2 MODULE CAPACITY. PINS THAT HAVE AN A/B ARE CONNECTED TO EACH OF THE SEPARATE DIMMS. PINS MARKED 'A' GO TO THE TOP MODULE AND PINS MARKED 'B' GO TO THE BOTTOM MODULE.

UNI-N MEMORY

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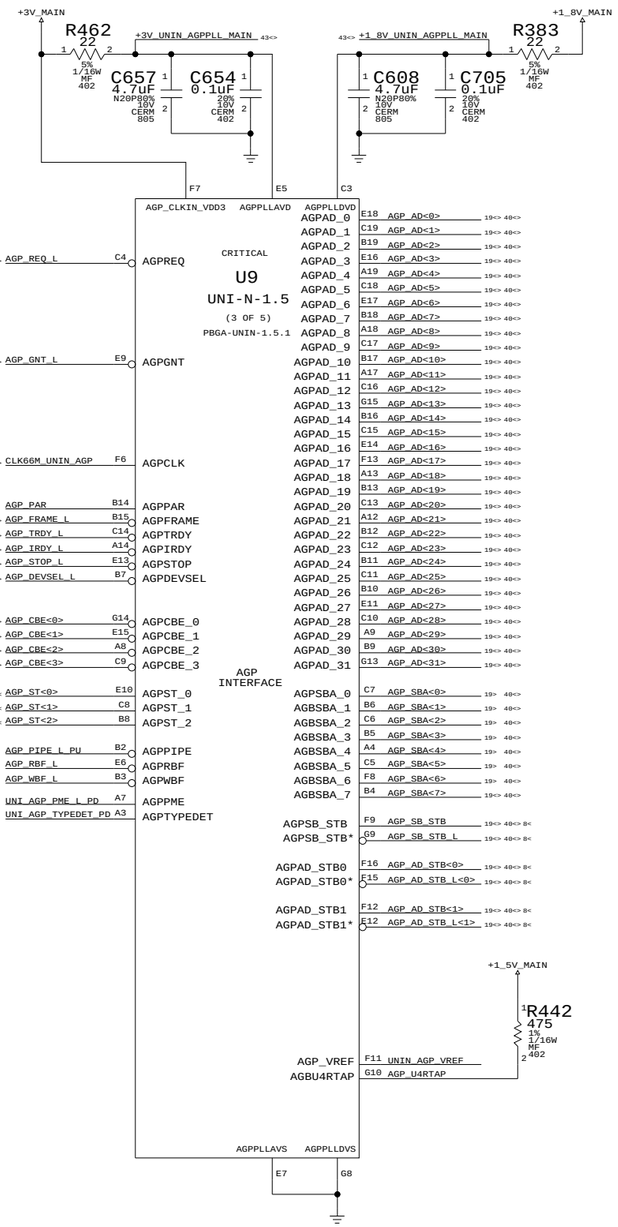
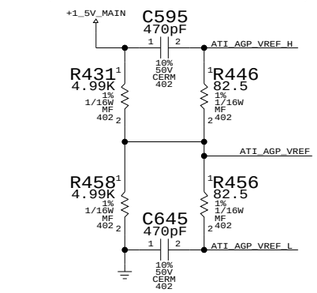
SCALE	SHT	OF
NONE	7	46

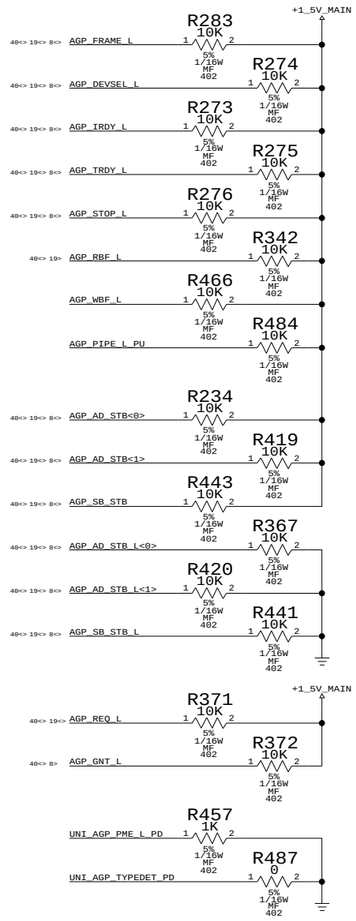


ATI AGP I/O REFERENCE

(PLACE CLOSE TO UNI-N AGP BALLS)



AGP PULL-UPS



UNI-N AGP

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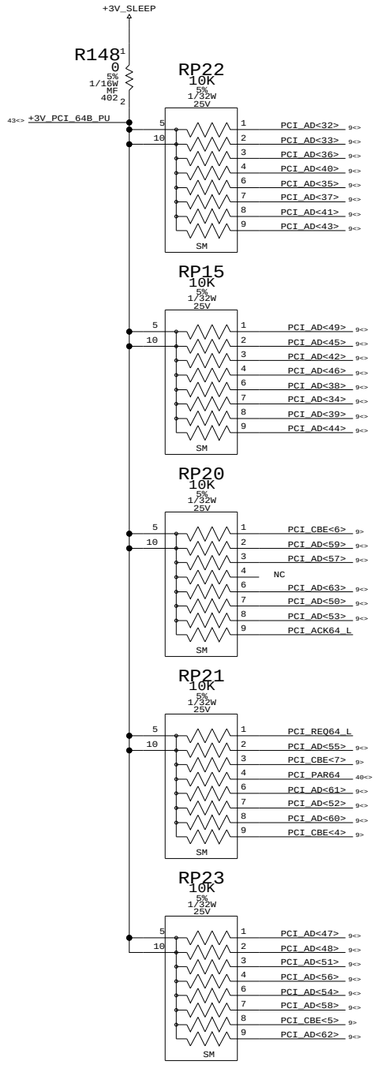
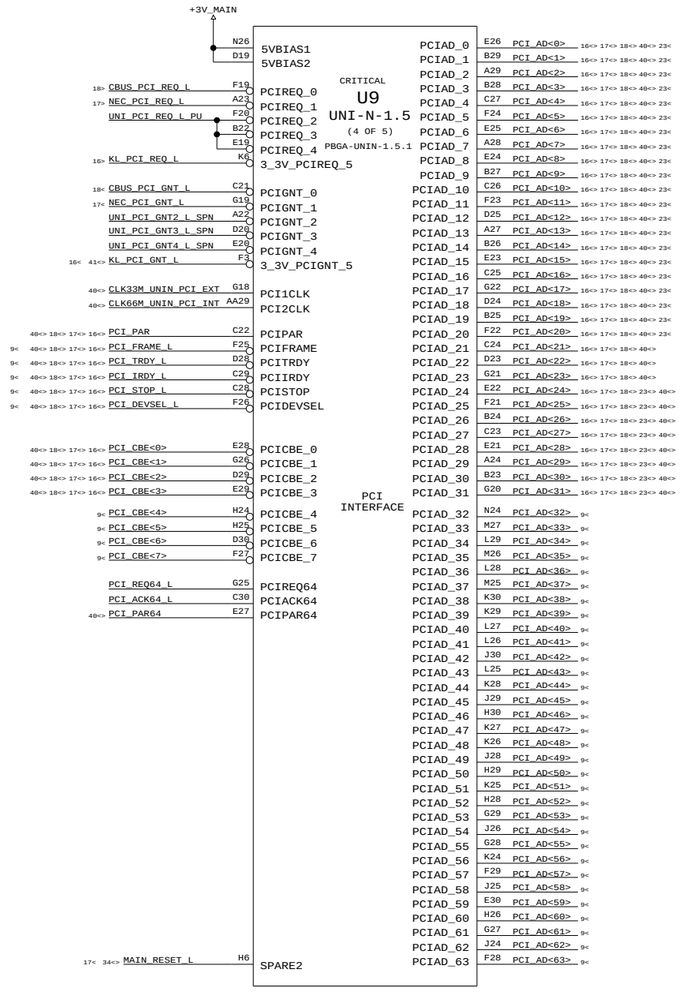
D	051-6403	E

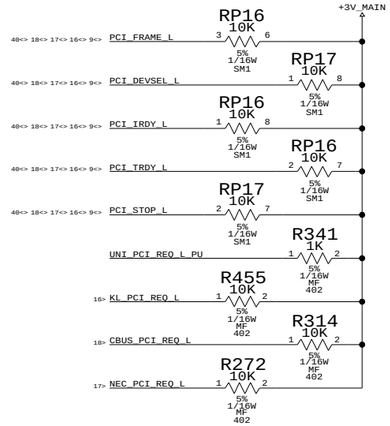
SCALE	SHT	OF
NONE	8	46

64-BIT PCI SUPPORT





PCI PULL-UPS



UNI-N PCI

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SIZE	DRAWING NUMBER	REV.
D	051-6403	E
SCALE: NONE	SHT 9 OF 46	

UNI-N I2C PULL-UPS

+3V_MAIN

RP14 10K 5% 1/16W SM1

1	8	UNIN_I2C_CLK0 7<> 10<> 24<>
2	7	UNIN_I2C_DATA0 7<> 10<> 24<>
3	6	UNIN_I2C_CLK1 7<> 10<> 24<>
4	5	UNIN_I2C_DATA1 7<> 10<> 24<>

UNI-N ETHERNET TERMINATION

R195 33 5% 1/16W MF 402
42<> ENET_PHY_TX_EN

R184 33 5% 1/16W MF 402
42<> ENET_PHY_TX_ER

RP19 33 5% 1/16W SM1

42<> ENET_PHY_TXD<0>	1	8
42<> ENET_PHY_TXD<1>	2	7
42<> ENET_PHY_TXD<2>	3	6
42<> ENET_PHY_TXD<3>	4	5

RP13 33 5% 1/16W SM1

42<> ENET_PHY_TXD<4>	1	8
42<> ENET_PHY_TXD<5>	2	7
42<> ENET_PHY_TXD<6>	3	6
42<> ENET_PHY_TXD<7>	4	5

R242 33 5% 1/16W MF 402
40<> ENET_PHY_GTX_CLK

TEST PULL-UPS

+3V_MAIN

R194	10K 5% 1/16W MF 402	JTAG_ASIC_TMS
R233	10K 5% 1/16W MF 402	JTAG_ASIC_TDI
R206	10K 5% 1/16W MF 402	JTAG_ASIC_TCK
R241	1K 5% 1/16W MF 402	JTAG_ASIC_TRST_L
R307	10K 5% 1/16W MF 402	UNIN_JTAG_TEI
R207	1K 5% 1/16W MF 402	FW_TEST 10<>

+1_8V_MAIN — VDDC X 18: M13 N15 N17 P13 P15 P17 R13 R15 R17 T13 T15 T17 U13 U15 U17 V13 V15 V17

+3V_MAIN — VDD_RAM X 18: AB4 AC7 AD1 AE4 AJ1 B1 F1 G4 H7 K4 L1 N4 N7 R1 T4 U7 W1 W4 R24 F6 AB6 AD12 AE23 R25 R6 AB7

+1_5V_MAIN — V3P X 5: AA24 AD8 AD14 AD18 AD23 AD27 AE30 AG6 AG9 AG12 AG15 AG18 AG21 AG24 AG27 AG30 AK2 AK7 AK12 AK16 AK20 AK25 AK30

V3I X 3: A2 A5 A10

VDD_AGP X 11: A15 D4 D7 D10 D13 D16 G11 G16 F17 F14 F10

CRITICAL

U9

UNI-N-1.5

(5 OF 5)

PBGA-UNIN-1.5.1

VDD_MAX X 23

V3AGP X 4: E8 A20 A25 A30 AA27 AA30 D21 D26 F30 G23 H27 L24 L30 N27 T24 T30 V27

VDD_MISC X 16

V2I X 2: AE24 AD26

GB ETHERNET

40<> CLK_ENET_LINK_TX	V24	TX_CLK
42<> ENET_TX_EN	T28	TX_EN
42<> ENET_TX_ER	R30	TX_ER
42<> ENET_TX_D<0>	T27	TXD_0
42<> ENET_TX_D<1>	T29	TXD_1
42<> ENET_TX_D<2>	U29	TXD_2
42<> ENET_TX_D<3>	T26	TXD_3
42<> ENET_TX_D<4>	R26	TXD_4
42<> ENET_TX_D<5>	V29	TXD_5
42<> ENET_TX_D<6>	V30	TXD_6
42<> ENET_TX_D<7>	U27	TXD_7
40<> CLK_ENET_LINK_RX	V25	RX_CLK
42<> 28> ENET_RX_DV	Y27	RX_DV
42<> 28> ENET_RX_ER	W30	RX_ER
42<> ENET_RXD<0>	U26	RXD_0
42<> ENET_RXD<1>	V26	RXD_1
42<> ENET_RXD<2>	Y29	RXD_2
42<> ENET_RXD<3>	W26	RXD_3
42<> ENET_RXD<4>	Y30	RXD_4
42<> ENET_RXD<5>	W28	RXD_5
42<> ENET_RXD<6>	W24	RXD_6
42<> ENET_RXD<7>	W25	RXD_7
28< 40<> ENET_GBE_REFCLK	U25	GBE_REFCLK
40<> ENET_GTX_CLK	T25	GTX_CLK
42<> 28> ENET_CRS	Y28	CRS
42<> 28> ENET_COL	W29	COL
42<> 28<> ENET_MDIO	V28	MDIO
28< 42<> ENET_MDC	U28	MDC

TEST

JTAG_ASIC_TDI	AC26	TDI
16< JTAG_KL_TDI	AD28	TDO
JTAG_ASIC_TCK	AC28	TCK
JTAG_ASIC_TMS	AD29	TMS
JTAG_ASIC_TRST_L	AB26	TRSTN
UNIN_JTAG_TEI	B20	TEI
10< 24<> 7<> UNIN_I2C_CLK0	AD30	ISCL0
10< 24<> 7<> UNIN_I2C_DATA0	AB27	ISDA0
10< 24<> 7<> UNIN_I2C_CLK1	AC29	ISCL1
10< 24<> 7<> UNIN_I2C_DATA1	AB28	ISDA1

MISC

INTDATA	AA25	MPIC_DATA_L 41<> 16<
INTSYNC	AC30	MPIC_SYNC_L 16>
INTCLK	AA28	MPIC_CLK 16> 41<>
RESET	AA26	UNIN_RESET_L 34<>
PURESET	Y25	UNIN_PU_RESET_L 34<>

FIREWIRE

PHY_DATA_0	P26	FW_LINK_DATA<0> 42<> 29<
PHY_DATA_1	N28	FW_LINK_DATA<1> 42<> 29<
PHY_DATA_2	P24	FW_LINK_DATA<2> 42<> 29<
PHY_DATA_3	N29	FW_LINK_DATA<3> 42<> 29<
PHY_DATA_4	N30	FW_LINK_DATA<4> 42<> 29<
PHY_DATA_5	P25	FW_LINK_DATA<5> 42<> 29<
PHY_DATA_6	P28	FW_LINK_DATA<6> 42<> 29<
PHY_DATA_7	P29	FW_LINK_DATA<7> 42<> 29<
PHY_LPS	R28	FW_PHY_LPS 29<
PHY_CTL_0	P30	FW_LINK_CNTL<0> 42<> 29<
PHY_CTL_1	R27	FW_LINK_CNTL<1> 42<> 29<
PHY_LREQ	R29	FW_LINK_LREQ 42<> 29<
PHY_SCLK	N25	CLK_UNIN_FW 40<>
GPIO_0	M29	FW_C_LKON 16<> 29<>
GPIO_1	M28	FW_TEST 10<
SPARE3	E2	PMU_PME_L 16> 34<> 17< 34<

U14 T18 T16 T14 T1 R18 R16 R14 R4 P27 P18 P16 P14 P7 N18 N16 N14 M30 M24 M4 M1 J27

Y24 Y1 W27 V18 V16 V14 V7 V4 U30 U24 U18 U16

VSS X 82: A1 A6 A11 A16 A21 A26 AA4 AB30 AC27 AD4 AD7 AD13 AD17 AD24 AE1 AF27 AF30 AG4 AG7 AG10 AG13 AG16 AG19 AG22 AG25 AK1 AK6 AK11 AK15 AK19 AK24 AK29 B30 D6 D9 D12 D15 D18 D22 D27 F4 G1 G7 G12 G17 G24 G30 J4

UNI-N MISC I/O

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6403	E

SCALE NONE — SHT 10 OF 46

UNI-N CORE DECOUPLING (18 0.1UF CAPS)

+1_8V_MAIN

C580 2.2uF N20P80% 16V CERM 805
C498 2.2uF N20P80% 16V CERM 805
C455 2.2uF N20P80% 16V CERM 805
C411 2.2uF N20P80% 16V CERM 805

C449 C450 C502 C503 C451 C504 C452 C453 C542 C543 C454 0.1uF 20% 10V CERM 402

C544 C499 C500 C546 C501 C547 C545 0.1uF 20% 10V CERM 402

MAXBUS INTERFACE DECOUPLING (35 0.1UF CAPS)

C409 C497 C287 C661 2.2uF N20P80% 16V CERM 805

C329 C605 C244 C359 C623 C328 C360 C496
C330 C606 C636 C254 C264 C378 C557 C541 C635
C447 C408 C288 C379 C711 C494 C540 C331 C448
C406 C289 C575 C316 C495 C407 C425 C634 C243
0.1uF 20% 10V CERM 402

AGP I/O DECOUPLING (20 0.1UF CAPS)

+1_5V_MAIN

C505 C558 C667 C550 2.2uF N20P80% 16V CERM 805

C706 C656 C685 C684 C613 C508 C594 C643 C644 C507
C612 C560 C655 C510 C611 C582 C509 C559 C506 C561
0.1uF 20% 10V CERM 402

SDRAM DECOUPLING (35 0.1UF CAPS)

+3V_MAIN

C410 C395 C579 C581 2.2uF N20P80% 16V CERM 805

C619 C700 C681 C652 C677 C666 C624 C701
C663 C683 C682 C639 C714 C715 C717 C627 C648
C702 C722 C649 C704 C678 C620 C625 C703 C664
C626 C640 C716 C679 C665 C641 C651 C650 C653
0.1uF 20% 10V CERM 402

PCI DECOUPLING (9 0.1UF CAPS)

C712 C713 C642 C628 C610 C577 C578 C576 C680
0.1uF 20% 10V CERM 402

1394/ETHERNET DECOUPLING (29 0.1UF CAPS)

C317 C333 C266 C299 C718 C265
C291 C297 C396 C296 C349 C380 C332 C348
C350 C548 C255 C246 C290 C456 C298 C457
C229 C247 C549 C318 C245 C609 C334
0.1uF 20% 10V CERM 402

UNI-N BYPASSING

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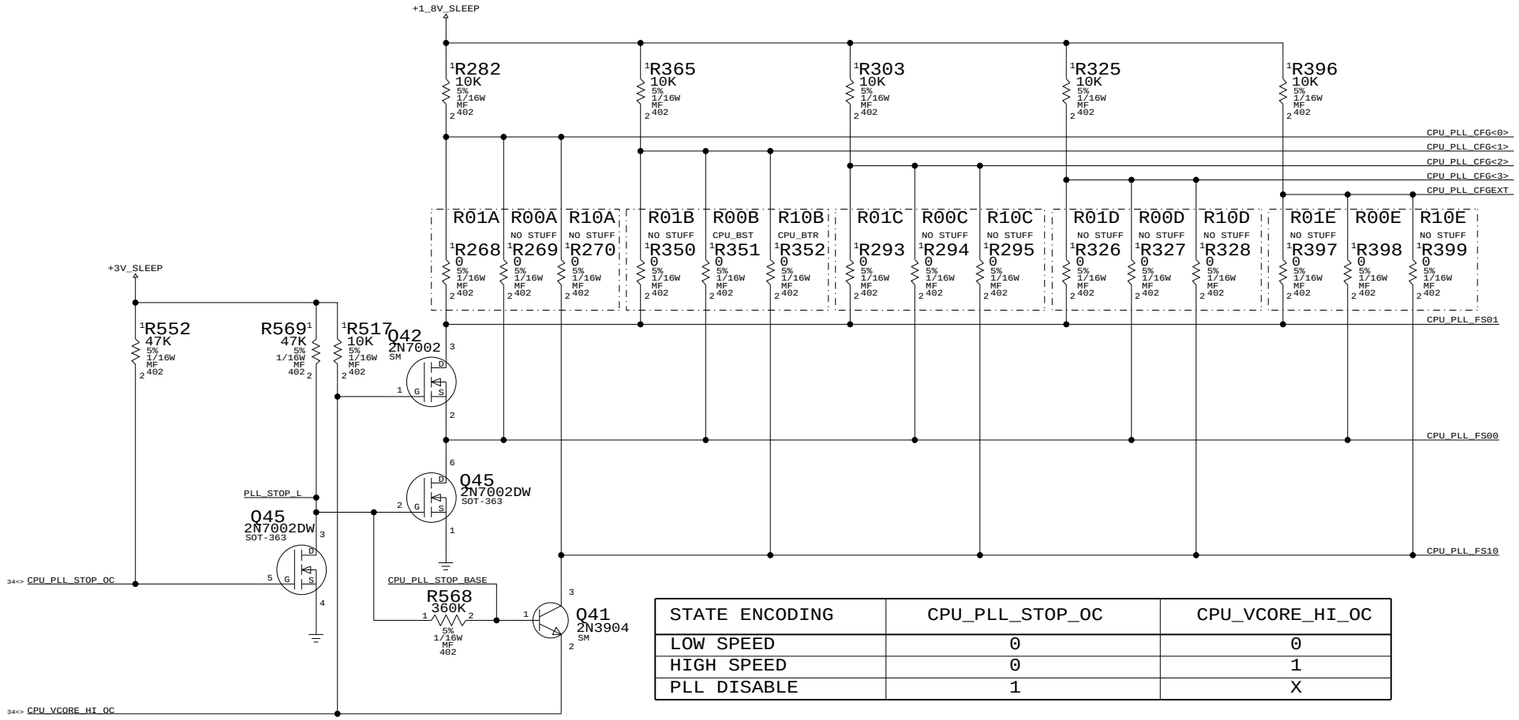
APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6403 | REV. E

SCALE NONE | SHT 11 OF 46

CPU PLL CONFIG CIRCUITRY



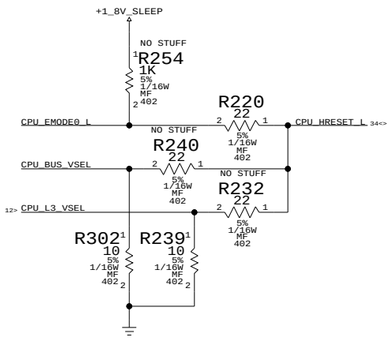
STATE ENCODING	CPU_PLL_STOP_OC	CPU_VCORE_HI_OC
LOW SPEED	0	0
HIGH SPEED	0	1
PLL DISABLE	1	X

CPU FREQUENCY CONFIGURATION

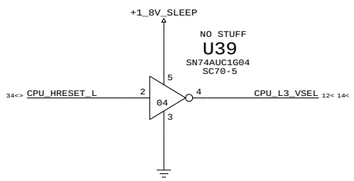
MULTIPLIER	CORE FREQUENCY (AT BUS FREQUENCY) 100MHZ	133MHZ	CPU_PLL_CFG	
(Bus-to-Core)	(MHZ)		E	ABCD HEX
0.0X	PLL OFF		0	1111 0F
0.5X	50	67	0	0000 00
1.0X	PLL BYPASS		0	0011 03
2.0X	200	267	0	0100 04
2.5X	250	333	0	0110 06
3.0X	300	400	0	1000 08
3.5X	350	467	0	1110 0E
4.0X	400	533	0	1010 0A
4.5X	450	600	0	0111 07
5.0X	500	667	0	1011 0B
5.5X	550	733	0	1001 09
6.0X	600	800	0	1101 0D
6.5X	650	867	0	0101 05
7.0X	700	933	0	0010 02
7.5X	750	1000	0	0001 01
8.0X	800	1067	0	1100 0C
9.0X	900	1200	1	0111 17
10.0X	1000	1333	1	1010 1A
11.0X	1100	1467	1	1001 19
12.0X	1200	1600	1	1011 1B
13.0X	1300	1733	1	0101 15
14.0X	1400	1867	1	1100 1C
15.0X	1500	2000	1	0001 11
16.0X	1600	2133	1	1101 1D

CPU CONFIGURATION

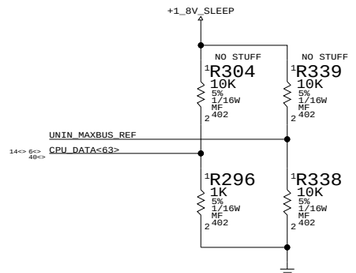
SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL (PROCESSOR)	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
CPU_L3_VSEL (PROCESSOR)	CPU_HRESET_L or INT. PU	2.5V INTERFACE
	LOW	1.8V INTERFACE



Inverter Gate placement for 1.5V L3 bus interface setting



UNIN CPU BUS CONFIGURATION



SIGNAL	TIED	APPLICATION
CPU_DATA<63> (UNIN)	HIGH	60X BUS MODE
	LOW	MAX BUS MODE
UNIN_MAXBUS_REF (UNIN)	HIGH	2.5V INTERFACE
	LOW	1.8V INTERFACE

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CPU CONFIGURATION

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6403	E
SCALE: NONE	SHT 12 OF 46	

CPU_VCORE DECOUPLING NETWORK

39< 13< 43> CPU_VCORE_SLEEP

R394 470 5% 1/16W MF 402

C441 10uF 20% 6.3V CERM 805
C535 10uF 20% 6.3V CERM 805
C573 2.2uF N20P80% 16V CERM 805
C572 2.2uF N20P80% 16V CERM 805
C864 10uF 20% 6.3V CERM 805
C865 10uF 20% 6.3V CERM 805

C443 0.1uF 20% 10V CERM 402
C536 0.1uF 20% 10V CERM 402
C492 0.1uF 20% 10V CERM 402
C444 0.1uF 20% 10V CERM 402
C538 0.1uF 20% 10V CERM 402
C490 0.1uF 20% 10V CERM 402
C537 0.1uF 20% 10V CERM 402
C539 0.1uF 20% 10V CERM 402
C493 0.1uF 20% 10V CERM 402
C442 0.1uF 20% 10V CERM 402
C491 0.1uF 20% 10V CERM 402
C445 0.1uF 20% 10V CERM 402

CPU_OVDD DECOUPLING NETWORK

+1_8V_SLEEP

R438 470 5% 1/16W MF 402

C622 0.1uF 20% 10V CERM 402
C284 0.1uF 20% 10V CERM 402
C632 0.1uF 20% 10V CERM 402
C593 0.1uF 20% 10V CERM 402
C358 0.1uF 20% 10V CERM 402
C394 0.1uF 20% 10V CERM 402
C601 0.1uF 20% 10V CERM 402
C603 0.1uF 20% 10V CERM 402
C602 0.1uF 20% 10V CERM 402
C631 0.1uF 20% 10V CERM 402
C446 0.1uF 20% 10V CERM 402
C347 0.1uF 20% 10V CERM 402

VDD

OVDD

CPU INTERNAL PLL FILTERING

CPU_VCORE_SLEEP 13< 43>

R221 10 5% 1/16W MF 402

43> CPU_AVDD

C315 0.1uF 20% 10V CERM 402
C295 2.2uF N20P80% 16V CERM 805

OMIT

U10

SCVger

CBGA-483

(1 OF 3)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S2635	1	IC,APOLLO,NODE 5,867MHZ,1.3V CORE,85C	U10	CRITICAL	CPU_BTR
337S2636	1	IC,APOLLO,NODE 5,1GHZ,1.3V CORE,85C	U10	CRITICAL	CPU_BST

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
337S2715	337S2635	CPU_BTR	U10	N5R3.3
337S2716	337S2636	CPU_BST	U10	N5R3.3
337S2827	337S2636	CPU_BST	U10	N5R3.3

6<	CPU_BR_L	K1 BR
6< 40<> 6>	CPU_BG_L	R3 BG
NC		F2 HPR
6< 40<> 6>	CPU_TS_L	P5 TS
13<	CPU_PULLDOWN	E10 A0
		N4 A1
		E8 A2
		N5 A3
40<> 6>	CPU_ADDR<0>	C8 A4
40<> 6>	CPU_ADDR<1>	R2 A5
40<> 6>	CPU_ADDR<2>	A7 A6
40<> 6>	CPU_ADDR<3>	M2 A7
40<> 6>	CPU_ADDR<4>	A6 A8
40<> 6>	CPU_ADDR<5>	M1 A9
40<> 6>	CPU_ADDR<6>	A10 A10
40<> 6>	CPU_ADDR<7>	U2 A11
40<> 6>	CPU_ADDR<8>	N2 A12
40<> 6>	CPU_ADDR<9>	P8 A13
40<> 6>	CPU_ADDR<10>	M8 A14
40<> 6>	CPU_ADDR<11>	W4 A15
40<> 6>	CPU_ADDR<12>	N6 A16
40<> 6>	CPU_ADDR<13>	U6 A17
40<> 6>	CPU_ADDR<14>	R5 A18
40<> 6>	CPU_ADDR<15>	Y4 A19
40<> 6>	CPU_ADDR<16>	P1 A20
40<> 6>	CPU_ADDR<17>	P4 A21
40<> 6>	CPU_ADDR<18>	R6 A22
40<> 6>	CPU_ADDR<19>	M7 A23
40<> 6>	CPU_ADDR<20>	N7 A24
40<> 6>	CPU_ADDR<21>	AA3 A25
40<> 6>	CPU_ADDR<22>	U4 A26
40<> 6>	CPU_ADDR<23>	W2 A27
40<> 6>	CPU_ADDR<24>	W1 A28
40<> 6>	CPU_ADDR<25>	W3 A29
40<> 6>	CPU_ADDR<26>	V4 A30
40<> 6>	CPU_ADDR<27>	AA1 A31
40<> 6>	CPU_ADDR<28>	D10 A32
40<> 6>	CPU_ADDR<29>	J4 A33
40<> 6>	CPU_ADDR<30>	G10 A34
40<> 6>	CPU_ADDR<31>	D9 A35
NC		L5 AP0
NC		L6 AP1
NC		J1 AP2
NC		H2 AP3
NC		G5 AP4
40<> 6>	CPU_TT<0>	F1 TT0
40<> 6>	CPU_TT<1>	F4 TT1
40<> 6>	CPU_TT<2>	K8 TT2
40<> 6>	CPU_TT<3>	A5 TT3
40<> 6>	CPU_TT<4>	E1 TT4
40<> 6>	CPU_TBST_L	B7 TBST
40<> 6>	CPU_TSIZ<0>	L1 TSIZ0
40<> 6>	CPU_TSIZ<1>	H3 TSIZ1
40<> 6>	CPU_TSIZ<2>	D1 TSIZ2
40<> 6>	CPU_GBL_L	M4 GBL
40<> 6>	CPU_WT_L	L2 WT
40<> 6>	CPU_CI_L	R1 CI
40<> 6>	CPU_AACK_L	U1 AACK
6< 40<> 6>	CPU_ARTRY_L	T2 ARTRY
13<	CPU_SHD0_L	L4 SHD0
13<	CPU_SHD1_L	L8 SHD1
6<	CPU_HIT_0_L	K2 HIT

GND

AVDD	G6	CPU_BUS_VSEL
BVSEL	D6	SYSCLK_CPU 40<
SYSCLK	N1	CPU_CLKOUT_SPN
CLK_OUT	A2	CPU_PLL_CFG<0>
PLL_CFG0	F7	CPU_PLL_CFG<1>
PLL_CFG1	C2	CPU_PLL_CFG<2>
PLL_CFG2	D4	CPU_PLL_CFG<3>
PLL_CFG3	H8	CPU_PLL_CFGEXT
PLL_CFG4	V1	CPU_DBG_L 6> 40<>
DBG	T6	CPU_DRDY_0_L_UF
DRDY	P2	CPU_EDTI
DTI0	T5	CPU_DTI<0> 6> 40<>
DTI1	U3	CPU_DTI<1> 6> 40<>
DTI2	P6	CPU_DTI<2> 6> 40<>
DTI3	E4	JTAG_CPU_TDI
TDI	H1	JTAG_CPU_TDO_TP
TDO	K4	JTAG_CPU_TMS
TMS	J7	JTAG_CPU_TCK
TCK	C1	JTAG_CPU_RST_L
TRST	F6	CPU_LSSD_MODE
LSSD_MODE	H4	CPU_L1TSTCLK
L1_TSTCLK	J2	CPU_L2TSTCLK
L2_TSTCLK	N8	CPU_TA_L 6> 40<>
TA	T1	CPU_TEA_L 6> 40<>
TEA	L3	CPU_TBEN
TBEN	Y1	CPU_QREQ_L 6<
QREQ	K7	CPU_QACK_L 6> 40<>
QACK	F3	
CKSTP_IN	K6	CHKSTP_OUT_L 13<
CKSTP_OUT	B10	CPU_CHKS_L
CHKS	J6	MPIC_CPU_INT_L 16>
INT	G8	CPU_SMI_L 34<>
SMI	B8	CPU_MCP_L
MCP	G1	CPU_SRESET_L 16<>
SRESET	A3	CPU_HRESET_L 34<>
HRESET	E6	CPU_PMONIN_L 16<>
PMON_IN	B4	NC
PMON_OUT	C6	CPU_EMODE0_L
BMODE0	C4	CPU_EMODE1_L
BMODE1	A9	CPU_PULLDOWN 13<>
DX	B9	
EXT_QUAL	H6	CPU_PULLUP
IARTRY0	H10	
IARTRY1	B6	NC
OSHD	D8	CPU_SRWX_L
SRW0	F9	
SRW1	F8	
WAIT	A8	NC
SPARE0	D3	NC
SPARE1	W9	NC
SPARE2	J8	NC
SPARE3	A11	NC
NC1	B11	NC
NC2	C11	NC
NC3	D5	NC
NC4	D11	NC
NC5	E7	NC
NC6	E11	NC
NC7	F11	NC
NC8	G2	NC
NC9	G11	NC
NC10	H11	NC
NC11		

RC glitch filter

R700 33 5% 1/16W MF 402

C878 22pF 5% 50V CERM 603

CPU_DRDY_0_L

MPC7455 PULL-UPS

+1_8V_SLEEP

CPU_TBEN	R353	1K
CPU_CHKS_L	R252	10K
13< CPU_SHD0_L	RP2	10K
13< CPU_SHD1_L	R349	10K
CPU_MCP_L	R253	10K
CPU_LSSD_MODE	R292	10K
CPU_L2TSTCLK	RP2	10K
13< CHKSTP_OUT_L	R271	1K
CPU_SRWX_L	R291	10K
16< CPU_PMONIN_L	R281	10K
CPU_EMODE1_L	R267	10K
CPU_PULLUP	R313	1K
34< CPU_HRESET_L	R416	10K
16< CPU_SRESET_L	RP1	10K
16< MPIC_CPU_INT_L	RP1	10K
34< CPU_SMI_L	R301	10K
JTAG_CPU_TDI	RP1	10K
JTAG_CPU_TMS	R329	10K
JTAG_CPU_TCK	R324	10K
JTAG_CPU_RST_L	R255	200
CPU_L1TSTCLK	RP1	10K
CPU_EDTI	R400	10K
13<> CPU_PULLDOWN	R395	470

All: 5% 1/16W MF 402 (SM1 for RP parts)

MPC7455 MAXBUS

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D	051-6403	E

SCALE NONE

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S1074	1	RES,1/16W,10.7K OHM,0402,SMD	R698	1415_L3_GVDD
114S6343	1	RES,1/16W,6.34K OHM,0402,SMD	R698	1325_L3_GVDD
114S7503	1	RES,1/16W,7.5K OHM,0402,SMD	R698	1352_L3_GVDD

OMIT
U10
SCVger
CBGA-483
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40<> 6<> CPU_DATA<0>	AB15	D0
40<> 6<> CPU_DATA<1>	T14	D1
40<> 6<> CPU_DATA<2>	R14	D2
40<> 6<> CPU_DATA<3>	AB13	D3
40<> 6<> CPU_DATA<4>	V14	D4
40<> 6<> CPU_DATA<5>	U14	D5
40<> 6<> CPU_DATA<6>	AB14	D6
40<> 6<> CPU_DATA<7>	W16	D7
40<> 6<> CPU_DATA<8>	AA11	D8
40<> 6<> CPU_DATA<9>	Y11	D9
40<> 6<> CPU_DATA<10>	U12	D10
40<> 6<> CPU_DATA<11>	W13	D11
40<> 6<> CPU_DATA<12>	Y14	D12
40<> 6<> CPU_DATA<13>	U13	D13
40<> 6<> CPU_DATA<14>	T12	D14
40<> 6<> CPU_DATA<15>	W12	D15
40<> 6<> CPU_DATA<16>	AB12	D16
40<> 6<> CPU_DATA<17>	R12	D17
40<> 6<> CPU_DATA<18>	AA13	D18
40<> 6<> CPU_DATA<19>	AB11	D19
40<> 6<> CPU_DATA<20>	Y12	D20
40<> 6<> CPU_DATA<21>	V11	D21
40<> 6<> CPU_DATA<22>	T11	D22
40<> 6<> CPU_DATA<23>	R11	D23
40<> 6<> CPU_DATA<24>	W10	D24
40<> 6<> CPU_DATA<25>	T10	D25
40<> 6<> CPU_DATA<26>	W11	D26
40<> 6<> CPU_DATA<27>	V10	D27
40<> 6<> CPU_DATA<28>	R10	D28
40<> 6<> CPU_DATA<29>	U10	D29
40<> 6<> CPU_DATA<30>	AA10	D30
40<> 6<> CPU_DATA<31>	U9	D31
40<> 6<> CPU_DATA<32>	V7	D32
40<> 6<> CPU_DATA<33>	T8	D33
40<> 6<> CPU_DATA<34>	AB4	D34
40<> 6<> CPU_DATA<35>	Y6	D35
40<> 6<> CPU_DATA<36>	AB7	D36
40<> 6<> CPU_DATA<37>	AA6	D37
40<> 6<> CPU_DATA<38>	Y8	D38
40<> 6<> CPU_DATA<39>	AA7	D39
40<> 6<> CPU_DATA<40>	W8	D40
40<> 6<> CPU_DATA<41>	AB10	D41
40<> 6<> CPU_DATA<42>	AA16	D42
40<> 6<> CPU_DATA<43>	AB16	D43
40<> 6<> CPU_DATA<44>	AB17	D44
40<> 6<> CPU_DATA<45>	Y18	D45
40<> 6<> CPU_DATA<46>	AB18	D46
40<> 6<> CPU_DATA<47>	Y16	D47
40<> 6<> CPU_DATA<48>	AA18	D48
40<> 6<> CPU_DATA<49>	W14	D49
40<> 6<> CPU_DATA<50>	R13	D50
40<> 6<> CPU_DATA<51>	W15	D51
40<> 6<> CPU_DATA<52>	AA14	D52
40<> 6<> CPU_DATA<53>	V16	D53
40<> 6<> CPU_DATA<54>	W6	D54
40<> 6<> CPU_DATA<55>	AA12	D55
40<> 6<> CPU_DATA<56>	V6	D56
40<> 6<> CPU_DATA<57>	AB9	D57
40<> 6<> CPU_DATA<58>	AB6	D58
40<> 6<> CPU_DATA<59>	R7	D59
40<> 6<> CPU_DATA<60>	R9	D60
40<> 6<> CPU_DATA<61>	AA9	D61
40<> 6<> CPU_DATA<62>	AB8	D62
12< 40<> 6<> CPU_DATA<63>	W9	D63
NC	AA2	DP0
NC	AB3	DP1
NC	AB2	DP2
NC	AA8	DP3
NC	R8	DP4
NC	W5	DP5
NC	U8	DP6
NC	AB5	DP7

15< 14< 43<> 14<> +1_5V_L3_VDDQ_SLEEP

B13 B15 B17 B19 B21 D12 D14 D16 D18 D21 E19 F13 F15 F17 F21 G19 H12 H14 H17 H21 J19 J17 K13 K21 L19 M17 M21 N19 P17 P21 R19 T17 T21 V19 V17 V21 W19 Y21

L3OVDD

OMIT
U10
SCVger
CBGA-483
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15< 41<> L3_ADDR<0>	L18	L3A0
15< 41<> L3_ADDR<1>	K22	L3A1
15< 41<> L3_ADDR<2>	L16	L3A2
15< 41<> L3_ADDR<3>	K20	L3A3
15< 41<> L3_ADDR<4>	K18	L3A4
15< 41<> L3_ADDR<5>	J22	L3A5
15< 41<> L3_ADDR<6>	J20	L3A6
15< 41<> L3_ADDR<7>	H22	L3A7
15< 41<> L3_ADDR<8>	J18	L3A8
15< 41<> L3_ADDR<9>	K16	L3A9
15< 41<> L3_ADDR<10>	H20	L3A10
15< 41<> L3_ADDR<11>	G22	L3A11
15< 41<> L3_ADDR<12>	F22	L3A12
15< 41<> L3_ADDR<13>	G20	L3A13
15< 41<> L3_ADDR<14>	H18	L3A14
15< 41<> L3_ADDR<15>	E22	L3A15
15< 41<> L3_ADDR<16>	J16	L3A16
15< 41<> L3_ADDR<17>	F20	L3A17
41<> 15<> L3_DATA<0>	AA19	L3D0
41<> 15<> L3_DATA<1>	AB20	L3D1
41<> 15<> L3_DATA<2>	U16	L3D2
41<> 15<> L3_DATA<3>	W18	L3D3
41<> 15<> L3_DATA<4>	AA20	L3D4
41<> 15<> L3_DATA<5>	AB21	L3D5
41<> 15<> L3_DATA<6>	AA21	L3D6
41<> 15<> L3_DATA<7>	T16	L3D7
41<> 15<> L3_DATA<8>	W20	L3D8
41<> 15<> L3_DATA<9>	U18	L3D9
41<> 15<> L3_DATA<10>	Y22	L3D10
41<> 15<> L3_DATA<11>	R16	L3D11
41<> 15<> L3_DATA<12>	V20	L3D12
41<> 15<> L3_DATA<13>	W22	L3D13
41<> 15<> L3_DATA<14>	T18	L3D14
41<> 15<> L3_DATA<15>	U20	L3D15
41<> 15<> L3_DATA<16>	N18	L3D16
41<> 15<> L3_DATA<17>	N20	L3D17
41<> 15<> L3_DATA<18>	N16	L3D18
41<> 15<> L3_DATA<19>	N22	L3D19
41<> 15<> L3_DATA<20>	M16	L3D20
41<> 15<> L3_DATA<21>	M18	L3D21
41<> 15<> L3_DATA<22>	M20	L3D22
41<> 15<> L3_DATA<23>	M22	L3D23
41<> 15<> L3_DATA<24>	R18	L3D24
41<> 15<> L3_DATA<25>	T20	L3D25
41<> 15<> L3_DATA<26>	U22	L3D26
41<> 15<> L3_DATA<27>	T22	L3D27
41<> 15<> L3_DATA<28>	R20	L3D28
41<> 15<> L3_DATA<29>	P18	L3D29
41<> 15<> L3_DATA<30>	R22	L3D30
41<> 15<> L3_DATA<31>	M15	L3D31
41<> 15<> L3_DATA<32>	G18	L3D32
41<> 15<> L3_DATA<33>	D22	L3D33
41<> 15<> L3_DATA<34>	E20	L3D34
41<> 15<> L3_DATA<35>	H16	L3D35
41<> 15<> L3_DATA<36>	C22	L3D36
41<> 15<> L3_DATA<37>	F18	L3D37
41<> 15<> L3_DATA<38>	D20	L3D38
41<> 15<> L3_DATA<39>	B22	L3D39
41<> 15<> L3_DATA<40>	G16	L3D40
41<> 15<> L3_DATA<41>	A21	L3D41
41<> 15<> L3_DATA<42>	G15	L3D42
41<> 15<> L3_DATA<43>	E17	L3D43
41<> 15<> L3_DATA<44>	A20	L3D44
41<> 15<> L3_DATA<45>	C19	L3D45
41<> 15<> L3_DATA<46>	C18	L3D46
41<> 15<> L3_DATA<47>	A19	L3D47
41<> 15<> L3_DATA<48>	A18	L3D48
41<> 15<> L3_DATA<49>	G14	L3D49
41<> 15<> L3_DATA<50>	E15	L3D50
41<> 15<> L3_DATA<51>	C16	L3D51
41<> 15<> L3_DATA<52>	A17	L3D52
41<> 15<> L3_DATA<53>	A16	L3D53
41<> 15<> L3_DATA<54>	C15	L3D54
41<> 15<> L3_DATA<55>	G13	L3D55
41<> 15<> L3_DATA<56>	C14	L3D56
41<> 15<> L3_DATA<57>	A14	L3D57
41<> 15<> L3_DATA<58>	E13	L3D58
41<> 15<> L3_DATA<59>	C13	L3D59
41<> 15<> L3_DATA<60>	G12	L3D60
41<> 15<> L3_DATA<61>	A13	L3D61
41<> 15<> L3_DATA<62>	E12	L3D62
41<> 15<> L3_DATA<63>	C12	L3D63
NC	AB19	L3DP0
NC	AA22	L3DP1
NC	P22	L3DP2
NC	P16	L3DP3
NC	C20	L3DP4
NC	E16	L3DP5
NC	A15	L3DP6
NC	A12	L3DP7

GND

A22 B12 B14 B18 B20 B8 C2 C11 D3 D10 D13 D17 D19 E2 E12 F3 F14 F19 F4 G21 G3 H13 H15 H19 H7 J11 J21 K19 L3 L11 L13 M19 N7 N12 N14 N9 P13 R3 R21 T15 T19 T9 U1 U19 V4 W17 W21 AB22

L3 I/O LDO Regulator

+2_5V_SLEEP
NO STUFF
R696 0 5% 1/16W MF 603
+1_8V_SLEEP
R697 0 5% 1/16W MF 603
L3_RC C875 1uF 20% 10V CERM 805
43<> +LT1962_SLEEP
L3_RC R702 0 5% 1/16W MF 402
LT1962_SHDN_L
NO_L3_RC R701 0 5% 1/16W MF 603
L3_RC U62 LT1962-ADJ MSOP
IN OUT NC NC NC ADJ BYP SHDN GND
LT1962_ADJ
LT1962_BYPASS
L3_RC C876 0.01uF 20% 10V CERM 402
OMIT R698 10.7K 1% 1/16W MF 402
L3_RC R699 68.1K 1% 1/16W MF 402
+1_5V_L3_VDDQ_SLEEP 14<> 43<> 14<> 15<
KEEP CLOSE TO REGULATOR
L3_RC C877 10uF 20% 6.3V CERM 805

NOTE: This rail is now positioned at 1.41V spscifically for PS9 processors. L3 GVDD will need to be re-evaluated for each project.

CPU L3 I/O Decoupling

Place 1 each near pins B15, D12, E19, F15, H17, K17, M19, R15, T17, V21 of processor

L3VSEL	A4	CPU_L3_VSEL	12>
L3CLK0	V22	L3_CLK<0>	40<> 15<
L3CLK1	C17	L3_CLK<1>	40<> 15<
L3CNTL0*	L20	L3_CNTL<0>	41<> 15<
L3CNTL1*	L22	L3_CNTL<1>	41<> 15<
L3ECHO_CLK0	V18	L3_ECHO_CLK<0>	15<> 40<>
L3ECHO_CLK1	P20	L3_ECHO_CLK<1>	15<> 40<>
L3ECHO_CLK2	E18	L3_ECHO_CLK<2>	15<> 40<>
L3ECHO_CLK3	E14	L3_ECHO_CLK<3>	15<> 40<>

43<> 14<> +1_5V_L3_VDDQ_SLEEP

C879 C880 C881 C882
C883 C884 C885 C886
C887 C888
0.1uF 20% 10V CERM 402

Additional CPU L3 I/O Decoupling

43<> 14<> +1_5V_L3_VDDQ_SLEEP

C50 C220 C321 C367
C187 C305 C322 C384
C219 C306 C366 C385
0.001uF 20% 50V CERM 402
10uF 20% 6.3V CERM 805

MPC7455 DATA/L3

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6403	E
SCALE: NONE	SHT 14 OF 46	

+2_5V_SLEEP
L3_RC R31 0 5% 1/16W MF 603 L3_VDD_SLEEP 43<>

L3_RC RP24 10K 5% 1/32W 25V SM
5 10
L3_DQPA<0> 15<>
L3_DQPB<0> 15<>
L3_DQPC<0> 15<>
L3_DQPD<0> 15<>
L3_DQPA<1> 15<>
L3_DQPB<1> 15<>
L3_DQPC<1> 15<>
L3_DQPD<1> 15<>

L3_RC R312 470 5% 1/16W MF 402 L3_PULLDOWN<0>
L3_RC R280 470 5% 1/16W MF 402 L3_PULLDOWN<1>
L3_RC R231 1K 5% 1/16W MF 402 JTAG_L3_TCK

Addr lines swappable within a SRAM (except ADDR<0..1>)

43<> L3_VDD_SLEEP
+1_5V_L3_VDDQ_SLEEP 14<> 43<>
VDD VDDQ

OMIT
U42
TEMPLATE
SRAM_DDR_153PBGA
PBGA

41<> 14<> L3_ADDR<0> 5T A0
L3_ADDR<1> 5R A1
L3_ADDR<6> 6R A2
L3_ADDR<12> 4R A3
L3_ADDR<10> 3T A4
L3_ADDR<2> 3A A5
L3_ADDR<11> 3C A6
L3_ADDR<13> 4A A7
L3_ADDR<4> 7C A8
L3_ADDR<7> 4C A9
L3_ADDR<5> 6C A10
L3_ADDR<9> 6A A11
L3_ADDR<3> 7P A12
L3_ADDR<14> 7T A13
L3_ADDR<8> 7A A14
L3_ADDR<15> 3B A15
L3_ADDR<16> 7B A16
L3_ADDR<17> 7D A17
L3_PULLDOWN<0> 3D A18
L3_PULLDOWN<0> 3P A19
40<> 14<> L3_CLK<0> 5G CK
L3_CLK_REF 5H CK*

L3_PULLDOWN<0> 5C G*
L3_PULLDOWN<0> 4L LBO*

41<> 14<> L3_CNTL<0> 5B B1*
41<> 14<> L3_CNTL<1> 5K B2*
5E VREF
L3_VREF 5N VREF
L3_ZQ<0> 5A ZQ

L3_RC R473 249 1% 1/16W MF 402

JTAG_L3_TMS 3U TMS
JTAG_L3_TDI_TP 4U TDI
15< JTAG_L3_SRAM2_TDI 6U TDO
JTAG_L3_TCK 5U TCK

Data lines swappable within a SRAM

9T L3_DATA<23> 14<> 41<>
8T L3_DATA<31> 14<> 41<>
9P L3_DATA<17> 14<> 41<>
8P L3_DATA<22> 14<> 41<>
9M L3_DATA<19> 14<> 41<>
9K L3_DATA<25> 14<> 41<>
8K L3_DATA<27> 14<> 41<>
7K L3_DATA<30> 14<> 41<>
9B L3_DATA<1> 14<> 41<>
8B L3_DATA<0> 14<> 41<>
9D L3_DATA<5> 14<> 41<>
8D L3_DATA<4> 14<> 41<>
9F L3_DATA<6> 14<> 41<>
9H L3_DATA<12> 14<> 41<>
8H L3_DATA<26> 14<> 41<>
7H L3_DATA<15> 14<> 41<>
1B L3_DATA<3> 14<> 41<>
2B L3_DATA<10> 14<> 41<>
1D L3_DATA<8> 14<> 41<>
2D L3_DATA<13> 14<> 41<>
1F L3_DATA<2> 14<> 41<>
1H L3_DATA<14> 14<> 41<>
2H L3_DATA<7> 14<> 41<>
3H L3_DATA<9> 14<> 41<>
1T L3_DATA<18> 14<> 41<>
2T L3_DATA<20> 14<> 41<>
1P L3_DATA<21> 14<> 41<>
2P L3_DATA<16> 14<> 41<>
1M L3_DATA<29> 14<> 41<>
1K L3_DATA<11> 14<> 41<>
2K L3_DATA<24> 14<> 41<>
3K L3_DATA<28> 14<> 41<>

7M L3_DQPA<0> 15<>
7F L3_DQPB<0> 15<>
3F L3_DQPC<0> 15<>
3M L3_DQPD<0> 15<>

2F L3_ECHO_CLK<0> 40<> 14<>
6M NC
8F L3_ECHO_CLK<1> 40<> 14<>
2M NC

5L L3_PULLDOWN<0>
6L NC
7U NC

43<> L3_VDD_SLEEP
+1_5V_L3_VDDQ_SLEEP 14<> 43<>
VDD VDDQ

OMIT
U11
TEMPLATE
SRAM_DDR_153PBGA
PBGA

41<> 14<> L3_ADDR<0> 5T A0
L3_ADDR<1> 5R A1
L3_ADDR<3> 6R A2
L3_ADDR<6> 4R A3
L3_ADDR<14> 3T A4
L3_ADDR<8> 3A A5
L3_ADDR<11> 3C A6
L3_ADDR<9> 4A A7
L3_ADDR<4> 7C A8
L3_ADDR<5> 4C A9
L3_ADDR<7> 6C A10
L3_ADDR<13> 6A A11
L3_ADDR<12> 7P A12
L3_ADDR<10> 7T A13
L3_ADDR<2> 7A A14
L3_ADDR<15> 3B A15
L3_ADDR<16> 7B A16
L3_ADDR<17> 7D A17
L3_PULLDOWN<1> 3D A18
L3_PULLDOWN<1> 3P A19
40<> 14<> L3_CLK<1> 5G CK
L3_CLK_REF 5H CK*

L3_PULLDOWN<1> 5C G*
L3_PULLDOWN<1> 4L LBO*

41<> 14<> L3_CNTL<0> 5B B1*
41<> 14<> L3_CNTL<1> 5K B2*
5E VREF
L3_VREF 5N VREF
L3_ZQ<1> 5A ZQ

L3_RC R472 249 1% 1/16W MF 402

JTAG_L3_TMS 3U TMS
15< JTAG_L3_SRAM2_TDI 4U TDI
JTAG_L3_TDO_TP 6U TDO
JTAG_L3_TCK 5U TCK

Data lines swappable within a SRAM

9T L3_DATA<54> 14<> 41<>
8T L3_DATA<39> 14<> 41<>
9P L3_DATA<46> 14<> 41<>
8P L3_DATA<51> 14<> 41<>
9M L3_DATA<36> 14<> 41<>
9K L3_DATA<58> 14<> 41<>
8K L3_DATA<62> 14<> 41<>
7K L3_DATA<45> 14<> 41<>
9B L3_DATA<60> 14<> 41<>
8B L3_DATA<55> 14<> 41<>
9D L3_DATA<35> 14<> 41<>
8D L3_DATA<49> 14<> 41<>
9F L3_DATA<42> 14<> 41<>
9H L3_DATA<50> 14<> 41<>
8H L3_DATA<34> 14<> 41<>
7H L3_DATA<38> 14<> 41<>
1B L3_DATA<32> 14<> 41<>
2B L3_DATA<40> 14<> 41<>
1D L3_DATA<43> 14<> 41<>
2D L3_DATA<37> 14<> 41<>
1F L3_DATA<56> 14<> 41<>
1H L3_DATA<41> 14<> 41<>
2H L3_DATA<59> 14<> 41<>
3H L3_DATA<33> 14<> 41<>
1T L3_DATA<61> 14<> 41<>
2T L3_DATA<57> 14<> 41<>
1P L3_DATA<53> 14<> 41<>
2P L3_DATA<52> 14<> 41<>
1M L3_DATA<48> 14<> 41<>
1K L3_DATA<47> 14<> 41<>
2K L3_DATA<44> 14<> 41<>
3K L3_DATA<63> 14<> 41<>

7M L3_DQPA<1> 15<>
7F L3_DQPB<1> 15<>
3F L3_DQPC<1> 15<>
3M L3_DQPD<1> 15<>

2F L3_ECHO_CLK<2> 40<> 14<>
6M NC
8F L3_ECHO_CLK<3> 40<> 14<>
2M NC

5L L3_PULLDOWN<1>
6L NC
7U NC

43<> 14<> +1_5V_L3_VDDQ_SLEEP

L3_RC R418 1K 1% 1/16W MF 402
L3_RC R311 1K 1% 1/16W MF 402

L3_VREF
L3_RC R428 1K 1% 1/16W MF 402
L3_RC C599 0.1uF 20% 10V CERM 402

L3_CLK_REF
L3_RC R290 1K 1% 1/16W MF 402
L3_RC C393 0.1uF 20% 10V CERM 402

Split caps of same value evenly between SRAM chips

43<> L3_VDD_SLEEP
L3_RC C440 0.1uF 20% 10V CERM 402
L3_RC C424 0.1uF 20% 10V CERM 402
L3_RC C532 0.1uF 20% 10V CERM 402
L3_RC C616 0.1uF 20% 10V CERM 402
L3_RC C327 0.1uF 20% 10V CERM 402
L3_RC C51 0.1uF 20% 10V CERM 402
L3_RC C53 0.1uF 20% 10V CERM 402
L3_RC C60 0.1uF 20% 10V CERM 402
L3_RC C276 0.1uF 20% 10V CERM 402
L3_RC C672 0.1uF 20% 10V CERM 402

Split caps of same value evenly between SRAM chips

43<> L3_VDD_SLEEP
L3_RC C263 10uF 20% 6.3V CERM 805
L3_RC C689 10uF 20% 6.3V CERM 805
L3_RC C17 2.2uF N20P80% 16V CERM 805
L3_RC C690 2.2uF N20P80% 16V CERM 805

Split caps of same value evenly between SRAM chips

43<> 14<> +1_5V_L3_VDDQ_SLEEP
L3_RC C44 0.1uF 20% 10V CERM 402
L3_RC C571 0.1uF 20% 10V CERM 402
L3_RC C630 0.1uF 20% 10V CERM 402
L3_RC C671 0.1uF 20% 10V CERM 402
L3_RC C40 0.1uF 20% 10V CERM 402
L3_RC C533 0.1uF 20% 10V CERM 402
L3_RC C676 0.1uF 20% 10V CERM 402
L3_RC C673 0.1uF 20% 10V CERM 402
L3_RC C314 0.1uF 20% 10V CERM 402
L3_RC C617 0.1uF 20% 10V CERM 402
L3_RC C439 0.1uF 20% 10V CERM 402
L3_RC C675 0.1uF 20% 10V CERM 402
L3_RC C674 0.1uF 20% 10V CERM 402
L3_RC C489 0.1uF 20% 10V CERM 402
L3_RC C277 0.1uF 20% 10V CERM 402
L3_RC C346 0.1uF 20% 10V CERM 402
L3_RC C556 0.1uF 20% 10V CERM 402
L3_RC C621 0.1uF 20% 10V CERM 402
L3_RC C280 0.1uF 20% 10V CERM 402
L3_RC C275 0.1uF 20% 10V CERM 402

Split caps of same value evenly between SRAM chips

43<> 14<> +1_5V_L3_VDDQ_SLEEP
L3_RC C262 10uF 20% 6.3V CERM 805
L3_RC C688 10uF 20% 6.3V CERM 805
L3_RC C687 2.2uF N20P80% 16V CERM 805
L3_RC C18 2.2uF N20P80% 16V CERM 805

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0009	2	IC,SRAM,DDR,256KX36,250MHZ,153P BGA	U11,U42	CRITICAL	L3_IC_2MB
333S0214	2	IC,SRAM,DDR,128KX36,250MHZ,153P BGA	U11,U42	CRITICAL	L3_IC_1MB
333S0244	2	IC,SRAM,DDR,128KX36,300MHZ,153P BGA	U11,U42	CRITICAL	300MHZ_L3_IC_1MB

L3 CACHE

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SIZE	DRAWING NUMBER	REV.
D	051-6403	E
SCALE: NONE	SHT 15 OF 46	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
343S0272	343S0008		U53	REV D CHANGE: ALTERNATE ADDITION

NOTE: CPU1_INT_L_PU, CPU1_SRESET_L_PU should be pulled up to CPU I/O plane, not +3V_MAIN. Since only one CPU is supported this is okay here

PLACE CREF CAP AT CRYSTAL GROUND

KEYLARGO

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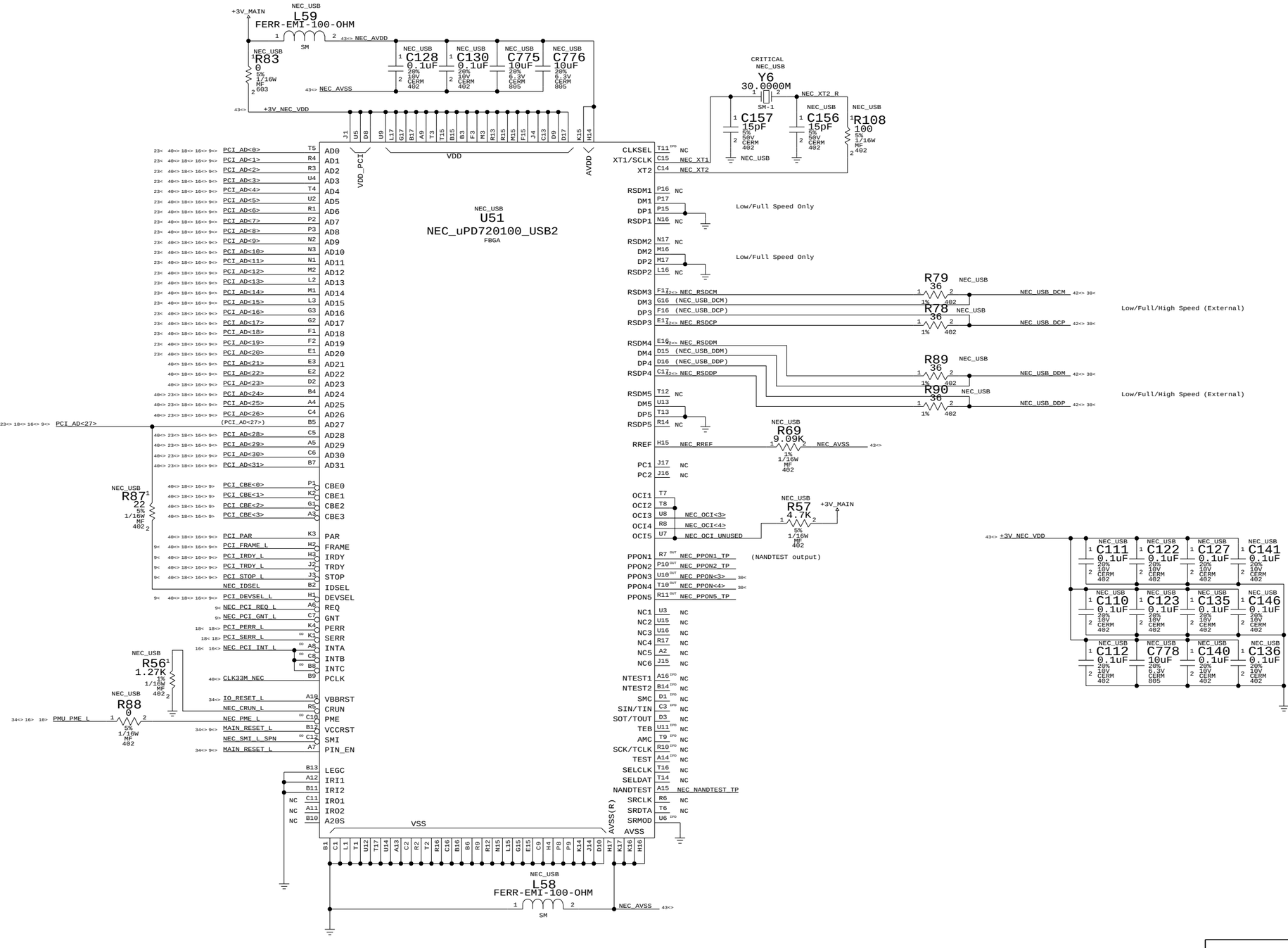
SCALE: NONE	SHT 16 OF 46	


+3V_MAIN
NEC_USB
L59
FERR-EMI-100-OHM
SM
43<> NEC_AVDD
R83
0
5%
1/16W
MF
603
C128
0.1uF
20%
10V
CERM
402
C130
0.1uF
20%
10V
CERM
402
C775
10uF
20%
6.3V
CERM
805
C776
10uF
20%
6.3V
CERM
805
43<> NEC_AVSS
43<> +3V_NEC_VDD
CRITICAL
Y6
30.0000M
SM-1
NEC_XT2_R
C157
15pF
5%
50V
CERM
402
C156
15pF
5%
50V
CERM
402
R108
100
5%
1/16W
MF
402
J1
U5
D8
U9
L17
G17
B17
A9
T3
T15
B15
B3
F3
M3
R13
R15
M15
F15
J4
C13
D9
D17
K15
H14
VDD
VDD_PCI
AVDD
U51
NEC_uPD720100_USB2
FBGA
AD0 T5
AD1 R4
AD2 R3
AD3 U4
AD4 T4
AD5 U2
AD6 R1
AD7 P2
AD8 P3
AD9 N2
AD10 N3
AD11 N1
AD12 M2
AD13 L2
AD14 M1
AD15 L3
AD16 G3
AD17 G2
AD18 F1
AD19 F2
AD20 E1
AD21 E3
AD22 E2
AD23 D2
AD24 B4
AD25 A4
AD26 C4
AD27 B5
AD28 C5
AD29 A5
AD30 C6
AD31 B7
CBE0 P1
CBE1 K2
CBE2 G1
CBE3 A3
PAR K3
FRAME H2
IRDY H3
TRDY J3
STOP J3
IDSEL B2
DEVSEL H1
REQ A6
GNT C7
PERR K4
SERR K1
INTA A8
INTB C8
INTC B8
PCLK B9
VBBRST A18
CRUN R5
PME C10
VCCRST B12
SMI C12
PIN_EN A7
LEGC B13
IRI1 A12
IRI2 B11
IRO1 C11
IRO2 A11
A20S B10
CLKSEL T11
XT1/SCLK C15 NEC_XT1
XT2 C14 NEC_XT2
RSDM1 P16 NC
DM1 P17
DP1 P15
RSDP1 N16 NC
Low/Full Speed Only
RSDM2 N17 NC
DM2 M16
DP2 M17
RSDP2 L16 NC
Low/Full Speed Only
RSDM3 F17
DM3 G16 (NEC_USB_DCM)
DP3 F16 (NEC_USB_DCP)
RSDP3 E17
RSDM4 E16
DM4 D15 (NEC_USB_DDM)
DP4 D16 (NEC_USB_DDP)
RSDP4 C17
RSDM5 T12 NC
DM5 U13
DP5 T13
RSDP5 R14 NC
Low/Full/High Speed (External)
Low/Full/High Speed (External)
R79
36
R78
36
R89
36
R90
36
1%
402
NEC_USB_DCM
NEC_USB_DCP
NEC_USB_DDM
NEC_USB_DDP
R69
9.09K
1%
1/16W
MF
402
RREF H15 NEC_RREF
NEC_AVSS
PC1 J17 NC
PC2 J16 NC
OCI1 T7
OCI2 T8
OCI3 U8 NEC_OCI<3>
OCI4 R8 NEC_OCI<4>
OCI5 U7 NEC_OCI_UNUSED
R57
4.7K
5%
1/16W
MF
402
+3V_MAIN
PPON1 R7 NEC_PPON1_TP
PPON2 P10 NEC_PPON2_TP
PPON3 U10 NEC_PPON<3>
PPON4 T10 NEC_PPON<4>
PPON5 R11 NEC_PPON5_TP
(NANDTEST output)
NC1 U3 NC
NC2 U15 NC
NC3 U16 NC
NC4 R17 NC
NC5 A2 NC
NC6 J15 NC
NTEST1 A16 NC
NTEST2 B14 NC
SMC D1 NC
SIN/TIN C3 NC
SOT/TOUT D3 NC
TEB U11 NC
AMC T9 NC
SCK/TCLK R10 NC
TEST A14 NC
SELCLK T16 NC
SELDAT T14 NC
NANDTEST A15 NEC_NANDTEST_TP
SRCLK R6 NC
SRDTA T6 NC
SRMOD U6 NC
AVSS
AVSS(R)
VSS
B1 C1 L1 T1 U12 T17 U14 A13 C2 R2 T2 R16 C16 B16 B6 R9 R12 N15 L15 G15 E15 C9 M4 P8 P9 K14 J14 D10 H17 K17 K16 H16
NEC_USB
L58
FERR-EMI-100-OHM
SM
NEC_AVSS
R87
22
5%
1/16W
MF
402
R56
1.27K
1%
1/16W
MF
402
R88
0
5%
1/16W
MF
402
PMU_PME_L
MAIN_RESET_L
IO_RESET_L
NEC_CRUN_L
NEC_PME_L
NEC_SMI_L_SPN
NEC_PCI_INT_L
NEC_PCI_REQ_L
NEC_PCI_GNT_L
PCI_PERR_L
PCI_SERR_L
PCI_DEVSEL_L
PCI_FRAME_L
PCI_IRDY_L
PCI_TRDY_L
PCI_STOP_L
NEC_IDSEL
PCI_PAR
PCI_CBE<0>
PCI_CBE<1>
PCI_CBE<2>
PCI_CBE<3>
PCI_AD<0>
PCI_AD<1>
PCI_AD<2>
PCI_AD<3>
PCI_AD<4>
PCI_AD<5>
PCI_AD<6>
PCI_AD<7>
PCI_AD<8>
PCI_AD<9>
PCI_AD<10>
PCI_AD<11>
PCI_AD<12>
PCI_AD<13>
PCI_AD<14>
PCI_AD<15>
PCI_AD<16>
PCI_AD<17>
PCI_AD<18>
PCI_AD<19>
PCI_AD<20>
PCI_AD<21>
PCI_AD<22>
PCI_AD<23>
PCI_AD<24>
PCI_AD<25>
PCI_AD<26>
PCI_AD<27>
(PCI_AD<27>)
PCI_AD<28>
PCI_AD<29>
PCI_AD<30>
PCI_AD<31>
CLK33M_NEC
NEC_USB
C111
C122
C127
C141
C110
C123
C135
C146
C112
C778
C140
C136
0.1uF
20%
10V
CERM
402
805
43<> +3V_NEC_VDD
USB 2.0
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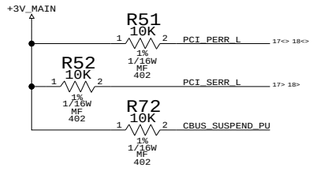
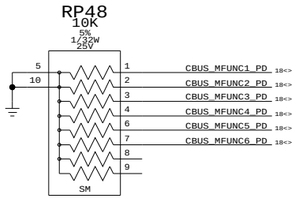
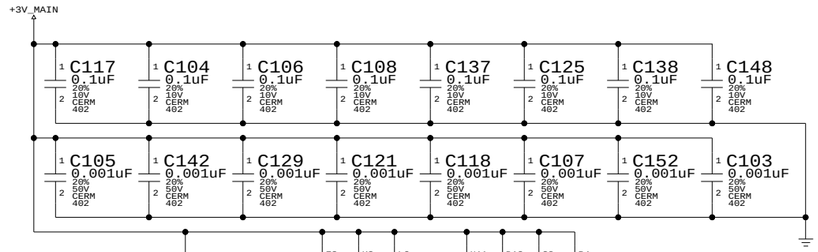
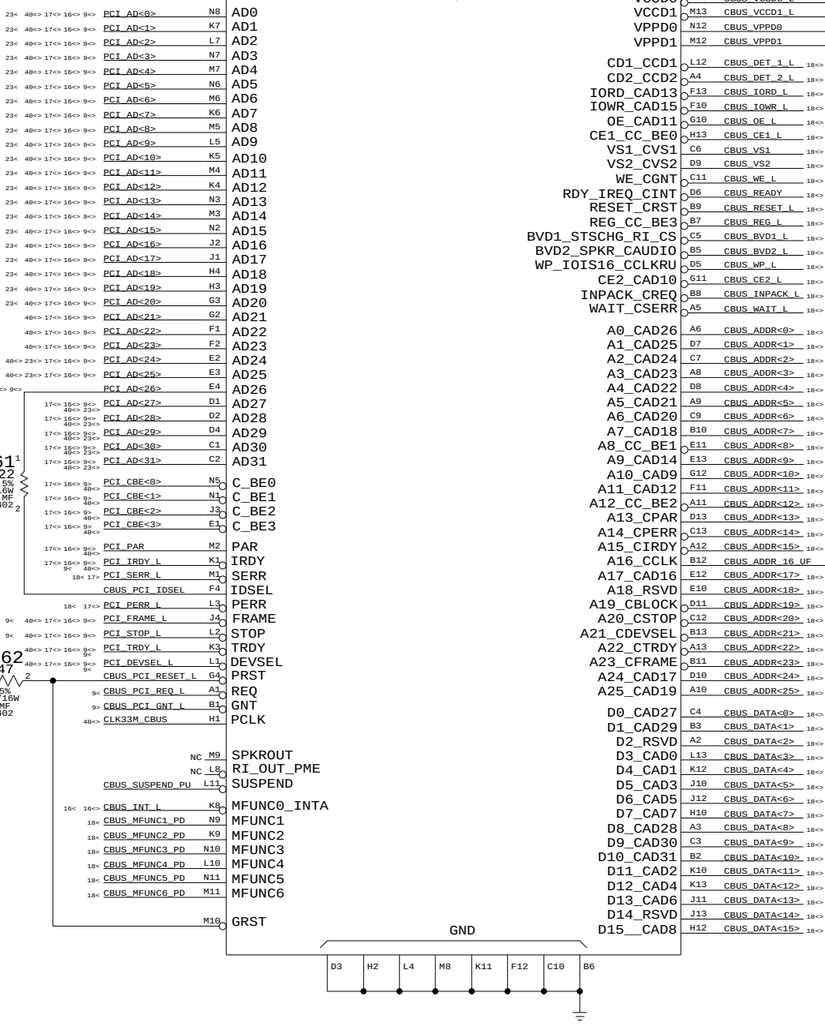
DRAWING NUMBER 051-6403
REV. E
SCALE NONE
SHT 17 OF 46

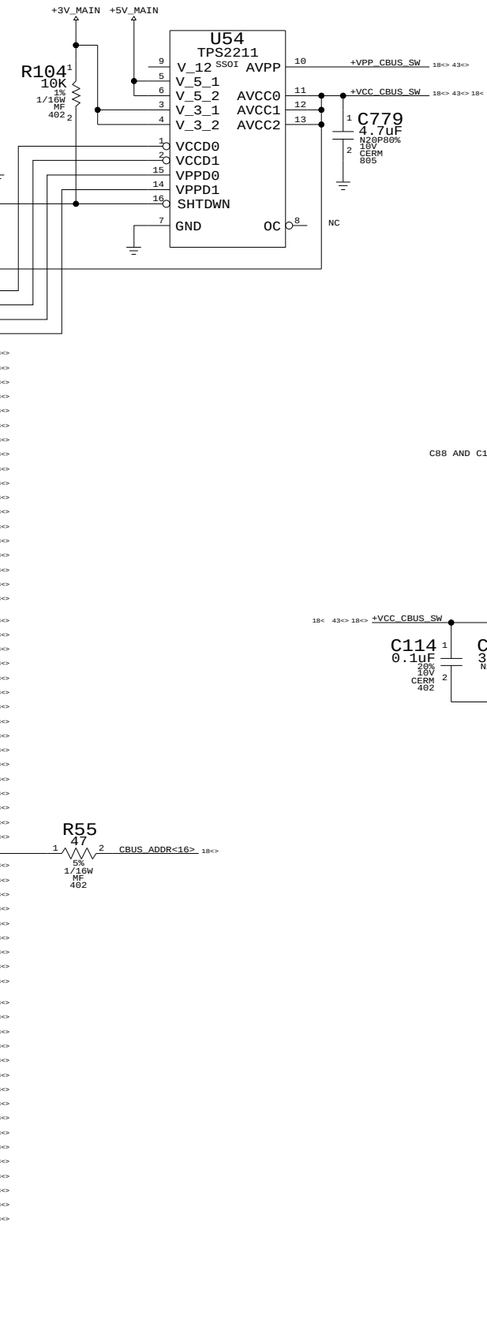
PCI1410 PULL-UPS





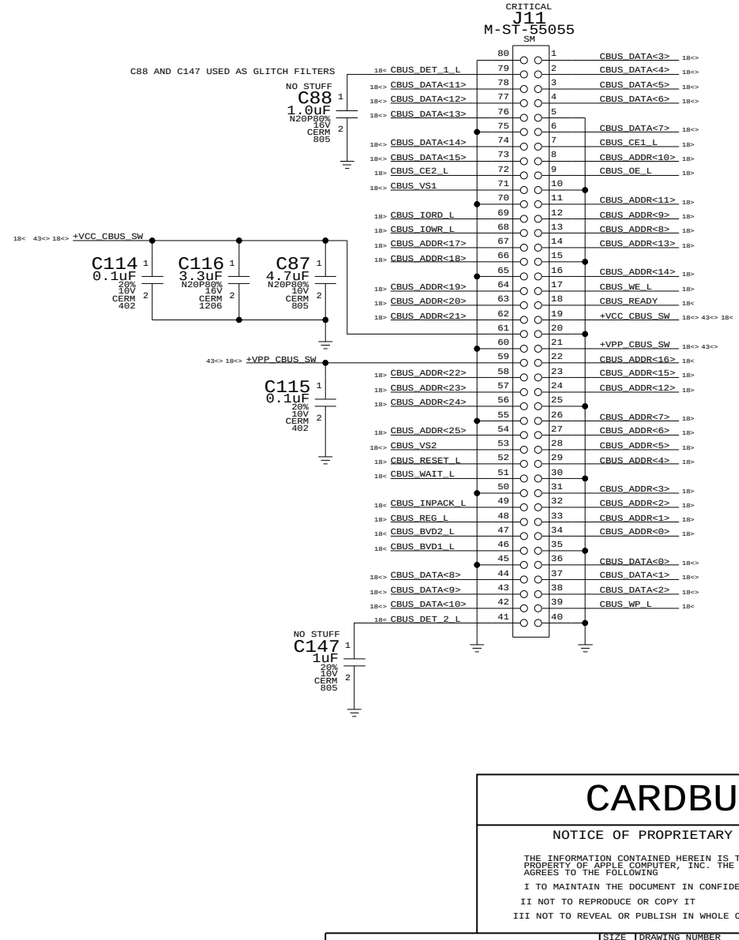






PC CARD/CARDBUS PULL-UPS

PC CARD/CARDBUS CONNECTOR



CARDBUS

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SIZE	DRAWING NUMBER	REV.
D	051-6403	E
SCALE: NONE	SHT 18 OF 46	

ATI PULL-UPS

+3V_MAIN

NO STUFF
R404 10K 5% 1/16W MF 402 — AGP_SUS_STAT_L_PU

R370 10K 5% 1/16W MF 402 — AGP_BUSY_L_PU 19>

R405 10K 5% 1/16W MF 402 — NO_ATI_SS / ATI_SS_PU

ATI_SS
[1]R703 470K 5% 1/16W MF 402

R227 0 5% 1/16W MF 402 — ATI_M9 / ATI_SSIN_PU

R235 0 5% 1/16W MF 402 — ATI_M7 / ATI_AUXWIN_PU 20<>

R208 45.3 1% 1/16W MF 402 — ATI_AGP_TEST

R384 1K 5% 1/16W MF 402 — ATI_TESTEN

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0033	1	IC,MOBILTY_M7,GRPHCS,696,BGA	U4	CRITICAL	ATI_M7
338S0090	1	IC,MOBILTY_M9_CSP32,768,BGA	U4	CRITICAL	ATI_M9

UNI-N AGP I/O REFERENCE
(PLACE CLOSE TO ATI AGP BALLS)

+1_5V_MAIN

C267 470pF 10% 50V CERM 402

R222[1] 4.99K 1% 1/16W MF 402 — UNIN_AGP_VREF_H

[1]R210 82.5 1% 1/16W MF 402 — UNIN_AGP_VREF

R223[1] 4.99K 1% 1/16W MF 402 — UNIN_AGP_VREF_L

C268 470pF 10% 50V CERM 402

ATI DDR I/O REFERENCE

R403 47 5% 1/16W MF 402 — IO_RESET_L 34<> / AGP_WBF_F

R259 0 5% 1/16W MF 402 — AGP_WBF_L

43<> +2_5V_ATI_VDDR

R162[1] 10K 1% 1/16W MF 402

R161[1] 10K 1% 1/16W MF 402

[1]C213 0.1uF 20% 10V CERM 402

+1_8V_ATI_VDDC18

SETUP FOR 2.5V MEMORY I/O

R256 10K 5% 1/16W MF 402 — ATI_MEMVMODE<0>

R152 4.7K 5% 1/16W MF 402 — ATI_MEMVMODE<1>

U4
RAGE_MOBILITY
M9-CSP32A13
32MB
BGA
(1 OF 6)
OMIT

40<> 8<> AGP_AD<31>	AB30	AD31	AD_STB0	N29	AGP_AD_STB<0> 8<> 40<> 8<
40<> 8<> AGP_AD<30>	AB27	AD30	AD_STB1	W29	AGP_AD_STB<1> 8<> 40<> 8<
40<> 8<> AGP_AD<29>	AA29	AD29	AD_STBB0	M28	AGP_AD_STB_L<0> 8<> 40<> 8<
40<> 8<> AGP_AD<28>	AB28	AD28	AD_STBB1	Y29	AGP_AD_STB_L<1> 8<> 40<> 8<
40<> 8<> AGP_AD<27>	AA30	AD27	AGP_BUSYB	AG28	AGP_BUSY_L_PU 19<
40<> 8<> AGP_AD<26>	AA27	AD26	AGPREF	K30	ATI_AGP_VREF
40<> 8<> AGP_AD<25>	Y30	AD25	AGPTEST	K29	ATI_AGP_TEST
40<> 8<> AGP_AD<24>	AA28	AD24	STEREO_SYNC	AJ28	AGP_SUS_STAT_L_PU
40<> 8<> AGP_AD<23>	W30	AD23	ST0	AF30	AGP_ST<0> 8>
40<> 8<> AGP_AD<22>	W27	AD22	ST1	AF28	AGP_ST<1> 8>
40<> 8<> AGP_AD<21>	V30	AD21	ST2	AE29	AGP_ST<2> 8>
40<> 8<> AGP_AD<20>	V28	AD20	SBA7	AC28	AGP_SBA<7> 40<> 8<
40<> 8<> AGP_AD<19>	V29	AD19	SBA6	AB29	AGP_SBA<6> 40<> 8<
40<> 8<> AGP_AD<18>	V27	AD18	SBA5	AC27	AGP_SBA<5> 40<> 8<
40<> 8<> AGP_AD<17>	U30	AD17	SBA4	AC30	AGP_SBA<4> 40<> 8<
40<> 8<> AGP_AD<16>	U28	AD16	SBA3	AD27	AGP_SBA<3> 40<> 8<
40<> 8<> AGP_AD<15>	R27	AD15	SBA2	AD30	AGP_SBA<2> 40<> 8<
40<> 8<> AGP_AD<14>	R29	AD14	SBA1	AE28	AGP_SBA<1> 40<> 8<
40<> 8<> AGP_AD<13>	P28	AD13	SBA0	AD29	AGP_SBA<0> 40<> 8<
40<> 8<> AGP_AD<12>	P30	AD12	RBFB	AE30	AGP_RBF_L 40<> 8<
40<> 8<> AGP_AD<11>	P27	AD11	STP_AGPB	AG29	AGP_STP_L
40<> 8<> AGP_AD<10>	P29	AD10	SB_STB	AC29	AGP_SB_STB 8<> 40<> 8<
40<> 8<> AGP_AD<9>	N28	AD9	SB_STBB	AD28	AGP_SB_STB_L 8<> 40<> 8<
40<> 8<> AGP_AD<8>	N30	AD8			
40<> 8<> AGP_AD<7>	M30	AD7	DPLUS	AC10	
40<> 8<> AGP_AD<6>	M27	AD6	DMINUS	AC11	
40<> 8<> AGP_AD<5>	M29	AD5			
40<> 8<> AGP_AD<4>	L28	AD4			
40<> 8<> AGP_AD<3>	L30	AD3			
40<> 8<> AGP_AD<2>	L27	AD2			
40<> 8<> AGP_AD<1>	L29	AD1			
40<> 8<> AGP_AD<0>	K28	AD0			
40<> 8<> AGP_CBE<3>	W28	CBEB3			
40<> 8<> AGP_CBE<2>	U29	CBEB2			
40<> 8<> AGP_CBE<1>	R30	CBEB1			
40<> 8<> AGP_CBE<0>	N27	CBEB0			
40<> CLK66M_AGP_ATI	AG30	PCICLK			
8< 40<> 8<> AGP_FRAME_L	U27	FRAMEB			
8< 40<> 8<> AGP_IRDY_L	T30	IRDYB			
8< 40<> 8<> AGP_TRDY_L	T28	TRDYB			
8< 40<> 8<> AGP_STOP_L	T27	STOPB			
8< 40<> 8<> AGP_DEVSEL_L	T29	DEVSELB			
40<> 8<> AGP_PAR	R28	PAR			
8< 40<> AGP_REQ_L	AF29	REQB			
40<> 8> AGP_GNT_L	AF27	GNTB			
16< 16<> AGP_ATI_INT_L	AH29	INTAB			
AGP_ATI_RESET_L	AH30	RSTB			
AGP_WBF_F	AE27	WBF/SERRB			
43<> +1_25V_ATI_VREF	D8	VREF			
NC	G29	QSA0	QSB0	C5	ATI_VMEM_QS<0> 22<> 41<>
NC	G27	QSA1	QSB1	A3	ATI_VMEM_QS<1> 22<> 41<>
NC	B29	QSA2	QSB2	G4	ATI_VMEM_QS<2> 22<> 41<>
NC	C26	QSA3	QSB3	E2	ATI_VMEM_QS<3> 22<> 41<>
NC	C16	QSA4	QSB4	U2	ATI_VMEM_QS<4> 22<> 41<>
NC	A15	QSA5	QSB5	V4	ATI_VMEM_QS<5> 22<> 41<>
NC	C11	QSA6	QSB6	AB2	ATI_VMEM_QS<6> 22<> 41<>
NC	A10	QSA7	QSB7	AC4	ATI_VMEM_QS<7> 22<> 41<>
NC	B18	RASAB	RASBB	P4	ATI_VMEM_RASB_L 41<> 22<
NC	A19	CASAB	CASBB	R3	ATI_VMEM_CASB_L 41<> 22<
NC	A18	WEAB	WEBB	R4	ATI_VMEM_WE_L 41<> 22<
NC	C19	CSAB0	CSBB0	P2	ATI_VMEM_CSB_L 41<> 22<
NC	B19	CSAB1	CSBB1	P3	NC
NC	D19	CKEA	CKEB	P1	ATI_VMEM_CKEB 41<> 22<
19< ATI_CLKA<0>	B23	CLKA0	CLKB0	K2	ATI_VMEM_CLKB<0> 42<> 22<
19< ATI_CLKA_L<0>	A23	CLKAB0	CLKBB0	K1	ATI_VMEM_CLKB_L<0> 42<> 22<
19< ATI_CLKA<1>	B22	CLKA1	CLKB1	L2	ATI_VMEM_CLKB<1> 42<> 22<
19< ATI_CLKA_L<1>	A22	CLKAB1	CLKBB1	L1	ATI_VMEM_CLKB_L<1> 42<> 22<
NC	A21	CLKAFB	CLKBFB	M2	NC
ATI_MEMVMODE<0>	B7	MEMVMODE0	MEMTEST	C8	ATI_MEMTEST
ATI_MEMVMODE<1>	B6	MEMVMODE1			

R687 10K 5% 1/16W MF 402 — SUS_STAT_L can be driven low in sleep to turn off AGP differential drivers. However, I/O pins can be (and are) driven immediately after power up. These resistors prevent ATI from contending with the PMU during startup. R402 << R687 to ensure all pins see valid logic levels prior to reset.

R402 1K 5% 1/16W MF 402 — SYSTEM_CLK_EN 34<>

R151 45.3 1% 1/16W MF 402

NO STUFF
R143 121 1% 1/16W MF 402 — ATI_CLKA<0> 19<> / ATI_CLKA_L<0> 19<>

NO STUFF
R150 121 1% 1/16W MF 402 — ATI_CLKA<1> 19<> / ATI_CLKA_L<1> 19<>

M7-CSP16
EXTERNAL MEMORY

U4
RAGE_MOBILITY
M9-CSP32A13
32MB
BGA
(2 OF 6)
OMIT

NC	B26	AA0	AB0	H2	ATI_VMEM_ADDR<0> 41<> 22<
NC	A26	AA1	AB1	H1	ATI_VMEM_ADDR<1> 41<> 22<
NC	B25	AA2	AB2	J2	ATI_VMEM_ADDR<2> 41<> 22<
NC	A25	AA3	AB3	J1	ATI_VMEM_ADDR<3> 41<> 22<
NC	C22	AA4	AB4	K4	ATI_VMEM_ADDR<4> 41<> 22<
NC	D21	AA5	AB5	K3	ATI_VMEM_ADDR<5> 41<> 22<
NC	C21	AA6	AB6	L4	ATI_VMEM_ADDR<6> 41<> 22<
NC	D20	AA7	AB7	M3	ATI_VMEM_ADDR<7> 41<> 22<
NC	C20	AA8	AB8	L3	ATI_VMEM_ADDR<8> 41<> 22<
NC	D22	AA9	AB9	M4	ATI_VMEM_ADDR<9> 41<> 22<
NC	C23	AA10	AB10	N2	ATI_VMEM_ADDR<10> 41<> 22<
NC	D23	AA11	AB11	N1	ATI_VMEM_ADDR<11> 22<> (4Mx32 only)
NC	A27	AA12	AB12	N4	ATI_VMEM_ADDR<12> 41<> 22<
NC	B27	AA13	AB13	N3	ATI_VMEM_ADDR<13> 41<> 22<
NC	J30	DQA0	DQB0	C7	ATI_VMEM_DATA<0> 22<> 41<>
NC	J29	DQA1	DQB1	D7	ATI_VMEM_DATA<1> 22<> 41<>
NC	H30	DQA2	DQB2	C6	ATI_VMEM_DATA<2> 22<> 41<>
NC	H29	DQA3	DQB3	D6	ATI_VMEM_DATA<3> 22<> 41<>
NC	F30	DQA4	DQB4	C4	ATI_VMEM_DATA<4> 22<> 41<>
NC	F29	DQA5	DQB5	D4	ATI_VMEM_DATA<5> 22<> 41<>
NC	E30	DQA6	DQB6	C3	ATI_VMEM_DATA<6> 22<> 41<>
NC	E29	DQA7	DQB7	D3	ATI_VMEM_DATA<7> 22<> 41<>
NC	J28	DQA8	DQB8	A5	ATI_VMEM_DATA<8> 22<> 41<>
NC	J27	DQA9	DQB9	B5	ATI_VMEM_DATA<9> 22<> 41<>
NC	H28	DQA10	DQB10	A4	ATI_VMEM_DATA<10> 22<> 41<>
NC	H27	DQA11	DQB11	B4	ATI_VMEM_DATA<11> 22<> 41<>
NC	F28	DQA12	DQB12	A2	ATI_VMEM_DATA<12> 22<> 41<>
NC	F27	DQA13	DQB13	B2	ATI_VMEM_DATA<13> 22<> 41<>
NC	E28	DQA14	DQB14	A1	ATI_VMEM_DATA<14> 22<> 41<>
NC	E27	DQA15	DQB15	B1	ATI_VMEM_DATA<15> 22<> 41<>
NC	D30	DQA16	DQB16	E4	ATI_VMEM_DATA<16> 22<> 41<>
NC	D29	DQA17	DQB17	E3	ATI_VMEM_DATA<17> 22<> 41<>
NC	C30	DQA18	DQB18	F3	ATI_VMEM_DATA<18> 22<> 41<>
NC	C29	DQA19	DQB19	F4	ATI_VMEM_DATA<19> 22<> 41<>
NC	A30	DQA20	DQB20	H3	ATI_VMEM_DATA<20> 22<> 41<>
NC	A29	DQA21	DQB21	H4	ATI_VMEM_DATA<21> 22<> 41<>
NC	A28	DQA22	DQB22	J3	ATI_VMEM_DATA<22> 22<> 41<>
NC	B28	DQA23	DQB23	J4	ATI_VMEM_DATA<23> 22<> 41<>
NC	D28	DQA24	DQB24	C1	ATI_VMEM_DATA<24> 22<> 41<>
NC	C28	DQA25	DQB25	C2	ATI_VMEM_DATA<25> 22<> 41<>
NC	D27	DQA26	DQB26	D1	ATI_VMEM_DATA<26> 22<> 41<>
NC	C27	DQA27	DQB27	D2	ATI_VMEM_DATA<27> 22<> 41<>
NC	D25	DQA28	DQB28	F1	ATI_VMEM_DATA<28> 22<> 41<>
NC	C25	DQA29	DQB29	F2	ATI_VMEM_DATA<29> 22<> 41<>
NC	D24	DQA30	DQB30	G1	ATI_VMEM_DATA<30> 22<> 41<>
NC	C24	DQA31	DQB31	G2	ATI_VMEM_DATA<31> 22<> 41<>
NC	D18	DQA32	DQB32	R1	ATI_VMEM_DATA<32> 22<> 41<>
NC	C18	DQA33	DQB33	R2	ATI_VMEM_DATA<33> 22<> 41<>
NC	D17	DQA34	DQB34	T1	ATI_VMEM_DATA<34> 22<> 41<>
NC	C17	DQA35	DQB35	T2	ATI_VMEM_DATA<35> 22<> 41<>
NC	D15	DQA36	DQB36	V1	ATI_VMEM_DATA<36> 22<> 41<>
NC	C15	DQA37	DQB37	V2	ATI_VMEM_DATA<37> 22<> 41<>
NC	D14	DQA38	DQB38	W1	ATI_VMEM_DATA<38> 22<> 41<>
NC	C14	DQA39	DQB39	W2	ATI_VMEM_DATA<39> 22<> 41<>
NC	B17	DQA40	DQB40	T3	ATI_VMEM_DATA<40> 22<> 41<>
NC	A17	DQA41	DQB41	T4	ATI_VMEM_DATA<41> 22<> 41<>
NC	B16	DQA42	DQB42	U3	ATI_VMEM_DATA<42> 22<> 41<>
NC	A16	DQA43	DQB43	U4	ATI_VMEM_DATA<43> 22<> 41<>
NC	B14	DQA44	DQB44	W3	ATI_VMEM_DATA<44> 22<> 41<>
NC	A14	DQA45	DQB45	W4	ATI_VMEM_DATA<45> 22<> 41<>
NC	B13	DQA46	DQB46	Y3	ATI_VMEM_DATA<46> 22<> 41<>
NC	A13	DQA47	DQB47	Y4	ATI_VMEM_DATA<47> 22<> 41<>
NC	D13	DQA48	DQB48	Y1	ATI_VMEM_DATA<48> 22<> 41<>
NC	C13	DQA49	DQB49	Y2	ATI_VMEM_DATA<49> 22<> 41<>
NC	D12	DQA50	DQB50	AA1	ATI_VMEM_DATA<50> 22<> 41<>
NC	C12	DQA51	DQB51	AA2	ATI_VMEM_DATA<51> 22<> 41<>
NC	D10	DQA52	DQB52	AC1	ATI_VMEM_DATA<52> 22<> 41<>
NC	C10	DQA53	DQB53	AC2	ATI_VMEM_DATA<53> 22<> 41<>
NC	D9	DQA54	DQB54	AD1	ATI_VMEM_DATA<54> 22<> 41<>
NC	C9	DQA55	DQB55	AD2	ATI_VMEM_DATA<55> 22<> 41<>
NC	B12	DQA56	DQB56	AA3	ATI_VMEM_DATA<56> 22<> 41<>
NC	A12	DQA57	DQB57	AA4	ATI_VMEM_DATA<57> 22<> 41<>
NC	B11	DQA58	DQB58	AB3	ATI_VMEM_DATA<58> 22<> 41<>
NC	A11	DQA59	DQB59	AB4	ATI_VMEM_DATA<59> 22<> 41<>
NC	B9	DQA60	DQB60	AD3	ATI_VMEM_DATA<60> 22<> 41<>
NC	A9	DQA61	DQB61	AD4	ATI_VMEM_DATA<61> 22<> 41<>
NC	B8	DQA62	DQB62	AE3	ATI_VMEM_DATA<62> 22<> 41<>
NC	A8	DQA63	DQB63	AE4	ATI_VMEM_DATA<63> 22<> 41<>
NC	G30	DQMAB0	DQMBB0	D5	ATI_VMEM_DQMB<0> 41<> 22<
NC	G28	DQMAB1	DQMBB1	B3	ATI_VMEM_DQMB<1> 41<> 22<
NC	B30	DQMAB2	DQMBB2	G3	ATI_VMEM_DQMB<2> 41<> 22<
NC	D26	DQMAB3	DQMBB3	E1	ATI_VMEM_DQMB<3> 41<> 22<
NC	D16	DQMAB4	DQMBB4	U1	ATI_VMEM_DQMB<4> 41<> 22<
NC	B15	DQMAB5	DQMBB5	V3	ATI_VMEM_DQMB<5> 41<> 22<
NC	D11	DQMAB6	DQMBB6	AB1	ATI_VMEM_DQMB<6> 41<> 22<
NC	B10	DQMAB7	DQMBB7	AC3	ATI_VMEM_DQMB<7> 41<> 22<

M9 EXTRA GND

U4
RAGE_MOBILITY
M9-CSP32A13
32MB
BGA
(6 OF 6)
OMIT

VSS: G7, G8, G9, G10, G11, G12, G13, G14, G15, G16, G17, G18, G19, G20, G21, G22, G23, G24, H7, H8, H23, H24, J7, J24, K7, K24, L7, L24, M7, M24, N7, N24, P7, P24, R7, R24, T7, T24, U7, U24, V7, V24, W7, W24, Y7, Y24, AA7, AA24, AB7, AB24, AC7, AC8, AC23, AC24, AD7, AD8, AD9, AD10, AD11, AD12, AD13, AD14, AD15, AD16, AD17, AD18, AD19, AD20, AD21, AD22, AD23, AD24

MOBILITY AGP & MEM

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SIZE D | DRAWING NUMBER 051-6403 | REV. E

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
155S0134	2	FLTR,EMI,FERR BEAD,0.1A,0402,SMD	R185,R159	

TMDS TERMINATION

Keep close to ATI chip

R705 330 5% 1/16W MF 402 — TMDS_DN<0> — TMDS_DP<0>
R706 330 5% 1/16W MF 402 — TMDS_DN<1> — TMDS_DP<1>
R707 330 5% 1/16W MF 402 — TMDS_DN<2> — TMDS_DP<2>

R708 49.9 1% 1/16W MF 402 — TMDS_CLKN — TMDS_CLK_CMT
R715 49.9 1% 1/16W MF 402 — TMDS_CLK_CMT — TMDS_CLKP
C892 470pF 10% 50V CERM 402
C893 470pF 10% 50V CERM 402

This clock termination network must be hooked up as drawn here. TMDS_CLK_CMT should be routed as a 4 mil surface trace so that it may be cut between the caps.

VGA SYNC BUFFERS

+3V_MAIN

OMIT 74AHC1G32 SM U32 — R185 33 5% 1/16W MF 402 — VGA_VSYNC — ATI_VSYNC — ATI_VSYNC_BUF

OMIT 74AHC1G32 SM U28 — R159 33 5% 1/16W MF 402 — VGA_HSYNC — ATI_HSYNC — ATI_HSYNC_BUF

PLACE THESE PARTS CLOSE TO ATI CHIP

U4 RAGE_MOBILITY M9-CSP32A13 32MB BGA (3 OF 6)

NC	AJ5	ZV_LCDDATA0	ROMCSB AE5 NC
NC	AK5	ZV_LCDDATA1	
NC	AG6	ZV_LCDDATA2	R AK28 ATI_R
NC	AH6	ZV_LCDDATA3	G AK27 ATI_G
NC	AJ6	ZV_LCDDATA4	B AK26 ATI_B
NC	AK6	ZV_LCDDATA5	
NC	AG7	ZV_LCDDATA6	VSYNC AG27 ATI_VSYNC
NC	AH7	ZV_LCDDATA7	V2SYNC AG25 NC
NC	AJ7	ZV_LCDDATA8	
NC	AK7	ZV_LCDDATA9	HSYNC AG26 ATI_HSYNC
NC	AG8	ZV_LCDDATA10	H2SYNC AG24 NC
NC	AH8	ZV_LCDDATA11	
NC	AJ8	ZV_LCDDATA12	RSET AK25 ATI_RSET
NC	AK8	ZV_LCDDATA13	R2SET AJ24 ATI_R2SET
NC	AG9	ZV_LCDDATA14	
NC	AH9	ZV_LCDDATA15	Y_G AK23 ATI_Y
NC	AJ9	ZV_LCDDATA16	C_R AK24 ATI_C
NC	AK9	ZV_LCDDATA17	COMP_B AK22 ATI_COMP
NC	AG10	ZV_LCDDATA18	
NC	AH10	ZV_LCDDATA19	
	AJ10	ZV_LCDDATA20	DIGON AE13 ATI_DIGON
NC	AK10	ZV_LCDDATA21	BLONB AF13 ATI_INV_ON_L
NC	AG11	ZV_LCDDATA22	HPD AF11 ATI_HPD
NC	AH11	ZV_LCDDATA23	
	AJ4	ZV_LCDCNTL0	
	AK4	ZV_LCDCNTL1	
	AH5	ZV_LCDCNTL2	
	AG5	ZV_LCDCNTL3	
	AJ2	GPIO0	AUXWIN AJ27 ATI_AUXWIN_PU
	AK2	GPIO1	
	AK1	GPIO2	VGADDCCLK AH27 ATI_DVI_DDC_CLK
	AH3	GPIO3	VGADDCDATA AH28 ATI_DVI_DDC_DATA
	AH2	GPIO4	
	AJ1	GPIO5	DVIDDCCLK AF12 LVDS_DDC_CLK
	AF4	GPIO6	DVIDDCDATA AE12 LVDS_DDC_DATA
	AH1	GPIO7	
	AG3	GPIO8	CRT2DDCCLK AH25 NC
	AF3	GPIO9	CRT2DDCDAT AH26 NC
	AG2	GPIO10	
	AF2	GPIO11	TXOUT_U0N AH18 NC
	AG1	GPIO12	TXOUT_U0P AG18 NC
	AF1	GPIO13	TXOUT_U1N AH19 NC
	AE2	GPIO14	TXOUT_U1P AG19 NC
	AE1	GPIO15	TXOUT_U2N AH20 NC
NC	M1	GPIO16	TXOUT_U2P AG20 NC
	AJ13	TX0M	TXOUT_U3N AH22 NC
	AK13	TX0P	TXOUT_U3P AG22 NC
	AJ14	TX1M	TXCLK_UN AH21 NC
	AK14	TX1P	TXCLK_UP AG21 NC
	AJ15	TX2M	TXOUT_L0N AK16 LVDS_L0N
	AK15	TX2P	TXOUT_L0P AJ16 LVDS_L0P
	AJ12	TXCM	TXOUT_L1N AK17 LVDS_L1N
	AK12	TXCP	TXOUT_L1P AJ17 LVDS_L1P
	AJ29	XTALIN	TXOUT_L2N AK18 LVDS_L2N
NC	AJ30	XTALOUT	TXOUT_L2P AJ18 LVDS_L2P
	AH24	TESTEN	TXOUT_L3N AK20 LVDS_L3N_SPN
	AJ26	SSIN	TXOUT_L3P AJ20 LVDS_L3P_SPN
	B24	VSS	TXCLK_LN AK19 CLKLVDS_N
	B20	VSS	TXCLK_LP AJ19 CLKLVDS_P
	A24	VSS	SSOUT AJ25
	A20	VSS	
	B21	VSS	

R422 10K 5% 1/16W MF 402 — ATI_SLAVE_VIP

M7/M9 I/O - 1.8V

+1_8V_MAIN — R343 0 5% 1/16W MF 603

C414 22uF 20% 10V TANT SMB
C413 10uF N20P80% 10V CERM 1206
C427 0.1uF 20% 10V CERM 402
C352 0.1uF 20% 10V CERM 402
C320 0.1uF 20% 10V CERM 402
C257 0.1uF 20% 10V CERM 402
C415 0.01uF 20% 16V CERM 402
C335 0.01uF 20% 16V CERM 402

+1_8V_ATI_VDDC18

R3 0 5% 1/4W FF 1210 — +1_2V_ATI_VCORE — +1_2V_ATI_VDDC

C270 10uF 20% 6.3V CERM 1206
C221 10uF 20% 6.3V CERM 1206
C473 0.1uF 20% 10V CERM 402
C474 0.1uF 20% 10V CERM 402
C399 0.1uF 20% 10V CERM 402
C300 0.1uF 20% 10V CERM 402
C239 0.1uF 20% 10V CERM 402
C258 0.1uF 20% 10V CERM 402
C269 0.1uF 20% 10V CERM 402
C382 0.1uF 20% 10V CERM 402
C460 0.1uF 20% 10V CERM 402
C236 0.1uF 20% 10V CERM 402
C428 0.1uF 20% 10V CERM 402
C478 0.1uF 20% 10V CERM 402
C256 0.1uF 20% 10V CERM 402
C426 0.1uF 20% 10V CERM 402
C271 0.01uF 20% 16V CERM 402
C398 0.01uF 20% 16V CERM 402
C524 0.01uF 20% 16V CERM 402
C233 0.01uF 20% 16V CERM 402
C397 0.01uF 20% 16V CERM 402
C477 0.01uF 20% 16V CERM 402
C364 0.01uF 20% 16V CERM 402
C248 0.01uF 20% 16V CERM 402

U4 RAGE_MOBILITY M9-CSP32A13 32MB BGA (5 OF 6) OMIT

(+1_8V_ATI_VDDC18) — VDDC18 — VDDC — VSS (DIE)

SPREAD SPECTRUM SUPPORT

+3V_SLEEP — L52 FERR-EMI-100-OHM SM — +3V_ATI_OSC_SLEEP

NO STUFF R477 100K 5% 1/16W MF 402

CRITICAL 14 — OSC SM-1 — VCC G1 27.0000M OUT GND 7 — OE

C707 0.1uF 20% 10V CERM 402
C708 4.7uF N20P80% 10V CERM 805

ATI_OSC_OE — CLK27M_ATI_UF — R463 182 1% 1/16W MF 402 — R448 22 5% 1/16W MF 402 — CLK27M_ATI — R447 150 1% 1/16W MF 402

Crystal input remains at 1.8V (not core voltage).

+3V_SLEEP — ATI_SS — L50 FERR-EMI-100-OHM SM — +3V_ATI_SS

C565 0.1uF 20% 10V CERM 402
C512 4.7uF N20P80% 10V CERM 805

CRITICAL — VDD U46 CY25811 SOI — XIN/CLKIN XOUT SSCLK FRSEL S1 S0 VSS 2

CLK27M_ATIMEM_US — R664 0 5% 1/16W MF 402

R690 0 5% 1/16W MF 402 — CY811_S1
R691 0 5% 1/16W MF 402
R692 0 5% 1/16W MF 402 — CY811_S0
R693 0 5% 1/16W MF 402

R667 33 5% 1/16W MF 402 — CLK27M_ATIMEM_SS — ATI_SS_PU

+5V_MAIN

C52 330uF 20% 6.3V TANT SMD
C526 10uF 20% 6.3V CERM 1206
C481 10uF 20% 6.3V CERM 1206
C432 0.1uF 20% 10V CERM 402

+3V_MAIN — NO STUFF R609 470K 5% 1/16W MF 402 — ATI_VCORE_CNTL

Q52 2N7002DW SOT-363 — ATI_VCORE_FB_SW

NO STUFF R610 0 5% 1/16W MF 402

Q52 2N7002DW SOT-363 — ATI_VCORE_CNTL_L

NO STUFF R611 470K 5% 1/16W MF 402

C586 680pF 5% 50V CERM 603
C587 47pF 5% 50V CERM 402
R437 4.7K 5% 1/16W MF 402
R385 0 5% 1/16W MF 402
NO STUFF R408 0 5% 1/16W MF 402
C567 1uF 20% 10V CERM 805
C566 0.1uF 20% 10V CERM 402

R35 0.02 1% 1/4W 1206 — XW16 SM — ATI_VCORE_SENSE — ATI_VCORE_L_SW

ATI_VCORE_VIN — ATI_VCORE_ITH — ATI_VCORE_SYNC_FCB — ATI_VCORE_RUN_SS — ATI_VCORE_VFB — ATI_VCORE_AGND

U14 LTC1773 MSOP

VIN — ITH — SENSE — SYNC_FCB — VFB — RUN_SS — SW — GND — TG — BG

ATI_VCORE_TG — ATI_VCORE_BG

CRITICAL Q5 SI4435DY SOI — S3 S2 S1 GATE — D4 D3 D2 D1

CRITICAL L6 3.3uH SM-3 — +1_2V_ATI_VCORE

Q4 FDS6680 SM-2 CRITICAL

C21 330uF 20% 6.3V TANT SMD
C20 330uF 20% 6.3V TANT SMD

C274 100pF 5% 50V CERM 402
C273 0.001uF 20% 50V CERM 402

R214 32.4K 1% 1/16W MF 402
R213 57.6K 1% 1/16W MF 402
R212 0 5% 1/16W MF 402

XW12 SM

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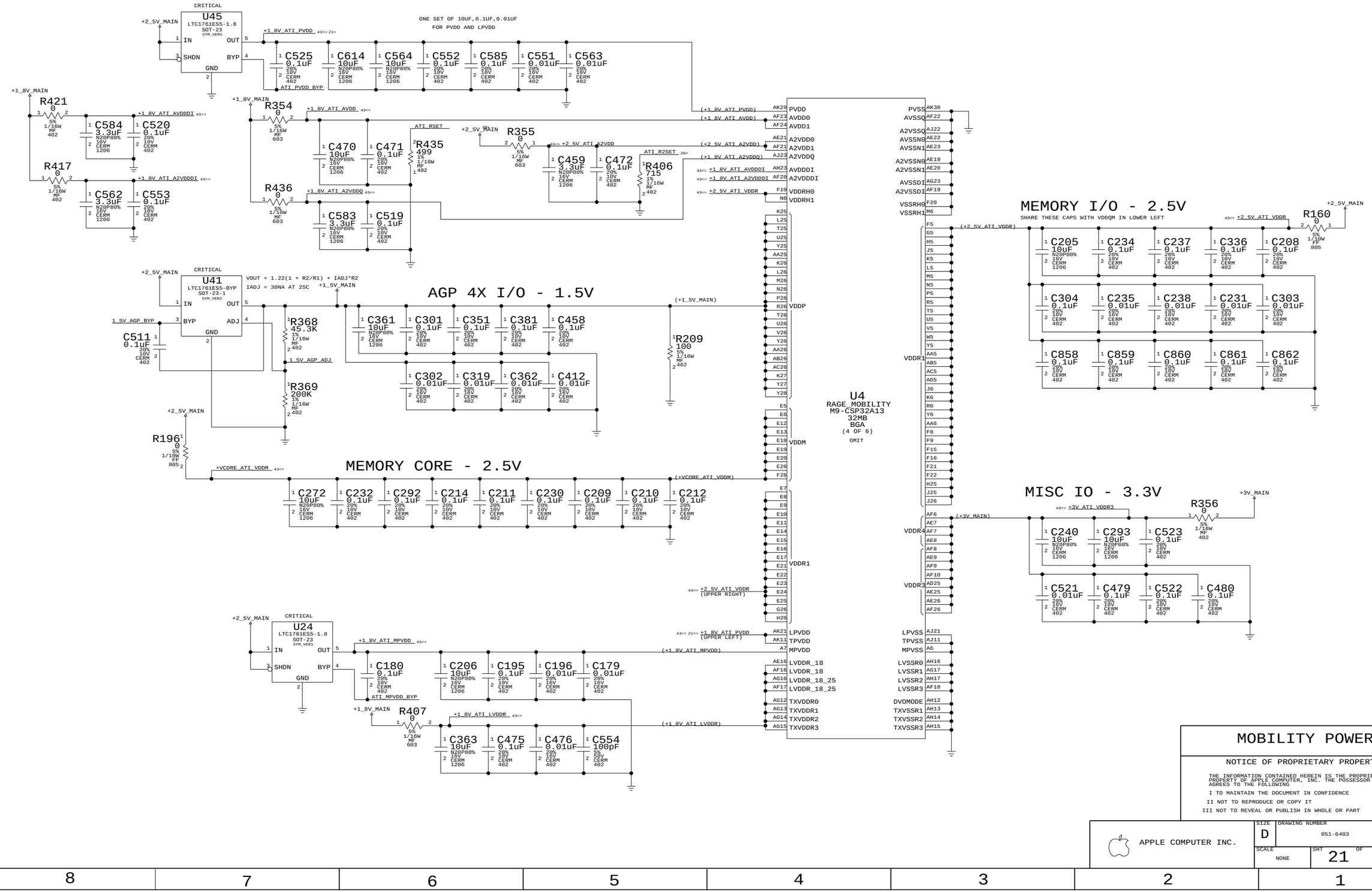
SIZE D | DRAWING NUMBER 051-6403 | REV. E

SCALE NONE | SHT 20 OF 46



MOBILITY POWER

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6403	E
SCALE: NONE	SHT 21 OF 46	

Keep close to memory

+VCORE_ATI_VDDM

C241 10uF 20% 6.3V CERM 1206
C200 0.01uF 20% 16V CERM 402
C198 0.1uF 20% 10V CERM 402
C251 0.01uF 20% 16V CERM 402
C250 0.1uF 20% 10V CERM 402

+2_5V_ATI_VDDR

C215 10uF 20% 6.3V CERM 1206
C222 0.01uF 20% 16V CERM 402
C197 0.1uF 20% 10V CERM 402
C199 0.01uF 20% 16V CERM 402
C249 0.1uF 20% 10V CERM 402

U2
SDRAM_DDR_2MX32
BGA
(1 OF 2)
OMIT

DATA LINES SWAPPABLE ONLY WITHIN SDRAM BYTE LANE.
BYTE LANE IS SWAPPABLE, IF NECESSARY. CONTACT DESIGNER.

ATI_VMEM_ADDR<0>	N5	A0	DQ0	B7 ATI_VMEM_DATA<0>
ATI_VMEM_ADDR<1>	N6	A1	DQ1	C6 ATI_VMEM_DATA<1>
ATI_VMEM_ADDR<2>	M6	A2	DQ2	B6 ATI_VMEM_DATA<2>
ATI_VMEM_ADDR<3>	N7	A3	DQ3	B5 ATI_VMEM_DATA<3>
ATI_VMEM_ADDR<4>	N8	A4	DQ4	C2 ATI_VMEM_DATA<4>
ATI_VMEM_ADDR<5>	M9	A5	DQ5	D3 ATI_VMEM_DATA<5>
ATI_VMEM_ADDR<6>	N9	A6	DQ6	D2 ATI_VMEM_DATA<6>
ATI_VMEM_ADDR<7>	N10	A7	DQ7	E2 ATI_VMEM_DATA<7>
ATI_VMEM_ADDR<8>	N11	A8	DQ8	K13 ATI_VMEM_DATA<24>
ATI_VMEM_ADDR<9>	M8	A9	DQ9	K12 ATI_VMEM_DATA<25>
ATI_VMEM_ADDR<10>	L6	A10	DQ10	J13 ATI_VMEM_DATA<26>
			DQ11	J12 ATI_VMEM_DATA<27>
ATI_VMEM_QS<0>	B2	DQS0	DQ12	G13 ATI_VMEM_DATA<28>
ATI_VMEM_QS<3>	H13	DQS1	DQ13	G12 ATI_VMEM_DATA<29>
ATI_VMEM_QS<1>	H2	DQS2	DQ14	F13 ATI_VMEM_DATA<30>
ATI_VMEM_QS<2>	B13	DQS3	DQ15	F12 ATI_VMEM_DATA<31>
			DQ16	F3 ATI_VMEM_DATA<8>
ATI_VMEM_DQMB<0>	B3	DM0	DQ17	F2 ATI_VMEM_DATA<9>
ATI_VMEM_DQMB<3>	H12	DM1	DQ18	G3 ATI_VMEM_DATA<10>
ATI_VMEM_DQMB<1>	H3	DM2	DQ19	G2 ATI_VMEM_DATA<11>
ATI_VMEM_DQMB<2>	B12	DM3	DQ20	J3 ATI_VMEM_DATA<12>
			DQ21	J2 ATI_VMEM_DATA<13>
ATI_VMEM_ADDR<13>	N4	BA0	DQ22	K2 ATI_VMEM_DATA<14>
ATI_VMEM_ADDR<12>	M5	BA1	DQ23	K3 ATI_VMEM_DATA<15>
			DQ24	E13 ATI_VMEM_DATA<16>
ATI_VMEM_CLKB<0>	M11	CK	DQ25	D13 ATI_VMEM_DATA<17>
ATI_VMEM_CLKB_L<0>	M12	CK	DQ26	D12 ATI_VMEM_DATA<18>
ATI_VMEM_CKEB	N12	CKE	DQ27	C13 ATI_VMEM_DATA<19>
ATI_VMEM_CSB_L	N2	CS	DQ28	B10 ATI_VMEM_DATA<20>
ATI_VMEM_RASB_L	M2	RAS	DQ29	B9 ATI_VMEM_DATA<21>
ATI_VMEM_CASB_L	L2	CAS	DQ30	C9 ATI_VMEM_DATA<22>
ATI_VMEM_WE_L	L3	WE	DQ31	B8 ATI_VMEM_DATA<23>
			MCL	M13
			RFU1	L9 NC
			RFU2	M10 NC
			RFU3	M7 ATI_VMEM_ADDR<11>

NC: C4, C11, H4, H11, L12, L13, M3, M4, N3

U2
SDRAM_DDR_2MX32
BGA
(2 OF 2)
OMIT

+VCORE_ATI_VDDM	D7	E5	
	D8	E7	
	E4	E8	
VDD	E11	E10	VSS
	L4	K6	
	L7	K7	
	L8	K8	
	L11	K9	
		L5	
+2_5V_ATI_VDDR	C3	L10	
	C5	F6	
	C7	F7	
	C8	F8	
	C10	F9	
	C12	G6	
	E3	G7	
VDDQ	E12	G8	VSS_THERM
	F4	G9	
	F11	H6	
	G4	H7	
	G11	H8	
	J4	H9	
+1_25V_ATI_VREF	J11	J6	
	K4	J7	
	K11	J8	
VREF	N13	J9	
		B4	
		B11	
		D4	
		D5	
		D6	
		D9	
		D10	
		D11	
		E6	
VSSQ		E9	
		F5	
		F10	
		G5	
		G10	
		H5	
		H10	
		J5	
		J10	
		K5	
		K10	

R187 121 1% 1/16W ME 402
ATI_VMEM_CLKB<0> — ATI_VMEM_CLKB_L<0>
Keep close to memory

Keep close to memory

+VCORE_ATI_VDDM

C400 10uF 20% 6.3V CERM 1206
C430 0.01uF 20% 16V CERM 402
C431 0.1uF 20% 10V CERM 402
C338 0.01uF 20% 16V CERM 402
C340 0.1uF 20% 10V CERM 402

+2_5V_ATI_VDDR

C365 10uF 20% 6.3V CERM 1206
C383 0.01uF 20% 16V CERM 402
C337 0.1uF 20% 10V CERM 402
C429 0.01uF 20% 16V CERM 402
C339 0.1uF 20% 10V CERM 402

U7
SDRAM_DDR_2MX32
BGA
(1 OF 2)
OMIT

DATA LINES SWAPPABLE ONLY WITHIN SDRAM BYTE LANE.
BYTE LANE IS SWAPPABLE, IF NECESSARY. CONTACT DESIGNER.

ATI_VMEM_ADDR<0>	N5	A0	DQ0	B7 ATI_VMEM_DATA<40>
ATI_VMEM_ADDR<1>	N6	A1	DQ1	C6 ATI_VMEM_DATA<41>
ATI_VMEM_ADDR<2>	M6	A2	DQ2	B6 ATI_VMEM_DATA<42>
ATI_VMEM_ADDR<3>	N7	A3	DQ3	B5 ATI_VMEM_DATA<43>
ATI_VMEM_ADDR<4>	N8	A4	DQ4	C2 ATI_VMEM_DATA<44>
ATI_VMEM_ADDR<5>	M9	A5	DQ5	D3 ATI_VMEM_DATA<45>
ATI_VMEM_ADDR<6>	N9	A6	DQ6	D2 ATI_VMEM_DATA<46>
ATI_VMEM_ADDR<7>	N10	A7	DQ7	E2 ATI_VMEM_DATA<47>
ATI_VMEM_ADDR<8>	N11	A8	DQ8	K13 ATI_VMEM_DATA<48>
ATI_VMEM_ADDR<9>	M8	A9	DQ9	K12 ATI_VMEM_DATA<49>
ATI_VMEM_ADDR<10>	L6	A10	DQ10	J13 ATI_VMEM_DATA<50>
			DQ11	J12 ATI_VMEM_DATA<51>
ATI_VMEM_QS<5>	B2	DQS0	DQ12	G13 ATI_VMEM_DATA<52>
ATI_VMEM_QS<6>	H13	DQS1	DQ13	G12 ATI_VMEM_DATA<53>
ATI_VMEM_QS<4>	H2	DQS2	DQ14	F13 ATI_VMEM_DATA<54>
ATI_VMEM_QS<7>	B13	DQS3	DQ15	F12 ATI_VMEM_DATA<55>
			DQ16	F3 ATI_VMEM_DATA<32>
ATI_VMEM_DQMB<5>	B3	DM0	DQ17	F2 ATI_VMEM_DATA<33>
ATI_VMEM_DQMB<6>	H12	DM1	DQ18	G3 ATI_VMEM_DATA<34>
ATI_VMEM_DQMB<4>	H3	DM2	DQ19	G2 ATI_VMEM_DATA<35>
ATI_VMEM_DQMB<7>	B12	DM3	DQ20	J3 ATI_VMEM_DATA<36>
			DQ21	J2 ATI_VMEM_DATA<37>
ATI_VMEM_ADDR<13>	N4	BA0	DQ22	K2 ATI_VMEM_DATA<38>
ATI_VMEM_ADDR<12>	M5	BA1	DQ23	K3 ATI_VMEM_DATA<39>
			DQ24	E13 ATI_VMEM_DATA<56>
ATI_VMEM_CLKB<1>	M11	CK	DQ25	D13 ATI_VMEM_DATA<57>
ATI_VMEM_CLKB_L<1>	M12	CK	DQ26	D12 ATI_VMEM_DATA<58>
ATI_VMEM_CKEB	N12	CKE	DQ27	C13 ATI_VMEM_DATA<59>
ATI_VMEM_CSB_L	N2	CS	DQ28	B10 ATI_VMEM_DATA<60>
ATI_VMEM_RASB_L	M2	RAS	DQ29	B9 ATI_VMEM_DATA<61>
ATI_VMEM_CASB_L	L2	CAS	DQ30	C9 ATI_VMEM_DATA<62>
ATI_VMEM_WE_L	L3	WE	DQ31	B8 ATI_VMEM_DATA<63>
			MCL	M13
			RFU1	L9 NC
			RFU2	M10 NC
			RFU3	M7 ATI_VMEM_ADDR<11>

NC: C4, C11, H4, H11, L12, L13, M3, M4, N3

U7
SDRAM_DDR_2MX32
BGA
(2 OF 2)
OMIT

+VCORE_ATI_VDDM	D7	E5	
	D8	E7	
	E4	E8	
VDD	E11	E10	VSS
	L4	K6	
	L7	K7	
	L8	K8	
	L11	K9	
		L5	
+2_5V_ATI_VDDR	C3	L10	
	C5	F6	
	C7	F7	
	C8	F8	
	C10	F9	
	C12	G6	
	E3	G7	
VDDQ	E12	G8	VSS_THERM
	F4	G9	
	F11	H6	
	G4	H7	
	G11	H8	
	J4	H9	
+1_25V_ATI_VREF	J11	J6	
	K4	J7	
	K11	J8	
VREF	N13	J9	
		B4	
		B11	
		D4	
		D5	
		D6	
		D9	
		D10	
		D11	
		E6	
VSSQ		E9	
		F5	
		F10	
		G5	
		G10	
		H5	
		H10	
		J5	
		J10	
		K5	
		K10	

R332 121 1% 1/16W ME 402
ATI_VMEM_CLKB<1> — ATI_VMEM_CLKB_L<1>
Keep close to memory

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0234	2	IC,SDRAM,DDR,4MX32,250MHZ,153P	BGA U2,U7	CRITICAL	M9_VMEM_32MB_HYNIX
333S0235	2	IC,SDRAM,DDR,4MX32,222MHZ,144P	FBGA U2,U7	CRITICAL	M9_VMEM_32MB_SAMSUNG
333S0108	2	IC,SDRAM,DDR,2MX32,222MHZ,144P	FBGA U2,U7	CRITICAL	M7_VMEM_16MB

EXT VIDEO MEM

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APPLE COMPUTER INC.

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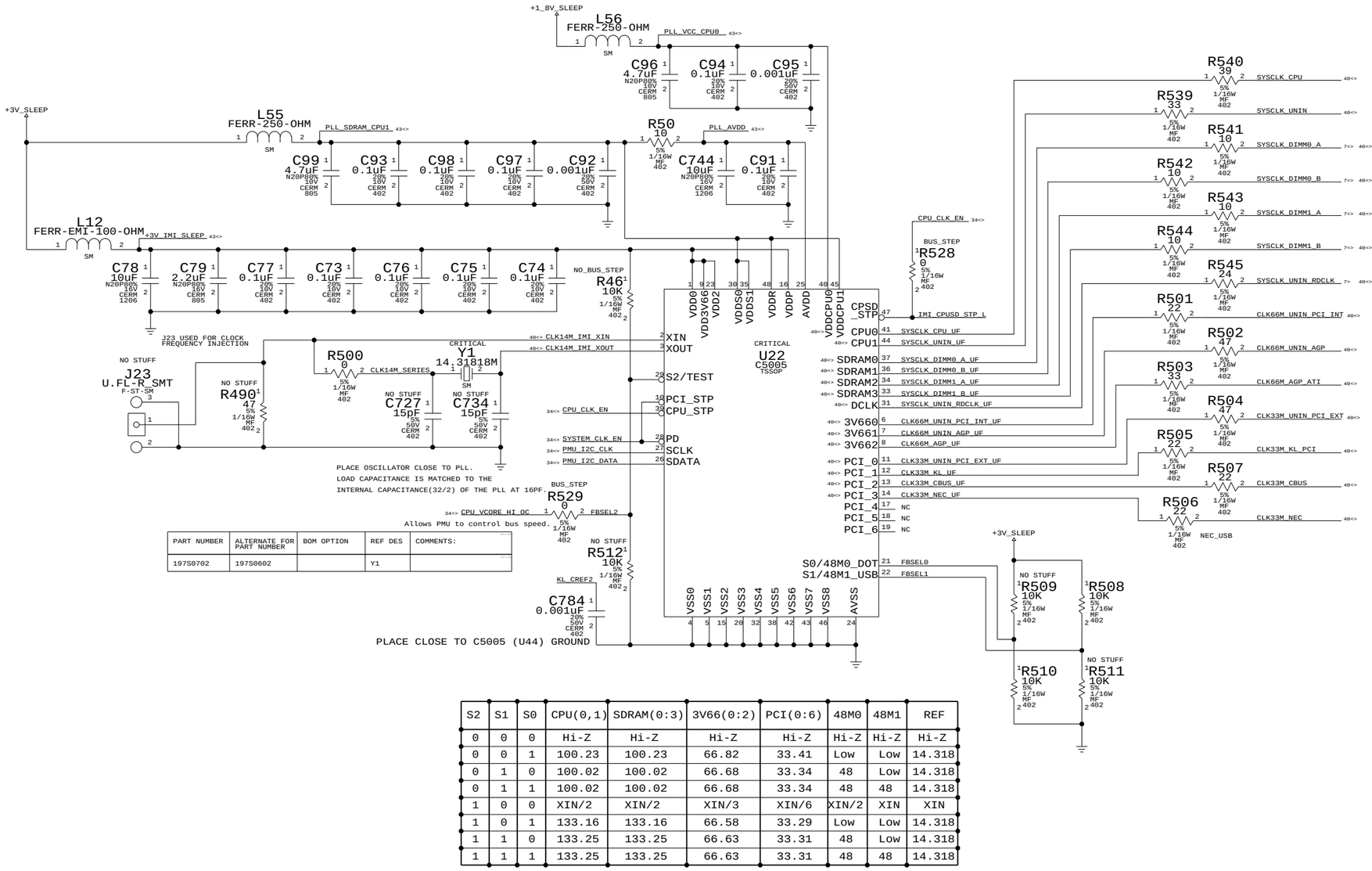
D	051-6403	E
SCALE	SHT 22 OF 46	
NONE		

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1045	1	FEPR_1MX8	40P TSOP	IC,FLASH,1Mx8,3.3V,PROGRAMMED	?	?	?	?	U23	CRITICAL	P59_ROM
341S1192	1	FEPR_1MX8	40P TSOP	IC,FLASH,1Mx8,3.3V,PROGRAMMED	?	?	?	?	U23	CRITICAL	P88_ROM

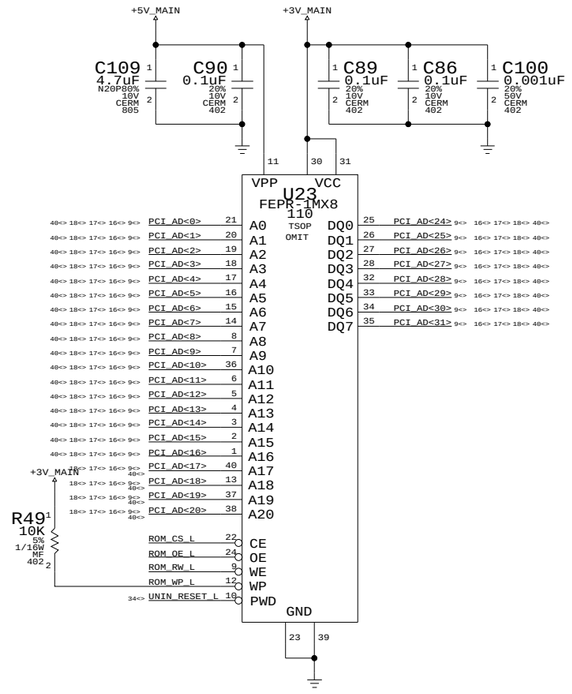
SYSTEM CLOCK GENERATOR



PART NUMBER	ALTERNATE_FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0702	197S0602		Y1	

S2	S1	S0	CPU(0,1)	SDRAM(0:3)	3V66(0:2)	PCI(0:6)	48M0	48M1	REF
0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
0	0	1	100.23	100.23	66.82	33.41	Low	Low	14.318
0	1	0	100.02	100.02	66.68	33.34	48	Low	14.318
0	1	1	100.02	100.02	66.68	33.34	48	48	14.318
1	0	0	XIN/2	XIN/2	XIN/3	XIN/6	XIN/2	XIN	XIN
1	0	1	133.16	133.16	66.58	33.29	Low	Low	14.318
1	1	0	133.25	133.25	66.63	33.31	48	Low	14.318
1	1	1	133.25	133.25	66.63	33.31	48	48	14.318

FLASH ROM



SYSTEM CLOCK GENERATOR / BOOTROM

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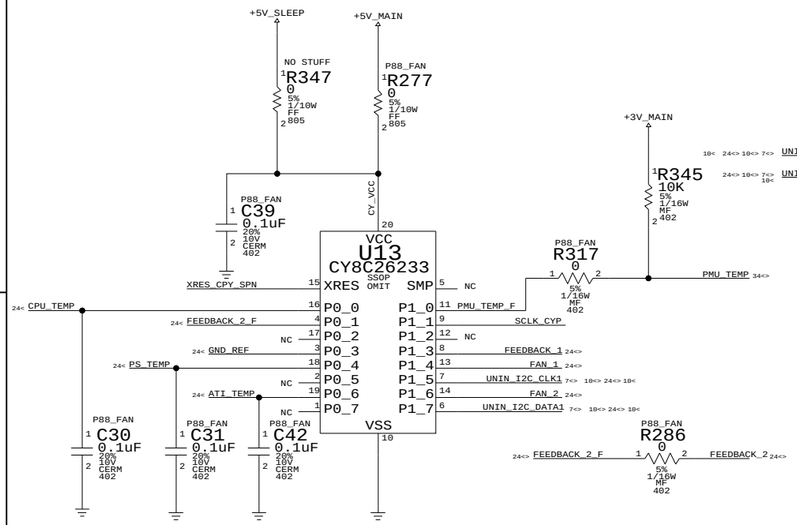
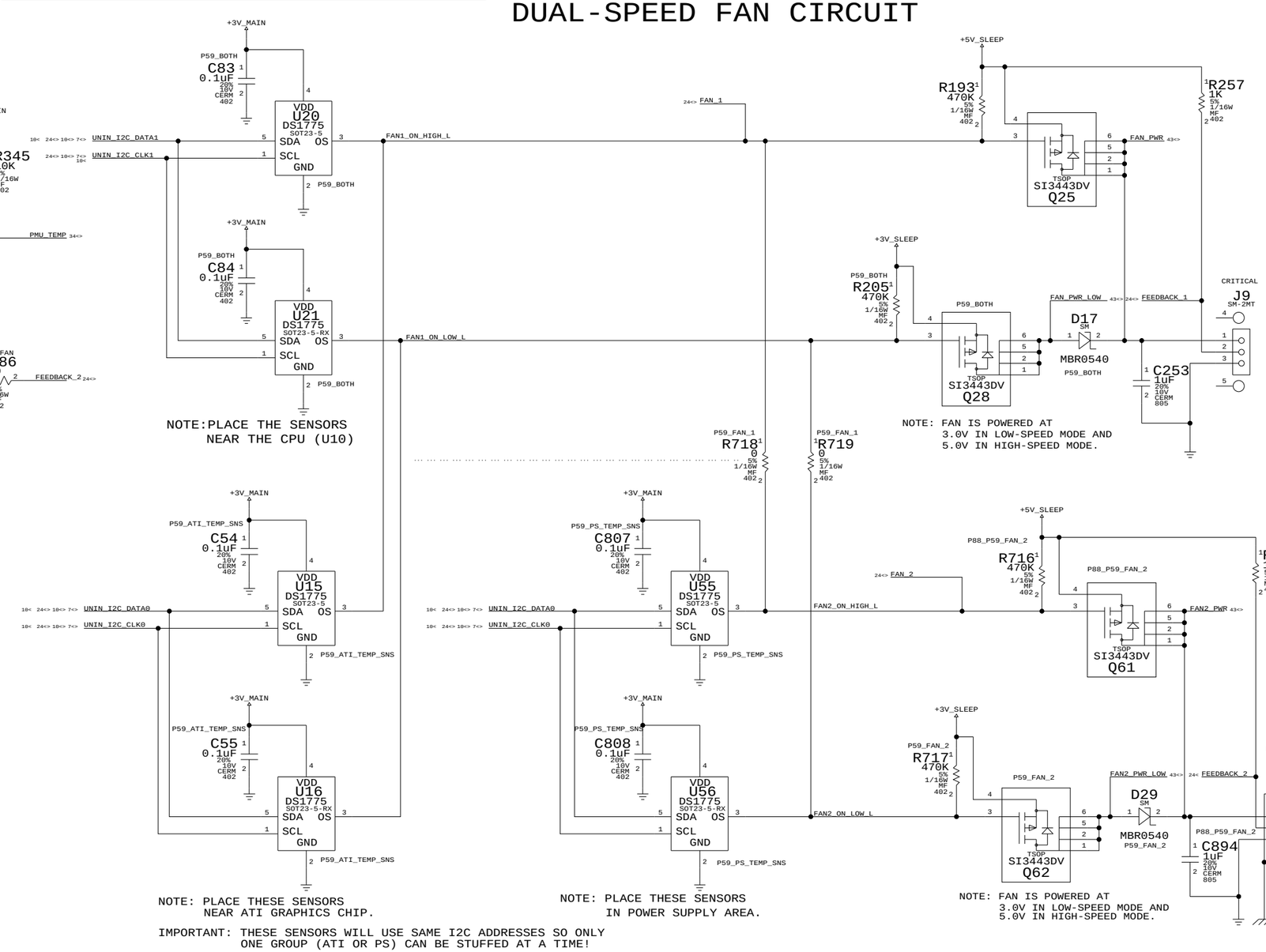
CYPRESS PSOC CONTROLLER

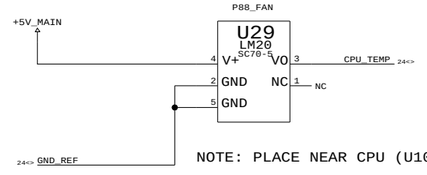
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1189	1	IC,MCU,PGRMD,CY8C26233,CP6099AMT	U13		P88_FAN

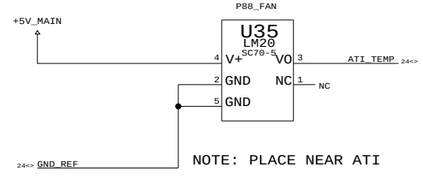


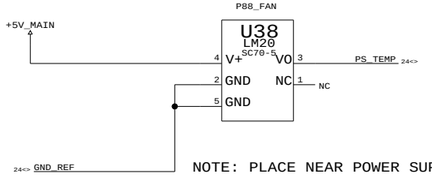
DUAL-SPEED FAN CIRCUIT



PCB TEMPERATURE SENSORS







FAN CIRCUIT OPTION

P59 SINGLE FAN : P59_BOTH + P59_FAN_1 + P59_PS_TEMP_SNS
P59 DUAL FAN : P59_BOTH + P59_FAN_2 + P88_P59_FAN_2 + P59_PS_TEMP_SNS
P88 FAN CIRCUIT: P88_FAN + P88_P59_FAN_2

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DUAL FAN CIRCUIT

APPLE COMPUTER INC.

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D	051-6403	E
SCALE: NONE	SHT 24 OF 46	

SNAPPER (AUDIO CODEC W/ EQ)

3V AUDIO POWER SUPPLY

PLACE VR1 CLOSE TO TASC3004

VR1 LP2951 SO1 — PLUS5VTAP, +5V_SLEEP, NC, IN, OUT, SENSE, ERR, SHUT, FDBK, GND

C797 10UF 20% 6.3V CERM 805

C113 0.1UF 20% 10V CERM 402

R38 100K 1% 1/16W MF 402

R58 60.4K 1% 1/16W MF 402

AUD3V_FDBK

43<> 26<> PWR3V_STAR_GND

43<> +AUD3V

PLACE THESE CAPS NEAR TAS3004C

R615 2.2 5% 1/16W MF 603 — 43<> FIL_AUD3V

C151 4.7UF N20P80% 10V CERM 805

C774 0.01UF 20% 16V CERM 402

43<> 26<> PWR3V_STAR_GND

R616 2.2 5% 1/16W MF 603 — 43<> FIL_DIG3V

C770 4.7UF N20P80% 10V CERM 805

C777 0.01UF 20% 10V CERM 402

R614 24.9K 1% 1/16W MF 603

R228 24.9K 1% 1/16W MF 603

C798 1200pF 5% 50V CERM 805

C810 1200pF 5% 50V CERM 805

C809 0.1UF 20% 10V CERM 402

43<> 26<> PWR3V_STAR_GND

SNDOUT0_FB

U57 TAS3004 PQFP

DVDD 17, AVDD 35

AIN_L_M → AINLM 46
AIN_L_P → AINLP 47
AIN_R_M → AINRM 43
AIN_R_P → AINRP 42
LINE_IN_L → LINA 1
LINE_IN_B → LINB 48
LINE_IN_R → RINA 46
MIC_IN → RINB 41
SND_TO_AUDIO → SDIN1 22
SDIN2 23

AOUTL 39 → AOUTL 26<
AOUTR 37 → AOUTR 26<

NO STUFF R619 0 5% 1/16W MF 402

SDOUT0 25 → TAS_SNDOUT0 → R64 10 5% 1/16W MF 402 → SND_TO_KL

SDOUT1 26 NC
SDOUT2 24 NC
INPA 5 NC
LRCLK/O 19 → SND_SYNC 16<
MCLKO 12 NC
SCL 15 → KL_I2C_CLK 16<> 32<> 16<
SCLK/O 20 → SND_SCLK 16<
SDA 16 → KL_I2C_DATA 16<> 32<> 16<
VRFILT 2 → TI_VRFILT
VCOM 38 → TI_VCOM
NC0 34 NC
NC1 36 NC

C812 10UF 20% 6.3V TANT SMA
C813 0.1UF 20% 10V CERM 402
C814 22UF 10% 6.3V TANT SMA
C815 0.1UF 20% 10V CERM 402

C811 1UF 20% 10V CERM 805

C799 0.01UF 20% 16V CERM 402

R617 5.11 1% 1/16W FF 805 — TI_CAP

R618 0 5% 1/16W MF 402 — NC

GPI0 28, GPI1 29, GPI2 30, GPI3 31, GPI4 32, GPI5 33

IFM/S 21
ALLPASS 27
TI_CAP_PLL → CAP_PLL 10
CLKSEL 11
CS_1 → CS1 7
VREFM 45
VREFP 44
40<> SND_CLKOUT → XTIN1/MCLK 13
XTLIN0 14
PWR_DN 8
16<> AUDIO_RESET_L (PD at KL) → RESET 6
TEST 9

DVSS 18, AVSS 4, AVSS (REF) 3

43<> +AUD3V

R59 10K 5% 1/16W MF 402

NO STUFF R63 10K 5% 1/16W MF 402

C119 1UF 20% 10V CERM 805

C120 0.1UF 20% 10V CERM 402

C145 0.1UF 20% 10V CERM 402

43<> 26<> PWR3V_STAR_GND

43<> 26<> TI_AVSS

SNAPPER CONTROL

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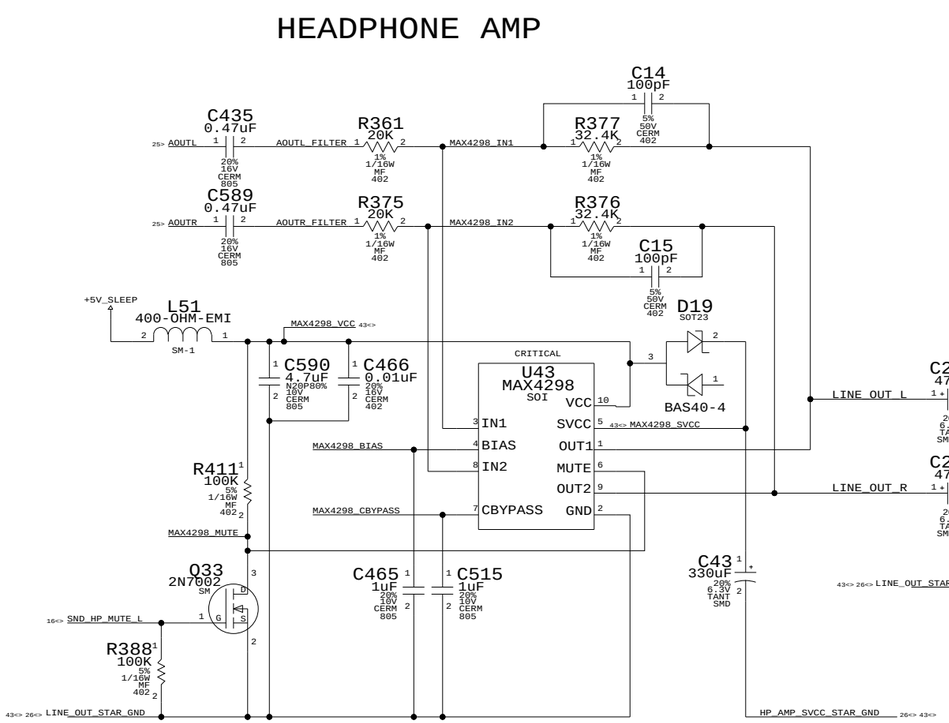
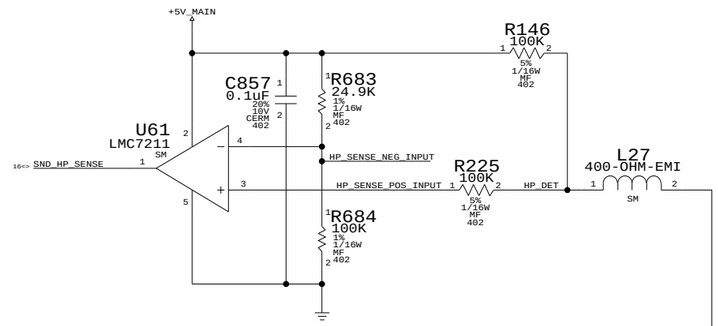
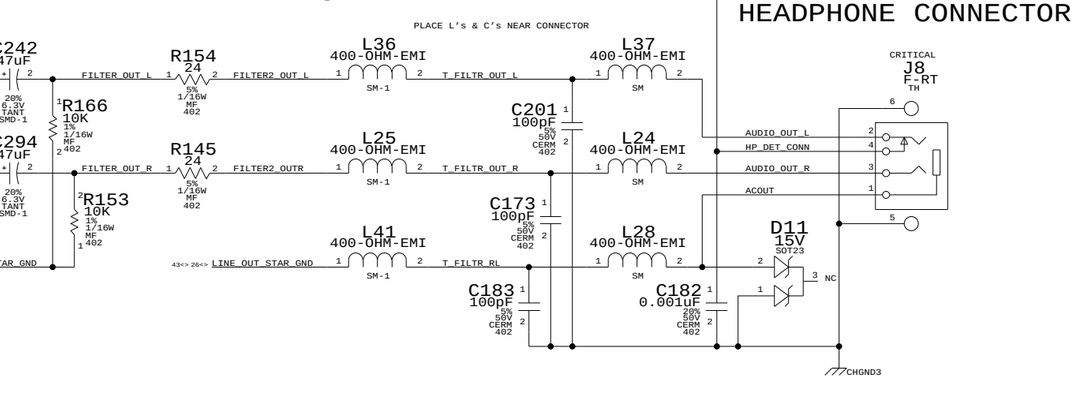
HEADPHONE AMP



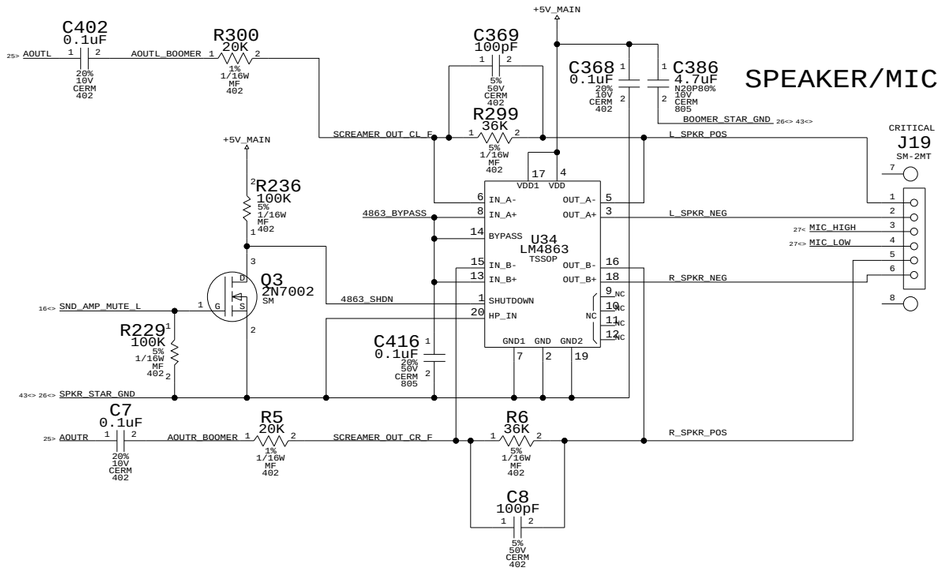
HEADPHONE DETECTION



HEADPHONE CONNECTOR

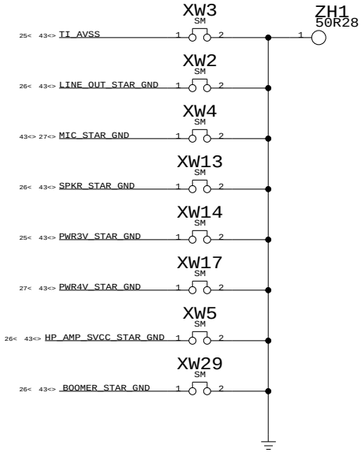


BOOMER SPEAKER AMP



SPEAKER/MIC CONNECTOR

AUDIO STAR GROUND



HEADPHONE/SPEAKERS

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D	051-6403	E
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SOI
TLV2362
CR-27

LINE IN AMPLIFIER

LINE IN CONNECTOR

CRITICAL
TH1
F-RT-3050100
J30
LIN_LCH
LIN_SNS
LIN_RCH
LIN_GND
L79 1000-OHM-EMI SM
L78 1000-OHM-EMI SM
L76 1000-OHM-EMI SM
L77 1000-OHM-EMI SM
LIN_DET_EMI
C838 100pF 5% 50V CERM 402
C837 100pF 5% 50V CERM 402
C836 100pF 5% 50V CERM 402
C835 100pF 5% 50V CERM 402
R642 100K 1% 1/16W MF 402
R643 100K 1% 1/16W MF 402
R638 200 5% 1/16W MF 402
CHGND2
LCH_HZ
GND_HZ
RCH_HZ

C840 4.7uF 20% 25V CERM 1210
C841 10uF 20% 6.3V CERM 1206
C842 4.7uF 20% 25V CERM 1210
LCH_GALVA
GND_GALVA
RCH_GALVA

R645 27.4K 1% 1/16W MF 402
R646 27.4K 1% 1/16W MF 402
R647 27.4K 1% 1/16W MF 402
R648 27.4K 1% 1/16W MF 402
R649 10.7K 1% 1/16W MF 402
R650 10.7K 1% 1/16W MF 402
R651 10.7K 1% 1/16W MF 402
R652 10.7K 1% 1/16W MF 402
SUDO_L_P
SUDO_L_M
SUDO_L
SUDO_GND
SUDO_R_P
SUDO_R_M
SUDO_R

CRITICAL
U58 TLV2362 SOI
43<> +AUD4V_F1
C845 2.2UF 20% 16V TANT SMA
C846 0.01uF 20% 16V CERM 402
C848 0.47UF 20% 16V CERM 805
C844 120PF 5% 50V CERM 402
C843 120PF 5% 50V CERM 402
C847 0.47UF 20% 16V CERM 805
LINE_IN_L
LINE_IN_R
PWR4V_STAR_GND 26<> 43<>

R653 4.7 5% 1/16W MF 402
R654 4.7 5% 1/16W MF 402
43<> +AUD4V
43<> +AUD4V_F2

CRITICAL
U59 TLV2362 SOI
C850 0.01uF 20% 16V CERM 402
C849 2.2UF 20% 16V TANT SMA

R658 12K 5% 1/16W MF 402
R659 12K 5% 1/16W MF 402
R660 33K 5% 1/16W MF 402
Q53 2N3904 SM
Q54 2N3904 SM
AUDIO_REF_3V
AUDIO_REF_2V
MIC_POLA
C853 4.7UF N20P80% 10V CERM 805
C854 4.7UF N20P80% 10V CERM 805
PWR4V_STAR_GND 26<> 43<>

AUDIO_REF
R17 47K 5% 1/16W MF 402
C23 0.01uF 20% 16V CERM 402
43<> 26<> PWR4V_STAR_GND

CRITICAL
U59 TLV2362 SOI
C856 0.47UF 20% 16V CERM 805
MIC_GAINED
MIC_IN

R655 2.2K 5% 1/16W MF 402
MIC_DIVIDER
R656 330 5% 1/16W MF 402
C852 0.1UF 20% 10V CERM 402
MIC_GALVA
R661 9.1K 5% 1/16W MF 402
MIC_DIFF_IN
R662 470K 5% 1/16W MF 402
C855 22pF 5% 50V CERM 603
C851 470pF 10% 50V CERM 402
R657 47K 5% 1/16W MF 402
XW28 SM
26<> MIC_HIGH
26<> MIC_LOW
MIC_STAR_GND 26<> 43<>

L80 GROUND MOAT

L80 1000-OHM-EMI SM
LIN_DET_EMI
LIN_DET
Span ground moat using L80
+5V_SLEEP
R15 470K 5% 1/16W MF 402
R16 47K 5% 1/16W MF 402
SND_LIN_SENSE 16<>
C19 0.001uF 20% 50V CERM 402

4V AUDIO POWER SUPPLY

NC
PLUS5VTAP VR2 LP2951 SOI
IN OUT
NC SENSE ERR NC
SHUT FDBK
GND
+5V_SLEEP
+AUD4V 43<>
C839 1.0uF N20P80% 10V CERM 805
C796 0.1UF 20% 10V CERM 402
AUD4V_FDBK
R180 49.9K 1% 1/16W MF 402
R226 20K 1% 1/16W MF 402
PWR4V_STAR_GND 26<> 43<>

MICROPHONE AMPLIFIER

MIC & LINE-IN INPUTS

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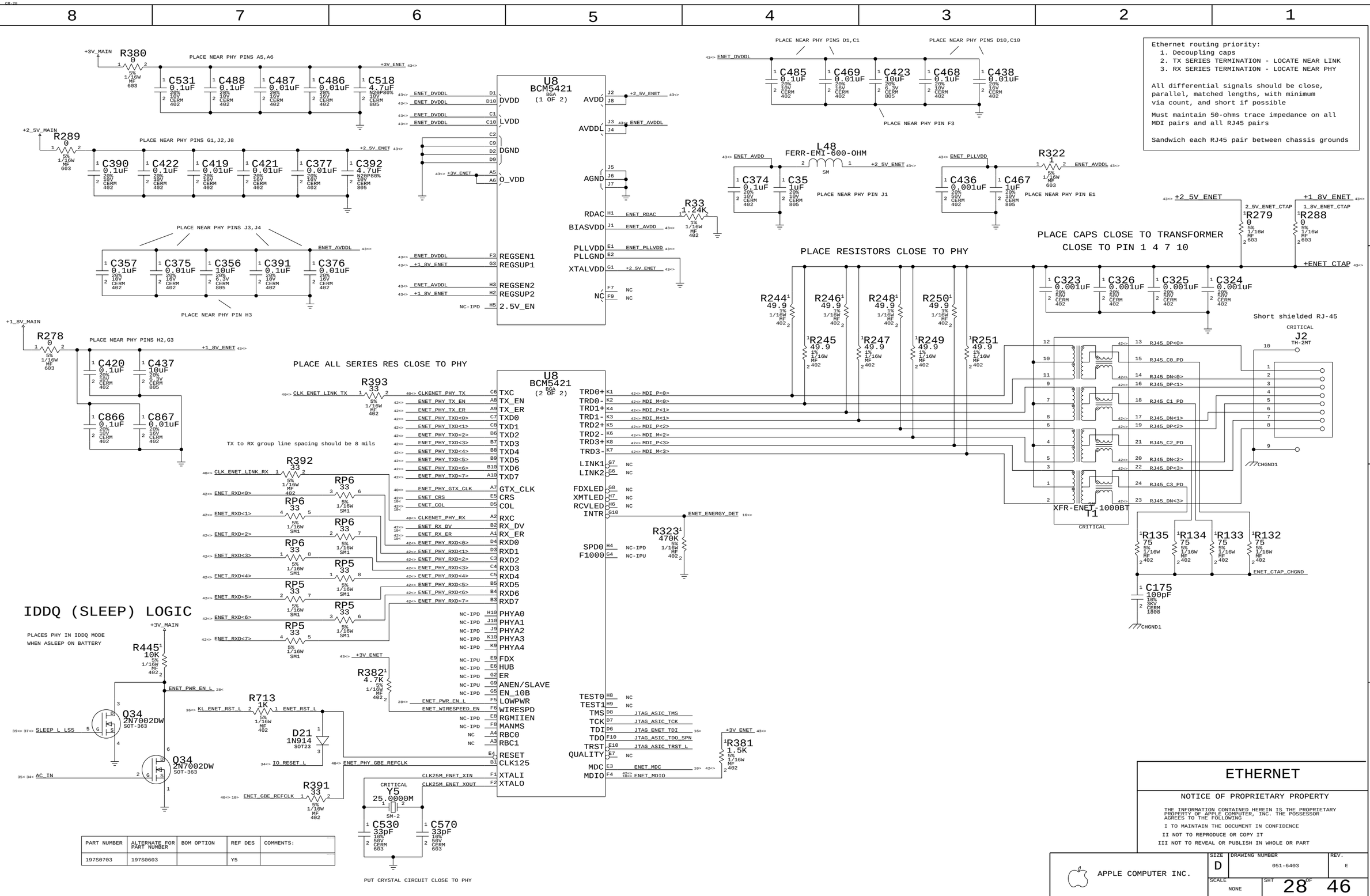
SCALE: NONE	SHT 27 OF 46	



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0703	197S0603		Y5	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
740S0527	1	OVERCURRENT PROTECTOR,0.75A,30V,SMB	F2	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0706	197S0606		Y4	

PORT POWER SWITCH

D25 SM 10BQ040 — 36< 43<> 36<> PWRBUS_14_24V — Allows sleep/shutdown charging of peripherals when on adapter

Q2 NDS9407 SOI — +PBUS — +PBUS_FW_SW 43<>

D1 SM 10BQ040

OMIT F2 0.9AMP-33V SM — +FW_VP_UF 43<>

L26 FERR-250-OHM SM

R157 330K 5% 1/10W MF 402 — C203 0.01uF 20% 10V CERM 402 — FW_PWR_GATE

R171 470K 5% 1/16W MF 402 — FW_PWREN_L

FW_PWREN — R189 10K 5% 1/16W MF 402 — 16<> KL_FW_PWREN — Q22 2N7002 SM

+3V_MAIN — L49 FERR-EMI-100-OHM SM — +3V_FW_VDD 29<> 43<>

KEEP CAPS CLOSE TO PHY POWER PINS.

C353 1uF 20% 10V CERM 805 — C387 1uF 20% 10V CERM 805 — C313 0.1uF 20% 10V CERM 402 — C344 0.1uF 20% 10V CERM 402 — C345 0.1uF 20% 10V CERM 402

C373 0.1uF 20% 10V CERM 402 — C389 0.1uF 20% 10V CERM 402 — C403 0.001uF 20% 50V CERM 402 — C388 0.001uF 20% 50V CERM 402

+FW_VP_FUSE 43<> — R23 422K 1% 1/16W MF 402

PLACE C354 CLOSE TO PLLVDD (U5 PIN 40)

C354 0.1uF 20% 10V CERM 402

CRITICAL Y4 24.576M SM-2 — CLK24M_FW_XIN — CLK24M_FW_XOUT

C261 22pF 5% 50V CERM 603 — C404 22pF 5% 50V CERM 603

C29 0.1uF 20% 10V CERM 402

U5 TSB41AB1 FLAS

FW_F0	38	FILTER0	R0	33	FW_R0
FW_F1	39	FILTER1	R1	34	FW_R1
FW_PHY_CPS	20	CPS			
	42	XI	TPBIAS	31	FW_BIAS0
	43	XO	TPA+	30	42<> FW_TPA0P
16<> FW_PHY_PD	12	PD	TPA-	29	42<> FW_TPA0N
FW_PHY_SE	23	SE	TPB+	28	42<> FW_TPB0P
FW_PHY_RST_L	24	SM	TPB-	27	42<> FW_TPB0N
	37	RESET			
	19	ISO	C_LKON	15	FW_C_LKON 10<> 16<>
10< FW_PHY_LPS	13	LPS			
42<> FW_PHY_LREQ	48	LREQ			
	40	PLLVDD	PLLGND	41	
40<> CLK_PHY_FW	1	SYSCLK			
42<> FW_PHY_CNTL<0>	2	CTL0	AVDD1	25	
42<> FW_PHY_CNTL<1>	3	CTL1	AVDD2	35	
42<> FW_PHY_DATA<0>	4	D0	DVDD1	21	
42<> FW_PHY_DATA<1>	5	D1	DVDD2	44	
42<> FW_PHY_DATA<2>	6	D2	DVDD3	45	
42<> FW_PHY_DATA<3>	7	D3	AGND1	26	
42<> FW_PHY_DATA<4>	8	D4	AGND2	32	
42<> FW_PHY_DATA<5>	9	D5	AGND3	36	
42<> FW_PHY_DATA<6>	10	D6	DGND1	14	
42<> FW_PHY_DATA<7>	11	D7	DGND2	46	
	22	TESTM	DGND3	47	
	16	PC0			
	17	PC1			
	18	PC2			

R204 6.34K 1% 1/16W MF 402

KEEP FW_LREQ SERIES R CLOSE TO LINK — R181 22 5% 1/16W MF 402 — 42<> 10< FW_LINK_LREQ

KEEP FW_CLK SERIES R CLOSE TO PHY — 40<> CLK_UNIN_FW — R34 22 5% 1/16W MF 402

R192 22 5% 1/16W MF 402 — 42<> 10<> FW_LINK_CNTL<0>

R183 22 5% 1/16W MF 402 — 42<> 10<> FW_LINK_CNTL<1>

RP18 22 5% 1/16W SM1 — 42<> 10<> FW_LINK_DATA<0> … FW_LINK_DATA<3>

RP12 22 5% 1/16W SM1 — 42<> 10<> FW_LINK_DATA<4> … FW_LINK_DATA<7>

C28 0.1uF 20% 10V CERM 402

R321 1K 5% 1/16W MF 402 — R238 1K 5% 1/16W MF 402

R320 10K 5% 1/16W MF 402 — R27 10K 5% 1/16W MF 402

R25 10K 5% 1/16W MF 402

PWR CLASS = 000
(REQUIRES NO PWR/PROVIDES NO PWR)
(PC0 IS MSB, PC2 IS LSB)

R203 56.2 1% 1/16W MF 402 — R202 56.2 1% 1/16W MF 402

CLEAR OUT ALL PLANES UNDER TRANSFORMERS

FL1 SM

CRITICAL J7 TH-1

42<> 29<> FW_TPO1P — TPO
42<> 29<> FW_TPO1N — TPO#
42<> 29<> FW_TPI1P — TPI
42<> 29<> FW_TPI1N — TPI#
43<> FW_VP — VP
43<> FW_VGND — VGND
NC — CHGND1

R201 56.2 1% 1/16W MF 402 — R200 56.2 1% 1/16W MF 402

C309 12pF 5% 50V CERM 603 — C311 12pF 5% 50V CERM 603

C310 12pF 5% 50V CERM 603 — C312 12pF 5% 50V CERM 603

C355 1uF 20% 10V CERM 805

C260 220pF 5% 50V CERM 805 — R199 4.99K 1% 1/16W MF 402 — FW_TPB0

C186 0.01uF 20% 50V CERM 603 — C174 0.01uF 20% 50V CERM 603

R704 0 5% 1/10W FF 805

Keep 12 pF caps close to FW PHY..

Diodes for transient protection

D27 BAV99DW SOT-363 — 42<> 29<> FW_TPO1P — +3V_FW_VDD 29<> 43<> 29<>

D28 BAV99DW SOT-363 — 42<> 29<> FW_TPI1P — +3V_FW_VDD 29<> 43<> 29<>

D27 BAV99DW SOT-363 — 42<> 29<> FW_TPO1N — +3V_FW_VDD 29<> 43<> 29<>

D28 BAV99DW SOT-363 — 42<> 29<> FW_TPI1N — +3V_FW_VDD 29<> 43<> 29<>

FIREWIRE

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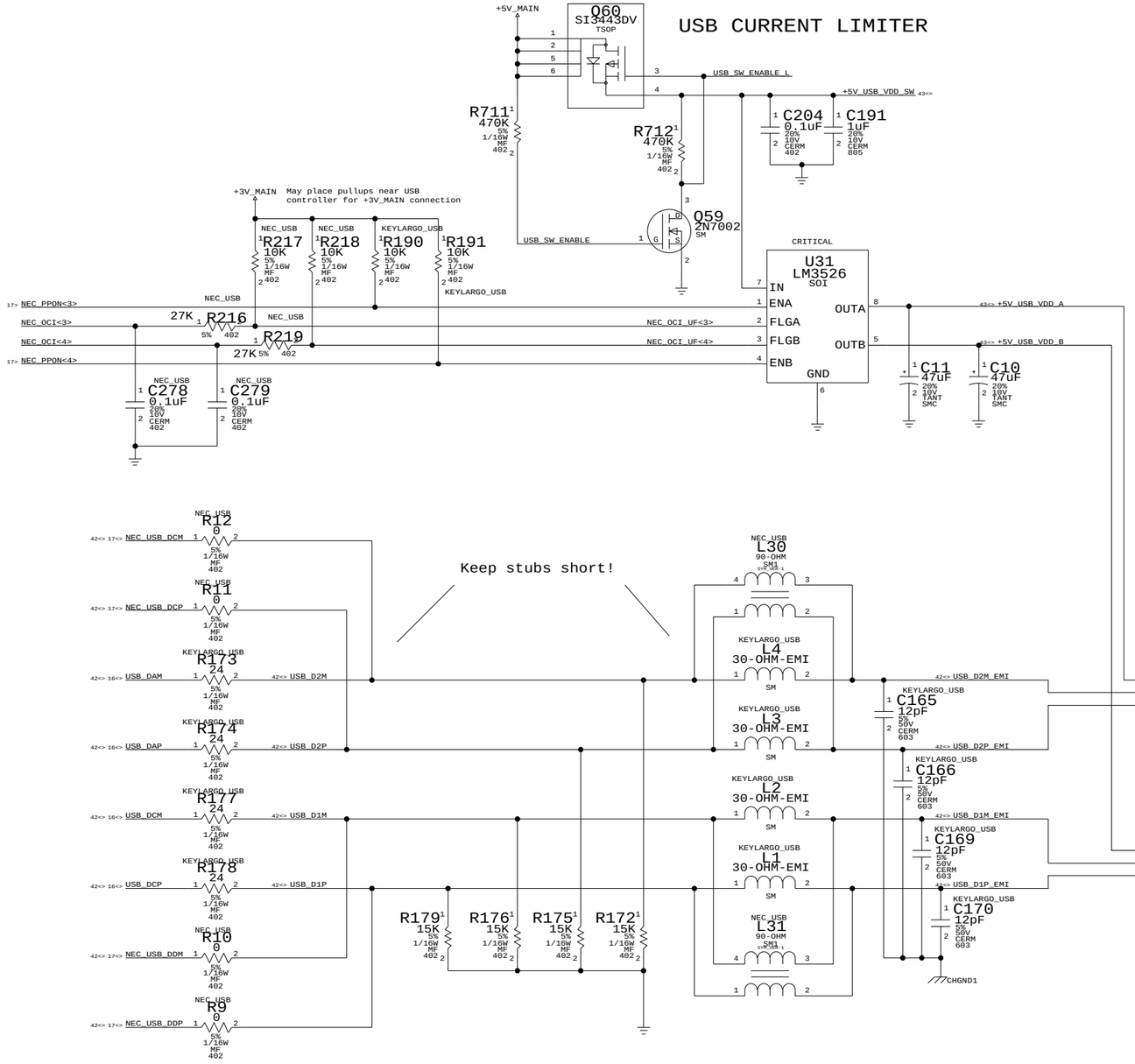
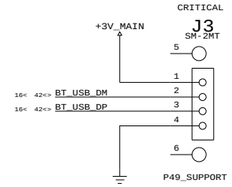
SCALE: NONE	SHT 29 OF 46	

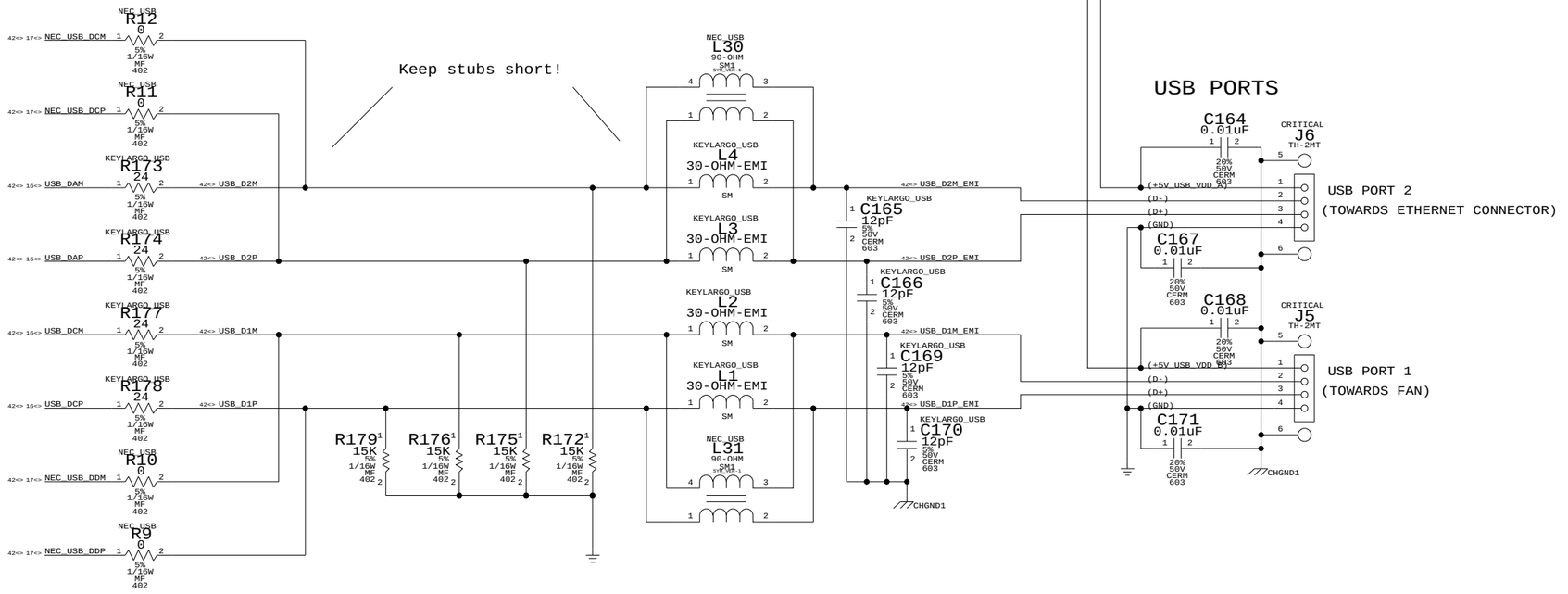
USB CURRENT LIMITER



BLUETOOTH INTERFACE



USB PORTS



USB & BT CONN

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D	051-6403	E
SCALE: NONE	SHT 30 OF 46	

EXTERNAL VIDEO (DVI) INTERFACE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
152S0092	3	IND,0.1UH,+/-10,15MA,SMD	L33,L34,L35	

TMDS TERMINATION

R142 330 5% 1/16W MF 402 — TMDS_DN<0> ↔ TMDS_DP<0>
R136 330 5% 1/16W MF 402 — TMDS_DN<1> ↔ TMDS_DP<1>
R129 330 5% 1/16W MF 402 — TMDS_DN<2> ↔ TMDS_DP<2>
R121 330 5% 1/16W MF 402 — TMDS_CLKN_F ↔ TMDS_CLKP_F
C889 22pF 5% 50V CERM 402 — EMI Filter

TMDS EMC SUPRESSION

L7 165-OHM SM SYM_VER-2
TMDS_CLKN ↔ TMDS_CLKN_F
TMDS_CLKP ↔ TMDS_CLKP_F

DVI DDC CURRENT LIMIT

(55mA requirement per DVI spec)
CRITICAL
+5V_SLEEP → F3 0.5AMP-13.2V SM → +5V_IO_SLEEP → L32 400-OHM-EMI SM-1 → +5V_DDC_SLEEP

ANALOG FILTERING

ATI_B → L38 0.068uH SM → ATI_B_FILTR → OMIT L33 0.068uH SM → VGA_B
ATI_G → L40 0.068uH SM → ATI_G_FILTR → OMIT L35 0.068uH SM → VGA_G
ATI_R → L39 0.068uH SM → ATI_R_FILTR → OMIT L34 0.068uH SM → VGA_R
R434 75 1% 1/16W MF 402; C5 4.7pF +/-0.25pF 50V CERM 603; C192 3.3pF 5% 50V CERM 805
R433 75 1% 1/16W MF 402; C3 4.7pF +/-0.25pF 50V CERM 603; C194 3.3pF 5% 50V CERM 805
R432 75 1% 1/16W MF 402; C4 4.7pF +/-0.25pF 50V CERM 603; C193 3.3pF 5% 50V CERM 805
Place these resistors close to Mobility chip

J4 74320 F-RT-TH (CRITICAL)

TMDS_DN<0> TMDS_DP<0> TMDS_DN<1> TMDS_DP<1> TMDS_DN<2> TMDS_DP<2> TMDS_DN<3> TMDS_DP<3> TMDS_DN<4> TMDS_DP<4> TMDS_DN<5> TMDS_DP<5>
DVI_DDC_CLK (DDC POWER) DVI_DDC_DATA VGA_VSYNC DVI_HPD VGA_R VGA_G VGA_B VGA_HSYNC
TMDS_CLKP_F TMDS_CLKN_F

D24 MBR0530

Isolation required for DVI power switch
+5V_DDC_ISO

R149 4.7K 5% 1/16W MF 402
R137 4.7K 5% 1/16W MF 402
R679 100 5% 1/16W MF 402 — DVI_DDC_CLK_F
R680 100 5% 1/16W MF 402 — DVI_DDC_DATA_F
R681 100 5% 1/16W MF 402 — DVI_HPD_F

C163 0.01uF 20% 50V CERM 603
C189 100pF 5% 50V CERM 402
C188 100pF 5% 50V CERM 402
C868 100pF 5% 50V CERM 402
CHGND2

R710 0 5% 1/16W MF 402 — Place near C5A/B
R709 0 5% 1/16W MF 402 — Place near 3/11/19

3V LEVEL SHIFTERS

+3V_SLEEP
Q21 2N7002DW SOT-363
R168 10K 5% 1/16W MF 402
R167 10K 5% 1/16W MF 402
R186 100K 5% 1/16W MF 402
ATI_DVI_DDC_CLK
Q21 2N7002DW SOT-363
ATI_DVI_DDC_DATA
Q50 2N7002DW SOT-363
ATI_HPD

NOTE: Pulldown for DVI_HPD provided by DVI power switch interface

LCD INTERFACE

POWER SWITCHES

+3V_MAIN
R668 100K 5% 1/16W MF 402; C225 2200pF 5% 50V CERM 603; R8 100K 5% 1/16W MF 402
LCD_DIGON_L; LCD_PWREN_L
TSOP SI3443DV Q23
+3V_LCD_SW
Q56 2N7002DW SOT-363 — ATI_DIGON

LVDS INTERFACE

L43 FERR-250-OHM SM — +3V_LCD
C2 0.001uF 20% 50V CERM 402 — CHGND4B
C6 0.001uF 20% 50V CERM 402 — CHGND4B
J17 F-RT-20143 SM (CRITICAL)
LVDS_L0N LVDS_L0P LVDS_L1N LVDS_L1P LVDS_L2N LVDS_L2P CLKLVDS_N CLKLVDS_P (LVDS_DDC_POWER) NC LVDS_DDC_CLK LVDS_DDC_DATA
C224 0.001uF 20% 50V CERM 402
C223 0.001uF 20% 50V CERM 402 — CHGND4A

100K pull-ups are for no-panel case (development)
Panel has 2K pull-ups
+3V_SLEEP
R170 100K 5% 1/16W MF 402; R169 100K 5% 1/16W MF 402

INVERTER INTERFACE

+PBUS → L10 FERR-1K-OHM-EMI SM → +PBUS_INV
+5V_MAIN
Q1 FDG6324L SC70-6 (CRITICAL)
R7 100K 5% 1/16W MF 402 — ATI_DIGON_L
+5V_INV_UF_SW → L54 400-OHM-EMI SM → +5V_INV_SW
C59 0.001uF 20% 50V CERM 402
C723 10uF 20% 6.3V CERM 1206
C719 0.001uF 20% 50V CERM 402
C709 0.001uF 20% 50V CERM 402 — CHGND7
J21 M-ST-5087 SM (CRITICAL)
+3V_PMU
C1 0.1uF 20% 10V CERM 402
Q1 FDG6324L SC70-6 — ATI_DIGON
74AHC1G02 SC70 U1 02 — ATI_INV_ON_L
BRIGHT_INV_BUF → L53 400-OHM-EMI SM → BRIGHT_INV

S-VIDEO/COMP OUT INTERFACE

Route this GND trace to Mobility chip before tying it into the GND plane
L22 10-OHM-EMI SM — TV_GND1
C162 0.01uF 20% 50V CERM 603
L23 FERR-EMI-100-OHM SM
L19 FERR-EMI-100-OHM SM
L21 FERR-EMI-100-OHM SM
L20 10-OHM-EMI SM — TV_GND2
ATI_Y; ATI_C
R125 75 1% 1/16W MF 402; C178 82pF 5% 50V CERM 805
R123 75 1% 1/16W MF 402; C176 82pF 5% 50V CERM 805
R124 75 1% 1/16W MF 402; C177 82pF 5% 50V CERM 805
C172 82pF 5% 50V CERM 805
C159 82pF 5% 50V CERM 805
C161 82pF 5% 50V CERM 805
C160 0.01uF 20% 50V CERM 603
Place these resistors close to Mobility chip
Route this GND trace to Mobility chip before tying it into the GND plane
J1 TH-2MT (CRITICAL) — TV_C, TV_Y, TV_COMP
CHGND2

VIDEO CONNECTORS

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CARDSLOT/EIDE SERIES TERMINATION

THESE LINES ARE SHARED BETWEEN THE CARDSLOT AND EIDE INTERFACES
PLEASE PLACE THESE TERMINATORS CLOSE TO KEYLARGO AND MINIMIZE THE LENGTH OF THE T

Place resistor packs
CLOSE TO KEY LARGO

EIDE_DATA<2>	1	RP47 33 5% 1/16W SM1	8	CSLOT_DATA<2>	
EIDE_DATA<1>	2		7	CSLOT_DATA<1>	
EIDE_DATA<0>	3		6	CSLOT_DATA<0>	
EIDE_DATA<3>	4		5	CSLOT_DATA<3>	
EIDE_DATA<6>	1	RP45 33 5% 1/16W SM1	8	CSLOT_DATA<6>	
EIDE_DATA<7>	2		7	CSLOT_DATA<7>	
EIDE_DATA<4>	3		6	CSLOT_DATA<4>	
EIDE_DATA<5>	4		5	CSLOT_DATA<5>	
EIDE_DATA<11>	1	RP43 33 5% 1/16W SM1	8	CSLOT_DATA<11>	
EIDE_DATA<9>	2		7	CSLOT_DATA<9>	
EIDE_DATA<10>	3		6	CSLOT_DATA<10>	
EIDE_DATA<8>	4		5	CSLOT_DATA<8>	
EIDE_DATA<15>	1	RP41 33 5% 1/16W SM1	8	CSLOT_DATA<15>	
EIDE_DATA<13>	2		7	CSLOT_DATA<13>	
EIDE_DATA<14>	3		6	CSLOT_DATA<14>	
EIDE_DATA<12>	4		5	CSLOT_DATA<12>	
EIDE_ADDR<0>	1	RP50 33 5% 1/16W SM1	8	CSLOT_ADDR<0>	
EIDE_ADDR<2>	2		7	CSLOT_ADDR<2>	
EIDE_ADDR<1>	3		6	CSLOT_ADDR<1>	
EIDE_CS1FX_L	4		5	CSLOT_CS1FX_L	

EIDE_CS3FX_L — R75 33 5% 1/16W MF 402 — CSLOT_CS3FX_L

PLACE TERMINATORS NEAR KEY LARGO

EIDE_DATA<8>	1	RP42 33 5% 1/16W SM1	8	EIDE_DB_<8>
EIDE_DATA<10>	2		7	EIDE_DB_<10>
EIDE_DATA<9>	3		6	EIDE_DB_<9>
EIDE_DATA<11>	4		5	EIDE_DB_<11>
EIDE_DATA<12>	1	RP40 33 5% 1/16W SM1	8	EIDE_DB_<12>
EIDE_DATA<14>	2		7	EIDE_DB_<14>
EIDE_DATA<13>	3		6	EIDE_DB_<13>
EIDE_DATA<15>	4		5	EIDE_DB_<15>
EIDE_DB_<2>	1	RP46 33 5% 1/16W SM1	8	EIDE_DATA<2>
EIDE_DB_<1>	2		7	EIDE_DATA<1>
EIDE_DB_<0>	3		6	EIDE_DATA<0>
EIDE_DB_<3>	4		5	EIDE_DATA<3>
EIDE_DB_<6>	1	RP44 33 5% 1/16W SM1	8	EIDE_DATA<6>
EIDE_DB_<7>	2		7	EIDE_DATA<7>
EIDE_DB_<4>	3		6	EIDE_DATA<4>
EIDE_DB_<5>	4		5	EIDE_DATA<5>
EIDE_CS1FX_L	1	RP49 33 5% 1/16W SM1	8	EIDE_CS1FX_L_OPU
EIDE_ADDR<1>	2		7	EIDE_ADDR_<1>
EIDE_ADDR<2>	3		6	EIDE_ADDR_<2>
EIDE_ADDR<0>	4		5	EIDE_ADDR_<0>

R74 10K 5% 1/16W MF 402

EIDE_CS3FX_L — R94 33 5% 1/16W MF 402 — EIDE_CS3FX_L_OPU

Place near Key Largo

EIDE0_DMARQ	R99 82 5% 1/16W MF 402	EIDE0_DMA_RQ
EIDE0_DMACK_L	R95 22 5% 1/16W MF 402	EIDE0_DMA_ACK_L
EIDE0_RD_L	R76 22 5% 1/16W MF 402	EIDE0_READ_L
EIDE0_WR_L	R93 22 5% 1/16W MF 402	EIDE0_WR_L_OPU
EIDE_IOCHRDY	R92 82 5% 1/16W MF 402	EIDE_IO_CHRDY
EIDE0_INT	R101 82 5% 1/16W MF 402	EIDE0_INTR
EIDE0_RST_L	R77 33 5% 1/16W MF 402	EIDE0_RST_L_OPU

CARDSLOT (WIRELESS) INTERFACE

+3V_SLEEP

RP39 10K 5% 1/16W SM1 — RP38 10K 5% 1/16W SM1

CRITICAL
J25
SM-M
M70SM_5MM

CSLOT_DATA<3>	69	Card Detect #1
CSLOT_DATA<4>	68	CSLOT_DATA<11>
CSLOT_DATA<5>	67	CSLOT_DATA<12>
CSLOT_DATA<6>	66	CSLOT_DATA<13>
CSLOT_DATA<7>	65	CSLOT_DATA<14>
CSLOT_CE1_L	64	CSLOT_DATA<15>
CSLOT_ADDR<10>	63	CSLOT_CE2_L
CSLOT_CS1FX_L	62	Voltage Sense #1
CSLOT_ADDR<11>	61	CSLOT_IORD_L
CSLOT_ADDR<9>	60	CSLOT_IOWR_L
CSLOT_ADDR<8>	59	
CSLOT_ADDR<13>	58	
CSLOT_ADDR<14>	57	
CSLOT_CS3FX_L	56	
CSLOT_IRQ_L	55	
	54	
	53	
(ADDR<16>)	52	
CSLOT_ADDR<15>	51	
CSLOT_ADDR<12>	50	
CSLOT_ADDR<7>	49	
CSLOT_ADDR<6>	48	(VOLTAGE SENSE #2)
CSLOT_ADDR<5>	47	CSLOT_RESET
CSLOT_ADDR<4>	46	CSLOT_IOWAIT_L
CSLOT_ADDR<3>	45	(INPUT PORT ACK)
CSLOT_ADDR<2>	44	CSLOT_REG_L
CSLOT_ADDR<1>	43	(SPEAKER)
CSLOT_ADDR<0>	42	(CARD STATUS CHANGED)
CSLOT_DATA<0>	41	CSLOT_DATA<8>
CSLOT_DATA<1>	40	CSLOT_DATA<9>
CSLOT_DATA<2>	39	CSLOT_DATA<10>
(IOCS16_L)	38	+5V_TOL
	37	
	36	
	35	

+5V_SLEEP — R534 470 5% 1/16W MF 402

OPTICAL DRIVE INTERFACE

+5V_SLEEP

R66 100K 5% 1/16W MF 402 — R81 10K 5% 1/16W MF 402 — R80 10K 5% 1/16W MF 402

CRITICAL
J26
SM-M

NC	50	NC
NC	49	NC
EIDE_DB_<8>	48	EIDE0_RST_L_OPU
EIDE_DB_<9>	47	EIDE_DB_<7>
EIDE_DB_<10>	46	EIDE_DB_<6>
EIDE_DB_<11>	45	EIDE_DB_<5>
EIDE_DB_<12>	44	EIDE_DB_<4>
EIDE_DB_<13>	43	EIDE_DB_<3>
EIDE_DB_<14>	42	EIDE_DB_<2>
EIDE_DB_<15>	41	EIDE_DB_<1>
EIDE0_DMA_RQ	40	EIDE_DB_<0>
EIDE0_READ_L	39	
	38	EIDE0_WR_L_OPU
EIDE0_DMA_ACK_L	37	EIDE_IO_CHRDY
PIN 30 NOT USED	36	EIDE0_INTR
PIN 32 NOT USED	35	EIDE_ADDR_<1>
EIDE_ADDR_<2>	34	EIDE_ADDR_<0>
EIDE_CS3FX_L_OPU	33	EIDE_CS1FX_L_OPU
	32	NC
	31	
	30	
NC	29	NC
	28	
	27	
	26	
	25	

R65 20K 5% 1/16W MF 402 — R82 10K 5% 1/16W MF 402

INTERNAL HARD DRIVE INTERFACE

UIDE_DATA<0>	1	RP54 33 5% 1/16W SM1	8	HD_DATA<0>
UIDE_DATA<1>	2		7	HD_DATA<1>
UIDE_DATA<2>	3		6	HD_DATA<2>
UIDE_DATA<3>	4		5	HD_DATA<3>
UIDE_DATA<4>	1	RP51 33 5% 1/16W SM1	8	HD_DATA<4>
UIDE_DATA<5>	2		7	HD_DATA<5>
UIDE_DATA<6>	3		6	HD_DATA<6>
UIDE_DATA<7>	4		5	HD_DATA<7>
UIDE_DATA<8>	1	RP52 33 5% 1/16W SM1	8	HD_DATA<8>
UIDE_DATA<9>	2		7	HD_DATA<9>
UIDE_DATA<10>	3		6	HD_DATA<10>
UIDE_DATA<11>	4		5	HD_DATA<11>
UIDE_DATA<12>	1	RP53 33 5% 1/16W SM1	8	HD_DATA<12>
UIDE_DATA<13>	2		7	HD_DATA<13>
UIDE_DATA<14>	3		6	HD_DATA<14>
UIDE_DATA<15>	4		5	HD_DATA<15>
UIDE_ADDR<0>	1	RP55 33 5% 1/16W SM1	8	HD_ADDR<0>
UIDE_ADDR<1>	2		7	HD_ADDR<1>
UIDE_ADDR<2>	3		6	HD_ADDR<2>
UIDE_CS1FX_L	4		5	HD_CS1_L

R595 10K 5% 1/16W MF 402

UIDE_CS3FX_L	R605 33 5% 1/16W MF 402	HD_CS3_L
UIDE_RST_L	R594 33 5% 1/16W MF 402	HD_RESET_L
UIDE_DMACK_L	R600 22 5% 1/16W MF 402	HD_DMACK_L
UIDE_DIOR_L	R598 22 5% 1/16W MF 402	HD_DIOR_L
UIDE_DIOW_L	R597 22 5% 1/16W MF 402	HD_DIOW_L

R599 10K 5% 1/16W MF 402 — R593 10K 5% 1/16W MF 402 — R601 100K 5% 1/16W MF 402

CRITICAL
J27
SM-M
M50SM_5MM

+5V_HD_SLEEP

HD_RESET_L	26	
	25	
HD_DATA<7>	27	HD_DATA<8>
HD_DATA<6>	24	HD_DATA<9>
HD_DATA<5>	23	HD_DATA<10>
	22	
HD_DATA<4>	21	HD_DATA<11>
HD_DATA<3>	20	HD_DATA<12>
HD_DATA<2>	19	HD_DATA<13>
	18	
HD_DATA<1>	17	HD_DATA<14>
HD_DATA<0>	16	HD_DATA<15>
	15	
HD_DMARQ	14	
HD_DIOW_L	13	
HD_DIOR_L	12	
HD_IOCHRDY	11	
HD_DMACK_L	10	
HD_INTRQ	9	
HD_ADDR<1>	8	
HD_ADDR<0>	7	NC
HD_CS1_L	6	HD_ADDR<2>
	5	HD_CS3_L
	4	
	3	
	2	NC
	1	NC

R602 10K 5% 1/16W MF 402 — R596 20K 5% 1/16W MF 402

SERIAL DEBUG INTERFACE

May repin connector as necessary

+5V_MAIN

SERIAL_DEBUG
CRITICAL
J12
M-ST-5087
SM

COMM_TXD_L	1	10	COMM_DTR_L
COMM_TRXC	2	9	COMM_RTS_L
	3	8	
COMM_GPIO_L	4	7	COMM_RXD
	5	6	

MODEM BOARD INTERFACE

May repin connector as necessary

+5V_MAIN

CRITICAL
J24
M-ST-5087
SM

	1	10	
KL_I2C_CLK	2	9	KL_I2C_DATA
COMM_RING_DET_L	3	8	MODEM_USB_DP
COMM_SHUTDOWN	4	7	MODEM_USB_DM
	5	6	COMM_RESET_L

+3V_MAIN

C751 10uF N20P80% 16V CERM 1206 — C752 0.1uF 20% 16V CERM 402 — R571 10K 5% 1/16W MF 402

Place near pin 4 of modem connector

+5V_MAIN

C765 0.1uF 20% 16V CERM 402 — C771 10uF N20P80% 16V CERM 1206

INTERNAL I/O CONNECTORS

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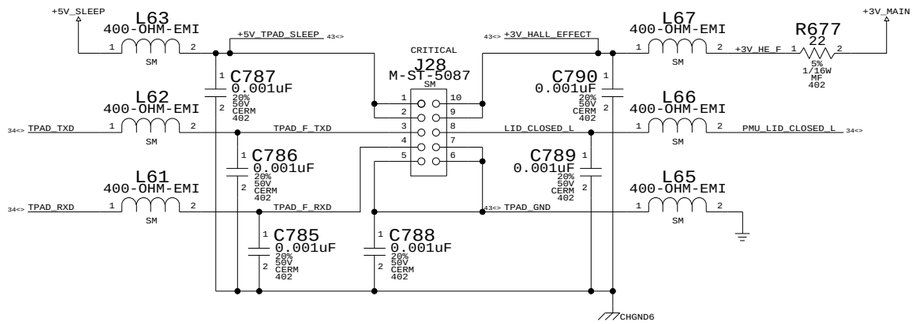
APPLE COMPUTER INC.

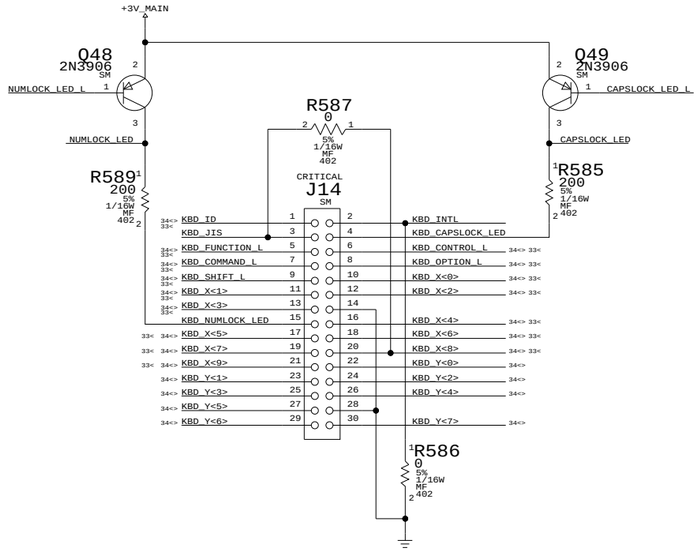
SIZE	DRAWING NUMBER	REV.
D	051-6403	E
SCALE: NONE	SHT 32 OF 46	

TRACKPAD/SLEEP SWITCH INTERFACE

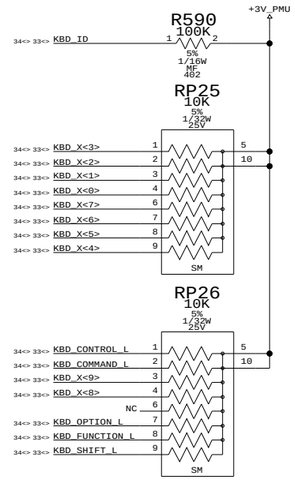
Place discretes close to connector



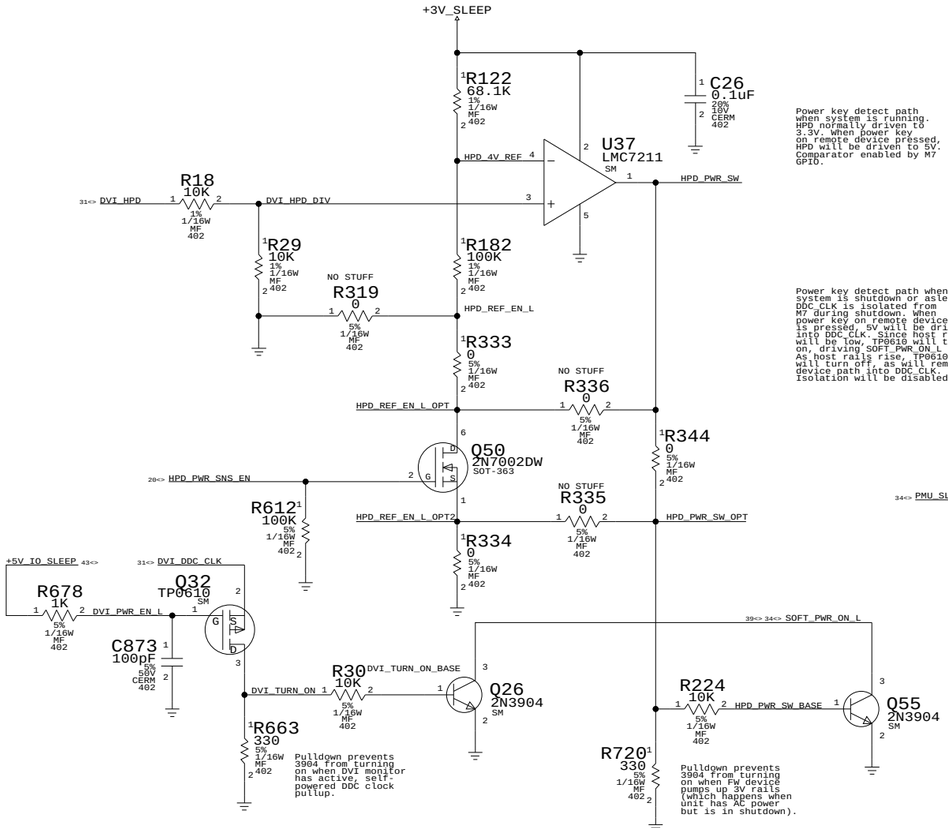
KEYBOARD INTERFACE



KEYBOARD PULLUPS



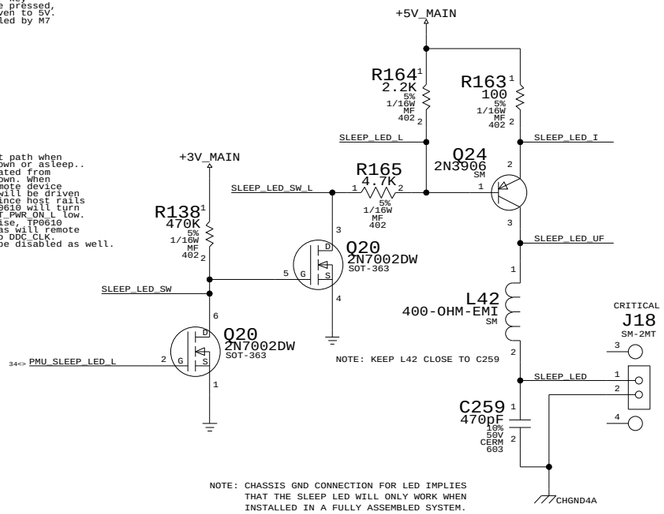
DVI POWER SWITCH



SLEEP LED

Power key detect path when system is running. HPD normally driven to 3.3V. When power key on remote device pressed, HPD will be driven to 5V. Comparator enabled by M7 GPIO.

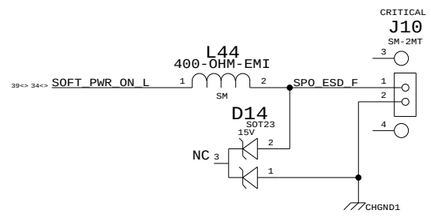
Power key detect path when system is shutdown or asleep.. DDC_CLK is isolated from M7 during shutdown. When power key on remote device is pressed, 5V will be driven into DDC_CLK. Since host rails will be low, TPD610 will turn on, driving SOFT_PWR_ON_L low. As host rails rise, TPD610 will turn off, as will remote device path into DDC_CLK. Isolation will be disabled as well.



CHARGE LED SUPPORT

(MOVED TO INVERTER)

POWER BUTTON INTERFACE



NOTE: CURRENT RETURN PATH IS VIA CHGND1, Rxx, AND Lxx AT DC JACK

PMU INTERFACES

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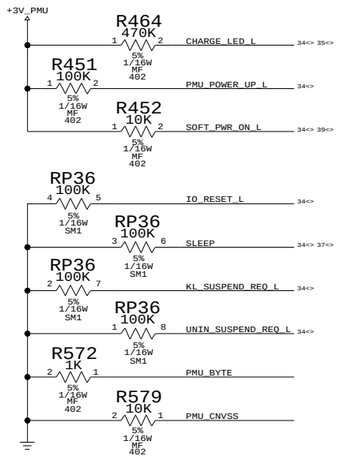
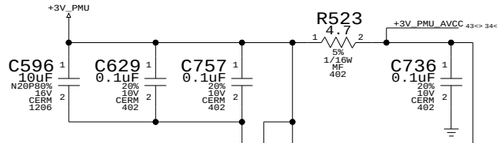
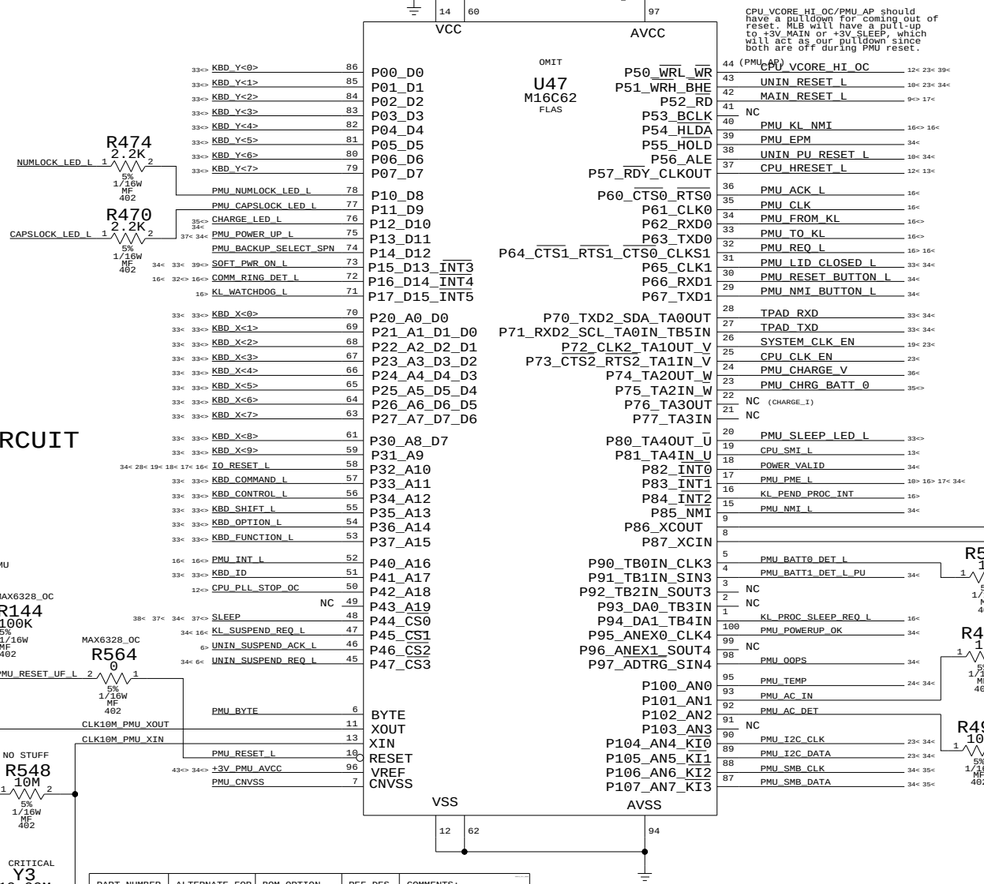
SIZE	DRAWING NUMBER	REV.
D	051-6403	E
SCALE: NONE	SHT 33 OF 46	





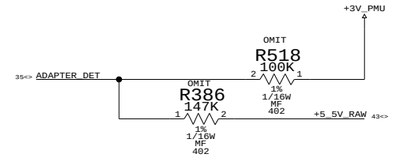
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1008	1	PMU,SW Image 81	U47	

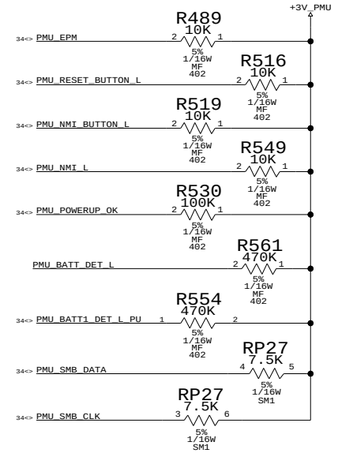


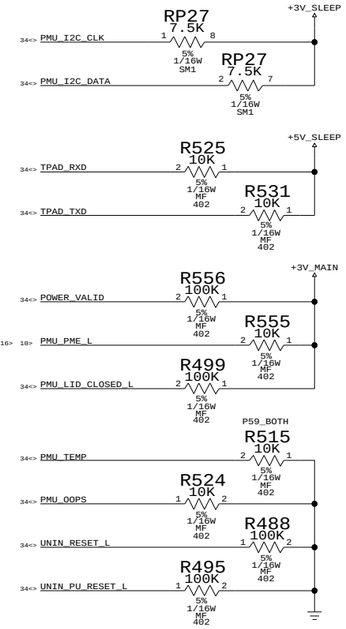
CPU_VCORE_HI_OC/PMU_AP should have a pulldown for coming out of reset. MLB will have a pull-up to +3V_MAIN or +3V_SLEEP, which will act as our pulldown since both are off during PMU reset.

44	(PMU_AP)	CPU_VCORE_HI_OC
43		UNIN_RESET_L
42		MAIN_RESET_L
41	NC	
40		PMU_KL_NMI
39		PMU_EPM
38		UNIN_PU_RESET_L
37		CPU_HRESET_L
36		PMU_ACK_L
35		PMU_CLK
34		PMU_FROM_KL
33		PMU_TO_KL
32		PMU_REQ_L
31		PMU_LID_CLOSED_L
30		PMU_RESET_BUTTON_L
29		PMU_NMI_BUTTON_L
28		TPAD_RXD
27		TPAD_TXD
26		SYSTEM_CLK_EN
25		CPU_CLK_EN
24		PMU_CHARGE_V
23		PMU_CHRG_BATT_0
22	NC (CHARGE_I)	
21	NC	
20		PMU_SLEEP_LED_L
19		CPU_SMI_L
18		POWER_VALID
17		PMU_PME_L
16		KL_PEND_PROC_INT
15		PMU_NMI_L
9		CLK32K_PMU_XOUT
8		CLK32K_PMU_XIN
5		PMU_BATT0_DET_L
4		PMU_BATT1_DET_L_PU
3	NC	
2	NC	
1		KL_PROC_SLEEP_REQ_L
100		PMU_POWERUP_OK
99	NC	
98		PMU_OOPS
95		PMU_TEMP
93		PMU_AC_IN
92		PMU_AC_DET
91	NC	
90		PMU_I2C_CLK
89		PMU_I2C_DATA
88		PMU_SMB_CLK
87		PMU_SMB_DATA

A29 & Q11 ADAPTOR OPTION



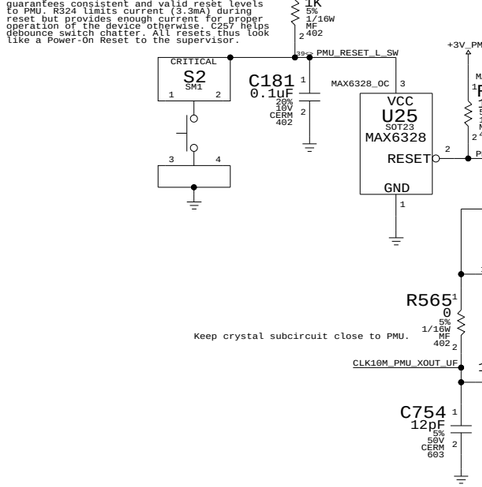




UNDERVOLTAGE RESET CIRCUIT

PMU RESET SWITCH

Placing switch on input to reset supervisor guarantees consistent and valid reset levels to PMU. R324 limits current (3.3mA) during reset but provides enough current for proper operation of the device otherwise. C257 helps debounce switch chatter. All resets thus look like a Power-On Reset to the supervisor.



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0704	197S0604		Y3	Alt crystal size

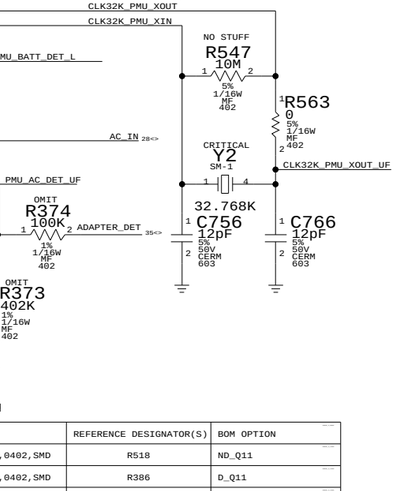
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
705S0051	705S0040		S2	

NOTE: PMU Undervoltage circuit supports MAX6328 (open-drain) as well as MAX6326 (push-pull)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S0255	1	IC, MAX6326 RESET, 2.63V, SOT23-3	U25	MAX6326_PP
116S1473	1	RES, 4.7K, 5%, 1/16W, MF, 402	R564	MAX6326_PP

R316 IS NO STUFFED FOR MAX6326_PP!!!

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0809	353S0255	MAX6326_PP	U25	MAX809S



A29 & Q11 ADAPTOR OPTION

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S1005	1	RES,1/16W,100K OHM,0402,SMD	R518	ND_Q11
114S1215	1	RES,1/16W,121K OHM,0402,SMD	R386	D_Q11
114S7324	1	RES,1/16W,73.2K OHM,0402,SMD	R374	D_Q11
116S1000	1	RES,1/16W,0 OHM,0402,SMD	R374	ND_Q11
114S2875	1	RES,1/16W,287K OHM,0402,SMD	R373	D_Q11

PMU Interface

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SIZE	DRAWING NUMBER	REV.
D	051-6403	E

SCALE	SHT	OF
NONE	34	46

DC POWER INPUT

(POWER JACK, ETC. ON DC INPUT BOARD)

CRITICAL
J20
53780
F-RT-SM

ADAPTER_DET 34<
CHARGE_LED_L 34<> 34<

C25 0.01uF 20% 50V CERM 603 — CHGND1

C216 0.01uF 20% 50V CERM 603 — CHGND1

DC INRUSH LIMITER

+ADAPTER 43<> 37<

R237 10K 1% 1/16W MF 402

R243 330K 5% 1/16W MF 402

C341 0.1uF 20% 50V CERM 805

Q30 SI4435DY SOI (S1 S2 S3 GATE D1 D2 D3 D4)

+ADAPTER_SW 36<> 43<>

AC_ENABLE_GATE

R261 470K 5% 1/16W MF 402

AC_ENABLE_L

+3V_PMU

R139 102K 1% 1/16W MF 402

R126 100K 1% 1/16W MF 402

C184 0.01uF 20% 10V CERM 402

U27 LMC7211 SM

1V20_REF

PBUS_DIV

AC_IN 28<>

Q29 2N7002 SM

R147 10K 1% 1/16W MF 402

R141 57.6K 1% 1/16W MF 402

R140 1M 5% 1/16W MF 402

R262 470K 5% 1/16W MF 402

GREATER THAN 13.5V DETECT

DC POWER SEQUENCING

D2 B540C SM

INPUT14_24V_SW 43<> -> TO CHARGER

+3V_PMU

C185 0.01uF 20% 10V CERM 402

R128 97.6K 1% 1/16W MF 402

1V20_REF

13_5V_DET

U26 LMC7211 SM

R127 1M 5% 1/16W MF 402

NO STUFF C190 0.1uF 20% 10V CERM 402

R131 10K 1% 1/16W MF 402

DP5 BAS16TW SOT-363

R410 0 5% 1/16W MF 402 — RUN/SS

GTR_THAN_13_0V 36<>

CRITICAL
Q31 FDG6324L SC70-6

+3V_PMU

R348 330K 5% 1/16W MF 402

3V_PMU_CHGR 36<> 43<>

PMU_CHRG_EN_L

Q31 FDG6324L SC70-6

BATTERY CONNECTOR

CRITICAL
J15
M-ST
TH

43<> BATT_POS
BATT_IN_PD
BATT_CLK
BATT_DATA
PMU_BATT_DET_L
43<> BATT_NEG

L16 FERR-50-OHM SM — BATT_POS_F 37<> 43<>

L17 FERR-EMI-100-OHM SM — PMU_SMB_CLK 34<>

L18 FERR-EMI-100-OHM SM — PMU_SMB_DATA 34<>

L64 FERR-50-OHM SM

R592 470K 5% 1/16W MF 402

LOW-VOLTAGE CHARGE LIMITER

R48 100 5% 1W FF 2512 — 43<> BATT_RES

R54 100 5% 1W FF 2512

R60 100 5% 1W FF 2512

D8 30BQ040 SM

Q12 SI4435DY SOI (S1 S2 S3 GATE D1 D2 D3 D4)

R492 39.2K 1% 1/16W MF 402

BYPASS_R_GATE

R513 35.7K 1% 1/16W MF 402

BYPASS_R_L

+3V_PMU

C731 0.01uF 20% 16V CERM 402

R522 665K 1% 1/16W MF 402

R514 100K 1% 1/16W FF 603

BATT_OK_REF

BATT_OK

U49 LMC7211 SM

Q43 2N7002 SM

BATT_V_GOOD

C806 0.047uF 5% 16V CERM 603

R521 100K 1% 1/16W FF 603

R493 100K 1% 1/16W FF 603

BATTERY SWITCH

BATT_LINE 43<> 36< <-> TO SYSTEM <-> FROM CHARGER

NO STUFF D26 S1A-13 SMA

Q8 FDS6975 SM (S1 S2 S3 G1 G2 G3 D1 D2 D3)

NO STUFF R676 0 5% 1/16W MF 402

43<> BATT_FET_SW

R669 470K 5% 1/16W MF 402

R42 470K 5% 1/16W MF 402

BATT_FET2_GATE

BATT_FET_GATE

C869 0.01uF 20% 16V CERM 402

R670 330K 5% 1/16W MF 402

C64 0.01uF 20% 16V CERM 402

R43 330K 5% 1/16W MF 402

BATT_ENABLE_L

+3V_PMU

R496 10K 5% 1/16W MF 402

Q35 2N7002DW SOT-363

ADAPTER_PWR_SW

R449 10K 1% 1/16W MF 402

BATT_FET_DRAIN

R450 665K 1% 1/16W MF 402

DP3 BAS40TW SOT-363

Q35 2N7002DW SOT-363

BATT_RC

C615 0.047uF 5% 16V CERM 603

CHRG_DSCHG_L

Q57 2N7002DW SOT-363

36<> ZENER_GTR_THAN_18V

Q57 2N7002DW SOT-363

DP3 BAS40TW SOT-363

PMU_CHRG_BATT_0 34<>

ADAPTER & BATTERY INTERFACES

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SIZE D | DRAWING NUMBER 051-6403 | REV: E

SCALE NONE | SHT 35 OF 46

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
376S0254	1	XSTR,MOSFET,N-CH,30V,.0135 OHM,10A,8P,SO	Q6	CRITICAL	
376S0104	1	XSTR,FET,N-CH,30V,14A,.012 OHM,8P,SOIC	Q7	CRITICAL	

BATTERY CHARGING CURRENT LIMIT

TO BATTERY <-
FROM BATTERY ->

BATT_LINE — R1 0.025 1% 1W MF 2512 (CRITICAL) — BATT_ISNS — F1 5AMP-125V SM-2 — PBUS hold-up caps — +PBUS -> TO SYSTEM

C13 220uF 20% 25V ELEC SM
C36 100uF 20% 35V ELEC SM-1

3V_PMU_CHGR
IBATT_RC_COMP — C517 0.1uF 20% 10V CERM 402 — R378 1K 1% 1/16W MF 402
PWRBUS_14_24V — C22 0.01uF 20% 50V CERM 603
R363 20.5K 1% 1/16W MF 402
R263 10K 1% 1/16W MF 402
U3 MAX4172 SOI (V+, RS-, RS+, PG, NC1, OUT, NC2, GND)
IBATT_FB
IBATT_SERVO
IBATTX0_65
DP2 BAS16TW SOT-363
ITH 1625
ICHRG_REG
U40 LMC6462 SOI
R379 15.8K 1% 1/16W MF 402
R188 2.61K 1% 1/16W MF 402

TO/FROM BACKUP BATTERY <->
J13 SM-2MT (CRITICAL)
BBATT_ENABLE

ADAPTER CURRENT LIMIT

-> FROM ADAPTER

INPUT14_24V_SW — R20 0.025 1% 1W MF 2512 (CRITICAL) — PWRBUS_14_24V

KEEP VIN/TK LOOP SHORT

CONNECT LTC1625 TK PIN AT TOP-SIDE FETS

3V_PMU_CHGR
C342 0.1uF 20% 10V CERM 402
R337 42.2K 0.1% 1/16W MF 603
IAC_RC_COMP — C343 0.1uF 20% 10V CERM 402
R264 1K 1% 1/16W MF 402
IAC_FB
IINX0_62
R265 10K 1% 1/16W MF 402
1_02V_AUX
R266 2.21K 0.1% 1/16W MF 603
OMIT R287 82.5K 1% 1/16W MF 603
R310 42.2K 0.1% 1/16W FF 603
CURRENT_ADJ
ADAPTER_I_REG
C202 0.01uF 20% 50V CERM 603
U30 MAX4172 SOI (V+, RS+, RS-, NC1, PG, NC2, OUT, GND)

LTC1625_EXTVCC — C890 0.1uF 20% 10V CERM 402
R414 1 5% 1/16W MF 603
R427 150 1% 1/16W MF 603
1625_VIN
RUN/SS — 1625_COMP
C569 0.1uF 20% 25V CERM 805
R41 4.99K 1% 1/16W MF 402
C597 4700pF 5% 25V CERM 603
COMP_RC
C61 470pF 10% 50V CERM 603
C65 4700pF 5% 25V CERM 603
R444 0 5% 1/16W MF 603 — 1625_SGND

U17 LTC1625 (EXTVCC, VIN, SSOP, BG, TK, TG, SYNC, VOSENSE, RUN/SS, INTVCC, ITH, FCB, BOOST, VPROG, SW, SGND, PGND)
1625_INTVCC
1625_TG
D4 MBR0540 (SM)
1625_BST
C49 0.33uF 20% 16V CERM 805
R346 0 5% 1/16W MF 402
1625_BST_F
1625_BG
C63 4.7uF 10% 10V TANT SMB
NO STUFF C401 0.0022uF 10% 50V CERM 402
Q6 SI4410DY SOI (CRITICAL OMIT)
Q7 IRF7822 SM (CRITICAL OMIT)
1625_VFB

CHGR_VSW — L11 15uH SM-2 — CHGR_OUT
D5 MBRS140T3 SM
C37 100uF 20% 35V ELEC SM-1
C418 1.5uF 20% 50V CERM 1812
C372 1.5uF 20% 50V CERM 1812
C417 1.5uF 20% 50V CERM 1812
C371 1.5uF 20% 50V CERM 1812
C483 1.5uF 20% 50V CERM 1812
C307 1.5uF 20% 50V CERM 1812
C484 1.5uF 20% 50V CERM 1812
C308 1.5uF 20% 50V CERM 1812
C102 4.7uF 20% 25V CERM 1812
C85 4.7uF 20% 25V CERM 1812
C124 100uF 20% 35V ELEC SM-1
Q17 SI4435DY SOI (D4, D3, D2, D1, S3, S2, S1, GATE)
R560 470K 5% 1/16W MF 402
R469 49.3K 0.1% 1/16W FF 603
PBUS_DIV1
R459 100K 1% 1/16W MF 805
R468 11.3K 0.1% 1/16W MF 805
R467 150 1% 1/16W MF 603
BF_FET_G
R553 330K 5% 1/16W MF 402
C749 0.01uF 20% 16V CERM 402
FET_DRAIN
Q44 2N7002 SM (D, G, S)
R497 330K 5% 1/16W MF 402
GTR_THAN_13_0V
DP5 BAS16TW SOT-363
PWR_STABLE_DELAY
C735 0.047uF 5% 16V CERM 603

VCHRG
Q40 2N7002 SM (D, G, S)
PMU_CHARGE_V

D16 1N5248B SOT23
+ADAPTER_SW
ZENER_GTR_THAN_18V
Q27 2N7002 SM (D, G, S)
R198 3.3K 5% 1/16W MF 402
C891 0.47uF 20% 16V CERM 805

ADJUSTS CURRENT LIMIT
FOR 15V AIRLINE ADAPTER
VS. 24V WALL ADAPTER

Provides power to LTC1625 if on an adapter and after all rails have been brought up. This will improve efficiency of LTC1625 since external switcher is used instead of internal LDO.

+5V_MAIN
Q58 FDG6324L SC70-6 (CRITICAL) — LTC1625_EXTVCC
R686 470K 5% 1/16W MF 402
EXTVCC_EN_L
DP2 BAS16TW SOT-363
R685 100K 5% 1/16W MF 402
GTR_THAN_13_0V — GTR_THAN_13V_RC
Q58 FDG6324L SC70-6 (CRITICAL)
C874 4.7uF N20P80% 16V CERM 805

1_02V_AUX
+3V_PMU
PMU_AC_DET_UF
U44 LMC7211 SM
R362 4.32K 1% 1/16W MF 402
R387 10.2K 1% 1/16W MF 402
R389 499K 1% 1/16W MF 402
C433 0.1uF 20% 10V CERM 402
R390 10K 5% 1/16W MF 402
Q63 2N7002DW SOT-363
R409 53.6K 1% 1/16W MF 603
Q63 2N7002DW SOT-363

ADDITIONAL POWER LIMITING CIRCUIT FOR P88 DVT2

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
110S8254	1	RES,82.5K,1%,1/16W,MF,402	R287	M_S_G
103S0559	1	RES,37.4K,0.1%,1/16W,MF,402	R287	S_B_G

PRIMARY REGULATOR

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PMU SUPPLY

DCDC_EN TRUTH TABLE

PMU_POWER_UP_L	SLEEP	DCDC_EN	State
0	0	1	Run
X	1	1	Sleep
1	0	0	Shutdown

ROUTE AS PAIR SHORT TRACE

NOTE: Place Rsense RC filter (R478/C660) close to MAX785 pins

ROUTE AS PAIR SHORT TRACE

+5V_SLEEP LOADS

1) Fan - High speed supply
2) Headphone amplifier
3) Modem - call progress ADC
4) DVD ROM
5) CardSlot - 5V tolerance
6) Trackpad

SLEEP LEVEL SHIFTER (3V -> 5V)

+3V_SLEEP LOADS

1) CPU PLL Config Control
2) Fan - Low speed supply
3) KeyLargo - IIC Pull-ups & Oscillator
4) CardBus - Card detect pull-ups
5) Mobility Radeon - Oscillator
6) C5005 - Core, I/O
7) IRDA - VCC, LEDA, FIR_SEL pull-up
8) LVDS DDC Pull-ups
9) VGA MonID Level Shifters & Pull-ups
10) CardSlot
11) PMU - IIC Pull-ups

BOOTSTRAP SYSTEM FROM ADAPTER OR BATTERY

PROVIDES PATH TO +3V_PMU FROM BACKUP BATTERY WHEN PRESENT

3.3V/5V SUPPLIES

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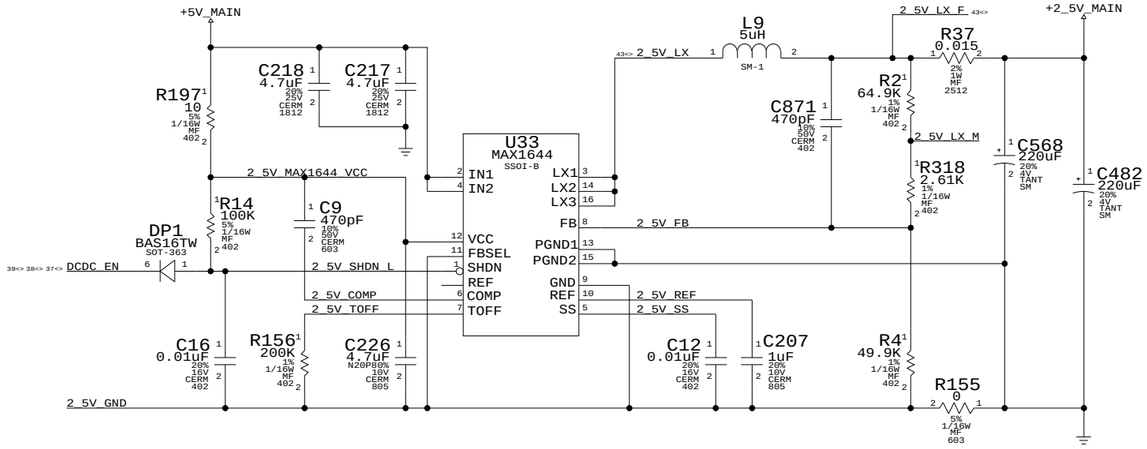
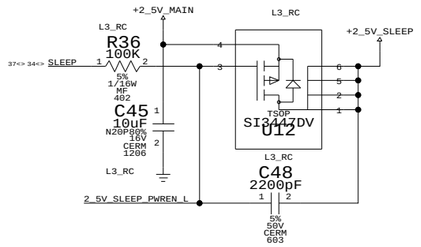
SCALE NONE | SHT 37 OF 46

2.5V SWITCHER



+2_5V_MAIN LOADS

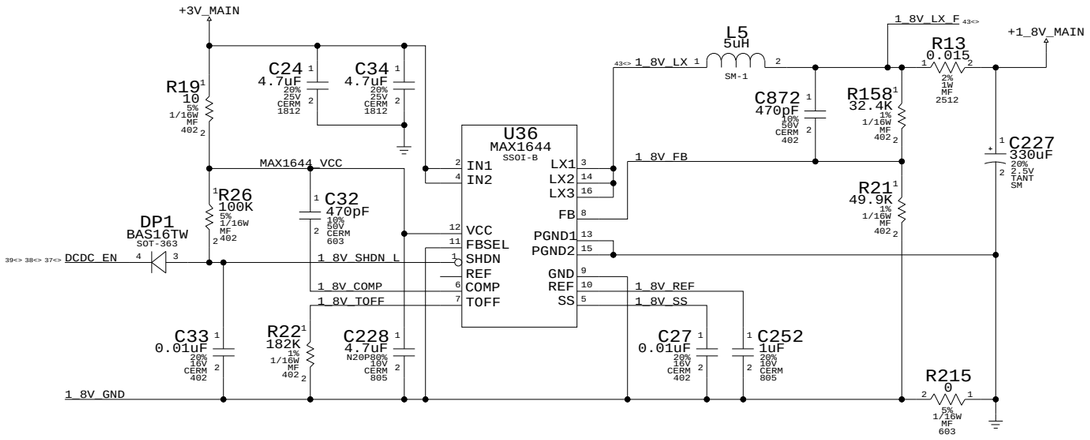
1) Mobility Radeon - AVDDs, DDR I/O and core
2) Gigabit Ethernet - AVDDL



+2_5V_SLEEP LOADS

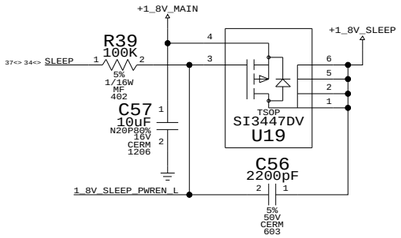
1) L3 Core

1.8V SWITCHER



+1_8V_MAIN LOADS

1) Uni-N - Core, PLL DVDDs, MaxBus I/O
2) Mobility Radeon - AVDDs
3) Gigabit Ethernet - DVDDH



+1_8V_SLEEP LOADS

1) MPC7450 - MaxBus I/O, L3 I/O
2) CPU JTAG & MaxBus Pull-ups
3) CPU PLL Config Straps
4) C5005 VDDCPU0

1.8V/2.5V SUPPLIES

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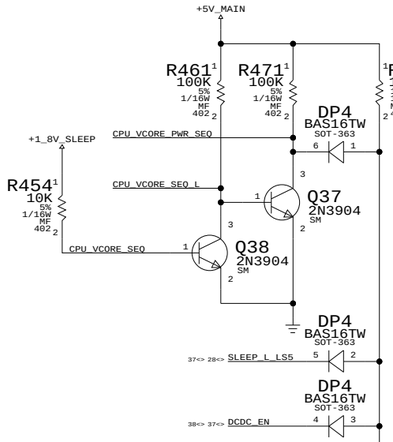
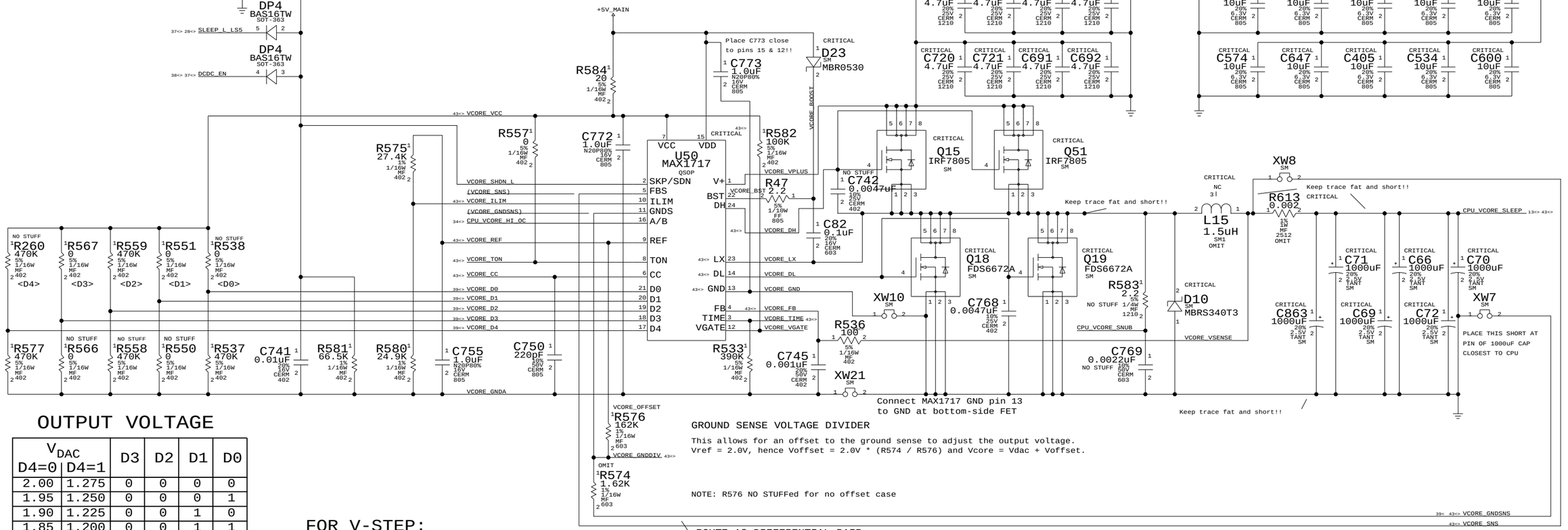
VCORE POWER SEQUENCING

CPU core follows CPU I/O voltage
(approx. 7ms delay)



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
152S0091	1	IND,1.4UF,20,W/W PWR,SHLD,20.4A,SMD	L15	
110S1625	1	RES,MF,1/16W,162K OHM,1,0603,SMD	R576	P59_VCORE_OFFSET
110S1625	1	RES,MF,1/16W,162K OHM,1,0603,SMD	R576	P88_VCORE_OFFSET
110S1623	1	RES,MF,1/16W,1.62K OHM,1,0603,SMD	R574	P59_VCORE_OFFSET
110S3013	1	RES,MF,1/16W,3.01K OHM,1,0603,SMD	R574	P88_VCORE_OFFSET

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
107S0019	1	RES,FILM,1W,0.002 OHM,2512,SMD	R613	CRITICAL	P59_SENSE
107S0023	1	RES,FILM,1W,0.001 OHM,2512,SMD	R613	CRITIAL	P88_SENSE



OUTPUT VOLTAGE

V_{DAC} D4=0	V_{DAC} D4=1	D3	D2	D1	D0
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

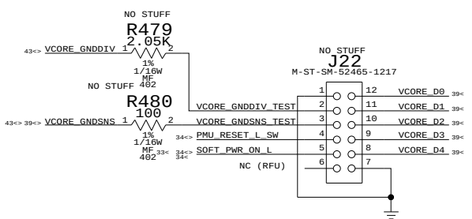
FOR V-STEP:

D<4..0>	A/B_ = Hi/Fast	A/B_ = Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1

If all pull-ups are >=100K and all pull-downs are <=1K, $V_A = V_B$.

Fmax Test Connections



VCORE SUPPLY

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DIGITAL SIGNALS

GROUP	SIG_NAME	DELAY_RULE	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	MIN_DAISY_CHAIN
MAXBUS	CPU_ADDR<31..0>	::560:3080	8		200		TRUE	133 MHz	
	CPU_DATA<62..0>	::560:3080	8		200		TRUE	133 MHz	
	CPU_DATA<63>	::560:3080	8		200			133 MHz	
	CPU_BG_L	::560:3080	8		200				
	CPU_DBG_L	::560:3080	8		200				
	CPU_TT<4..0>	::560:3080	8		200		TRUE		
	CPU_TBST_L						TRUE		
	CPU_TSIZ<2..0>						TRUE		
	CPU_GBL_L	::560:3080	8		200		TRUE		
	CPU_WT_L	::560:3080	8		200		TRUE		
	CPU_CI_L	::560:3080	8		200		TRUE		
	CPU_AACK_L	::560:3080	8		200		TRUE		
	CPU_DTI<2..0>	::560:3080	8		200		TRUE		
	CPU_QACK_L						TRUE		
	CPU_TS_L	::560:3080	8		200				
	CPU_TA_L	::560:3080	8		200				
	CPU_ARTRY_L	::560:3080	8		200				
	CPU_TEA_L	::560:3080	8		200				
MAIN MEMORY	MEM_DATA<63..0>	::2000:4872	8		200			133 MHz	
	RAD<12..0>	:::600						133 MHz	
	FMA_AR<12..0>	::1680:3880	8		200				
	BA_0	:::1000							
	FBA_0	::2000:3480	8		200				
	BA_1	:::1000							
	FBA_1	::2000:3480	8		200				
	RAS_CS0_L	:::500							
	FRAS_CS0_L	::2000:3980	8		200				
	RAS_CS1_L	:::500							
	FRAS_CS1_L	::2000:3980	8		200				
	RAS_CS2_L	:::500							
	FRAS_CS2_L	::2000:3980	8		200				
	RAS_CS3_L	:::500							
	FRAS_CS3_L	::2000:3980	8		200				
	CAS_DQM0_L	:::500							
	FCAS_DQM0_L	::1680:4372	8		200				
	CAS_DQM1_L	:::500							
	FCAS_DQM1_L	::1680:4372	8		200				
	CAS_DQM2_L	:::500							
	FCAS_DQM2_L	::1680:4372	8		200				
	CAS_DQM3_L	:::500							
	FCAS_DQM3_L	::1680:4372	8		200				
	CAS_DQM4_L	:::500							
	FCAS_DQM4_L	::1680:4372	8		200				
	CAS_DQM5_L	:::500							
	FCAS_DQM5_L	::1680:4372	8		200				
	CAS_DQM6_L	:::500							
	FCAS_DQM6_L	::1680:4372	8		200				
	CAS_DQM7_L	:::500							
	FCAS_DQM7_L	::1680:4372	8		200				
	SDRAS_L	:::500			200				
	FSDRAS_L	::2000:3980	8		200				
	SDCAS_L	:::500			200				
	FSDCAS_L	::2000:3980	8		200				
	MEMWE_L	:::1000			200				
	FMEMWE_L	::2000:3480	8		200				
	RAM_CKE0	:::600			200				
	FRAM_CKE1_A	::2000:3880	8		200				
	RAM_CKE1	:::600			200				
	FRAM_CKE0_A	::2000:3880	8		200				
	RAM_CKE2	:::600			200				
	FRAM_CKE1_B	::2000:5200	8		200				
	RAM_CKE3	:::600			200				
	FRAM_CKE0_B	::2000:5200	8		200				
	MEM_EXT_R	:::500							
AGP BYTES 0-1	AGP_AD<15..0>	::650:1350	6		100			66 MHz	
	AGP_CBE<1..0>	::900:1600	6		100			66 MHz	
	AGP_AD_STB<0>	U4.N29:U9.F16:1350:1600	8	500	90	8 MIL SPACING		66 MHz	
	AGP_AD_STB_L<0>	U4.M28:U9.F15:1350:1600	8	500	90	8 MIL SPACING		66 MHz	
AGP BYTES 2-3	AGP_AD<31..16>	::650:1350	6		100			66 MHz	
	AGP_CBE<3..2>	::900:1600	6		100			66 MHz	
	AGP_AD_STB<1>	U4.W29:U9.F12:1350:1600	8	500	90	8 MIL SPACING		66 MHz	
	AGP_AD_STB_L<1>	U4.Y29:U9.E12:1350:1600	8	500	90	8 MIL SPACING		66 MHz	
AGP SIDEBAND	AGP_SBA<7..0>	::950:1450	6		100			66 MHz	
	AGP_SB_STB	U4.AC29:U9.F9:1450:1700	8	500	90	8 MIL SPACING		66 MHz	
	AGP_SB_STB_L	U4.AD28:U9.G9:1450:1700	8	500	90	8 MIL SPACING		66 MHz	
AGP CONTROL	AGP_FRAME_L	U4.U27:U9.B15:900:1400	8		490			66 MHz	
	AGP_IRDY_L	U4.T30:U9.A14:850:1400	8		490			66 MHz	
	AGP_TRDY_L	U4.T28:U9.C14:900:1400	8		490			66 MHz	
	AGP_DEVSEL_L	U4.T29:U9.B7:900:1400	8		490			66 MHz	
	AGP_STOP_L	U4.T27:U9.E13:900:1400	8		490			66 MHz	
	AGP_PAR	::900:1400	8		490			66 MHz	
	AGP_REQ_L	U4.AF29:U9.C4:900:1400	8		490			66 MHz	
	AGP_GNT_L	U4.AF27:U9.E9:900:1400	8		490			66 MHz	
	AGP_RBF_L	U4.AE30:U9.E6:900:1450	8		490			66 MHz	
PCI	PCI_AD<31..0>	::4000:11000						33 MHz	MIN_DAISY_CHAIN
	PCI_CBE<3..0>	::4000:11000						33 MHz	MIN_DAISY_CHAIN
	PCI_FRAME_L	::4000:11000						33 MHz	MIN_DAISY_CHAIN
	PCI_IRDY_L	::4000:11000						33 MHz	MIN_DAISY_CHAIN
	PCI_TRDY_L	::4000:11000						33 MHz	MIN_DAISY_CHAIN
	PCI_DEVSEL_L	::4000:11000						33 MHz	MIN_DAISY_CHAIN
	PCI_STOP_L	::4000:11000						33 MHz	MIN_DAISY_CHAIN
	PCI_PAR	::4000:11000						33 MHz	MIN_DAISY_CHAIN
	PCI_PAR64	:::300						33 MHz	MIN_DAISY_CHAIN

CLOCK LINE CONSTRAINTS

GROUP	SIG_NAME	DELAY_RULE	MAX VIAS	MAX EXPOSED LENGTH	STUB_LENGTH	NET_SPACING_TYPE	PULSE PARAM
CLOCK CKT (C5005)	SYSCLK_CPU_UF	:::150					133 MHz
	SYSCLK_CPU	::6850:7100	3	250	200	10 MIL SPACING	133 MHz
	SYSCLK_UNIN_UF	:::150					133 MHz
	SYSCLK_UNIN	::1500:1750	3	250	200	10 MIL SPACING	133 MHz
	SYSCLK_UNIN_RDCLK_UF	:::150					133 MHz
	SYSCLK_UNIN_RDCLK	::5600:5880	3	250	200	10 MIL SPACING	133 MHz
	SYSCLK_DIMM0_A_UF	:::150					133 MHz
	SYSCLK_DIMM0_A	::3000:4750	3	250	200	10 MIL SPACING	133 MHz
	SYSCLK_DIMM0_B_UF	:::150					133 MHz
	SYSCLK_DIMM0_B	::3000:4750	3	250	200	10 MIL SPACING	133 MHz
	SYSCLK_DIMM1_A_UF	:::150					133 MHz
	SYSCLK_DIMM1_A	::3000:4750	3	250	200	10 MIL SPACING	133 MHz
	SYSCLK_DIMM1_B_UF	:::150					133 MHz
	SYSCLK_DIMM1_B	::3000:4750	3	250	200	10 MIL SPACING	133 MHz
	CLK66M_UNIN_AGP_UF	:::200			200		66 MHz
	CLK66M_UNIN_AGP	::2500:3000	4	500	200	10 MIL SPACING	66 MHz
	CLK66M_AGP_UF	:::200			200		66 MHz
	CLK66M_AGP_ATI	::3000:3500	4	500	200	10 MIL SPACING	66 MHz
	CLK66M_UNIN_PCI_INT_UF	:::200			200		66 MHz
	CLK66M_UNIN_PCI_INT	::2500:3000	4	500	200	10 MIL SPACING	66 MHz
	CLK33M_UNIN_PCI_EXT_UF	:::200			200		33 MHz
	CLK33M_UNIN_PCI_EXT	::2600:3200	4	500	200	10 MIL SPACING	33 MHz
CRYSTALS/ OSCS	CLK33M_KL_UF	:::200			200		33 MHz
	CLK33M_KL_PCI	::1800:2400	4	500	200	10 MIL SPACING	33 MHz
	CLK33M_CBUS_UF	:::200			200		33 MHz
	CLK33M_CBUS	::2400:2900	4	500	200	10 MIL SPACING	33 MHz
	CLK33M_NEC_UF	:::200			200		33 MHz
	CLK33M_NEC	::1000:1500	4	500	200	10 MIL SPACING	33 MHz
	CLK14M_IMI_XIN	::300:636					
	CLK14M_IMI_XOUT	::300:636					
	CLK18M_KL_UF	:::200			200		
	CLK18M_KL_PLL		4		200		
	CLK27M_ATI_UF	:::200			200		
	CLK27M_ATI		4	500	200		
	SND_CLKOUT		4	500	200		
MOBILITY M7	CLK27M_ATIMEM_SS	:::200			200		
ETHERNET	CLKENET_PHY_RX	:::200					125 MHz
	CLK_ENET_LINK_RX	::5500:6000	4	500	200		125 MHz
	CLKENET_PHY_TX	:::400					25 MHz
	CLK_ENET_LINK_TX	::5500:5800	4	500	200		25 MHz
	ENET_GTX_CLK	:::200					125 MHz
	ENET_PHY_GTX_CLK	::5000:5500	4	500	200		125 MHz
	ENET_PHY_GBE_REFCLK	:::300					125 MHz
	ENET_GBE_REFCLK	::5500:6000	4	500	200		125 MHz
FIREWIRE	CLK_PHY_FW	:::200					49.152 MHz
	CLK_UNIN_FW	::5300:6500	4	500	200		49.152 MHz
L3 CACHE	L3_CLK<0>	::1008:1232 NO_TEST=TRUE	4	250	200	10 MIL SPACING	200 MHz
	L3_ECHO_CLK<0..1>	::1008:1232 NO_TEST=TRUE	4	250	200	10 MIL SPACING	200 MHz
	L3_CLK<1>	::1288:1512 NO_TEST=TRUE	4	250	200	10 MIL SPACING	200 MHz
	L3_ECHO_CLK<2..3>	::1288:1512 NO_TEST=TRUE	4	250	200	10 MIL SPACING	200 MHz
ATI EXT SDRAM	See differential area for SDRAM clks						

SIGNAL CONSTRAINTS - PAGE 1

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Digital Signals (cont'd)

GROUP	SIG_NAME	DELAY_RULE	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	RATS_SCHEDULE	NO_TEST	PULSE_PARAM	
L3 CACHE	L3_ADDR<0..17>	::1400:1680					TRUE		14D6> 15C3< 15C6< 15D3< 15D6<
	L3_CNTL<0..1>	::1400:1680					TRUE		14C3> 15C3< 15C6<
	L3_DATA<0..31>	::560:1320					TRUE		14B6<> 14C6<> 15C4<> 15D4<>
	L3_DATA<32..63>	::840:1600					TRUE		14A6<> 14B6<> 15C1<> 15D1<>
EXT ATI SDRAM	ATI_VMEM_ADDR<0..13>	::280:3360				MIN_DAISY_CHAIN			19C3> 19D3> 22B3<> 22B7<> 22B4< 22B8< 22C4< 22C8<
	ATI_VMEM_CKEB	::280:3360				MIN_DAISY_CHAIN			19A5> 22B4< 22B8<
	ATI_VMEM_CSB_L	::280:3360				MIN_DAISY_CHAIN			19A5> 22B4< 22B8<
	ATI_VMEM_RASB_L	::280:3360				MIN_DAISY_CHAIN			19A5> 22B4< 22B8<
	ATI_VMEM_CASB_L	::280:3360				MIN_DAISY_CHAIN			19A5> 22B4< 22B8<
	ATI_VMEM_WE_L	::280:3360				MIN_DAISY_CHAIN			19A5> 22B4< 22B8<
	ATI_VMEM_QS<0..7>	::400:1000							19A5<> 19B5<> 22C4<> 22C8<>
	ATI_VMEM_DQMB<0..7>	::400:1000							19A3> 22B4< 22B8< 22C4< 22C8<
	ATI_VMEM_DATA<0..63>	::400:1000							19A3<> 19B3<> 19C3<> 22B3<> 22B7<> 22C3<> 22C7<>
	KL_PCI_GNT_L						TRUE		9C5> 16B8<
	MPIC_CLK						TRUE		10C2<> 16B4>
	MPIC_DATA_L						TRUE		10C2<> 16B4<
		U45.C7:J23.14:3300:4900		1500					
		U45.A6:J23.13:3300:4900		1500					
		::3300:5112		1500					
		::3300:4900		1500					
		::3300:4900		1500					
		U45.U20:J23.16:3300:4900		1500					
		U45.B6:J23.47:3293:4900		1500					
		U45.T17:J23.46:2688:4900		1500					
		U45.T18:J23.44:3032:4900		1500					
		::5200:6800		1500					
		::5200:6800		1500					
		::5200:6800		1500					
		::5200:6800		1500					
		::5200:6800		1500					
		::5200:6800		1500					
		::5200:6800		1500					
		::5200:6800		1500					
		::5200:6800		1500					
		::5200:6800		1500					
		::5200:6800		1500					
		::5200:6800		1500					
		::1000:1800	6	1500	200	4 MIL SPACING	TRUE		
		::1000:1800	6	1500	200	4 MIL SPACING			
		::1000:1800	6	1500	200	4 MIL SPACING	TRUE		
		::1000:1800	6	1500	200	4 MIL SPACING			
		U45.C10:RP36.4:1000:1800	6	1500	200	4 MIL SPACING			
		::974:1800	6	1500	200	4 MIL SPACING	TRUE		
		::1000:1800	6	1500	200	4 MIL SPACING			
		::1000:2602	6	1500	200	4 MIL SPACING			
		::1000:1800	6	1500	200	4 MIL SPACING			
		::1000:2012	6	1500	200	4 MIL SPACING			
		::1000:2096	6	1500	200	4 MIL SPACING			
		::1000:1936	6	1500	200	4 MIL SPACING			
		::1000:2149	6	1500	200	4 MIL SPACING			
		::1000:2259	6	1500	200	4 MIL SPACING			
		::300:500	6	1500	200	4 MIL SPACING			
		U45.D10:R611.1:300:506	6	1500	200	4 MIL SPACING			
		::300:500	6	1500	200	4 MIL SPACING			
		::300:503				4 MIL SPACING			
		::300:500				4 MIL SPACING			
		R632.2:J24.25:300:500				4 MIL SPACING			
		::300:500				4 MIL SPACING			
		::300:500				4 MIL SPACING			
		R624.2:J24.8:300:500				4 MIL SPACING			
		::300:500				4 MIL SPACING			
		::300:500				4 MIL SPACING			
		R169.2:J24.12:1000:2032				4 MIL SPACING			
		R611.2:J24.9:1000:2105				4 MIL SPACING			
		R168.2:J24.7:1000:2200				4 MIL SPACING			
		:::350							
		::4097:5000							
		:::600							
		::4600:5700	6						
		:::500							
		::4700:5300	6						
		:::500							
		::4700:5300	6						
		::5100:5500	6						
		::4000:4775	6						
		::3565:4900	6						
		::1700:2223							
		::3400:3700							
		::1800:2000							
		::200:300							
		::5100:6600							

SIGNAL CONSTRAINTS - PAGE 2

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Digital Signals (cont'd)

GROUP	SIG_NAME	DELAY_RULE	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
	EIDE_DATA<15..0>	:::1100						33 MHZ	16C6<> 16D6<> 32B7< 32C7< 32C8< 32D8<
	EIDE_ADDR<2..0>	:::800						33 MHZ	16C6> 32B8< 32C8<
	EIDE_CS1FX_L	:::800						33 MHZ	16C6> 32B8< 32C8<
	EIDE_CS3FX_L	:::700						33 MHZ	16C6> 32B8< 32C8<
EIDE / KEYLARGO	EIDE0_RD_L	:::700						33 MHZ	16B6> 32A8<
	EIDE0_WR_L	:::700						33 MHZ	16B6> 32A8<
	EIDE_IOCHRDY	:::700						33 MHZ	16C6< 32A8<
	EIDE0_INT	:::500						33 MHZ	16B6< 32A8<
	EIDE0_RST_L	:::700						33 MHZ	16C6> 32A8<
	EIDE0_DMACK_L	:::500						33 MHZ	16B6> 32B8<
	EIDE0_DMARQ	:::500						33 MHZ	16B6< 32B8<
	KL_CSLOT_IORD_L	:::700						33 MHZ	16B3<>
	KL_CSLOT_IOWR_L	:::700						33 MHZ	16B3<>
	CSLOT_DATA<15..0>	::1800:5500						33 MHZ	32C5<> 32C6<> 32D5<> 32D6<> 32D7<
	CSLOT_ADDR<2..0>	::1800:5500						33 MHZ	32C6<> 32C7<
EIDE / CARDSLOT	CSLOT_CS1FX_L	::1800:5500						33 MHZ	32C6<> 32C7<
	CSLOT_CS3FX_L	::1800:5500						33 MHZ	32C6<> 32C7<
	CSLOT_IORD_L	::1800:5500						33 MHZ	32C5<> 16B1<
	CSLOT_IOWR_L	::1800:5500						33 MHZ	32C5<> 16B1<
	CSLOT_ADDR<15>	U53.C2:J25.20:1800:5500						33 MHZ	16B4<> 32C6<>
CARDSLOT	CSLOT_ADDR<14>	U53.B6:J25.14:1800:5500						33 MHZ	16C4<> 32C6<>
	CSLOT_ADDR<13>	U53.A6:J25.13:1800:5500						33 MHZ	16C4<> 32C6<>
	CSLOT_ADDR<12..3>	::1800:5500						33 MHZ	16B2> 16C6> 32C6<>
	CSLOT_CE1_L	::1800:5500						33 MHZ	16B6> 32C6<>
	CSLOT_CE2_L	::1800:5500						33 MHZ	16B6> 32C5<>
	CSLOT_IRQ_L	U53.N15:J25.16:1800:5500						33 MHZ	16B4<> 32C6<>
	CSLOT_RESET	U53.C6:J25.47:1800:5500						33 MHZ	16C4<> 32C5<>
	CSLOT_IOWAIT_L	U53.P16:J25.46:1800:5500						33 MHZ	32C5<> 16B2<
	CSLOT_REG_L	U53.M13:J25.44:1800:5500						33 MHZ	16B4<> 32C5<>
	EIDE_DB_<15..0>	::2700:4400						33 MHZ	32A5<> 32A6<> 32B5<> 32B6<> 32B8< 32C7< 32C8<
	EIDE_ADDR_<2..0>	::2700:4400						33 MHZ	32A5<> 32A6<> 32B7<
	EIDE_CS1FX_L_OPU	::2700:4400						33 MHZ	32A5<> 32B7<
	EIDE_CS3FX_L_OPU	::2700:4400						33 MHZ	32A6<> 32B7<
	EIDE0_READ_L	::2700:5200						33 MHZ	32A6<> 32A7<
EIDE / DVD	EIDE0_WR_L_OPU	::2700:5200						33 MHZ	32A5<> 32A7<
	EIDE_IO_CHRDY	::2700:4400						33 MHZ	32A5<> 32A7<
	EIDE0_INTR	::2700:4400						33 MHZ	32A5<> 32A7<
	EIDE0_RST_L_OPU	::2700:4400						33 MHZ	32B5<> 32A7<
	EIDE0_DMA_ACK_L	::2700:4400						33 MHZ	32A6<> 32B7<
	EIDE0_DMA_RQ	::2700:4400						33 MHZ	32A6<> 32B7<
	UIDE_DATA<15..13>	::1000:2500	6		200			66 MHZ	16A6<> 32D4<
	UIDE_DATA<12>	::1000:2500	6		200			66 MHZ	16A6<> 32D4<
	UIDE_DATA<11..9>	::1000:2500	6		200			66 MHZ	16A6<> 32D4<
	UIDE_DATA<8>	::1000:2500	6		200			66 MHZ	16A6<> 32D4<
	UIDE_DATA<7>	U53.E8:RP51.4:1000:2500	6		200			66 MHZ	16B6<> 32D4<
	UIDE_DATA<6..1>	::1000:2500	6		200			66 MHZ	16B6<> 32D4<
	UIDE_DATA<0>	::1000:2500	6		200			66 MHZ	16B6<> 32D4<
	UIDE_ADDR<2..0>	::950:2500	6		200			66 MHZ	16A6> 32D4<
	UIDE_RST_L	::1000:2300	6		200			66 MHZ	16A6> 32C4<
	UIDE_DIOW_L	::1000:2012	6		200			66 MHZ	16A6> 32C4<
	UIDE_DIOR_L	::1000:2096	6		200			66 MHZ	16A6> 32C4<
	UIDE_DMACK_L	::1000:1936	6		200			66 MHZ	16A6> 32C4<
ULTRA ATA/66	UIDE_CS1FX_L	::750:2000	6		200			66 MHZ	16A6> 32D4<
	UIDE_CS3FX_L	::1000:2259	6		200			66 MHZ	16A6> 32C4<
	UIDE_DMARQ	:::500	6		200			66 MHZ	16A6<
	UIDE_IOCHRDY	U53.D8:R119.1:300:506	6		200			66 MHZ	16A6<
	UIDE_INTRQ	:::500	6		200			66 MHZ	16A6<
	HD_DATA<15..0>	::300:600						66 MHZ	32D1<> 32D2<> 32D3<
	HD_ADDR<2..0>	::300:600						66 MHZ	32C1<> 32C2<> 32D3<
	HD_RESET_L	R594.2:J27.25:300:500						66 MHZ	32D2<> 32C3<
	HD_DIOW_L	::300:500						66 MHZ	32C2<> 32C3<
	HD_DIOR_L	::300:500						66 MHZ	32C2<> 32C3<
	HD_DMACK_L	R600.2:J27.8:300:500						66 MHZ	32C2<> 32C3<
	HD_CS1_L	::300:600						66 MHZ	32C2<> 32D3<
	HD_CS3_L	::300:500						66 MHZ	32C1<> 32C3<
	HD_DMARQ	R117.2:J27.12:1000:2032						66 MHZ	32D2<> 16A5<
	HD_IOCHRDY	R119.2:J27.9:1000:2105						66 MHZ	32C2<> 16A5<
	HD_INTRQ	R118.2:J27.7:1000:2200						66 MHZ	32C2<> 16A5<
	ENET_PHY_RXD<7..0>	:::400							28B6<>
	ENET_RXD<7..0>	::4097:5000							10B6< 28B7<
ETHERNET MII	ENET_RX_DV	::4700:5300					TRUE		28B6> 10C6<
	ENET_RX_ER	::4700:5300					TRUE		28B6> 10B6<
	ENET_TX_D<7..0>	:::600							10C6<>
	ENET_PHY_TXD<7..0>	::4500:5700	6						10B7< 10C7< 28B6< 28C6<
	ENET_TX_EN	:::500							10C6<>
	ENET_PHY_TX_EN	::4700:5300	6						10C7< 28C6<
	ENET_TX_ER	:::500							10C6<>
	ENET_PHY_TX_ER	::4680:5300	6						10C7< 28C6<
	ENET_MDIO	::5100:6000	6						10B6> 28A5<>
	ENET_MDC	::4000:4775	6				TRUE		10B6> 28A4<
	ENET_COL						TRUE		28B6> 10B6<
	ENET_CRS						TRUE		28B6> 10B6<
	FW_LINK_DATA<7..0>	::2500:4500	6						10B2<> 10C2<> 29B7<
	FW_PHY_DATA<7..0>	::2300:4300							29B6<>
FIREWIRE MII	FW_LINK_CNTL<1..0>	::2400:4400							10B2<> 29B7<
	FW_PHY_CNTL<1..0>	::2400:4400							29B6<>
	FW_LINK_LREQ	:::500							10B2> 29B7<
	FW_PHY_LREQ	::4800:7300							29B6<

Differential Signals

GROUP	SIG_NAME	DIFFERENTIAL_PAIR	MATCHED_DELAY	MIN_LINE_WIDTH	PULSE_PARAM	MAX_EXPOSED_LENGTH	MAX_VIAS	
	MDI_P<0>	ENET_TRD0	ENET_TRD0:U8.K1:T1.12:100	5				28C5<>
	MDI_M<0>	ENET_TRD0	ENET_TRD0:U8.K2:T1.11:100	5				28C5<>
	RJ45_DP<0>	RJ45_DP0	RJ45_DP0:T1.13:J2.1:100	5				28C2<>
	RJ45_DN<0>	RJ45_DP0	RJ45_DP0:T1.14:J2.2:100	5				28C2<>
	MDI_P<1>	ENET_TRD1	ENET_TRD1:U8.K4:T1.9:100	5				28C5<>
	MDI_M<1>	ENET_TRD1	ENET_TRD1:U8.K3:T1.8:100	5				28C5<>
	RJ45_DP<1>		DELAY_RULE=T1.16:J2.3:414.5:415	5				28C2< DELAY_RULE used as these could not
ETHERNET	RJ45_DN<1>		DELAY_RULE=T1.17:J2.6:213:213.5	5				28C2< be routed as true differential pairs.
	MDI_P<2>	ENET_TRD2	ENET_TRD2:U8.K5:T1.6:100	5				28C5<>
	MDI_M<2>	ENET_TRD2	ENET_TRD2:U8.K6:T1.5:100	5				28C5<>
	RJ45_DP<2>		DELAY_RULE=T1.19:J2.4:206:206.5	5				28C2< DELAY_RULE used as these could not
	RJ45_DN<2>		DELAY_RULE=T1.20:J2.5:337:338	5				28B2< be routed as true differential pairs.
	MDI_P<3>	ENET_TRD3	ENET_TRD3:U8.K8:T1.3:100	5				28B5<>
	MDI_M<3>	ENET_TRD3	ENET_TRD3:U8.K7:T1.2:100	5				28B5<>
	RJ45_DP<3>	RJ45_DP3	RJ45_DP3:T1.22:J2.7:100	5				28B2<>
	RJ45_DN<3>	RJ45_DP3	RJ45_DP3:T1.23:J2.8:100	5				28B2<>
	FW_TPA0N	FW_TPA0	FW_TPA0:::4%			500		29B4<>
	FW_TPA0P	FW_TPA0	FW_TPA0:::4%			500		29B4<>
	FW_TPB0N	FW_TPB0	FW_TPB0:::4%			500		29B4<>
FIREWIRE	FW_TPB0P	FW_TPB0	FW_TPB0:::4%			500		29B4<>
	FW_TPI1N	FW_TPI1	FW_TPI1:::4%					29A3<> 29B2<>
	FW_TPI1P	FW_TPI1	FW_TPI1:::4%					29A3<> 29B2<>
	FW_TPO1N	FW_TPO1	FW_TPO1:::4%					29A3<> 29B2<>
	FW_TPO1P	FW_TPO1	FW_TPO1:::4%					29A3<> 29B2<>
	CLKLVDS_N	CLKLVDS	LVDS:::110			500	4	20B5> 31B5<>
	CLKLVDS_P	CLKLVDS	LVDS:::110			500	4	20B5> 31B5<>
	LVDS_L0N	LVDS_L0	LVDS:::110					20B5> 31B5<>
LVDS	LVDS_L0P	LVDS_L0	LVDS:::110					20B5> 31B5<>
	LVDS_L1N	LVDS_L1	LVDS:::110					20B5> 31B5<>
	LVDS_L1P	LVDS_L1	LVDS:::110					20B5> 31B5<>
	LVDS_L2N	LVDS_L2	LVDS:::110					20B5> 31B5<>
	LVDS_L2P	LVDS_L2	LVDS:::110					20B5> 31B5<>
	TMDS_CLKN	CLKTMDS	CLKTMDS:::100			500	4	20B6> 31D6<> 20D4<
	TMDS_CLKP	CLKTMDS	CLKTMDS:::100			500	4	20B6> 31D6<> 20D3<
	TMDS_DN<0>	TMDS_D0	TMDS_D0:::100					20B6> 31D5<> 20D7< 31D7<
	TMDS_DP<0>	TMDS_D0	TMDS_D0:::100					20B6> 31D5<> 20D6< 31D6<
TMDS	TMDS_DN<1>	TMDS_D1	TMDS_D1:::100					20B6> 31D4<> 20D7< 31D7<
	TMDS_DP<1>	TMDS_D1	TMDS_D1:::100					20B6> 31D4<> 20D6< 31D6<
	TMDS_DN<2>	TMDS_D2	TMDS_D2:::100					20B6> 31D4<> 20D7< 31D7<
	TMDS_DP<2>	TMDS_D2	TMDS_D2:::100					20B6> 31D4<> 20D6< 31D6<
	USB_DAM	USB_DA	USB_DA:::200					16C2<> 30B8<
	USB_DAP	USB_DA	USB_DA:::200					16C2<> 30B8<
	USB_DBM	USB_DB	USB_DB:::200					16C3<>
	USB_DBP	USB_DB	USB_DB:::200					16C3<>
	USB_DCM	USB_DC	USB_DC:::200					16B2<> 30B8<
	USB_DCP	USB_DC	USB_DC:::200					16B2<> 30B8<
	USB_DDM	USB_DD	USB_DD:::200					16B3<>
	USB_DDP	USB_DD	USB_DD:::200					16B3<>
	BT_USB_DM	BT_USB_D	BT_USB:::200					30C2<> 16C1< 16D1<
	BT_USB_DP	BT_USB_D	BT_USB:::200					30C2<> 16C1< 16D1<
USB	MODEM_USB_DM	MODEM_USB_D	MODEM_USB:::200					32A3<> 16B1<
	MODEM_USB_DP	MODEM_USB_D	MODEM_USB:::200					32B3<> 16B1<
	USB_D1M	USB_D1	USB_D1:R177.2:L2.1:200					30B7<>
	USB_D1P	USB_D1	USB_D1:R178.2:L1.1:200					30B7<>
	USB_D1M_EMI	USB_D1_EMI	USB_D1_EMI:L2.2:J5.2:200					30B5<>
	USB_D1P_EMI	USB_D1_EMI	USB_D1_EMI:L1.2:J5.3:200					30B5<>
	USB_D2M	USB_D2	USB_D2:R173.2:L4.1:200					30B7<>
	USB_D2P	USB_D2	USB_D2:R174.2:L3.1:200					30B7<>
	USB_D2M_EMI	USB_D2_EMI	USB_D2_EMI:L4.2:J6.2:200					30B5<>
	USB_D2P_EMI	USB_D2_EMI	USB_D2_EMI:L3.2:J6.3:200					30B5<>
	NEC_RSDCM	NEC_RSDC	NEC_RSDC:::150 DELAY_RULE=:::500					17C5<>
	NEC_RSDCP	NEC_RSDC	NEC_RSDC:::150 DELAY_RULE=:::500					17C5<>
	NEC_USB_DCM	NEC_USB_DC	NEC_USB_DC:::150 DELAY_RULE=U51.G16:R79.2::500					17C3<> 30C8<
USB 2.0	NEC_USB_DCP	NEC_USB_DC	NEC_USB_DC:::150 DELAY_RULE=U51.F16:R78.2::500					17C3<> 30B8<
	NEC_RSDDM	NEC_RSDD	NEC_RSDD:::150 DELAY_RULE=:::500					17C5<>
	NEC_RSDDP	NEC_RSDD	NEC_RSDD:::150 DELAY_RULE=:::500					17C5<>
	NEC_USB_DDM	NEC_USB_DD	NEC_USB_DD:::150 DELAY_RULE=U51.D15:R89.2::500					17C3<> 30A8<
	NEC_USB_DDP	NEC_USB_DD	NEC_USB_DD:::150 DELAY_RULE=U51.D16:R90.2::500					17C3<> 30A8<
ATI DDR MEM CLKS	ATI_VMEM_CLKB<0>	ATI_VMEM_CLKB0	ATI_VMEM_CLKB0:::100 DELAY_RULE=:::700:1008	183 MHZ		250		19A5<> 22A8< 22B8<
	ATI_VMEM_CLKB_L<0>	ATI_VMEM_CLKB0	ATI_VMEM_CLKB0:::100 DELAY_RULE=:::700:1008	183 MHZ		250		19A5<> 22A8< 22B8<
	ATI_VMEM_CLKB<1>	ATI_VMEM_CLKB1	ATI_VMEM_CLKB1:::100 DELAY_RULE=:::700:1008	183 MHZ		250		19A5<> 22A4< 22B4<
	ATI_VMEM_CLKB_L<1>	ATI_VMEM_CLKB1	ATI_VMEM_CLKB1:::100 DELAY_RULE=:::700:1008	183 MHZ		250		19A5<> 22A4< 22B4<

SIGNAL CONSTRAINTS - PAGE 3

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POWER NET CONSTRAINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
MAIN/SLEEP	/+PBUS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	/+5V_MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	/+5V_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	/+3V_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	/+3V_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	/+3V_PMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	/+2_5V_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	/+2_5V_SLEEP	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	/+1_8V_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	
	/+1_8V_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	/+1_5V_MAIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
ADAPTER/ BATTERY	+ADAPTER_UF	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	
	+ADAPTER	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	35D6<> 37A7<
	+ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	35D4<> 36B8<>
	INPUT14_24V_SW	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	35D2< 36C8<
	PWRBUS_14_24V	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	1625_VIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		36C5<
	CHGR_VSW	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	36B4<>
	CHGR_OUT	VOLTAGE=16.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	36B2<>
	BATT_FET_SW	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	35B4<>
	BATT_ISNS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	36D4<
	BATT_LINE	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	35B2<> 36D5<
	BATT_POS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	35B8<
	BATT_POS_F	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	35B7<> 37A8<>
	BATT_RES	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	35B6<>
	1625_INTVCC	VOLTAGE=5.3V	MIN_LINE_WIDTH=10		36C4<>
	3V_PMU_CHGR	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		36D6<> 36C1<> 36C7<>
	1625_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	36B6<
	BATT_NEG	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	35B8<
BACKUP	+5_5V_RAW	VOLTAGE=5.5V	MIN_LINE_WIDTH=10		37A5<
	+5_5V_BU	VOLTAGE=5.5V	MIN_LINE_WIDTH=10		37A4<> 34Z2<
	LTC1625_EXTVCC	VOLTAGE=5.5V	MIN_LINE_WIDTH=10		36A3<> 36C6<
POWER SUPPLIES	PS_VL	VOLTAGE=5V	MIN_LINE_WIDTH=10		37D7<
	PS_LX_5V	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	37D5<>
	+5V_RSNS	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	37D4<>
	PS_LX_3V	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	37B5<>
	PS_CS_3V	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	37C6<
	2_5V_LX	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	38D6<
	2_5V_LX_F	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	38D5<
	1_8V_LX	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	38B6<
	1_8V_LX_F	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	38B5<
	VCORE_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	39C6<
	VCORE_LX	VOLTAGE=1.4V	MIN_LINE_WIDTH=200	MIN_NECK_WIDTH=10	39B5<>
	VCORE_DH		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	39B5<>
	VCORE_DL		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	39B5<>
	VCORE_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	39C4<>
	VCORE_ILIM		MIN_LINE_WIDTH=8		39C6<
	VCORE_REF		MIN_LINE_WIDTH=8		39B6<>
	VCORE_TON	VOLTAGE=5V	MIN_LINE_WIDTH=8		39B6<
	VCORE_CC		MIN_LINE_WIDTH=8		39B6<>
	VCORE_FB	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		39B5<
	VCORE_TIME		MIN_LINE_WIDTH=8		39B4<>
	VCORE_VGATE		MIN_LINE_WIDTH=8		39B4<>
	VCORE_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30		39B5<>
	VCORE_GNDSNS	VOLTAGE=0V	MIN_LINE_WIDTH=8		39A1<> 39A5<
	VCORE_SNS	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		39A1<>
	VCORE_GNDDIV	VOLTAGE=0V	MIN_LINE_WIDTH=8		39A5< 39B5<
MISC	+PBUS_INV	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31A7<>
	+5V_HD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33D1<> 37D1<>
	+5V_INV_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31A7<>
	+5V_INV_UF_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31A7<>
	+5V_IO_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31D5< 33A8<
	+5V_TPAD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=10		33D7<>
	+5V_USB_VDD_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30D5<>
	+5V_USB_VDD_A	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	30C5<>
	+5V_USB_VDD_B	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	30C5<>
	+5V_DDC_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	31D4<>
	FAN_PWR	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	24D1<>
	FAN_PWR_LOW	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	24C2<>
	FAN2_PWR	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	24B1<>
	FAN2_PWR_LOW	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	24B1<>
	+3V_HALL_EFFECT	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		33D6<>
	+3V_LCD	VOLTAGE=3.3V	MIN_LINE_WIDTH=12	MIN_NECK_WIDTH=10	31B5<>
	+3V_LCD_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31B6<>
	+3V_PMU_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		34D5<> 34B6<
	TPAD_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10		33C6<>
	TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		31B1<>
	TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		31A1<>

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
UNIN	+3V_UNIN_MAXPLL_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	6D5<
	+3V_UNIN_AGPPLL_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	8D6<
	+1_8V_UNIN_MAXPLL_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	6D5<
	+1_8V_UNIN_AGPPLL_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	8D6<
CPU	+3V_PCI_64B_PU	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	9D8<
	CPU_VCORE_SLEEP	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	13D8<> 13D3< 39C1< 39D2<
	CPU_AVDD	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	13D4<>
KEY LARGO	+3V_KL	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	16D5<
	+3V_KL_AVDD1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	16D3<
	+3V_KL_AVDD2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	16D3<
	+3V_KL_AVDD3	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	16D3<
	+3V_KL_AVDD4	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	16D6<
	+3V_KL_OSC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	16A5<
	+3V_KL_USB	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	16C1<>
	KL_AGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	16A5<> 16D3< 16D6<
CARDBUS	+VCC_CBUS_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18B1<> 18B3<> 18D3<> 18D1<
	+VPP_CBUS_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18B1<> 18B3<> 18D3<>
MOBILITY RADEON	+VCORE_ATI_VDDM	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21B7< 22C2< 22C6< 22D4< 22D6<
	+3V_ATI_VDDR3	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21B3<
	+3V_ATI_OSC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	20B7<
	+3V_ATI_SS	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	20A7< 20A8<
	+2_5V_ATI_VDDR	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22D4< 22D6< 19B7< 21B5< 21C2< 21C4< 22C2< 22C6<
	+1_8V_ATI_LVDDR	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21A6<
	+2_5V_ATI_A2VDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=10		21D5<
	+1_2V_ATI_VDDC	VOLTAGE=1.2V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	20C4<
	+1_2V_ATI_VCORE	VOLTAGE=1.2V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	20B3< 20C4<
	+1_8V_ATI_A2VDDQ	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21C6<
	+1_8V_ATI_AVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21D6<
	+1_8V_ATI_MPVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21A6<>
	+1_8V_ATI_PVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21D7<> 21A5<
	+1_25V_ATI_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		19B7< 22B2< 22B6<
	+1_8V_ATI_AVDDDI	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21C4< 21D7<
	+1_8V_ATI_A2VDDDI	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21C4< 21C7<
IMI C5005	+3V_IMI_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23C7<
	PLL_SDRAM_CPU1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23C7<
	PLL_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	23C5<
	PLL_VCC_CPU0	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	23C5<
ETHERNET	+3V_ENET	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28A4< 28B6< 28D6<
	ENET_AVDDL	VOLTAGE=1.2V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28C6< 28D2< 28D5<
	+2_5V_ENET	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28C5< 28D2< 28D3< 28D5< 28D6<
	+1_8V_ENET	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28C6< 28C7< 28D1<
	ENET_DVDDL	VOLTAGE=1.2V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28C6< 28D4< 28D6<
	ENET_AVDD	VOLTAGE=1.2V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28C5< 28D4<
	ENET_PLLVDD	VOLTAGE=1.2V	MIN_LINE_WIDTH=10		28C5< 28D3<
FW	+ENET_CTAP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28C1<>
	+PBUS_FW_SW	VOLTAGE=16.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29D6<>
	+FW_VP_FUSE	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29C5<>
	+FW_VP_UF	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29D5<
	FW_VP	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29B2<>
	+3V_FW_VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29A2<> 29A3<> 29D4<
	FW_VGND	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29B2<>
AUDIO	+AUD4V	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27B4< 27D3<
	MAX4298_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26C7<>
	MAX4298_SVCC	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26C6<>
	+AUD3V	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25B5< 25C6<
	FIL_AUD3V	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25D4<
	FIL_DIG3V	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25C4<
	+AUD4V_F1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27D5<
	+AUD4V_F2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27D4<
	TI_AVSS	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26B3<> 25A4<
	LINE_OUT_STAR_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26B3<> 26B8< 26C4< 26C5<
	MIC_STAR_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26B3<> 27B2<>
	SPKR_STAR_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26B3<> 26A8<
	PWR3V_STAR_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26A3<> 25A4< 25C5< 25C7< 25D4<
	PWR4V_STAR_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26A3<> 27A4< 27B4< 27C1< 27D4<
	HP_AMP_SVCC_STAR_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26A4<> 26B5<
	BOOMER_STAR_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26A3<> 26B5<

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
NEC L3 CACHE	+3V_NEC_VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	17B3< 17D7<
	NEC_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	17D6<
	NEC_AVSS	VOLTAGE=0V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	17A5< 17B4< 17D7<
	L3_VDD_SLEEP	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	15A6< 15A8< 15D3< 15D6< 15D7<
	+LT1962_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	14D3<
	+1_5V_L3_VDDQ_SLEEP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	15B8< 15D1< 15D4< 14D1<> 14D6<> 14B3< 14C3< 15B2< 15B5<
		VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
		VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
		VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
		VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
		VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
		VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
		VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
		VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
		VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
		VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
		VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
		VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
		VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	
		VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
		VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	
		VOLTAGE=2.5V	MIN_LINE_WIDTH=10		
		VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
		VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
		VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	
		VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	
		VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	
		VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	
		VOLTAGE=1.25V	MIN_LINE_WIDTH=10		
		VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	
		VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	
		VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
		VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
		VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	
		VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	
		VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
		VOLTAGE=3.3V	MIN_LINE_WIDTH=10		
		VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
		VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
		VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
		VOLTAGE=16.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	
		VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	
		VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	
		VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	
		VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
		VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	
		VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
		VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
		VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
		VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
		VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
		VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
		VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
		VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
		VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
		VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
		VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
		VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
		VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
		VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
		VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
		VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	

VOLTAGE=0V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=6 /GND

VOLTAGE=0V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=12 /CHGND1
CHGND1

VOLTAGE=0V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=12 /CHGND2
CHGND2

VOLTAGE=0V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=12 /CHGND3
CHGND3

VOLTAGE=0V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=12 /CHGND4A
CHGND4A

VOLTAGE=0V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=12 /CHGND4B
CHGND4B

VOLTAGE=0V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=12 /CHGND5
CHGND5

VOLTAGE=0V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=12 /CHGND6
CHGND6

VOLTAGE=0V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=12 /CHGND7
CHGND7

SIGNAL CONSTRAINTS - PAGE 4

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SIZE	DRAWING NUMBER	REV.
D	051-6403	E

SCALE	SHT	OF
NONE	43	46

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      *** Signal Cross-Reference ***
         --- for the entire design --

+1_2V_ATI_VCORE 43C4<> 20B3< 20C4<
+1_2V_ATI_VDDC  43C4<> 20C4<
+1_5V_L3_VDDQ_SLEEP 14D1<> 14D6<> 43D1<> 14B3<
               14C3< 15B2< 15B5< 15B8< 15D1< 15D4<
+1_8V_ATI_A2VDDDI 43C4<> 21C4< 21C7<
+1_8V_ATI_A2VDDQ 43C4<> 21C6<
+1_8V_ATI_AVDD  43C4<> 21D6<
+1_8V_ATI_AVDDDI 43C4<> 21C4< 21D7<
+1_8V_ATI_LVDDR 43C4<> 21A6<
+1_8V_ATI_MPVDD 21A6<> 43C4<>
+1_8V_ATI_PVDD  21D7<> 43C4<> 21A5<
+1_8V_ATI_VDDC18 19A8< 20C3<
+1_8V_ENET      43B4<> 28C6< 28C7< 28D1<
+1_8V_UNIN_AGPPLL_MAIN 43D4<> 8D6<
+1_8V_UNIN_MAXPLL_MAIN 43D4<> 6D5<
+1_25V_ATI_VREF 43C4<> 19B7< 22B2< 22B6<
+2_5V_ATI_A2VDD 43C4<> 21D5<
+2_5V_ATI_VDDR  43C4<> 19B7< 21B5< 21C2< 21C4<
               22C2< 22C6< 22D4< 22D8<
+2_5V_ENET      43C4<> 28C5< 28D2< 28D3< 28D5<
               28D6<
+3V_ATI_OSC_SLEEP 43C4<> 20B7<
+3V_ATI_SS      43C4<> 20A7< 20A8<
+3V_ATI_VDDR3   43C4<> 21B3<
+3V_ENET        43C4<> 28A4< 28B6< 28D6<
+3V_FW_VDD      29A2<> 29A3<> 43B4<> 29D4<
+3V_HALL_EFFECT 33D6<> 43A6<>
+3V_HE_F        33D6<
+3V_IMI_SLEEP   43C4<> 23C7<
+3V_KL          43D4<> 16D5<
+3V_KL_AVDD1    43D4<> 16D3<
+3V_KL_AVDD2    43D4<> 16D3<
+3V_KL_AVDD3    43D4<> 16D3<
+3V_KL_AVDD4    43D4<> 16D6<
+3V_KL_OSC_SLEEP 43D4<> 16A5<
+3V_KL_USB      16C1<> 43D4<>
+3V_LCD         31B5<> 43A6<>
+3V_LCD_SW      31B6<> 43A6<>
+3V_NEC_VDD     43D1<> 17B3< 17D7<
+3V_PCI_64B_PU  43D4<> 9D8<
+3V_PMU_AVCC    34D5<> 43A6<> 34B6<
+3V_PMU_ESR     37A3<
+3V_UNIN_AGPPLL_MAIN 43D4<> 8D6<
+3V_UNIN_MAXPLL_MAIN 43D4<> 6D5<
+5V_DDC_ISO     31D3<>
+5V_DDC_SLEEP   31D4<> 43A6<>
+5V_HD_SLEEP    32D1<> 37D1<> 43B6<>
+5V_INV_SW      31A7<> 43B6<>
+5V_INV_UF_SW   31A7<> 43B6<>
+5V_IO_SLEEP    43B6<> 31D5< 33A8<
+5V_RSNS        37D4<> 43C6<>
+5V_TOL         32B5<>
+5V_TPAD_SLEEP  33D7<> 43A6<>
+5V_USB_VDD_A   30C5<> 43A6<>
+5V_USB_VDD_B   30C5<> 43A6<>
+5V_USB_VDD_SW  30D5<> 43A6<>
+5_5V_BU        37A4<> 43C6<> 34D2<
+5_5V_ESR       37A4<
+5_5V_RAW       43C6<> 37A5<
+ADAPTER        35D6<> 43D6<> 37A7<
+ADAPTER_ILIM   37A7<>
+ADAPTER_OR_BATT 37A6<>
+ADAPTER_SW     35D4<> 36B8<> 43D6<>
+ADAPTER_UF     43D6<>
+AUD3V          43B4<> 25B5< 25C6<
+AUD4V          43B4<> 27B4< 27D3<
+AUD4V_F1       43B4<> 27D5<
+AUD4V_F2       43B4<> 27D4<
+BBATT_BYPASS   37A6<>
+ENET_CTAP      28C1<> 43B4<>
+FW_VP_FUSE     29C5<> 43B4<>
+FW_VP_UF       43B4<> 29D5<
+LT1962_SLEEP   43D1<> 14D3<
+PBUS_FW_SW     29D6<> 43B4<>
+PBUS_INV       31A7<> 43B6<>
+VCC_CBUS_SW    18B1<> 18B3<> 18D3<> 43D4<> 18D1<
+VCORE_ATI_VDDM 43C4<> 21B7< 22C2< 22C6< 22D4<
               22D8<
+VPP_CBUS_SW    18B1<> 18B3<> 18D3<> 43D4<>
/+1_5V_MAIN     43D6<>
/+1_8V_MAIN     43D6<>
/+1_8V_SLEEP    43D6<>
/+2_5V_MAIN     43D6<>
/+2_5V_SLEEP    43D6<>
/+3V_MAIN       43D6<>
/+3V_PMU        43D6<>
/+3V_SLEEP      43D6<>
/+5V_MAIN       43D6<>
/+5V_SLEEP      43D6<>
/+PBUS          43D6<>
/CHGND1         43A4>
/CHGND2         43A4>
/CHGND3         43A4>
/CHGND4A        43A4>
/CHGND4B        43A4>
/CHGND5         43A4>
/CHGND6         43A4>
/CHGND7         43A4>
/GND            43A4>
1V20_REF        35C4< 35C6<
1_02V_AUX       36B6< 36B7<
1_5V_AGP_ADJ    21C7<
1_5V_AGP_BYP    21C8<>
1_8V_COMP       38A7<
1_8V_FB         38B6<
1_8V_GND        38A8<
1_8V_LX         43B6<> 38B6<
1_8V_LX_F       43B6<> 38B5<
1_8V_REF        38A6<
1_8V_SHDN_L     38B7<>
1_8V_SLEEP_PWREN_L 38B3<>
1_8V_SS         38A6<
1_8V_TOFF       38A7<
2_5V_COMP       38C7<
2_5V_FB         38C6<
2_5V_GND        38C8<
2_5V_LX         43C6<> 38D6<
2_5V_LX_F       43B6<> 38D5<
2_5V_LX_M       38D5<
2_5V_MAX1644_VCC 38C7<
2_5V_REF        38C6<
2_5V_SHDN_L     38C7<>
2_5V_SLEEP_PWREN_L 38C3<>
2_5V_SS         38C6<
2_5V_TOFF       38C7<
3V_PMU_CHGR     35C1<> 36C7<> 36D6<> 43C6<>
3V_PMU_SENSE    37A4<
3V_PMU_VTAP     37A4<
3V_SLEEP_PWREN_L 37A3<>
5V_HD_PWREN     37D2<>
5V_SLEEP_PWREN  37C2<>
13_5V_DET       35C4<
1625_BG         36B4<>
1625_BST        36C4<>
1625_BST_F      36C4<
1625_COMP       36C5<
1625_INTVCC     36C4<> 43C6<>
1625_SGND       43C6<> 36B6<
1625_TG         36C4<>
1625_VFB        36B4<>
1625_VIN        43C6<> 36C5<
4863_BYPASS     26A7<
4863_SHDN       26A7<
ACOUT           26C2<>
AC_ENABLE_GATE  35D4<>
AC_ENABLE_L     35C4<
AC_IN           28A8<> 34B3< 35C5<
ADAPTER_DET     35D7<> 34B3< 34D3<
ADAPTER_I_REG   36B6<>
ADAPTER_PWR_SW  35A3<>
AGP_AD<31..0>   8B5<> 8C5<> 8D5<> 19C7<> 19D7<>
               40A5<> 40B5<>
AGP_AD_STB<1..0> 8B5<> 19D5<> 40A5<> 40B5<> 8C2<
AGP_AD_STB_L<1..0> 8B5<> 19D5<> 40A5<> 40B5<> 8C2<
AGP_ATI_INT_L   16C4<> 19B7> 16C5<
AGP_ATI_RESET_L 19B7<
AGP_BUSY_L_PU   19D5> 19D7<
AGP_CBE<3..0>   8B7<> 19B7<> 40A5<> 40B5<>
AGP_DEVSEL_L    8C7<> 19B7<> 40A5<> 8D2<
AGP_FRAME_L     8C7<> 19B7<> 40A5<> 8D2<
AGP_GNT_L       8C7> 40A5<> 8B2< 19B7<
AGP_IRDY_L      8C7<> 19B7<> 40A5<> 8D2<
AGP_PAR         8C7<> 19B7> 40A5<>
AGP_PIPE_L_PU   8B7< 8C2<
AGP_RBF_L       19C5> 40A5<> 8B7< 8D2<
```

```
AGP_REQ_L       19B7<> 40A5<> 8B2< 8C7<
AGP_SBA<7..0>   19C5> 19C5<> 19C5> 40A5<> 8B5<
AGP_SB_STB      8B5<> 19C5<> 40A5<> 8C2<
AGP_SB_STB_L    8B5<> 19C5<> 40A5<> 8C2<
AGP_ST<2..0>    8B7> 19C5<
AGP_STOP_L      8C7<> 19B7<> 40A5<> 8D2<
AGP_STP_L       19C5<
AGP_SUS_STAT_L_PU 19C5< 19D7<
AGP_TRDY_L      8C7<> 19B7<> 40A5<> 8D2<
AGP_U4RTAP      8A6<
AGP_WBF_F       19B7<>
AGP_WBF_L       8B7< 8C2< 19B7<
AIN_L_M         25C4<
AIN_L_P         25C4<
AIN_R_M         25C4<
AIN_R_P         25C4<
AOUTL           25C2> 26B8< 26D7<
AOUTL_BOOMER    26B8<
AOUTL_FILTER    26D7<
AOUTR           25C2> 26A8< 26D7<
AOUTR_BOOMER    26A7<
AOUTR_FILTER    26D7<
ATI_AGP_FBSKEW<1..0> 20C6<>
ATI_AGP_TEST    19C7< 19D5<
ATI_AGP_VREF    8B3< 19D5<
ATI_AGP_VREF_H  8C3<
ATI_AGP_VREF_L  8B3<
ATI_AUXWIN_PU   20C5<> 19D7<
ATI_B           20D5> 31C8<
ATI_BUS_CFG<2..0> 20C6<>
ATI_B_FILTR     31C7<
ATI_C           20C5> 31B4<
ATI_CLKA<1..0>  19A7<> 19A6<
ATI_CLKA_L<1..0> 19A7<> 19A6<
ATI_COMP        20C5> 31B4<
ATI_DIGON       20C5> 31A8<> 31B8<>
ATI_DIGON_L     31A8<>
ATI_DVI_DDC_CLK 20C5<> 31C1<>
ATI_DVI_DDC_DATA 20C5<> 31C1<>
ATI_G           20D5> 31C8<
ATI_GPIO7_SPN   20C6<>
ATI_GPIO8_SPN   20C6<>
ATI_GPIO9_SPN   20C6<>
ATI_GPIO10_SPN  20B6<>
ATI_GPIO11_SPN  20B6<>
ATI_GPIO12_SPN  20B6<>
ATI_GPIO13_SPN  20B6<>
ATI_G_FLTR      31C7<
ATI_HPD         31C1<> 20C5<
ATI_HSYNC       20D5<> 20D7<
ATI_HSYNC_BUF   20C8<>
ATI_INV_ON_L    20C5> 31A8<
ATI_LCDCNTL0_TP 20C6<>
ATI_LCDCNTL1_TP 20C6<>
ATI_LCDCNTL2_TP 20C6<>
ATI_LCDCNTL3_TP 20C6<>
ATI_MEMTEST     19A6<>
ATI_MEMVMODE<1..0> 19A7<
ATI_MPVDD_BYP   21A6<>
ATI_OSC_OE      20B8<
ATI_PVDD_BYP    21D7<>
ATI_R           20D5> 31C8<
ATI_R2SET       20D5> 21D5<
ATI_RSET        20D5> 21D6<
ATI_R_FILTR     31C7<
ATI_SLAVE_VIP   20C6<>
ATI_SSIN_PU     19D7< 20B6<
ATI_SS_PU       19D8< 20A6<
ATI_TEMP        24C8<> 24B7<
ATI_TESTEN      19C7< 20B6<
ATI_VCORE_AGND  20A4<>
ATI_VCORE_BG    20A4<>
ATI_VCORE_CNTL  20A6<>
ATI_VCORE_CNTL_L 20A6<> 20B6<>
ATI_VCORE_FB_SW 20A7<> 20A3<
ATI_VCORE_ITH   20A5<
ATI_VCORE_ITH_RC 20A6<
ATI_VCORE_L_SW  20A5<>
ATI_VCORE_RUN_SS 20A5<>
ATI_VCORE_SENSE 20A5<>
ATI_VCORE_SYNC_FCB 20A5<
ATI_VCORE_TG    20A4<>
ATI_VCORE_VFB   20A4<
ATI_VCORE_VIN   20A5<>
ATI_VMEM_ADDR<13..0> 19C3> 19D3> 22B3<> 22B7<>
               41D5<> 22B4< 22B8< 22C4< 22C8<
ATI_VMEM_CASB_L 19A5> 41D5<> 22B4< 22B8<
ATI_VMEM_CKEB   19A5> 41D5<> 22B4< 22B8<
ATI_VMEM_CLKB<1..0> 19A5<> 42A2<> 22A4< 22A8< 22B4<
               22B8<
ATI_VMEM_CLKB_L<1..0> 19A5<> 42A2<> 22A4< 22A8<
               22B4< 22B8<
ATI_VMEM_CSB_L  19A5> 41D5<> 22B4< 22B8<
ATI_VMEM_DATA<63..0> 19A3<> 19B3<> 19C3<> 22B3<>
               22B7<> 22C3<> 22C7<> 41D5<>
ATI_VMEM_DQMB<7..0> 19A3> 41D5<> 22B4< 22B8< 22C4<
               22C8<
ATI_VMEM_QS<7..0> 19A5<> 19B5<> 22C4<> 22C8<>
               41D5<>
ATI_VMEM_RASB_L 19A5> 41D5<> 22B4< 22B8<
ATI_VMEM_WE_L   19A5> 41D5<> 22B4< 22B8<
ATI_VSYNC       20D5<> 20D7<
ATI_VSYNC_BUF   20D8<>
ATI_X1CLK_SKEW<1..0> 20C6<>
ATI_Y           20C5> 31B4<
AUD3V_FDBK      25C6<
AUD4V_FDBK      27B5<
AUDIO_OUT_L     26C2<
AUDIO_OUT_R     26C2<
AUDIO_REF       27C3<
AUDIO_REF_2V    27C2<
AUDIO_REF_3V    27C2<
AUDIO_RESET_L   16C4<> 16C5< 25B4<
BATT_CLK        35B8<
BATT_DATA       35B8<
BATT_ENABLE_L   35A3<>
BATT_FET2_GATE  35B4<>
BATT_FET_DRAIN  35A3<>
BATT_FET_GATE   35B3<>
BATT_FET_SW     35B4<> 43C6<>
BATT_IN_PD      35B7<
BATT_ISNS       43C6<> 36D4<
BATT_LINE       35B2<> 43C6<> 36D5<
BATT_NEG        43C6<> 35B8<
BATT_OK         35A7<
BATT_OK_REF     35A7<
BATT_POS        43C6<> 35B8<
BATT_POS_F      35B7<> 37A8<> 43C6<>
BATT_RC         35A2<>
BATT_RES        35B6<> 43C6<>
BATT_V_GOOD     35A6<
BA_0            7C6> 40C5<> 7B5<
BA_1            7C6> 40C5<> 7C5<
BBATT_ENABLE    36C2<> 37A8<
BBATT_ENABLE_ESD 37A7<>
BBATT_EN_L      37A7<>
BF_FET_G        36B2<>
BOOMER_STAR_GND 26A3<> 43A4<> 26B5<
BRIGHT_INV      31A7<>
BRIGHT_INV_BUF  31A7<>
BT_USB_DM       30C2<> 42B2<> 16C1< 16D1<
BT_USB_DP       30C2<> 42B2<> 16C1< 16D1<
BYPASS_R_GATE   35A5<>
BYPASS_R_L      35A5<
CAPSLOCK_LED    33D3<
CAPSLOCK_LED_L  33D2< 34C7<
CAS_DQM0_L      7C6> 40C5<> 7D5<
CAS_DQM1_L      7C6> 40C5<> 7D5<
CAS_DQM2_L      7C6> 40C5<> 7D5<
CAS_DQM3_L      7C6> 40C5<> 7D5<
CAS_DQM4_L      7C6> 40C5<> 7D5<
CAS_DQM5_L      7C6> 40C5<> 7D5<
CAS_DQM6_L      7C6> 40B5<> 7D5<
CAS_DQM7_L      7C6> 40B5<> 7C5<
CBUS_ADDR<25..0> 18A4> 18B1<> 18B2<> 18B4> 18C1<>
               18B4<
CBUS_ADDR_16_UF 18B5<>
CBUS_BVD1_L     18B2<> 18C4<
CBUS_BVD2_L     18B2<> 18C4<
CBUS_CE1_L      18C1<> 18C4>
CBUS_CE2_L      18C2<> 18C4>
CBUS_DATA<15..0> 18A2<> 18A4<> 18B1<> 18B2<> 18C1<>
               18C2<>
CBUS_DET_1_L    18C2<> 18C4<
CBUS_DET_2_L    18A2<> 18C4<
CBUS_INPACK_L   18B2<> 18C4<
CBUS_INT_L      16B4<> 18A7<> 16B5<
CBUS_IORD_L     18C2<> 18C4>
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CBUS_IOWR_L     18B2<> 18C4>
CBUS_MFUNC1_PD  18A7<> 18D7<
CBUS_MFUNC2_PD  18A7<> 18C7<
CBUS_MFUNC3_PD  18A7<> 18C7<
CBUS_MFUNC4_PD  18A7<> 18C7<
CBUS_MFUNC5_PD  18A7<> 18C7<
CBUS_MFUNC6_PD  18A7<> 18C7<
CBUS_OE_L       18C1<> 18C4>
CBUS_PCI_GNT_L  9C5> 18A7<
CBUS_PCI_IDSEL  18B7<
CBUS_PCI_REQ_L  18A7> 9C2< 9D5<
CBUS_PCI_RESET_L 18B7<
CBUS_READY      18B1<> 18C4<
CBUS_REG_L      18B2<> 18C4>
CBUS_RESET_L    18B2<> 18C4>
CBUS_SUSPEND_PU 18A7< 18D7<
CBUS_VCCD0_L    18C5<
CBUS_VCCD1_L    18C5<
CBUS_VPPD0      18C5<
CBUS_VPPD1      18C5<
CBUS_VS1        18C2<> 18C4<>
CBUS_VS2        18B2<> 18C4<>
CBUS_WAIT_L     18B2<> 18C4<
CBUS_WE_L       18B1<> 18C4>
CBUS_WP_L       18A1<> 18C4< 18D2<
CHARGE_LED_L    34C6<> 35D7<> 34D7<
CHGR_OUT        36B2<> 43C6<>
CHGR_VSW        36B4<> 43C6<>
CHKSTP_OUT_L    13B3<> 13C2<
CHRG_DSCHG_L    35A4<>
CLK10M_PMU_XIN  34B6<
CLK10M_PMU_XOUT 34B6<
CLK10M_PMU_XOUT_UF 34B7<
CLK14M_IMI_XIN  23B6<> 40C1<>
CLK14M_IMI_XOUT 23B6<> 40C1<>
CLK14M_SERIES   23B7<
CLK18M_KL_PLL   40C1<> 16B4<
CLK18M_KL_UF    40C1<> 16A4<
CLK24M_FW_XIN   29C6<>
CLK24M_FW_XOUT  29C6<>
CLK25M_ENET_XIN 28A6<
CLK25M_ENET_XOUT 28A6<>
CLK27M_ATI      40C1<> 20B6<
CLK27M_ATIMEM_SS 20A7<> 40B1<>
CLK27M_ATIMEM_US 20A8<
CLK27M_ATI_LS1_8 20B7<
CLK27M_ATI_UF   40C1<> 20A8< 20B7<
CLK32K_PMU_XIN  34B3<>
CLK32K_PMU_XOUT 34B3<>
CLK32K_PMU_XOUT_UF 34B2<>
CLK33M_CBUS     40C1<> 18A7< 23B3<
CLK33M_CBUS_UF  40C1<> 23B5<
CLK33M_KL_PCI   40C1<> 16A8< 23B3<
CLK33M_KL_UF    40C1<> 23B5<
CLK33M_NEC      40C1<> 17B7< 23B3<
CLK33M_NEC_UF   40C1<> 23B5<
CLK33M_UNIN_PCI_EXT 40C1<> 9C5< 23B3<
CLK33M_UNIN_PCI_EXT_UF 40C1<> 23B5<
CLK66M_AGP_ATI  40D1<> 19B7< 23B3<
CLK66M_AGP_UF   40D1<> 23B5<
CLK66M_UNIN_AGP 40D1<> 8C7< 23B3<
CLK66M_UNIN_AGP_UF 40D1<> 23B5<
CLK66M_UNIN_PCI_INT 40C1<> 9C5< 23C3<
CLK66M_UNIN_PCI_INT_UF 40D1<> 23B5<
CLKENET_PHY_RX  28B6<> 40B1<>
CLKENET_PHY_TX  28C6<> 40B1<>
CLKLVDS_N       20B5> 31B5<> 42C2<>
CLKLVDS_P       20B5> 31B5<> 42C2<>
CLK_ENET_LINK_RX 40B1<> 10C6< 28B7<
CLK_ENET_LINK_TX 40B1<> 10C6< 28C7<
CLK_PHY_FW      29B6<> 40B1<>
CLK_UNIN_FW     40B1<> 10B2< 29B7<
COMM_DTR_L      16C2> 32B2<>
COMM_GPIO_L     16C2> 32B3<>
COMM_RESET_L    16C4<> 32A3<>
COMM_RING_DET_L 16C4<> 32B4<> 34C6<> 16C5<
COMM_RTS_L      16C2> 32B2<>
COMM_RXD        32B2<> 16C2<
COMM_SHUTDOWN   16B8> 32A4<>
COMM_TRXC       16C2<> 32B3<>
COMM_TXD_L      16C2> 32B3<>
COMP_RC         36B6<
CPU1_INT_L_PU   16C4<> 16B5<
CPU_AACK_L      6B7> 40D5<> 6C2< 13A7<
CPU_ADDR<31..0> 6B7<> 6C7<> 13B7<> 13C7<> 40D5<>
CPU_ARTRY_L     6B7<> 13A7<> 40D5<> 6C2<
CPU_AVDD        13D4<> 43D4<>
CPU_BG_L        6D7> 13C7> 40D5<> 6C2<
CPU_BR_L        13C7> 6C2< 6D7<
CPU_BUS_VSEL    12A6< 13C3<
CPU_CHKS_L      13B3< 13D2<
CPU_CI_L        6B7> 13A7> 40D5<>
CPU_CLKOUT_SPN  13C3>
CPU_CLK_EN      34C4<> 23B6< 23C4<
CPU_DATA<63..0> 6A3<> 6B3<> 6C3<> 6D3<> 14A8<>
               14B8<> 14C8<> 14D8<> 40D5<> 12A3<
CPU_DBG_L       6A3> 40D5<> 6C2< 13C3<
CPU_DRDY_0_L    6A3< 6C2< 13C3<
CPU_DRDY_0_L_UF 13C4<>
CPU_DTI<2..0>   6A3> 40D5<> 13C3<
CPU_EDTI        13A2< 13C3<
CPU_EMODE0_L    12A6< 13A3<
CPU_EMODE1_L    13A3< 13C2<
CPU_GBL_L       6B7> 13A7<> 40D5<>
CPU_HIT_0_L     13A7> 6B7< 6C2<
CPU_HRESET_L    34C4<> 12A5< 13B3< 13C2<
CPU_L1TSTCLK    13B2< 13B3<
CPU_L2TSTCLK    13B3< 13D2<
CPU_L3_VSEL     12A4> 12A6< 14C3<
CPU_LSSD_MODE   13B3< 13D2<
CPU_MCP_L       13B3< 13D2<
CPU_PLL_CFG<3..0> 12D3< 13C3<
CPU_PLL_CFGEXT  12D3< 13C3<
CPU_PLL_FS00    12C3<>
CPU_PLL_FS01    12C3<
CPU_PLL_FS10    12C3<
CPU_PLL_STOP_BASE 12C7<
CPU_PLL_STOP_OC 12C8<> 34B6<>
CPU_PMONIN_L    16C4<> 13B3< 13C2<
CPU_PULLDOWN    13C7<> 13A2< 13A3<
CPU_PULLUP      13A3< 13C2<
CPU_QACK_L      6A7> 40D5<> 13B3<
CPU_QREQ_L      13B3> 6A7< 6C2<
CPU_SHD0_L      13A7<> 13D2<
CPU_SHD1_L      13A7<> 13D2<
CPU_SMI_L       34C4<> 13B2< 13B3<
CPU_SRESET_L    16C4<> 13B3< 13C2<
CPU_SRWX_L      13A3< 13C2<
CPU_TA_L        6A3> 40D5<> 6D2< 13B3<
CPU_TBEN        13B3< 13D2<
CPU_TBST_L      6B7<> 13A7> 40D5<>
CPU_TEA_L       6A3> 40D5<> 6D2< 13B3<
CPU_TEMP        24C8<> 24B7<
CPU_TSIZ<2..0>  6B7<> 13A7> 40D5<>
CPU_TS_L        6C7<> 13C7> 40D5<> 6D2<
CPU_TT<4..0>    6B7<> 13A7<> 40D5<>
CPU_VCORE_HI_OC 34D4<> 12B8< 23B6< 39C6<
CPU_VCORE_PWR_SEQ 39D8<>
CPU_VCORE_SEQ   39D8<
CPU_VCORE_SEQ_L 39D8<
CPU_VCORE_SLEEP 13D8<> 43D4<> 13D3< 39C1< 39D2<
CPU_VCORE_SNUB  39B3<
CPU_WT_L        6B7> 13A7> 40D5<>
CSLOT_ADDR<15..0> 16B2> 16B4<> 16C4<> 16C6> 32C6<>
               42C5<> 42D5<> 32C7<
CSLOT_CE1_L     16B6> 32C6<> 42C5<>
CSLOT_CE2_L     16B6> 32C5<> 42C5<>
CSLOT_CS1FX_L   32C6<> 42D5<> 32C7<
CSLOT_CS3FX_L   32C6<> 42D5<> 32C7<
CSLOT_DATA<15..0> 32C5<> 32C6<> 32D5<> 32D6<>
               42D5<> 32D7<
CSLOT_IORD_L    32C5<> 42D5<> 16B1<
CSLOT_IOWAIT_L  32C5<> 42C5<> 16B2<
CSLOT_IOWR_L    32C5<> 42C5<> 16B1<
CSLOT_IRQ_L     16B4<> 32C6<> 42C5<>
CSLOT_REG_L     16B4<> 32C5<> 42C5<>
CSLOT_RESET     16C4<> 32C5<> 42C5<>
CS_1            25B4<
CURRENT_ADJ     36B7<
CY811_S0        20A7<
CY811_S1        20A8<
CY_VCC          24D7<
DCDC_EN         37D7<> 38B8<> 38C8<> 39C7<>
DCDC_EN_L       37D7<>
DVI_DDC_CLK     31C4<> 33A8<>
DVI_DDC_CLK_F   31C3<>
DVI_DDC_DATA    31C4<>
DVI_DDC_DATA_F  31C3<>
```

```
DVI_HPD         31C4<> 33B8<
DVI_HPD_DIV     33B8<
DVI_HPD_F       31C2<>
DVI_PWR_EN_L    33A8<>
DVI_TURN_ON     33A8<>
DVI_TURN_ON_BASE 33A7<
EIDE0_DMACK_L   16B6> 42D5<> 32B8<
EIDE0_DMARQ     42D5<> 16B6< 32B8<
EIDE0_DMA_ACK_L 32A6<> 42C5<> 32B7<
EIDE0_DMA_RQ    32A6<> 42C5<> 32B7<
EIDE0_INT       42D5<> 16B6< 32A8<
EIDE0_INTR      32A5<> 42C5<> 32A7<
EIDE0_RD_L      16B6> 42D5<> 32A8<
EIDE0_READ_L    32A6<> 42C5<> 32A7<
EIDE0_RST_L     16C6> 42D5<> 32A8<
EIDE0_RST_L_OPU 32B5<> 42C5<> 32A7<
EIDE0_WR_L      16B6> 42D5<> 32A8<
EIDE0_WR_L_OPU  32A5<> 42C5<> 32A7<
EIDE1_DMAREQ_PD 16B6<
EIDE1_INT_PD    16B6<
EIDE_ADDR<2..0> 16C6> 42D5<> 32B8< 32C8<
EIDE_ADDR_<2..0> 32A5<> 32A6<> 42C5<> 32B7<
EIDE_CS1FX_L    16C6> 42D5<> 32B8< 32C8<
EIDE_CS1FX_L_OPU 32A5<> 42C5<> 32B7<
EIDE_CS3FX_L    16C6> 42D5<> 32B8< 32C8<
EIDE_CS3FX_L_OPU 32A6<> 42C5<> 32B7<
EIDE_DATA<15..0> 16C6<> 16D6<> 42D5<> 32B7< 32C7<
               32C8< 32D8<
EIDE_DB_<15..0> 32A5<> 32A6<> 32B5<> 32B6<> 42C5<>
               32B8< 32C7< 32C8<
EIDE_DET_PU     16C4<> 16C5<
EIDE_IOCHRDY    42D5<> 16C6< 32A8<
EIDE_IO_CHRDY   32A5<> 42C5<> 32A7<
ENET_AVDD       43B4<> 28C5< 28D4<
ENET_AVDDL      43C4<> 28C6< 28D2< 28D5<
ENET_COL        28B6> 42A5<> 10B6<
ENET_CRS        28B6> 42A5<> 10B6<
ENET_CTAP_CHGND 28B1<
ENET_DVDDL      43B4<> 28C6< 28D4< 28D6<
ENET_ENERGY_DET 16B4<> 28B4<>
ENET_GBE_REFCLK 10B6> 40B1<> 28A7<
ENET_GTX_CLK    10B6<> 40B1<>
ENET_MDC        10B6> 42A5<> 28A4<
ENET_MDIO       10B6<> 28A5<> 42A5<>
ENET_PHY_GBE_REFCLK 28A6<> 40B1<>
ENET_PHY_GTX_CLK 40B1<> 10B7< 28B6<
ENET_PHY_RXD<7..0> 28B6<> 42A5<>
ENET_PHY_TXD<7..0> 42A5<> 10B7< 10C7< 28B6< 28C6<
ENET_PHY_TX_EN  42A5<> 10C7< 28C6<
ENET_PHY_TX_ER  42A5<> 10C7< 28C6<
ENET_PLLVDD     43B4<> 28C5< 28D3<
ENET_PWR_EN_L   28A7<> 28A6<
ENET_RDAC       28D5<>
ENET_RST_L      28A7<
ENET_RXD<7..0>  42A5<> 10B6< 28B7<
ENET_RX_DV      28B6> 42A5<> 10C6<
ENET_RX_ER      28B6> 42A5<> 10B6<
ENET_TX_D<7..0> 10C6<> 42A5<>
ENET_TX_EN      10C6<> 42A5<>
ENET_TX_ER      10C6<> 42A5<>
ENET_WIRESPEED_EN 28A6<
EXTINT6_UNUSED_L 16B4<> 16C5<
EXTVCC_EN_L     36A4<>
FAN1_ON_LOW_L   24C5<>
FAN2_ON_LOW_L   24B3<>
FAN2_PWR        24B1<> 43A6<>
FAN2_PWR_LOW    24B1<> 43A6<>
FAN_1           24C7<> 24D3<>
FAN_2           24B3<> 24C7<>
FAN_PWR         24D1<> 43A6<>
FAN_PWR_LOW     24C2<> 43A6<>
FBA_0           7B2<> 40C5<> 7B4<
FBA_1           7B2<> 40C5<> 7C4<
FBSEL0          23B5<
FBSEL1          23B5<
FBSEL2          23B6<
FB_5_5V_BU      37A5<
FCAS_DQM0_L     7C3<> 40C5<> 7D4<
FCAS_DQM1_L     7C3<> 40C5<> 7D4<
FCAS_DQM2_L     7B3<> 40C5<> 7D4<
FCAS_DQM3_L     7B3<> 40C5<> 7D4<
FCAS_DQM4_L     7C2<> 40C5<> 7D4<
FCAS_DQM5_L     7C2<> 40B5<> 7D4<
FCAS_DQM6_L     7B2<> 40B5<> 7D4<
FCAS_DQM7_L     7B2<> 40B5<> 7C4<
FEEDBACK_1      24C1<> 24C7<>
FEEDBACK_2      24B1<> 24C6<
FEEDBACK_2_F    24C7<>
FET_DRAIN       36B2<
FILTER2_OUTR    26C4<
FILTER2_OUT_L   26C4<
FILTER_OUT_L    26C5<
FILTER_OUT_R    26C5<
FIL_AUD3V       43B4<> 25D4<
FIL_DIG3V       43B4<> 25C4<
FMA_AR<12..0>   7B2<> 7B3<> 7C2<> 7C3<> 40C5<> 7B4<
               7C4<
FMEMWE_L        7C3<> 40B5<> 7C4<
FRAM_CKE0_A     7C2<> 40B5<> 7B4<
FRAM_CKE0_B     7C2<> 40B5<> 7B4<
FRAM_CKE1_A     7C2<> 40B5<> 7B4<
FRAM_CKE1_B     7C2<> 40B5<> 7B4<
FRAS_CS0_L      7C3<> 40C5<> 7C4<
FRAS_CS1_L      7B3<> 40C5<> 7C4<
FRAS_CS2_L      7C3<> 40C5<> 7C4<
FRAS_CS3_L      7B3<> 40C5<> 7C4<
FSDCAS_L        7C2<> 40B5<> 7B4<
FSDRAS_L        7C3<> 40B5<> 7B4<
FW_BIAS0        29B4<>
FW_C_LKON       10B2<> 16B4<> 29B4<>
FW_F0           29C5<>
FW_F1           29C5<>
FW_LINK_CNTL<1..0> 10B2<> 42A5<> 29B7<
FW_LINK_DATA<7..0> 10B2<> 10C2<> 42A5<> 29B7<
FW_LINK_LREQ    10B2> 42A5<> 29B7<
FW_PHY_CNTL<1..0> 29B6<> 42A5<>
FW_PHY_CPS      29C5<
FW_PHY_DATA<7..0> 29B6<> 42A5<>
FW_PHY_LPS      10B2> 29B6<
FW_PHY_LREQ     42A5<> 29B6<
FW_PHY_PD       16C4<> 29B6<
FW_PHY_RST_L    29B6<
FW_PHY_SE       29B6<
FW_PWREN        29C7<
FW_PWREN_L      29C6<
FW_PWR_GATE     29D7<>
FW_R0           29C4<>
FW_R1           29C4<>
FW_TEST         10B2<> 10A7<
FW_TPA0N        29B4<> 42D2<>
FW_TPA0P        29B4<> 42C2<>
FW_TPB0         29B2<
FW_TPB0N        29B4<> 42C2<>
FW_TPB0P        29B4<> 42C2<>
FW_TPI1N        29A3<> 29B2<> 42C2<>
FW_TPI1P        29A3<> 29B2<> 42C2<>
FW_TPO1N        29A3<> 29B2<> 42C2<>
FW_TPO1P        29A3<> 29B2<> 42C2<>
FW_VGND         29B2<> 43B4<>
FW_VP           29B2<> 43B4<>
GND_GALVA       27C5<
GND_HZ          27C6<
GND_REF         24C8<> 24A8< 24B8<
GTR_THAN_13V_RC 36A5<>
GTR_THAN_13_0V  35C2<> 36A5<> 36B1<>
HD_ADDR<2..0>   32C1<> 32C2<> 42B5<> 32D3<
HD_CS1_L        32C2<> 42B5<> 32D3<
HD_CS3_L        32C1<> 42B5<> 32C3<
HD_DATA<15..0>  32D1<> 32D2<> 42B5<> 32D3<
HD_DIOR_L       32C2<> 42B5<> 32C3<
HD_DIOW_L       32C2<> 42B5<> 32C3<
HD_DMACK_L      32C2<> 42B5<> 32C3<
HD_DMARQ        32D2<> 42B5<> 16A5<
HD_INTRQ        32C2<> 42B5<> 16A5<
HD_IOCHRDY      32C2<> 42B5<> 16A5<
HD_RESET_L      32D2<> 42B5<> 32C3<
HOLE_22R10A     5B2<> 5C3<>
HOLE_22R10D     5B2<> 5C3<>
HPD_4V_REF      33B7<
HPD_PWR_SNS_EN  20B6<> 33A8<>
HPD_PWR_SW      33B6<
HPD_PWR_SW_BASE 33A6<
HPD_PWR_SW_OPT  33A6<
HPD_REF_EN_L    33B7<
HPD_REF_EN_L_OPT 33B7<>
HPD_REF_EN_L_OPT2 33A7<>
HP_AMP_SVCC_STAR_GND 26A4<> 43A4<> 26B5<
HP_DET          26D3<
```

```
HP_DET_CONN     26C2<
HP_SENSE_NEG_INPUT 26D3<
HP_SENSE_POS_INPUT 26D4<
IAC_FB          36C7<
IAC_RC_COMP     36C6<
IBATTX0_65      36D4<>
IBATT_FB        36D5<
IBATT_RC_COMP   36D6<
IBATT_SERVO     36D5<
ICHRG_REG       36C6<>
IINX0_62        36C7<>
IMI_CPUSD_STP_L 23C4<
INPUT14_24V_SW  43D6<> 35D2< 36C8<
IO_RESET_L      34C6<> 16B8< 17B7< 18B7< 19B7<
               28A7< 34D7<
ITH_1625        36D6<>
JTAG_ASIC_TCK   10A7< 10B6< 16A2< 28A4<
JTAG_ASIC_TDI   10A7< 10B6<
JTAG_ASIC_TDO_SPN 28A4>
JTAG_ASIC_TMS   10A7< 10B6< 16A2< 28A4<
JTAG_ASIC_TRST_L 10A7< 10B6< 16A2< 28A4<
JTAG_CPU_RST_L  13B2< 13B3<
JTAG_CPU_TCK    13B2< 13C3<
JTAG_CPU_TDI    13B2< 13C3<
JTAG_CPU_TDO_TP 13C3>
JTAG_CPU_TMS    13B2< 13C3<
JTAG_ENET_TDI   16A2> 28A4<
JTAG_KL_TDI     10B6> 16A2<
JTAG_L3_SRAM2_TDI 15B6> 15B3<
JTAG_L3_TCK     15B3< 15B6< 15C7<
JTAG_L3_TDI_TP  15B6<
JTAG_L3_TDO_TP  15B3>
JTAG_L3_TMS     15B3< 15B6<
KBD_CAPSLOCK_LED 33C3<>
KBD_COMMAND_L   33C4<> 34C6<> 33C2<
KBD_CONTROL_L   33C3<> 34C6<> 33C2<
KBD_FUNCTION_L  33C4<> 34B6<> 33C2<
KBD_ID          33C4<> 34B6<> 33D2<
KBD_INTL        33C3<>
KBD_JIS         33C4<>
KBD_NUMLOCK_LED 33C4<>
KBD_OPTION_L    33C3<> 34B6<> 33C2<
KBD_SHIFT_L     33C4<> 34C6<> 33C2<
KBD_X<9..0>     33C3<> 33C4<> 34C6<> 33C2< 33D2<
KBD_Y<7..0>     33C3<> 33C4<> 34C6<> 34D6<>
KL_AGND         16A5<> 43D4<> 16D3< 16D6<
KL_CREF         16B4<
KL_CREF2        16B4< 23B6<
KL_CSLOT_IORD_L 16B3<> 42D5<>
KL_CSLOT_IOWR_L 16B3<> 42D5<>
KL_DEVCS3_SPN   16B6>
KL_DEVCS4_SPN   16B6>
KL_DEV_ID<1..1> 16B4<> 16B5<
KL_DEV_IN_L     16B4<> 16B5<
KL_DIR_245_SPN  16B6>
KL_ENET_RST_L   16C4<> 28A7<
KL_FW_PWREN     16C4<> 16C5< 29C7<
KL_I2C_CLK      16A2<> 25B2<> 32B4<> 16D1<
KL_I2C_DATA     16A2<> 25B2<> 32B3<> 16D1<
KL_IRDA_FIR_L   16C2<> 16C2<
KL_IRDA_LOF     16C2<> 16C2<
KL_IRDA_RXD_L   16C2<
KL_OSC_EN       16A5<
KL_PCI_GNT_L    9C5> 41D5<> 16B8<
KL_PCI_IDSEL    16B8<
KL_PCI_REQ_L    16B8> 9C2< 9C5<
KL_PEND_PROC_INT 16B4> 34C4<>
KL_PLL_EN       16A4< 16C5<
KL_PROC_SLEEP_REQ_L 34B4<> 16B4<
KL_SND_CLKOUT   16B3<>
KL_SND_SCLK     16B3<>
KL_SND_SYNC     16B3<>
KL_SND_TO_AUDIO 16B3<>
KL_SUSPEND_REQ_L 34B6<> 16B4< 34D7<
KL_USB0_PCI_IDSEL 16B8<
KL_USB1_PCI_IDSEL 16B8<
KL_WATCHDOG_L   16A4> 34C6<>
L3_ADDR<17..0>  14D6> 41D5<> 15C3< 15C6< 15D3<
               15D6<
L3_CLK<1..0>    14C3> 40B1<> 15C3< 15C6<
L3_CLK_REF      15B6< 15C3< 15C6<
L3_CNTL<1..0>   14C3> 41D5<> 15C3< 15C6<
L3_DATA<63..0>  14A6<> 14B6<> 14C6<> 15C1<> 15C4<>
               15D1<> 15D4<> 41D5<>
L3_DQPA<1..0>   15C1<> 15C4<> 15C7<
L3_DQPB<1..0>   15C1<> 15C4<> 15C7<
L3_DQPC<1..0>   15C1<> 15C4<> 15C7<
L3_DQPD<1..0>   15C1<> 15C4<> 15C7<
L3_ECHO_CLK<3..0> 15B1<> 15B4<> 40B1<> 14B3<
L3_PULLDOWN<1..0> 15B1< 15B4< 15C3< 15C6< 15C7<
L3_VDD_SLEEP    43D1<> 15A6< 15A8< 15D3< 15D6<
               15D7<
L3_VREF         15B7< 15C3< 15C6<
L3_ZQ<1..0>     15C3< 15C6<
LCD_DIGON_L     31B8<>
LCD_PWREN_L     31B7<>
LCH_GALVA       27D5<
LCH_HZ          27D6<
LID_CLOSED_L    33D6<>
LINE_IN_B       25C4<
LINE_IN_L       25C4< 27D4<
LINE_IN_R       25C4< 27C4<
LINE_OUT_L      26C5<>
LINE_OUT_R      26C5<>
LINE_OUT_STAR_GND 26B3<> 43B4<> 26B8< 26C4< 26C5<
LIN_DET         27B7<
LIN_DET_EMI     27B8< 27D7<
LIN_GND         27C8<>
LIN_LCH         27C8<>
LIN_RCH         27C8<>
LIN_SNS         27C8<>
LT1962_ADJ      14D2<
LT1962_BYPASS   14D2<>
LT1962_SHDN_L   14C3<>
LTC1625_EXTVCC  36A3<> 43C6<> 36C6<
LVDS_DDC_CLK    20C5<> 31A6<>
LVDS_DDC_DATA   20C5<> 31A6<>
LVDS_L0N        20B5> 31B5<> 42C2<>
LVDS_L0P        20B5> 31B5<> 42C2<>
LVDS_L1N        20B5> 31B5<> 42C2<>
LVDS_L1P        20B5> 31B5<> 42C2<>
LVDS_L2N        20B5> 31B5<> 42C2<>
LVDS_L2P        20B5> 31B5<> 42C2<>
LVDS_L3N_SPN    20B5>
LVDS_L3P_SPN    20B5>
L_SPKR_NEG      26A6<>
L_SPKR_POS      26B6<>
MAIN_RESET_L    9A5<> 34D4<> 17A7<
MAX785_EN       37C7<
MAX785_GND      37C7<>
MAX1644_VCC     38B7<
MAX4298_BIAS    26C7<>
MAX4298_CBYPASS 26C7<>
MAX4298_IN1     26D6<
MAX4298_IN2     26D6<
MAX4298_MUTE    26C7<
MAX4298_SVCC    26C6<> 43B4<>
MAX4298_VCC     26C7<> 43B4<>
MB2_IDE_OE_PU   16C4<> 16B5<
MB_IRQ_PU       16B4<> 16C5<
MB_PWREN_L      16C4<> 16C5<
MDI_M<3..0>     28B5<> 28C5<> 42D2<>
MDI_P<3..0>     28B5<> 28C5<> 42D2<>
MEMWE_L         7B6> 40B5<> 7C5<
MEM_DATA<63..0> 7A2<> 7A3<> 7A8<> 7B2<> 7B3<> 7B8<>
               7C2<> 7C3<> 7C8<> 7D2<> 7D3<> 7D8<>
               40C5<>
MEM_EXT_R       7B7<> 40B5<>
MIC_DIFF_IN     27B2<
MIC_DIVIDER     27B2<
MIC_GAINED      27B1<>
MIC_GALVA       27B2<
MIC_HIGH        26A5<> 27B3<
MIC_IN          25C4< 27B1<
MIC_LOW         26A5<> 27B3<>
MIC_POLA        27C3<
MIC_STAR_GND    26B3<> 27B2<> 43B4<>
MODEM_HOOK_PU   16C4<> 16B5<
MODEM_USB_DM    32A3<> 42B2<> 16B1<
MODEM_USB_DP    32B3<> 42B2<> 16B1<
MPIC_CLK        10C2<> 16B4> 41C5<>
MPIC_CPU_INT_L  16B4> 13B2< 13B3<
MPIC_DATA_L     10C2<> 41C5<> 16B4<
MPIC_SYNC_L     10C2<> 16B4>
NEC_AVDD        43D1<> 17D6<
NEC_AVSS        43D1<> 17A5< 17B4< 17D7<
NEC_CRUN_L      17A7<>
NEC_IDSEL       17B7<
```

```
NEC_NANDTEST_TP 17A5<
NEC_OCI<4..3>   17B5< 30C8<
NEC_OCI_UF<4..3> 30C6<>
NEC_OCI_UNUSED  17B5<
NEC_PCI_GNT_L   9C5> 17B7<
NEC_PCI_INT_L   16B4<> 17B7> 16B5<
NEC_PCI_REQ_L   17B7> 9C2< 9D5<
NEC_PME_L       17A7<>
NEC_PPON1_TP    17B5>
NEC_PPON2_TP    17B5>
NEC_PPON5_TP    17B5>
NEC_PPON<4..3>  17B5> 30C8<
NEC_RREF        17B5<>
NEC_RSDCM       17C5<> 42B2<>
NEC_RSDCP       17C5<> 42B2<>
NEC_RSDDM       17C5<> 42B2<>
NEC_RSDDP       17C5<> 42B2<>
NEC_SMI_L_SPN   17A7>
NEC_USB_DCM     17C3<> 42B2<> 30C8<
NEC_USB_DCP     17C3<> 42B2<> 30B8<
NEC_USB_DDM     17C3<> 42A2<> 30A8<
NEC_USB_DDP     17C3<> 42A2<> 30A8<
NEC_XT1         17D5<
NEC_XT2         17D5<>
NEC_XT2_R       17D4<
NUMLOCK_LED     33D5<
NUMLOCK_LED_L   33D5< 34C7<
PBUS_DIV        35C6<
PBUS_DIV1       36B2<
PCI_ACK64_L     9B5< 9B7<
PCI_AD<63..0>   9A4<> 9B4<> 9C4<> 9D4<> 16B8<>
               16C8<> 16D8<> 17B7<> 17C7<> 17C8<>
               17D7<> 18B7<> 18C7<> 23C1<> 40A5<>
               9A7< 9B7< 9C7< 9D7< 23B2< 23C2<
PCI_CBE<7..0>   9B5> 9C5> 16B8<> 17B7<> 18B7<>
               40A5<> 9A7< 9B7< 9C7<
PCI_DEVSEL_L    9C5<> 16B8<> 17B7<> 18B7<> 40A5<>
               9D2<
PCI_FRAME_L     9C5<> 16B8<> 17B7<> 18B7<> 40A5<>
               9D2<
PCI_IRDY_L      9C5<> 16B8<> 17B7<> 18B7<> 40A5<>
               9D2<
PCI_PAR         9C5<> 16B8<> 17B7<> 18B7<> 40A5<>
PCI_PAR64       40A5<> 9B5< 9B7<
PCI_PERR_L      17B7<> 18B7<> 18D7<
PCI_REQ64_L     9B5< 9B7<
PCI_SERR_L      17B7> 18B7> 18D7<
PCI_STOP_L      9C5<> 16B8<> 17B7<> 18B7<> 40A5<>
               9D2<
PCI_TRDY_L      9C5<> 16B8<> 17B7<> 18B7<> 40A5<>
               9D2<
PLL_AVDD        43C4<> 23C5<
PLL_SDRAM_CPU1  43C4<> 23C7<
PLL_STOP_L      12C7<>
PLL_VCC_CPU0    43C4<> 23C5<
PMU_ACK_L       34C4<> 16A2<
PMU_AC_DET      34B4<>
PMU_AC_DET_UF   34B3< 36A8<
PMU_AC_IN       34B4<>
PMU_BACKUP_SELECT_SPN 34C6<>
PMU_BATT0_DET_L 34B4<>
PMU_BATT1_DET_L_PU 34B4<> 34C2<
PMU_BATT_DET_L  34B3< 34D2< 35B7<
PMU_BYTE        34B6< 34C7<
PMU_CAPSLOCK_LED_L 34C6<>
PMU_CHARGE_V    34C4<> 36A3<
PMU_CHRG_BATT_0 34C4<> 35A3<>
PMU_CHRG_EN_L   35C2<>
PMU_CLK         34C4<> 16A2<
PMU_CNVSS       34B6< 34C7<
PMU_EPM         34D4<> 34D2<
PMU_FROM_KL     16B2<> 34C4<>
PMU_I2C_CLK     34B4<> 23B6< 34C2<
PMU_I2C_DATA    34B4<> 23B6< 34C2<
PMU_INT_L       16C4<> 34B6<> 16B5<
PMU_KL_NMI      16B4<> 34D4<> 16C5<
PMU_LID_CLOSED_L 34C4<> 33D5< 34B2<
PMU_NMI_BUTTON_L 34C4<> 34D2<
PMU_NMI_L       34C4<> 34D2<
PMU_NUMLOCK_LED_L 34C6<>
PMU_OOPS        34B4<> 34B2<
PMU_PME_L       10B2> 16B4> 34C4<> 17A8< 34B2<
PMU_POWERUP_OK  34B4<> 34D2<
PMU_POWER_UP_L  34C6<> 34D7< 37D8<
PMU_REQ_L       16A2> 34C4<> 16C5<
PMU_RESET_BUTTON_L 34C4<> 34D2<
PMU_RESET_L     34B6<
PMU_RESET_L_SW  34B7<> 39A4<>
PMU_RESET_UF_L  34B7<
PMU_SLEEP_LED_L 33A5<> 34C4<>
PMU_SMB_CLK     34B4<> 34C2< 35B7<
PMU_SMB_DATA    34B4<> 34C2< 35B7<
PMU_TEMP        34B4<> 24C6< 34B2<
PMU_TEMP_F      24C7<>
PMU_TO_KL       16B2<> 34C4<>
POWER_VALID     34C4<> 34B2<
PS_BST_3V       37C6<
PS_BST_5V       37C6<
PS_CS_3V        43C6<> 37C6<
PS_CS_5V        37C6<
PS_FB_3V        37C6<>
PS_FB_5V        37C6<>
PS_LX_3V        37B5<> 43C6<>
PS_LX_5V        37D5<> 43C6<>
PS_NGATE_3V     37C6<>
PS_NGATE_5V     37C6<>
PS_PGATE_3V     37C6<>
PS_PGATE_5V     37C6<>
PS_REF          37C7<
PS_SS_3V        37C7<
PS_SS_5V        37C7<
PS_SYNC         37C7<
PS_TEMP         24C8<> 24A7<
PS_VL           43C6<> 37D7<
PWR3V_STAR_GND  26A3<> 43B4<> 25A4< 25C5< 25C7<
               25D4<
PWR4V_STAR_GND  26A3<> 43B4<> 27A4< 27B4< 27C1<
               27D4<
PWRBUS_14_24V   29D6<> 36C7<> 43D6<> 36D5<
PWR_STABLE_DELAY 36B1<>
RAD<12..0>      7C6> 7D6> 40C5<> 7B5< 7C5<
RAM_CKE0        7B6> 40B5<> 7B5<
RAM_CKE1        7B6> 40B5<> 7B5<
RAM_CKE2        7B6> 40B5<> 7B5<
RAM_CKE3        7B6> 40B5<> 7B5<
RAS_CS0_L       7C6> 40C5<> 7C5<
RAS_CS1_L       7C6> 40C5<> 7C5<
RAS_CS2_L       7C6> 40C5<> 7C5<
RAS_CS3_L       7C6> 40C5<> 7C5<
RCH_GALVA       27C5<
RCH_HZ          27C6<
RJ45_C0_PD      28C2<>
RJ45_C1_PD      28C2<>
RJ45_C2_PD      28B2<>
RJ45_C3_PD      28B2<>
RJ45_DN<3..0>   28B2<> 28C2<> 42D2<>
RJ45_DP<3..0>   28B2<> 28C2<> 42D2<>
ROM_CS_L        7B6< 23B2<
ROM_OE_L        7A6< 23B2<
ROM_RW_L        7A6< 23B2<
ROM_WP_L        23B2<
RUN/SS          35D1< 36C5<
R_SPKR_NEG      26A6<>
R_SPKR_POS      26A6<>
SCREAMER_OUT_CL_F 26B7<
SCREAMER_OUT_CR_F 26A7<
SDCAS_L         7C6> 40B5<> 7B5<
SDRAS_L         7C6> 40B5<> 7B5<
SLEEP           34B6<> 37C8<> 34D7< 37B3< 38B3<
               38C3<
SLEEP_LED       33A4<>
SLEEP_LED_I     33B3<
SLEEP_LED_L     33B4<
SLEEP_LED_SW    33B5<>
SLEEP_LED_SW_L  33B5<>
SLEEP_LED_UF    33B3<
SLEEP_LS5       37D3<>
SLEEP_LS5_EN_L  37B2<>
SLEEP_L_LS5     28A8<> 37B2<> 39C7<>
SLEEP_L_LS5_EN_L 37B3<>
SNDOUT0_FB      25C3<
SND_AMP_MUTE_L  16C4<> 26A8<
SND_CLKOUT      40C1<> 16A1< 25B4<
SND_HP_MUTE_L   16C4<> 26C8<
SND_HP_SENSE    16B4<> 26D5<
SND_LIN_SENSE   16B4<> 27B6<
SND_SCLK        25B2<> 16B1<
SND_SYNC        25B2<> 16B1<
```

```
SND_TO_AUDIO    16B1< 25C4<
SND_TO_KL       16B2< 25C2<
SOFT_PWR_ON_L   34C6<> 39A4<> 33A6< 33B2< 34D7<
SPKR_STAR_GND   26B3<> 43B4<> 26A8<
SPO_ESD_F       33B2<>
SUDO_GND        27C5<>
SUDO_L          27D4<>
SUDO_L_M        27D5<
SUDO_L_P        27D5<
SUDO_R          27C4<>
SUDO_R_M        27C5<
SUDO_R_P        27C5<
SYSCLK_CPU      40D1<> 13C3< 23C3<
SYSCLK_CPU_UF   40D1<> 23B5<
SYSCLK_DIMM0_A  7C3<> 40D1<> 23C3<
SYSCLK_DIMM0_A_UF 40D1<> 23B5<
SYSCLK_DIMM0_B  7B2<> 40D1<> 23C3<
SYSCLK_DIMM0_B_UF 40D1<> 23B5<
SYSCLK_DIMM1_A  7C3<> 40D1<> 23C3<
SYSCLK_DIMM1_A_UF 40D1<> 23B5<
SYSCLK_DIMM1_B  7B2<> 40D1<> 23C3<
SYSCLK_DIMM1_B_UF 40D1<> 23B5<
SYSCLK_UNIN     40D1<> 6D7< 23C3<
SYSCLK_UNIN_RDCLK 7B6> 40D1<> 23C3<
SYSCLK_UNIN_RDCLK_UF 40D1<> 23B5<
SYSCLK_UNIN_UF  40D1<> 23B5<
SYSTEM_CLK_EN   34C4<> 19C4< 23B6<
TAS_SNDOUT0     25C2<>
TI_AVSS         26B3<> 43B4<> 25A4<
TI_CAP          25B4<
TI_CAP_PLL      25B4<
TI_VCOM         25B3<>
TI_VRFILT       25B3<>
TMDS_CLKN       20B6> 31D6<> 42C2<> 20D4<
TMDS_CLKN_F     31C5<> 31D5<> 31D7<
TMDS_CLKP       20B6> 31D6<> 42C2<> 20D3<
TMDS_CLKP_F     31C5<> 31D5<> 31D6<
TMDS_CLK_CMT    20D4<
TMDS_DN<2..0>   20B6> 31D4<> 31D5<> 42C2<> 20D7<
               31D7<
TMDS_DP<2..0>   20B6> 31D4<> 31D5<> 42C2<> 20D6<
               31D6<
TPAD_F_RXD      33C7<>
TPAD_F_TXD      33D7<>
TPAD_GND        33C6<> 43A6<>
TPAD_RXD        34C4<> 33C8< 34B2<
TPAD_TXD        34C4<> 33D8< 34B2<
TPS2211_SHDN_L_PU 18D5<
TV_C            31B1<>
TV_COMP         31B1<>
TV_GND1         31B1<> 43A6<>
TV_GND2         31A1<> 43A6<>
TV_Y            31B1<>
T_FILTR_OUT_L   26C3<
T_FILTR_OUT_R   26C3<
T_FILTR_RL      26C3<
UATA_DET_PD     16C4<> 16B5<
UIDE_ADDR<2..0> 16A6> 42B5<> 32D4<
UIDE_CS1FX_L    16A6> 42B5<> 32D4<
UIDE_CS3FX_L    16A6> 42B5<> 32C4<
UIDE_DATA<15..0> 16A6<> 16B6<> 42B5<> 42C5<> 32D4<
UIDE_DIOR_L     16A6> 42B5<> 32C4<
UIDE_DIOW_L     16A6> 42B5<> 32C4<
UIDE_DMACK_L    16A6> 42B5<> 32C4<
UIDE_DMARQ      42B5<> 16A6<
UIDE_INTRQ      42B5<> 16A6<
UIDE_IOCHRDY    42B5<> 16A6<
UIDE_RST_L      16A6> 42B5<> 32C4<
UNIN_AGP_VREF   8A5< 19B7<
UNIN_AGP_VREF_H 19C7<
UNIN_AGP_VREF_L 19B7<
UNIN_BR_1_L_PU  6B2< 6C7<
UNIN_DRDY_1_L_PU 6A3< 6B2<
UNIN_HIT_1_L_PU 6A7< 6B2<
UNIN_I2C_CLK0   7A2<> 10B6<> 24B4<> 24B6<> 10D7<
UNIN_I2C_CLK1   7A2<> 10A6<> 24C7<> 24D6<> 10D7<
UNIN_I2C_DATA0  7A3<> 10B6<> 24B4<> 24B6<> 10D7<
UNIN_I2C_DATA1  7A3<> 10A6<> 24C7<> 24D6<> 10D7<
UNIN_JTAG_TEI   10A7< 10B6<
UNIN_MAXBUS_REF 6A7< 12A3<
UNIN_PU_RESET_L 34C4<> 10C2< 34A2<
UNIN_QREQ_1_L_PD 6A7< 6B2<
UNIN_RESET_L    34D4<> 10C2< 23B2< 34A2<
UNIN_SPARE_AB6  6A7<
UNIN_SUSPEND_ACK_L 6A7> 34B6<>
UNIN_SUSPEND_REQ_L 34B6<> 6A7< 34C7<
UNI_AGP_PME_L_PD 8B2< 8B7<
UNI_AGP_TYPEDET_PD 8B2< 8B7<
UNI_PCI_GNT2_L_SPN 9C5>
UNI_PCI_GNT3_L_SPN 9C5>
UNI_PCI_GNT4_L_SPN 9C5>
UNI_PCI_REQ_L_PU 9C2< 9C5<
UNI_ROM_CS_L    7A7<>
UNI_ROM_OE_L    7A7<>
UNI_ROM_RW_L    7A7<>
USB_D1M         30B7<> 42B2<>
USB_D1M_EMI     30B5<> 42B2<>
USB_D1P         30B7<> 42B2<>
USB_D1P_EMI     30B5<> 42B2<>
USB_D2M         30B7<> 42B2<>
USB_D2M_EMI     30B5<> 42B2<>
USB_D2P         30B7<> 42B2<>
USB_D2P_EMI     30B5<> 42B2<>
USB_DAM         16C2<> 42C2<> 30B8<
USB_DAP         16C2<> 42B2<> 30B8<
USB_DBM         16C3<> 42B2<>
USB_DBP         16C3<> 42B2<>
USB_DCM         16B2<> 42B2<> 30B8<
USB_DCP         16B2<> 42B2<> 30B8<
USB_DDM         16B3<> 42B2<>
USB_DDP         16B3<> 42B2<>
USB_OC_AB_L     16C2< 16D1<
USB_OC_CD_L     16B2< 16D1<
USB_PWREN_AB_L  16C2> 16D1<
USB_PWREN_CD_L  16B2> 16D1<
USB_SW_ENABLE   30D6<
USB_SW_ENABLE_L 30D5<>
VCORE_BOOST     39C4<> 43B6<>
VCORE_BST       39C5<>
VCORE_CC        39B6<> 43B6<>
VCORE_D0        39A3<> 39B6<
VCORE_D1        39A3<> 39B6<
VCORE_D2        39A3<> 39B6<
VCORE_D3        39A3<> 39B6<
VCORE_D4        39A3<> 39B6<
VCORE_DH        39B5<> 43B6<>
VCORE_DL        39B5<> 43B6<>
VCORE_FB        43B6<> 39B5<
VCORE_GND       39B5<> 43B6<>
VCORE_GNDA      39B6<>
VCORE_GNDDIV    43B6<> 39A5< 39B5<
VCORE_GNDDIV_TEST 39A4<>
VCORE_GNDSNS    39A1<> 43B6<> 39A5<
VCORE_GNDSNS_TEST 39A4<>
VCORE_ILIM      39C6<> 43B6<>
VCORE_LX        39B5<> 43B6<>
VCORE_REF       39B6<> 43B6<>
VCORE_SHDN_L    39C6<>
VCORE_SNS       39A1<> 43B6<>
VCORE_TIME      39B4<> 43B6<>
VCORE_TON       43B6<> 39B6<
VCORE_VCC       43B6<> 39C6<
VCORE_VGATE     39B4<> 43B6<>
VCORE_VPLUS     39C5<>
VCORE_VSENSE    39B3<>
VGA_B           31C5<> 31C6<
VGA_G           31C4<> 31C6<
VGA_HSYNC       31C5<> 20C8<
VGA_R           31C4<> 31C6<
VGA_VSYNC       31C4<> 20D8<
VREFM           25B4<
VREFP           25B4<
ZENER_GTR_THAN_18V 35A4<> 36B8<>
_VCHRG          36B3<
```

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*** Unit Cross-Reference ***
--- for the entire design --

BS1	MTGHOLE	5B3
BS3	MTGHOLE	5B2
BS5	MTGHOLE	5B2
C1	CAP	31A8
C2	CAP	31B5
C3	CAP	31C7
C4	CAP	31C7
C5	CAP	31C7
C6	CAP	31B5
C7	CAP	26A8
C8	CAP	26A6
C9	CAP	38C7
C10	CAP_P	39C5
C11	CAP_P	30C5
C12	CAP	38C6
C13	CAP_P	36D3
C14	CAP	26D6
C15	CAP	26D6
C16	CAP	38C8
C17	CAP	15A5
C18	CAP	15B1
C19	CAP	27B7
C20	CAP_P	20A3
C21	CAP_P	20A3
C22	CAP	36D5
C23	CAP	27B3
C24	CAP	38B7
C25	CAP	25D6
C26	CAP	38B6
C27	CAP	38A6
C28	CAP	29B6
C29	CAP	29C5
C30	CAP	24C8
C31	CAP	24C8
C32	CAP	38B7
C33	CAP	38A7
C34	CAP	38B7
C35	CAP	28D4
C36	CAP_P	36D2
C37	CAP_P	36C3
C38	CAP	37A5
C39	CAP	24D8
C40	CAP	15B3
C41	CAP	37A5
C42	CAP	24C8
C43	CAP_P	26C5
C44	CAP	15B4
C45	CAP	38C3
C46	CAP	37A4
C47	CAP	37A5
C48	CAP	38C3
C49	CAP	36C4
C50	CAP	14B2
C51	CAP	15A8
C52	CAP_P	20A6
C53	CAP	15A7
C54	CAP	24B5
C55	CAP	24B5
C56	CAP	38B2
C57	CAP	38B3
C58	CAP_P	37B4
C59	CAP	31A6
C60	CAP	15A7
C61	CAP	36B5
C62	CAP_P	37B3
C63	CAP_P	36B4
C64	CAP	35B3
C65	CAP	36B6
C66	CAP_P	39B1
C67	CAP	37D2
C68	CAP	37D2
C69	CAP_P	39B2
C70	CAP_P	39B1
C71	CAP_P	39B2
C72	CAP_P	39B1
C73	CAP	22C1
C74	CAP	23C6
C75	CAP	23C6
C76	CAP	23C7
C77	CAP	23C7
C78	CAP	23C8
C79	CAP	23C7
C80	CAP_P	37D2
C81	CAP_P	37C2
C82	CAP	39B4
C83	CAP	24D5
C84	CAP	24C5
C85	CAP	36B3
C86	CAP	23C1
C87	CAP	18B2
C88	CAP	18C2
C89	CAP	23C1
C90	CAP	23C2
C91	CAP	23C5
C92	CAP	23C6
C93	CAP	23C7
C94	CAP	23C5
C95	CAP	23C5
C96	CAP	23C6
C97	CAP	23C6
C98	CAP	23C6
C99	CAP	23C7
C100	CAP	23C1
C101	CAP_P	37C4
C102	CAP	36B3
C103	CAP	18D5
C104	CAP	18D7
C105	CAP	18D7
C106	CAP	18D6
C107	CAP	18D5
C108	CAP	18D6
C109	CAP	23C2
C110	CAP	17B3
C111	CAP	17B3
C112	CAP	17B3
C113	CAP	25C6
C114	CAP	18B3
C115	CAP	18B2
C116	CAP	18B3
C117	CAP	18D7
C118	CAP	18D6
C119	CAP	25B5
C120	CAP	25B4
C121	CAP	18D6
C122	CAP	17B3
C123	CAP	17B3
C124	CAP_P	36B2
C125	CAP	18D5
C126	CAP	16D2
C127	CAP	17B2
C128	CAP	17D6
C129	CAP	18D6
C130	CAP	17D6
C131	CAP	16D4
C132	CAP	16D5
C133	CAP	16D4
C134	CAP	16D4
C135	CAP	17B2
C136	CAP	17B2
C137	CAP	18D6
C138	CAP	18D5
C139	CAP	16D2
C140	CAP	17B2
C141	CAP	17B2
C142	CAP	18D7
C143	CAP	16D2
C144	CAP	16D5
C145	CAP	25B4
C146	CAP	17B2
C147	CAP	18A2
C148	CAP	18D5
C149	CAP	16D3
C150	CAP	16D4
C151	CAP	25D4
C152	CAP	18D5
C153	CAP	16D3
C154	CAP	16D7
C155	CAP	16C2
C156	CAP	17D4
C157	CAP	17D5
C158	CAP	16A6
C159	CAP	31B2
C160	CAP	31A2
C161	CAP	31B2
C162	CAP	31B2
C163	CAP	31C4
C164	CAP	30B4
C165	CAP	30B5
C166	CAP	30B5
C167	CAP	30B4
C168	CAP	30B4
C169	CAP	30B5
C170	CAP	30A5
C171	CAP	30B4
C172	CAP	31B2
C173	CAP	26C3
C174	CAP	29B2
C175	CAP	28B2
C176	CAP	23B3
C177	CAP	31B3
C178	CAP	31B3
C179	CAP	21A5
C180	CAP	21A6
C181	CAP	34B7
C182	CAP	26C2
C183	CAP	26C3
C184	CAP	30D5
C185	CAP	35D3
C186	CAP	29B2
C187	CAP	14B2
C188	CAP	31C3
C189	CAP	31C4
C190	CAP	35C4
C191	CAP	30D5
C192	CAP	31D3
C193	CAP	31C6
C194	CAP	31C6
C195	CAP	21A6
C196	CAP	21A5
C197	CAP	22D7
C198	CAP	22D7
C199	CAP	22D6
C200	CAP	22D7
C201	CAP	26C3
C202	CAP	36C8
C203	CAP	29D7
C204	CAP	30D5
C205	CAP	21C3
C206	CAP	21A6
C207	CAP	30C6
C208	CAP	21C1
C209	CAP	21B5
C210	CAP	21B5
C211	CAP	21B6
C212	CAP	21B5
C213	CAP	19A7
C214	CAP	21B6
C215	CAP	22D7
C216	CAP	35C7
C217	CAP	38D7
C218	CAP	38D7
C219	CAP	14A2
C220	CAP	14B2
C221	CAP	29C4
C222	CAP	22D7
C223	CAP	31A5
C224	CAP	31A5
C225	CAP	31B7
C226	CAP	38C7
C227	CAP_P	38B5
C228	CAP	38A7
C229	CAP	11B3
C230	CAP	21B5
C231	CAP	21C2
C232	CAP	21B6
C233	CAP	20B4
C234	CAP	21C2
C235	CAP	21C2
C236	CAP	20B4
C237	CAP	21C2
C238	CAP	21C2
C239	CAP	20C3
C240	CAP	21B3
C241	CAP	22D7
C242	CAP_P	26C5
C243	CAP	11C5
C244	CAP	11C7
C245	CAP	11B2
C246	CAP	11B3
C247	CAP	11B3
C248	CAP	20B2
C249	CAP	22D6
C250	CAP	22D6
C251	CAP	22D6
C252	CAP	38A6
C253	CAP	24C1
C254	CAP	11C7
C255	CAP	11B3
C256	CAP	20B3
C257	CAP	20C3
C258	CAP	20C3
C259	CAP	33A4
C260	CAP	29B3
C261	CAP	29C6
C262	CAP	15B2
C263	CAP	15A6
C264	CAP	11C6
C265	CAP	24C1
C266	CAP	11C3
C267	CAP	19C3
C268	CAP	19B8
C269	CAP	20B4
C270	CAP	20C4
C271	CAP	20B4
C272	CAP	21B7
C273	CAP	20A3
C274	CAP	20A3
C275	CAP	15A3
C276	CAP	15A7
C277	CAP	15A3
C278	CAP	30C8
C279	CAP	30C7
C280	CAP	15A3
C281	CAP	39C1
C282	CAP	39D2
C283	CAP	39C2
C284	CAP	13D5
C285	CAP	39C2
C286	CAP	35C2
C287	CAP	11C8
C288	CAP	11C7
C289	CAP	11C7
C290	CAP	11B3
C291	CAP	11B4
C292	CAP	21B6
C293	CAP	21B2
C294	CAP_P	35C5
C295	CAP	13D4
C296	CAP	11B3
C297	CAP	11B3
C298	CAP	11B2
C299	CAP	20C3
C300	CAP	20C3
C301	CAP	21C6
C302	CAP	21C6
C303	CAP	21C1
C304	CAP	21C3
C305	CAP	14B2
C306	CAP	14A2
C307	CAP	26C2
C308	CAP	36C2
C309	CAP	29B4
C310	CAP	29B4
C311	CAP	29B3
C312	CAP	29B3
C313	CAP	29C4
C314	CAP	15A3
C315	CAP	13D4
C316	CAP	11C7
C317	CAP	11C4
C318	CAP	11B3
C319	CAP	21C6
C320	CAP	20C3
C321	CAP	14B2
C322	CAP	14B2
C323	CAP	28C2
C324	CAP	28C1
C325	CAP	28C2
C326	CAP	28C2
C327	CAP	15A6
C328	CAP	11C6
C329	CAP	11C7
C330	CAP	11C7
C331	CAP	11C6
C332	CAP	11B2
C333	CAP	11C3
C334	CAP	11B2
C335	CAP	20C3
C336	CAP	21C2
C337	CAP	22D3
C338	CAP	22D3
C339	CAP	22D2
C340	CAP	22D2
C341	CAP	35D5
C342	CAP	36C7
C343	CAP	36C6
C344	CAP	29C3
C345	CAP	29C3
C346	CAP	15A4
C347	CAP	13D5
C348	CAP	11B2
C349	CAP	11B3
C350	CAP	11B4
C351	CAP	21C6
C352	CAP	20C4
C353	CAP	29C4
C354	CAP	29C5
C355	CAP	29B3
C356	CAP	28C7
C357	CAP	28C8
C358	CAP	13D6
C359	CAP	11C7
C360	CAP	11C6
C361	CAP	21C6
C362	CAP	21C6
C363	CAP	21A6
C364	CAP	20B3
C365	CAP	22D3
C366	CAP	14A2
C367	CAP	14B1
C368	CAP	26B6
C369	CAP	26B6
C370	CAP	37A6
C371	CAP	36C2
C372	CAP	36C3
C373	CAP	29C4
C374	CAP	28D4
C375	CAP	28C7
C376	CAP	28C7
C377	CAP	28D7
C378	CAP	11C6
C379	CAP	11C7
C380	CAP	11B2
C381	CAP	21C6
C382	CAP	20B4
C383	CAP	22D3
C384	CAP	14B1
C385	CAP	14A1
C386	CAP	26B6
C387	CAP	29C4
C388	CAP	29C3
C389	CAP	29C4
C390	CAP	28D8
C391	CAP	28C7
C392	CAP	28D6
C393	CAP	15B7
C394	CAP	13D5
C395	CAP	11D4
C396	CAP	11B3
C397	CAP	20B3
C398	CAP	20B4
C399	CAP	20C3
C400	CAP	22D3
C401	CAP	36B4
C402	CAP	26B8
C403	CAP	29C4
C404	CAP	29C6
C405	CAP	39C2
C406	CAP	11C7
C407	CAP	11C6
C408	CAP	11C7
C409	CAP	11C8
C410	CAP	11D4
C411	CAP	11D8
C412	CAP	21C5
C413	CAP	20D4
C414	CAP_P	20D4
C415	CAP	20C3
C416	CAP	26A7
C417	CAP	36C2
C418	CAP	36C3
C419	CAP	29D7
C420	CAP	28C8
C421	CAP	28D7
C422	CAP	28D8
C423	CAP	28D3
C424	CAP	15A7
C425	CAP	11C6
C426	CAP	20B3
C427	CAP	20C4
C428	CAP	20B3
C429	CAP	22D3
C430	CAP	22D3
C431	CAP	22D3
C432	CAP	20A5
C433	CAP	36A7
C435	CAP	26D7
C436	CAP	28D3
C437	CAP	28C8
C438	CAP	28D3
C439	CAP	15A4
C440	CAP	15A8
C441	CAP	15A3
C442	CAP	13D7
C443	CAP	13D7
C444	CAP	13D6
C445	CAP	13D6
C446	CAP	13D5
C447	CAP	11C7
C448	CAP	11C5
C449	CAP	11D7
C450	CAP	11D7
C451	CAP	11D6
C452	CAP	11D6
C453	CAP	11D6
C454	CAP	11D5
C455	CAP	11D8
C456	CAP	11B2
C457	CAP	11B2
C458	CAP	21C5
C459	CAP	21D5
C460	CAP	20B4
C465	CAP	26C7
C466	CAP	26C7
C467	CAP	28D3
C468	CAP	28D3
C469	CAP	28D4
C470	CAP	21D7
C471	CAP	21D6
C472	CAP	21D5
C473	CAP	20C4
C474	CAP	20C4
C475	CAP	21A6
C476	CAP	21A5
C477	CAP	20B3
C478	CAP	20B3
C479	CAP	21B2
C480	CAP	21B2
C481	CAP	20A6
C482	CAP_P	38C5
C483	CAP	36C2
C484	CAP	36C2
C485	CAP	28D4
C486	CAP	28D7
C487	CAP	28D7
C488	CAP	28D7
C489	CAP	15A3
C490	CAP	13D7
C491	CAP	13D6
C492	CAP	13D6
C493	CAP	13C7
C494	CAP	11C6
C495	CAP	11C6
C496	CAP	11C6
C497	CAP	11C8
C498	CAP	11D8
C499	CAP	11D6
C500	CAP	11D6
C501	CAP	11D5
C502	CAP	11D7
C503	CAP	11D7
C504	CAP	11D6
C505	CAP	11B8
C506	CAP	11A5
C507	CAP	11B5
C508	CAP	11B6
C509	CAP	11A6
C510	CAP	11A7
C511	CAP	21C8
C512	CAP	20A7
C515	CAP	26C6
C517	CAP	36D6
C518	CAP	28D6
C519	CAP	21C6
C520	CAP	21D8
C521	CAP	21B3
C522	CAP	21B2
C523	CAP	21B2
C524	CAP	20B4
C525	CAP	21D7
C526	CAP	20A6
C528	CAP_P	37B4
C529	CAP	37A3
C530	CAP	28A6
C531	CAP	28D7
C532	CAP	15A7
C533	CAP	15A4
C534	CAP	39C1
C535	CAP	13D7
C536	CAP	13D7
C537	CAP	13D6
C538	CAP	13D7
C539	CAP	13D6
C540	CAP	11C6
C541	CAP	11C6
C542	CAP	11D5
C543	CAP	11D5
C544	CAP	11D6
C545	CAP	11D5
C546	CAP	11D6
C547	CAP	11D5
C548	CAP	11B3
C549	CAP	11B3
C550	CAP	11A8
C551	CAP	21D5
C552	CAP	21D6
C553	CAP	21C8
C554	CAP	21A5
C555	CAP	15A4
C557	CAP	11C6
C558	CAP	11B8
C559	CAP	11A6
C560	CAP	11A7
C561	CAP	11A5
C562	CAP	21C8
C563	CAP	21D5
C564	CAP	21D6
C565	CAP	20A7
C566	CAP	20A5
C567	CAP	20A5
C568	CAP_P	38D5
C569	CAP	36B6
C570	CAP	28A6
C571	CAP	15B4
C572	CAP	13D7
C573	CAP	13D8
C574	CAP	39C2
C575	CAP	11C7
C576	CAP	11C2
C577	CAP	11C2
C578	CAP	11C2
C579	CAP	11D4
C580	CAP	11D8
C581	CAP	11D4
C582	CAP	11A6
C583	CAP	21C7
C584	CAP	21D8
C585	CAP	21D6
C586	CAP	20A5
C587	CAP	20A6
C589	CAP	26D7
C590	CAP	26C7
C592	CAP	13D5
C594	CAP	11B6
C595	CAP	8C3
C596	CAP	34D6
C597	CAP	36B5
C598	CAP_P	37B3
C599	CAP	15B7
C600	CAP	39C1
C601	CAP	13D5
C602	CAP	13D6
C603	CAP	13D5
C604	CAP	39D2
C605	CAP	11C7
C606	CAP	11C7
C607	CAP	6D5
C608	CAP	8D6
C609	CAP	11B2
C610	CAP	11C3
C611	CAP	11A6
C612	CAP	11A7
C613	CAP	11B6
C614	CAP	21D7
C615	CAP	35A2
C616	CAP	15A7
C617	CAP	15A3
C618	CAP	39C1
C619	CAP	11D4
C620	CAP	11D2
C621	CAP	15A3
C622	CAP	13D6
C623	CAP	11C6
C624	CAP	11D2
C625	CAP	11D2
C626	CAP	11C4
C627	CAP	11D2
C628	CAP	11C3
C629	CAP	34D6
C630	CAP	15B3
C631	CAP	13D5
C632	CAP	13D5
C633	CAP	39D2
C634	CAP	11C6
C635	CAP	11C5
C636	CAP	11C7
C637	CAP	6D6
C638	CAP	6D5
C639	CAP	11D3
C640	CAP	11C3
C641	CAP	11C2
C642	CAP	11C3
C643	CAP	11B6
C644	CAP	11B5
C645	CAP	8B3
C646	CAP_P	37B4
C647	CAP	39C2
C648	CAP	11D1
C649	CAP	11D3
C650	CAP	11C2
C651	CAP	11C2
C652	CAP	11D3
C653	CAP	11C1
C654	CAP	8D6
C655	CAP	11A7
C656	CAP	11B7
C657	CAP	8D6
C658	CAP	37D6
C659	CAP	37D6
C660	CAP	37C4
C661	CAP	11C8
C662	CAP	6D6
C663	CAP	11D4
C664	CAP	11D1
C665	CAP	11C3
C666	CAP	11D2
C667	CAP	11A8
C668	CAP	37C6
C669	CAP	37D5
C670	CAP	37A2
C671	CAP	15B3
C672	CAP	15A6
C673	CAP	15A3
C674	CAP	15A3
C675	CAP	15A4
C676	CAP	15A4
C677	CAP	11D3
C678	CAP	11D3
C679	CAP	11C3
C680	CAP	11C1
C681	CAP	11D3
C682	CAP	11D3
C683	CAP	11D3
C684	CAP	11B7
C685	CAP	11B7
C686	CAP	37B1
C687	CAP	15B1
C688	CAP	15B2
C689	CAP	15A5
C690	CAP	15A5
C691	CAP	39C3
C692	CAP	39C3
C693	CAP	39D1
C694	CAP	39D2
C695	CAP	39D2
C696	CAP	39D1
C697	CAP	39D1
C698	CAP	39D2
C699	CAP	39D1
C700	CAP	11D3
C701	CAP	11D2
C702	CAP	11D4
C703	CAP	11D2
C704	CAP	11D3
C705	CAP	8D5
C706	CAP	11B7
C707	CAP	20B7
C708	CAP	20B7
C709	CAP	31A6
C710	CAP_P	37B3
C711	CAP	11C6
C712	CAP	11C4
C713	CAP	11C3
C714	CAP	11D3
C715	CAP	11D2
C716	CAP	11C3
C717	CAP	11D2
C718	CAP	11C3
C719	CAP	31A6
C720	CAP	39C4
C721	CAP	39C3
C722	CAP	11D3
C723	CAP	31A6
C724	CAP	37C2
C725	CAP	39C3
C726	CAP	39D4
C727	CAP	23B7
C728	CAP	37C4
C729	CAP	37D5
C730	CAP	37C7
C731	CAP	35A6
C732	CAP	37C5
C733	CAP	37D5
C734	CAP	23B6
C735	CAP	36B1
C736	CAP	34D5
C737	CAP	39C3
C738	CAP	39D3
C739	CAP	37C7
C740	CAP	37C7
C741	CAP	39B7
C742	CAP	39C4
C743	CAP	16A4
C744	CAP	23C5
C745	CAP	39B4
C746	CAP	39C3
C747	CAP	39D3
C748	CAP	16A5
C749	CAP	36B1
C750	CAP	39B6
C751	CAP	32A4
C752	CAP	32A3
C753	CAP	34A6
C754	CAP	34A7
C755	CAP	39B6
C756	CAP	34B3
C757	CAP	34D5
C758	CAP_P	37C3
C759	CAP_P	37D3
C760	CAP_P	37D3
C761	CAP	39D3
C762	CAP	39C4
C763	CAP	16D4
C764	CAP	16D5
C765	CAP	32A3
C766	CAP	34B2
C767	CAP	37C7
C768	CAP	39B3
C769	CAP	39B3
C770	CAP	25C4
C771	CAP	32A2
C772	CAP	39C5
C773	CAP	39C5
C774	CAP	25D3
C775	CAP	17D6
C776	CAP	17D5
C777	CAP	25C3
C778	CAP	17B3
C779	CAP	18D3
C780	CAP	16D4
C781	CAP	16D5
C782	CAP	16C1
C783	CAP	16C2
C784	CAP	23B6
C785	CAP	33C7
C786	CAP	33C7
C787	CAP	33D7
C788	CAP	33C7
C789	CAP	33C6
C790	CAP	33D6
C796	CAP	27B5
C797	CAP	25C7
C798	CAP	25C5
C799	CAP	25B4
C800	CAP	7D2
C801	CAP	7C2
C802	CAP	7C2
C803	CAP	7B2
C804	CAP	7B2
C805	CAP	7A2
C806	CAP	35A7
C807	CAP	24B4
C808	CAP	24B4
C809	CAP	25C4
C810	CAP	25C4
C811	CAP	25B4
C812	CAP_P	25B2
C813	CAP	25B2
C814	CAP_P	25B2
C815	CAP	25B2
C835	CAP	27C7
C836	CAP	27C7
C837	CAP	27C7
C838	CAP	27D7
C839	CAP	27B6
C840	CAP	27D6
C841	CAP	27C6
C842	CAP	27C6
C843	CAP	27C5
C844	CAP	27D5
C845	CAP_P	27D4
C846	CAP	27D4
C847	CAP	27C4
C848	CAP	27D4
C849	CAP_P	27C3
C850	CAP	27C3
C851	CAP	27B3
C852	CAP	27B2
C853	CAP	27C2
C854	CAP	27C2
C855	CAP	27B1
C856	CAP	27C1
C857	CAP	26D4
C858	CAP	21C3
C859	CAP	21C2
C860	CAP	21C2
C861	CAP	21C2
C862	CAP	21C1
C863	CAP_P	39B2
C864	CAP	13D8
C865	CAP	13D7
C866	CAP	28C8
C867	CAP	28C8
C868	CAP	31C3
C869	CAP	35B4
C871	CAP	38D6
C872	CAP	38B6
C873	CAP	33A8
C874	CAP	36A4
C875	CAP	14D3
C876	CAP	14D2
C877	CAP	14D1
C878	CAP	13C3
C879	CAP	14C2
C880	CAP	14C2
C881	CAP	14C2
C882	CAP	14C1
C883	CAP	14C2
C884	CAP	14C2
C885	CAP	14C2
C886	CAP	14C1
C887	CAP	14B2
C888	CAP	14B2
C889	CAP	31D7
C890	CAP	36C5
C891	CAP	36B7
C892	CAP	20D4
C893	CAP	20D4
C894	CAP	24A1
D1	DIODE_SCHOT	29D6
D2	DIODE	35D3
D3	DIODE	37A4
D4	DIODE_SCHOT	36C4
D5	DIODE	36B3
D6	DIODE_SCHOT	37A4
D7	DIODE_SCHOT	37C4
D8	DIODE_SCHOT	35B6
D9	DIODE_SCHOT	37B5
D10	DIODE_SCHOT	39B3
D11	ZENER_MMBZ15VDLT1	26C2
D13	DIODE_SCHOT	37A7
D14	ZENER_MMBZ15VDLT1	33B2
D15	DIODE_SCHOT	37A7
D16	ZENER	31C7
D17	DIODE_SCHOT	24C2
D18	DIODE_SCHOT	37B6
D19	DIODE_SCHOT_3P	26C6
D20	DIODE	37D5
D21	DIODE	28A7
D22	DIODE	37D6
D23	DIODE_SCHOT	39C4
D24	DIODE_SCHOT	31D4
D25	DIODE_SCHOT	29D5
D26	DIODE	35B4
D27	DIODE_DUAL_6P	29A3 29B3
D28	DIODE_DUAL_6P	29A2 29B2
D29	DIODE_SCHOT	24B1
DP1	DPAK3P	38B8 38C8
DP2	DPAK3P	36A5 36B6 36D6
DP3	DPAK3P_SCHOT	35A2 35A3
DP4	DPAK3P	39C7 39D7
DP5	DPAK3P	35D2 36B1
F1	FUSE	36D4
F2	FUSE	29D5
F3	FUSE	31D5
FL1	FILTER_CHOKE_DUAL	29C2
G1	OSC	20B7
G2	OSC	16A4
J1	CON_F7RT_MINIDIN	31B1
J2	CON_RJ45_SHORT	28C1
J3	CON_4RT_WRIB	30C2
J4	CON_F30RT_T2MT_TH1	31D5
J5	CON_F4RT_USBMINK	30B3
J6	CON_F4RT_USBMINK	30B3
J7	CON_FWVERT_SKT	29C1
J8	CON_F4RT_SDOUT	26C2
J9	CON_M3SM_WRIB	24C1
J10	CON_2MTSM_125	33B1
J11	CON_M06STSM_550S5	18C2
J12	CON_10STSM_S087	32B2
J13	CON_M3SM_WRIB	36D2
J14	CON_F30SM_LPS_J3_PCT	33D4
J15	CON_MSST_BTRY	35B6
J16	CON_1525M_STCKS0	7D3
J17	CON_F20RTSM_20143	31B4
J18	CON_2MTSM_125	33A3
J19	CON_6MTSM_125	26B5
J20	CON_F8RT_S2MT_SM	35D7
J21	CON_10STSM_S087	31A6
J22	CON_12	39A4
J23	CON_F1ST_S2MT_SM	23B8
J24	CON_10STSM_S087	32B3
J25	CON_M70SM_5MM	32D5
J26	CON_M50SM_5MM	32B5
J27	CON_M50SM_5MM	32D2
J31	CON_M3SM_WRIB	24B1
L1	IND	30B5
L2	IND	30B5
L3	IND	30B5
L4	IND	30B5
L5	IND	38B6
L6	IND	20B3
L7	FILTER_4P	31D6
L9	IND	38D6
L10	IND	31B7
L11	IND	36C3
L12	IND	23C8
L13	IND	37B4
L14	IND_3P	37D4
L15	IND_3P	39C2
L16	IND	35B7
L17	IND	35B7
L18	IND	35B7
L19	IND	31B2
L20	IND	31B3
L21	IND	31B2
L22	IND	31C2
L23	IND	31B2
L24	IND	26C3
L25	IND	26C4
L26	IND	29D3
L27	IND	26D3
L28	IND	26C3
L30	FILTER_4P	30C5
L31	FILTER_4P	30A5
L32	IND	31D4
L33	IND	31C6
L34	IND	31C6
L35	IND	31C6
L36	IND	26C4
L37	IND	26C3
L38	I

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R459  RES     36B2
R460  RES     37C2
R461  RES     39D7
R462  RES     8D7
R463  RES     20B6
R464  RES     34D8
R465  RES     37B2
R466  RES     8C1
R467  RES     36A2
R468  RES     36B2
R469  RES     36B2
R470  RES     34C6
R471  RES     39D7
R472  RES     15B3
R473  RES     15B6
R474  RES     34C6
R475  RES     37C1
R476  RES     7B6
R477  RES     20B8
R478  RES     37D4
R479  RES     39A4
R480  RES     39A4
R481  RES     6D6
R482  RES     7B4
R483  RES     7B6
R484  RES     8C1
R485  RES     37B3
R486  RES     37B3
R487  RES     8B1
R488  RES     34B1
R489  RES     34D1
R490  RES     23B7
R491  RES     7B5
R492  RES     35B6
R493  RES     35A6
R494  RES     34B3
R495  RES     34A1
R496  RES     35A3
R497  RES     36B1
R498  RES     34B3
R499  RES     34B1
R500  RES     23B7
R501  RES     23C3
R502  RES     23B3
R503  RES     23B3
R504  RES     23B3
R505  RES     23B3
R506  RES     23B3
R507  RES     23B3
R508  RES     23B4
R509  RES     23B4
R510  RES     23A4
R511  RES     23A4
R512  RES     23B6
R513  RES     35A6
R514  RES     35A6
R515  RES     34B1
R516  RES     34D1
R517  RES     12C7
R518  RES     34D2
R519  RES     34D1
R520  RES     39D7
R521  RES     35A7
R522  RES     35A7
R523  RES     34D5
R524  RES     34B1
R525  RES     34C1
R526  RES     37C7
R527  RES     37D7
R528  RES     23C5
R529  RES     23B6
R530  RES     34D1
R531  RES     34B1
R532  RES     37C7
R533  RES     39B5
R534  RES     32C4
R535  RES     37D7
R536  RES     39B4
R537  RES     39B7
R538  RES     39B7
R539  RES     23C3
R540  RES     23C3
R541  RES     23C3
R542  RES     23C3
R543  RES     23C3
R544  RES     23C3
R545  RES     23C3
R546  RES     16A5
R547  RES     34B3
R548  RES     34B7
R549  RES     34D1
R550  RES     39B7
R551  RES     39B7
R552  RES     12C8
R553  RES     36B2
R554  RES     34D1
R555  RES     34B1
R556  RES     34B1
R557  RES     39C6
R558  RES     39B8
R559  RES     39B8
R560  RES     36B1
R561  RES     34D1
R562  RES     34B3
R563  RES     34B2
R564  RES     34B6
R565  RES     34B7
R566  RES     39B8
R567  RES     39B8
R568  RES     12C7
R569  RES     12C7
R570  RES     16D5
R571  RES     32A3
R572  RES     34C8
R573  RES     37D8
R574  RES     39B5
R575  RES     39C6
R576  RES     39B5
R577  RES     39B8
R578  RES     16A4
R579  RES     34C8
R580  RES     39B6
R581  RES     39B7
R582  RES     39C5
R583  RES     39B3
R584  RES     39C5
R585  RES     33D3
R586  RES     33C3
R587  RES     33D4
R588  RES     37A7
R589  RES     33D4
R590  RES     33D2
R591  RES     18D2
R592  RES     35B8
R593  RES     32D2
R594  RES     32C3
R595  RES     32D4
R596  RES     32C2
R597  RES     32C3
R598  RES     32C3
R599  RES     32D2
R600  RES     32C3
R601  RES     32D2
R602  RES     32C2
R603  RES     16C5
R604  RES     16C5
R605  RES     32C3
R608  RES     20B6
R609  RES     20A6
R610  RES     20A6
R611  RES     20A6
R612  RES     33A7
R613  RES     39C2
R614  RES     25C5
R615  RES     25D4
R616  RES     25D4
R617  RES     25B4
R618  RES     25B4
R619  RES     25C2
R638  RES     27C7
R642  RES     27D6
R643  RES     27C6
R645  RES     27D5
R646  RES     27C5
R647  RES     27C5
R648  RES     27C5
R649  RES     27C5
R650  RES     27C5
```

```
R651  RES     27D4
R652  RES     27C4
R653  RES     27D4
R654  RES     27D3
R655  RES     27B3
R656  RES     27B3
R657  RES     27B2
R658  RES     27D2
R659  RES     27C2
R660  RES     27C2
R661  RES     27B2
R662  RES     27B2
R663  RES     33A8
R664  RES     20A8
R667  RES     20A7
R668  RES     31B8
R669  RES     35B4
R670  RES     35B4
R676  RES     35B3
R677  RES     33D5
R678  RES     33A8
R679  RES     31C3
R680  RES     31C3
R681  RES     31C3
R683  RES     26D4
R684  RES     26D4
R685  RES     36A5
R686  RES     36A4
R687  RES     19C5
R690  RES     20A8
R691  RES     20A8
R692  RES     20A7
R693  RES     28A7
R694  RES     37A8
R695  RES     37A7
R696  RES     14D3
R697  RES     14D3
R698  RES     14D2
R699  RES     14D2
R700  RES     13C3
R701  RES     14D2
R702  RES     14D3
R703  RES     19D8
R704  RES     29B2
R705  RES     20D6
R706  RES     20D6
R707  RES     20D6
R708  RES     20D4
R709  RES     31C4
R710  RES     31C5
R711  RES     30D6
R712  RES     30D6
R713  RES     28A7
R714  RES     16C5
R715  RES     28D3
R716  RES     24B2
R717  RES     24B2
R718  RES     24C3
R719  RES     24C3
R720  RES     33A6
RP1   RPAK4P  13B1 13C1
RP2   RPAK4P  6D1 13D1
RP3   RPAK4P  6B1 6B1 6C1 6D1
RP4   RPAK4P  6B1 6C1
RP5   RPAK4P  28B6 28B6 28B7
RP6   RPAK4P  28B6 28B6 28B7
RP7   RPAK4P  16C5
RP8   RPAK4P  16C5
RP9   RPAK4P  16D1
RP10  RPAK4P  16B5
RP11  RPAK4P  16B5
RP12  RPAK4P  29B6
RP13  RPAK4P  10C6
RP14  RPAK4P  10D8
RP15  RPAK10P2C 9C8
RP16  RPAK4P  9D1
RP17  RPAK4P  9D1
RP18  RPAK4P  29B6
RP19  RPAK4P  10C6
RP20  RPAK10P2C 9C8
RP21  RPAK10P2C 9B8
RP22  RPAK10P2C 9D8
RP23  RPAK10P2C 9B8
RP24  RPAK10P2C 15D8
RP25  RPAK10P2C 33D2
RP26  RPAK10P2C 33C2
RP27  RPAK4P  34C1
RP28  RPAK4P  7C5
RP29  RPAK4P  7C5
RP30  RPAK4P  7C5
RP31  RPAK4P  7C5
RP32  RPAK4P  7D5
RP33  RPAK4P  7D5
RP34  RPAK4P  7C5
RP35  RPAK4P  7B5
RP36  RPAK4P  34D8
RP37  RPAK4P  16C1
RP38  RPAK4P  32D5
RP39  RPAK4P  32D6
RP40  RPAK4P  32C7
RP41  RPAK4P  32D7
RP42  RPAK4P  32C7
RP43  RPAK4P  32D7
RP44  RPAK4P  32B7
RP45  RPAK4P  32D7
RP46  RPAK4P  32C7
RP47  RPAK4P  32D7
RP48  RPAK10P2C 18D8
RP49  RPAK4P  32B7
RP50  RPAK4P  32C7
RP51  RPAK4P  32D3
RP52  RPAK4P  32D3
RP53  RPAK4P  32D3
RP54  RPAK4P  32D3
RP55  RPAK4P  32D3
S2    SWI_AW2195M_H63 34B8
SL1   SLOT    5B3
T1    XFR_ENET_1000BT 28B2
U1    74AHC1G02 31A8
U2    SDRAM_DDR_2MX32 22C5 22C7
U3    AMP_MAX4172 36D4
U4    RAGE_MBLTY_M9_CSP32A13 19D1 19D3 19D6 20D2
                20D5 21B4
U5    TSB41AB1  29C5
U6    VREG_LP2951 37A6
U7    SDRAM_DDR_2MX32 22C1 22C4
U8    TRANSC_ENET_BCM5421BGA100 28C5 28D5
U9    UNI_N_GSBP 6C5 7D7 8C6 9D4 10D4
U10   SCVG8R483 13C5 14D4 14D7
U11   SRAM_DDR_153PBGA 15D2
U12   TRA_SI3447DV 38C3
U13   CY8C26233 24C7
U14   LTC1773   20A4
U15   DS1775    24B5
U16   DS1775    24B5
U17   LTC1625   36C5
U18   VREG_LP2951 37A4
U19   TRA_SI3447DV 38B3
U20   DS1775    24D5
U21   DS1775    24C5
U22   CLK_GEN_CS005 23B5
U23   FEPR_1MX8 23C2
U24   LTC1761   21A7
U25   MAX6328   34B7
U26   COMPARATOR_LMC7211 35C3
U27   COMPARATOR_LMC7211 35C5
U28   741G32    20C7
U29   TEMP_SENS_LM20 24B7
U30   AMP_MAX4172 36C8
U31   LM3526    30C5
U32   741G32    28D7
U33   MAX1644   38D6
U34   AUDIO_LM4863 26A6
U35   TEMP_SENS_LM20 24B7
U36   MAX1644   38B6
U37   COMPARATOR_LMC7211 33B6
U38   TEMP_SENS_LM20 24A7
U39   SN74AUC1G04 12B4
U40   OPAMP_LMC6462 36B7 36D6
U41   LTC1761   21C7
U42   SRAM_DDR_153PBGA 15D5
U43   MAX4298   26C6
U44   COMPARATOR_LMC7211 36A7
U45   LTC1761   21D7
U46   CLK_GEN_CY25811 20A8
U47   M16C62    34D5
U48   MAX785    37C6
U49   COMPARATOR_LMC7211 35A6
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```
U50   MAX1717   39C5
U51   UPD720100_FBGA 17C6
U52   PCI1410AGGU 18C6
U53   KEYLARGO_17X17 16C3 16C7
U54   PWR_CNTRL_TPS2211 18D4
U55   DS1775    24B3
U56   DS1775    24B3
U57   TAS3004   25C3
U58   OPAMP_TLV2362 27C5 27D5
U59   OPAMP_TLV2362 27C1 27C4
U61   COMPARATOR_LMC7211 26D4
U62   VREG_LT1962 14D2
VR1   VREG_LP2951 25D7
VR2   VREG_LP2951 27B5
XH1   MTGHOLE   5C2
XH2   MTGHOLE   5C2
XH3   MTGHOLE   5C2
XH4   MTGHOLE   5C2
XW2   SHORT     26B3
XW3   SHORT     26B3
XW4   SHORT     26B3
XW5   SHORT     26A3
XW6   SHORT     37B4
XW7   SHORT     39B1
XW8   SHORT     39C2
XW9   SHORT     37C4
XW10  SHORT     39B4
XW12  SHORT     20A4
XW13  SHORT     26B3
XW14  SHORT     26A3
XW16  SHORT     20A5
XW17  SHORT     26A3
XW19  SHORT     37C6
XW20  SHORT     16A3
XW21  SHORT     39B4
XW28  SHORT     27B2
XW29  SHORT     26A3
Y1    CRYSTAL   23B6
Y2    CRYSTAL_4PIN 34B3
Y3    CRYSTAL   34B7
Y4    CRYSTAL   29C6
Y5    CRYSTAL   28A6
Y6    CRYSTAL   17D4
ZH1   MTGHOLE   26B3
ZT1   MTGHOLE   5B3
ZT2   MTGHOLE   5D2
ZT3   MTGHOLE   5D3
ZT4   MTGHOLE   5C2
ZT5   MTGHOLE   5D1
ZT6   MTGHOLE   5D3
ZT7   MTGHOLE   5D1
ZT8   MTGHOLE   5D2
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