

M39 - DVT

12/07/05

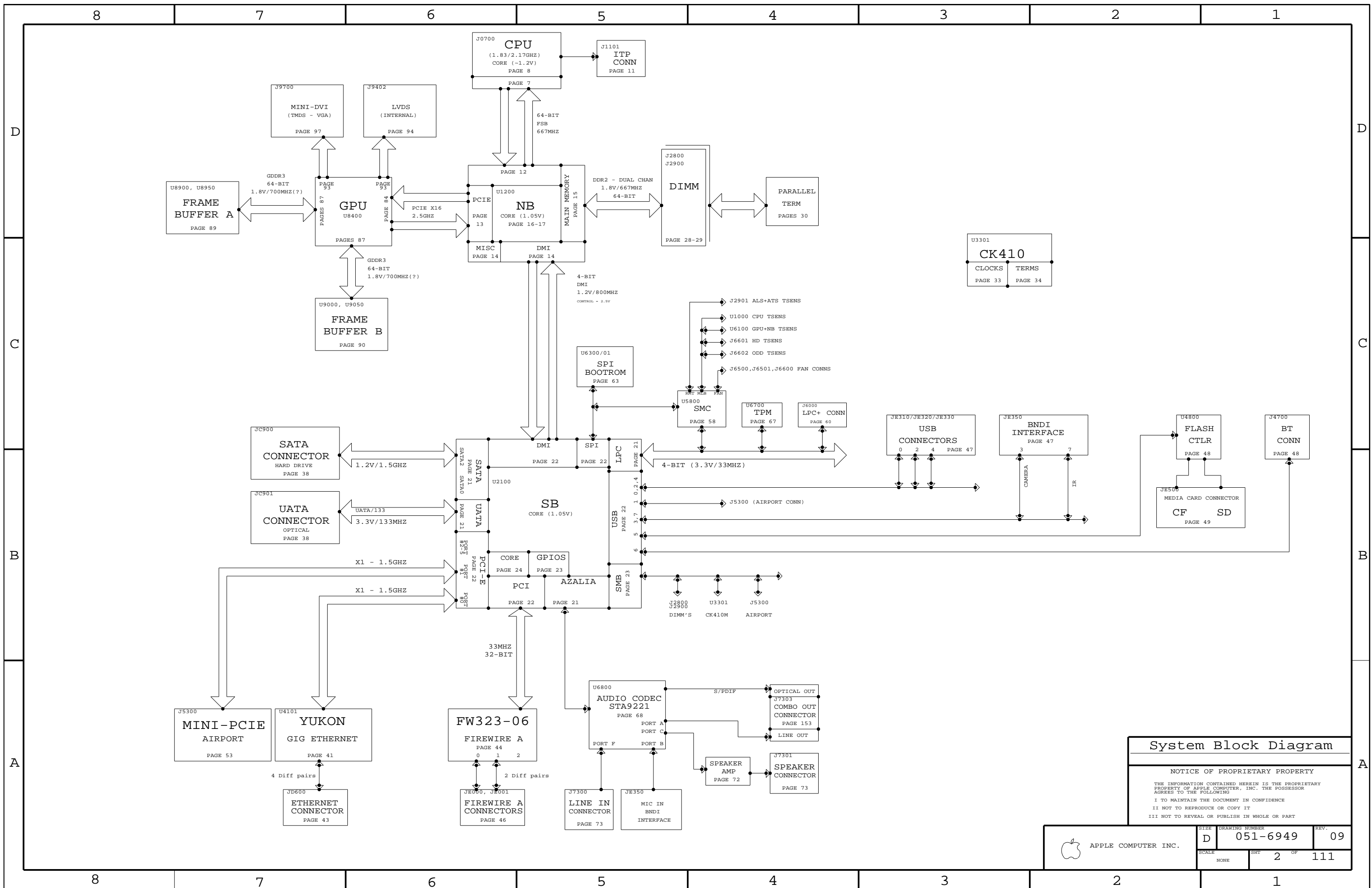
1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
				DATE	DATE
06		400374	ENGINEERING RELEASED	09/16/05	06/22/04

PAGE	DRI	PDF	CIRCUIT
1	JD	JD	1 TABLE OF CONTENTS
2	JD	JD	2 SYSTEM BLOCK DIAGRAM
3	RT	RT	3 POWER BLOCK DIAGRAM
4	JD	JD	4 TABLE ITEMS & REVISION HISTORY
5	JD	JD	5 FUNC TEST
6	RT	RT	6 POWER CONNECTOR / POWER ALIAS
(M42) 7	MS	JD	7 CPU - BUS INTERFACE
(M42) 8	MS	JD	8 CPU - PWR & GND
9	MS	JD	9 CPU - DECAPS
(M42) 10	MS	JD	10 CPU - THERMAL SENSOR
M42 11	MS	JD	11 CPU - ITP CONN
M1 12	PS	JH	12 NB - CPU INTERFACE
M1 13	PS	JH	13 NB - VIDEO INTERFACE
14	PS	JH	14 NB - MISC INTERFACES
M1 15	PS	JH	15 NB - DDR2 INTERFACE
M1 16	PS	JH	16 NB - POWER 1
M1 17	PS	JH	17 NB - POWER 2
M1 18	PS	JH	18 NB - GROUNDS
19	PS	JH	19 NB - DECAPS
M1 20	PS	JH	20 NB - CONFIG STRAPS
21	JD	JD	21 SB - RTC, LAN, AUDIO, ATA, CPU, LPC
22	JD	JD	22 SB - PCIE, SPI, USB, DMI, PCI
23	JD	JD	23 SB - SMB, GPIO, PM, CLKS
24	JD	JD	24 SB - POWERS AND GROUNDS
25	JD	JD	25 SB - DECAPS
26	JD	JD	26 SB - MISC
27	JD	JD	27 SB - SMB BUS CONNECTIONS
28	PS	JD	28 DDR2 - SO-DIMM CONN A
29	PS	JD	29 DDR2 - SO-DIMM CONN B (REVERSED)
30	PS	JD	30 DDR2 - TERMINATION
M1 31	RT	RT	31 DDR2 - VTT SUPPLY
M42 33	JD	JD	33 CLOCKS - GENERATOR
34	JD	JD	34 CLOCKS - TERMINATIONS
38	JD	JD	38 ATA (SATA AND IDE) CONN'S
(M42) 41	JD	JD	41 LAN - YUKON'S PCIE INTERFACE
42	JD	JD	42 LAN - YUKON'S PWR, MISC
43	JD	JD	43 LAN - CONN
44	JD	JD	44 FIREWIRE - FW323-06
45	JD	JD	45 FIREWIRE - DECAPS
46	JD	JD	46 FIREWIRE - CONN'S
47	JD	JD	47 USB - CONN'S
49	JD	JD	49 USB - FLASH CONN

PAGE	DRI	PDF	CIRCUIT
53	JD	JD	43 PCI-E - AIRPORT MINI-PCIE CONN
54	JD	JD	44 PCI-E - UNUSED PORTS
58	MS	MS	45 SMC - H8S2116
59	MS	MS	46 SMC - SMB BUSSES, MISC
60	MS	MS	47 SMC - LPC+ CONN
61	JH	JH	48 SMC - GPU/NB THERMAL SENSOR
RX 63	MS	JD	49 SMC - SPI BOOTROM
65	MS	MS	50 SMC - FANS
66	MS	MS	51 SMC - FANS
67	JD	JD	52 SMC - TPM
SO 68	PT	JD	53 AUDIO - CODEC, VREG, MIC BIAS
SO 72	PT	JD	54 AUDIO - INTERNAL SPEAKER AMP
SO 73	PT	JD	55 AUDIO - I/O CONN'S, EMC
SO 74	PT	JD	56 AUDIO - DETECT TRANSLATORS
RP 75	RT	RT	57 VR - CPU CORE
RP 76	RT	RT	58 VR - CPU I-V SENSE CKT
RP 77	RT	RT	59 VR - "S0" 1.2V & 2.5V (GRAFIX)
RP 78	RT	RT	60 VR - "S0" 1.8V
RP 79	RT	RT	61 VR - "S3" 1.8V
RP 80	RT	RT	62 VR - "S0" 1.5V
RP 81	RT	RT	63 VR - "S0" 1.05V
RP 83	RT	RT	64 VR - "S3" 3.3V AND 5V
JH 84	JH	JH	65 GPU - M56 PCI-E
M1 85	JH	JH	66 GPU - VCORE SUPPLY
M1 86	JH	JH	67 GPU - M56 CORE PWR
M1 87	JH	JH	68 GPU - M56 FRAME BUFFER
M1 88	JH	JH	69 GPU - MISC
M1 89	JH	JH	70 GPU - GDDR SDRAM A
M1 90	JH	JH	71 GPU - GDDR SDRAM B
M1 91	JH	JH	72 GPU - M56 GPIO, DVO, MISC
M1 92	JH	JH	73 GPU - M56 CLOCKS
M1 93	JH	JH	74 GPU - M56 VIDEO INTERFACES
JH 94	JH	JH	75 GPU - INTERNAL DISPLAY CONN'S
JH 95	JH	JH	76 GPU - TP'S
JH 96	JH	JH	77 GPU - TMDS, INVERTER, EXT VGA
JH 97	JH	JH	78 GPU - EXTERNAL DISPLAY CONN'S

<p style="font-size: small;">DIMENSIONS ARE IN MILLIMETERS</p> <p>XX : _____</p> <p>X.XX : _____</p> <p>X.XXX : _____</p> <p>ANGLES : _____</p> <p style="text-align: center; font-size: x-small;">DO NOT SCALE DRAWING</p> <div style="text-align: center;"> <p style="font-size: x-small;">THIRD ANGLE PROJECTION</p> </div>	<p>METRIC</p>	Apple Computer Inc.
<p>DRAPPER</p> <p>ENG APPD</p> <p>QA APPD</p> <p>RELEASE</p>	<p>DESIGN CR</p> <p>MFG APPD</p> <p>DESIGNER</p> <p>SCALE</p>	<p>NOTICE OF PROPRIETARY PROPERTY</p> <p>THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING</p> <p>I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART</p>
<p>SCHEM, M39</p>		<p>TITLE</p>
<p>MATERIAL/FINISH NOTED AS APPLICABLE</p>		<p>SIZE D</p>
<p>DRAWING NUMBER 051-6950</p>		<p>REV. 06</p>
<p>SHT 1 OF 111</p>		

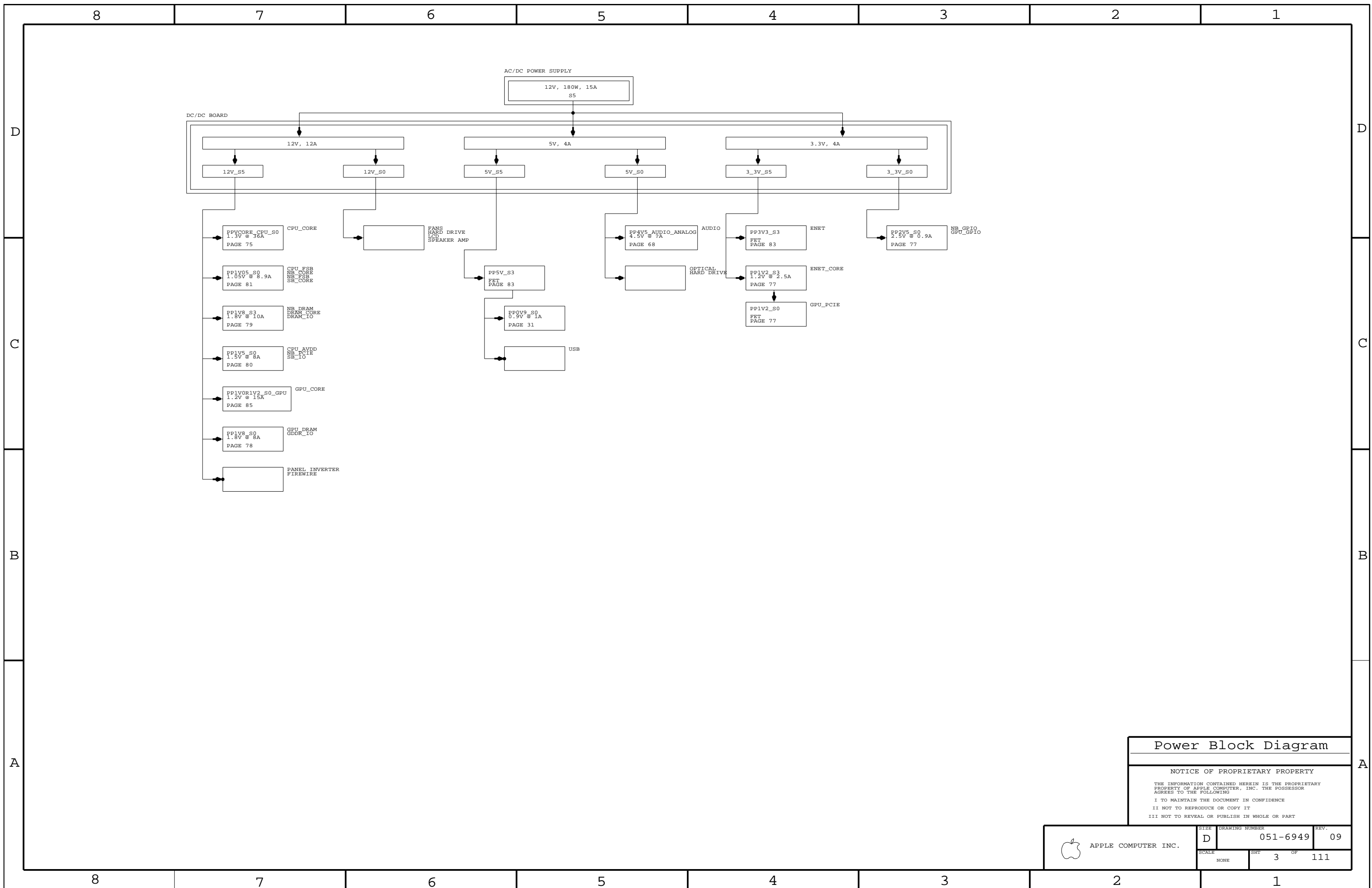


System Block Diagram

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	SCALE NONE	SHEET 2	OF 111



Power Block Diagram

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	D	051-6949	09
SCALE	SHT	OF	
NONE	3	111	

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1

COMMON

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0025	1	IC,CPU-SKT,479BGA	J0700	CRITICAL	
338S0269	1	IC,945GM,NORTHBRIDGE	U1200	CRITICAL	
343S0385	1	IC,SB,652BGA	U2100	CRITICAL	
742-0048	1	BAT,COIN,3V,220MAH,CR2032	BT2600	CRITICAL	
359S0101	1	IC,CY28445-5,CLK GEN,68PIN QFN	U3301	CRITICAL	
338S0270	1	IC,88E8053,1GIGABIT ETHY XCVR,64P QFN,BD	U4101	CRITICAL	
(335S0382) 341S1797	1	IC,ENET LAN ROM	U4102	CRITICAL	
338S0279	1	IC,FW32306,1394A LINK,TQFP	U4400	CRITICAL	
338S0274	1	IC,SMC,HSS/2116,BLANK	U5800	CRITICAL	
341S1789	1	IC,TPM,TSSOP,28P	U6700	CRITICAL	LEMENU
353S1235	1	IC,CPU VREG,IMVP,TWO PHASE	U7500	CRITICAL	
338S0266	1	IC,ATI,M56P,GRAFIX CTLR,880BGA,LF	U8400	CRITICAL	ATI_B24
338S0305	1	IC,ATI,M56P,GRAFIX CTLR,880BGA,LF	U8400	CRITICAL	ATI_A24
128S0078	3	CAP,EL,AL,330UF,20A,16V,10X12.7MM,SMD,LF	C7517,C7518,C7910	CRITICAL	
825-6402	1	LBL,SERIAL NUMBER	X14	CRITICAL	

M38

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-6949	1	PCB,SCHEM,MLB,M38	SCH1		17_INCH_LCD
820-1919	1	PCB,FAB,MLB,M38	MLB1		17_INCH_LCD
(335S0384) 341T0003	1	EFI ROM,M38	U6301	CRITICAL	17_INCH_LCD
114S0287	1	5.11K,1%,1/16W,402,MF-LF	R8522		17_INCH_LCD
337S3242	1	M00-SPEED CPU (QINZ)	CPU	CRITICAL	CPU_M00
337S3241	1	M38/M39 LOW-SPEED CPU (QINY)	CPU	CRITICAL	CPU_M38

M39

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-6950	1	PCB,SCHEM,MLB,M39	SCH1		20_INCH_LCD
820-1888	1	PCB,FAB,MLB,M39	MLB1		20_INCH_LCD
(335S0384) 341T0004	1	EFI ROM,M39	U6301	CRITICAL	20_INCH_LCD
114S0276	1	4.02K,1%,1/16W,402,MF-LF	R8522		20_INCH_LCD
337S3243	1	M39 HI-SPEED CPU (QHJY)	CPU	CRITICAL	CPU_M39

M38 / M39

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0354	4	IC,SURAM,GDDR3,8MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_128M_SAMSUNG
333S0358	4	IC,SURAM,GDDR3,8MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_128M_HYNIX

M39 - CTO

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0350	4	IC,SURAM,GDDR3,16MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_256M_SAMSUNG
333S0351	4	IC,SURAM,GDDR3,16MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_256M_HYNIX

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0096	126S0076		C7801	SANYO W16C680EX 680UF 16V LFP
126S0086	126S0078		C699,C940,C1900,C1901,C1968	SANYO W6CE330F8 330UF 6.3V LFP
128S0080	128S0078		C7517,C7518,C7910	SANYO 160VP330W 330UF 16V SMD LFP
338S0309	338S0266		U8400	IC,ATI,M56LP,GRAFIX CTLR,880PBGA,LF
197S0177	197S0020		Y4101	XTAL,25MHZ,50PFM,16PF,3.220+-5 SMD,LF

124-0338 124-0333 C7501,C8014 CAP,AL,EL,680UF,16V,RAD,10X12.5MM

Table Items

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SCALE	SHT	4 OF	111
NONE			

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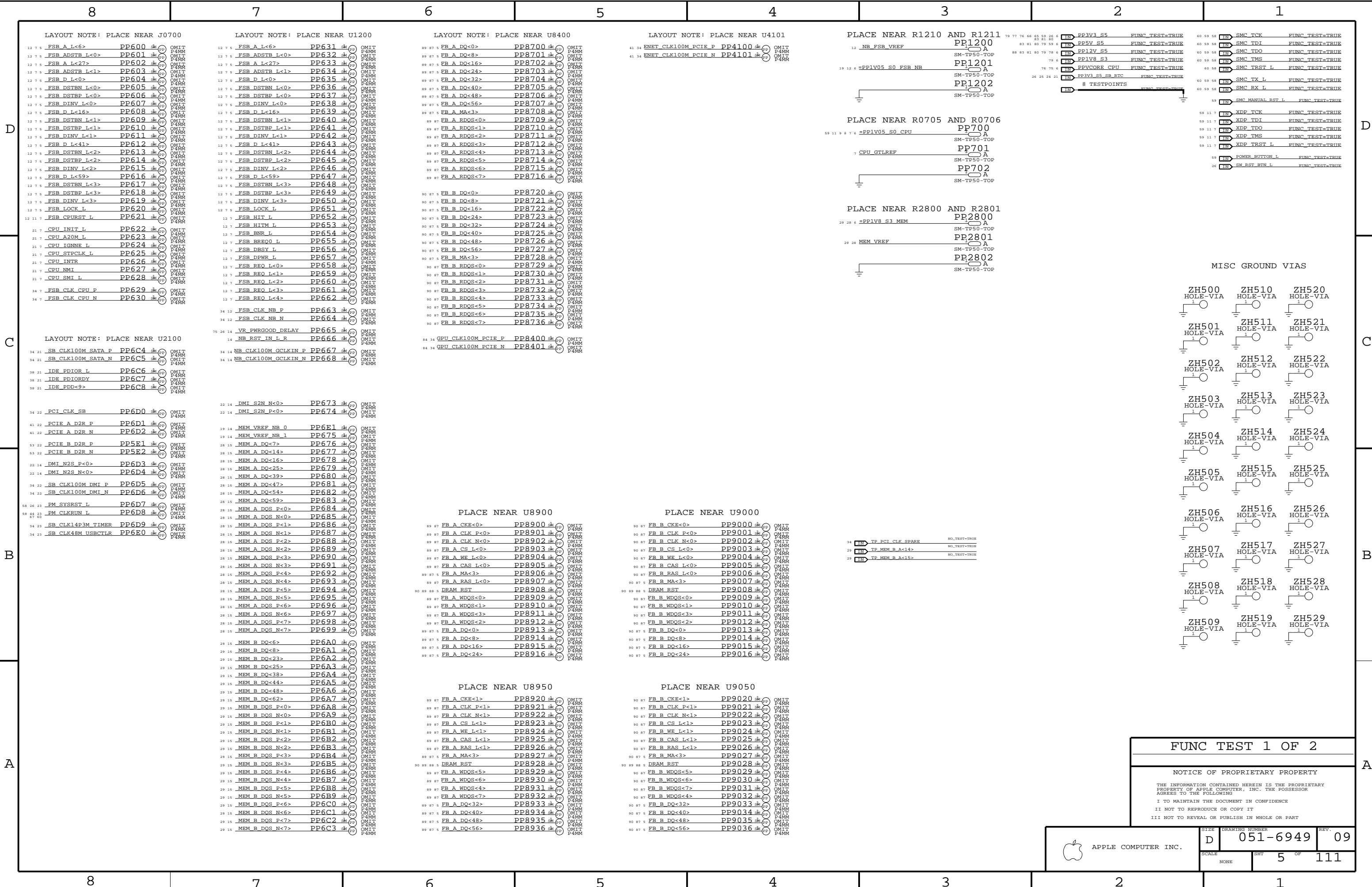
5

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2

1



LAYOUT NOTE: PLACE NEAR J0700

LAYOUT NOTE: PLACE NEAR U1200

LAYOUT NOTE: PLACE NEAR U8400

LAYOUT NOTE: PLACE NEAR U4101

PLACE NEAR R1210 AND R1211

PLACE NEAR R0705 AND R0706

PLACE NEAR R2800 AND R2801

LAYOUT NOTE: PLACE NEAR U2100

LAYOUT NOTE: PLACE NEAR U8900

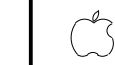
LAYOUT NOTE: PLACE NEAR U9000

LAYOUT NOTE: PLACE NEAR U8950

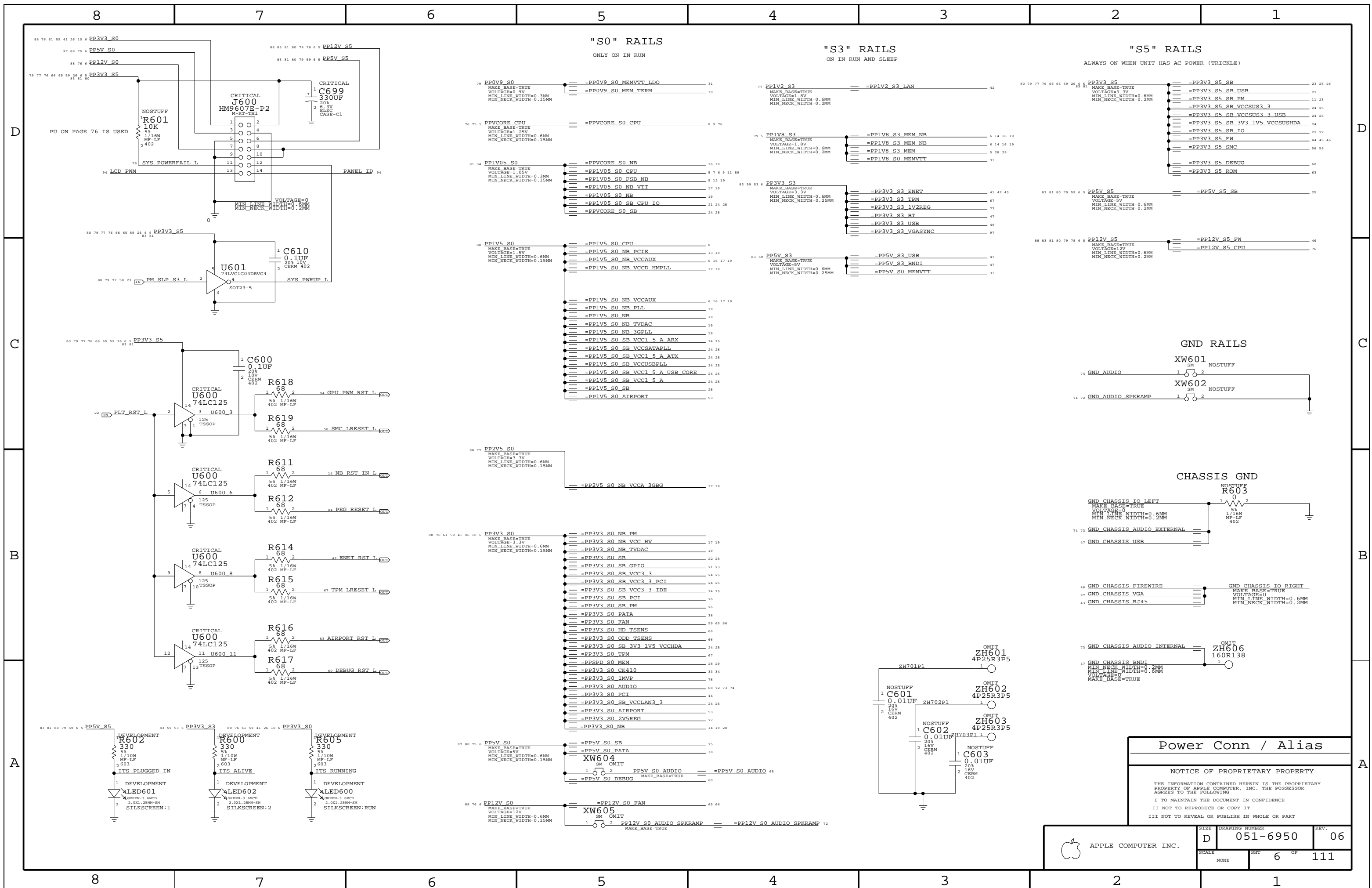
LAYOUT NOTE: PLACE NEAR U9050

FUNC TEST 1 OF 2		
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APPLE COMPUTER INC.



"S0" RAILS

ONLY ON IN RUN

"S3" RAILS

ON IN RUN AND SLEEP

"S5" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)

GND RAILS

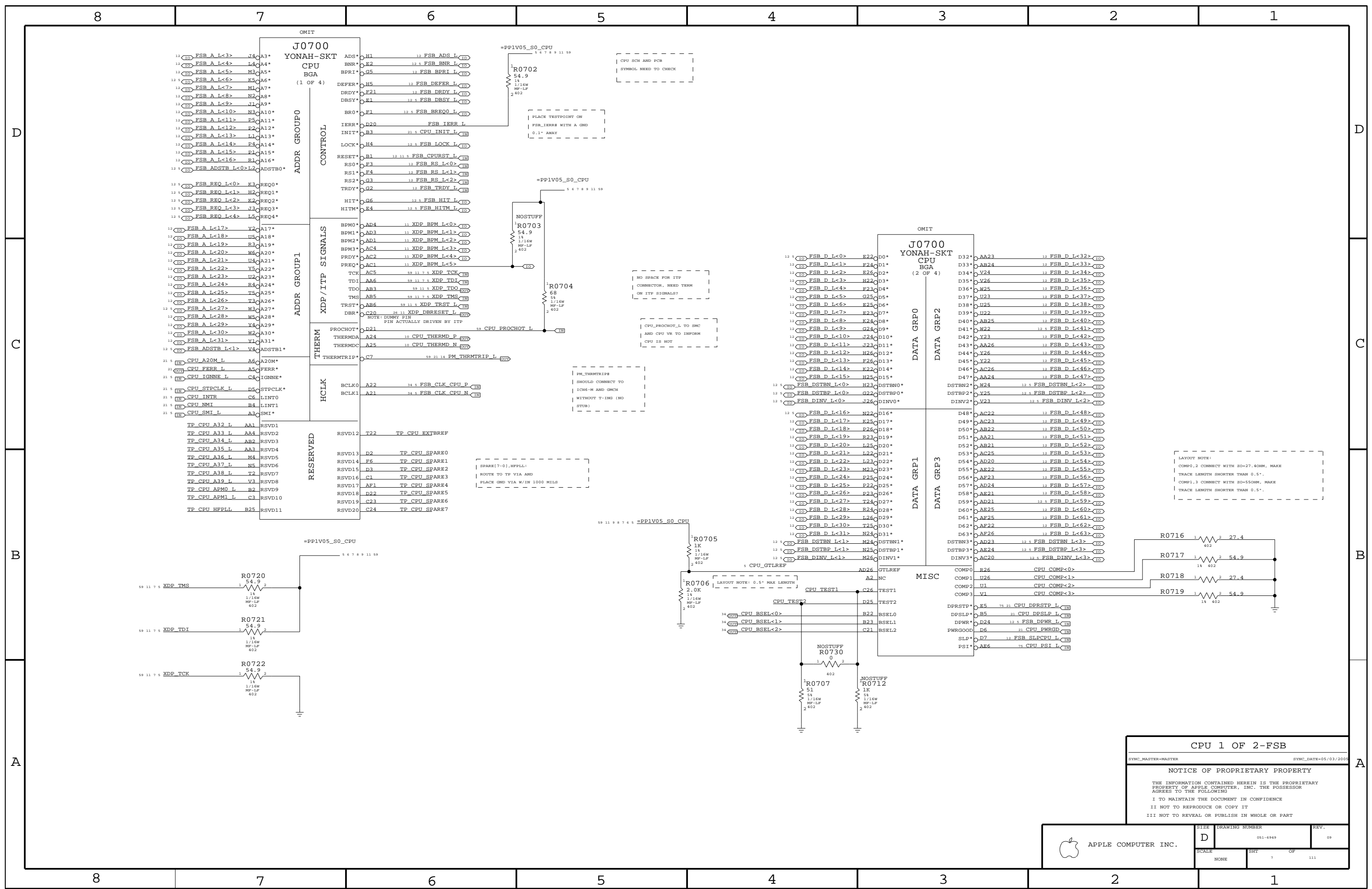
CHASSIS GND

Power Conn / Alias

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	NONE	6 OF 111	06



CPU 1 OF 2-FSB

SYNC_MASTER=MASTER SYNC_DATE=05/03/2005

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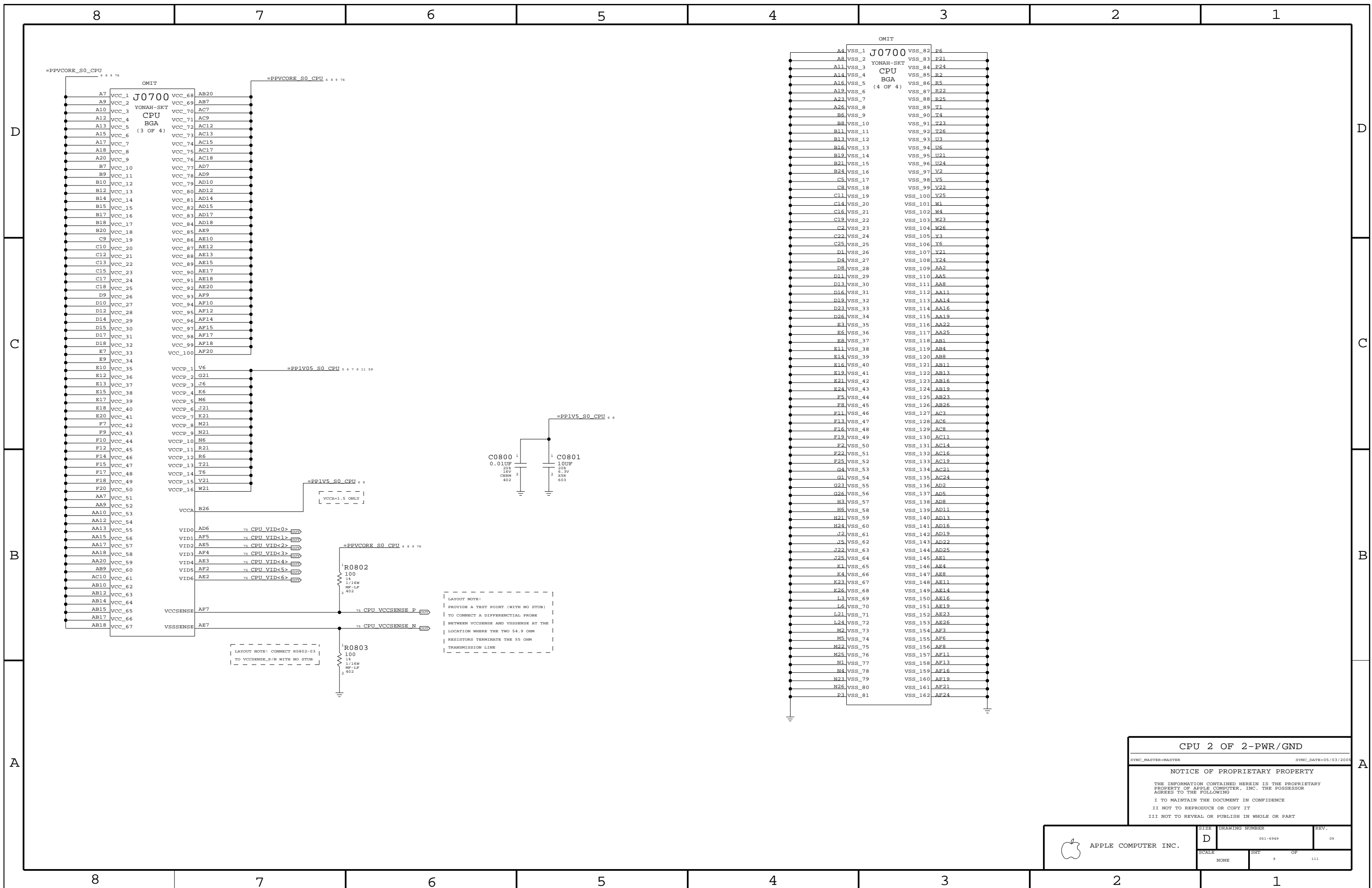
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	SCALE: NONE	SHEET: 7	OF: 111



CPU 2 OF 2-PWR/GND

SYNC_MASTER-MASTER SYNC_DATE=05/03/2005

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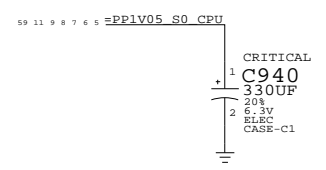
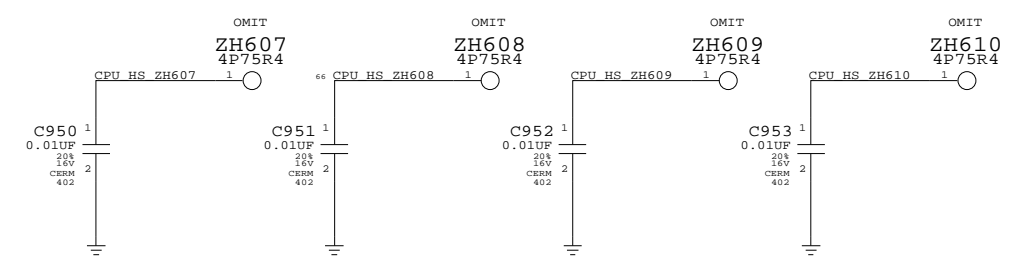
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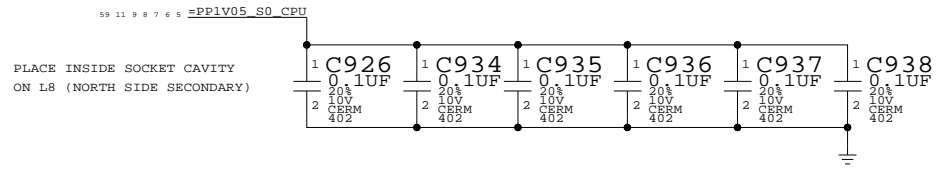
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NONE	8		111

8 7 6 5 4 3 2 1

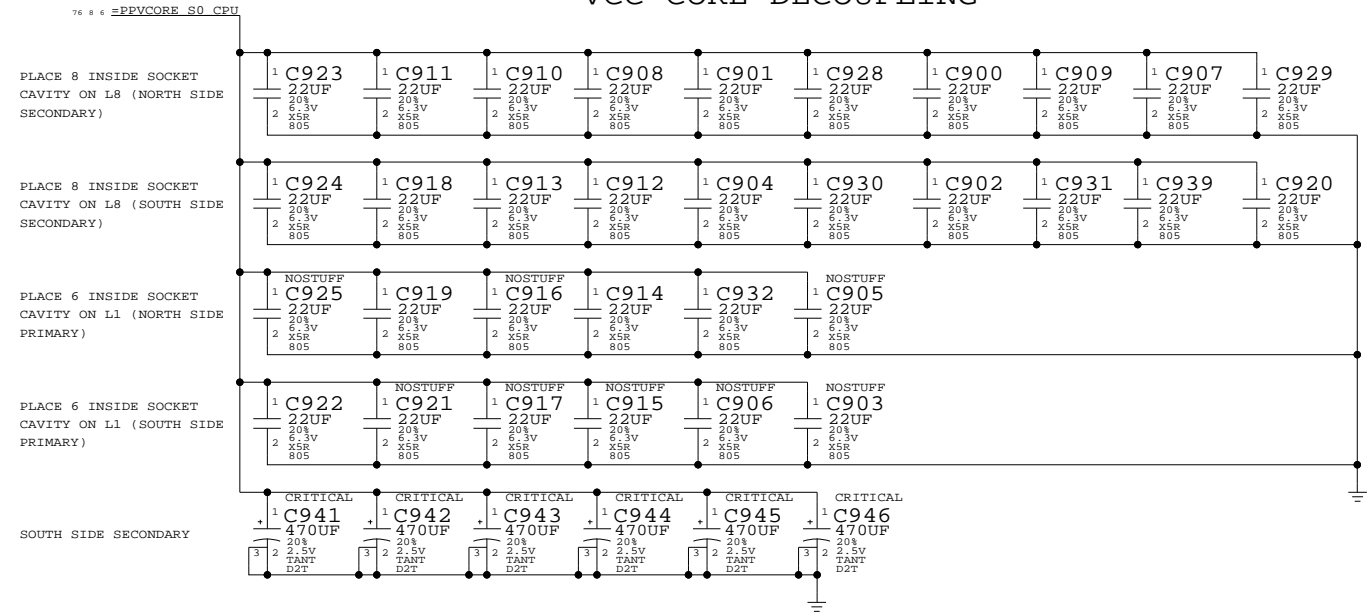
CPU HEATSINK MOUNTING HOLES



VCCP CORE DECOUPLING



VCC CORE DECOUPLING



CPU DECAPS & VID<>

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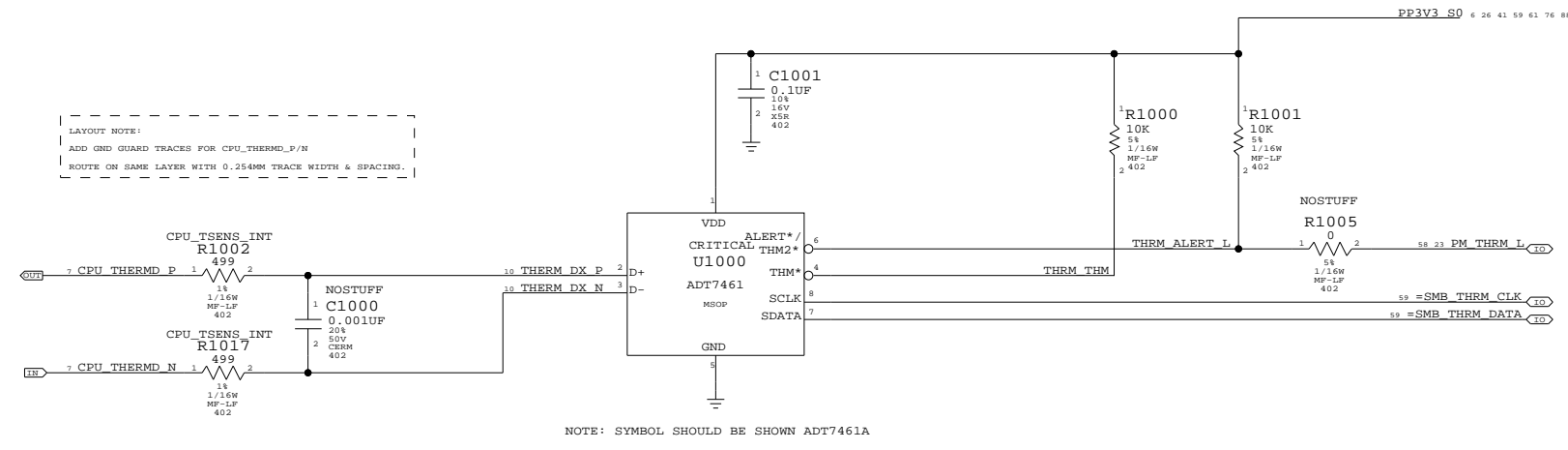
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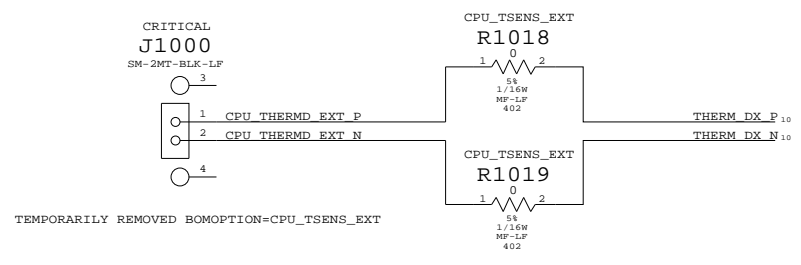
8 7 6 5 4 3 2 1

CPU THERMAL SENSOR

NOTE:
IF CPU T DIODE TO BE READ IN OFF STATE,
THEN THIS SHOULD BE S5



LAYOUT NOTE:
PLACE R1002 AND R1018 SUCH THAT THEY SHARE ONE PAD
PLACE R1017 AND R1019 SUCH THAT THEY SHARE ONE PAD



CPU TEMP SENSOR

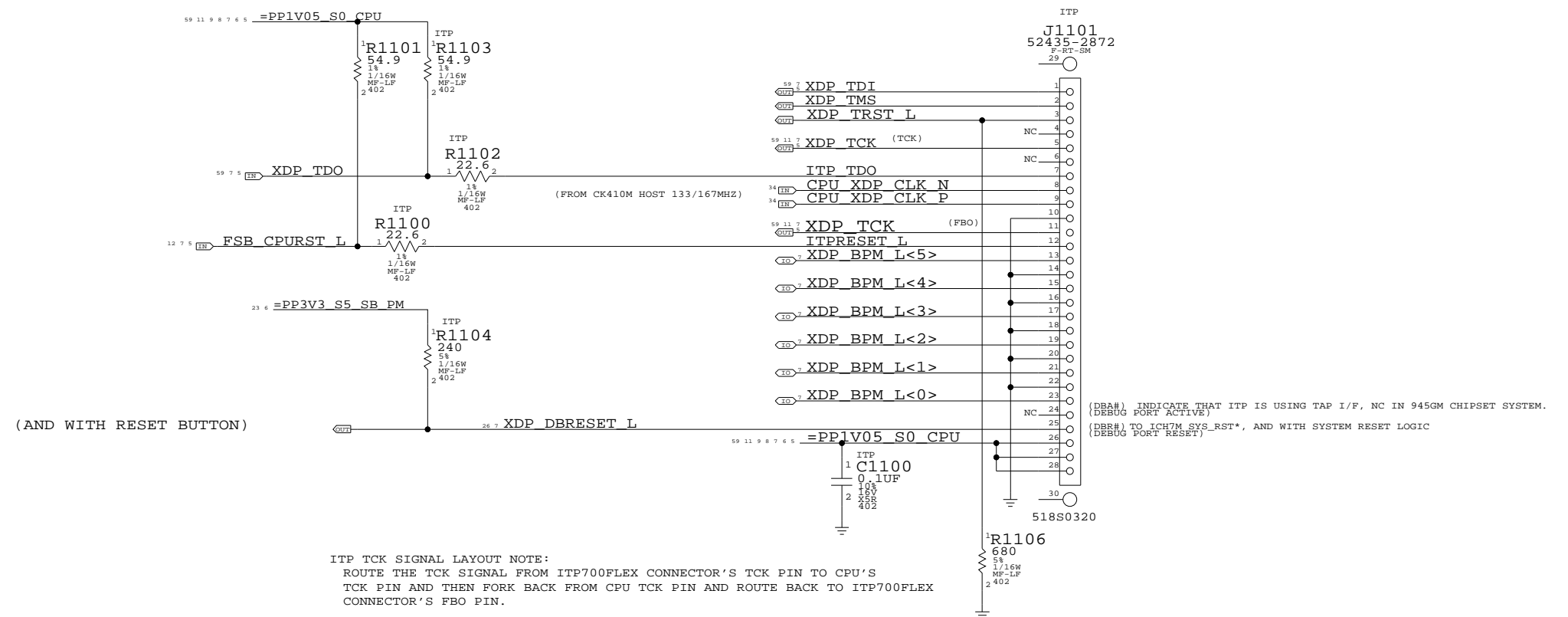
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SCALE	SHT	OF	111
NONE	10		

CPU ITP700FLEX DEBUG SUPPORT



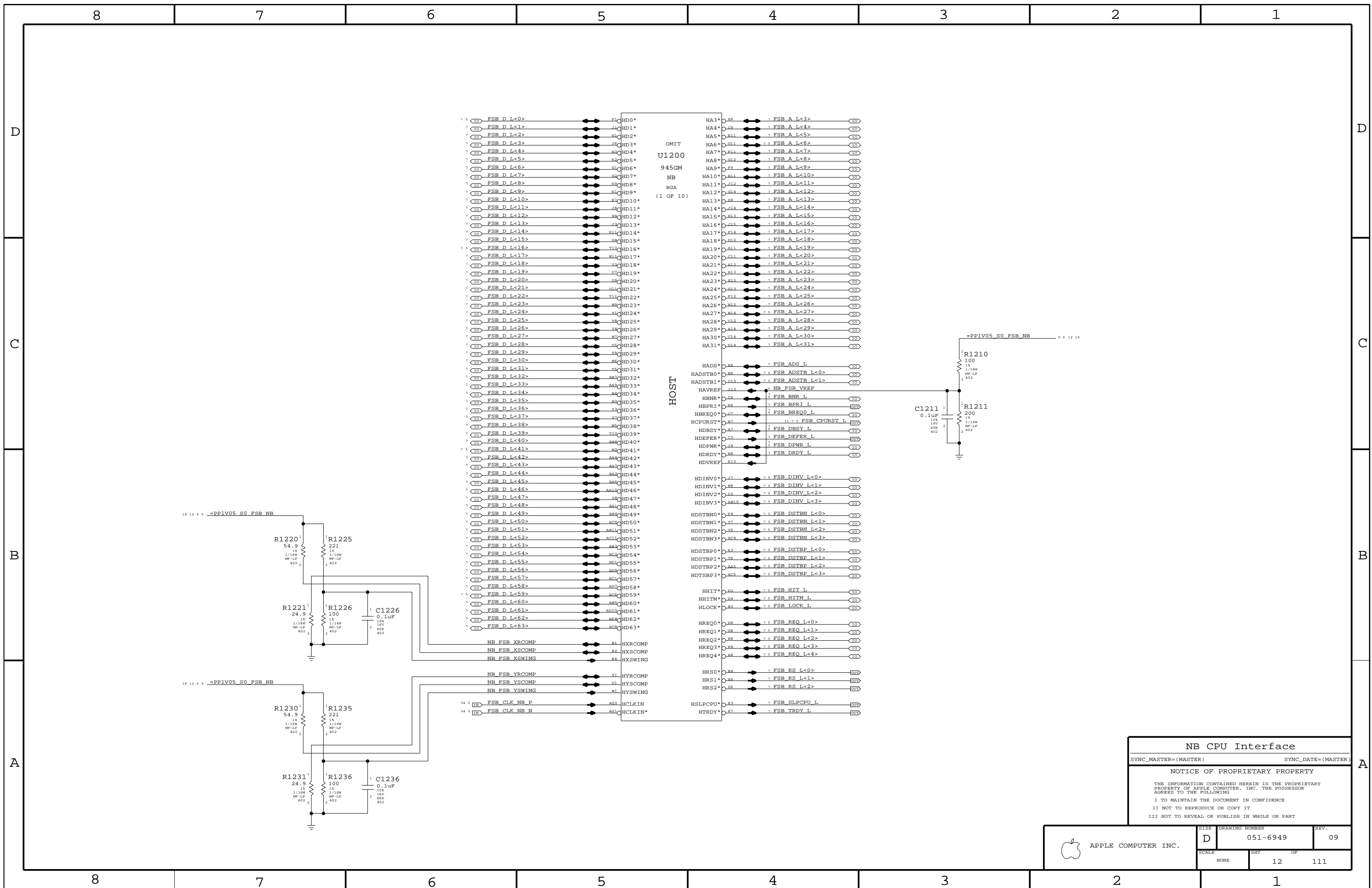
CPU ITP700FLEX DEBUG
 SYNC_MASTER=MASTER SYNC_DATE=5/23/05

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SCALE	SHT	OF	111
NONE	11		



NB CPU Interface

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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	SCALE: NONE	SHEET: 12	OF: 111

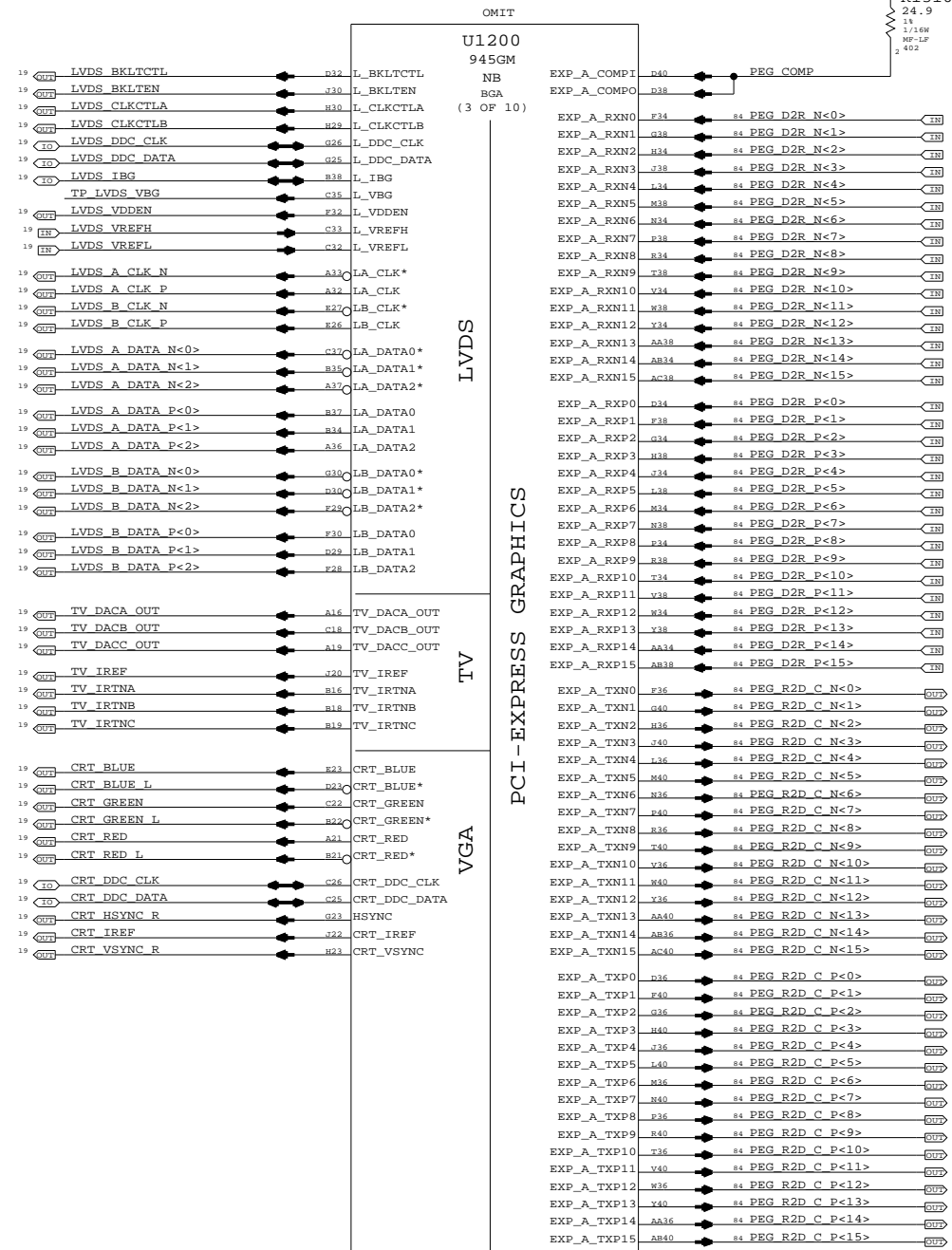
LVDS Disable
 Can leave all signals NC if LVDS is not implemented
 Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
 VCCD_LVDS must remain powered with proper decoupling.
 Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:
 Composite: DACA only
 S-Video: DACB & DACC only
 Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit
 filtering components. Unused DAC outputs should
 connect to GND through 75-ohm resistors.

TV-Out Disable
 Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
 Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
 VCCA_TVVBG to 1.5V power rail. Tie VSSA_TVVBG to GND.

CRT Disable
 Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
 HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
 rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



SDVO Alternate Function

SDVO_TVCLKIN#
 SDVO_INT#
 SDVO_FLDSTALL#

SDVO_TVCLKIN
 SDVO_INT
 SDVO_FLDSTALL

SDVOB_RED#
 SDVOB_GREEN#
 SDVOB_BLUE#
 SDVOB_CLKN
 SDVOC_RED#
 SDVOC_GREEN#
 SDVOC_BLUE#
 SDVOC_CLKN

SDVOB_RED
 SDVOB_GREEN
 SDVOB_BLUE
 SDVOB_CLKP
 SDVOC_RED
 SDVOC_GREEN
 SDVOC_BLUE
 SDVOC_CLKP

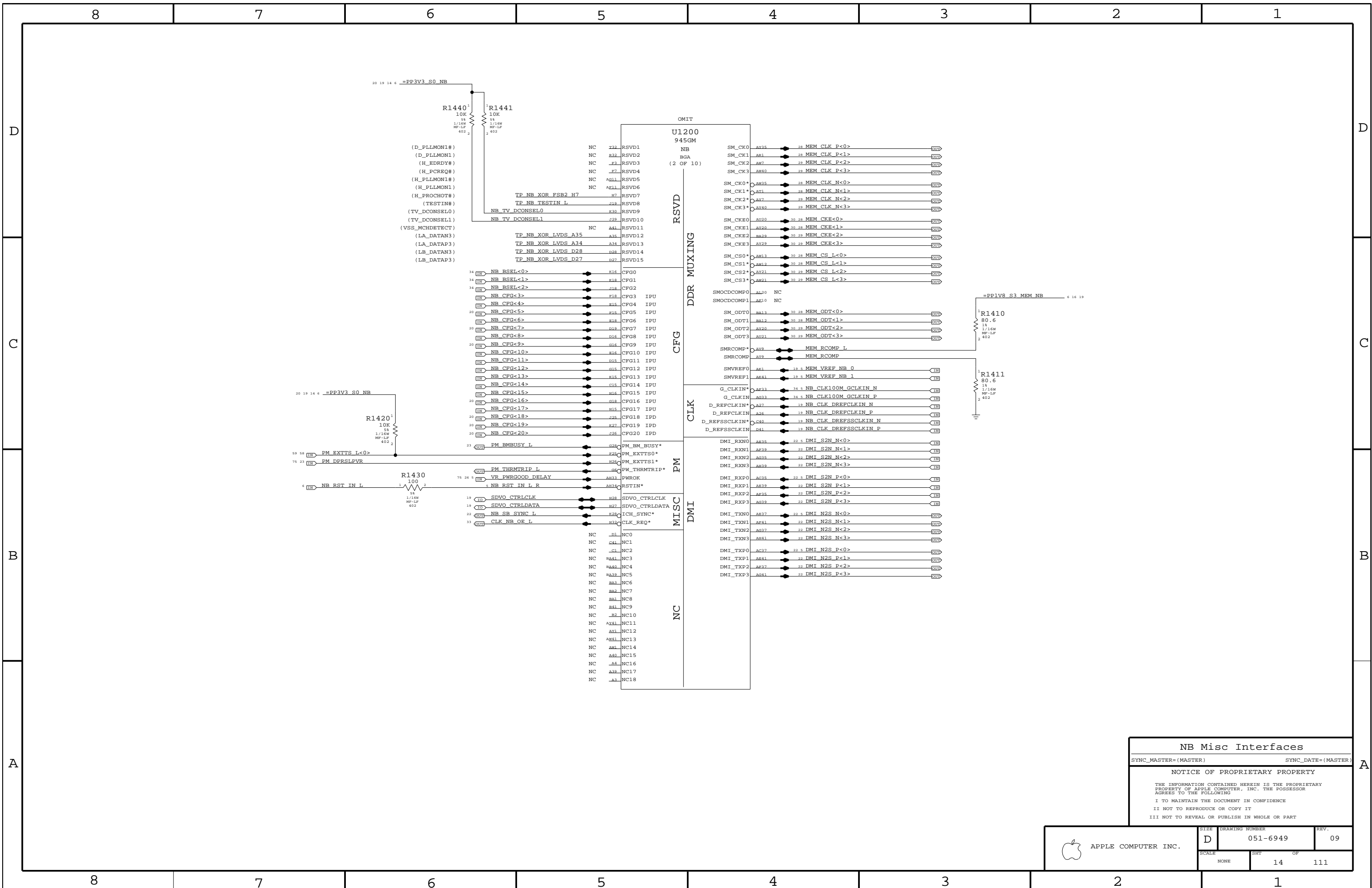
NB PEG / Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE	SHT		OF
NONE	13		111



NB Misc Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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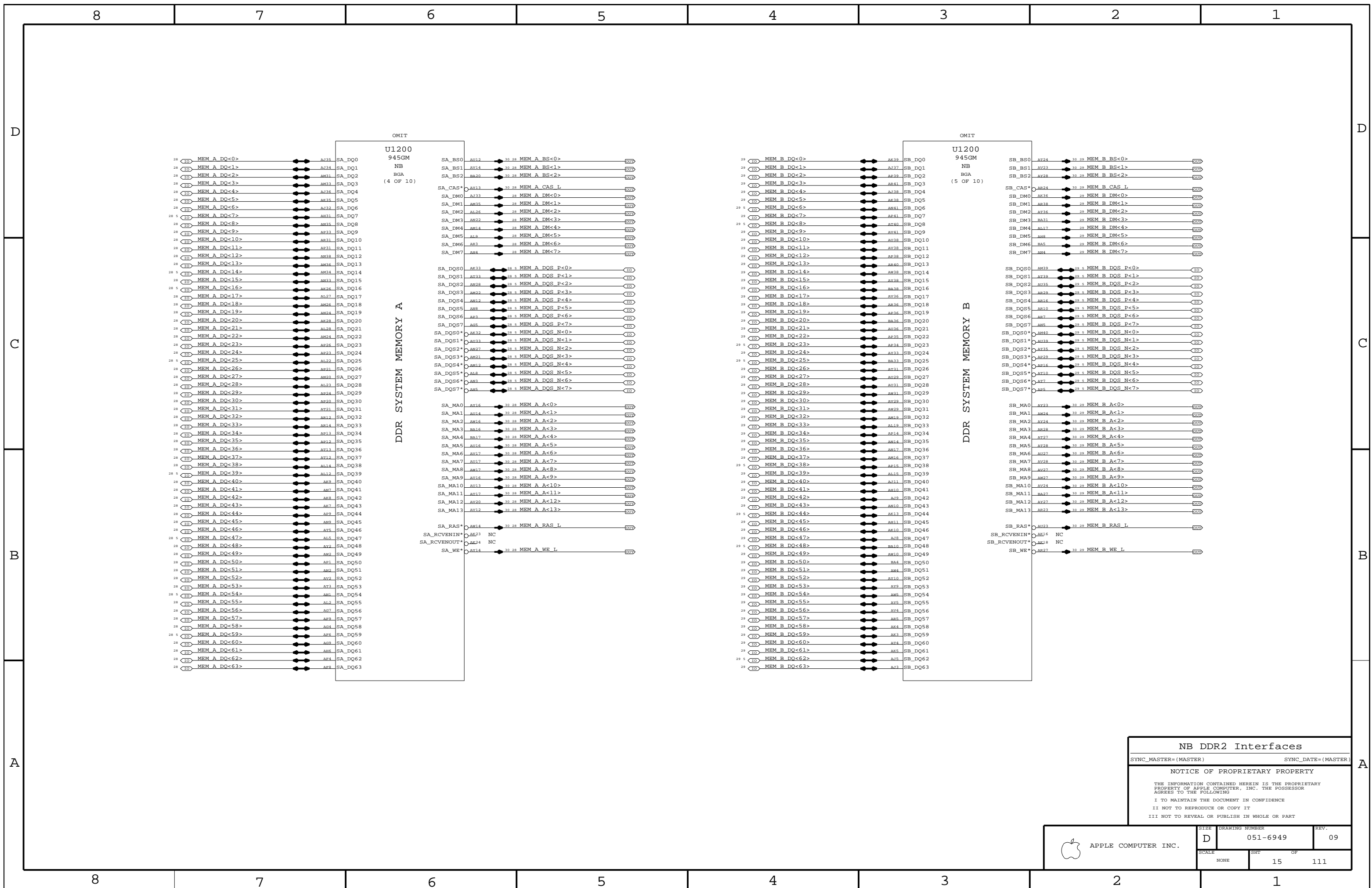
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	SCALE: NONE	SHEET: 14	OF: 111



NB DDR2 Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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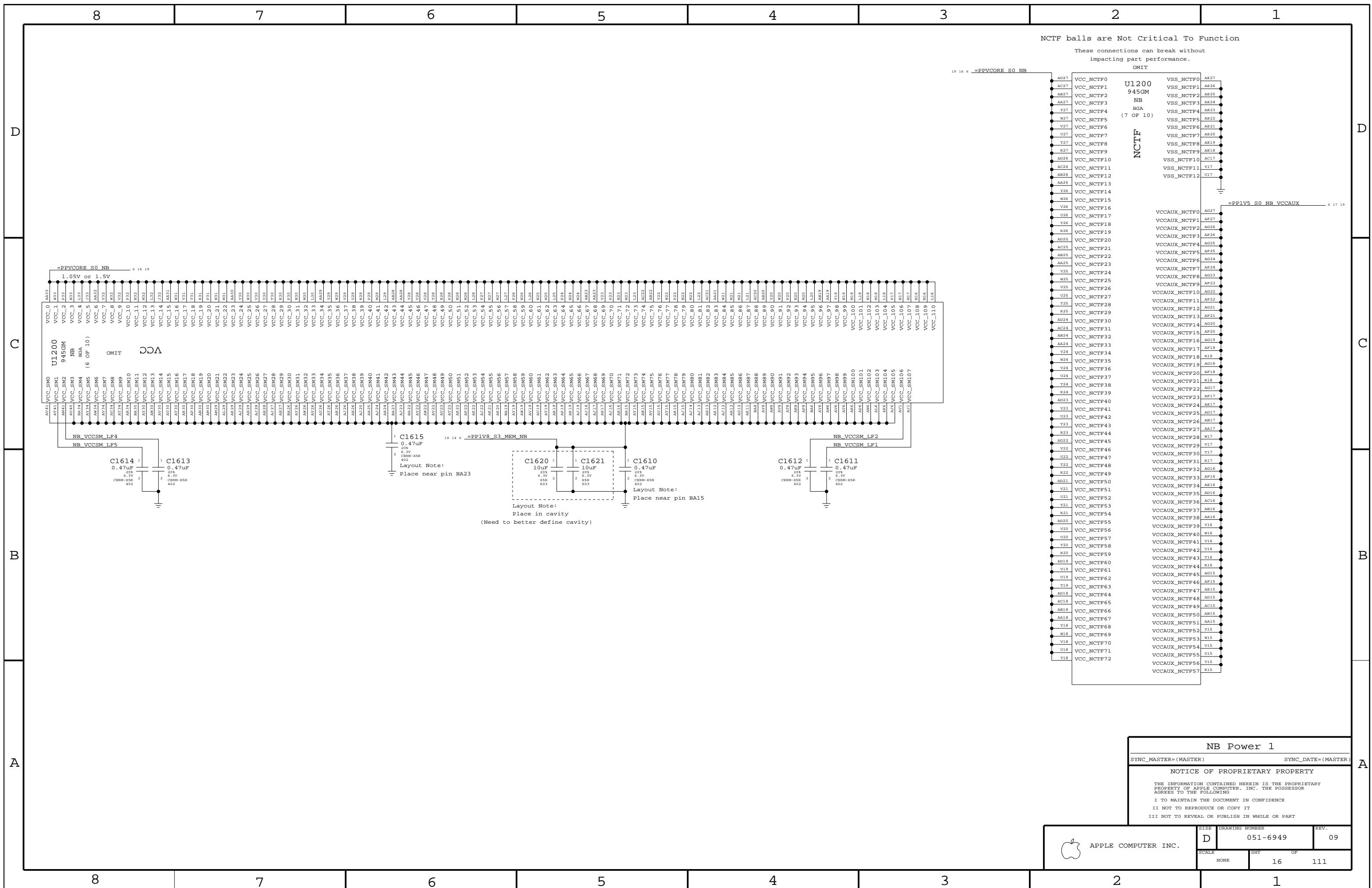
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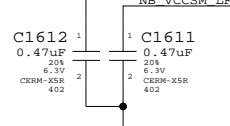
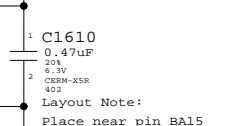
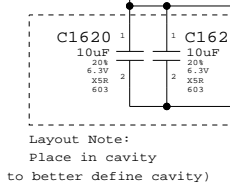
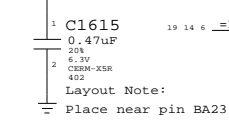
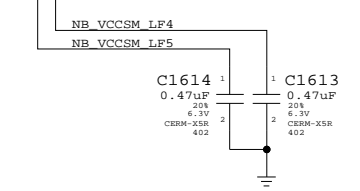
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE: D	DRAWING NUMBER: 051-6949	REV.: 09
	SCALE: NONE	SHEET OF: 15 OF 111	



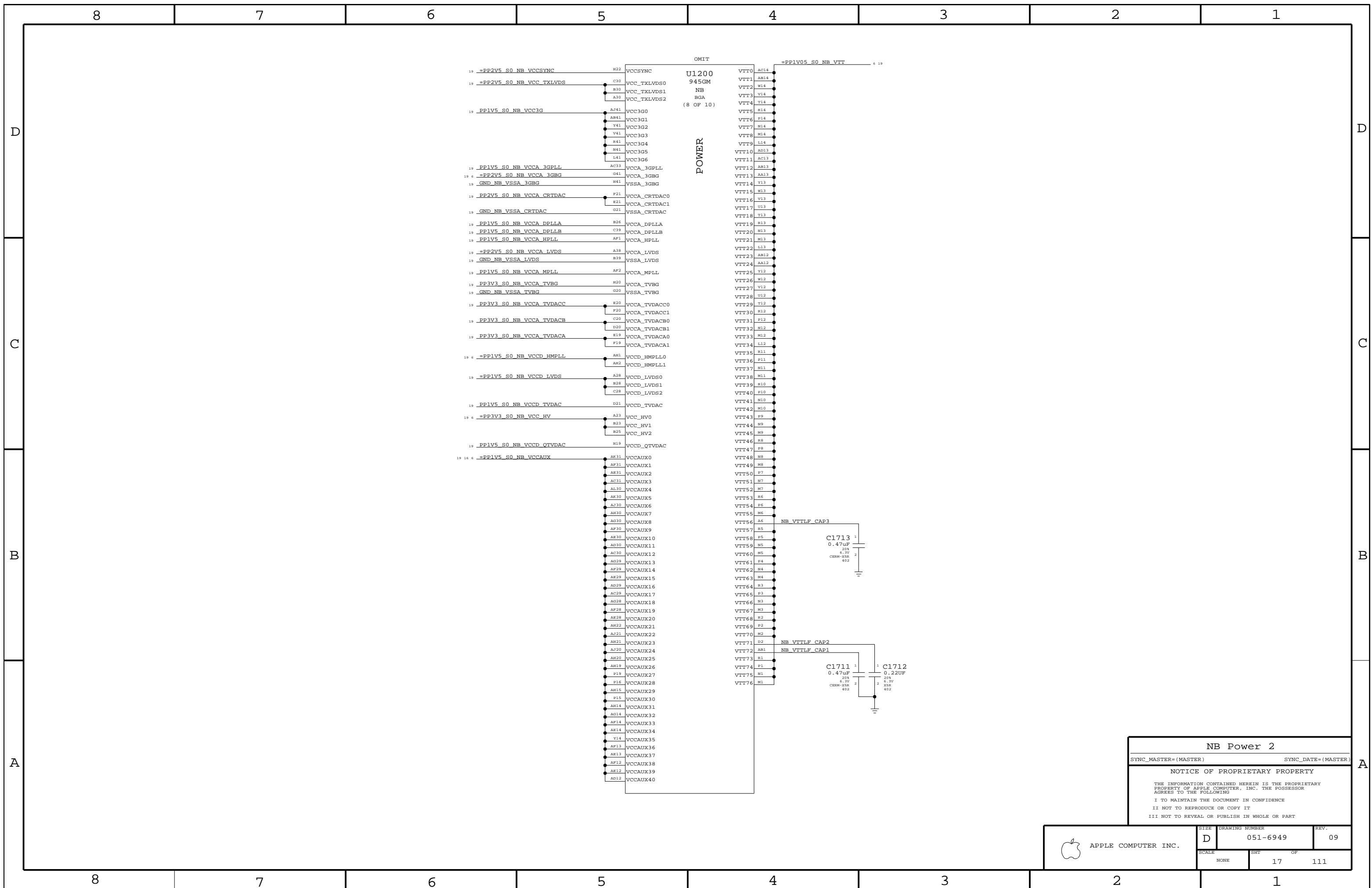
NCTF balls are Not Critical To Function
 These connections can break without impacting part performance.
 OMIT

U1200 945GM NB BGA (7 OF 10)
 OMIT



NB Power 1
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6949	09
SCALE	SHEET OF		
NONE	16		111



NB Power 2

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

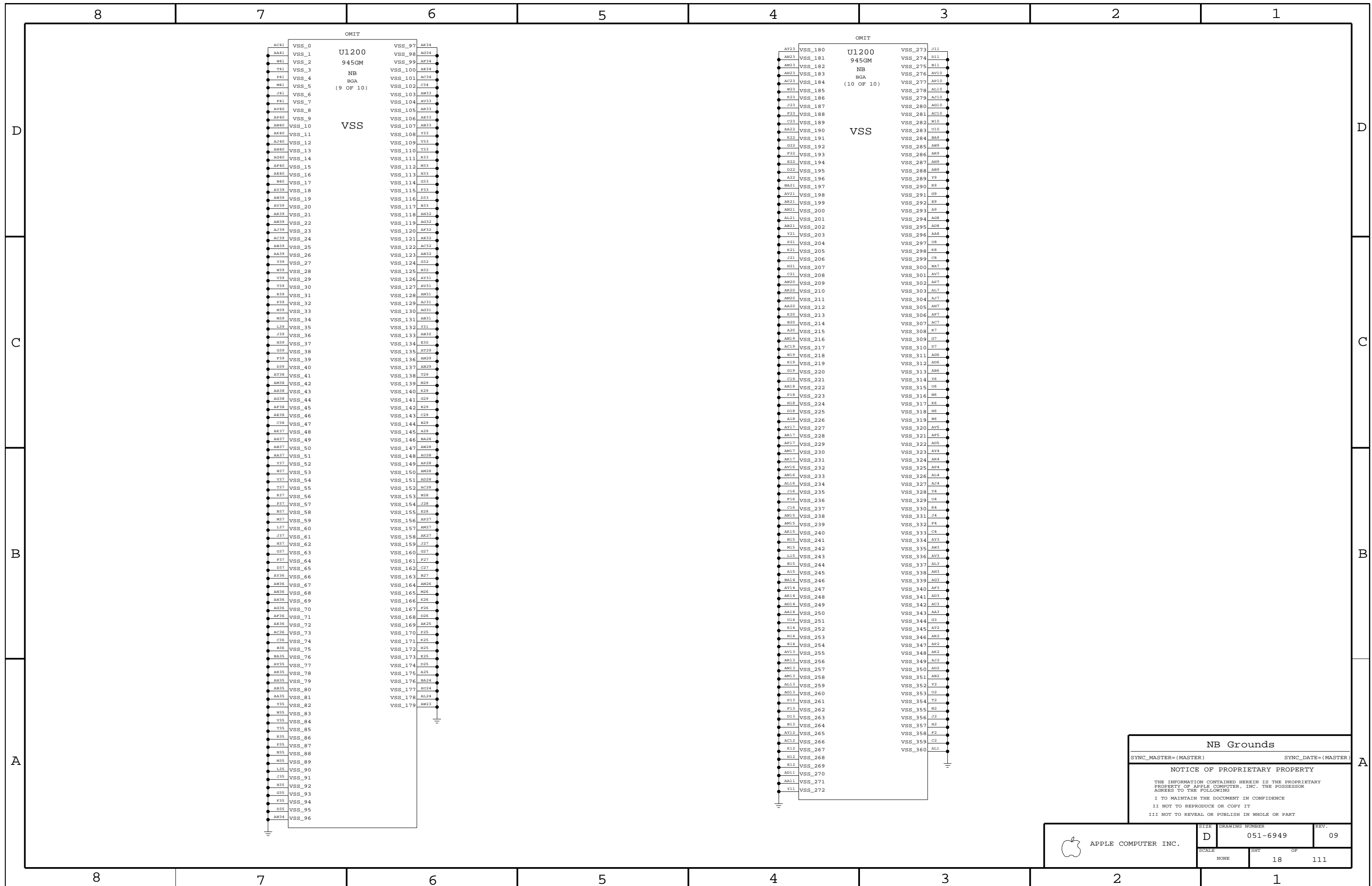
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	D	051-6949	09
SCALE	SHT	OF	
NONE	17	111	



NB Grounds

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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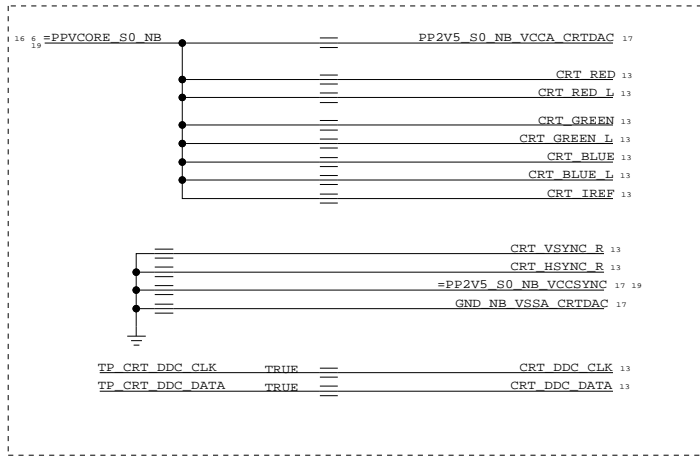
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6949	REV. 09
	SCALE NONE	SHEET 18	OF 111

Power Interface

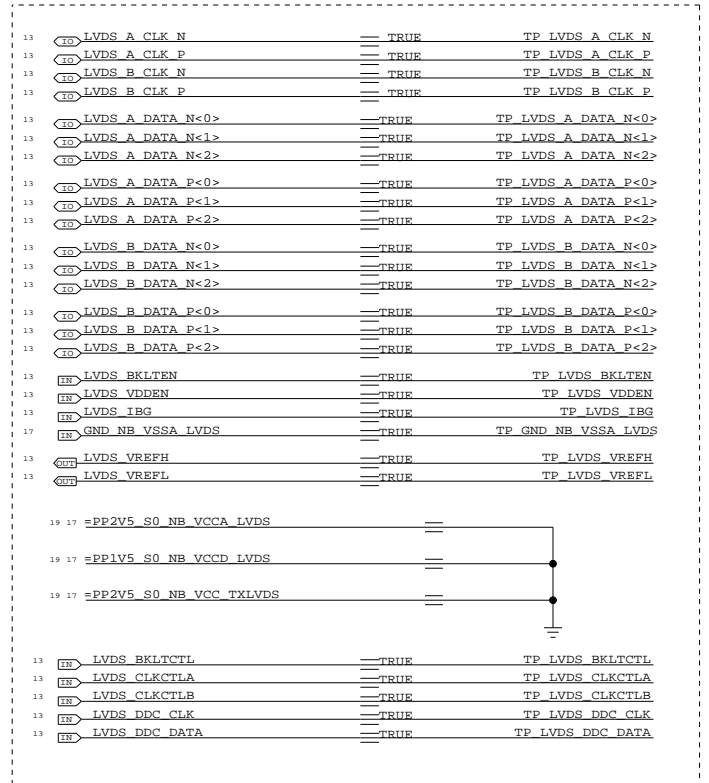
These are the power signals that leave the NB "block"

PP1V05_S0_FSB_NB	5 6 12
PPVCORE_S0_NB	6 16 19
PP1V05_S0_NB	6
PP1V05_S0_NB_VTT	6 17 19
PP1V5_S0_NB	6 19
PP1V5_S0_NB_PCIE	6 13
PP1V5_S0_NB_PLL	6 19
PP1V5_S0_NB_TVDAC	6 19
PP1V5_S0_NB_VCCD_HMPLL	6 17
PP1V5_S0_NB_VCCD_LVDS	17 19
PP1V5_S0_NB_VCCAUX	6 16 17 19
PP1V8_S3_MEM_NB	6 14 16 19
PP2V5_S0_NB_VCCSYNCR	17 19
PP2V5_S0_NB_VCC_TXLVDS	17 19
PP2V5_S0_NB_VCCA_3GBG	6 17 19
PP2V5_S0_NB_VCCA_LVDS	17 19
PP3V3_S0_NB	6 14 20
PP3V3_S0_NB_TVDAC	6
PP3V3_S0_NB_VCC_HV	6 17 19

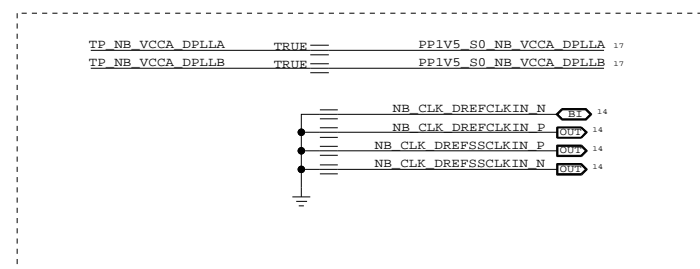
TVOUT DISABLE



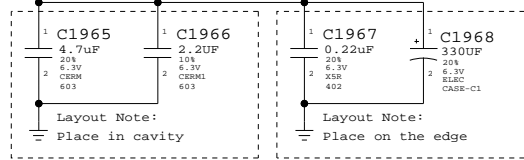
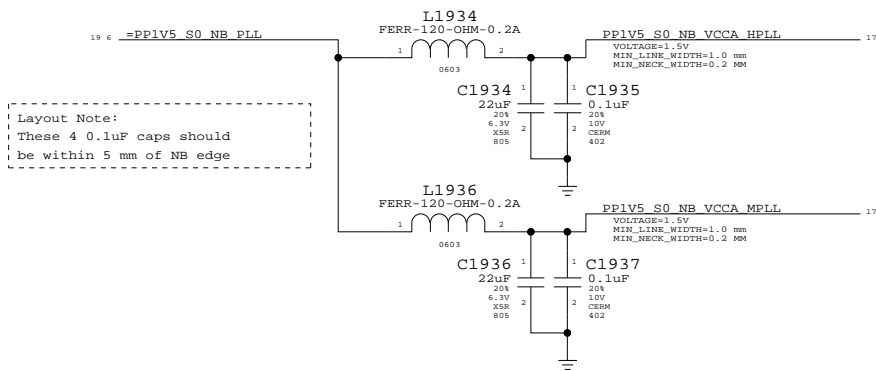
LVDS DISABLE



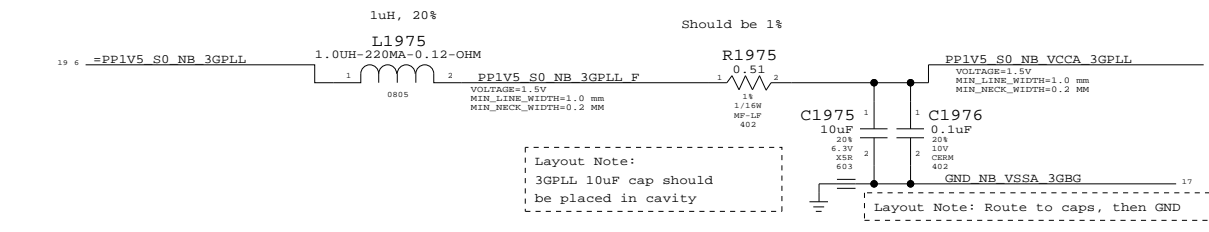
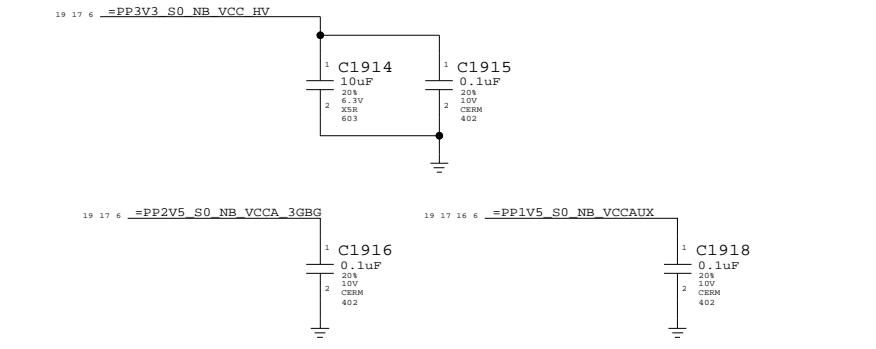
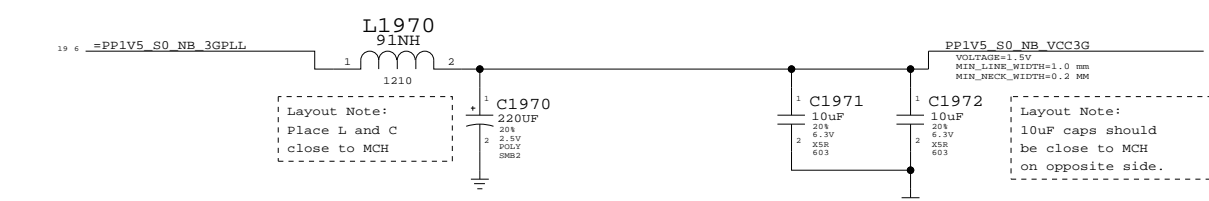
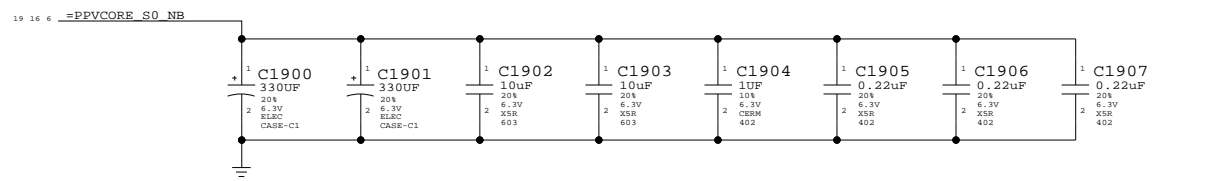
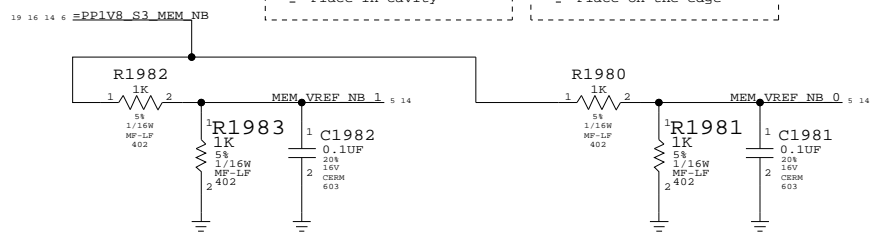
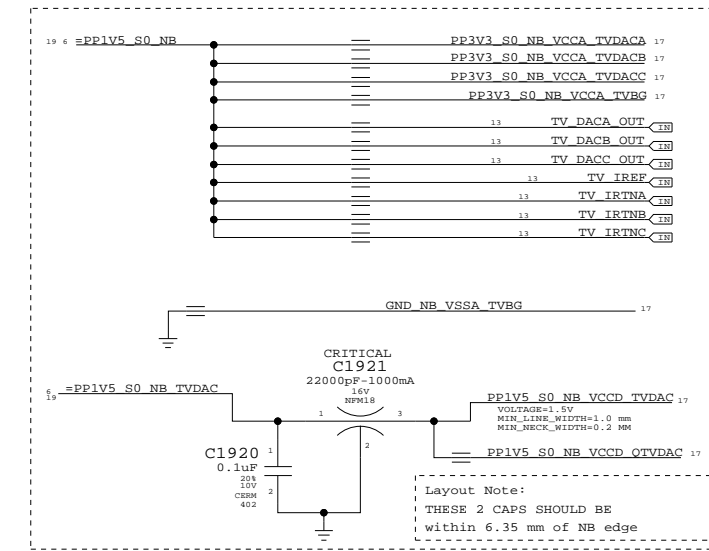
DISPLAY DISABLE



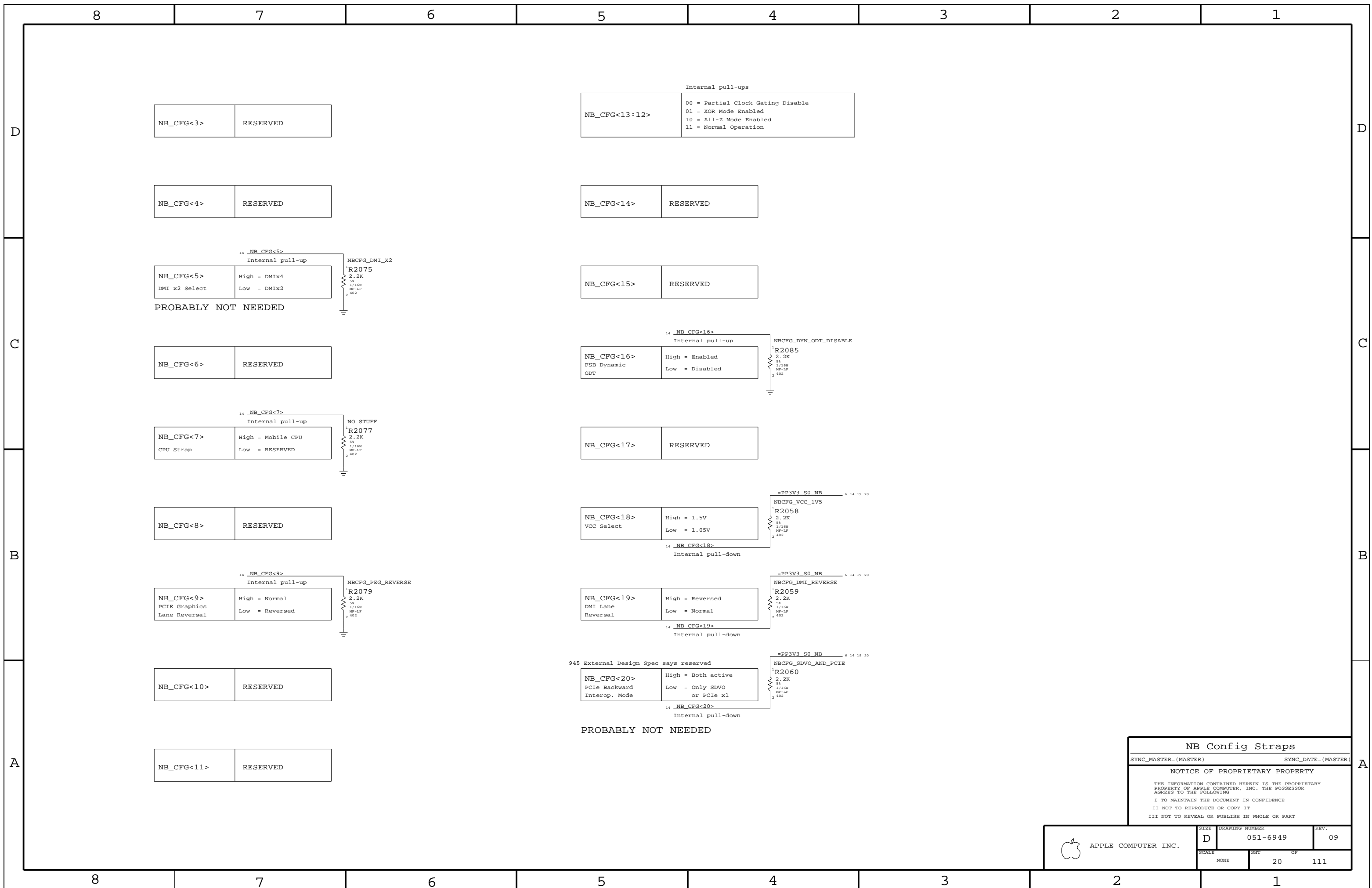
Layout Note:
These 4 0.1uF caps should be within 5 mm of NB edge



TVOUT DISABLE



NB (GM) Decoupling
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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NB_CFG<3>	RESERVED
-----------	----------

NB_CFG<4>	RESERVED
-----------	----------

14 NB_CFG<5> Internal pull-up	
NB_CFG<5>	High = DMiX4 DMI x2 Select Low = DMiX2
PROBABLY NOT NEEDED	

NB_CFG<6>	RESERVED
-----------	----------

14 NB_CFG<7> Internal pull-up	
NB_CFG<7>	High = Mobile CPU CPU Strap Low = RESERVED

NB_CFG<8>	RESERVED
-----------	----------

14 NB_CFG<9> Internal pull-up	
NB_CFG<9>	High = Normal PCIe Graphics Lane Reversal Low = Reversed

NB_CFG<10>	RESERVED
------------	----------

NB_CFG<11>	RESERVED
------------	----------

Internal pull-ups	
NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<14>	RESERVED
------------	----------

NB_CFG<15>	RESERVED
------------	----------

14 NB_CFG<16> Internal pull-up	
NB_CFG<16>	High = Enabled FSB Dynamic ODT Low = Disabled

NB_CFG<17>	RESERVED
------------	----------

14 NB_CFG<18> Internal pull-down	
NB_CFG<18>	High = 1.5V VCC Select Low = 1.05V

14 NB_CFG<19> Internal pull-down	
NB_CFG<19>	High = Reversed DMI Lane Reversal Low = Normal

945 External Design Spec says reserved	
14 NB_CFG<20> Internal pull-down	
NB_CFG<20>	High = Both active PCIe Backward Interop. Mode Low = Only SDVO or PCIe x1
PROBABLY NOT NEEDED	

NB Config Straps

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

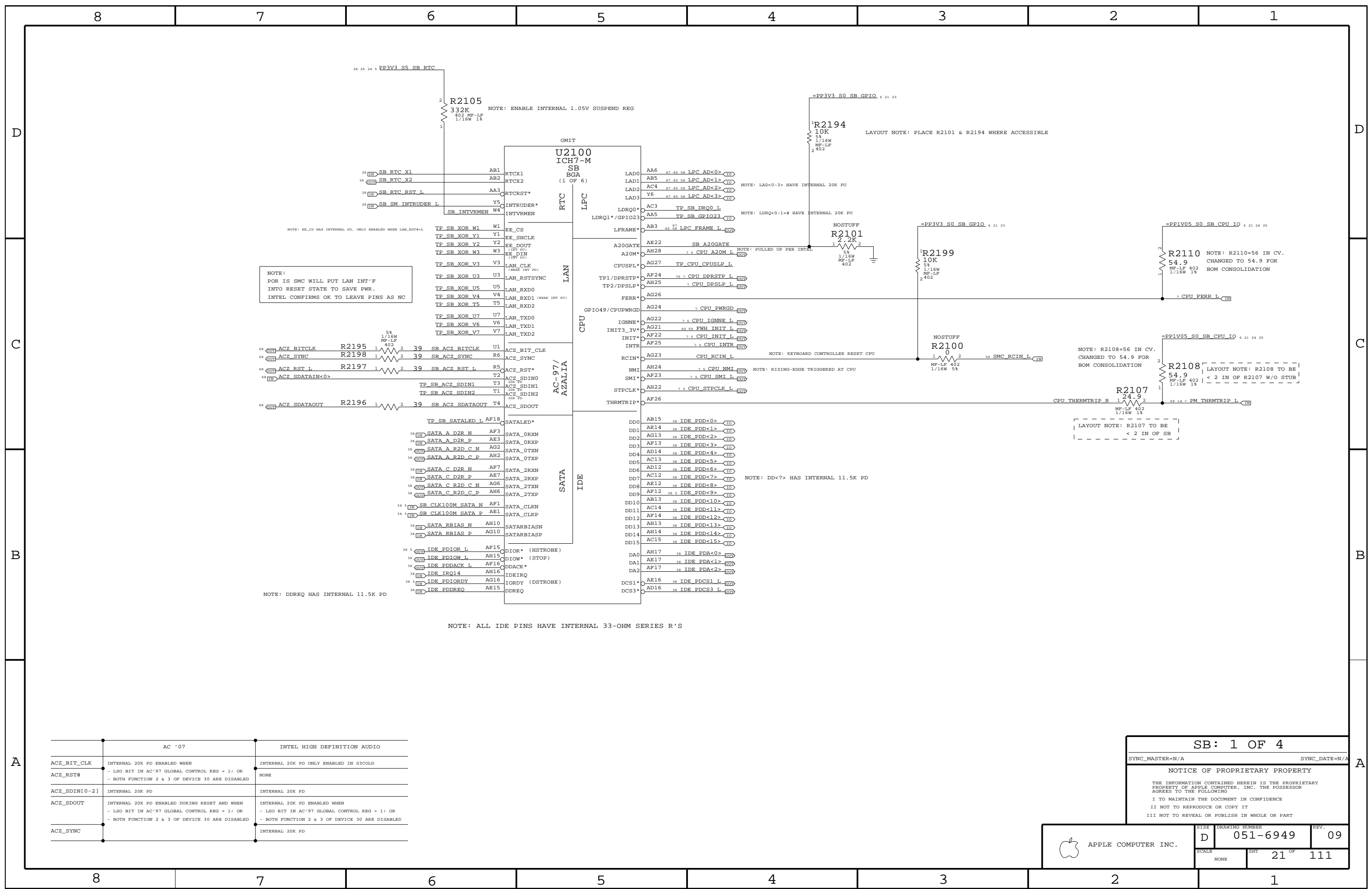
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	D	051-6949	09
SCALE	SHT	OF	
NONE	20	111	



NOTE:
 POR IS SMC WILL PUT LAN INT'F
 INTO RESET STATE TO SAVE PWR.
 INTEL CONFIRMS OK TO LEAVE PINS AS NC

NOTE: DDREQ HAS INTERNAL 11.5K PD

NOTE: ALL IDE PINS HAVE INTERNAL 33-OHM SERIES R'S

AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR
ACZ_RST#	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC	INTERNAL 20K PD

SB: 1 OF 4

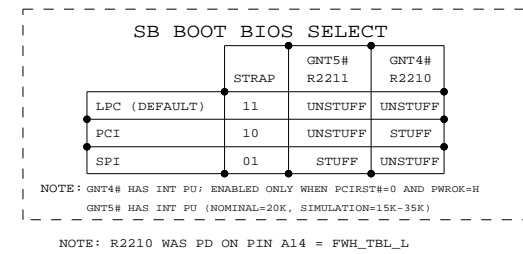
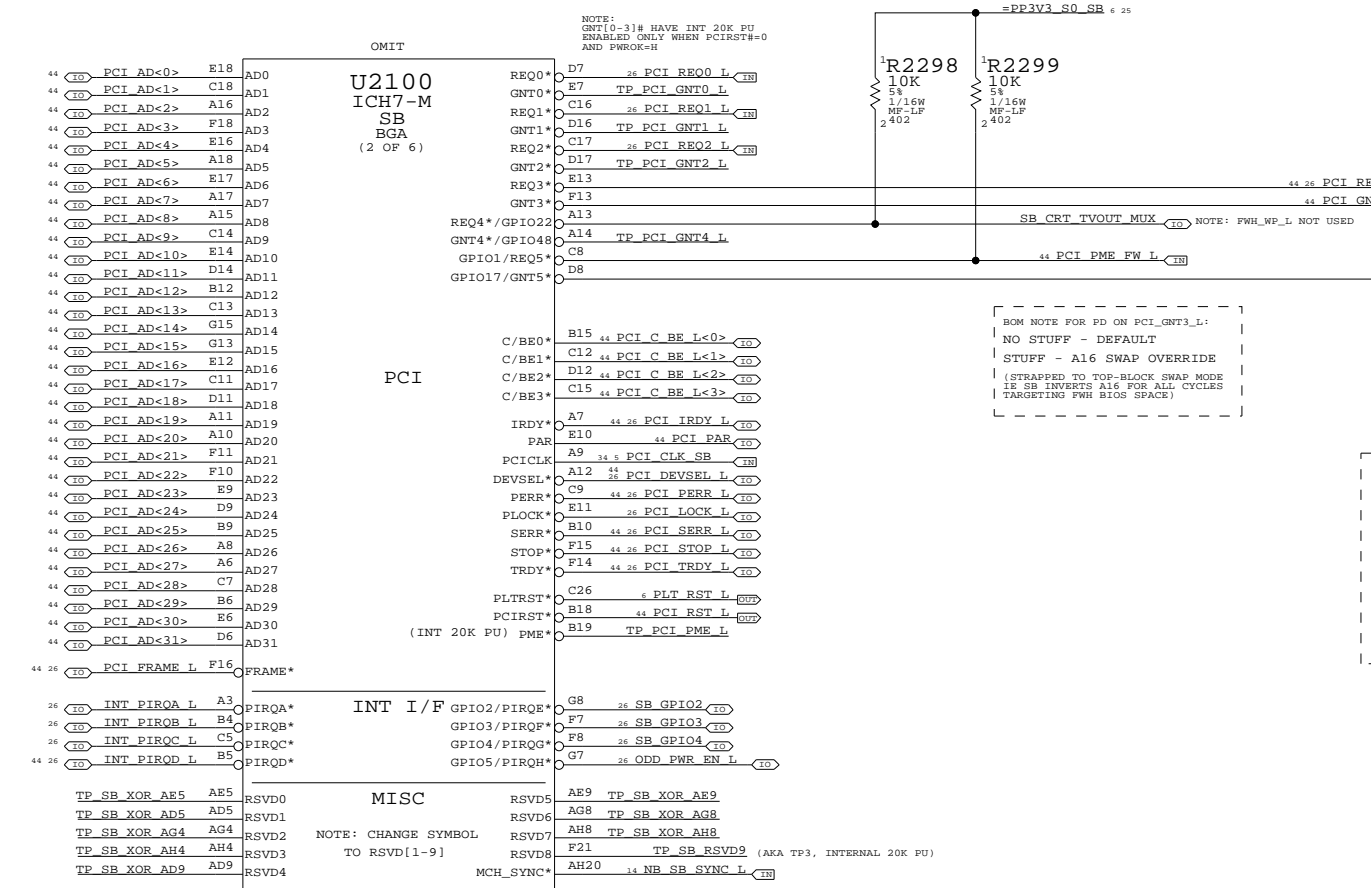
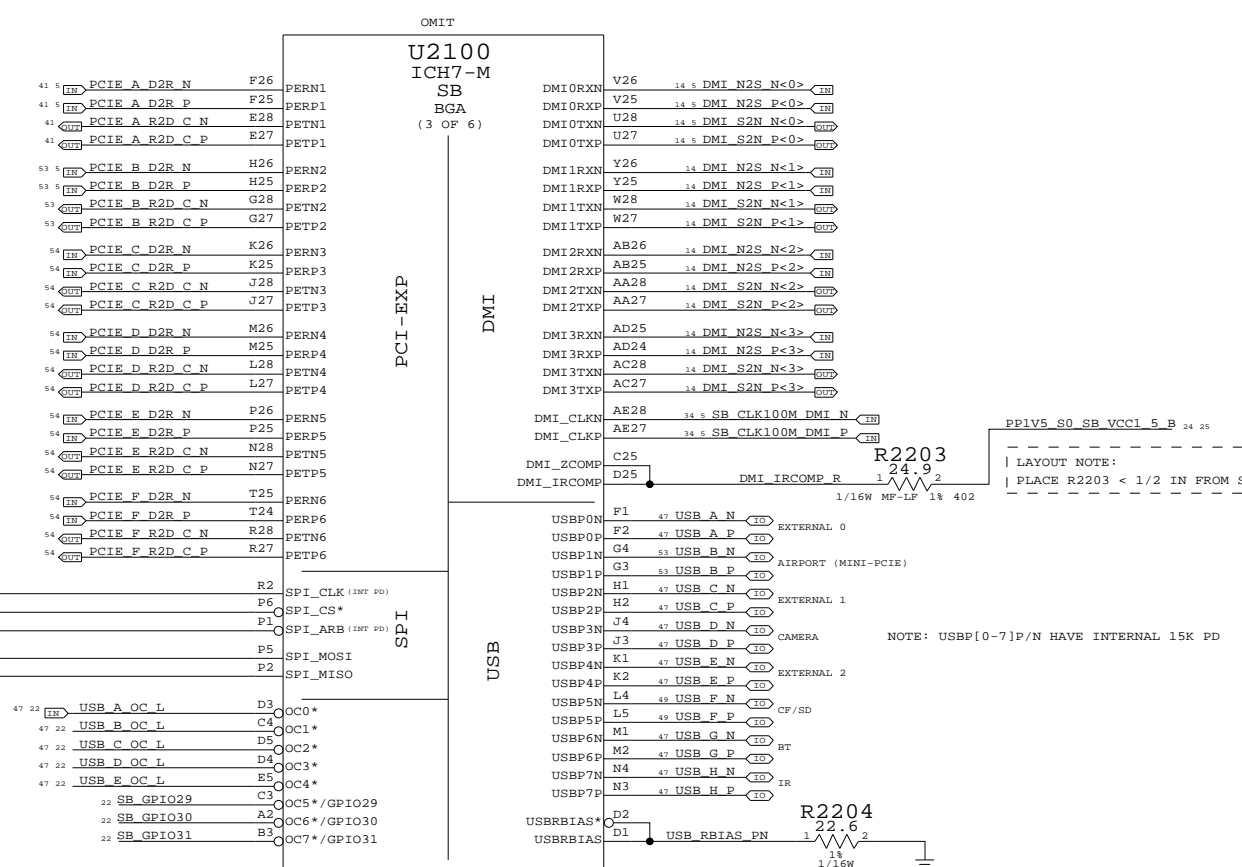
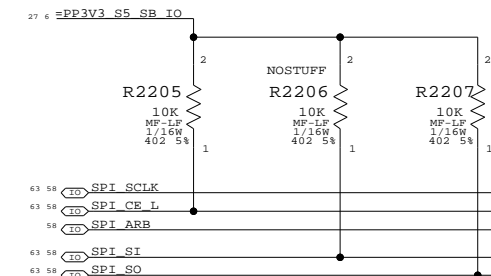
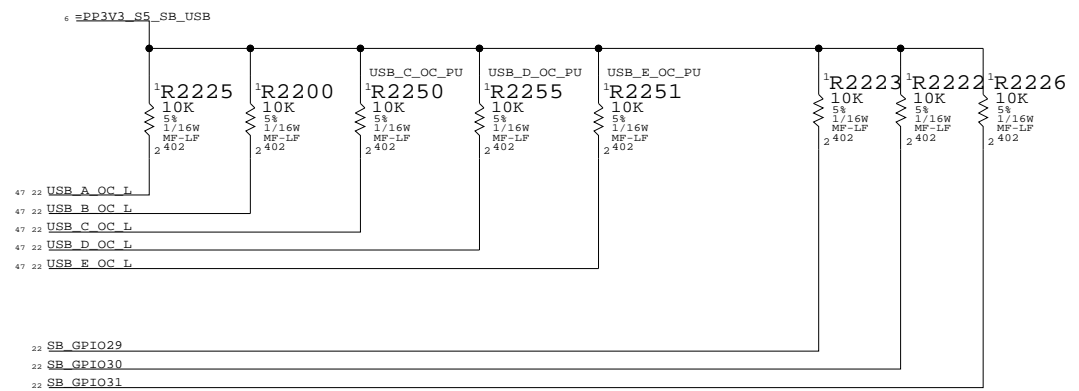
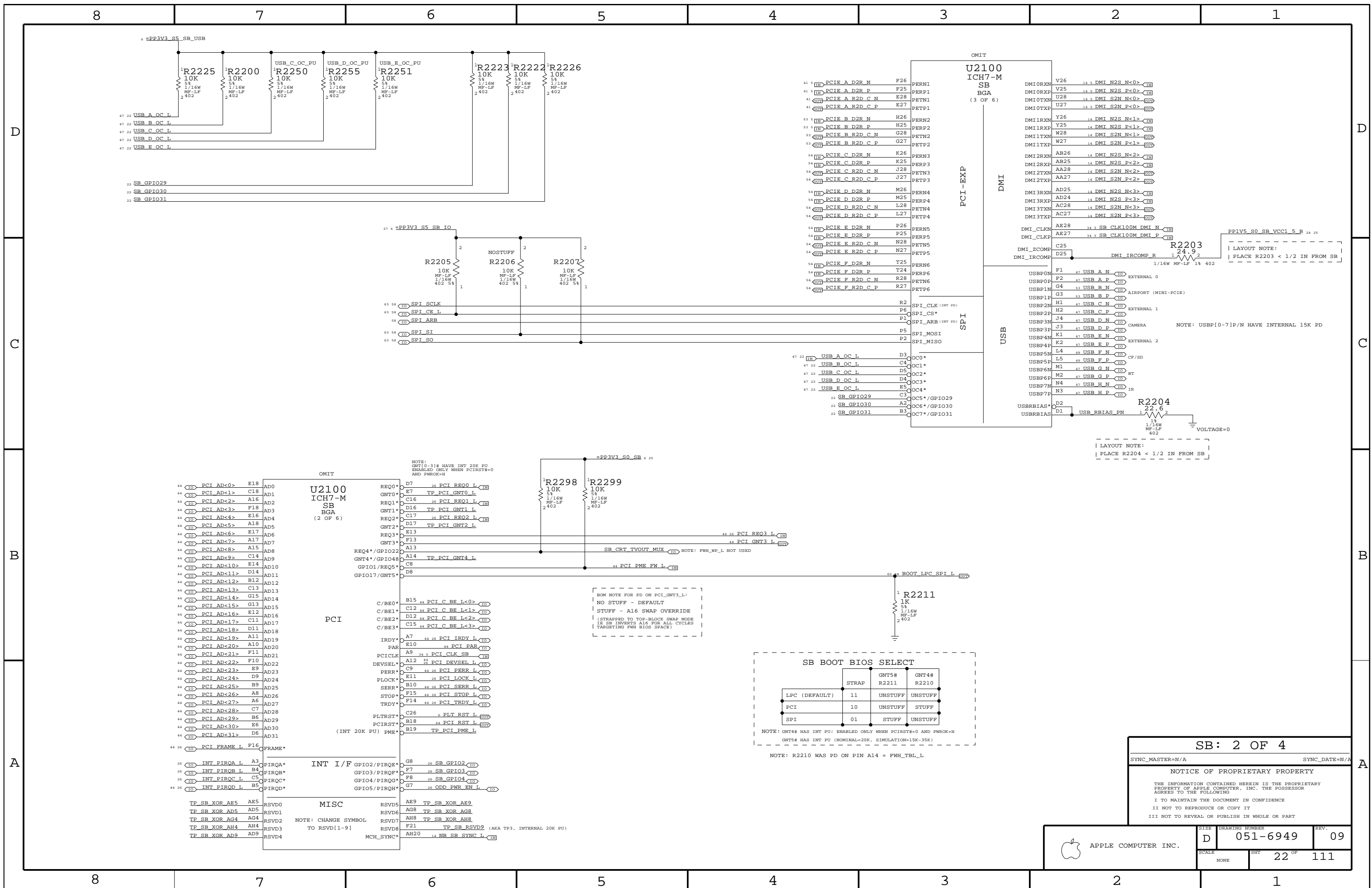
SYNC_MASTER=N/A SYNC_DATE=N/A

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	D	051-6949	09
SCALE	NONE	SHT	21 OF 111



SB: 2 OF 4

SYNC_MASTER=N/A SYNC_DATE=N/A

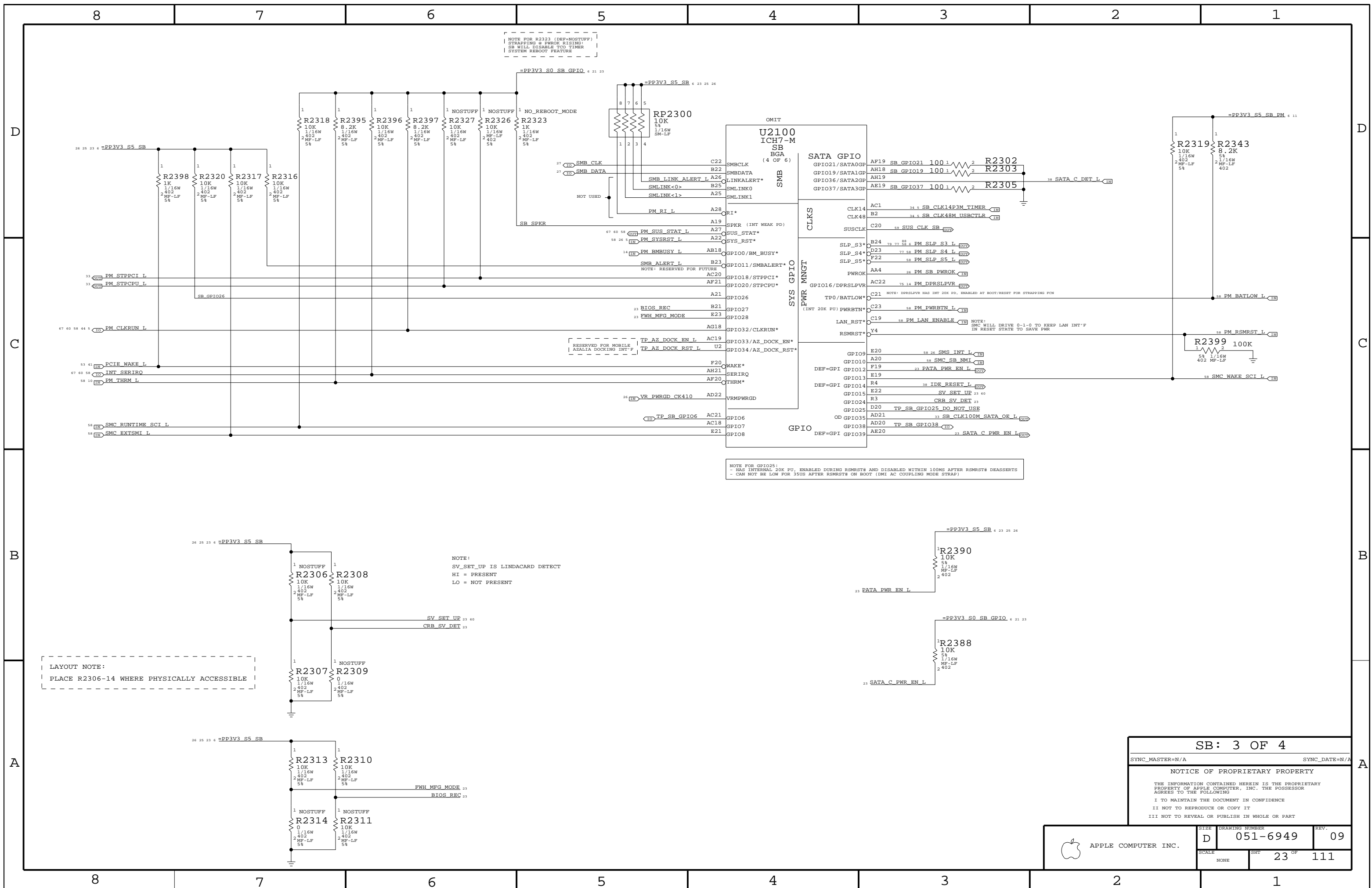
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NOTE FOR R2323 (DEF-NOSTUFF)
STRAPPING # PWROK RISING:
SB WILL DISABLE TCO TIMER
SYSTEM REBOOT FEATURE

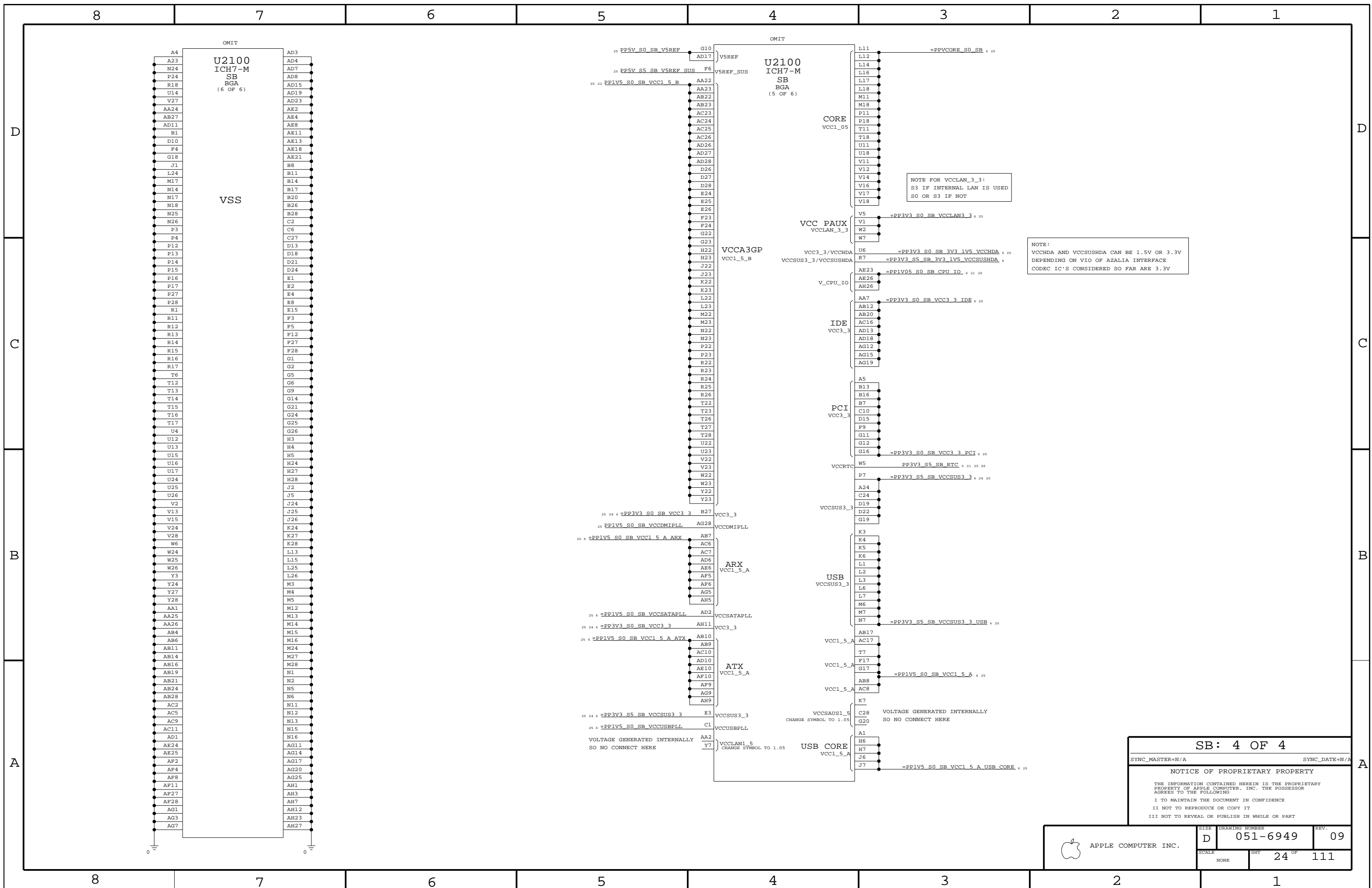
NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

SB: 3 OF 4
SYNC_MASTER=N/A SYNC_DATE=N/A
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	D	051-6949	09
SCALE	NONE	SHT	23 OF 111



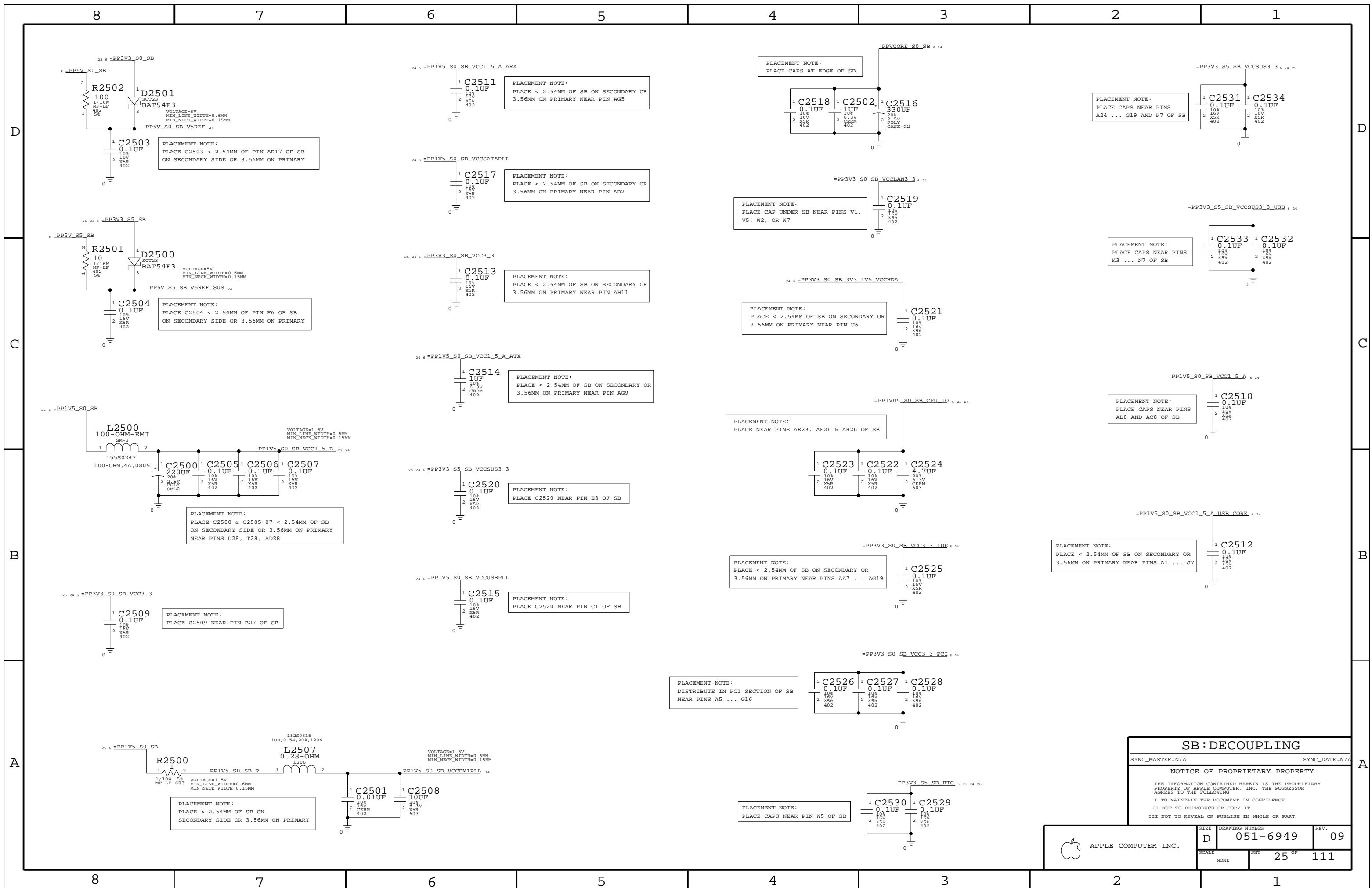
SB: 4 OF 4

SYNC_MASTER=N/A SYNC_DATE=N/A

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	D	051-6949	09
SCALE	SHT	REV.	
NONE	24 OF 111		



SB: DECOUPLING

SYNC_MASTER=N/A SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

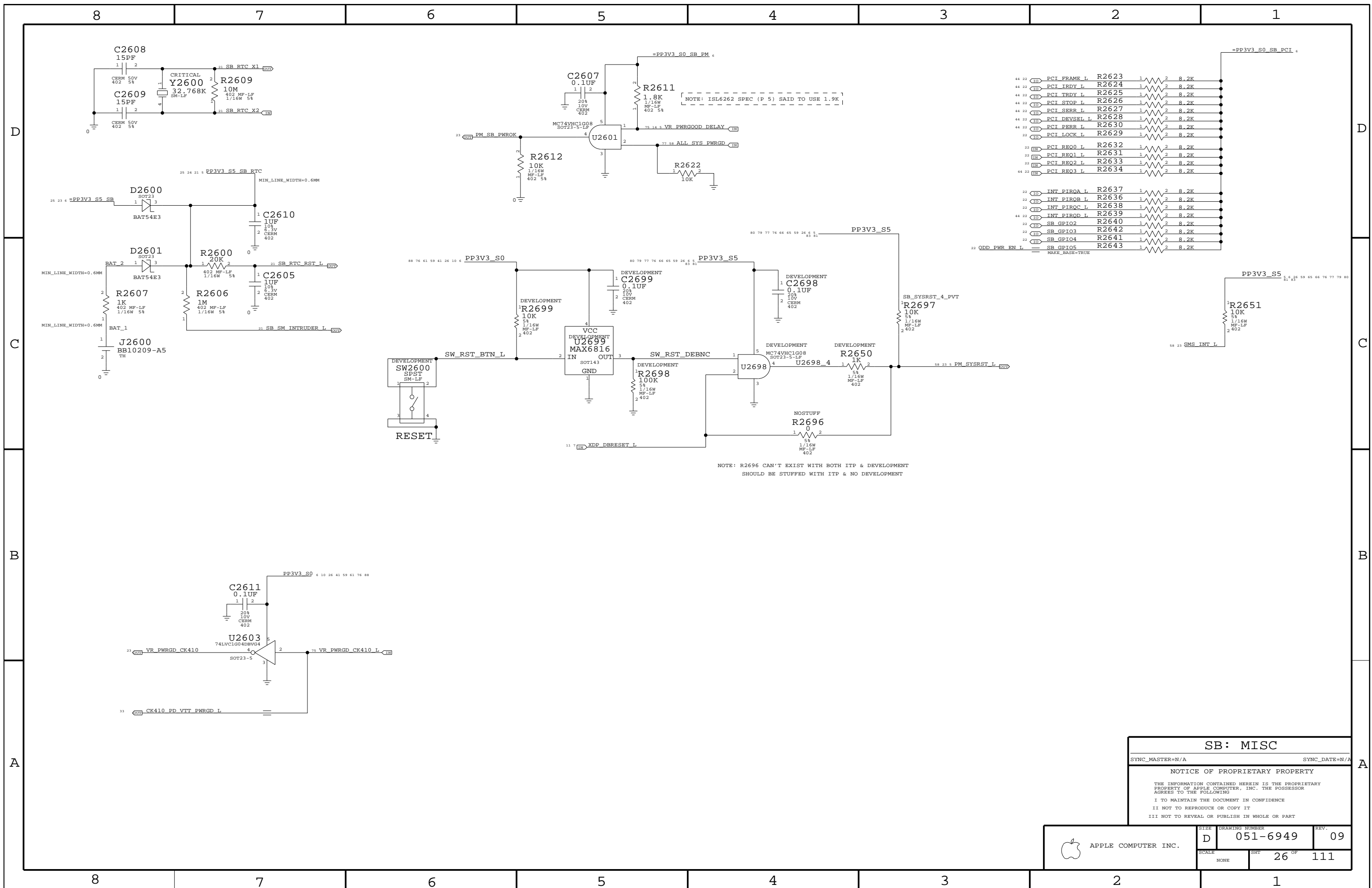
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	D	051-6949	09
SCALE	SHT	25 OF	111
NONE			



SB: MISC

SYNC_MASTER=N/A SYNC_DATE=N/A

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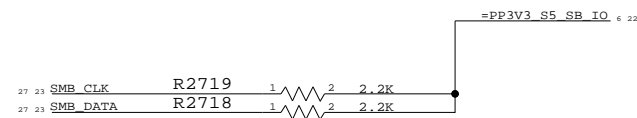
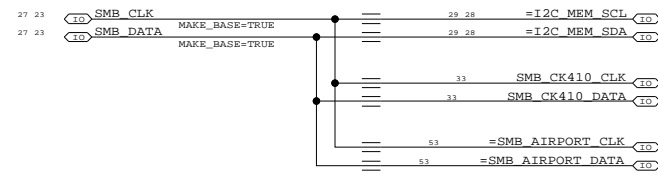
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6949	09
SCALE	SHT	OF	
NONE	26	111	

SB I2C BUSSES



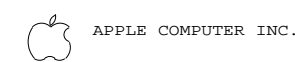
SB: SMB HUB

SYNC_MASTER=N/A SYNC_DATE=N/A

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SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE	SHT	OF
NONE	27	111

Page Notes

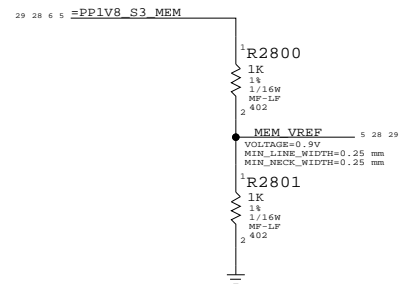
Power aliases required by this page:
- =PPIV8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

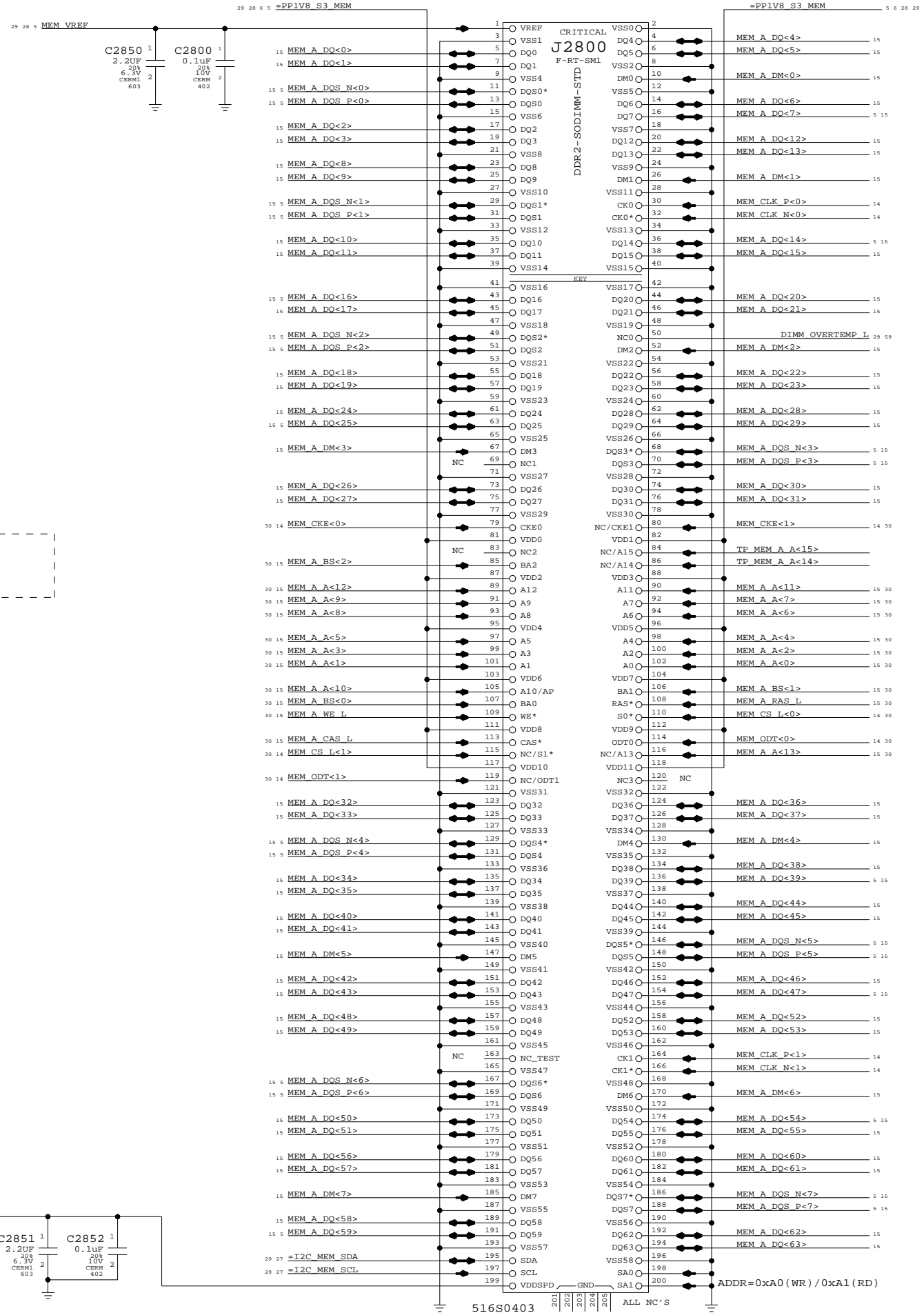
BOM options provided by this page:
(NONE)

DDR2 Vref

One 0.1uF per connector

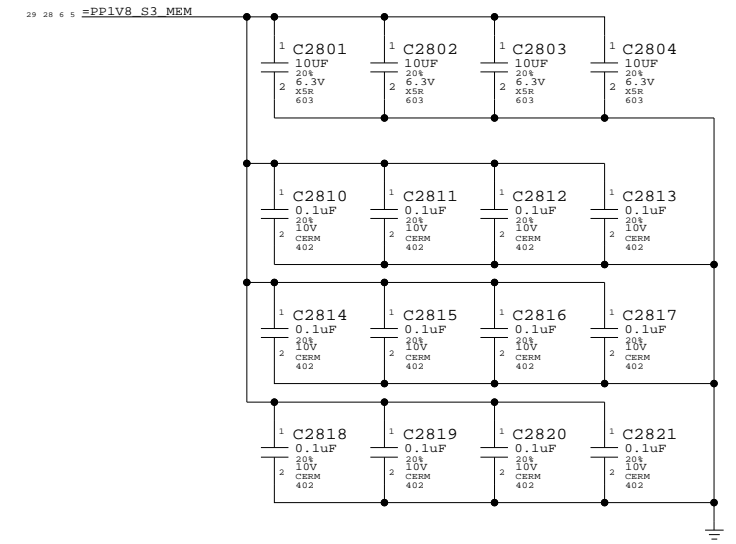


Yellow uses 10K divider and TLV2463 to drive MCH and DIMM connectors.
(See Capell Valley pg 47)



DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector A
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6949	09
SCALE	SHT	OF	
NONE	28	111	

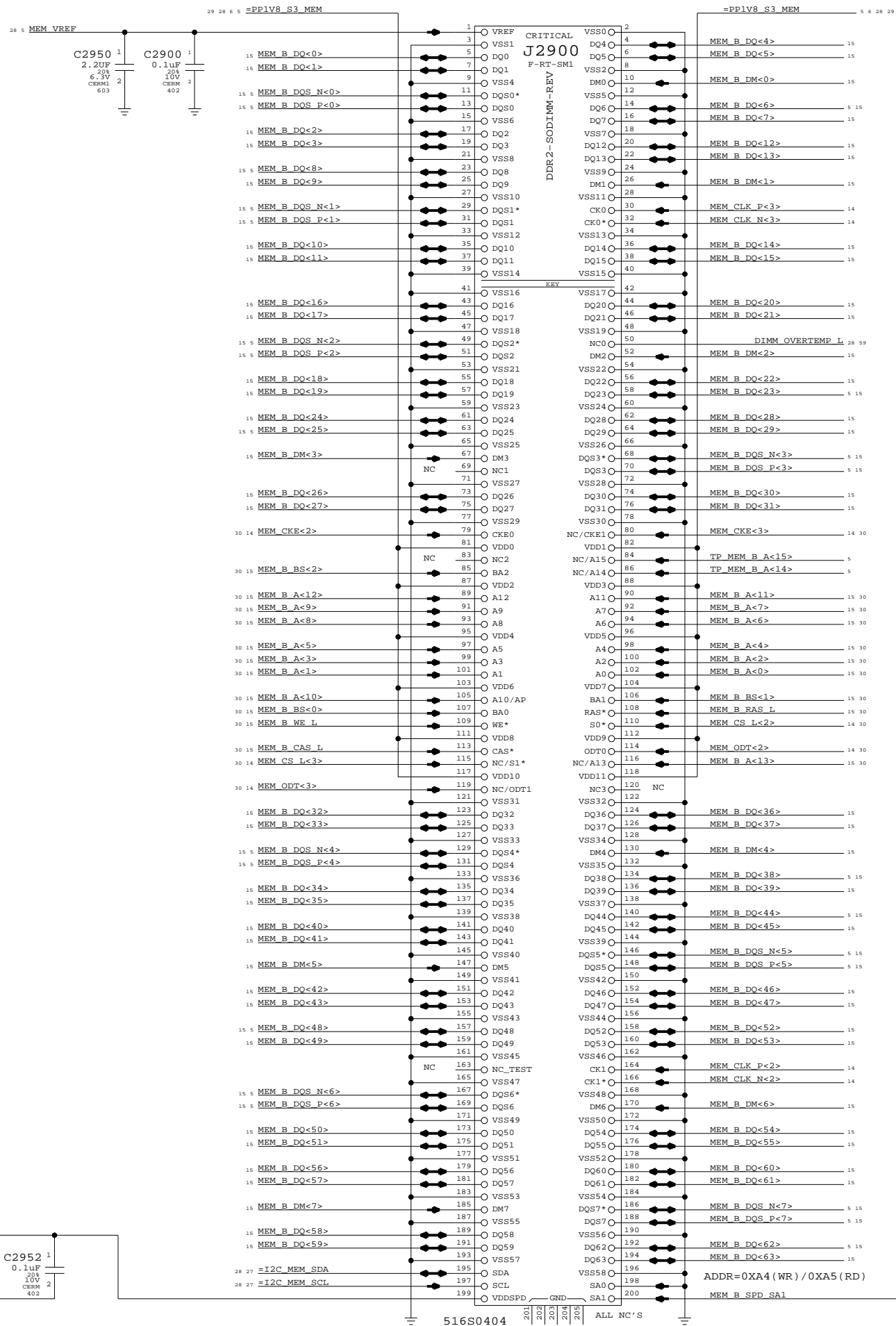
Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

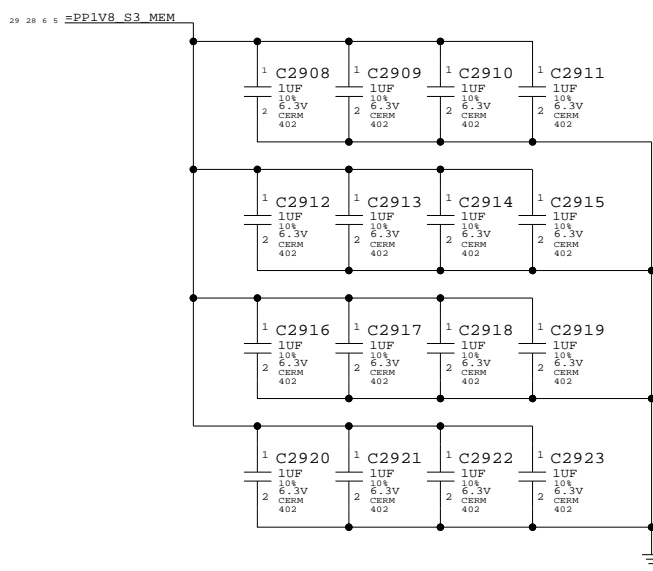
BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided by another page.



DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE	DRAWING NUMBER	REV.
NONE	051-6949	09
SHT	OF	
29	111	



APPLE COMPUTER INC.

8

7

6

5

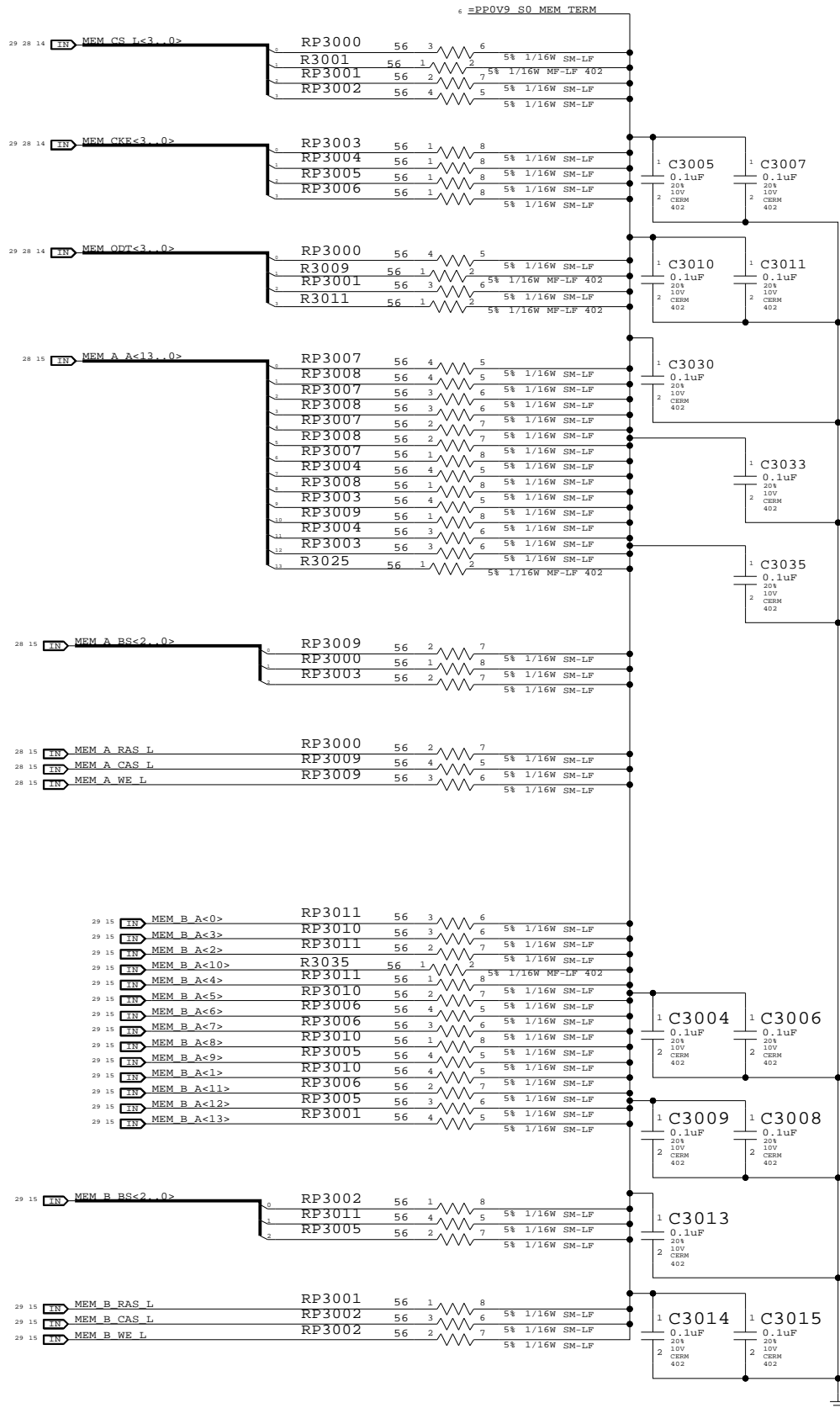
4

3

2

1

One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



Memory Active Termination

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	D	051-6949	09
SCALE	SHT OF		
NONE	30		111

8

7

6

5

4

3

2

1

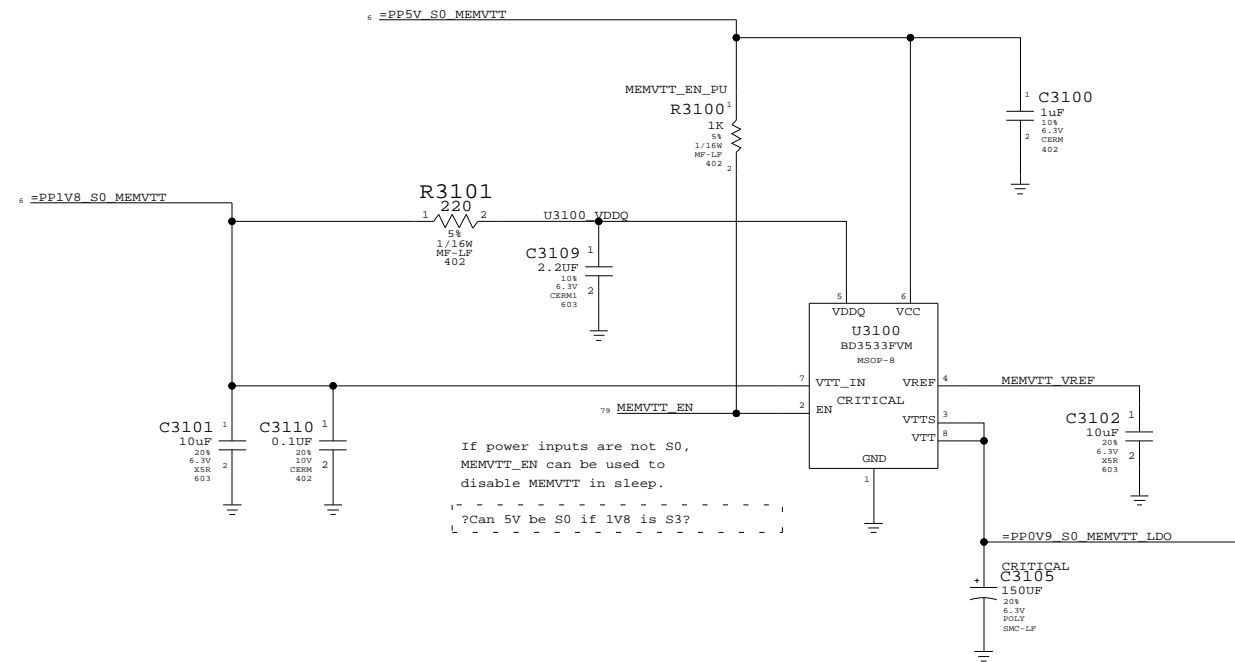
Page Notes

Power aliases required by this page:
 - =PP5V_S0_MEMVTT
 - =PP1V8_S0_MEMVTT
 - =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

DDR2 Vtt Regulator



Memory Vtt Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

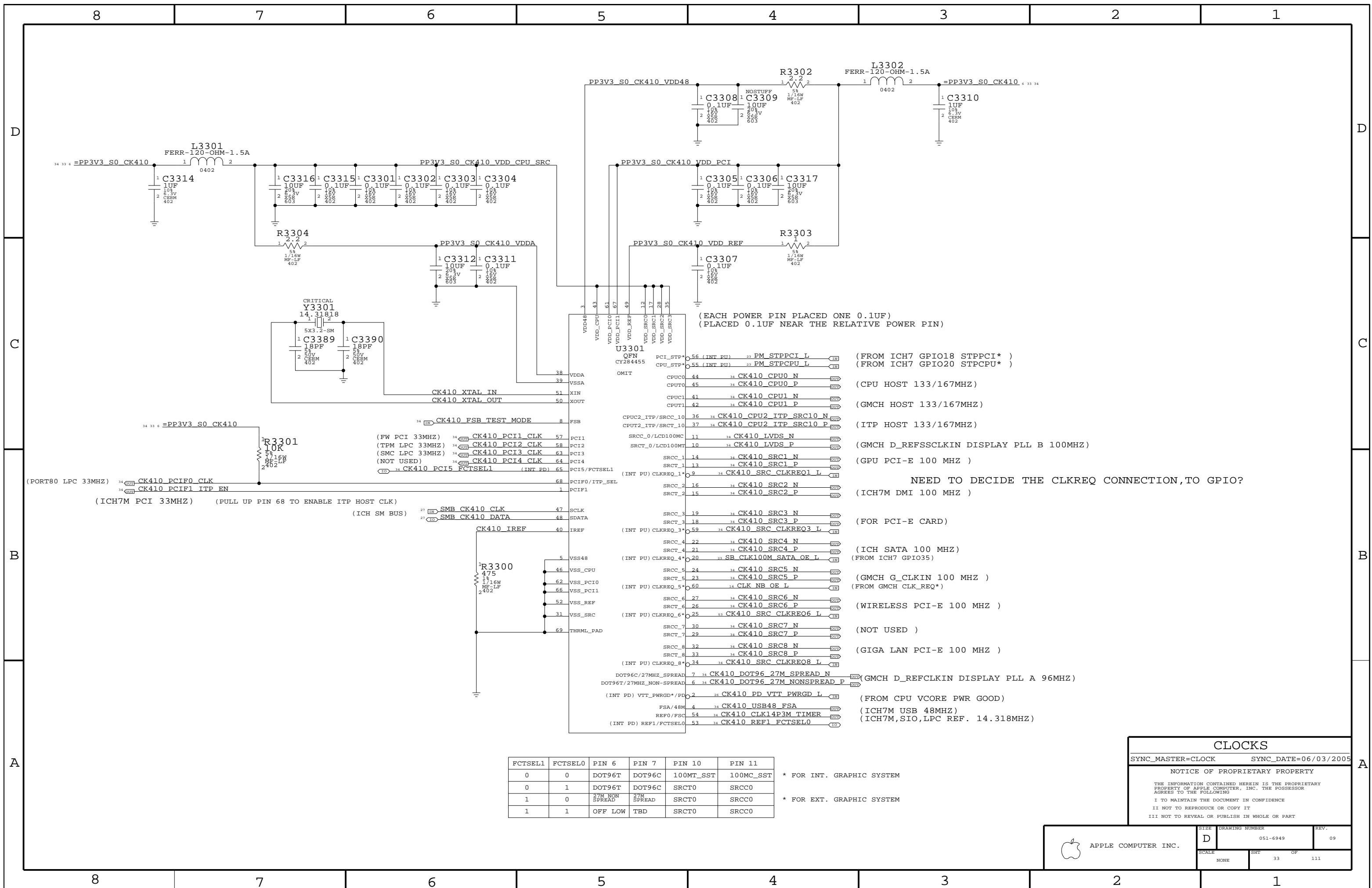
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	D	051-6949	09
SCALE	SHT	OF	
NONE	31	111	



(EACH POWER PIN PLACED ONE 0.1UF)
(PLACED 0.1UF NEAR THE RELATIVE POWER PIN)

(FROM ICH7 GPIO18 STPPCI*)
(FROM ICH7 GPIO20 STPCPU*)

(CPU HOST 133/167MHZ)

(GMCH HOST 133/167MHZ)

(ITP HOST 133/167MHZ)

(GMCH D_REFSSCLKIN DISPLAY PLL B 100MHZ)

(GPU PCI-E 100 MHZ)

NEED TO DECIDE THE CLKREQ CONNECTION, TO GPIO?

(ICH7M DMI 100 MHZ)

(FOR PCI-E CARD)

(ICH SATA 100 MHZ)

(FROM ICH7 GPIO35)

(GMCH G_CLKIN 100 MHZ)

(FROM GMCH CLK_REQ*)

(WIRELESS PCI-E 100 MHZ)

(NOT USED)

(GIGA LAN PCI-E 100 MHZ)

(GMCH D_REFCLKIN DISPLAY PLL A 96MHZ)

(FROM CPU VCORE PWR GOOD)

(ICH7M USB 48MHZ)

(ICH7M, SIO, LPC REF. 14.318MHZ)

FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST
0	1	DOT96T	DOT96C	SRCT0	SRCC0
1	0	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0
1	1	OFF LOW	TBD	SRCT0	SRCC0

* FOR INT. GRAPHIC SYSTEM

* FOR EXT. GRAPHIC SYSTEM

CLOCKS

SYNC_MASTER=CLOCK SYNC_DATE=06/03/2005

NOTICE OF PROPRIETARY PROPERTY

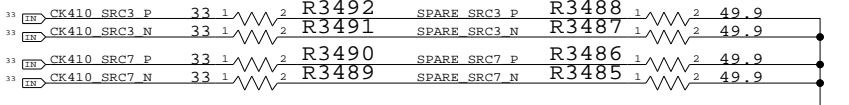
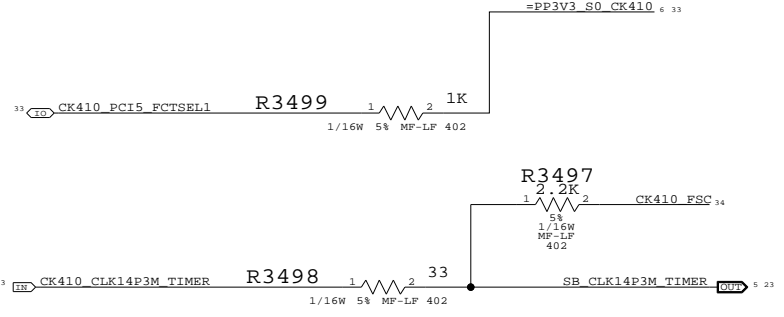
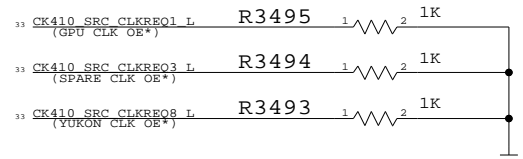
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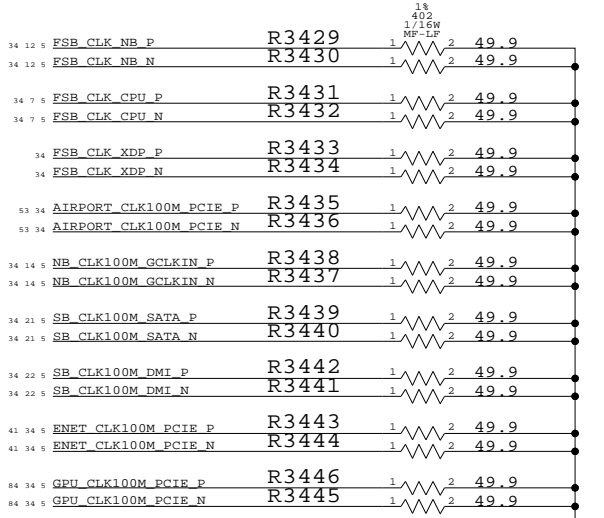
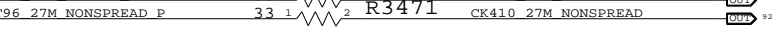
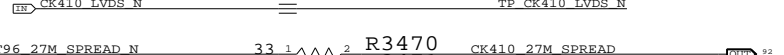
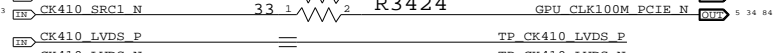
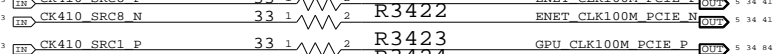
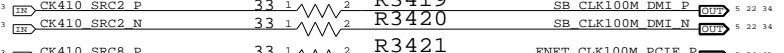
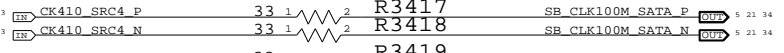
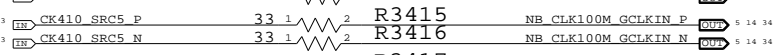
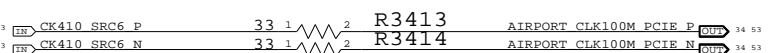
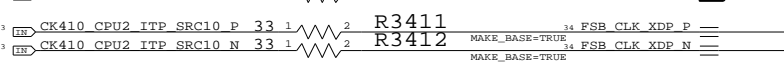
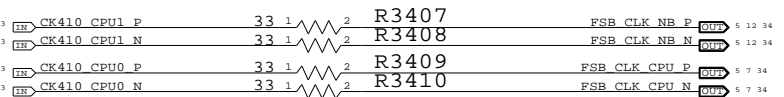
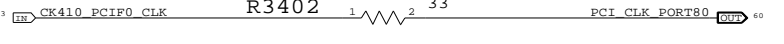
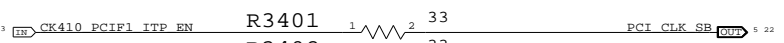
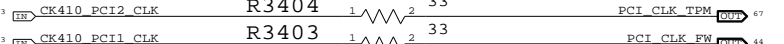
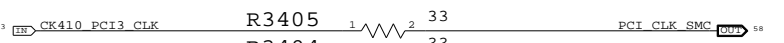
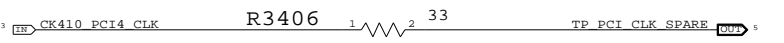
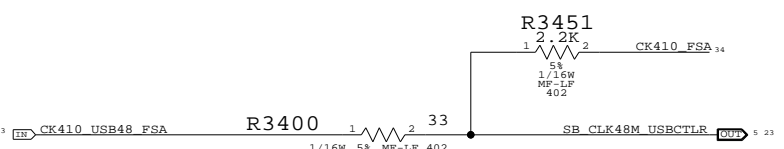
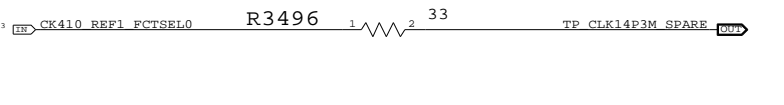
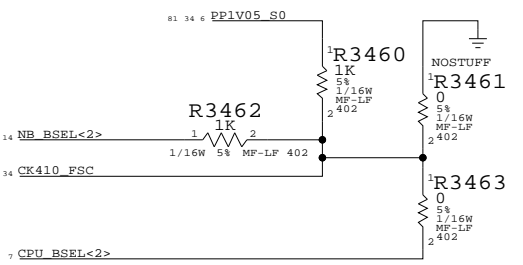
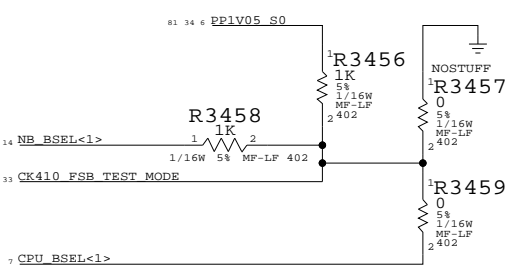
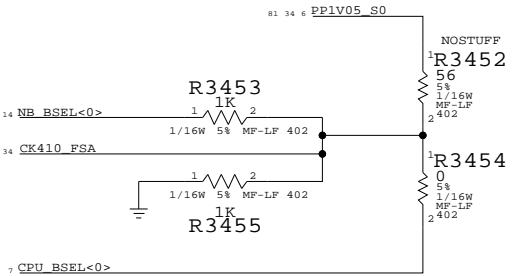
SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE	SHT	OF
NONE	33	111

NOTE: USE THESE PULL-DOWNS IF NOT CONNECTED TO GPIO'S



FSB FREQUENCY SELECT:

	STUFF	NO STUFF
CPU DRIVEN	R3453 R3454 R3455	R3456 R3457
533MHZ (133MHZ CPU CLK)	R3452 R3461	R3458 R3459
667MHZ (166MHZ CPU CLK)	R3452 R3461	R3458 R3459



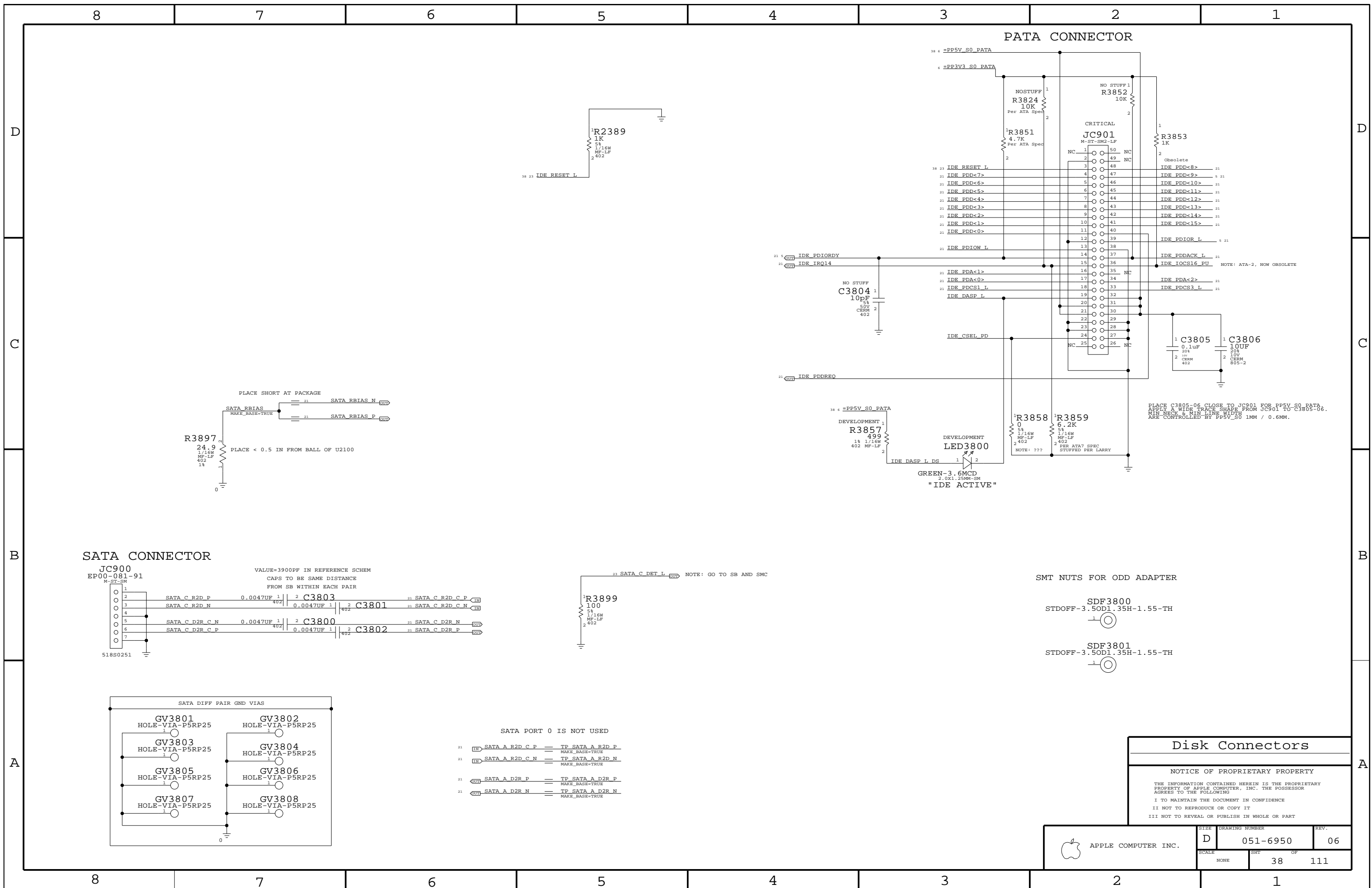
CLOCKS: TERMINATIONS

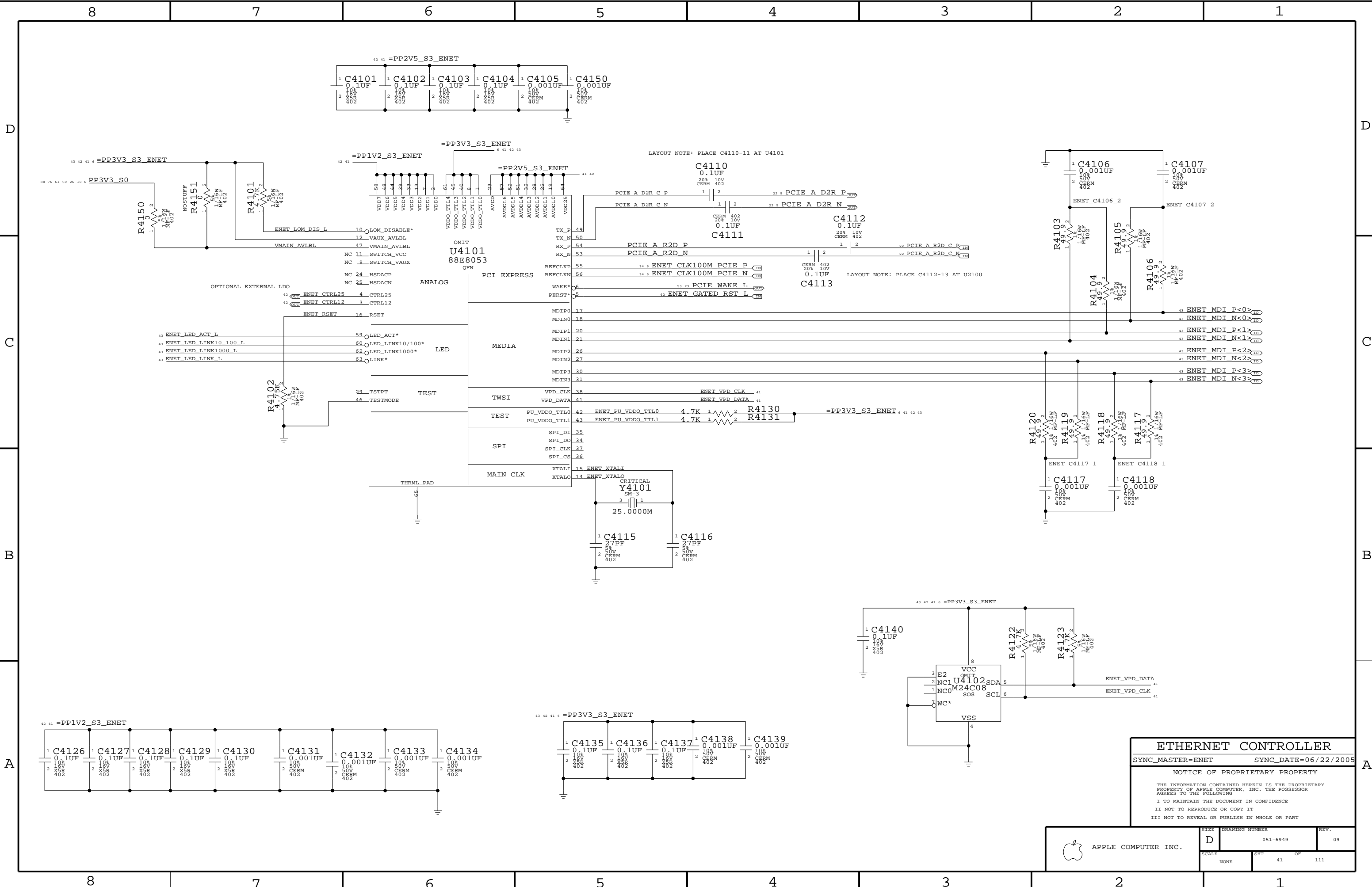
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SCALE	SHT	OF
NONE	34	111





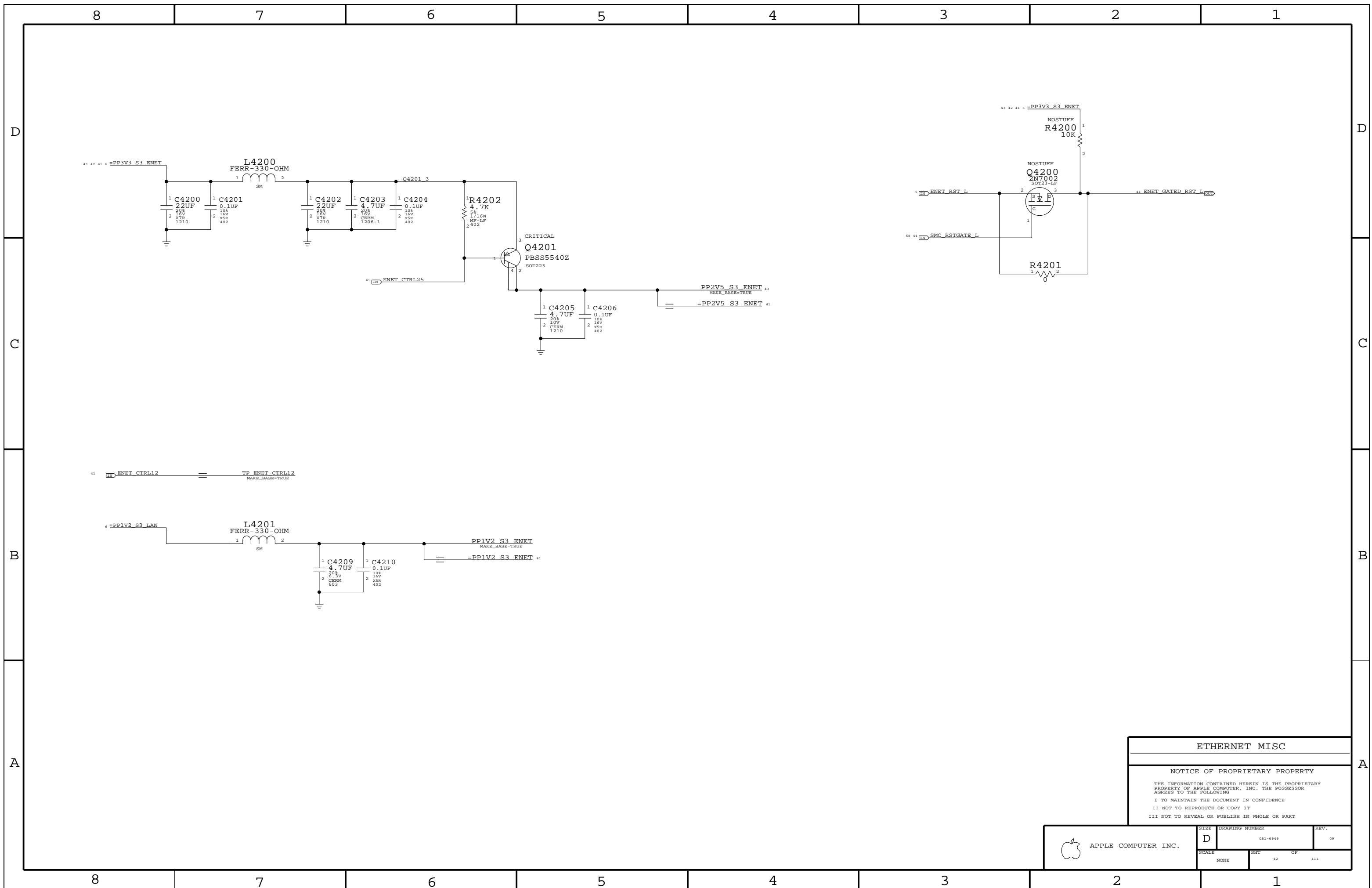
ETHERNET CONTROLLER

SYNC_MASTER=ENET SYNC_DATE=06/22/2005

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	SCALE NONE	SHEET 41	OF 111



ETHERNET MISC

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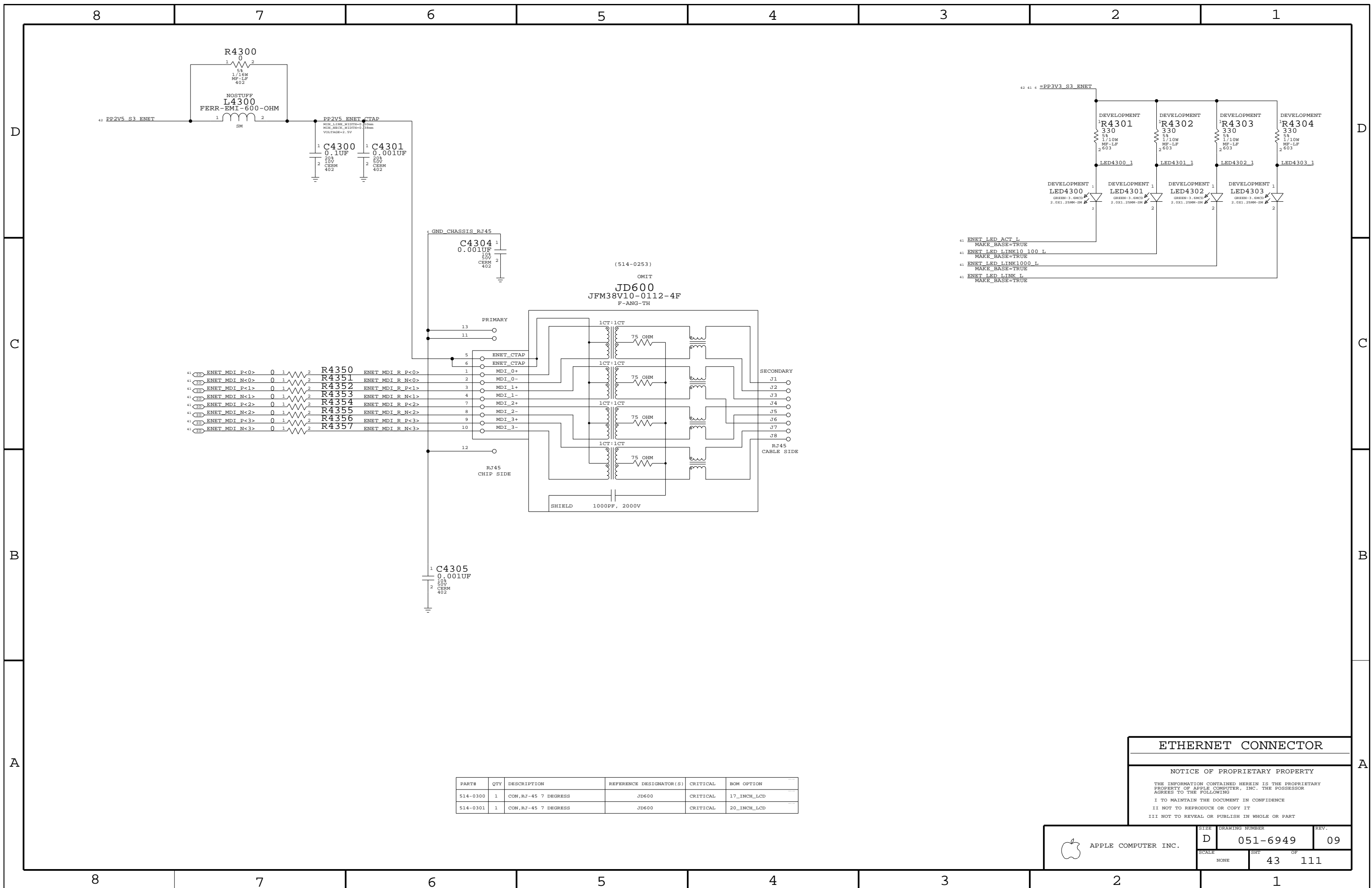
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6949	REV. 09
	SCALE NONE	SHEET 42	OF 111



ENET MDI P<0>	0	1	2	R4350	ENET MDI R P<0>
ENET MDI N<0>	0	1	2	R4351	ENET MDI R N<0>
ENET MDI P<1>	0	1	2	R4352	ENET MDI R P<1>
ENET MDI N<1>	0	1	2	R4353	ENET MDI R N<1>
ENET MDI P<2>	0	1	2	R4354	ENET MDI R P<2>
ENET MDI N<2>	0	1	2	R4355	ENET MDI R N<2>
ENET MDI P<3>	0	1	2	R4356	ENET MDI R P<3>
ENET MDI N<3>	0	1	2	R4357	ENET MDI R N<3>

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0300	1	CON,RJ-45 7 DEGRESS	JD600	CRITICAL	17_INCH_LCD
514-0301	1	CON,RJ-45 7 DEGRESS	JD600	CRITICAL	20_INCH_LCD

ETHERNET CONNECTOR

NOTICE OF PROPRIETARY PROPERTY

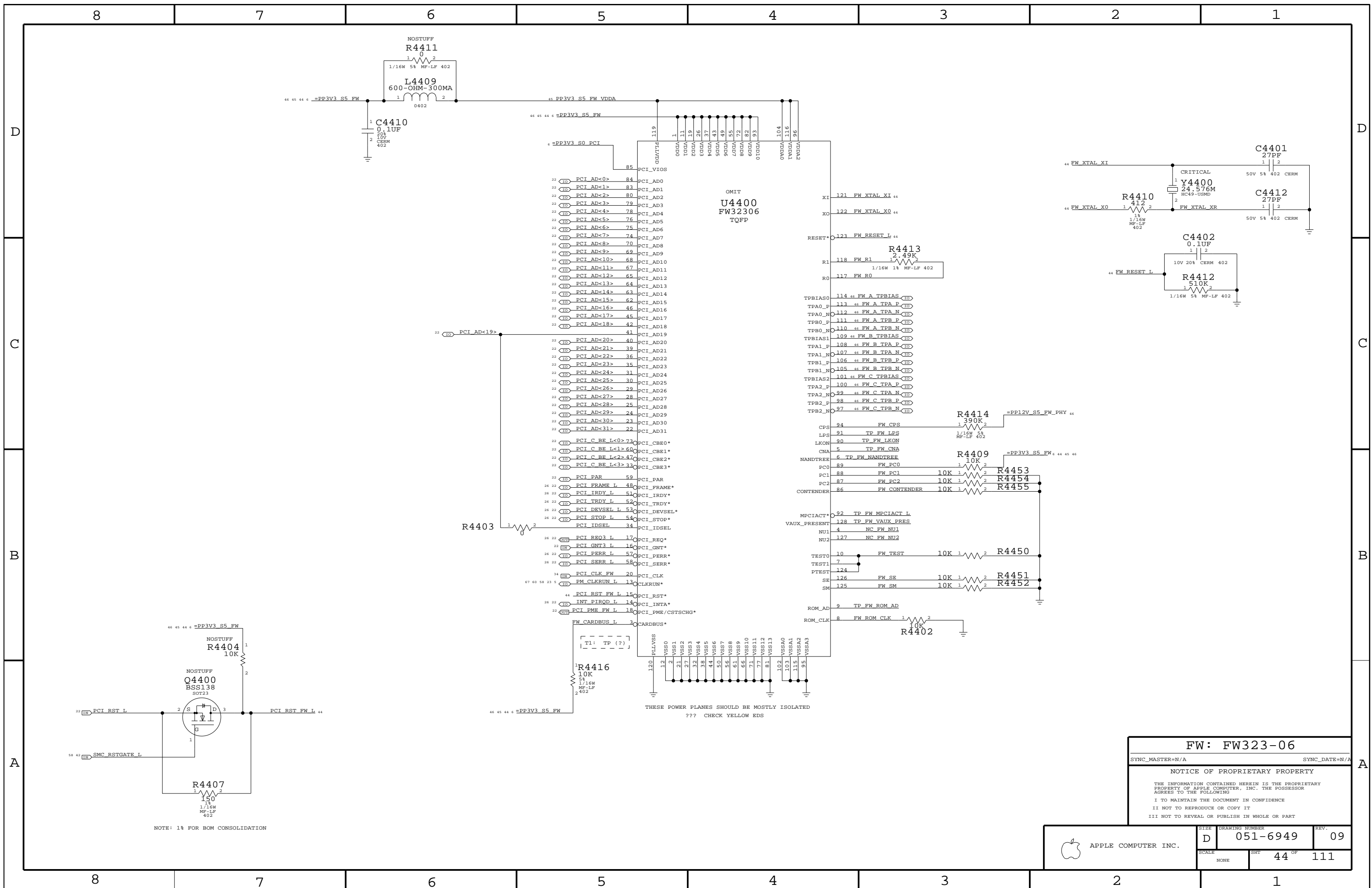
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SCALE	SHT		OF
NONE	43		111



FW: FW323-06

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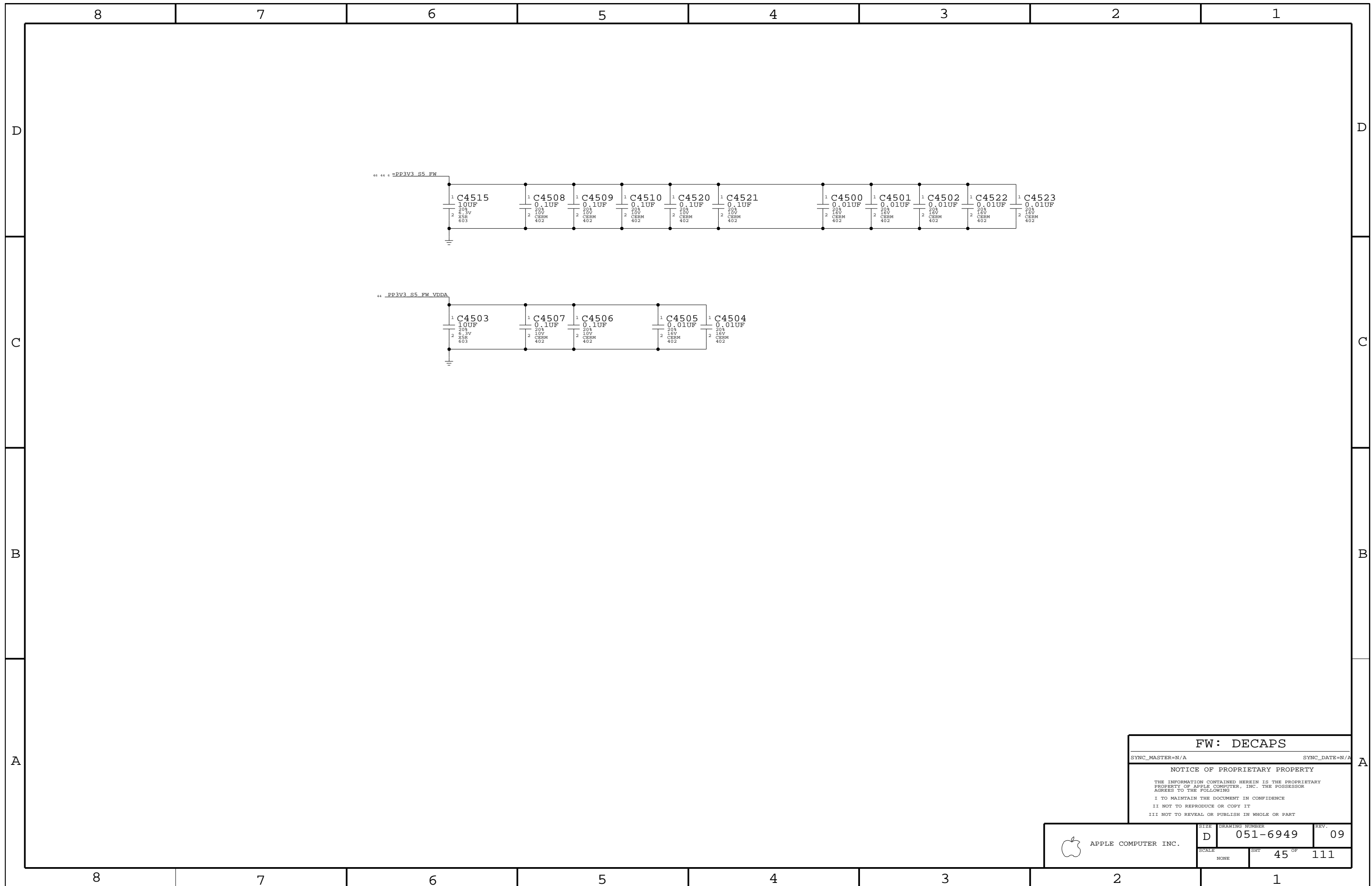
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NOTE: 1% FOR BOM CONSOLIDATION

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6949	REV. 09
	SCALE NONE	SHEET 44 OF 111	



FW: DECAPS

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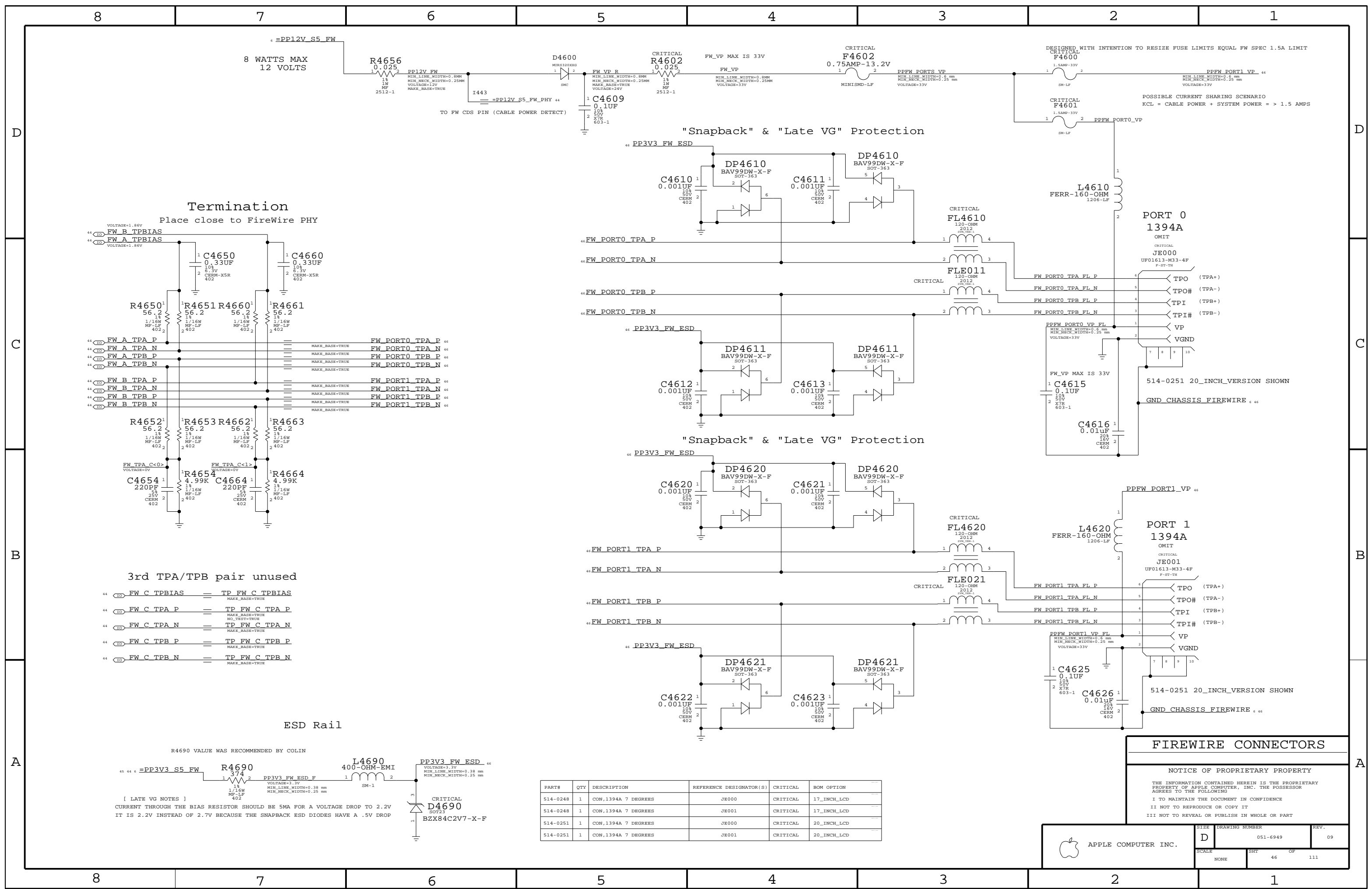
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	D	051-6949	09
SCALE	SHT	OF	
NONE	45	111	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0248	1	CON, 1394A 7 DEGREES	JE000	CRITICAL	17_INCH_LCD
514-0248	1	CON, 1394A 7 DEGREES	JE001	CRITICAL	17_INCH_LCD
514-0251	1	CON, 1394A 7 DEGREES	JE000	CRITICAL	20_INCH_LCD
514-0251	1	CON, 1394A 7 DEGREES	JE001	CRITICAL	20_INCH_LCD

FIREWIRE CONNECTORS

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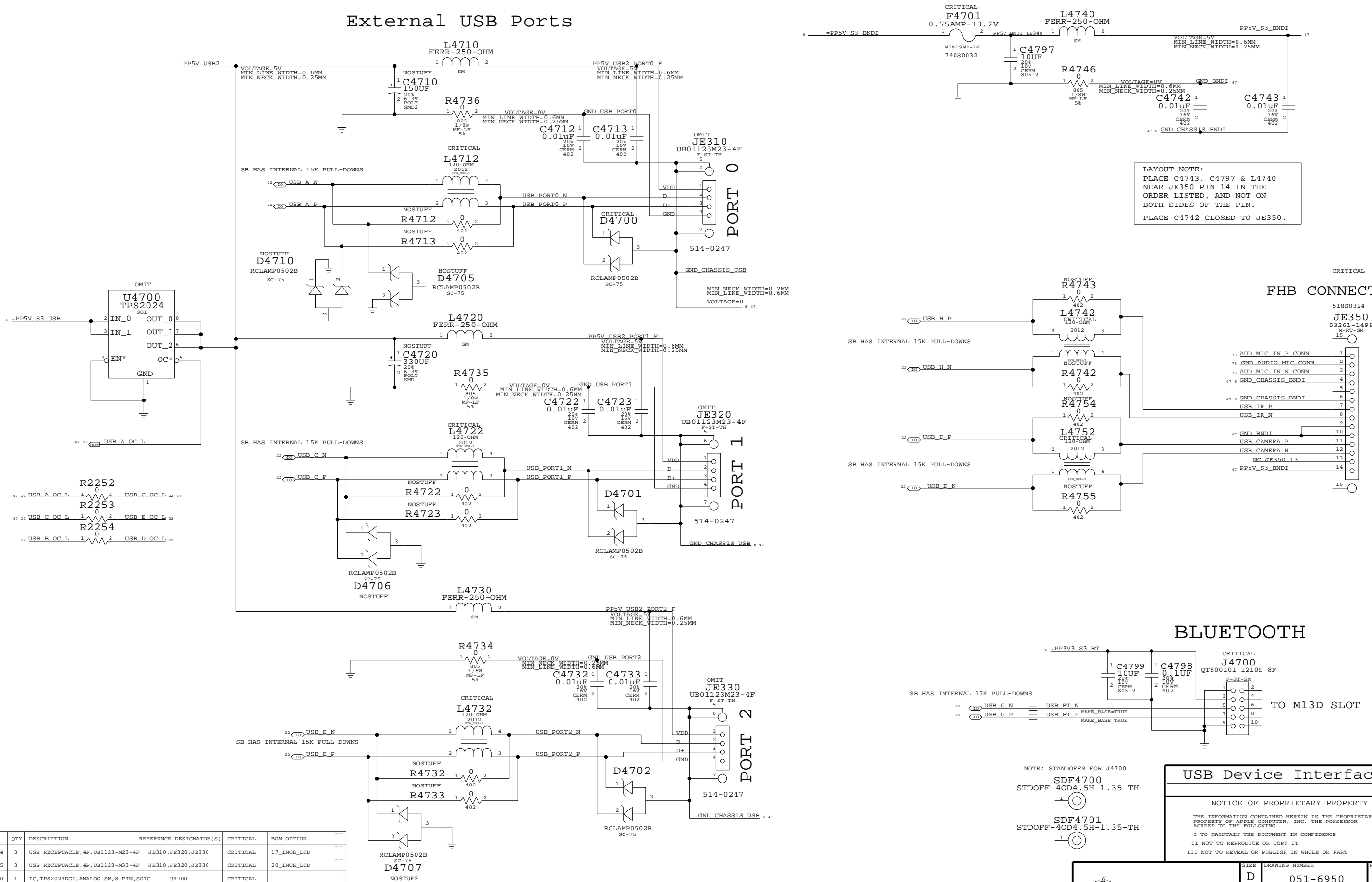
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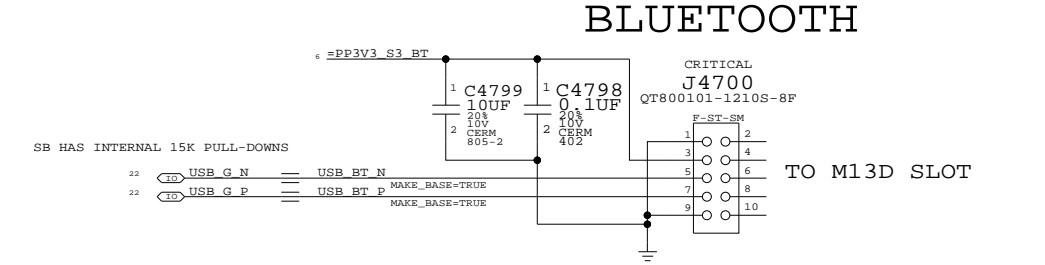
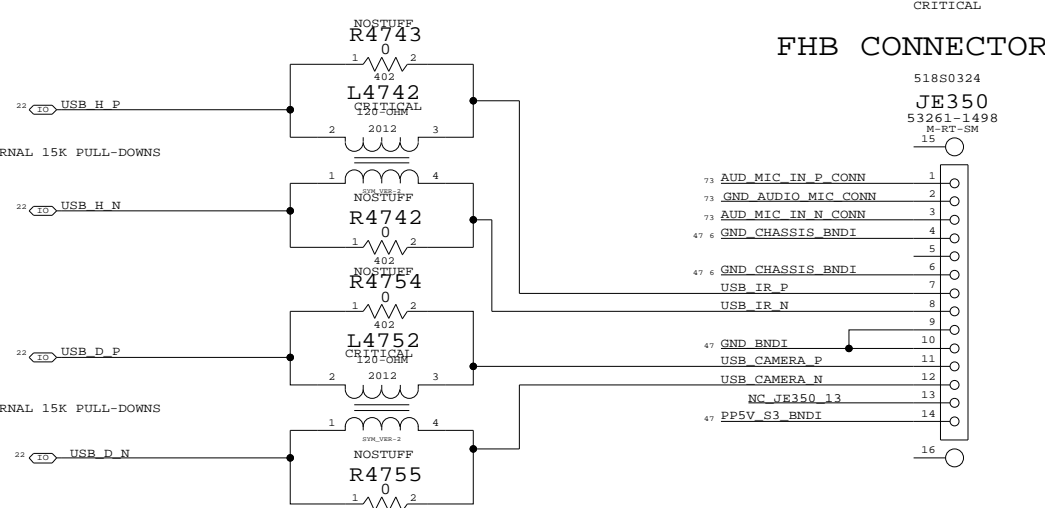
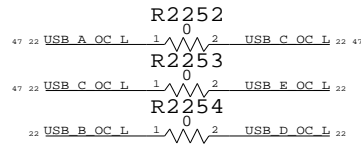
SCALE: NONE SHEET: 46 OF 111

DRAWING NUMBER: 051-6949 REV: 09

External USB Ports



LAYOUT NOTE:
 PLACE C4743, C4797 & L4740
 NEAR JE350 PIN 14 IN THE
 ORDER LISTED, AND NOT ON
 BOTH SIDES OF THE PIN.
 PLACE C4742 CLOSED TO JE350.



NOTE: STANDOFFS FOR J4700
 SDF4700
 STDOFF-40D4.5H-1.35-TH
 SDF4701
 STDOFF-40D4.5H-1.35-TH

USB Device Interfaces

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0294	3	USB RECEPTACLE,4P,UB1123-M23-4F	JE310,JE320,JE330	CRITICAL	17_INCH_LCD
514-0295	3	USB RECEPTACLE,4P,UB1123-M33-4F	JE310,JE320,JE330	CRITICAL	20_INCH_LCD
353S1370	1	IC,TPS2023DG4,ANALOG SW,8 PIN,SOIC	U4700	CRITICAL	

APPLE COMPUTER INC.

DRAWING NUMBER: 051-6950

REV: 06

SCALE: NONE

SHT: 47

OF: 111

8

7

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	SCALE NONE	SHEET 48 OF	111

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6

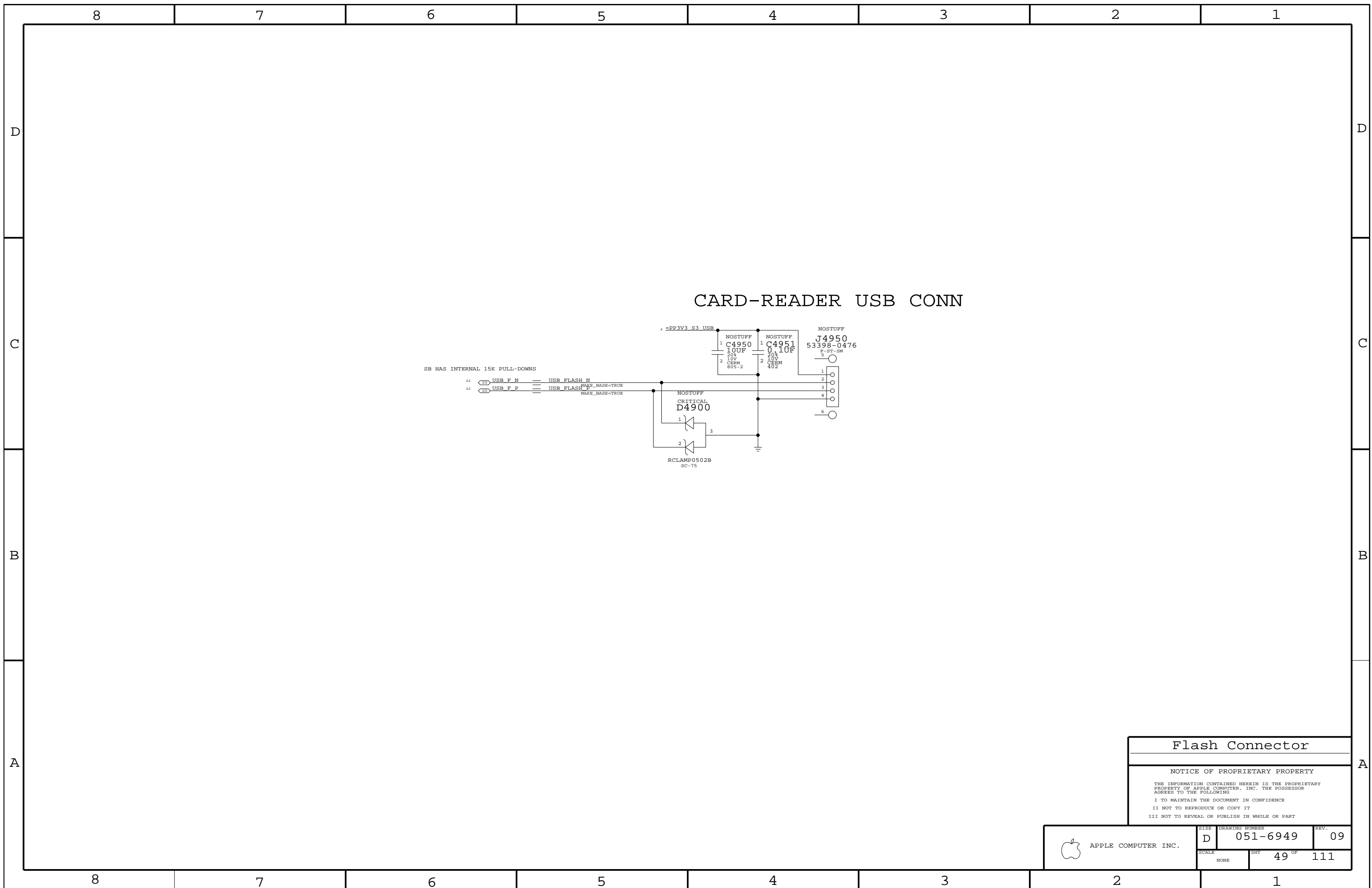
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4

3

2

1



CARD-READER USB CONN

Flash Connector

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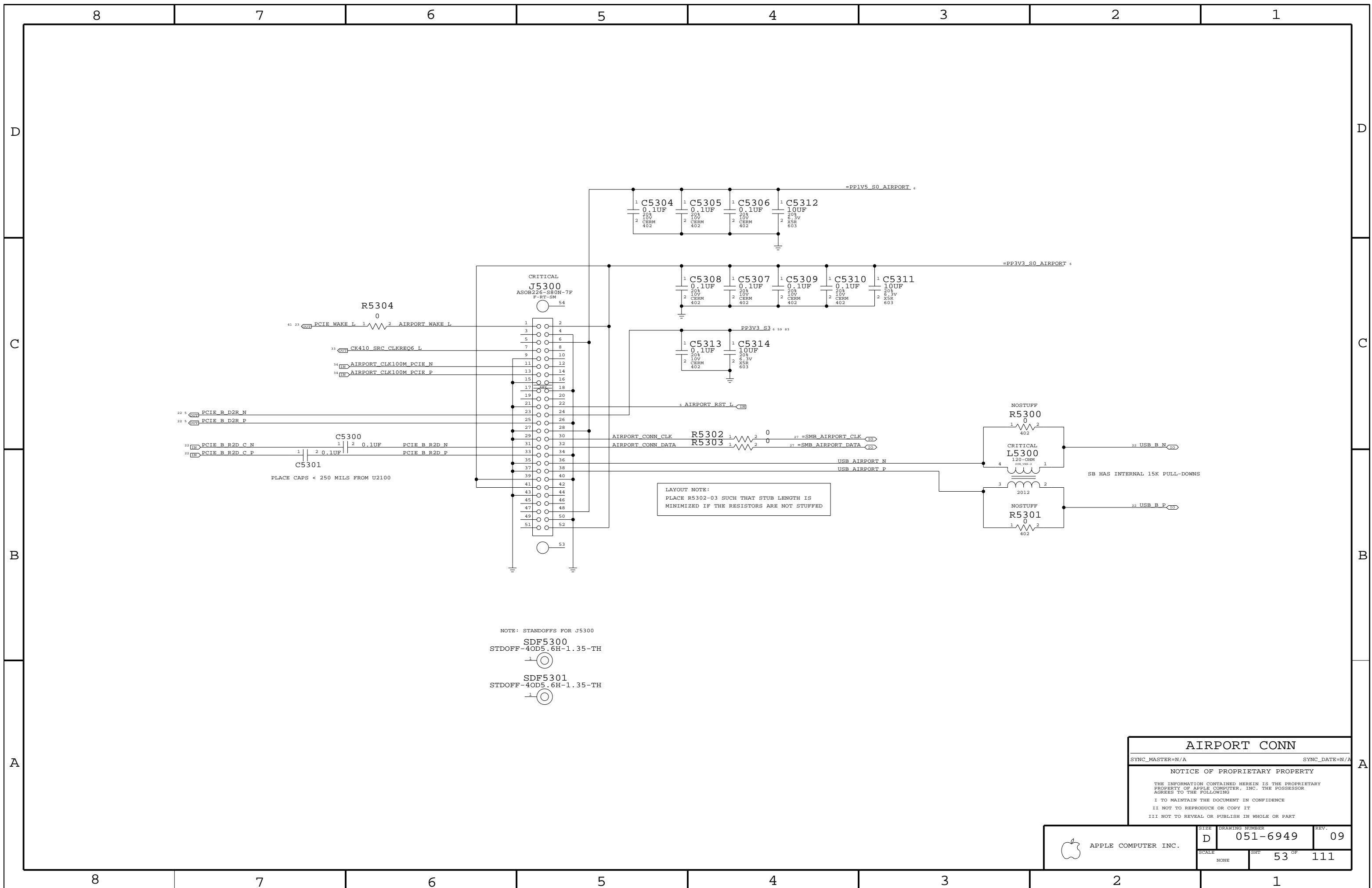
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	SCALE NONE	SHEET 49 OF 111	



R5304
0

41 23 PCIE WAKE L 1 2 AIRPORT WAKE L

33 CK410_SRC_CLKREQ6 L

34 AIRPORT_CLK100M_PCIE_N

34 AIRPORT_CLK100M_PCIE_P

22 5 PCIE_B_D2R_N

22 6 PCIE_B_D2R_P

C5300

22 5 PCIE_B_R2D_C_N

22 6 PCIE_B_R2D_C_P

C5301

PLACE CAPS < 250 MILS FROM U2100

=PP1V5_S0_AIRPORT

C5304 0.1UF

C5305 0.1UF

C5306 0.1UF

C5312 10UF

=PP3V3_S0_AIRPORT

C5308 0.1UF

C5307 0.1UF

C5309 0.1UF

C5310 0.1UF

C5311 10UF

PP3V3_S3 6 59 83

C5313 0.1UF

C5314 10UF

AIRPORT_CONN_CLK R5302 1 2 0

AIRPORT_CONN_DATA R5303 1 2 0

23 =SMB_AIRPORT_CLK

27 =SMB_AIRPORT_DATA

NOSTUFF R5300 0

CRITICAL L5300 120-OHM

NOSTUFF R5301 0

22 USB_B_N

22 USB_B_P

SB HAS INTERNAL 15K PULL-DOWNS

LAYOUT NOTE:

PLACE R5302-03 SUCH THAT STUB LENGTH IS MINIMIZED IF THE RESISTORS ARE NOT STUFFED

NOTE: STANDOFFS FOR J5300

SDF5300

STDOFF-4OD5.6H-1.35-TH

SDF5301

STDOFF-4OD5.6H-1.35-TH

AIRPORT CONN

SYNC_MASTER=N/A SYNC_DATE=N/A

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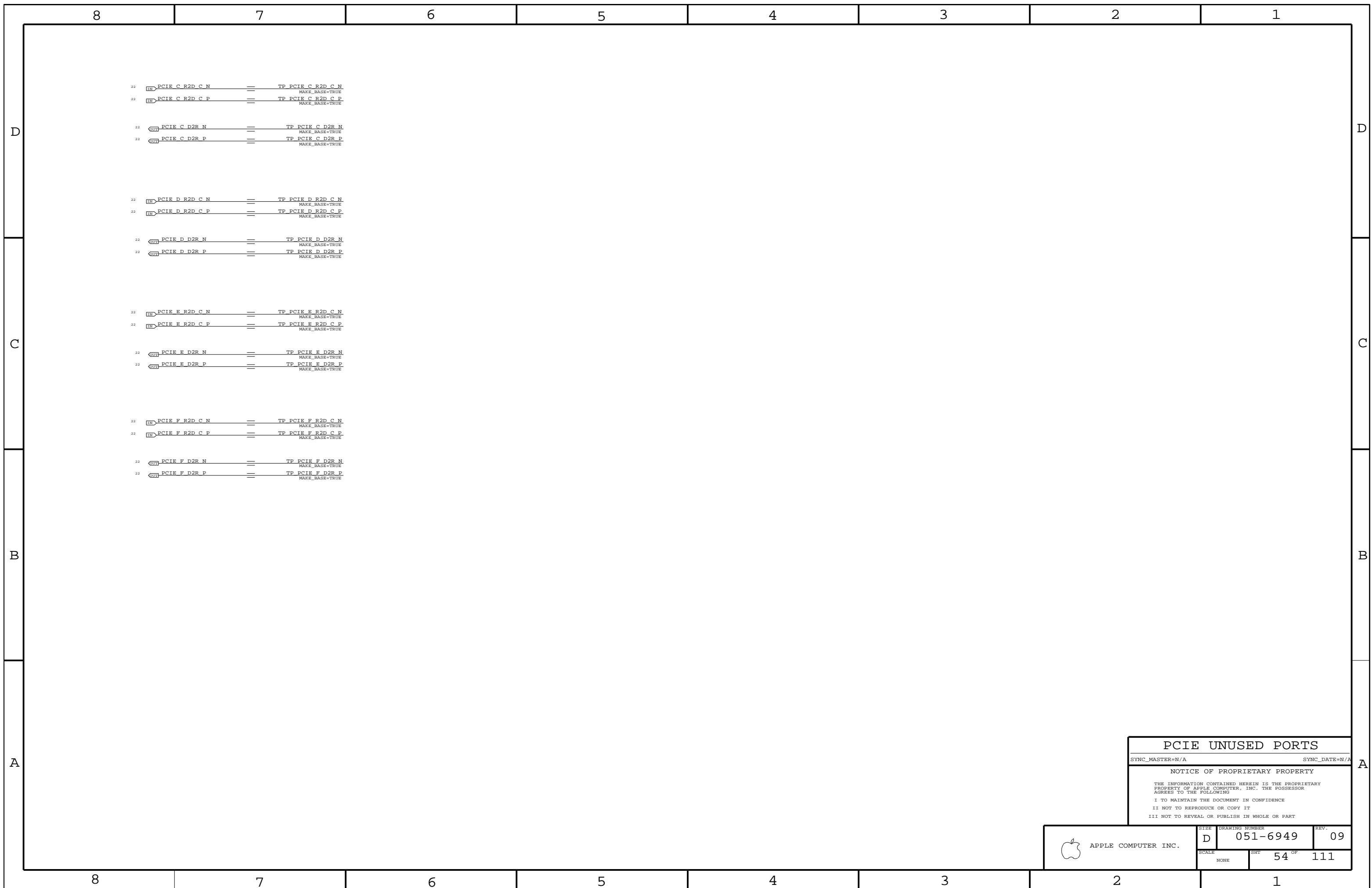
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SCALE NONE SHEET 53 OF 111

DRAWING NUMBER 051-6949 REV. 09




PCIE UNUSED PORTS

SYNC_MASTER=N/A SYNC_DATE=N/A

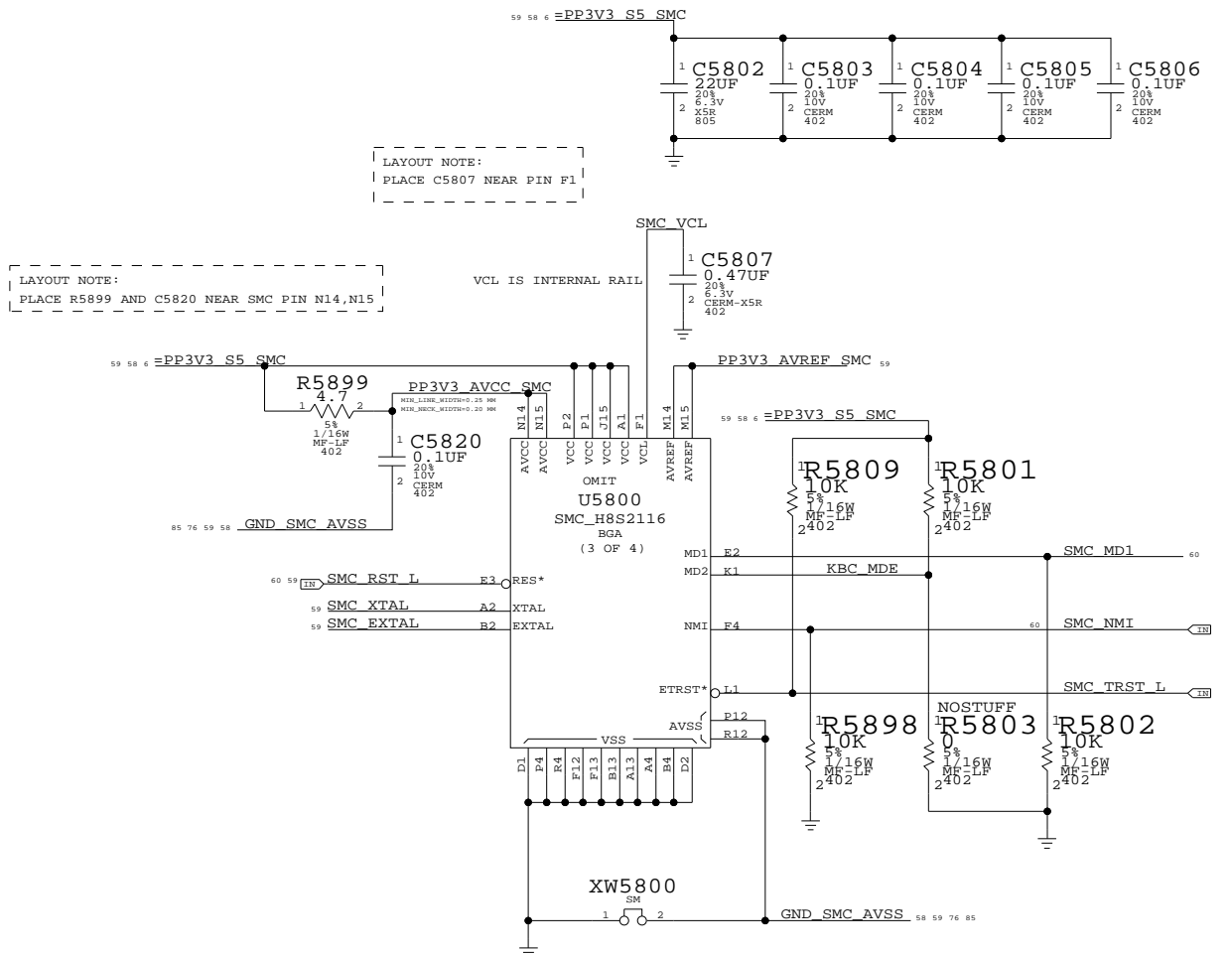
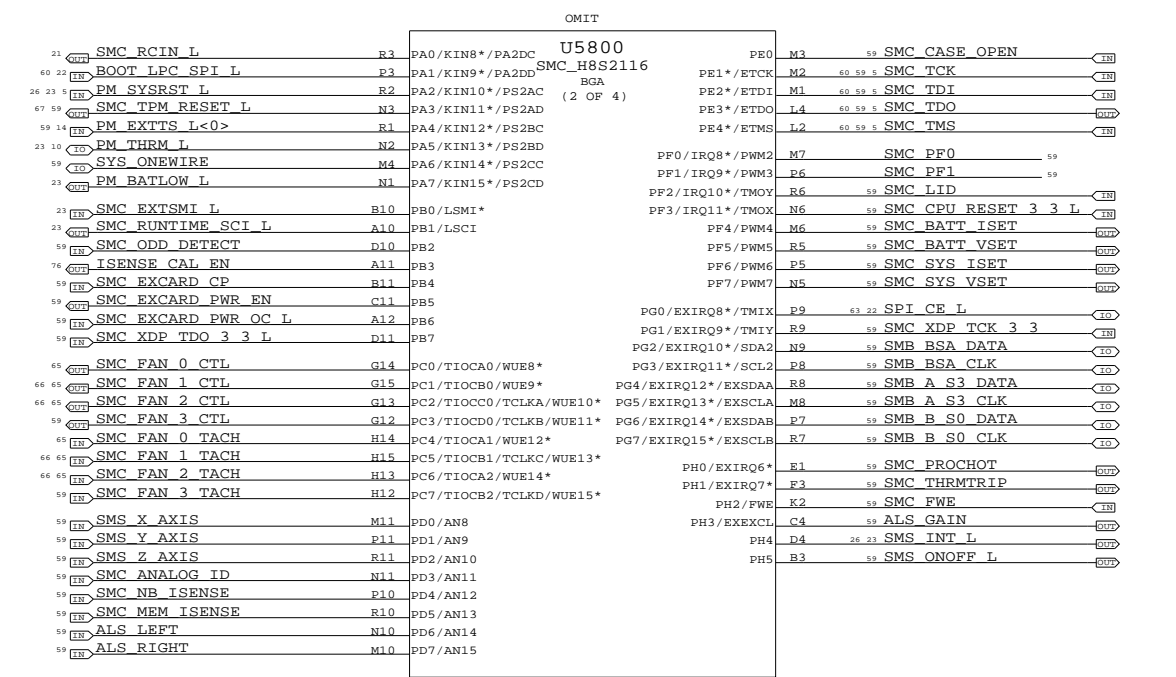
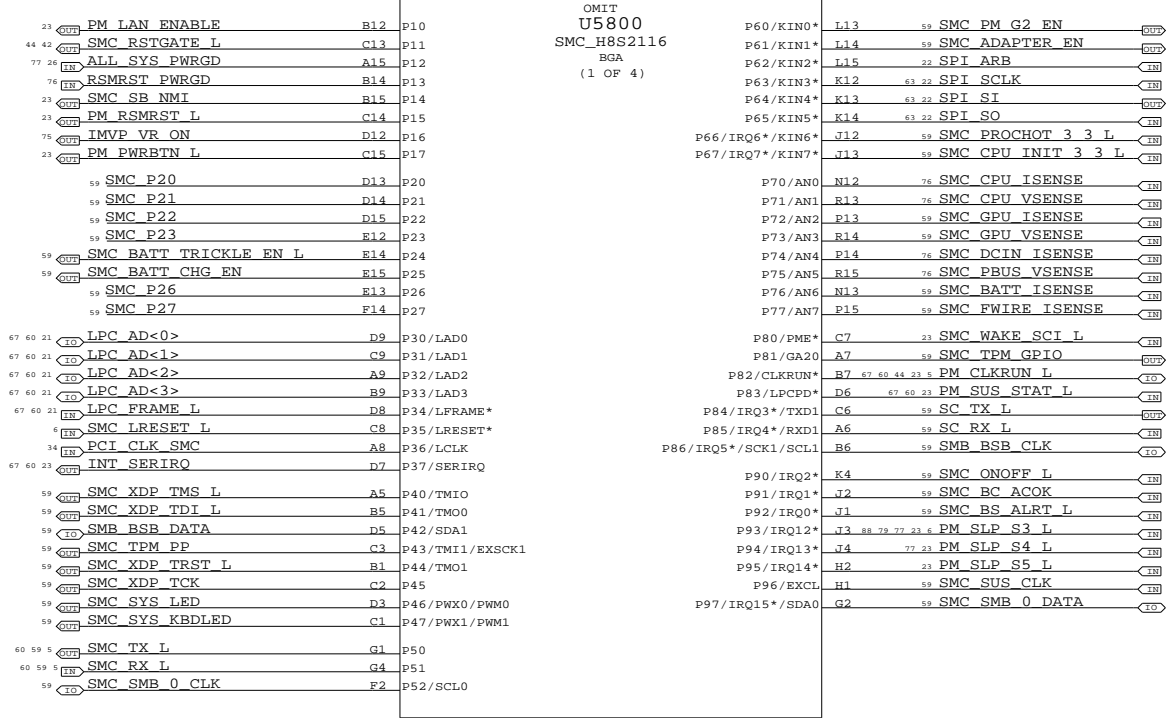
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	D	051-6949	09
SCALE	SHT		OF
NONE	54		111

UNUSED PINS HAVE THE FORMAT SMC_XXX WHERE XXX IS THE PORT NUMBER. THEY ARE SET BY SOFTWARE TO BE DRIVEN OUTPUTS ALWAYS SO THEY CAN BE LEFT NO-CONNECTED.

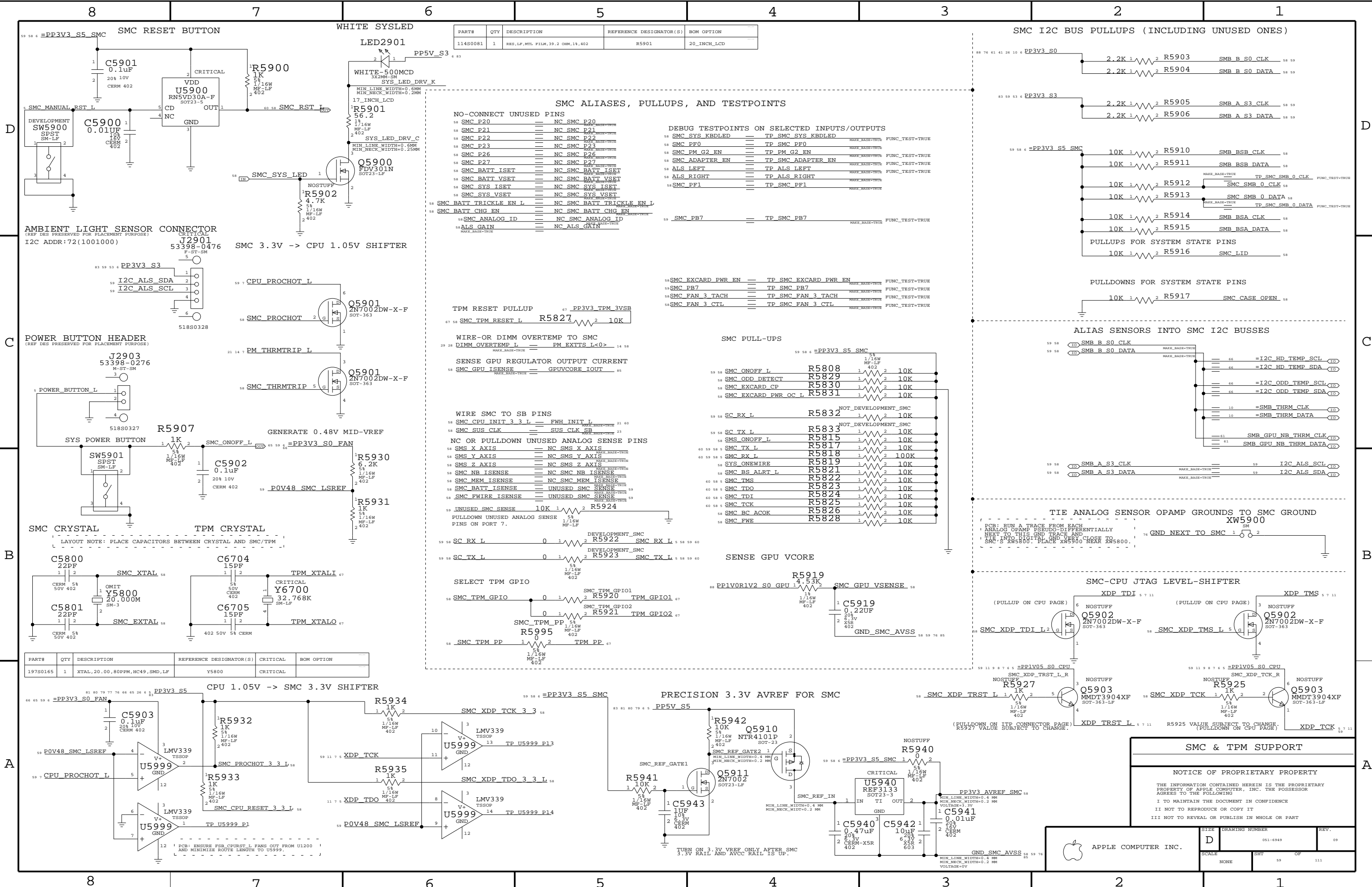


LAYOUT NOTE: PLACE C5807 NEAR PIN F1

LAYOUT NOTE: PLACE R5899 AND C5820 NEAR SMC PIN N14,N15

SMC SYNC_MASTER=N/A SYNC_DATE=N/A NOTICE OF PROPRIETARY PROPERTY THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC. DRAWING NUMBER 051-6949 REV. 09 SCALE NONE SHT 58 OF 111



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
11450081	1	RES,LP,WTL FILM,39.2 OHM,14,402	R5901	20_INCH_LCD

SMC ALIASES, PULLUPS, AND TESTPOINTS

NO-CONNECT UNUSED PINS	DEBUG TESTPOINTS ON SELECTED INPUTS/OUTPUTS
58 SMC P20 == NC SMC P20	58 SMC SYS_KBDLED == TP_SMC_SYS_KBDLED MAKE_BASE=TRUE FUNC_TEST=TRUE
58 SMC P21 == NC SMC P21	58 SMC PF0 == TP_SMC_PF0 MAKE_BASE=TRUE
58 SMC P22 == NC SMC P22	58 SMC PM_G2_EN == TP_PM_G2_EN MAKE_BASE=TRUE
58 SMC P23 == NC SMC P23	58 SMC_ADAPTER_EN == TP_SMC_ADAPTER_EN MAKE_BASE=TRUE FUNC_TEST=TRUE
58 SMC P26 == NC SMC P26	58 ALS_LEFT == TP_ALS_LEFT MAKE_BASE=TRUE FUNC_TEST=TRUE
58 SMC P27 == NC SMC P27	58 ALS_RIGHT == TP_ALS_RIGHT MAKE_BASE=TRUE FUNC_TEST=TRUE
58 SMC_BATT_ISET == NC SMC_BATT_ISET	58 SMC_PF1 == TP_SMC_PF1 MAKE_BASE=TRUE
58 SMC_BATT_VSET == NC SMC_BATT_VSET	
58 SMC_SYS_ISET == NC SMC_SYS_ISET	
58 SMC_SYS_VSET == NC SMC_SYS_VSET	
58 SMC_BATT_TRICKLE_EN_L == NC SMC_BATT_TRICKLE_EN_L	59 SMC_PB7 == TP_SMC_PB7 MAKE_BASE=TRUE FUNC_TEST=TRUE
58 SMC_BATT_CHG_EN == NC SMC_BATT_CHG_EN	
58 SMC_ANALOG_ID == NC SMC_ANALOG_ID	
58 ALS_GAIN == NC ALS_GAIN	

SMC PULL-UPS

58 SMC_ONOFF_L	R5808	10K
58 SMC_ODD_DETECT	R5829	10K
58 SMC_EXCARD_CP	R5830	10K
58 SMC_EXCARD_PWR_OC_L	R5831	10K
58 SC_RX_L	R5832	10K
58 SC_TX_L	R5833	10K
58 SMS_ONOFF_L	R5815	10K
58 SMC_TX_L	R5817	10K
58 SMC_RX_L	R5818	100K
58 SYS_ONEWIRE	R5819	10K
58 SMC_BS_ALERT_L	R5821	10K
58 SMC_TMS	R5822	10K
58 SMC_TDO	R5823	10K
58 SMC_TDI	R5824	10K
58 SMC_TCK	R5825	10K
58 SMC_BC_ACOK	R5826	10K
58 SMC_FWE	R5828	10K

SMC CRISTALS

SMC XTAL	TPM XTAL
C5800 22PF	C6704 15PF
C5801 22PF	C6705 15PF
Y5800 20.000M	Y6700 32.768K

SMC CPU INIT 3 3 L

58 SMC_CPU_INIT_3_3_L	R5934	1K
58 SMC_XDP_TCK_3_3	R5932	1K
58 SMC_XDP_TDO_3_3_L	R5933	1K
58 SMC_XDP_TDI	R5927	1K
58 SMC_XDP_TCK_R	R5925	1K
58 SMC_XDP_TCK_L	R5925	1K

SMC & TPM SUPPORT

SMC REF	TPM
58 SMC_REF_GATE1	TP U5999_P1
58 SMC_REF_GATE2	TP U5999_P13
58 SMC_REF_IN	TP U5999_P14

SMC & TPM SUPPORT

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SMC & TPM SUPPORT

SMC	TPM
58 SMC_TPM_RESET_L	R5827
58 SMC_TPM_PP	R5995
58 SMC_TPM_GPIO	R5920, R5921
58 SMC_TPM_PP	R5995

SMC & TPM SUPPORT

SMC	TPM
58 SMC_TPM_RESET_L	R5827
58 SMC_TPM_PP	R5995
58 SMC_TPM_GPIO	R5920, R5921
58 SMC_TPM_PP	R5995

SMC & TPM SUPPORT

SMC	TPM
58 SMC_TPM_RESET_L	R5827
58 SMC_TPM_PP	R5995
58 SMC_TPM_GPIO	R5920, R5921
58 SMC_TPM_PP	R5995

SMC & TPM SUPPORT

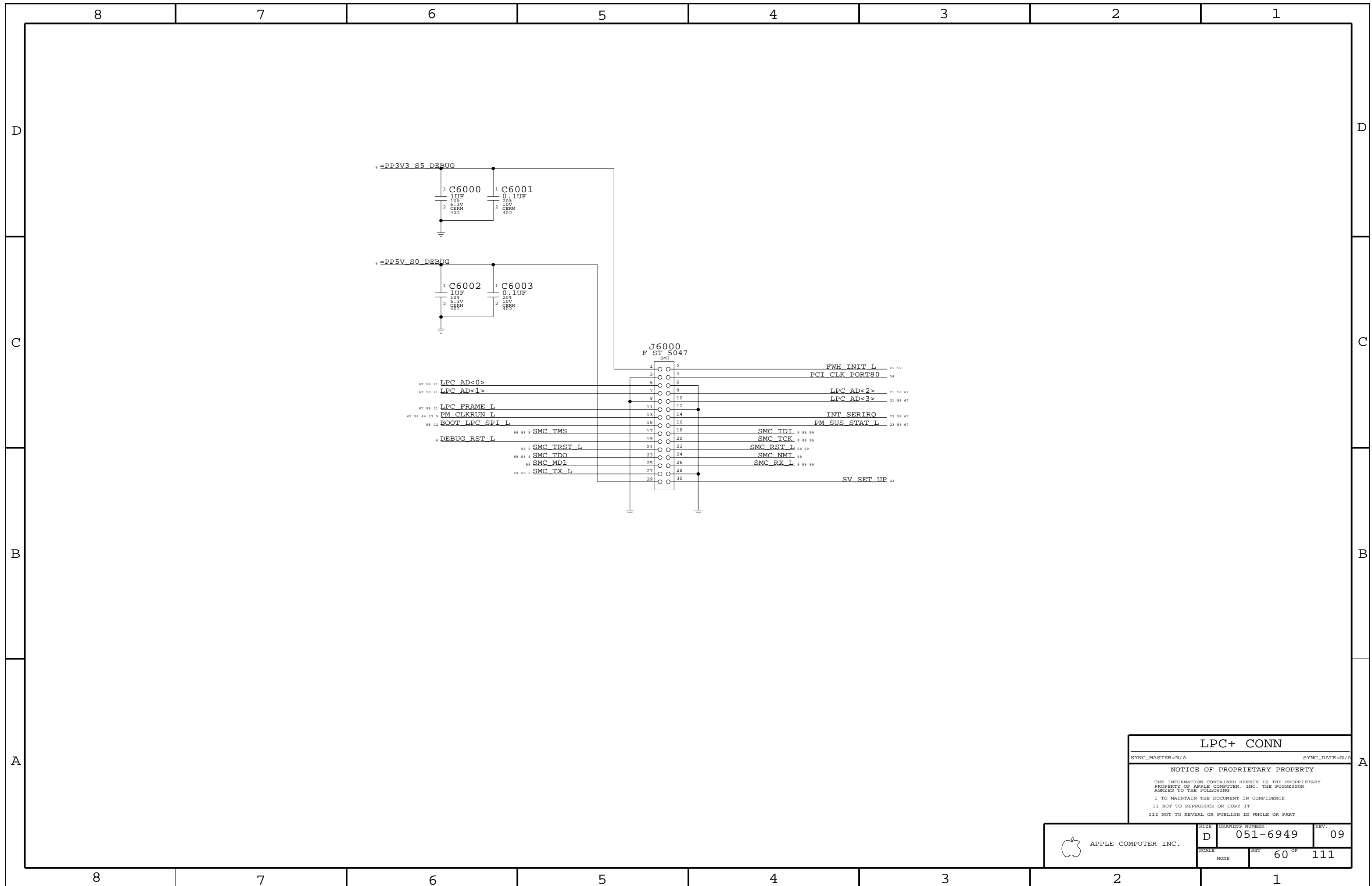
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SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE	SHEET	OF
NONE	59	111

APPLE COMPUTER INC.



LPC+ CONN

SYNC_MASTER=N/A SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

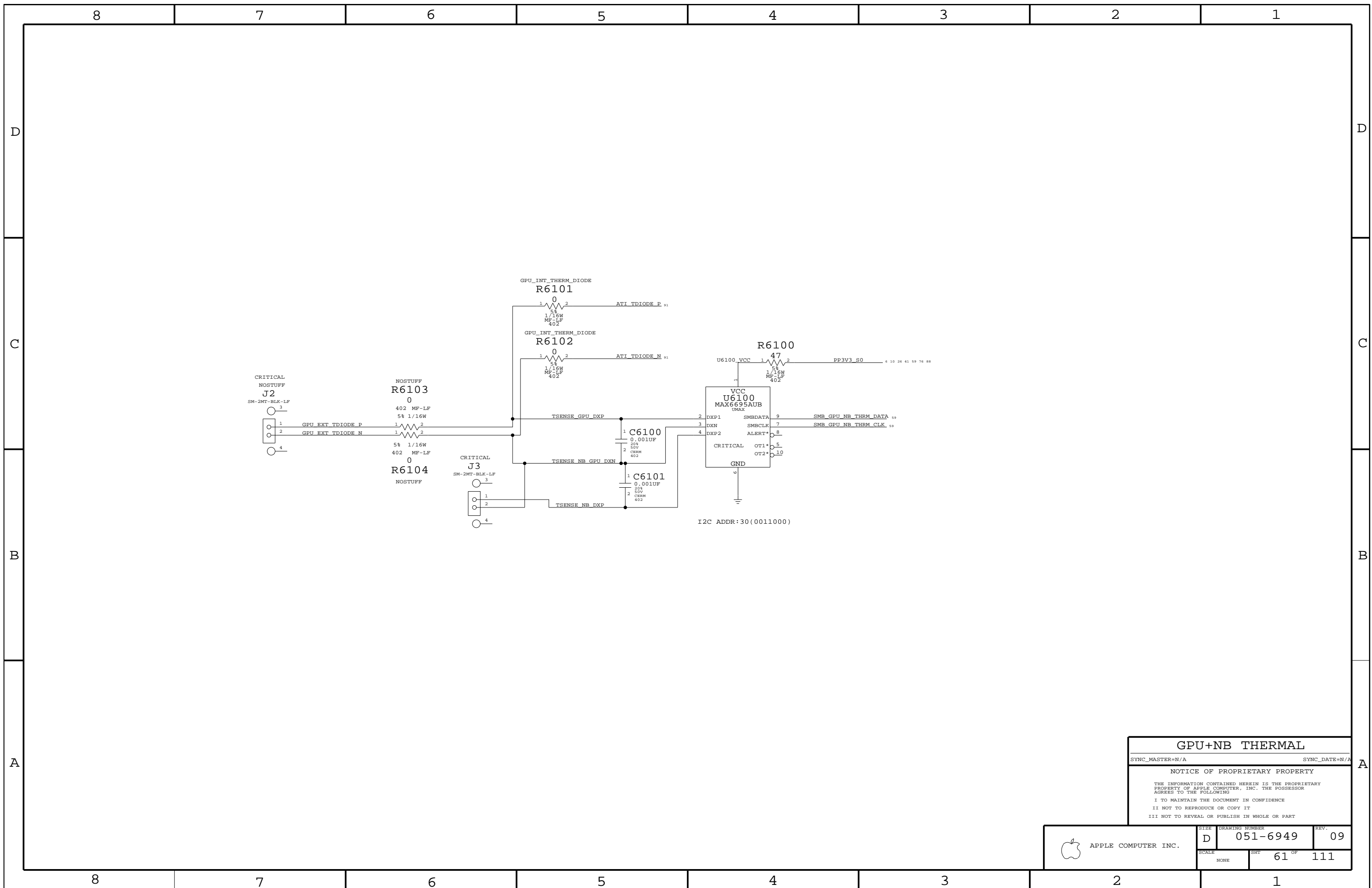
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6949	REV. 09
	SCALE NONE	SHEET 60 OF 111	



GPU+NB THERMAL

SYNC_MASTER=N/A SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

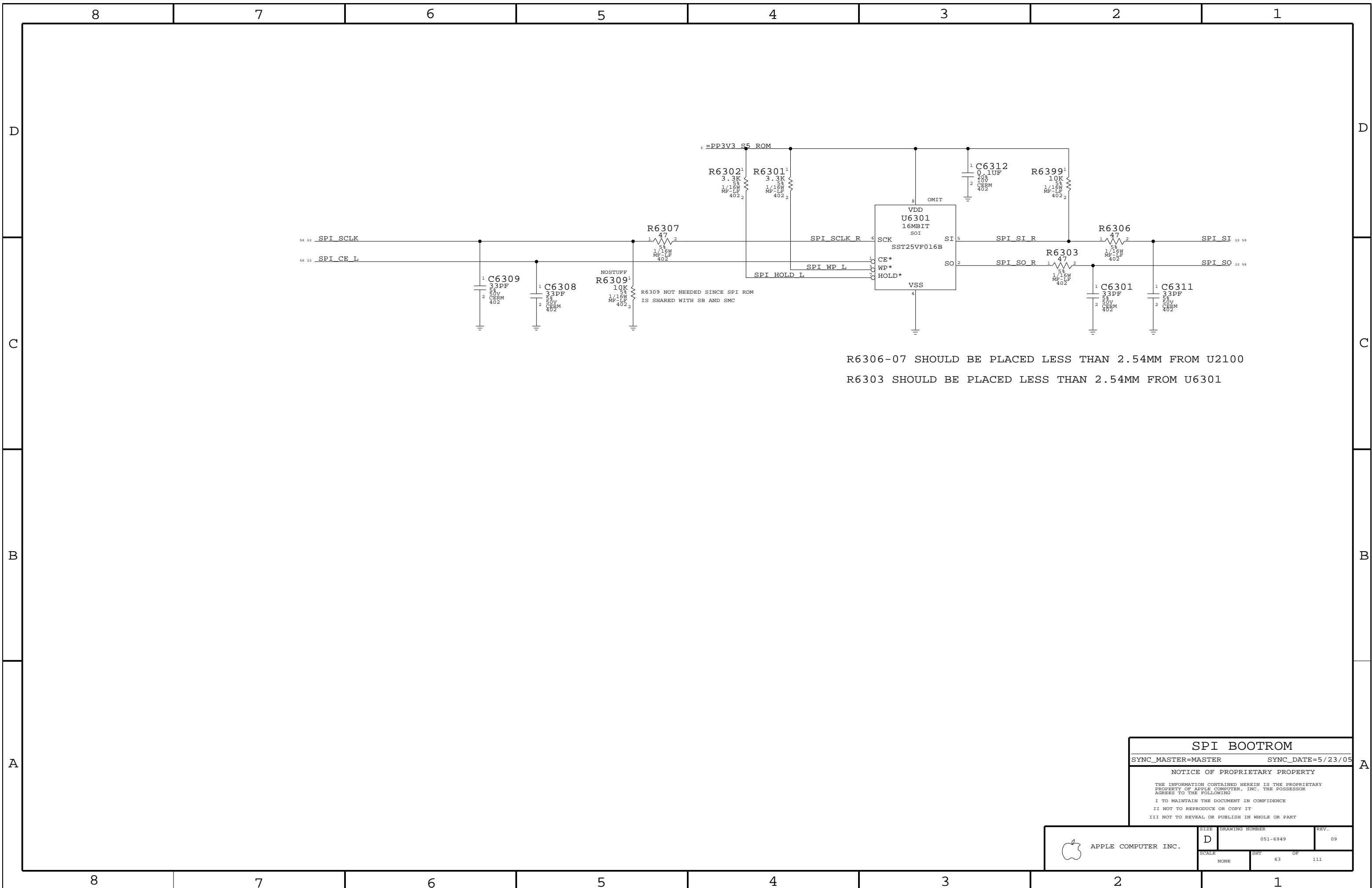
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	D	051-6949	09
SCALE		SHT	OF
NONE		61	111



R6306-07 SHOULD BE PLACED LESS THAN 2.54MM FROM U2100
 R6303 SHOULD BE PLACED LESS THAN 2.54MM FROM U6301

SPI BOOTROM
 SYNC_MASTER=MASTER SYNC_DATE=5/23/05

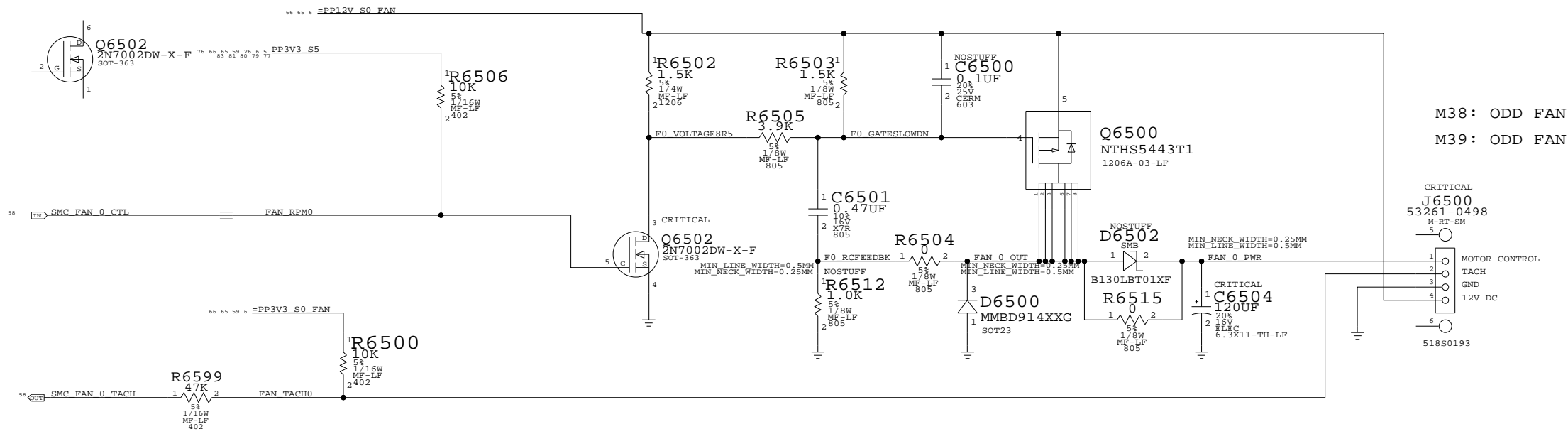
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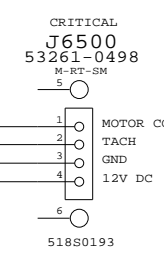
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6949	REV. 09
	SCALE NONE	SHEET 63	OF 111

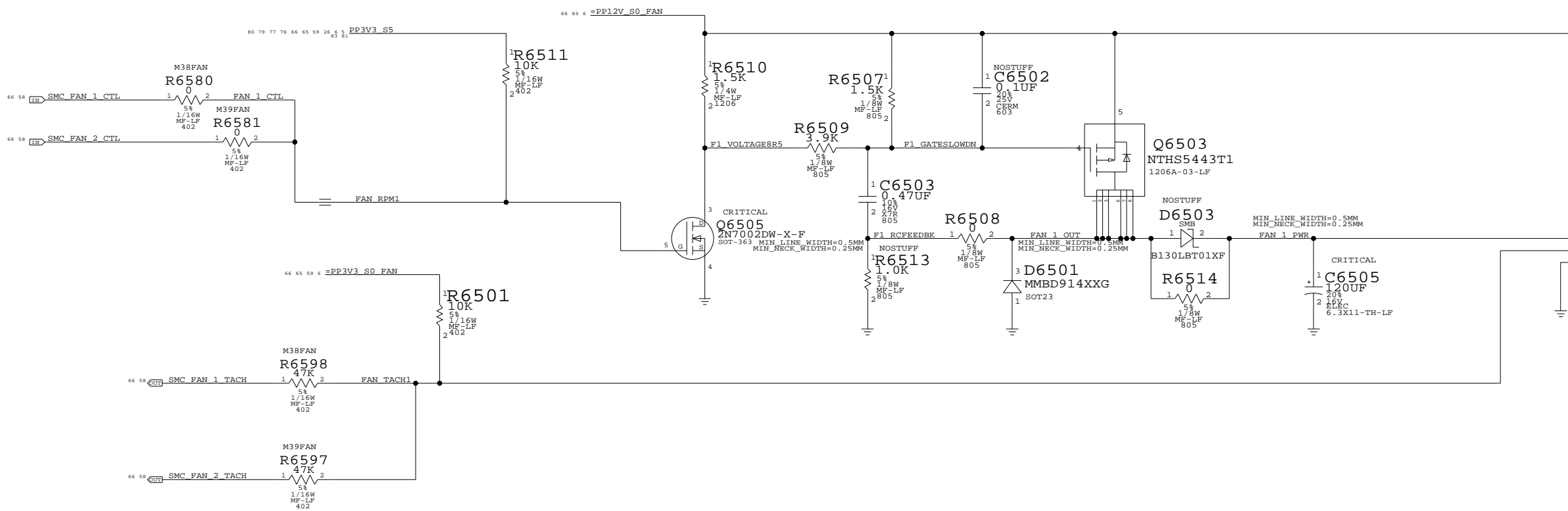
FAN 0



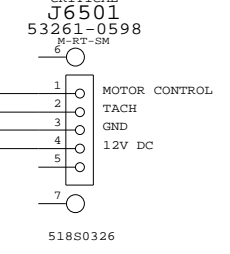
M38: ODD FAN
M39: ODD FAN



FAN 1



M38: HD FAN
M39: CPU FAN



Fan 0, 1 & System Temp

NOTICE OF PROPRIETARY PROPERTY

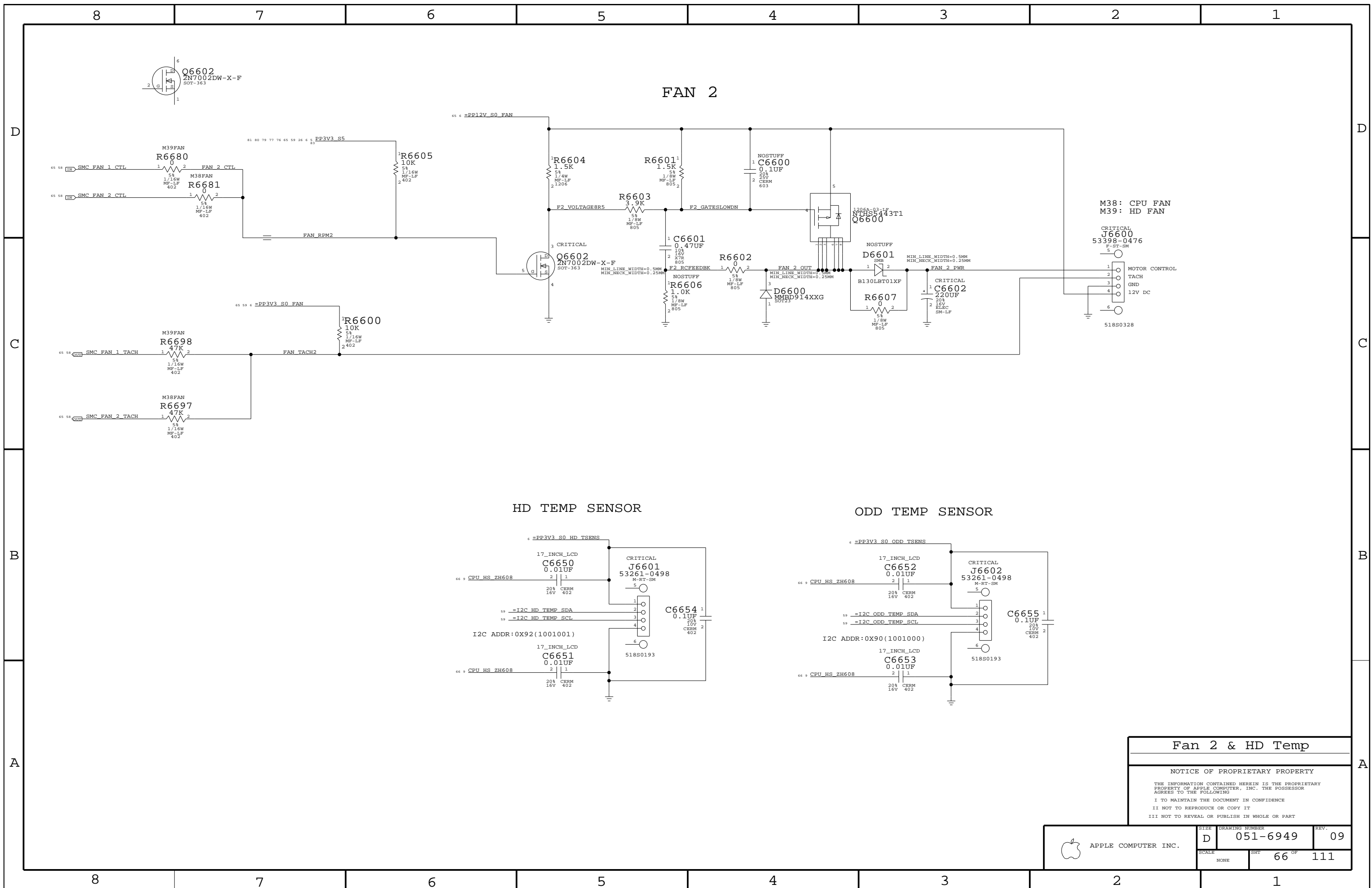
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	NONE	051-6949 09	
SCALE		SHT	OF
NONE		65	111



FAN 2

HD TEMP SENSOR

ODD TEMP SENSOR

Fan 2 & HD Temp

NOTICE OF PROPRIETARY PROPERTY

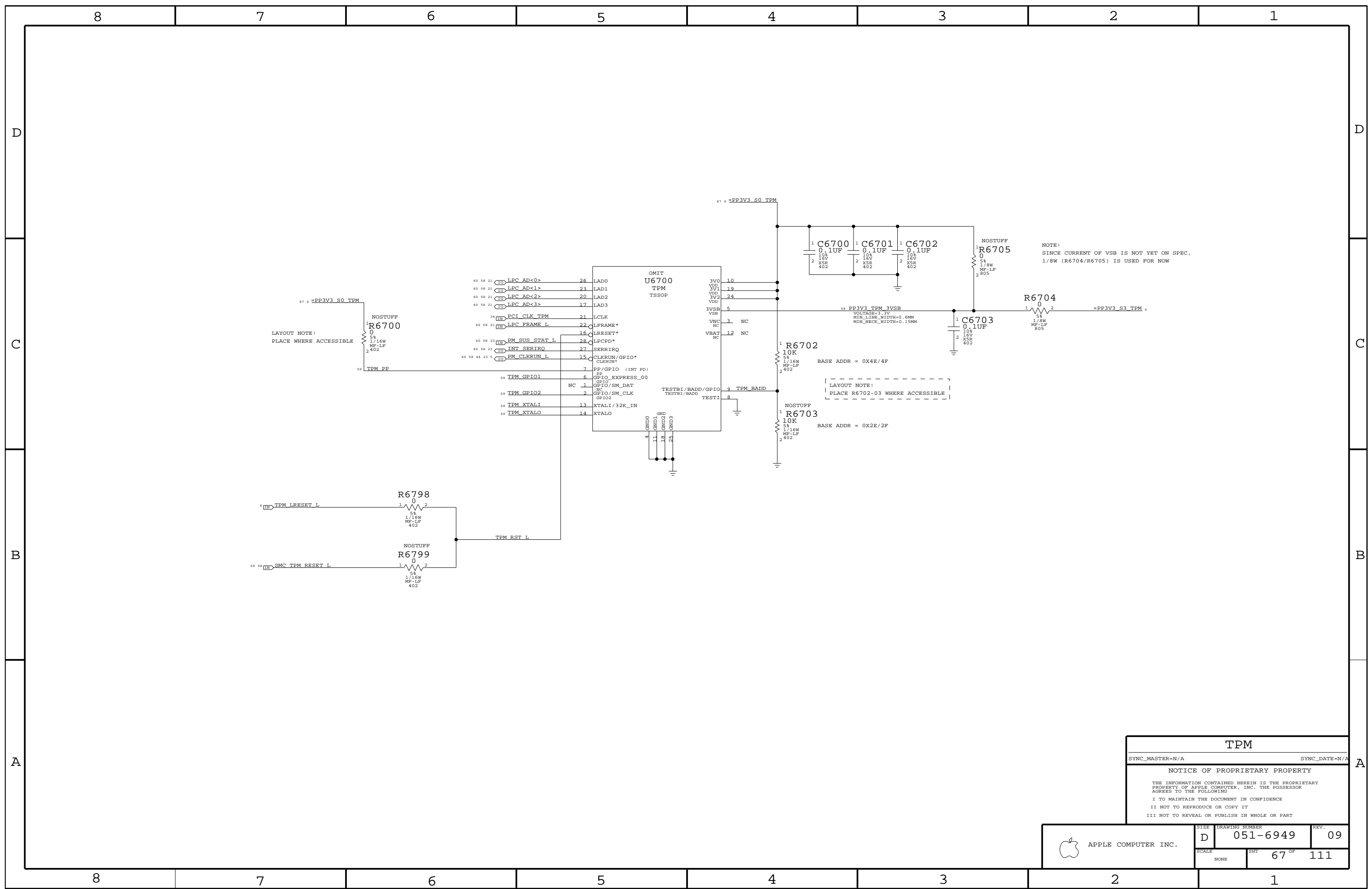
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APPLE COMPUTER INC.	SIZE D SCALE NONE	DRAWING NUMBER 051-6949	REV. 09
	SHEET 66 OF 111		



LAYOUT NOTE:
PLACE WHERE ACCESSIBLE

LAYOUT NOTE:
PLACE R6702-03 WHERE ACCESSIBLE

NOTE:
SINCE CURRENT OF VSB IS NOT YET ON SPEC,
1/8W (R6704/R6705) IS USED FOR NOW

TPM

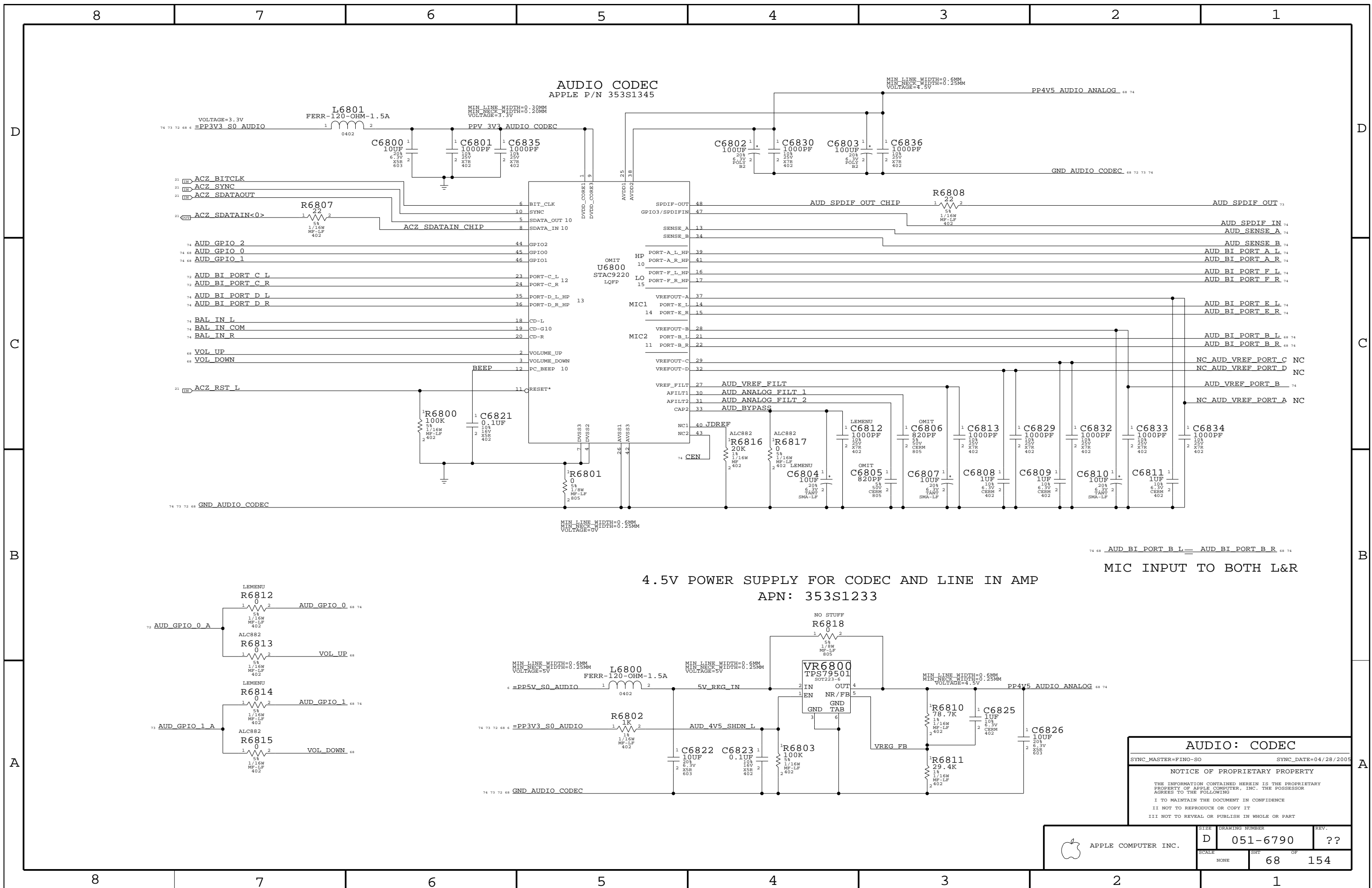
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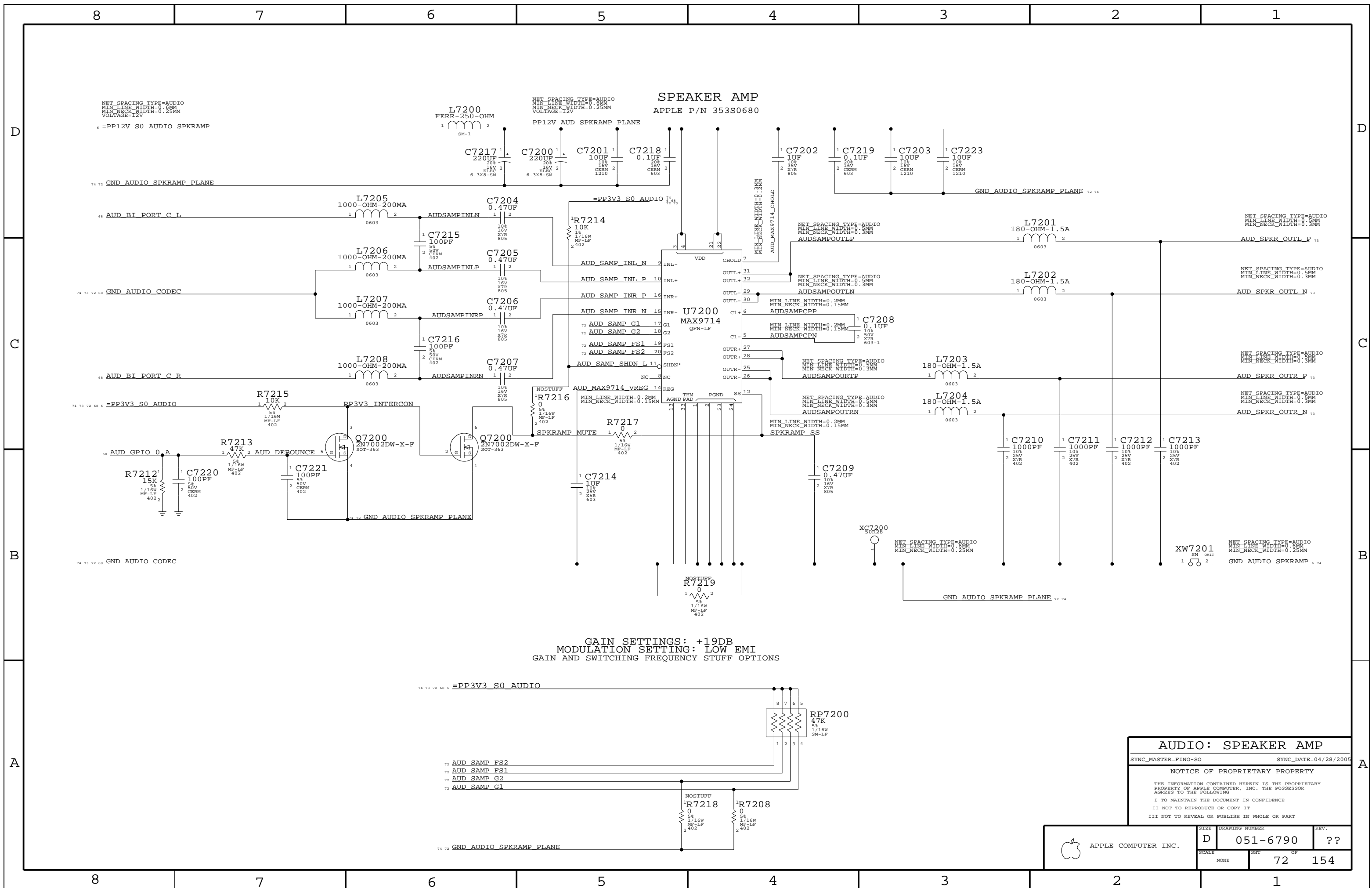
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6949	09
SCALE	SHT	67 OF	111
NONE			



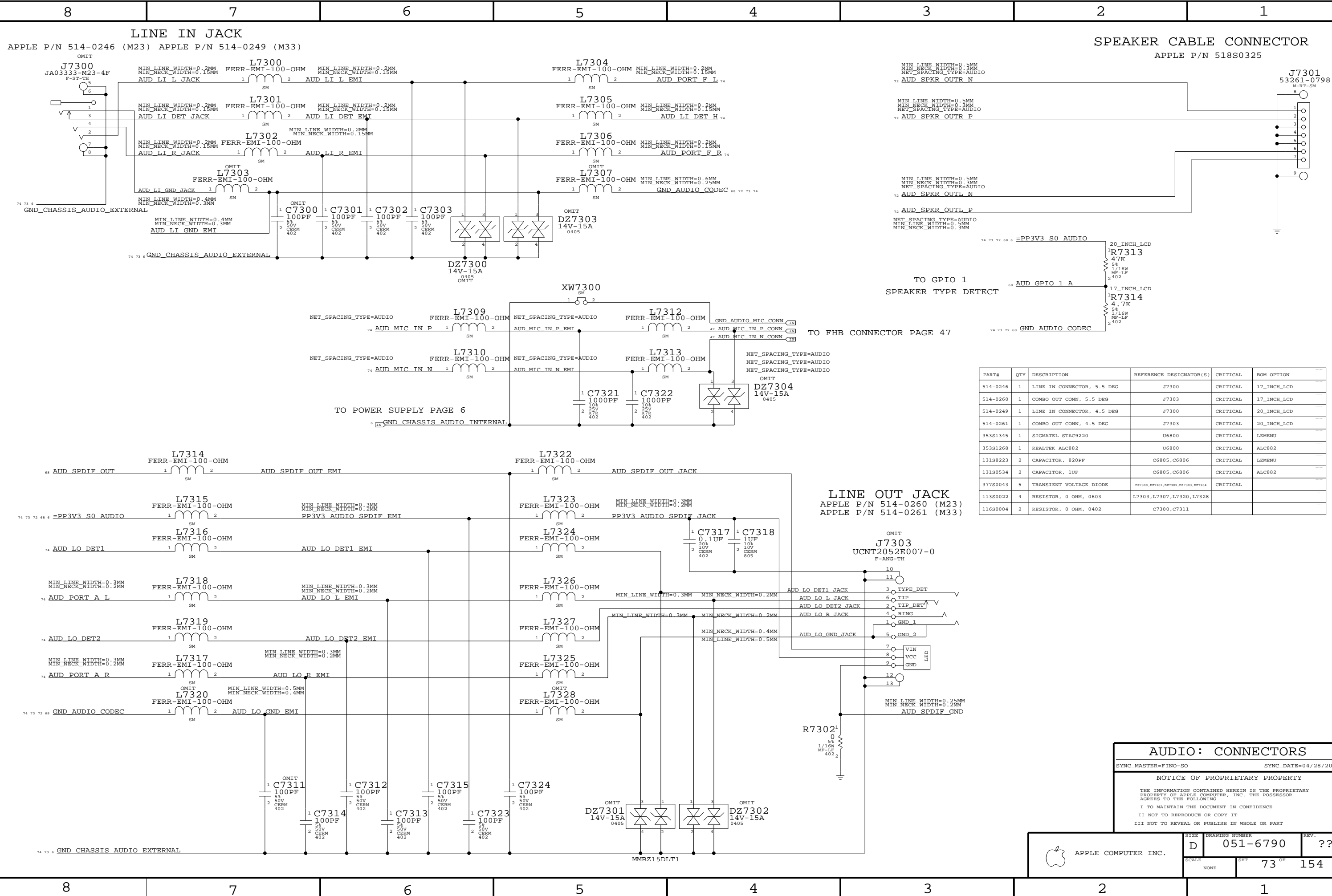


SPEAKER AMP
APPLE P/N 353S0680

GAIN SETTINGS: +19DB
MODULATION SETTING: LOW EMI
GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

AUDIO: SPEAKER AMP
SYNC_MASTER=FINO-SO SYNC_DATE=04/28/2005
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	??
SCALE	NONE	SHT	OF
		72	154



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0246	1	LINE IN CONNECTOR, 5.5 DEG	J7300	CRITICAL	17_INCH_LCD
514-0260	1	COMBO OUT CONN, 5.5 DEG	J7303	CRITICAL	17_INCH_LCD
514-0249	1	LINE IN CONNECTOR, 4.5 DEG	J7300	CRITICAL	20_INCH_LCD
514-0261	1	COMBO OUT CONN, 4.5 DEG	J7303	CRITICAL	20_INCH_LCD
353S1345	1	SIGMATEL STAC9220	U6800	CRITICAL	LEMENU
353S1268	1	REALTEK ALC882	U6800	CRITICAL	ALC882
131S8223	2	CAPACITOR, 820PF	C6805,C6806	CRITICAL	LEMENU
131S0534	2	CAPACITOR, 1UF	C6805,C6806	CRITICAL	ALC882
377S0043	5	TRANSIENT VOLTAGE DIODE	DZ7300,DZ7301,DZ7302,DZ7303,DZ7304	CRITICAL	
113S0022	4	RESISTOR, 0 OHM, 0603	L7303,L7307,L7320,L7328		
116S0004	2	RESISTOR, 0 OHM, 0402	C7300,C7311		

AUDIO: CONNECTORS

SYNC_MASTER=FINO-SO SYNC_DATE=04/28/2005

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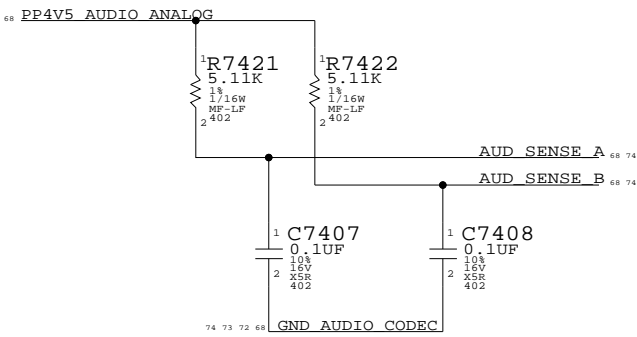
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APPLE COMPUTER INC.	SIZE: D	DRAWING NUMBER: 051-6790	REV.: ??
	SCALE: NONE	SHEET: 73 OF 154	

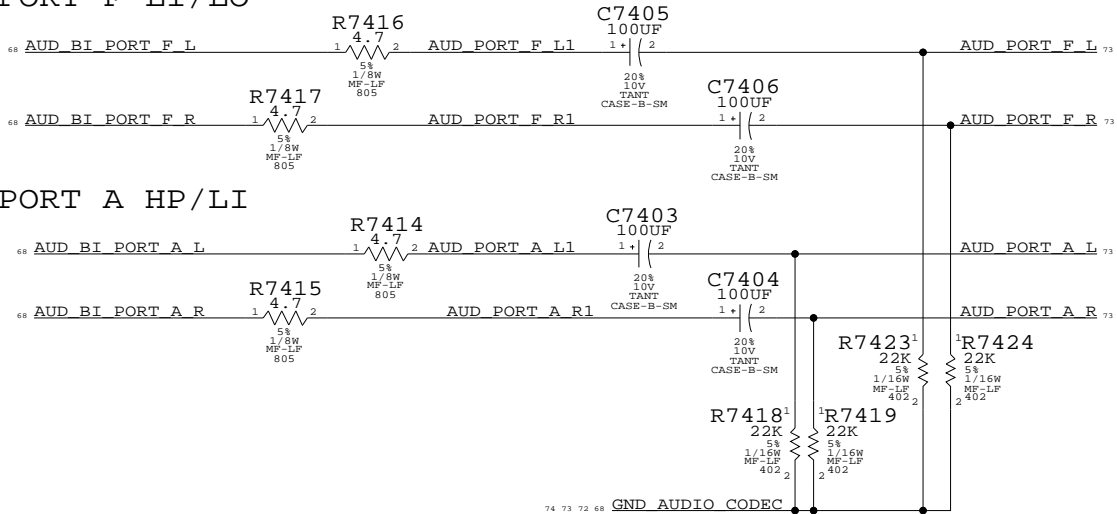
JACK SENSE PULL UPS (PLACE NEXT TO CODEC)



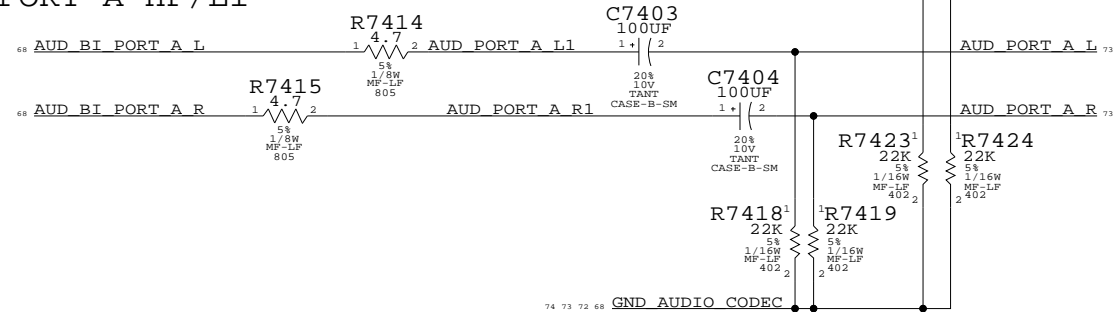
USED PORTS
 PORT A HP/LI
 PORT B MIC IN
 PORT C BI SPEAKERS
 PORT F LI/LO

UNUSED PORTS
 PORT E
 PORT D

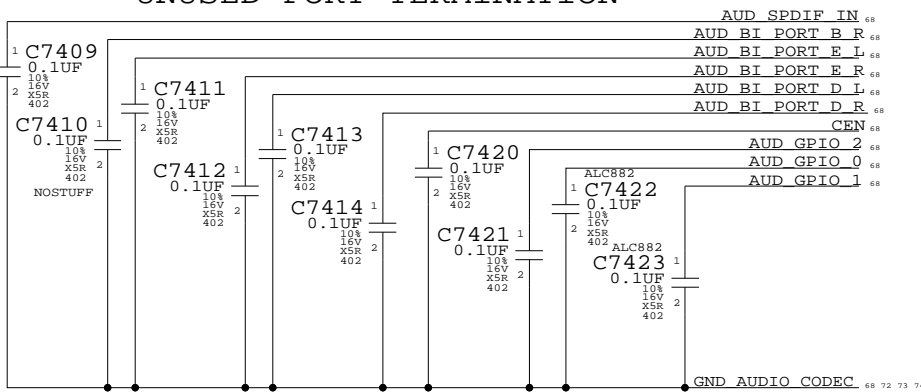
PORT F LI/LO



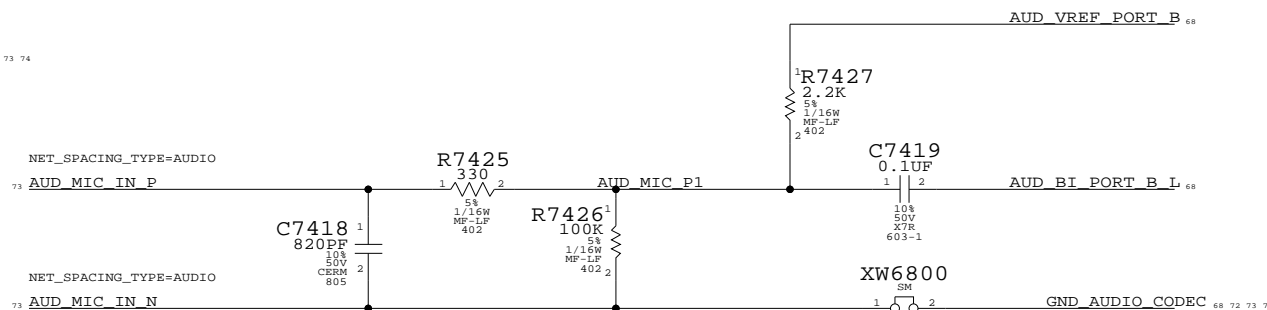
PORT A HP/LI



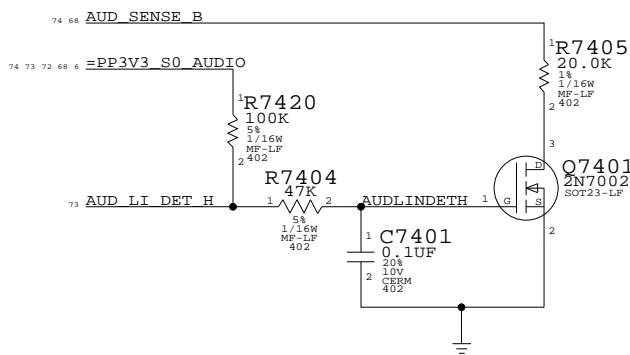
UNUSED PORT TERMINATION



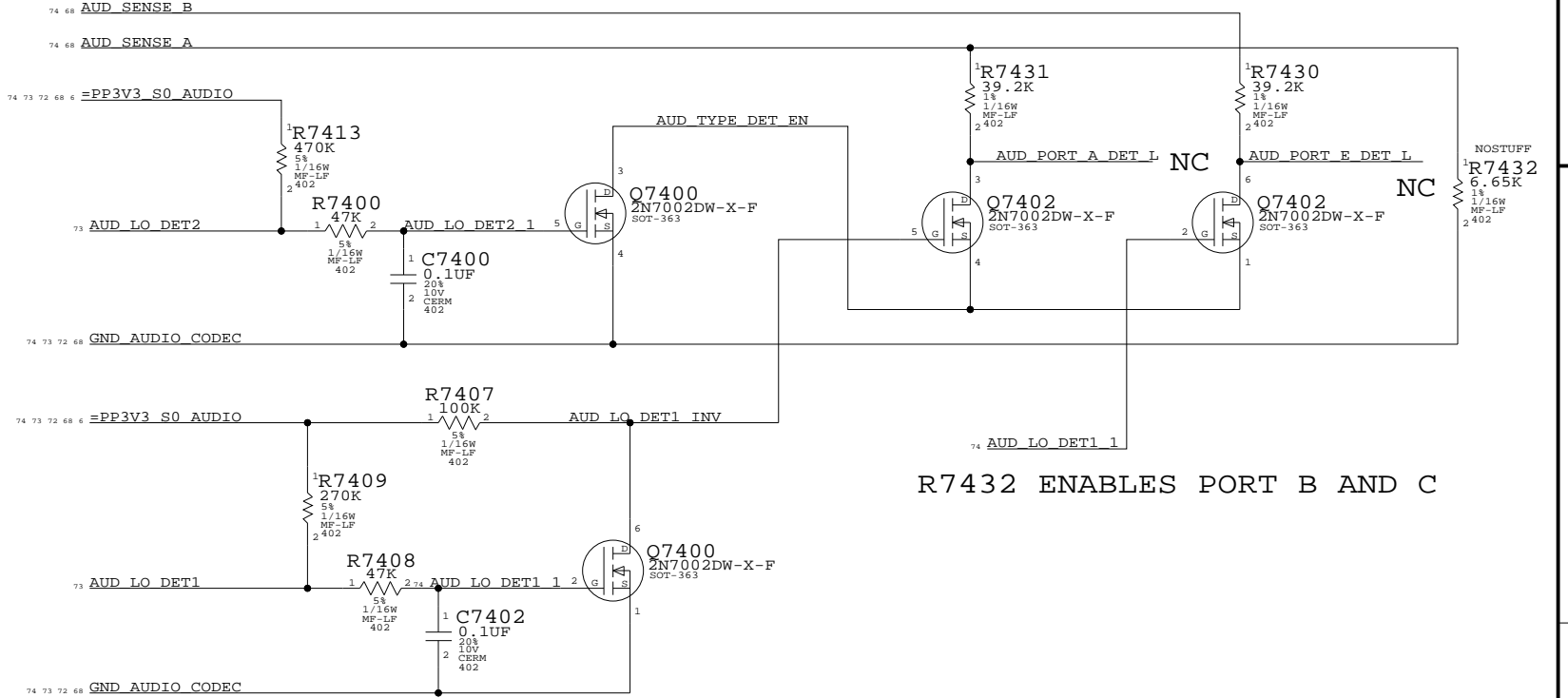
MICROPHONE IMPEDANCE MATCHING CIRCUIT



PORT F (LI/LO) PLUG DETECT

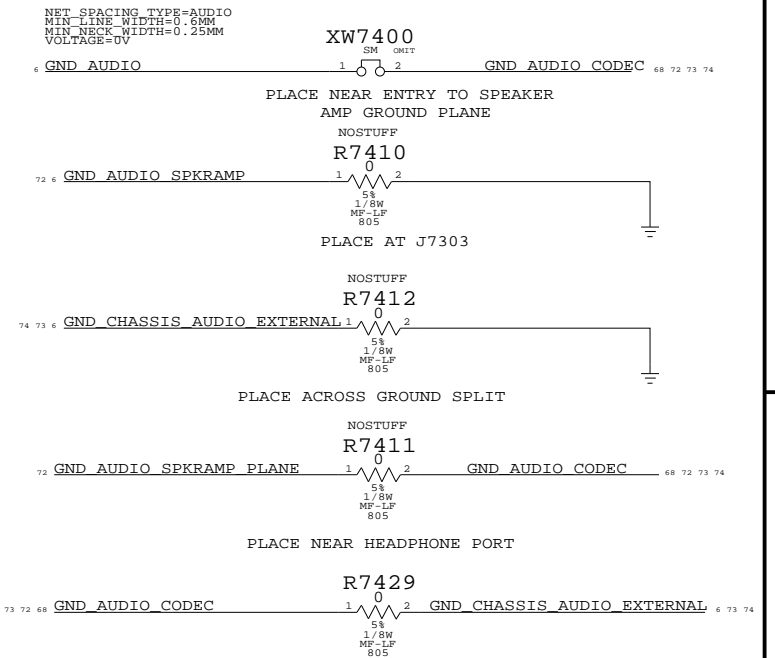


PORT A/H (HP/LI/DIG_OUT) PLUG DETECT (E TELLS H TO COME ON)



R7432 ENABLES PORT B AND C

AUDIO GROUND RETURNS



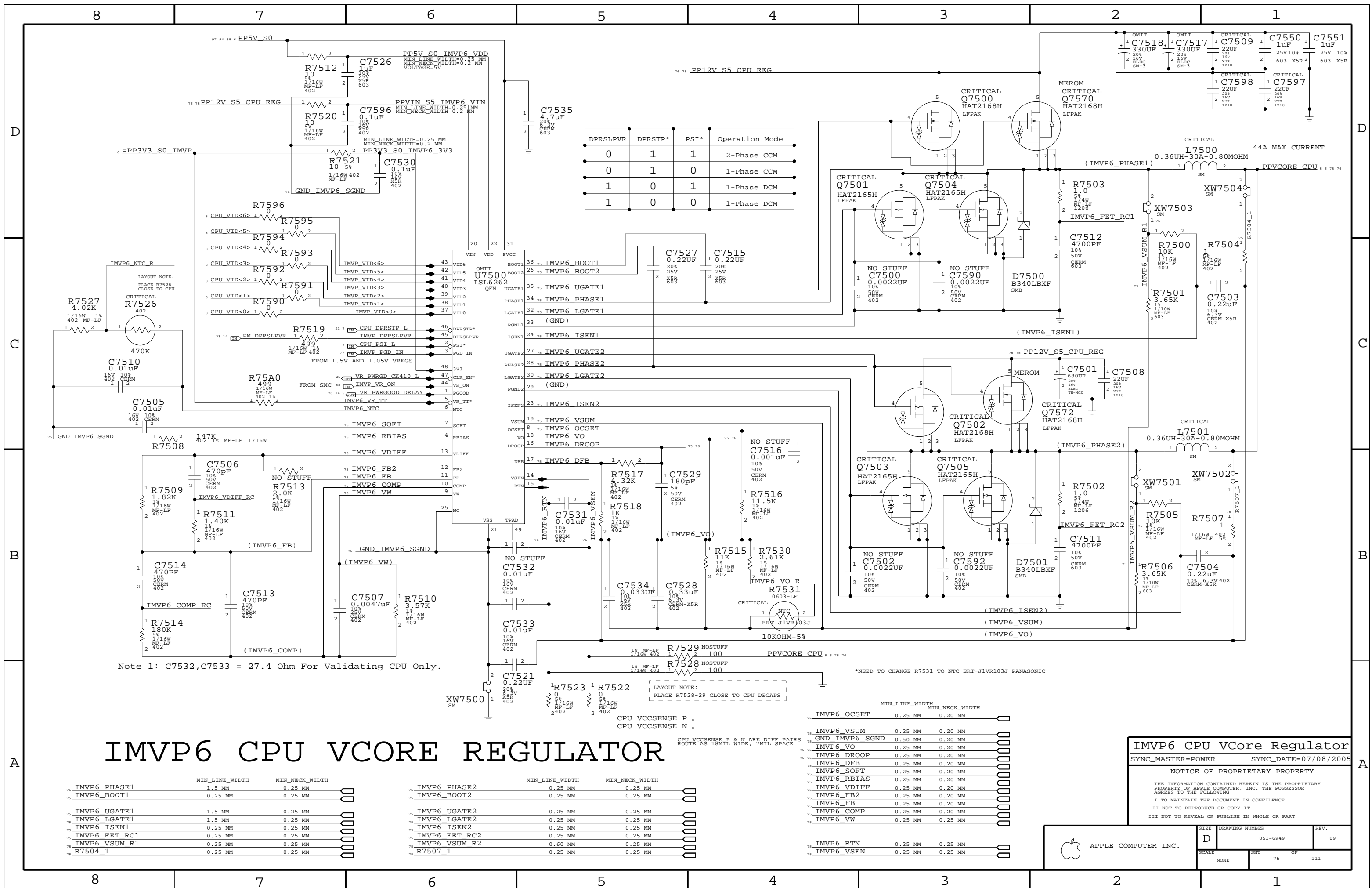
AUDIO: POWER SUPPLIES

SYNC_MASTER=FINO-SO SYNC_DATE=04/28/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	??
SCALE	NONE	SHT	OF
		74	154



DPRSLPVR	DPRSTP*	PSI*	Operation Mode
0	1	1	2-Phase CCM
0	1	0	1-Phase CCM
1	0	1	1-Phase DCM
1	0	0	1-Phase DCM

Pin	Signal	Notes
36	IMVP6_BOOT1	
26	IMVP6_BOOT2	
35	IMVP6_UGATE1	
34	IMVP6_PHASE1	
32	IMVP6_LGATE1	
33	(GND)	
24	IMVP6_ISEN1	
27	IMVP6_UGATE2	
28	IMVP6_PHASE2	
30	IMVP6_LGATE2	
29	(GND)	
23	IMVP6_ISEN2	
19	IMVP6_VSUM	
8	IMVP6_OCSET	
18	IMVP6_VO	
16	IMVP6_DROOP	
17	IMVP6_DFB	
14	IMVP6_VSEN	
15	IMVP6_VSEN	
21	IMVP6_VSEN	
49	IMVP6_VSEN	
75	IMVP6_VSEN	

Note 1: C7532, C7533 = 27.4 Ohm For Validating CPU Only.

*NEED TO CHANGE R7531 TO NTC ERT-J1VR103J PANASONIC

IMVP6 CPU VCore Regulator

Signal	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM
IMVP6_FET_RC1	0.25 MM	0.25 MM
IMVP6_VSUM_R1	0.25 MM	0.25 MM
R7504_1	0.25 MM	0.25 MM

Signal	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM
IMVP6_FET_RC2	0.25 MM	0.25 MM
IMVP6_VSUM_R2	0.60 MM	0.25 MM
R7507_1	0.25 MM	0.25 MM

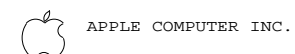
Signal	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
IMVP6_RTIN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

IMVP6 CPU VCore Regulator
 SYNC_MASTER=POWER SYNC_DATE=07/08/2005

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SCALE	DRAWING NUMBER	REV.
NONE	D 051-6949	09
SHEET	75	OF 111

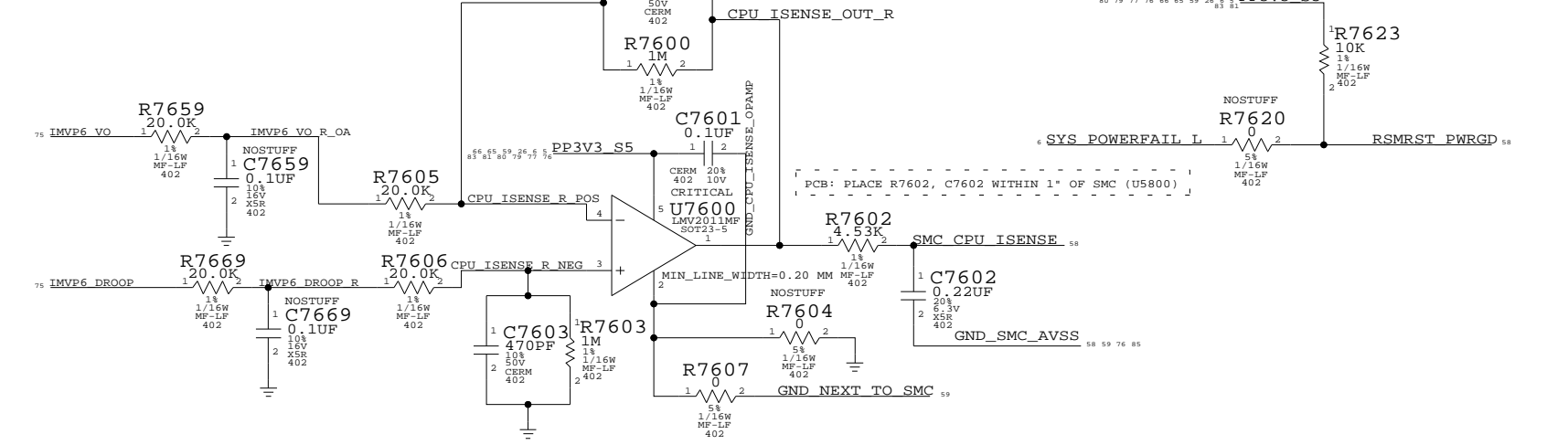
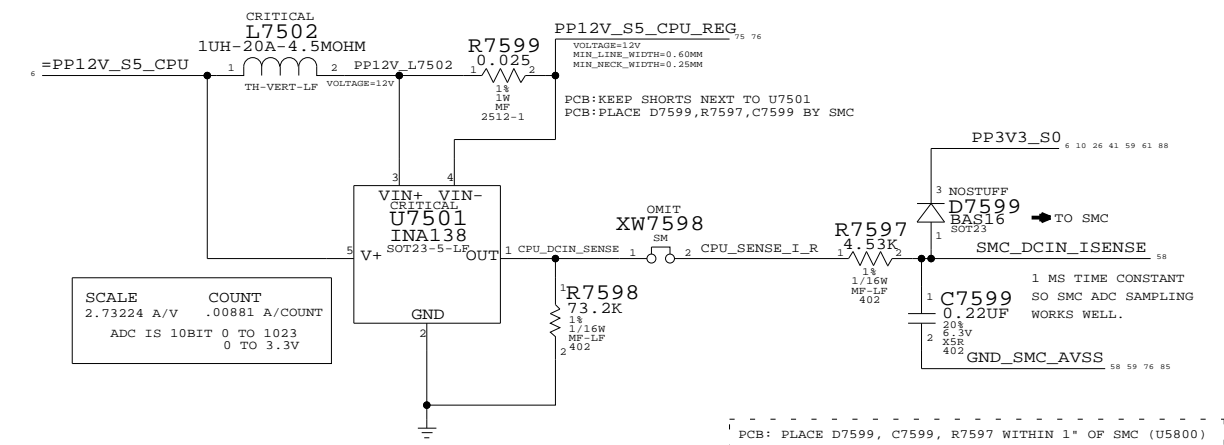


8 7 6 5 4 3 2 1

PROCESSOR VCORE CURRENT SENSE
(USING 12V INPUT CURRENT TO DERIVE CPU CURRENT)

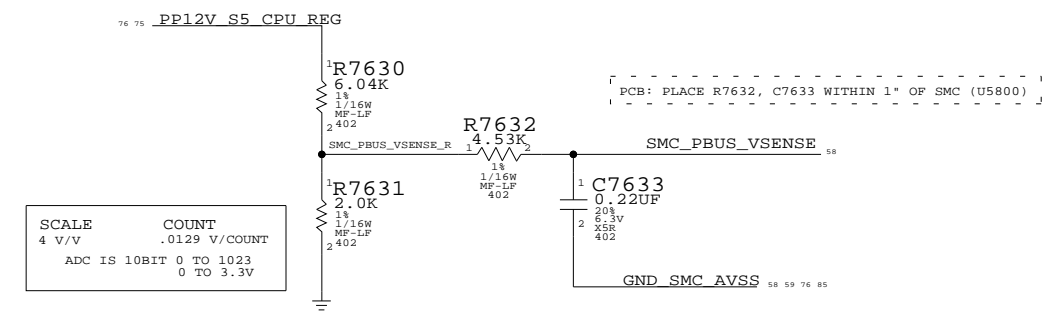
PROCESSOR VCORE CURRENT SENSE
(MEASURING DC/DC INDUCTOR DCR TO DERIVE CPU CURRENT)

SMC PWRGD PULLUP

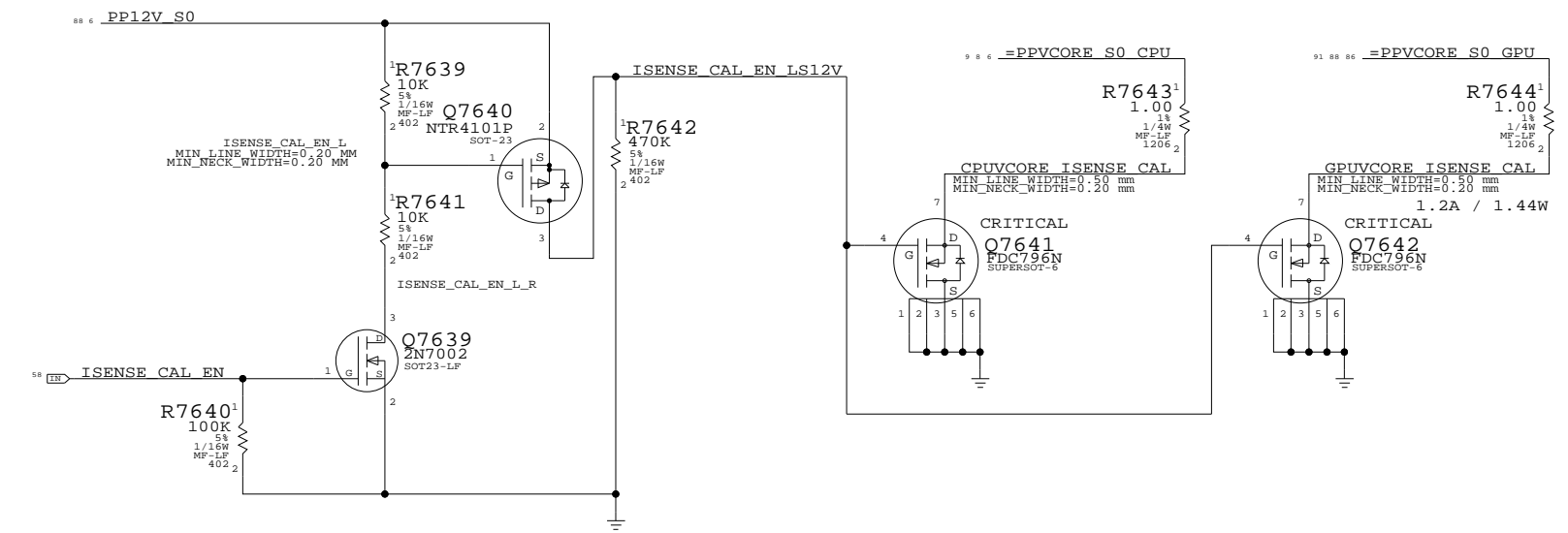


PROCESSOR DCIN VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)

PROCESSOR VCORE SENSE



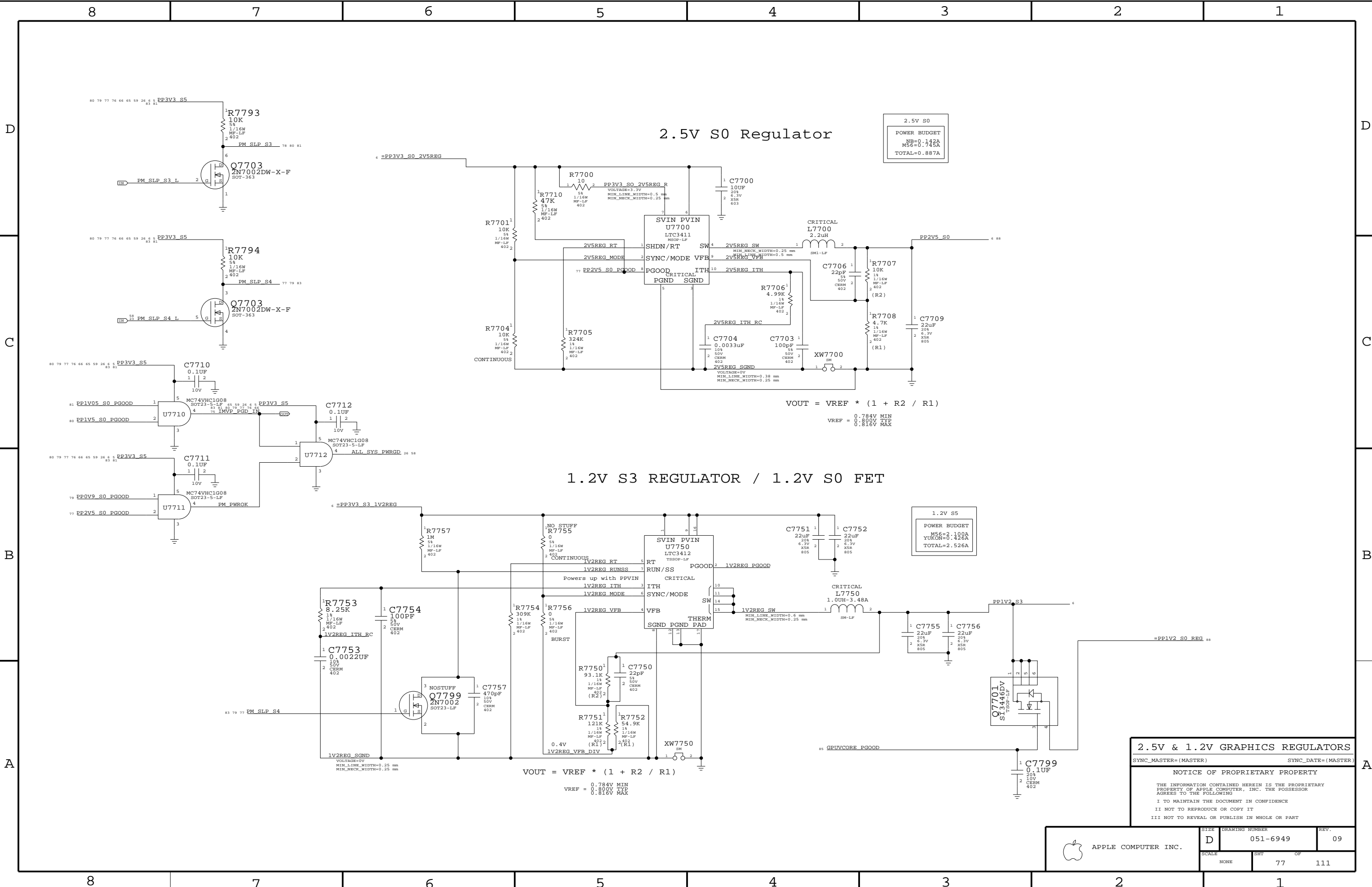
Current Sense Calibration Circuit
Switches in fixed load on power supplies to calibrate current sense circuits



CPU SENSE CIRCUITRIES
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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	D	051-6949	09
SCALE	SHT	76 OF	111
NONE			

8 7 6 5 4 3 2 1



2.5V S0 Regulator

2.5V S0
POWER BUDGET
MSE=1.42A
MBS=0.745A
TOTAL=0.887A

$V_{OUT} = V_{REF} * (1 + R2 / R1)$
 $V_{REF} = 0.784V \text{ MIN}$
 $V_{REF} = 0.800V \text{ TYP}$
 $V_{REF} = 0.816V \text{ MAX}$

1.2V S3 REGULATOR / 1.2V S0 FET

1.2V S5
POWER BUDGET
MSE=1.408A
YUSEN=0.108A
TOTAL=2.526A

$V_{OUT} = V_{REF} * (1 + R2 / R1)$
 $V_{REF} = 0.784V \text{ MIN}$
 $V_{REF} = 0.800V \text{ TYP}$
 $V_{REF} = 0.816V \text{ MAX}$

2.5V & 1.2V GRAPHICS REGULATORS

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

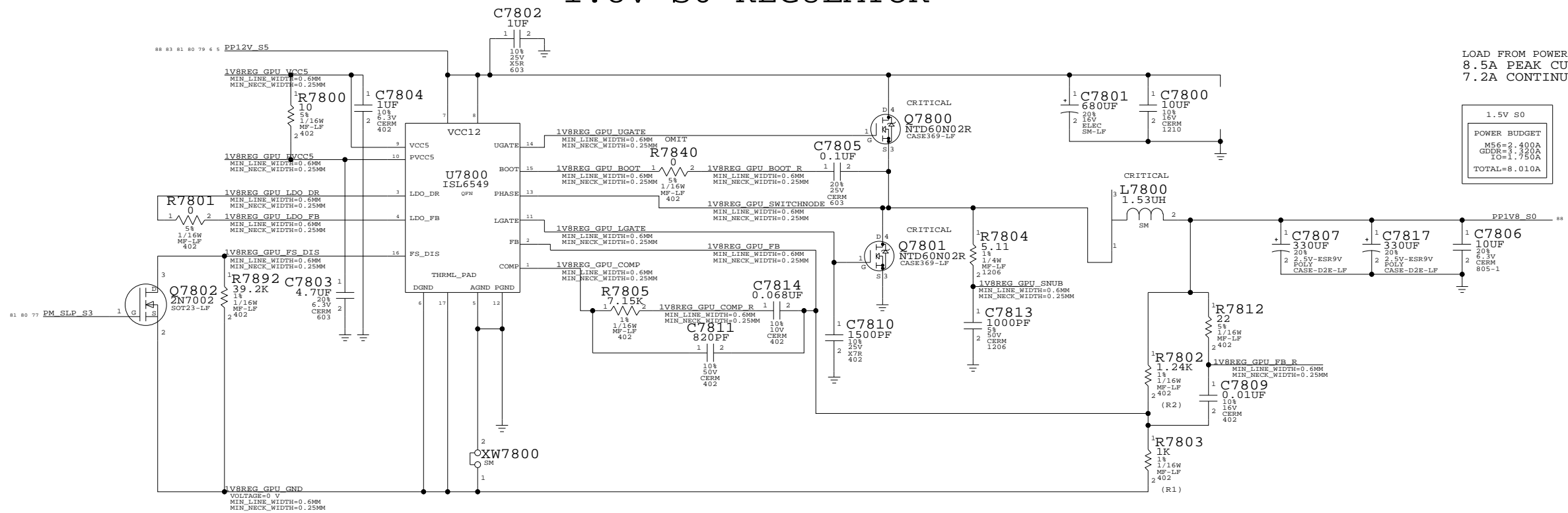
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	D	051-6949	09
SCALE	SHT	OF	
NONE	77	111	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
11480514	1	5.11 OHM 0402 1% 1/16W LF	R7840		

1.8V S0 REGULATOR



LOAD FROM POWER BUDGET
8.5A PEAK CURRENT DRAW
7.2A CONTINUOUS CURRENT DRAW

1.5V S0	
POWER BUDGET	
M56=	2.400A
GDDR=	3.200A
IO=	1.750A
TOTAL=8.010A	

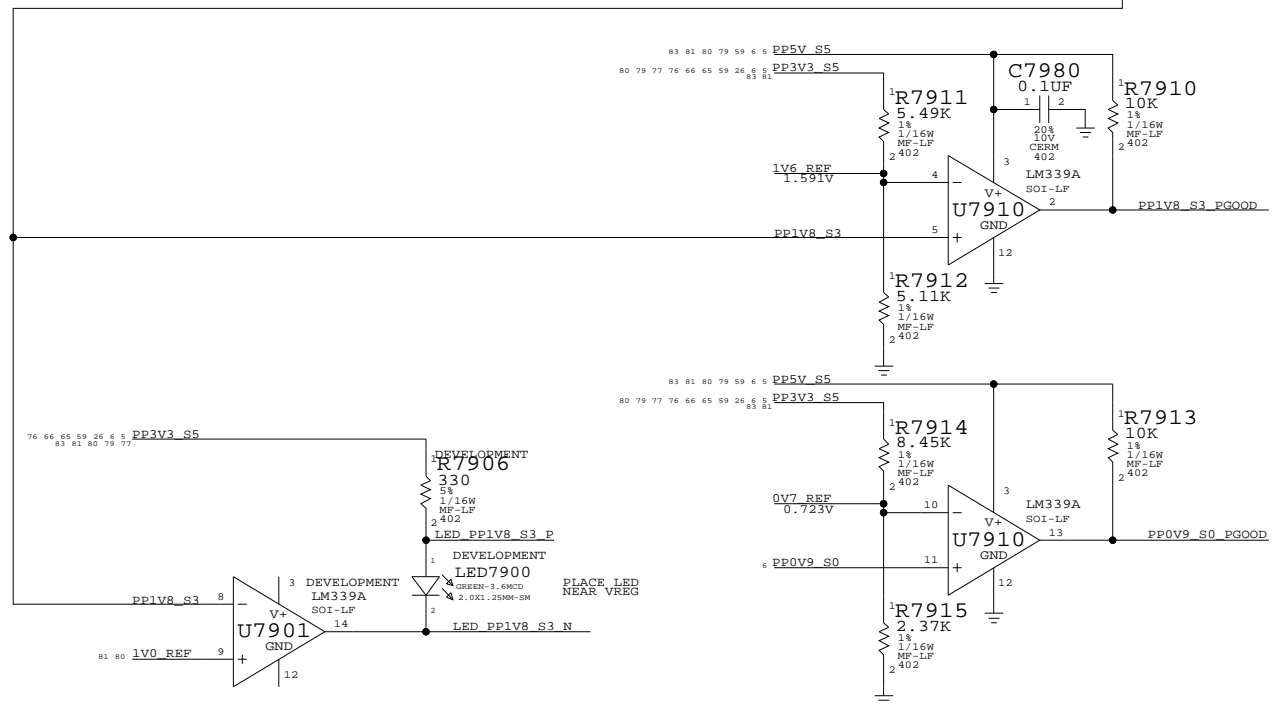
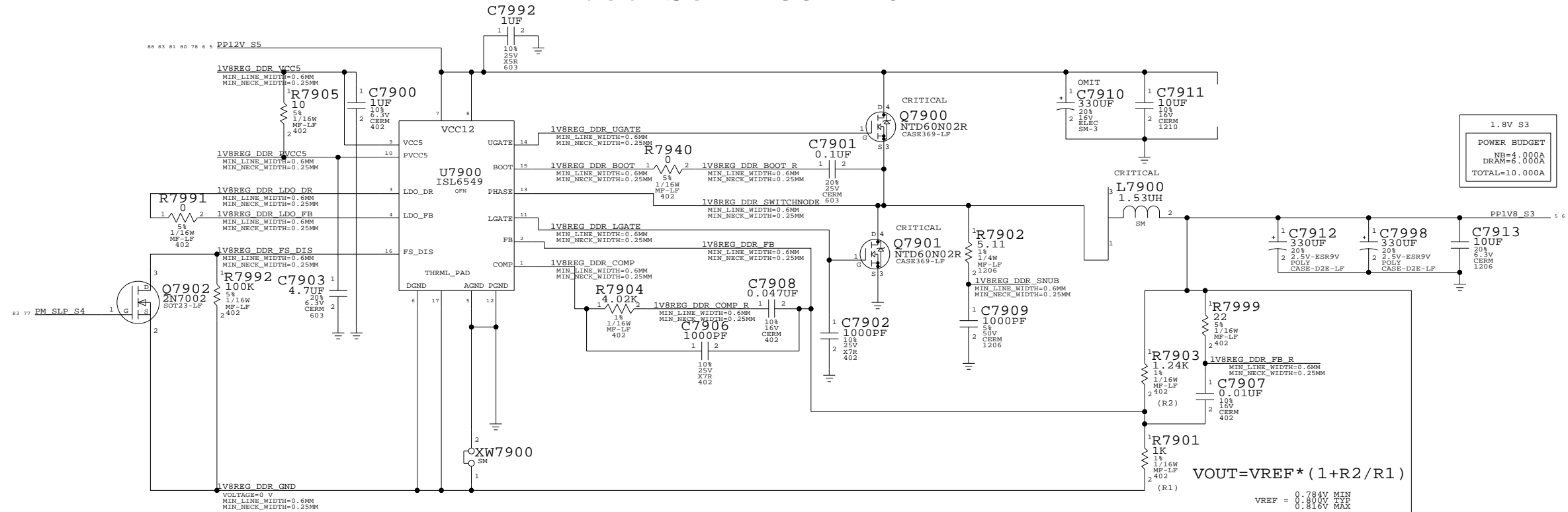
$$V_{OUT} = V_{REF} * (1 + R2/R1)$$

VREF = 0.784V MIN
0.800V TYP
0.816V MAX

1.8V GDDR REGULATOR
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6949	09
SCALE	SHT	78 OF 111	
NONE			

1.8V S3 REGULATOR

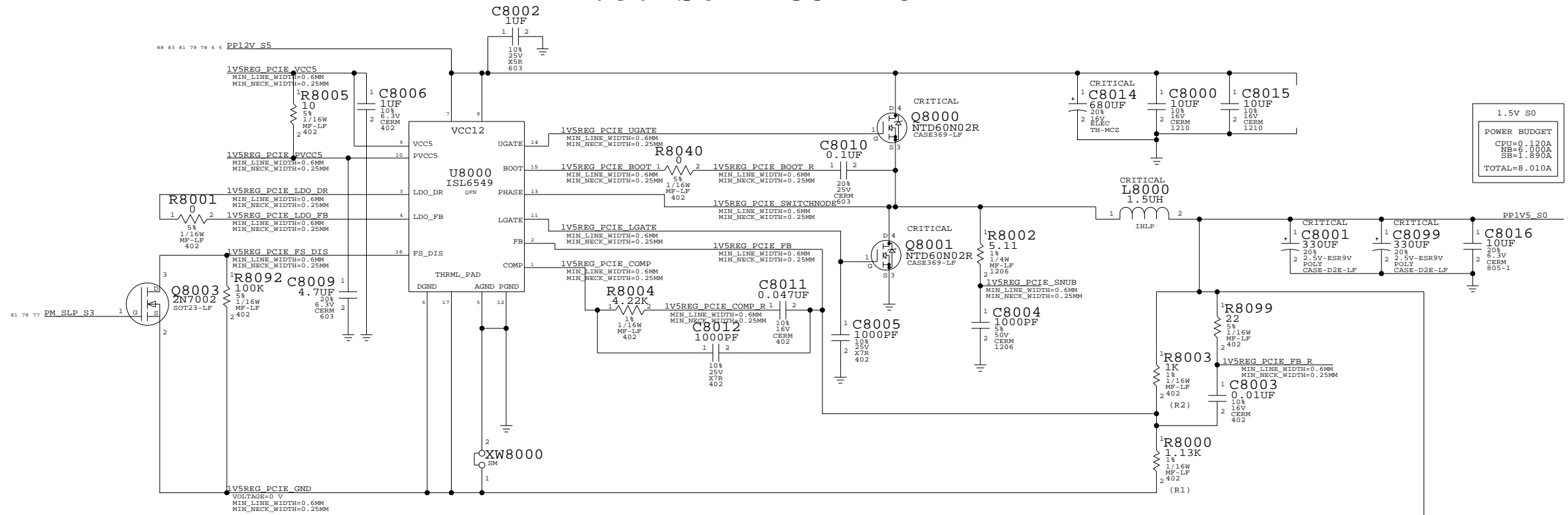


1.8V Vreg
 SYNC_MASTER=M23-PC SYNC_DATE=04/12/2005

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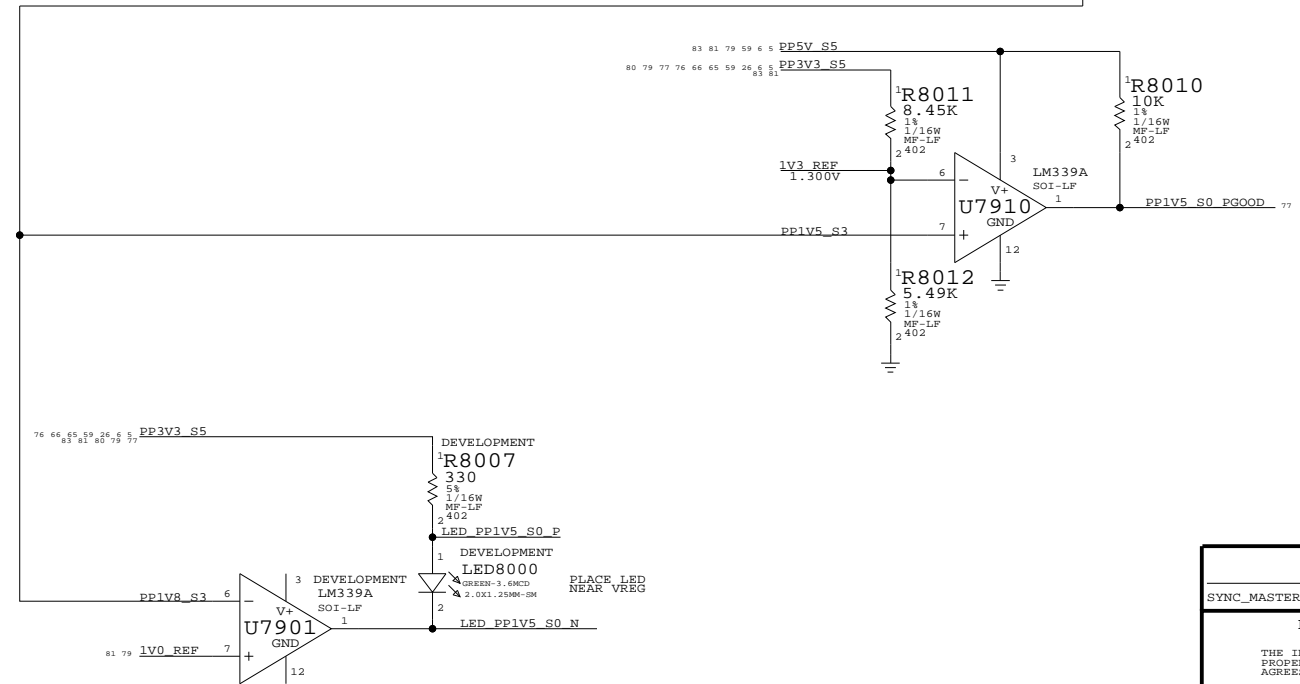
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6949	09
SCALE	SHT	79	OF 111
NONE			

1.5V S0 REGULATOR



$$V_{OUT} = V_{REF} * (1 + R2/R1)$$

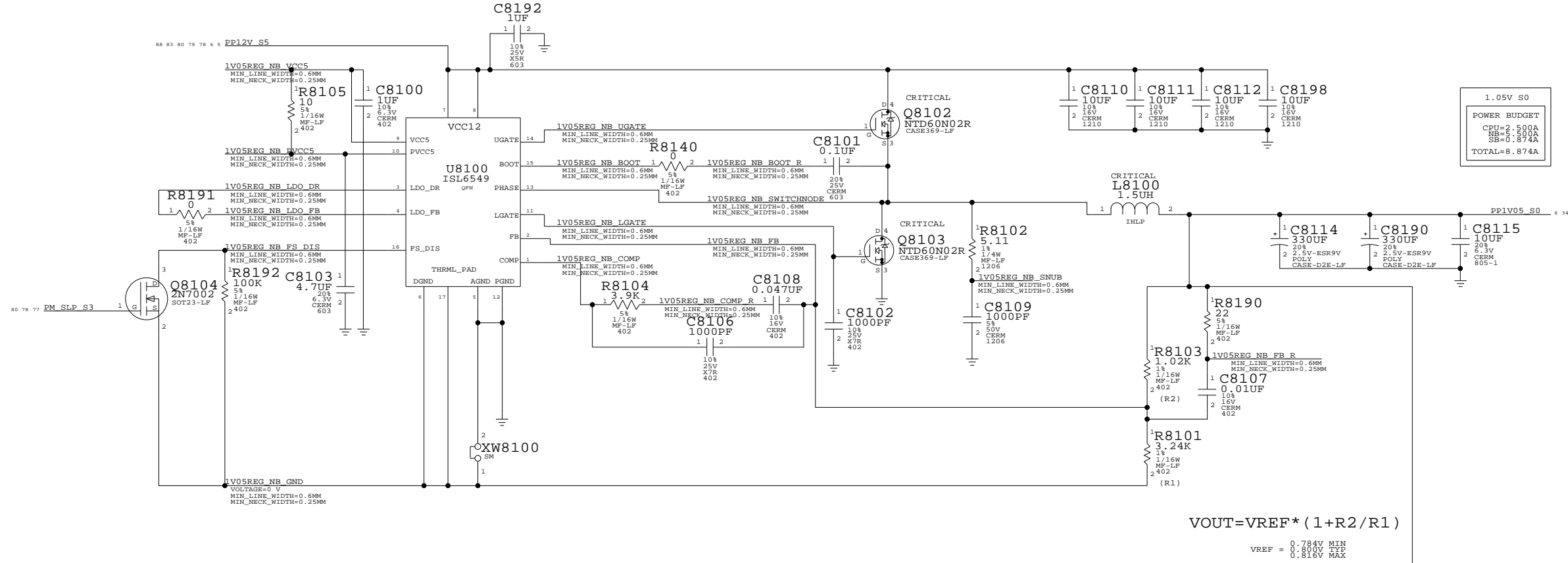
$$V_{REF} = \begin{matrix} 0.784V \text{ MIN} \\ 0.800V \text{ TYP} \\ 0.816V \text{ MAX} \end{matrix}$$



1.5V Vreg
 SYNC_MASTER=FINO-PC SYNC_DATE=05/18/2005
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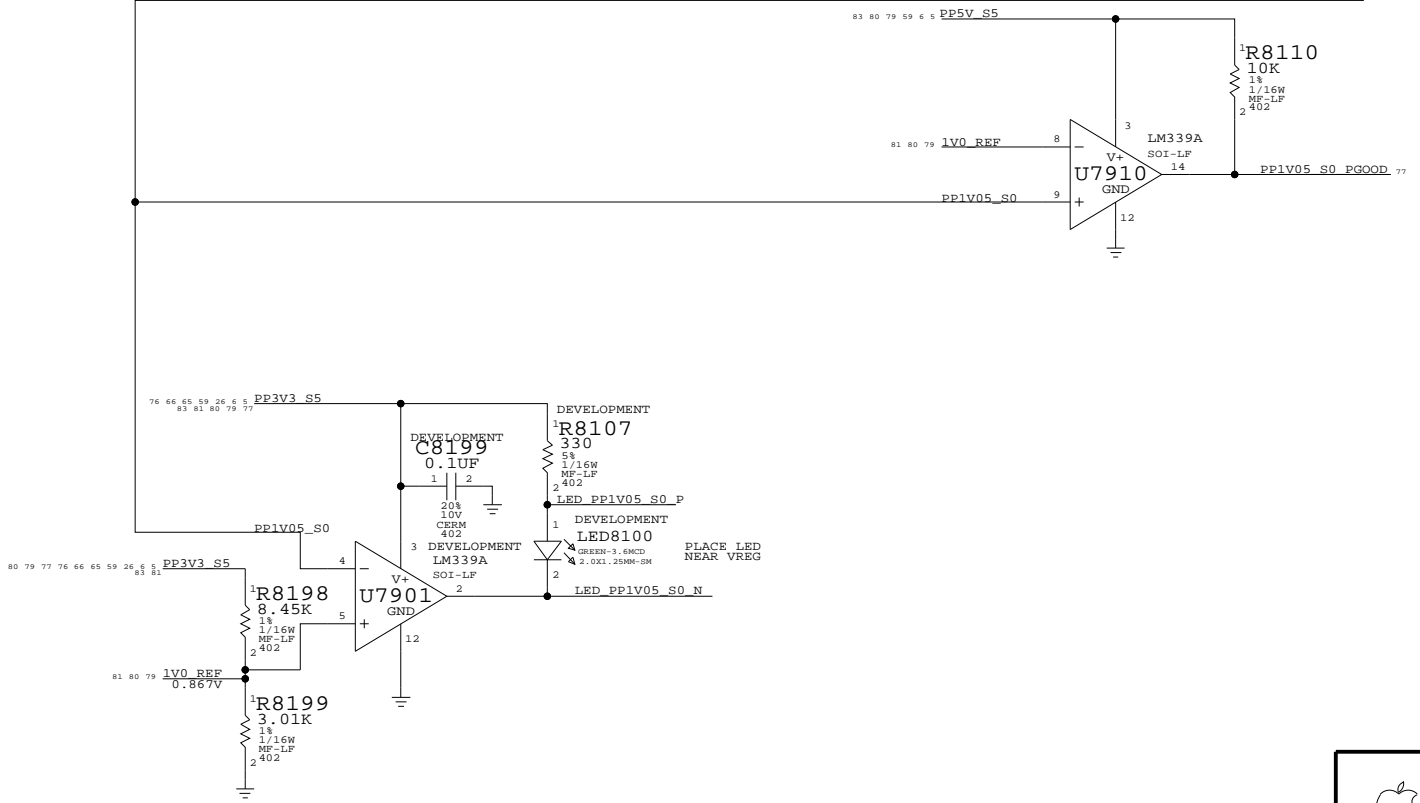
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6950	06
SCALE	SHT	80 OF	111
NONE			

1.05V S0 REGULATOR



$$V_{OUT} = V_{REF} * (1 + R2/R1)$$

VREF = 0.784V MIN
0.800V TYP
0.816V MAX



1.05V VREG

SYNC_MASTER=M38-RT SYNC_DATE=05/18/2005

NOTICE OF PROPRIETARY PROPERTY

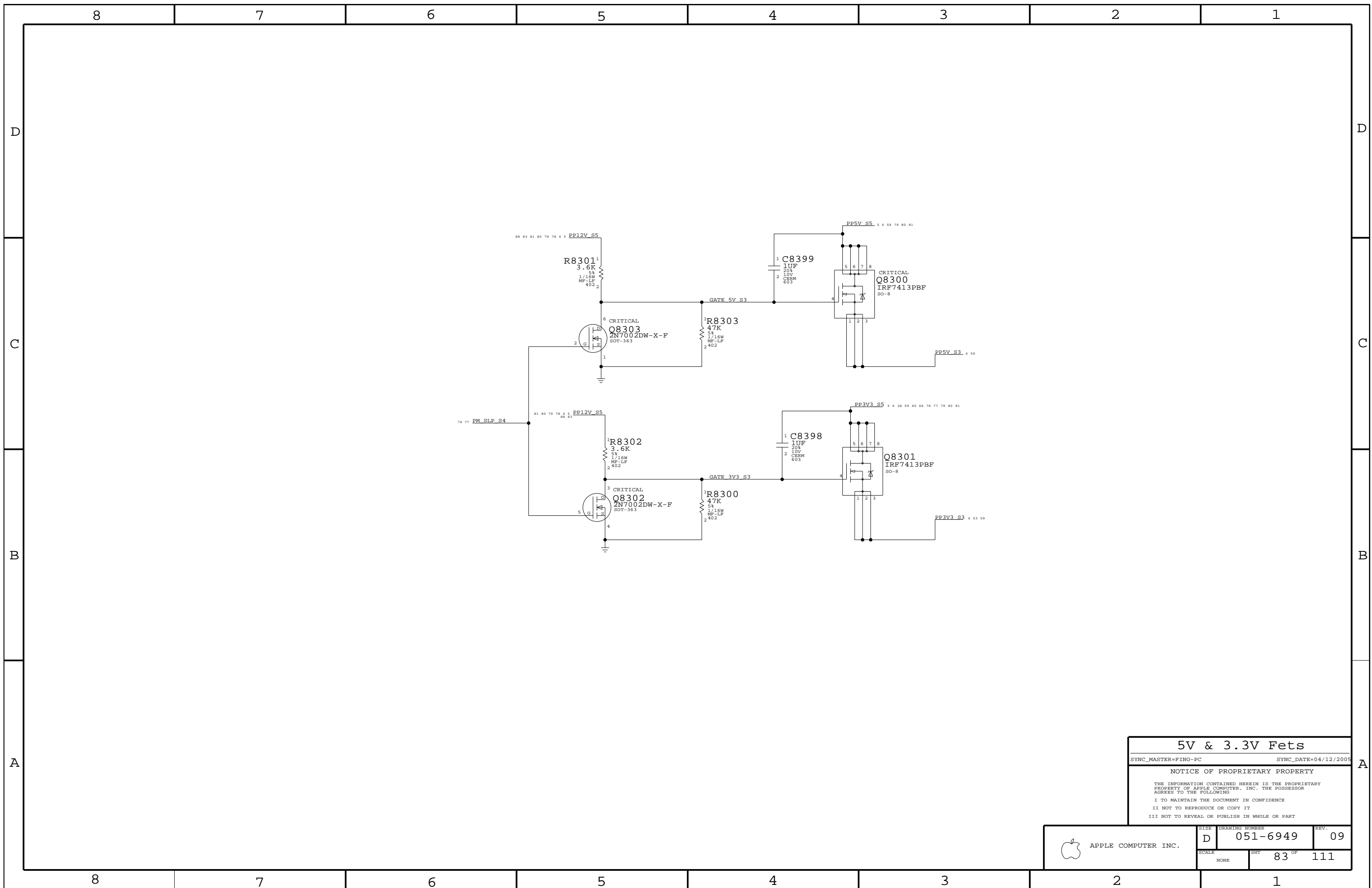
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	D	051-6949	09
SCALE	SHT	81 OF	111
NONE			



5V & 3.3V Fets

SYNC_MASTER=FINO-PC SYNC_DATE=04/12/2005

NOTICE OF PROPRIETARY PROPERTY

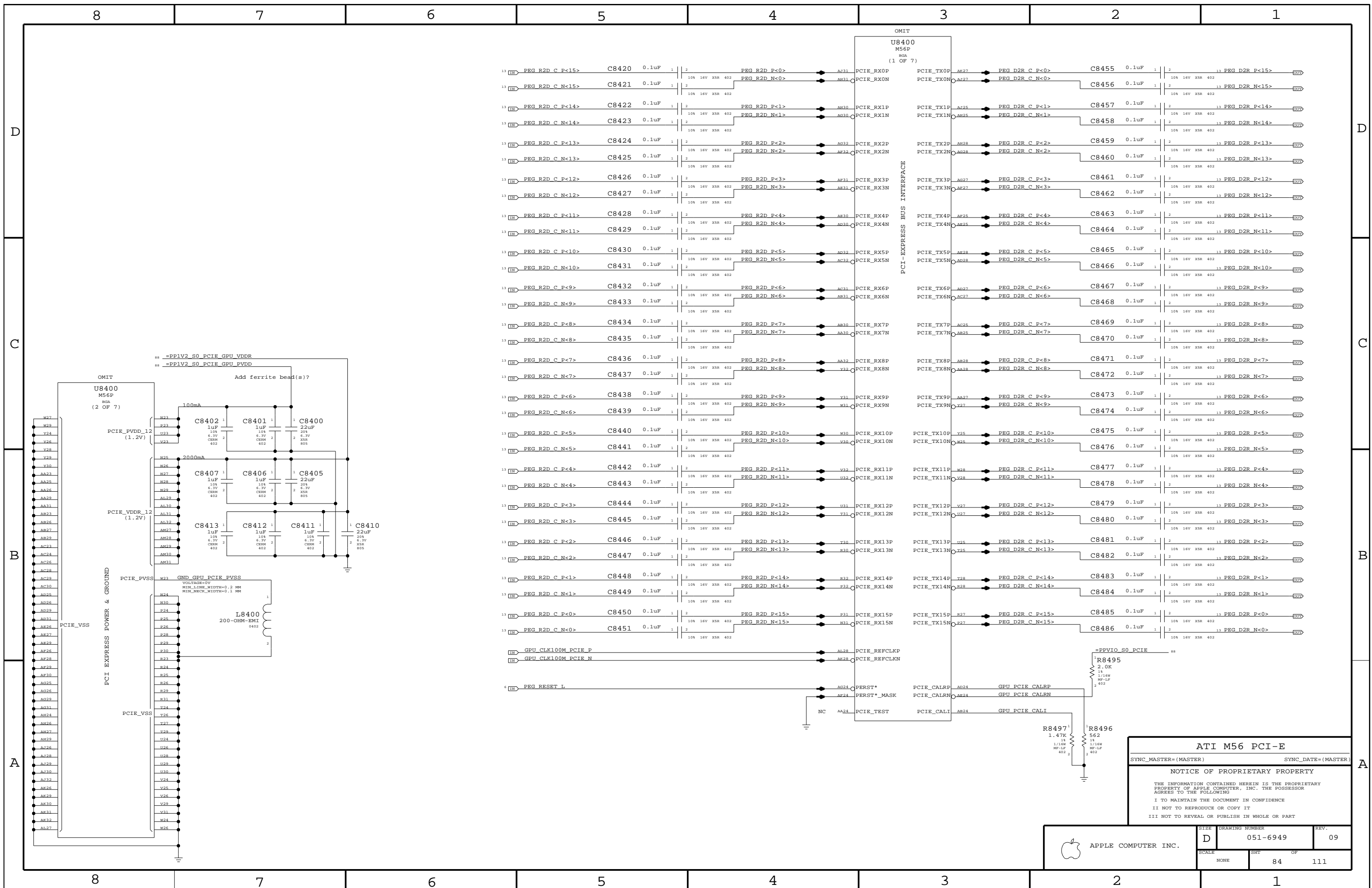
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	D	051-6949	09
SCALE	SHT	83 OF 111	
NONE			



ATI M56 PCI-E

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

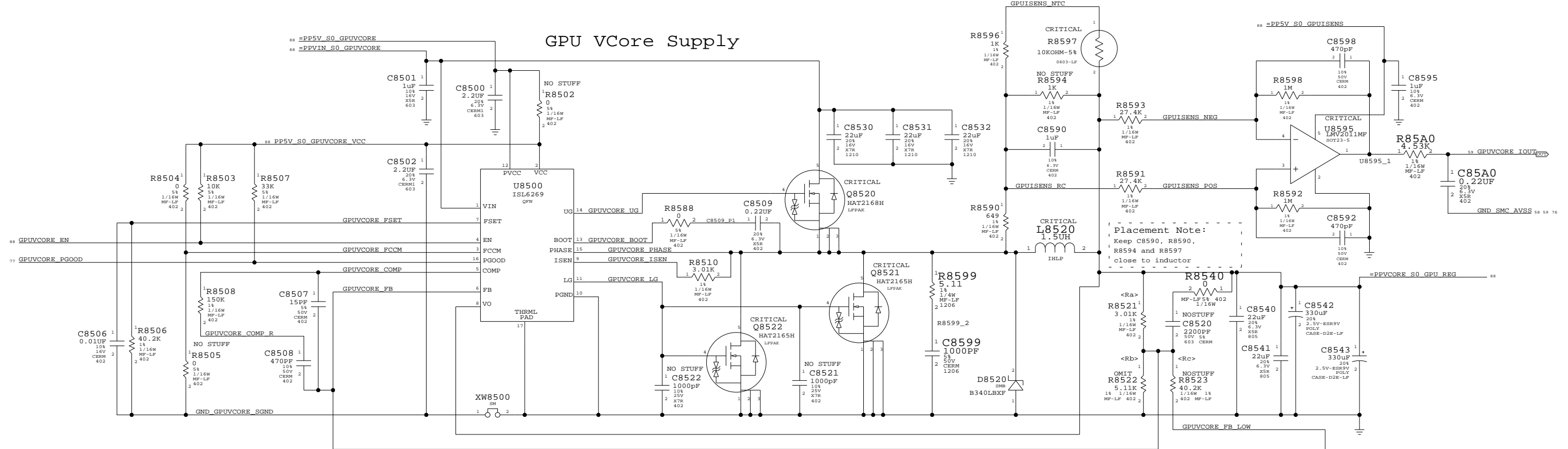
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GPU VCore Current Sense



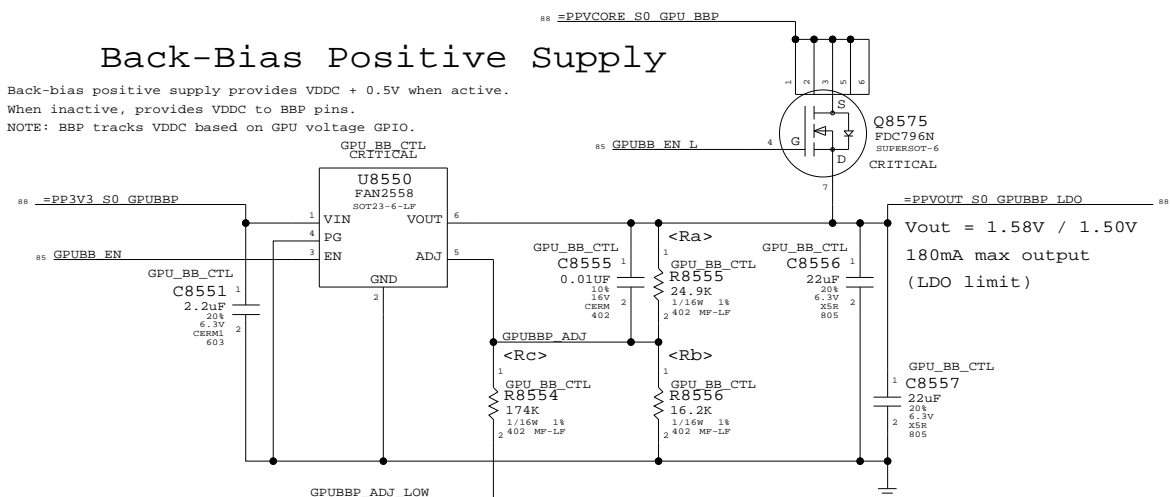
$$V_{out}(low) = 0.6V * (1 + R_a/R_b)$$

$$V_{out}(high) = 0.6V * (1 + R_a/Req)$$

$$Req = R_b || R_c$$

Back-Bias Positive Supply

Back-bias positive supply provides VDDC + 0.5V when active. When inactive, provides VDDC to BBP pins.
NOTE: BBP tracks VDDC based on GPU voltage GPIO.



$$V_{out}(low) = 0.59V * (1 + R_a/R_b)$$

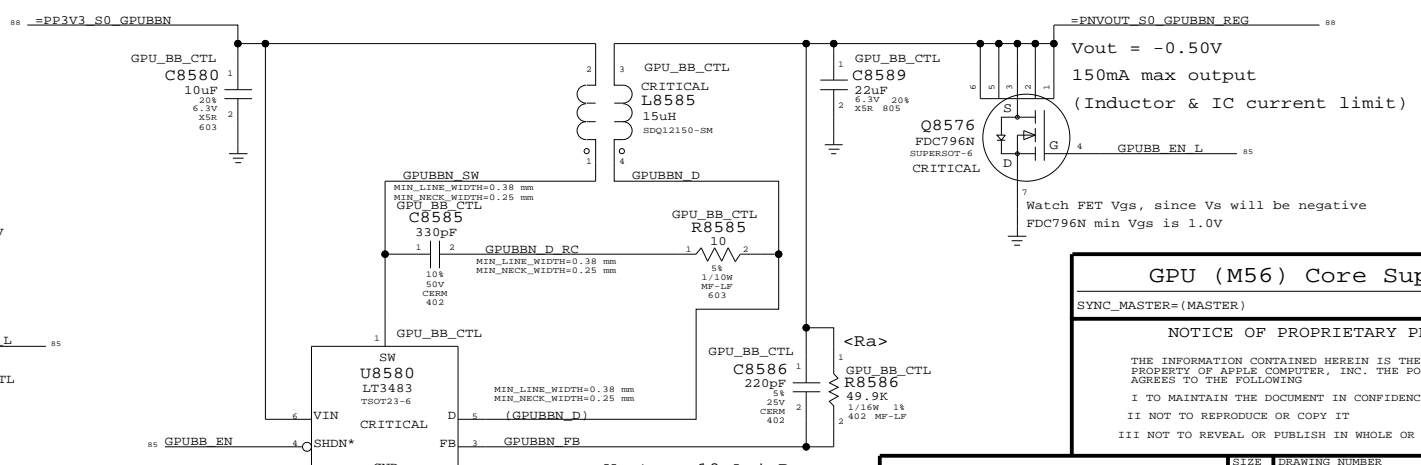
$$V_{out}(high) = 0.59V * (1 + R_a/Req)$$

$$Req = R_b || R_c$$

Pull-up voltage must be high enough to satisfy BBP FET Vgs (where Vs = 1.2V)
FDC796N max Vgs is 3.0V
Vin must be > 4.2V

Back-Bias Negative Supply

Back-bias negative supply provides VSS - 0.5V when active. When inactive, provides VSS to BBN pins.



GPU (M56) Core Supplies

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6949	09
SCALE	SHT	OF	
NONE	85	111	

Page Notes

Power aliases required by this page:
 - =PP1V5_GPU_VDD15
 - =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

8 7 6 5 4 3 2 1

D

C

B

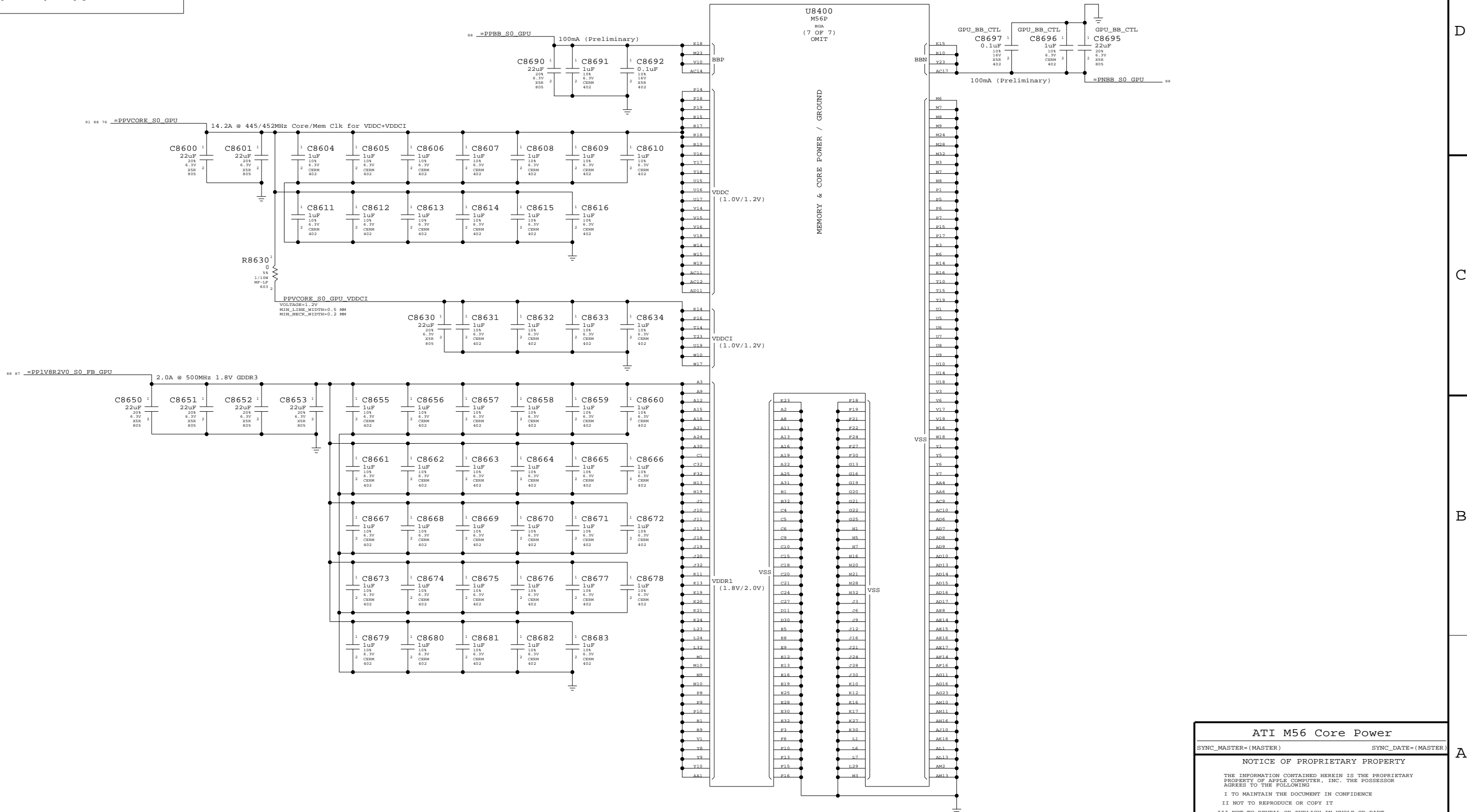
A

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ATI M56 Core Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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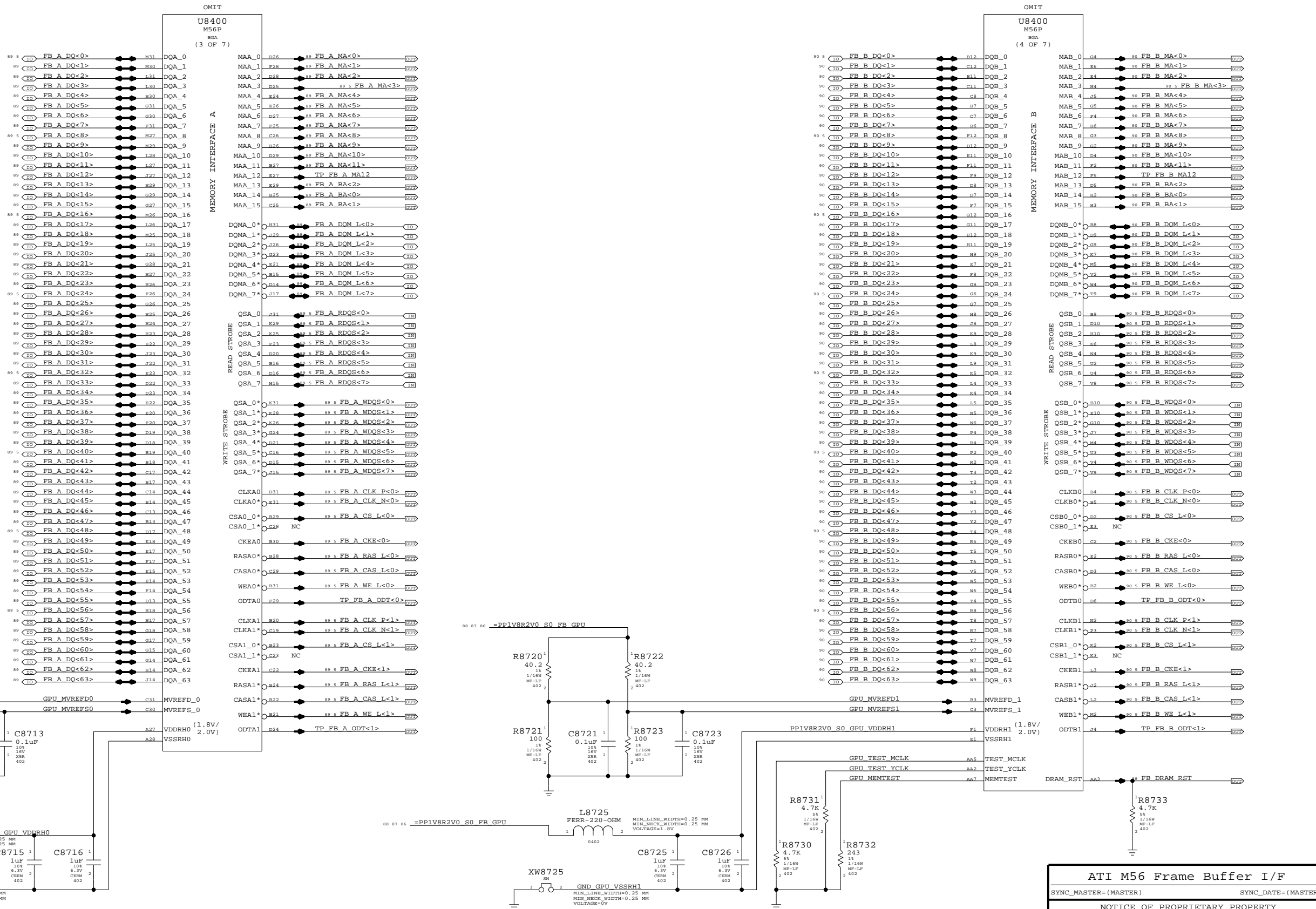
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6949	09
SCALE	NONE	SHT	OF
		86	111

8 7 6 5 4 3 2 1

Page Notes

Power aliases required by this page:
- =PP1V8R2V0_S0_FB_GPU
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)



ATI M56 Frame Buffer I/F

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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Table with columns for DRAWING NUMBER (D 051-6949), REV. (09), SCALE (NONE), SHEET (87 OF 111), and APPLE COMPUTER INC. logo.

8

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"S0" GPU RAILS

ONLY ON IN RUN

M56 GPIOs

=PP3V3_S0_GPU_VDDR3 #8 #1

59 EP1V0R1V2_S0_GPU
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=1.2V

85 PP5V_S0_GPUVCORE_VCC
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=5V

PP1V2_GPU_IO_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=1.2V

PPBB_S0_GPU
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=1.2V

PPNB_S0_GPU
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=0V

76 61 59 41 26 10 6 PP3V3_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=1.2V

77 6 PP2V5_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=1.2V

PP1V8R2V0_S0_FB_GPU
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=1.8V

83 81 80 79 78 6 5 PP12V_S5
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=1.2V

76 6 PP12V_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=1.2V

97 94 76 6 PP5V_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=5V

85 GPUVCORE_EN
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=5V

87 FB_DRAM_RST
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=5V

94 91 GPU_GPIO_0
GPIO 0 = TRANSMITTER POWER SAVINGS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_1
GPIO 1 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_2
GPIO 2 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_3
GPIO 3 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_4
GPIO 4 = DEBUG SIGNALS OUT

91 GPU_GPIO_5
GPIO 5 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_6
GPIO 6 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

TP_GPU_GPIO_7
MAKE_BASE=TRUE

91 GPU_GPIO_8
GPIO 8 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

NC_GPU_GPIO_10
MAKE_BASE=TRUE

91 GPU_GPIO_9
GPIO 9 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_13
GPIO 13 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_12
GPIO 12 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_11
GPIO 11 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_24
GPIO 24 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_27
GPIO 27 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_28
GPIO 28 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_29
GPIO 29 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

85 GPU_VCORE_LOW
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=5V

91 GPU_GPIO_15
GPIO 15 = SWITCH CORE VOLTAGE HIGH TO LOW
EXTERNAL PULL DOWN RECOMMENDED

TP_GPU_GPIO_14
MAKE_BASE=TRUE

TP_GPU_GPIO_17
MAKE_BASE=TRUE

TP_GPU_VGA_R
MAKE_BASE=TRUE

TP_GPU_VGA_G
MAKE_BASE=TRUE

TP_GPU_VGA_B
MAKE_BASE=TRUE

TP_GPU_VGA_HSYNC
MAKE_BASE=TRUE

TP_GPU_VGA_VSYNC
MAKE_BASE=TRUE

TP_GPU_TV_Y
MAKE_BASE=TRUE

TP_GPU_TV_COMP
MAKE_BASE=TRUE

TP_GPU_TV_C
MAKE_BASE=TRUE

TP_GPU_DDC_B_CLK
MAKE_BASE=TRUE

TP_GPU_DDC_B_DATA
MAKE_BASE=TRUE

GPU MISC

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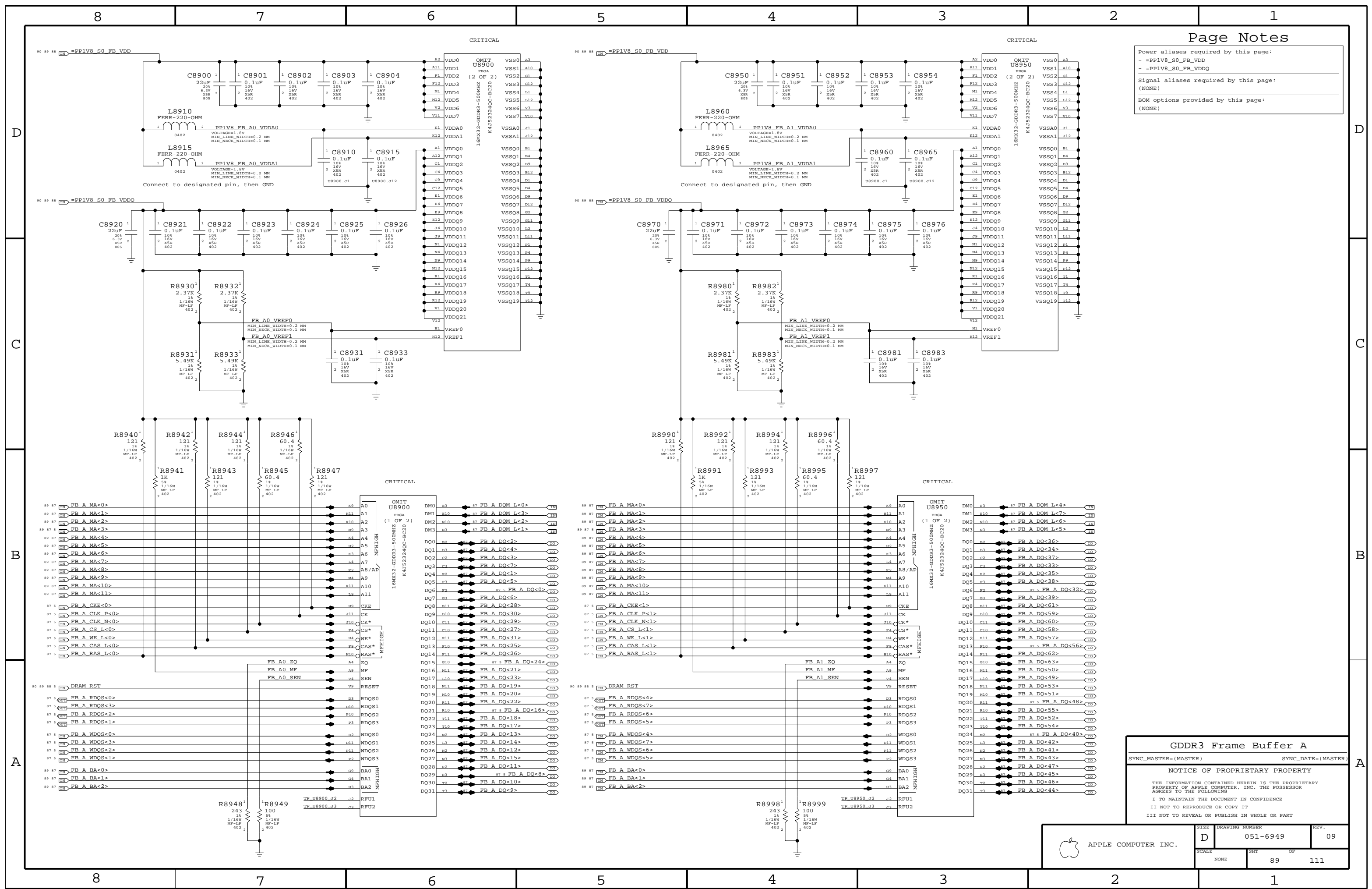
2

1

Power aliases required by this page:
 - =PPIV8_S0_FB_VDD
 - =PPIV8_S0_FB_VDDQ

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)



GDDR3 Frame Buffer A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

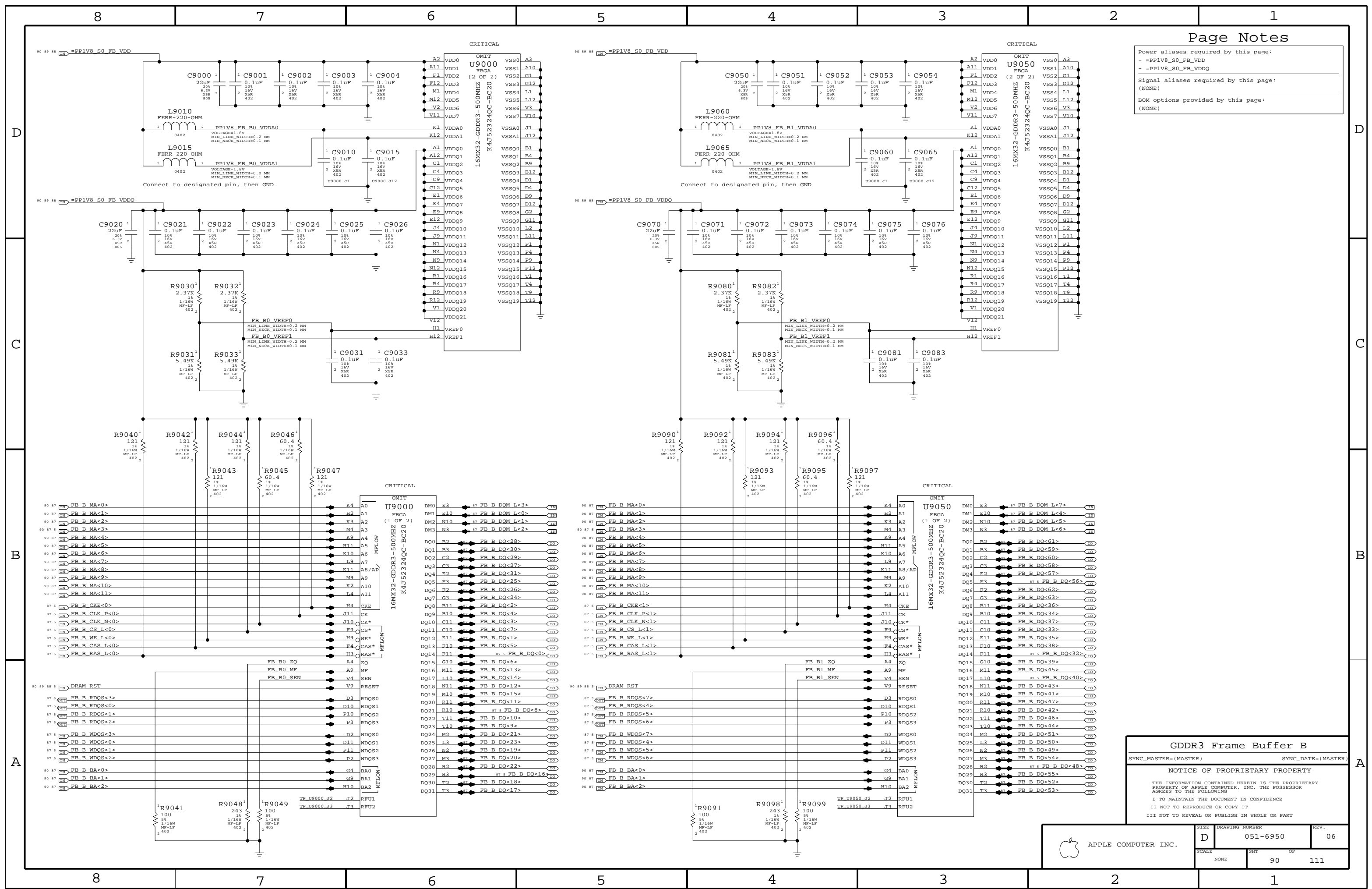
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Power aliases required by this page:
 - =PPIV8_S0_FB_VDD
 - =PPIV8_S0_FB_VDDQ

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)



GDDR3 Frame Buffer B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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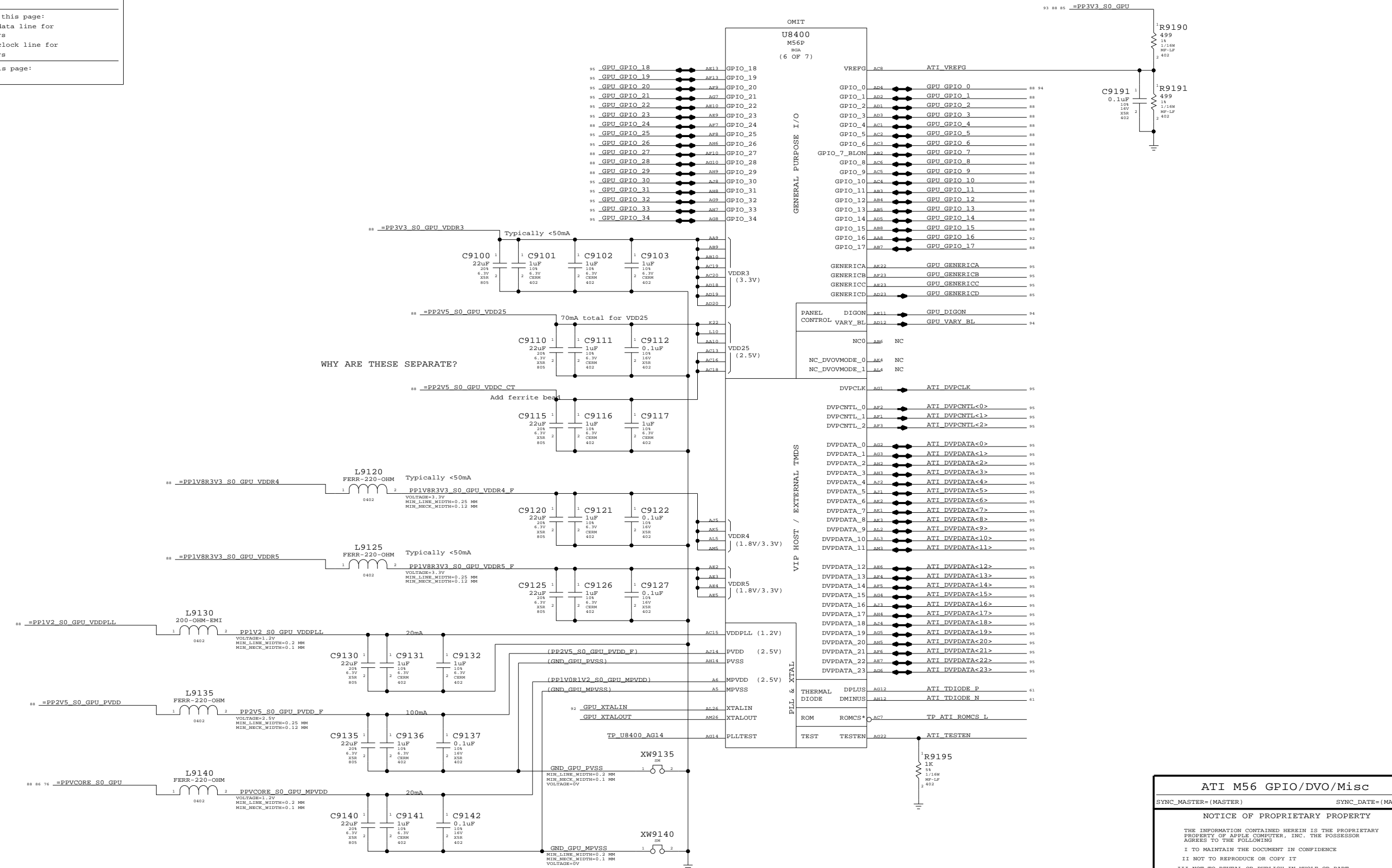
Page Notes

Power aliases required by this page:
 - =PP3V3_GPU_GPIOS
 - =PP2V5_PVDD
 - =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
 - =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
 - =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
 (NONE)

D
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ATI M56 GPIO/DVO/Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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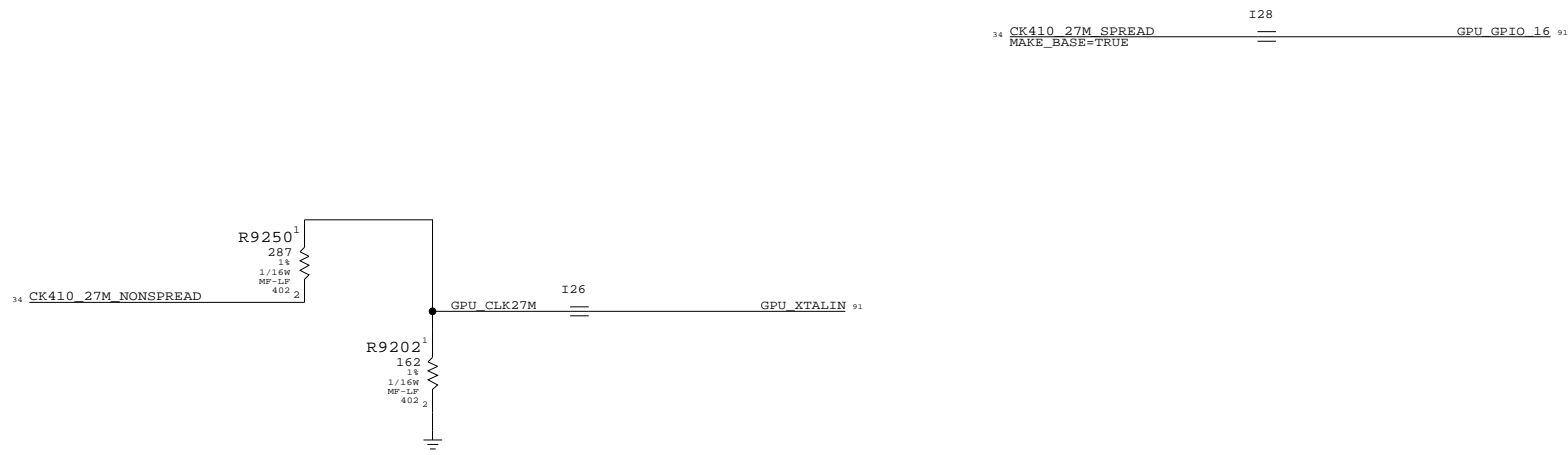
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Page Notes

Power aliases required by this page:
 - =PP3V3_GPU_CLOCKS - =PP3V3_GPU_PWRSEQ
 - =PPVIN_GPU_LVDDR_LDO - =PP2V5_GPU_PWRSEQ
 - =PP2V5_GPU_LVDDR_LDO - =PP1V8_GPU_PWRSEQ
 - =PP1V5_GPU_PWRSEQ

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - GPU_SS - GPU_LVDDR_2V8



GPU CLOCKS

SYNC_MASTER=BOZEMAN SYNC_DATE=05/21/2005

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SCALE	SHT	OF	
NONE	92	111	

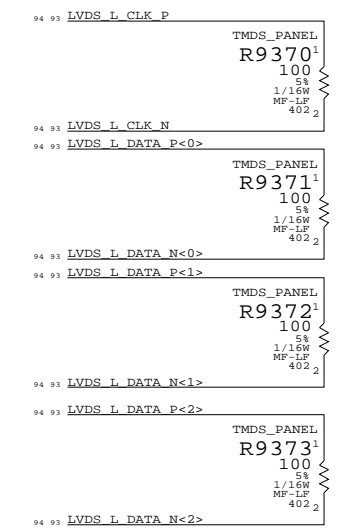
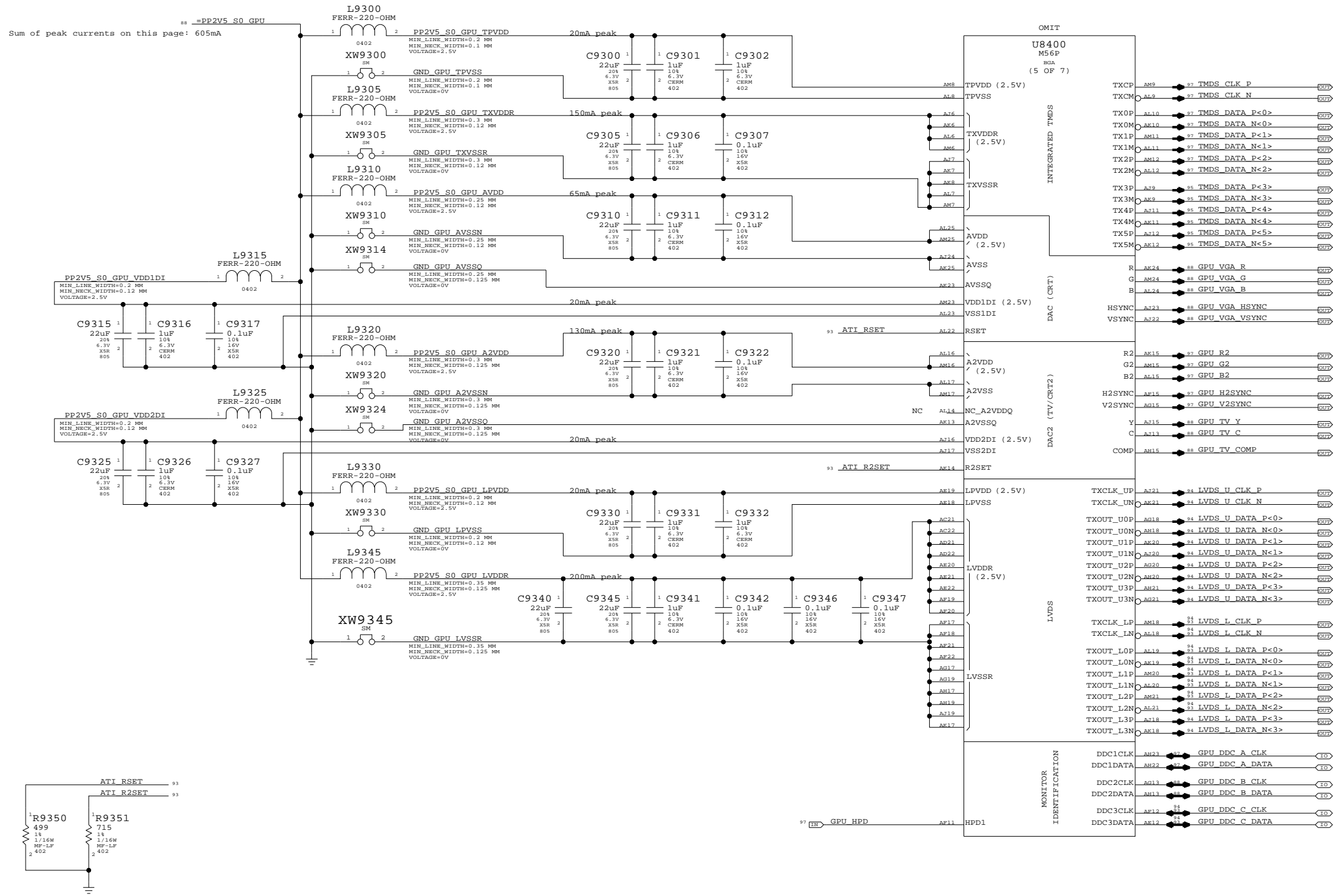
Page Notes

Power aliases required by this page:
 - =PP2V5_S0_GPU
 - =PP1V8R2V5_S0_GPU_LVDDR

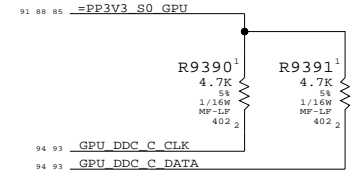
Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

TERMINATION FOR TMDS USAGE OF LVDS PINS
 PLACE CLOSE TO GPU (U8400)



Composite/S-Video	VGA	Component
Y	G	Y
C	R	Pr
Comp	B	Pb



ATI M56 Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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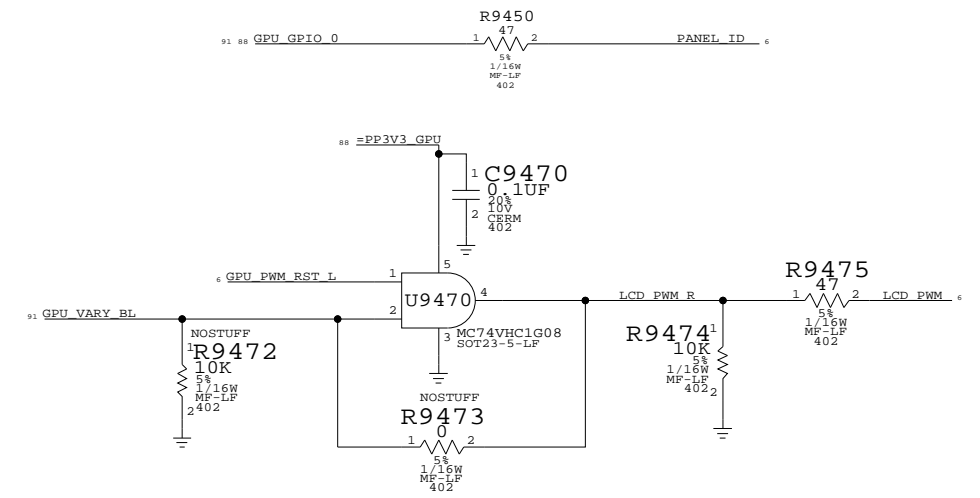
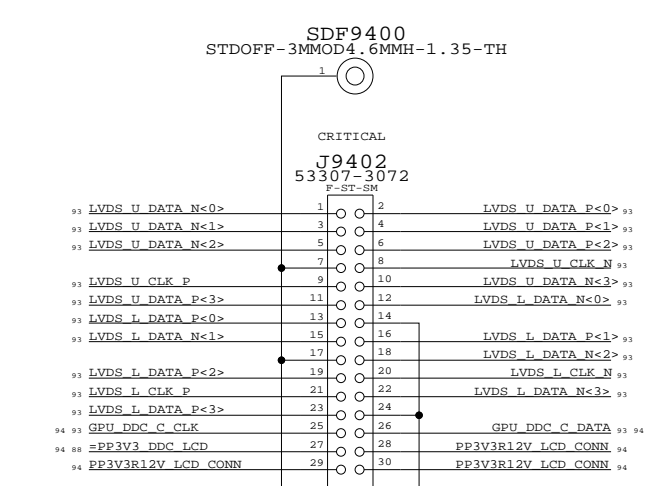
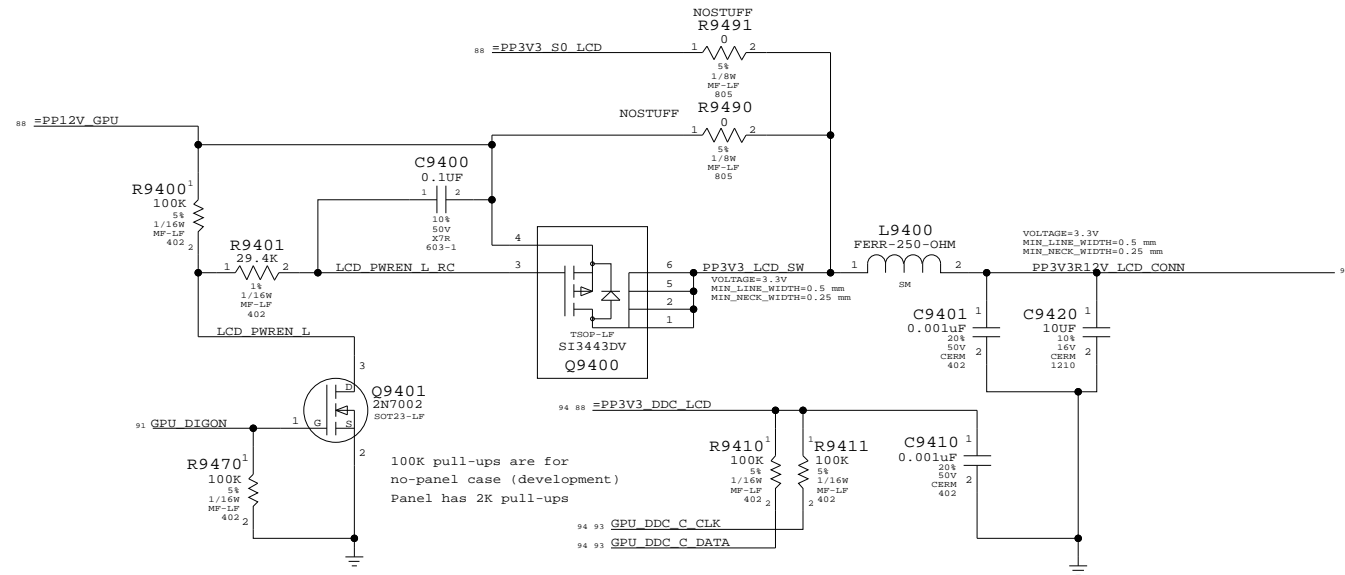
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APPLE COMPUTER INC.	SCALE	SHT	OF	REV.
	NONE	93	111	09

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S0302	338S0266		U8400	IC,ATI,M560,GRAFIX CTLR,88P8GA,LF

INVERTER INTERFACE

LCD (LVDS) INTERFACE



GATE TO PREVENT LEAKAGE ONTO PWM
MIGHT BE ABLE TO BYPASS IF SMC DRIVES SIGNAL

Internal Display Conns
 SYNC_MASTER=BOZEMAN SYNC_DATE=04/27/2005
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	D	051-6950	06
SCALE	SHT	OF	
NONE	94	111	

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D

D

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TP GPU GPIO<33> == GPU_GPIO_33 91
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TP GPU GPIO<32> == GPU_GPIO_32 91
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TP GPU GPIO<31> == GPU_GPIO_31 91
 MAKE_BASE=TRUE

TP GPU GPIO<30> == GPU_GPIO_30 91
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TP GPU GPIO<26> == GPU_GPIO_26 91
 MAKE_BASE=TRUE

TP GPU GPIO<25> == GPU_GPIO_25 91
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TP GPU GPIO<23> == GPU_GPIO_23 91
 MAKE_BASE=TRUE

TP GPU GPIO<22> == GPU_GPIO_22 91
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TP GPU GPIO<21> == GPU_GPIO_21 91
 MAKE_BASE=TRUE

TP GPU GPIO<20> == GPU_GPIO_20 91
 MAKE_BASE=TRUE

TP GPU GPIO<19> == GPU_GPIO_19 91
 MAKE_BASE=TRUE

TP GPU GPIO<18> == GPU_GPIO_18 91
 MAKE_BASE=TRUE

TP GPU GENERIC A == GPU_GENERIC A 91
 MAKE_BASE=TRUE

TP GPU GENERIC B == GPU_GENERIC B 91
 MAKE_BASE=TRUE

TP GPU GENERIC C == GPU_GENERIC C 91
 MAKE_BASE=TRUE

C

C

B

B

A

A

8

7

6

5

4

3

2

1

M56 TPS

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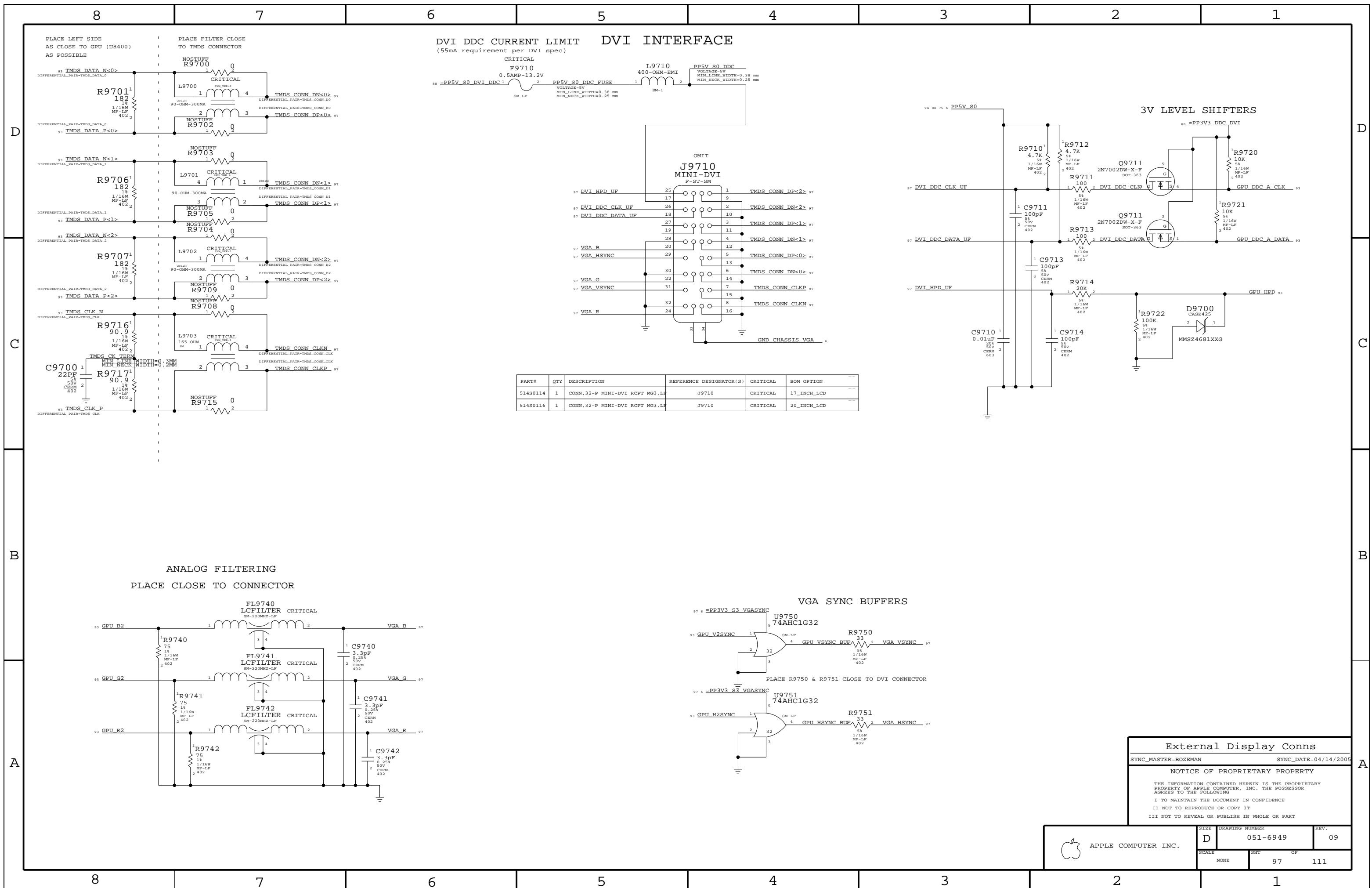
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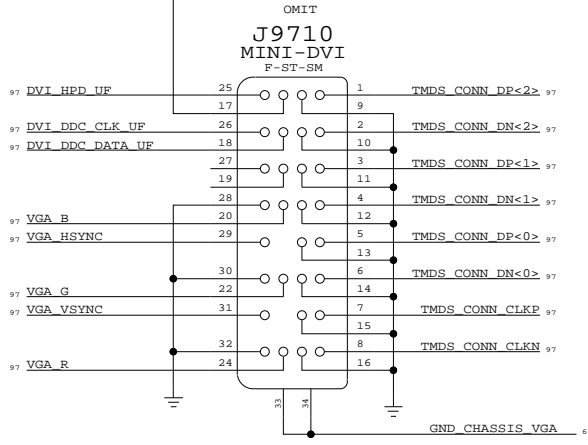
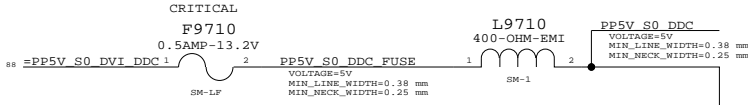
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SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE	SHT 95 OF 111	
NONE		

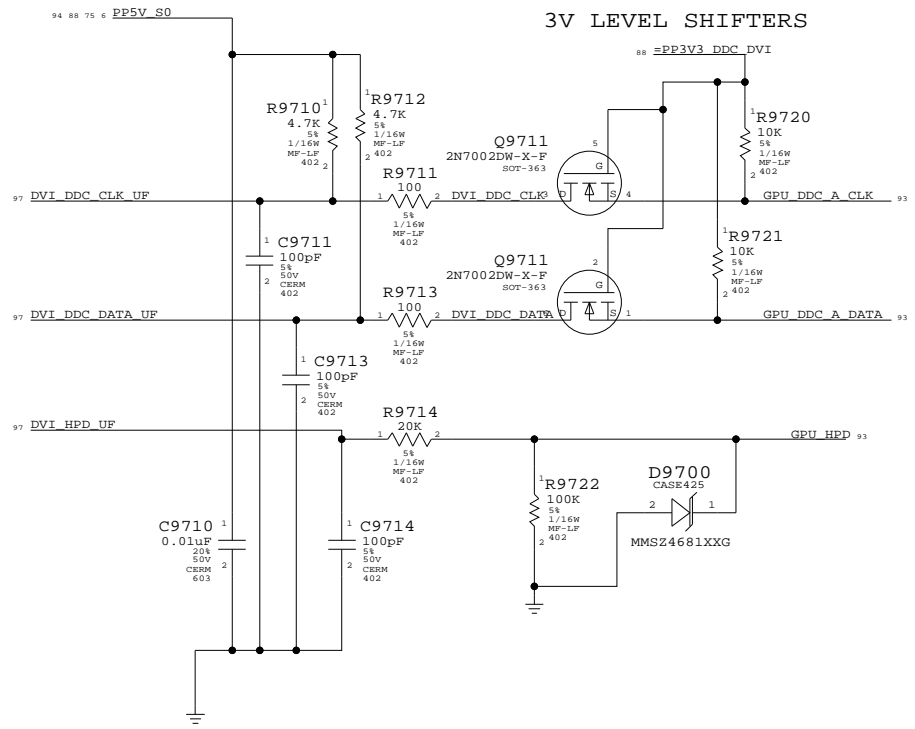


DVI DDC CURRENT LIMIT DVI INTERFACE

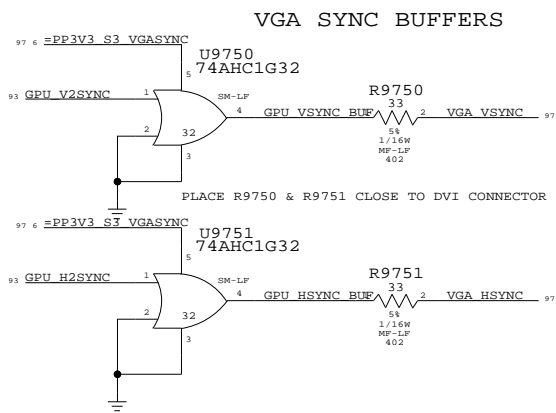
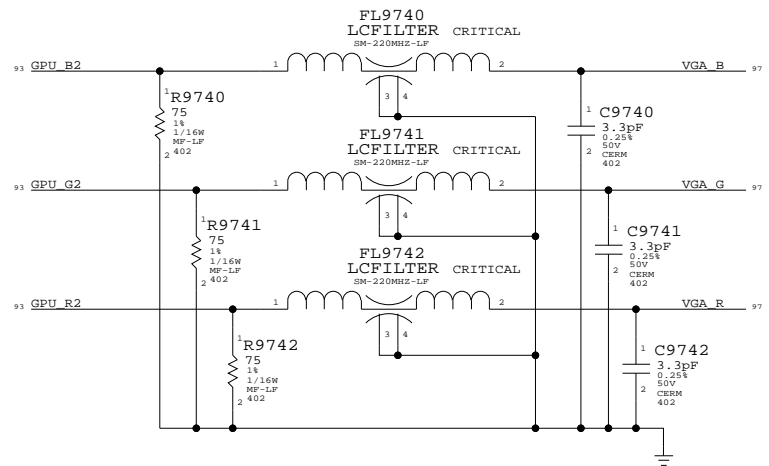
(55mA requirement per DVI spec)



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
51480114	1	CONN, 32-P MINI-DVI RCPT MG3,LF	J9710	CRITICAL	17_INCH_LCD
51480116	1	CONN, 32-P MINI-DVI RCPT MG3,LF	J9710	CRITICAL	20_INCH_LCD



ANALOG FILTERING
PLACE CLOSE TO CONNECTOR



External Display Conns

SYNC_MASTER=BOZEMAN SYNC_DATE=04/14/2005

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Table with 8 columns (8 to 1) and 5 rows (A to D), containing component names and reference designators. The table is divided into sections A, B, C, and D on both sides.

Table with 8 columns and 8 rows. Each cell contains alphanumeric codes and IDs. The table is framed by letters A, B, C, D on the sides and numbers 1-8 on the top and bottom.

D

C

B

A

D

C

B

A

