1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

IMG5 17" REV E
11/01/05

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
E		408158	PRODUCTION RELEASED	11/01/05	?

PDF	CSA	CONTENTS	SYNC	MASTER	DATE
2	2	System Block Diagram		FINO-DD	06/20/2005
3	4	Power Block Diagram		FINO-PC	06/20/2005
4	5	Table Items		FINO-M23	08/26/2005
5	6	FUNC TEST 1 OF 2		FINO-ME	06/20/2005
6	7	Power Conn / Alias		M23-PC	06/20/2005
7	8	Signal Alias		FINO-DD	06/20/2005
8	9	FUNC TEST 2 OF 2		FINO-ME	06/20/2005
9	11	1.8V Vreg		M23-PC	06/20/2005
10	12	1.5V Vreg		FINO-PC	06/20/2005
11	13	1.2V Vreg		FINO-PC	06/20/2005
12	15	2.5V Vreg		FINO-PC	06/20/2005
13	16	5V & 3.3V Fets		FINO-PC	06/20/2005
14	17	Vesta Core / Misc		FINO-DC	06/20/2005
15	19	KODIAK CORE & BYPASS		Q63	08/01/2005
16	20	KODIAK & SHASTA MISC		FINO-ME	06/20/2005
17	23	Shasta Core Power		Q63	08/01/2005
18	24	Shasta Serial / Misc		FINO-ME	06/20/2005
19	25	PULSAR2 POWER		Q63	08/01/2005
20	26	PULSAR2 CLOCKS		FINO-ME	06/20/2005
21	27	Pulsar Aliases		FINO-ME	06/20/2005
22	28	System Management Unit		Q63	08/01/2005
23	29	SMU SUPPLEMENTAL (2)		FINO-HS	06/20/2005
24	30	SMU SUPPLEMENTAL (3)		FINO-HS	06/20/2005
25	31	SMU SUPPLEMENTAL (4)		FINO-HS	06/20/2005
26	32	Fan 0, 1 & System Temp		FINO-HS	06/20/2005
27	33	Fan 2 & HD Temp		FINO-HS	06/20/2005
28	39	I2C Connections		FINO-ME	06/20/2005
29	41	KODIAK EI PWR & CAPS		Q63	08/01/2005
30	42	KODIAK EI A		Q63	08/01/2005
31	43	CPU EI AND IO		FINO-HS	06/20/2005
32	44	KODIAK EI B		Q63	08/01/2005
33	47	CPU STRAPS		FINO-HS	06/20/2005
34	48	CPU POWER AND BYPASS		FINO-HS	06/20/2005
35	49	PROC DECOUPLING		FINO-HS	06/20/2005
36	50	CPU VCORE VREG		M23-HS	06/20/2005
37	52	CPU VCORE MORE BYPASS		FINO-HS	06/20/2005
38	54	CPU AVDD VREG		FINO-HS	06/20/2005
39	55	T,V,I SENSORS		FINO-HS	06/20/2005
40	56	CPU ALIASES & MISC		FINO-HS	06/20/2005
41	58	KODIAC NBMEM PWR & CAPS		Q63	08/01/2005
42	59	Kodiak Memory Dq/Ctl		FINO-DS	06/20/2005
43	61	Parallel Term		FINO-DS	06/20/2005
44	62	Main Memory Clock Buffer		FINO-DS	06/20/2005
45	63	MEMORY ADDR BRANCHING		FINO-DS	06/20/2005
46	67	Memory Dimm A		FINO-DS	06/20/2005
47	68	MLB Mem Series Term		FINO-DS	06/20/2005
48	69	On-Board DDR SDRAM		FINO-DS	06/20/2005
49	70	On-Board DDR SDRAM		FINO-DS	06/20/2005
50	82	KODIAK PCI-E X16		Q63	08/01/2005
51	84	GPU PCIe		M23-DD	06/20/2005
52	85	Graphics Vregs		M23-DD	06/20/2005
53	86	GPU Core Power		FINO-DD	06/20/2005
54	87	GPU Frame Buffer		FINO-DD	06/20/2005
55	88	FB Series Termination		FINO-DD	06/20/2005
56	89	GPU GDDR SDRAM A		FINO-DD	06/20/2005
57	90	GPU GDDR SDRAM B		FINO-DD	06/20/2005
58	92	GPU Straps		FINO-DD	06/20/2005
59	93	GPU DVI & DACs		FINO-DD	06/20/2005
60	96	TMDS/Inverter/ExtVGA		M23-DD	06/20/2005
61	97	KODIAK PCI-E CONST		FINO-DD	06/20/2005
62	98	KODIAK HT16		Q63	08/01/2005
63	101	HT ALIASES		FINO-ME	06/20/2005
64	103	Shasta HyperTransport		Q63	08/01/2005
65	119	Shasta PCI Interface		Q63	08/01/2005
66	120	PCI SERIES TERMINATION		FINO-MW	06/20/2005
67	121	AIRPORT & BLUETOOTH		FINO-MW	06/20/2005
68	122	USB 2.0 PCI Interface		Q63	08/01/2005
69	125	BootROM		Q63	08/01/2005
70	127	Shasta Disk		M23-DC	06/20/2005
71	129	Disk Connectors		M23-DC	06/20/2005
72	130	ENET SERIES TERM		FINO-DC	06/20/2005
73	131	Shasta Ethernet		Q63	08/01/2005
74	132	Vesta Ethernet PHY		Q63	08/01/2005
75	136	ETHERNET CONNECTOR		FINO-DC	06/20/2005
76	138	Shasta FireWire		Q63	08/01/2005
77	139	Vesta FireWire PHY		Q63	08/01/2005
78	140	FIREWIRE CONNECTORS		FINO-DC	06/20/2005
79	142	USB Host Interfaces		FINO-PC	07/05/2005
80	143	USB Device Interfaces		FINO-PC	06/20/2005
81	144	Flash Media Ctrl		FINO-PC	06/20/2005
82	145	Flash Connector		FINO-PC	06/20/2005
83	147	AUDIO: CODEC		FINO-SO	10/07/2005
84	148	AUDIO: LINE INPUT AMP		FINO-SO	10/07/2005
85	150	AUDIO: LINE OUT AMP		FINO-SO	10/07/2005
86	152	AUDIO: SPEAKER AMP		FINO-SO	10/07/2005
87	153	AUDIO: CONNECTORS		FINO-SO	10/07/2005
88	154	AUDIO: POWER SUPPLIES		FINO-SO	10/07/2005

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER | DESIGN CK
ENG APPD | MFG APPD
QA APPD | DESIGNER
RELEASE | SCALE NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

Apple Computer Inc.

TITLE
SCH,MLB,IMG5,17

DRAWING NUMBER 051-6790 REV. E

SHT 1 OF 154

U4300
CPU
NEO 10S
PAGE 43,48

32-BIT
APPLE PI
ELASTIC INTERFACE
667MHZ OR 733MHZ

J9602, J9603
TMDS
EXT VGA
PAGE 96

U6200
CLOCK
BUFFER
PAGE 62

FANS
TEMP SENSORS
PAGES 32,33

U2800
SMU
PAGE 28

U2801
RTC
PAGE 28

SMU SUPPLEMENTAL
BUTTONS
ALS
SYSTEM LED
BATTERY
PAGES 29,30

APPLE PI
PAGE 42

U8900, U8901
FRAME
BUFFER A
PAGE 89

64-BIT
FRAME BUFFER
M23:1.8V/600MHZ
M33:1.8V/700MHZ

U8400
GPU
M23:RV370 XT
M33:RV380 XT
PAGES 84,86,87,93

PCIE X16
2.5GHZ

PCIE
PAGE 82

U1900
KODIAK
CORE
PAGE 19

MAIN MEMORY
PAGE 59

64-BIT
MAIN MEMORY
1.8V/533MHZ

PARALLEL
TERM
PAGE 61

J6700
DIMM
PAGE 67

ONBOARD MEMORY

SERIES
TERM
PAGES 68

64MX8
MEMORY
PAGES 67,70

MISC
PAGE 20

HYPERTRANSPORT
PAGE 98

64-BIT
FRAME BUFFER
M23:1.8V/600MHZ
M33:1.8V/700MHZ

U9000, U9001
FRAME
BUFFER B
PAGE 90

8-BIT
HYPERTRANSPORT
1.2V/800MHZ
CONTROL = 2.5V

U2500
PULSAR2
POWER
PAGE 25
CLOCKS
PAGE 26

I2C
PAGE 39

JE310/JE320/JE330
USB
CONNECTORS
PAGE 143

JE350
BNDI
INTERFACE
PAGE 143

UE401
USB
HUB
PAGE 144

UE400
FLASH
CTLR
PAGE 144

USB
PAGE 142

UC200
USB 2.0
uPD720101
PCI
PAGE 122

UC500
BOOTROM
PAGE 125

JC150
WIRELESS
CONNECTOR
PAGE 121

JE500
MEDIA CARD CONNECTOR
CF SD
PAGE 145

HARD DRIVE

JC900
SATA
CONNECTOR
PAGE 129

SATA/150
1.2V/1.5GHZ

SATA1
SATA2
SATA
PAGE 127

HYPERTRANSPORT
PAGE 103

U2300
SHASTA

PCI
PAGE 119

32-bit PCI (5V-3.3V/33MHz)

GPIO/PCI64
PAGE 24

OPTICAL

JC901
UATA
CONNECTOR
PAGE 129

UATA/133
3.3V/133MHZ

UATA
PAGE 127

CORE
PAGE 23

NCS
PAGE 142

ETHERNET
PAGE 131

FIREWIRE
PAGE 138

I2S
PAGE 24
SCCA I2S1
SCCB I2S2
I2S0

GMII (3.3V/125MHz)
8-bit TX & 8-bit RX

1394 PHY (3.3V/98MHz)
8-bit TX & RX

UE700
AUDIO CODEC
PCM3052A
PAGE 147

S/PDIF

OPTICAL OUT

JF303
COMBO OUT
CONNECTOR
PAGE 153

LINE OUT

LINE OUT
AMP
PAGE 150

SPEAKER
AMP
PAGE 152

JF301
SPEAKER
CONNECTOR
PAGE 153

LINE IN
AMP
PAGE 148

JF300
LINE IN
CONNECTOR
PAGE 153

BNDI
INTERFACE

U1701
VESTA
GIG ETHERNET
PAGE 132
FIREWIRE A
PAGE 139
0 1

4 Diff pairs
2 Diff pairs

JD600
ETHERNET
CONNECTOR
PAGE 136

JEC00, JEC01
FIREWIRE A
CONNECTORS
PAGE 140

System Block Diagram

SYNC_MASTER=FINO-DD SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E

SCALE NONE SHT 2 OF 154

POWER CONNECTOR

J700
PAGE 7

SYS_POWERUP_L

PP12V_ALL — FW CONN
PP12V_RUN — 20" PANEL POWER, 17" LCD INVERTER
PP5V_RUN — OPTICAL
PP5V_ALL
PP3V3_ALL
PP3V3_RUN — PCI BUS, AUDIO CODEC

SMU
POWER SEQUENCE PIN

SYS_POWERUP_L
NC_SMU_PWRSEQ_P1_0 — SMU_PWRSEQ_P1_0
NC_SMU_PWRSEQ_P1_4 — SMU_PWRSEQ_P1_4
TURN_ON_PP1V2_L — SMU_PWRSEQ_P1_1
PP3V3_PWRON
PWR_GOOD_PP1V5 — SMU_PWRSEQ_P9_5
PWR_GOOD_PP1V8 — SMU_PWRSEQ_P9_6
TURN_ON_PP3V3_PWRON_L — SMU_PWRSEQ_P1_2
SMU_PWRSEQ_P1_3

PP1V5_PWRON SWITCHER — PAGE 12 — PULSAR, KODIAK CORE
PP1V5_RUN FET SWITCH — PAGE 12 — EI
CPU CORE SWITCHER — PAGE 50
GPU CORE SWITCHER — PAGE 85
PP1V8_PWRON SWITCHER — PAGE 11 — MAIN MEMORY
PP1V8_RUN POWER SW — PAGE 11 — GPU MEMORY
PP0V9_GPU_VTT LINEAR — PAGE 91
PP4V5_RUN_AUDIO LINEAR — PAGE 154 — AUDIO CODEC
PP5V_PWRON FET SWITCH — PAGE 16 — USB CONN
PP2V5_ALL LINEAR — PAGE 15 — VESTA
PP2V5_PWRON FET SWITCH — PAGE 15
PP2V5_RUN FET SWITCH — PAGE 15
PP3V3_PWRON FET SWITCH — PAGE 16 — MODEM & BT USB2 HOST
PP2V5_RUN_CPU_AVDD LINEAR — PAGE 54
PP2V5_GPU_A2VDD LINEAR — PAGE 85
PP1V8_TPVDD LINEAR — PAGE 85
PP1V5_VDDC_CT LINEAR — PAGE 85
PP1V8_GPU LINEAR — PAGE 85
PP1V2_TPVDD LINEAR — PAGE 85
PP1V2_ALL SWITCHER — PAGE 13 — VESTA CORE
PP1V2_PWRON FET SWITCH — PAGE 13 — SHASTA CORE
PP1V2_RUN FET SWITCH — PAGE 13 — HT BUS

PP2V5_ALL
R431 10K 5% 1/16W MF-LF 402

PP1V5_PWRON
R430 100K 5% 1/10W MF-LF 402 — COMPARE_PP1V5
PS_1V_REF
U400 LM339A SOI-LF GND V+
C430 0.01UF 20% 16V CERM 402

R440 100K 5% 1/16W MF-LF 402 — COMPARE_PP1V8
C440 0.01UF 20% 16V CERM 402

PP2V5_ALL
R442 150K 5% 1/16W MF-LF 402
R443 100K 1% 1/10W MF-LF 402
PP5V_ALL
PS_1V_REF
U400 LM339A SOI-LF GND V+
PP2V5_ALL
R441 10K 5% 1/16W MF-LF 402
C441 0.1UF 20% 10V CERM 402

PP2V5_ALL
U400P2
U400 LM339A SOI-LF GND V+

Power Block Diagram

SYNC_MASTER=FINO-PC
SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E

SCALE: NONE
SHT 4 OF 154

PROCESSORS

NEED TO UPDATED BIN CODES AS NOTES

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION	
337S3224	1	PROCESSOR	CBGA-576-1MM	IC,GPUL,DD3.1,1.9G,85C	1.9GHZ	1.10V	45W	50MV	U4300	17_INCH_LCD	CRITICAL
337S3220	1	PROCESSOR	CBGA-576-1MM	IC,GPUL,DD3.1,2.1G,85C	2.1GHZ	1.10V	45W	50MV	U4300	20_INCH_LCD	CRITICAL

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
337S3225	337S3224	17_INCH_LCD	U4300	IC,DD3.1,1.9G,1.15V
337S3226	337S3224	17_INCH_LCD	U4300	IC,DD3.1,1.9G,1.20V
337S3227	337S3224	17_INCH_LCD	U4300	IC,DD3.1,1.9G,1.25V
337S3228	337S3224	17_INCH_LCD	U4300	IC,DD3.0X,1.9G,1.15V
337S3229	337S3224	17_INCH_LCD	U4300	IC,DD3.0X,1.9G,1.20V
337S3230	337S3224	17_INCH_LCD	U4300	IC,DD3.0X,1.9G,1.25V
337S3231	337S3224	17_INCH_LCD	U4300	IC,DD3.0X,1.9G,1.30V
337S3221	337S3220	20_INCH_LCD	U4300	IC,DD3.1,2.1G,1.15V
337S3222	337S3220	20_INCH_LCD	U4300	IC,DD3.1,2.1G,1.20V
337S3223	337S3220	20_INCH_LCD	U4300	IC,DD3.1,2.1G,1.25V

ASICS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
343S0379	1	IC,KODIAK,V1.2,PBGA,200MM	U1900		CRITICAL
343S0377	1	IC,ASIC,SHASTA,V1.1,PBGA,LF	U2300		CRITICAL
343S0356	1	IC,ASIC,VESTA,V1.3,LF	U1701		CRITICAL
343S0319	1	IC,PULSAR2,100P,P8MM,BGA	U2500		CRITICAL

MISC PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION		
051-6790	1	PCB,SCHEM,MLB,M23	SCH1	17_INCH_LCD		
051-6863	1	PCB,SCHEM,MLB,M33	SCH1	20_INCH_LCD		
820-1783	1	PCB,FAB,MLB,M23	MLB1	17_INCH_LCD	CRITICAL	
820-1766	1	PCB,FAB,MLB,M33	MLB1	20_INCH_LCD	CRITICAL	
062-2082	1	SPEC,VENDOR PACKAGING PROCEDURE	VPP1			
825-6447	1	BARCODE LABEL, MLB	LBL1			
341T1751	1	IC,FLASH,1MX8,3.3V,90NS	UC500		CRITICAL	
341T1752	1	PURCH ASSY, SMU BIG	U2800		CRITICAL	
603-7318	1	M23 CPU HEATSINK	MECH1	OMIT	CRITICAL	
603-7321	1	M33 CPU HEATSINK	MECH1	OMIT	CRITICAL	
603-7319	1	M23 GPU HEATSINK	MECH2	OMIT	CRITICAL	HEATSINKS ARE NOW ON THE PD BOM
603-7322	1	M33 GPU HEATSINK	MECH2	OMIT	CRITICAL	
603-7320	1	M23 NB HEATSINK	MECH3	OMIT	CRITICAL	
603-7323	1	M33 NB HEATSINK	MECH3	OMIT	CRITICAL	
875-1905	1	CPU GAP FILLER	GAP1			
875-2429	1	LED COVER TAPE	TAPE1	17_INCH_LCD		

ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
378S0140	378S0141		LED700,LED702	KINGBRIGHT LED
343S0388	343S0356		U1701	VESTA A4
126S0078	126S0086		C722	EL CAP
126S0068	126S0088		CF000	EL CAP
353S1321	353S1105		U400	LM339
138S0558	138S0547			10UF CAP ALL LOC.
124-0338	124-0333			PANASONIC CAPS

Table Items

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E

SCALE NONE SHT 5 OF 154

NO TEST XW NETS

I97	NO_TEST=YES	GND_U1100	11
I98	NO_TEST=YES	GND_U1200	12
I99	NO_TEST=YES	GND_U1300	13
I95	NO_TEST=YES	PP_2V5PWRONNBMISC	20
I93	NO_TEST=YES	PP_1V2PWRONSBVCORE	23
I92	NO_TEST=YES	PP_3V3PWRONSBPCIG4	23
I95	NO_TEST=YES	PP_2V5PWRONSB	23
I95	NO_TEST=YES	PP_1V2PWRONSBPLL45VDD	24
I94	NO_TEST=YES	PP_OVDD_PULSAR1	25
I96	NO_TEST=YES	PP_1V2PWRONPULSAR1	25
I96	NO_TEST=YES	PP_1V5PULSAR2	25
I97	NO_TEST=YES	PP_1V5PWRONPULSAR2	25
I98	NO_TEST=YES	GND_SMU_AVSS	28 55
I98	NO_TEST=YES	PP_3V3ALLSMUAVCC	28
I99	NO_TEST=YES	PP_3V3ALLSMU	28
I91	NO_TEST=YES	PP_VEINB	41
I92	NO_TEST=YES	GND_CPU_AVDD	48
I93	NO_TEST=YES	VC_AGND	50
I93	NO_TEST=YES	VC_OUTSEN_R	50
I95	NO_TEST=YES	KPVDD2_FMAX	55
I96	NO_TEST=YES	GND_GPU_PVSS	86
I97	NO_TEST=YES	GND_GPU_MPVSS	87
I106	NO_TEST=YES	GND_AUDIO_MIC	153 154

I90	NO_TEST=YES	GND_GPU_TPVSS	93
I90	NO_TEST=YES	GND_GPU_TXVSSR	93
I90	NO_TEST=YES	GND_GPU_VSSDI	93
I90	NO_TEST=YES	GND_GPU_AVSSN	93
I90	NO_TEST=YES	GND_GPU_AVSSQ	93
I90	NO_TEST=YES	GND_GPU_A2VSSN	93
I90	NO_TEST=YES	GND_GPU_A2VSSQ	93
I100	NO_TEST=YES	KOD_L15_GND	98 101
I100	NO_TEST=YES	PP_3V3SBPCI_B9	
I100	NO_TEST=YES	PP_2V5PWRONSB_B9	119
I100	NO_TEST=YES	PP_VIOPCIUSB2_C2	122
I101	NO_TEST=YES	PP_1V2PWRONDISKSB_CC	127
I101	NO_TEST=YES	PP2V5_VESTA_BIASVDD1	132
I101	NO_TEST=YES	PP2V5_VESTA_XTALVDD1	132
I102	NO_TEST=YES	PP1V2_VESTA_PLLVDD1	132
I102	NO_TEST=YES	PP1V2_VESTA_PLLVDD2	139
I102	NO_TEST=YES	PP2V5_VESTA_BIASVDD2	139
I102	NO_TEST=YES	PP2V5_VESTA_XTALVDD2	139
I103	NO_TEST=YES	PP1V2_VESTA_FAVDDL	139
I103	NO_TEST=YES	PP2V5_VESTA_FAVDDM	139
I103	NO_TEST=YES	PP3V3_VESTA_FAVDDH	139
I104	NO_TEST=YES	PP3V3_PWRON_NEC_AVDD	142
I104	NO_TEST=YES	GND_AUD_LOAMP	150 154

I101	NO_TEST=YES	GND_NEC_AVSS_R	142
I101	NO_TEST=YES	GND_AUDIO_SPKRAMP_PLANE	152 154
I101	NO_TEST=YES	GND_AUDIO_CODEC	147 148 150 154
I101	NO_TEST=YES	KPGND2_FMAX	55
I101	NO_TEST=YES	TDIODE_POS_FMAX	55
I101	NO_TEST=YES	TDIODE_NEG_FMAX	55
I101	NO_TEST=YES	DAGND	55
I101	NO_TEST=YES	INA138_OUT	55
I105	NO_TEST=YES	RAMCLK_AVSS	62
I105	NO_TEST=YES	PP12V_AUDIO_SPKRAMP	7 152
I105	NO_TEST=YES	GND_AUDIO	7 154
I105	NO_TEST=YES	GND_AUDIO_SPKRAMP	7 152 154
I101	NO_TEST=YES	KOD_H05_GND	82 97
I101	NO_TEST=YES	KOD_K07_GND	82 97
I101	NO_TEST=YES	KOD_G10_GND	82 97
I101	NO_TEST=YES	KOD_J13_GND	82 97
I101	NO_TEST=YES	KOD_L13_GND	82 97
I101	NO_TEST=YES	KOD_H08_GND	82 97
I101	NO_TEST=YES	PCIE_SLOTA_PRSNT_L	82 84
I101	NO_TEST=YES	U8500_GND	85
I101	NO_TEST=YES	GND_AUD_LOAMP_CHGPMP	150 154

EE IDENTIFIED NO TEST NETS

I955	NO_TEST=YES	NC_EI_NB_TO_CPU_B_CLK_P	56
I957	NO_TEST=YES	NC_EI_NB_TO_CPU_B_CLK_N	56
I958	NO_TEST=YES	NC_EI_NB_TO_CPU_B_AD<0..43>	56
I959	NO_TEST=YES	NC_EI_NB_TO_CPU_B_SR_P<0..1>	56
I960	NO_TEST=YES	NC_EI_NB_TO_CPU_B_SR_N<0..1>	56
I961	NO_TEST=YES	NC_EI_CPU_B_TO_NB_CLK_P	56
I962	NO_TEST=YES	NC_EI_CPU_B_TO_NB_CLK_N	56
I963	NO_TEST=YES	NC_EI_CPU_B_TO_NB_AD<0..43>	56
I964	NO_TEST=YES	NC_EI_CPU_B_TO_NB_SR_P<0..1>	56
I965	NO_TEST=YES	NC_EI_CPU_B_TO_NB_SR_N<0..1>	56
I969	NO_TEST=YES	NC_NB_CPU_A1_INT_L	56
I972	NO_TEST=YES	NC_NB_CPU_B0_INT_L	56
I972	NO_TEST=YES	NC_NB_CPU_B1_INT_L	56
I972	NO_TEST=YES	NC_CPU_A1_QACK_L	56
I976	NO_TEST=YES	NC_CPU_B0_QACK_L	56
I974	NO_TEST=YES	NC_CPU_B1_QACK_L	56
I976	NO_TEST=YES	NC_HT_MB_TO_NB_CAD_P<8..15>	101
I976	NO_TEST=YES	NC_HT_MB_TO_NB_CAD_N<8..15>	101
I977	NO_TEST=YES	NC_HT_NB_TO_MB_CAD_P<8..15>	101
I982	NO_TEST=YES	NC_HT_NB_TO_MB_CAD_N<8..15>	101
I102	NO_TEST=YES	NC_CLK_RAI_200M_N<0>	27
I102	NO_TEST=YES	NC_CLK_RAI_200M_P<0>	27
I102	NO_TEST=YES	NC_CLK_RAI_PCIEA_N<0>	27
I104	NO_TEST=YES	NC_CLK_RAI_PCIEA_P<0>	27
I104	NO_TEST=YES	NC_CLK_RAI_PCIEB_N<0>	27
I105	NO_TEST=YES	NC_CLK_RAI_PCIEB_P<0>	27
I105	NO_TEST=YES	NC_CLK_RAI_PCIEC_N<0>	27
I105	NO_TEST=YES	NC_CLK_RAI_PCIEC_P<0>	27
I105	NO_TEST=YES	NC_A_AVREG_0	82
I105	NO_TEST=YES	NC_A_AVREG_1	82
I105	NO_TEST=YES	NC_A_AVREG_2	82
I105	NO_TEST=YES	NC_CPU_B_APSYNC	27
I105	NO_TEST=YES	NC_EI_CPU_B_SYSCLK_N	27
I105	NO_TEST=YES	NC_EI_CPU_B_SYSCLK_P	27
I105	NO_TEST=YES	NC_HT_NB_TO_MB_CLK_N<1>	101
I105	NO_TEST=YES	NC_HT_NB_TO_MB_CLK_P<1>	101
I100	NO_TEST=YES	NC_J2904_11	29
I100	NO_TEST=YES	NC_J2904_12	29
I100	NO_TEST=YES	NC_NCV1009_1	55
I100	NO_TEST=YES	NC_NCV1009_2	55
I100	NO_TEST=YES	NC_NCV1009_3	55
I100	NO_TEST=YES	NC_NCV1009_4	55
I100	NO_TEST=YES	NC_NCV1009_5	55
I100	NO_TEST=YES	NC_NCV1009_ADJ	55
I100	NO_TEST=YES	NC_RAM_ARB0_REF25MHZ	27
I107	NO_TEST=YES	NC_RAM_ARB1_REF25MHZ	27
I107	NO_TEST=YES	NC_SMU_PWRSEQ_P1_0	4
I107	NO_TEST=YES	NC_SMU_PWRSEQ_P1_4	4
I116	NO_TEST=YES	RFBD<38>	88 89
I116	NO_TEST=YES	RFBD<37>	88 89
I116	NO_TEST=YES	RFBD<36>	88 89
I116	NO_TEST=YES	RFBD<34>	88 89
I116	NO_TEST=YES	RFBD<33>	88 89
I116	NO_TEST=YES	RFBD<32>	88 89
I116	NO_TEST=YES	RFBD<31>	88 89
I116	NO_TEST=YES	RFBD<30>	88 89
I117	NO_TEST=YES	RFBD<28>	88 89
I117	NO_TEST=YES	RFBD<27>	88 89
I117	NO_TEST=YES	RFBD<26>	88 89
I117	NO_TEST=YES	RFBD<25>	88 89
I117	NO_TEST=YES	RFBD<23>	88 89
I117	NO_TEST=YES	RFBD<22>	88 89
I117	NO_TEST=YES	RFBD<21>	88 89

I109	NO_TEST=YES	KPVDD2	48 50 55
I109	NO_TEST=YES	KPGND2	48 50 55
I109	NO_TEST=YES	CPU_DIODE_POS	48 55
I109	NO_TEST=YES	CPU_DIODE_NEG	48 55
I110	NO_TEST=YES	FMAXT_P	55
I110	NO_TEST=YES	FMAXT_M	55
I110	NO_TEST=YES	CORE_ISNS_P	55
I110	NO_TEST=YES	CORE_ISNS_M	55
I110	NO_TEST=YES	PPV_RUN_CPU_AVDD_R_L	48
I110	NO_TEST=YES	NC_CLK_RAI_GIGE_25MHZ	27
I110	NO_TEST=YES	NC_CLK_RAI_REFCLK_66M	27
I110	NO_TEST=YES	NC_CPU_B_TBEN_CLK_US	26
I110	NO_TEST=YES	NC_PMR_CLK_DIS_L	20
I110	NO_TEST=YES	NC_I2S2_MCLK	154
I111	NO_TEST=YES	NC_SATA_RXD_N2_C	129
I111	NO_TEST=YES	NC_SATA_RXD_P2_C	129
I111	NO_TEST=YES	NC_SATA_TXD_N2	129
I111	NO_TEST=YES	NC_SATA_TXD_P2	129
I111	NO_TEST=YES	TP_SB<29>	142
I111	NO_TEST=YES	TP_SB<28>	142
I111	NO_TEST=YES	TP_SB<27>	142
I111	NO_TEST=YES	TP_SB<26>	142
I111	NO_TEST=YES	TP_SB<25>	142
I112	NO_TEST=YES	TP_SB<24>	142
I112	NO_TEST=YES	TP_SB<23>	142
I112	NO_TEST=YES	TP_SB<22>	142
I112	NO_TEST=YES	TP_SB<21>	142
I112	NO_TEST=YES	TP_SB<20>	142
I112	NO_TEST=YES	TP_SB<19>	142
I112	NO_TEST=YES	TP_SB<18>	142
I112	NO_TEST=YES	TP_SB<17>	142
I112	NO_TEST=YES	TP_SB<16>	142
I112	NO_TEST=YES	TP_SB<15>	142
I112	NO_TEST=YES	TP_SB<14>	142
I113	NO_TEST=YES	TP_SB<13>	142
I113	NO_TEST=YES	TP_SB<12>	142
I113	NO_TEST=YES	TP_SB<11>	142
I113	NO_TEST=YES	TP_SB<10>	142
I113	NO_TEST=YES	TP_SB<9>	142
I113	NO_TEST=YES	TP_SB<8>	142
I113	NO_TEST=YES	TP_SB<7>	142
I113	NO_TEST=YES	TP_SB<6>	142
I113	NO_TEST=YES	TP_SB<5>	142
I114	NO_TEST=YES	TP_SB<4>	142
I114	NO_TEST=YES	TP_SB<3>	142
I114	NO_TEST=YES	TP_SB<2>	142
I114	NO_TEST=YES	TP_SB<1>	142
I114	NO_TEST=YES	TP_SB<0>	142
I115	NO_TEST=YES	RFBD<61>	88 89
I115	NO_TEST=YES	RFBD<60>	88 89
I115	NO_TEST=YES	RFBD<59>	88 89
I117	NO_TEST=YES	RFBD<57>	88 89
I118	NO_TEST=YES	RFBD<56>	88 89
I118	NO_TEST=YES	RFBD<54>	88 89
I118	NO_TEST=YES	RFBD<53>	88 89
I118	NO_TEST=YES	RFBD<52>	88 89
I118	NO_TEST=YES	RFBD<50>	88 89
I118	NO_TEST=YES	RFBD<49>	88 89
I118	NO_TEST=YES	RFBD<48>	88 89
I118	NO_TEST=YES	RFBD<47>	88 89
I119	NO_TEST=YES	RFBD<45>	88 89
I119	NO_TEST=YES	RFBD<44>	88 89
I119	NO_TEST=YES	RFBD<42>	88 89
I119	NO_TEST=YES	RFBD<41>	88 89
I119	NO_TEST=YES	RFBD<40>	88 89

I119	NO_TEST=YES	RFBD<126>	88 90
I120	NO_TEST=YES	RFBD<125>	88 90
I119	NO_TEST=YES	RFBD<124>	88 90
I120	NO_TEST=YES	RFBD<122>	88 90
I120	NO_TEST=YES	RFBD<121>	88 90
I120	NO_TEST=YES	RFBD<120>	88 90
I120	NO_TEST=YES	RFBD<118>	88 90
I120	NO_TEST=YES	RFBD<117>	88 90
I120	NO_TEST=YES	RFBD<116>	88 90
I121	NO_TEST=YES	RFBD<114>	88 90
I121	NO_TEST=YES	RFBD<113>	88 90
I121	NO_TEST=YES	RFBD<112>	88 90
I121	NO_TEST=YES	RFBD<110>	88 90
I121	NO_TEST=YES	RFBD<109>	88 90
I121	NO_TEST=YES	RFBD<108>	88 90
I121	NO_TEST=YES	RFBD<106>	88 90
I122	NO_TEST=YES	RFBD<105>	88 90
I122	NO_TEST=YES	RFBD<104>	88 90
I122	NO_TEST=YES	RFBD<102>	88 90
I122	NO_TEST=YES	RFBD<101>	88 90
I122	NO_TEST=YES	RFBD<100>	88 90
I122	NO_TEST=YES	RFBD<98>	88 90
I122	NO_TEST=YES	RFBD<97>	88 90
I122	NO_TEST=YES	RFBD<96>	88 90
I122	NO_TEST=YES	RFBD<95>	88 90
I122	NO_TEST=YES	RFBD<94>	88 90
I123	NO_TEST=YES	RFBD<92>	88 90
I123	NO_TEST=YES	RFBD<91>	88 90
I123	NO_TEST=YES	RFBD<90>	88 90
I123	NO_TEST=YES	RFBD<88>	88 90
I123	NO_TEST=YES	RFBD<87>	88 90
I123	NO_TEST=YES	RFBD<86>	88 90
I123	NO_TEST=YES	RFBD<85>	88 90
I124	NO_TEST=YES	RFBD<83>	88 90
I124	NO_TEST=YES	RFBD<82>	88 90
I124	NO_TEST=YES	RFBD<81>	88 90
I124	NO_TEST=YES	RFBD<79>	88 90
I124	NO_TEST=YES	RFBD<78>	88 90
I124	NO_TEST=YES	RFBD<76>	88 90
I124	NO_TEST=YES	RFBD<75>	88 90
I124	NO_TEST=YES	RFBD<74>	88 90
I125	NO_TEST=YES	RFBD<72>	88 90
I125	NO_TEST=YES	RFBD<71>	88 90
I125	NO_TEST=YES	RFBD<70>	88 90
I125	NO_TEST=YES	RFBD<69>	88 90
I125	NO_TEST=YES	RFBD<67>	88 90
I125	NO_TEST=YES	RFBD<66>	88 90
I125	NO_TEST=YES	RFBD<65>	88 90
I126	NO_TEST=YES	RFBD<62>	88 89

I80	NO_TEST=YES	TP_FBBCS1_L	87
I82	NO_TEST=YES	AUD_4V5_FB	154
I83	NO_TEST=YES	ITS_RUNNING	7
I83	NO_TEST=YES	LED801_1	8
I83	NO_TEST=YES	LED802_1	8
I84	NO_TEST=YES	PCI_CLK66M_SB_INT_R	26
I84	NO_TEST=YES	Q800_D	8
I84	NO_TEST=YES	Q800_G	8
I84	NO_TEST=YES	Q801_B	8
I84	NO_TEST=YES	Q802_B	8
I85	NO_TEST=YES	Q802_E	8
I85	NO_TEST=YES	Q803_B	8
I42	NO_TEST=YES	TP_USB2_PWREN<0>	143
I42	NO_TEST=YES	TP_USB2_PWREN<1>	143
I87	NO_TEST=YES	TP_SB_FSTEST	24
I87	NO_TEST=YES	TP_SB_PLLTEST	24
I84	NO_TEST=YES	TP_USB2_PWREN<2>	143
I85	NO_TEST=YES	TP_USB2_PWREN<3>	143
I84	NO_TEST=YES	TP_USB2_PWREN<4>	143
I85	NO_TEST=YES	TP_NEC_NTEST1	122
I85	NO_TEST=YES	TP_NEC_SMC	122
I85	NO_TEST=YES	TP_NEC_SMI_L	122
I86	NO_TEST=YES	TP_NEC_SRCLK	122
I86	NO_TEST=YES	TP_NEC_SRMOD	122
I86	NO_TEST=YES	TP_NEC_TEST	122
I88	NO_TEST=YES	UATA_DASP_L_DS	129
I126	NO_TEST=YES	RFBD<19>	88 89
I126	NO_TEST=YES	RFBD<18>	88 89
I126	NO_TEST=YES	RFBD<16>	88 89
I126	NO_TEST=YES	RFBD<15>	88 89
I126	NO_TEST=YES	RFBD<14>	88 89
I126	NO_TEST=YES	RFBD<13>	88 89
I127	NO_TEST=YES	RFBD<11>	88 89
I127	NO_TEST=YES	RFBD<10>	88 89
I127	NO_TEST=YES	RFBD<8>	88 89
I127	NO_TEST=YES	RFBD<7>	88 89
I127	NO_TEST=YES	RFBD<6>	88 89
I127	NO_TEST=YES	RFBD<5>	88 89
I127	NO_TEST=YES	RFBD<3>	88 89
I128	NO_TEST=YES	RFBD<2>	88 89
I128	NO_TEST=YES	RFBD<1>	88 89
I128	NO_TEST=YES	RAM_DQ_R<63>	61 68 70
I128	NO_TEST=YES	RAM_DQ_R<60>	61 68 70
I128	NO_TEST=YES	RAM_DQ_R<59>	61 68 70
I128	NO_TEST=YES	RAM_DQ_R<58>	61 68 70
I128	NO_TEST=YES	RAM_DQ_R<57>	61 68 70
I128	NO_TEST=YES	RAM_DQ_R<56>	61 68 70
I128	NO_TEST=YES	RAM_DQ_R<54>	61 68 70
I128	NO_TEST=YES	RAM_DQ_R<53>	61 68 70
I128	NO_TEST=YES	RAM_DQ_R<52>	61 68 70
I128	NO_TEST=YES	RAM_DQ_R<50>	61 68 70
I128	NO_TEST=YES	RAM_DQ_R<49>	61 68 70
I128	NO_TEST=YES	RAM_DQ_R<48>	61 68 70
I129	NO_TEST=YES	RAM_DQ_R<46>	61 68 70
I130	NO_TEST=YES	RAM_DQ_R<45>	61 68 70
I130	NO_TEST=YES	RAM_DQ_R<44>	61 68 70
I130	NO_TEST=YES	RAM_DQ_R<43>	61 68 70
I130	NO_TEST=YES	RAM_DQ_R<41>	61 68 70
I130	NO_TEST=YES	RAM_DQ_R<40>	61 68 70
I130	NO_TEST=YES	RAM_DQ_R<37>	61 68 70
I130	NO_TEST=YES	RAM_DQ_R<38>	61 68 70
I131	NO_TEST=YES	RAM_DQ_R<36>	61 68 70
I131	NO_TEST=YES	RAM_DQ_R<34>	61 68 70
I131	NO_TEST=YES	RAM_DQ_R<33>	61 68 70
I131	NO_TEST=YES	RAM_DQ_R<32>	61 68 70
I133	NO_TEST=YES	RAM_DQ_R<30>	61 68 69
I133	NO_TEST=YES	RAM_DQ_R<29>	61 68 69
I133	NO_TEST=YES	RAM_DQ_R<28>	61 68 69
I133	NO_TEST=YES	RAM_DQ_R<31>	61 68 69
I133	NO_TEST=YES	RAM_DQ_R<25>	61 68 69
I133	NO_TEST=YES	RAM_DQ_R<24>	61 68 69
I132	NO_TEST=YES	RAM_DQ_R<22>	61 68 69
I132	NO_TEST=YES	RAM_DQ_R<21>	61 68 69
I132	NO_TEST=YES	RAM_DQ_R<20>	61 68 69
I132	NO_TEST=YES	RAM_DQ_R<19>	61 68 69
I135	NO_TEST=YES	RAM_DQ_R<17>	61 68 69
I135	NO_TEST=YES	RAM_DQ_R<16>	61 68 69
I135	NO_TEST=YES	RAM_DQ_R<14>	61 68 69
I135	NO_TEST=YES	RAM_DQ_R<13>	61 68 69
I135	NO_TEST=YES	RAM_DQ_R<12>	61 68 69
I135	NO_TEST=YES	RAM_DQ_R<11>	61 68 69
I134	NO_TEST=YES	RAM_DQ_R<9>	61 68 69
I134	NO_TEST=YES	RAM_DQ_R<8>	61 68 69
I134	NO_TEST=YES	RAM_DQ_R<7>	61 68 69
I134	NO_TEST=YES	RAM_DQ_R<6>	61 68 69
I134	NO_TEST=YES	RAM_DQ_R<5>	61 68 69
I136	NO_TEST=YES	RAM_DQ_R<3>	61 68 69
I136	NO_TEST=YES	RAM_DQ_R<2>	61 68 69
I136	NO_TEST=YES	RAM_DQ_R<1>	61 68 69

FUNC TEST NETS

NOTES FROM TOM FUSSELMAN

PLACE TWO TEST POINTS ON TOP SIDE
FOR PP3V3_ALL AND GND
PLACE WITHIN 1 INCH OF EACH OTHER
USE FAT TRACES

I108	FUNC_TEST=TRUE	PPVCORE_CPU	50
I108	FUNC_TEST=TRUE	=PP3V3_ALL_SMU	7 28 29
I108	FUNC_TEST=TRUE	=PP5V_RUN_CPU	7 8
I108	FUNC_TEST=TRUE	SYS_POWER_BUTTON_L	28 29
I108	FUNC_TEST=TRUE	POWER_BUTTON_L	29
I108	FUNC_TEST=TRUE	RESET_BUTTON_L	29
I108	FUNC_TEST=TRUE	SMU_RESET_L	28 29
I108	FUNC_TEST=TRUE	SYS_POWERUP_L	7 12 28 50 85

TOP SIDE ONLY

I138	FUNC_TEST=TRUE	SMU_BOOT_SCLK	28 29
I138	FUNC_TEST=TRUE	SMU_BOOT_RXD	28 29
I138	FUNC_TEST=TRUE	SMU_BOOT_CE	28 29
I138	FUNC_TEST=TRUE	SMU_BOOT_CNVSS	28 29
I138	FUNC_TEST=TRUE	SMU_BOOT_TXD	28 29
I138	FUNC_TEST=TRUE	SMU_BOOT_BUSY	28 29
I108	FUNC_TEST=TRUE	SMU_MANUAL_RESET_L	29

PP1V2_ALL PP3V3_ALL PP5V_ALL

7 PP1V2_ALL FUNC_TEST=TRUE
7 PP3V3_ALL FUNC_TEST=TRUE
7 PP5V_ALL FUNC_TEST=TRUE

PP1V8_RUN PP2V5_RUN PP3V3_RUN PP12V_RUN

7 PP1V8_RUN FUNC_TEST=TRUE
7 PP2V5_RUN FUNC_TEST=TRUE
16 7 PP3V3_RUN FUNC_TEST=TRUE
7 PP12V_RUN FUNC_TEST=TRUE

PP1V5_PWRON

7 PP1V5_PWRON FUNC_TEST=TRUE

GND FUNC_TEST=TRUE

FUNC TEST 1 OF 2

SYNC_MASTER=FINO-ME SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E

SCALE NONE SHT 6 OF 154

RUN RAILS

ONLY ON IN RUN

PWRON RAILS

ON IN RUN AND SLEEP

ALL RAILS

ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)

GND RAILS

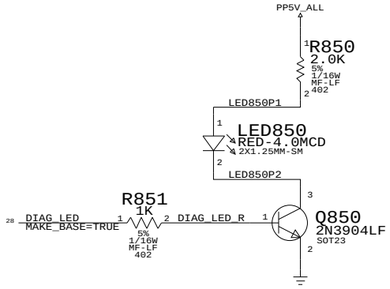
CHASSIS GND

PLANE STICHING CAPS

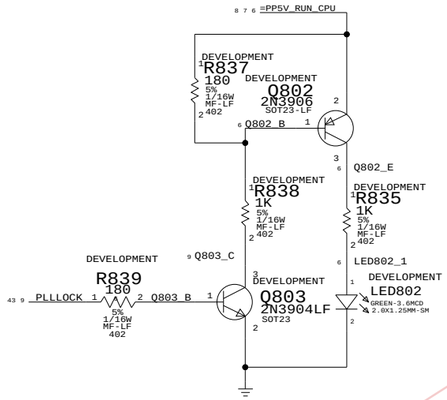
Power Conn / Alias		
SYNC_MASTER=M23-PC	SYNC_DATE=06/20/2005	
NOTICE OF PROPRIETARY PROPERTY		
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART		
APPLE COMPUTER INC.	SIZE D / DRAWING NUMBER 051-6790 / REV. E	
	SCALE NONE	SHT 7 OF 154

DIAG LED

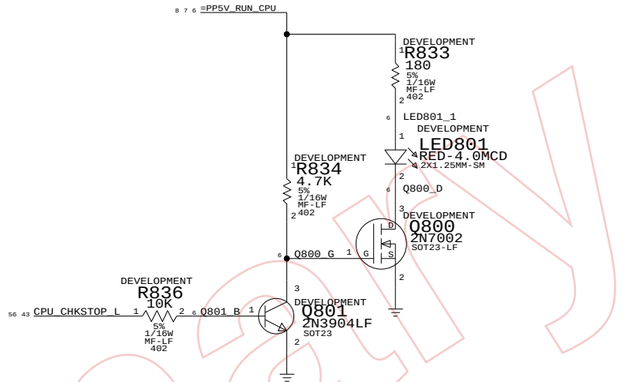
(OVERTEMP LED)



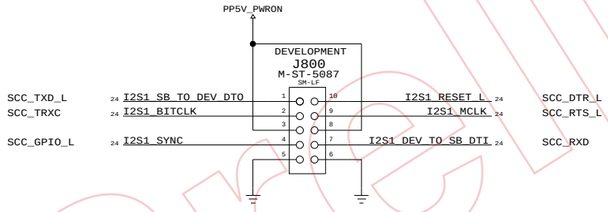
PLL LOCK LED



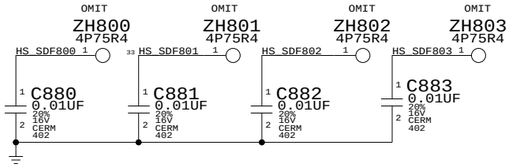
CHKSTOP LED



SERIAL DEBUG



CPU HEATSINK MOUNTING HOLES



Signal Alias

SYNC_MASTER=FINO-DD SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 8 OF 154	

J1	NO_TEST=YES	ENET_TXD_R<7>	130 131
J2	NO_TEST=YES	ENET_TXD_R<6>	130 131
J3	NO_TEST=YES	ENET_TXD_R<5>	130 131
J4	NO_TEST=YES	ENET_TXD_R<4>	130 131
J5	NO_TEST=YES	ENET_TXD_R<3>	130 131
J6	NO_TEST=YES	ENET_TXD_R<2>	130 131
J7	NO_TEST=YES	ENET_TXD_R<1>	130 131
J8	NO_TEST=YES	ENET_TXD_R<0>	130 131
J9	NO_TEST=YES	ENET_TXD<7>	130 131 132
J10	NO_TEST=YES	ENET_TXD<6>	130 131 132
J12	NO_TEST=YES	ENET_TXD<5>	130 131 132
J11	NO_TEST=YES	ENET_TXD<4>	130 131 132
J13	NO_TEST=YES	ENET_TXD<3>	130 131 132
J14	NO_TEST=YES	ENET_TXD<2>	130 131 132
J15	NO_TEST=YES	ENET_TXD<1>	130 131 132
J16	NO_TEST=YES	ENET_TXD<0>	130 131 132
J18	NO_TEST=YES	ENET_RXD_R<7>	130 131 132
J17	NO_TEST=YES	ENET_RXD_R<6>	130 131 132
J19	NO_TEST=YES	ENET_RXD_R<5>	130 131 132
J20	NO_TEST=YES	ENET_RXD_R<4>	130 131 132
J21	NO_TEST=YES	ENET_RXD_R<3>	130 131 132
J22	NO_TEST=YES	ENET_RXD_R<2>	130 131 132
J24	NO_TEST=YES	ENET_RXD_R<1>	130 131 132
J23	NO_TEST=YES	ENET_RXD_R<0>	130 131 132
J25	NO_TEST=YES	ENET_RXD<7>	130 131
J26	NO_TEST=YES	ENET_RXD<6>	130 131
J27	NO_TEST=YES	ENET_RXD<5>	130 131
J28	NO_TEST=YES	ENET_RXD<4>	130 131
J30	NO_TEST=YES	ENET_RXD<3>	130 131
J29	NO_TEST=YES	ENET_RXD<2>	130 131
J31	NO_TEST=YES	ENET_RXD<1>	130 131
J32	NO_TEST=YES	ENET_RXD<0>	130 131
J33	NO_TEST=YES	ENET_TX_EN_R	130 131
J34	NO_TEST=YES	ENET_TX_ER_R	130 131
J36	NO_TEST=YES	ENET_TX_EN	130 131 132
J35	NO_TEST=YES	ENET_TX_ER	130 131 132
J37	NO_TEST=YES	TP_HT_MB_TO_NB_CLK_N<1>	101
J38	NO_TEST=YES	TP_HT_MB_TO_NB_CLK_P<1>	101
J39	NO_TEST=YES	NC_CPU_AFN	56
J40	NO_TEST=YES	NC_I2C_SMU_CPU_SCL_IN	31
J42	NO_TEST=YES	NC_PSRO	56
J41	NO_TEST=YES	NC_PSRO_ENABLE	56
J43	NO_TEST=YES	NC_SLOT_TOTAL_PWR	31
J44	NO_TEST=YES	NC_SMU_CPU_VID_LE0	31
J45	NO_TEST=YES	NC_SMU_CPU_VID_LE1	31
J46	NO_TEST=YES	NC_SMU_FAN_RPM3	31
J48	NO_TEST=YES	NC_SMU_FAN_RPM4	31
J47	NO_TEST=YES	NC_SMU_FAN_RPM5	31
J49	NO_TEST=YES	NC_SMU_FAN_TACH3	31
J50	NO_TEST=YES	NC_SMU_FAN_TACH4	31
J51	NO_TEST=YES	NC_SMU_FAN_TACH5	31
J52	NO_TEST=YES	NC_SMU_FAN_TACH7	31
J54	NO_TEST=YES	NC_SMU_SER_SEL	31
J53	NO_TEST=YES	NC_SYS_DOOR_AJAR_L	31
J55	NO_TEST=YES	TP_VESTA_2_5V_EN	17
J56	NO_TEST=YES	TP_VESTA_AN_EN	132
J57	NO_TEST=YES	TP_VESTA_DNC_C9	17
J58	NO_TEST=YES	TP_VESTA_DNC_E9	17
J60	NO_TEST=YES	TP_VESTA_EN_10B	132
J59	NO_TEST=YES	TP_VESTA_ER	132
J61	NO_TEST=YES	TP_VESTA_F1000	132
J62	NO_TEST=YES	TP_VESTA_FDX	132
J63	NO_TEST=YES	TP_VESTA_FDXLED_L	132
J64	NO_TEST=YES	TP_VESTA_HUB	132
J66	NO_TEST=YES	TP_VESTA_LINK1_L	132
J65	NO_TEST=YES	TP_VESTA_LINK2_L	132
J67	NO_TEST=YES	TP_VESTA_MANMS	132
J68	NO_TEST=YES	TP_VESTA_PHYA<0>	132
J69	NO_TEST=YES	TP_VESTA_PHYA<1>	132
J70	NO_TEST=YES	TP_VESTA_PHYA<2>	132
J72	NO_TEST=YES	TP_VESTA_PHYA<3>	132
J71	NO_TEST=YES	TP_VESTA_PHYA<4>	132
J73	NO_TEST=YES	TP_VESTA_RBC0	132
J74	NO_TEST=YES	TP_VESTA_RBC1	132
J76	NO_TEST=YES	TP_VESTA_REGCTL1	17
J76	NO_TEST=YES	TP_VESTA_REGCTL2	17
J78	NO_TEST=YES	TP_VESTA_REGSEN1	17
J77	NO_TEST=YES	TP_VESTA_REGSEN2	17
J79	NO_TEST=YES	TP_VESTA_REGSUP1	17
J80	NO_TEST=YES	TP_VESTA_REGSUP2	17
J81	NO_TEST=YES	TP_VESTA_RGMIIEN	132
J82	NO_TEST=YES	TP_VESTA_SPD0	132
J84	NO_TEST=YES	TP_VESTA_TDBL<0>	139
J83	NO_TEST=YES	TP_VESTA_TDBL<1>	139
J85	NO_TEST=YES	TP_VESTA_TDBL<2>	139
J86	NO_TEST=YES	TP_VESTA_TEST<0>	132
J87	NO_TEST=YES	TP_VESTA_TEST<1>	132
J88	NO_TEST=YES	TP_VESTA_TEST_1394<0>	139
J90	NO_TEST=YES	TP_VESTA_TEST_1394<1>	139
J89	NO_TEST=YES	TP_VESTA_TVCO	132
J222	NO_TEST=YES	CARD_READER_ACTIVITY_R	144
J223	NO_TEST=YES	TP_VESTA_FAVDDL	139
J224	NO_TEST=YES	TP_NB_A_TRIGGER_OUT	56
J225	NO_TEST=YES	TP_NB_B_TRIGGER_OUT	56

J91	NO_TEST=YES	TP_VESTA_TVCO_24	139
J92	NO_TEST=YES	TP_VESTA_TXC_RXC_DELAY	132
J93	NO_TEST=YES	TP_I2S2_SB_TO_DEV_DTO	154
J94	NO_TEST=YES	TP_NB_APSYNC	44
J95	NO_TEST=YES	TP_SB_WATCHDOG	24
J96	NO_TEST=YES	NC_CPU_TBEN_CLK	
J97	NO_TEST=YES	NC_J3108_10	31
J98	NO_TEST=YES	NC_J3108_11	31
J99	NO_TEST=YES	NC_J3108_12	31
J100	NO_TEST=YES	NC_J3108_8	31
J101	NO_TEST=YES	NC_J3108_9	31
J102	NO_TEST=YES	NC_JTAGMUX_3	30
J103	NO_TEST=YES	NC_PP1V5_PULSAR	12

THE FOLLOWING NETS ARE USED ONLY
WHEN THE DEVELOPMENT BOM OPTION IS ENABLED

J109	NO_TEST=YES	Q803_C	8
J109	NO_TEST=YES	PLLLOCK	8 43

J111	NO_TEST=YES	LED_PP1V8_RUN_P	11
J112	NO_TEST=YES	LED_PP1V8_RUN_N	11
J113	NO_TEST=YES	PP1V5_RUN_FOR_LED	12
J114	NO_TEST=YES	LED_PP1V5_RUN_N	12
J115	NO_TEST=YES	LED_PP1V5_RUN_P	12
J116	NO_TEST=YES	PULSAR_1V5_RUN_SWITCH	12
J120	NO_TEST=YES	PP1V2_RUN_FOR_LED	13
J121	NO_TEST=YES	LED_PP1V2_RUN_N	13
J122	NO_TEST=YES	LED_PP1V2_RUN_P	13
J123	NO_TEST=YES	KP_V<1>	55
J124	NO_TEST=YES	KP_V<2>	55
J125	NO_TEST=YES	CPU_SENSE_KP_V	55
J126	NO_TEST=YES	NB_PLL_OUT_TRG_R	
J127	NO_TEST=YES	NB_PLL_OUT_TRG	59
J128	NO_TEST=YES	PP5V_T555	
J133	NO_TEST=YES	T555_DISC	
J130	NO_TEST=YES	T555_THRES	
J129	NO_TEST=YES	T555_OUT	
J132	NO_TEST=YES	T555_PWM	
J131	NO_TEST=YES	PP3V3_GPU_TSENSE	93
J134	NO_TEST=YES	TSENSE_GPU_OVERTEMP_L	93
J135	NO_TEST=YES	TSENSE_GPU_ADD0	93
J136	NO_TEST=YES	TSENSE_GPU_ADD1	93
J137	NO_TEST=YES	GPU_DIODE_PLUS	93
J138	NO_TEST=YES	GPU_DIODE_MINUS	93
J139	NO_TEST=YES	LED8700_P	136
J140	NO_TEST=YES	LED8701_P	136

THE FOLLOWING PULSAR NETS WILL BE
TESTED VIA TEST JET

J143	NO_TEST=YES	CPU_A_TBEN_CLK_R	26
J144	NO_TEST=YES	CPU_B_TBEN_CLK_R	26
J145	NO_TEST=YES	CPU_A_APSYNC_R	26
J146	NO_TEST=YES	CPU_B_APSYNC_R	26
J147	NO_TEST=YES	NB_APSYNC_R	26
J148	NO_TEST=YES	HT_SB_REFCLK_R	26
J149	NO_TEST=YES	HT_NB_REFCLK_H0_R	26
J150	NO_TEST=YES	HT_NB_REFCLK_L0_R	26
J151	NO_TEST=YES	CLK_RAIREF_200M_P_R	26
J152	NO_TEST=YES	CLK_RAIREF_200M_N_R	26
J153	NO_TEST=YES	NB_PMR_CLK_P_R	26
J154	NO_TEST=YES	NB_PMR_CLK_N_R	26
J155	NO_TEST=YES	NB_PCIE_REFCLK_P_C	26
J156	NO_TEST=YES	NB_PCIE_REFCLK_N_C	26
J157	NO_TEST=YES	GFX_SLOT_PCIE_REFCLK_P_C	26
J158	NO_TEST=YES	GFX_SLOT_PCIE_REFCLK_N_C	26
J159	NO_TEST=YES	PCIE_A_REFCLKIN_P_C	26
J160	NO_TEST=YES	PCIE_A_REFCLKIN_N_C	26
J161	NO_TEST=YES	PCIE_B_REFCLKIN_P_C	26
J162	NO_TEST=YES	PCIE_B_REFCLKIN_N_C	26
J163	NO_TEST=YES	PCIE_C_REFCLKIN_P_C	26
J164	NO_TEST=YES	PCIE_C_REFCLKIN_N_C	26
J167	NO_TEST=YES	NB_DDR_REFCLK_P_R	26
J168	NO_TEST=YES	NB_DDR_REFCLK_N_R	26
J165	NO_TEST=YES	CLK_RAI_GIGE_25MHZ_R	26
J166	NO_TEST=YES	QUA0_REF_25MHZ_R	26
J169	NO_TEST=YES	SB_CLK25M_SATA_R	26
J170	NO_TEST=YES	QUA1_REF_25MHZ_R	26
J171	NO_TEST=YES	PCI_CLK33M_SB_EXT_R	26
J172	NO_TEST=YES	SB_AIRPRT_CLK_33MHZ_R	26
J173	NO_TEST=YES	CLK_RAI_REFCLK_66M_R	26
J174	NO_TEST=YES	SB_USB2_CLK_33MHZ_R	26

THE FOLLOWING NETS DO NOT HAVE
TEST POINT BECAUSE OF ROUTING DENSITY
AND SIGNAL INTEGRITY.
TEST COVERAGE WILL BE BY FCT
NOTE FOR SHARING: DO NOT INCLUDE THIS LIST UNTIL
PCB LAYOUT ADDS TEST POINTS. THIS LIST IS A RESULT OF PCB
LAYOUT HAVING DIFFICULTY PLACING TEST POINTS ON THESE NETS

J177	NO_TEST=YES	100M_N<0>	82 97
J178	NO_TEST=YES	100M_P<0>	82 97
J179	NO_TEST=YES	CKA_N<0>	84 97
J179	NO_TEST=YES	CKA_P<0>	84 97
J177	NO_TEST=YES	HT_NB_N<0>	98 101
J178	NO_TEST=YES	HT_NB_P<0>	98 101
J179	NO_TEST=YES	HT_NB_REFCLK_NF<0>	98 101
J180	NO_TEST=YES	HT_NB_REFCLK_PF<0>	98 101
J185	NO_TEST=YES	HT_NB_TO_SB_CAD_N<0..7>	101
J186	NO_TEST=YES	HT_NB_TO_SB_CAD_P<0..7>	101
J183	NO_TEST=YES	HT_NB_TO_SB_CLK_P<0>	101
J184	NO_TEST=YES	HT_NB_TO_SB_CLK_N<0>	101
J181	NO_TEST=YES	HT_SB_TO_NB_CAD_N<0..7>	101
J182	NO_TEST=YES	HT_SB_TO_NB_CAD_P<0..7>	101
J187	NO_TEST=YES	HT_SB_TO_NB_CLK_P<0>	101
J188	NO_TEST=YES	HT_SB_TO_NB_CLK_N<0>	101
J189	NO_TEST=YES	PCIE_SLOTA_TO_NB_N<0..15>	9 82 84 97
J190	NO_TEST=YES	PCIE_SLOTA_TO_NB_P<0..15>	9 82 84 97
J191	NO_TEST=YES	UATA_DA<0>	127 129
J192	NO_TEST=YES	UATA_DD<1>	127 129
J193	NO_TEST=YES	UATA_DD<14>	127 129
J195	NO_TEST=YES	PCIE_NB_TO_SLOTA_N<0>	9 82 84 97
J196	NO_TEST=YES	PCIE_NB_TO_SLOTA_N<3>	9 82 84 97
J197	NO_TEST=YES	PCIE_NB_TO_SLOTA_NF<13>	9 82 97
J198	NO_TEST=YES	PCIE_NB_TO_SLOTA_NF<7>	9 82 97
J199	NO_TEST=YES	PCIE_NB_TO_SLOTA_P<1>	9 82 84 97
J200	NO_TEST=YES	PCIE_NB_TO_SLOTA_P<10>	9 82 84 97
J207	NO_TEST=YES	PCIE_NB_TO_SLOTA_PF<13>	9 82 97
J208	NO_TEST=YES	PCIE_NB_TO_SLOTA_PF<14>	9 82 97
J209	NO_TEST=YES	PCIE_NB_TO_SLOTA_NF<12>	9 82 97
J205	NO_TEST=YES	PCIE_NB_TO_SLOTA_PF<10>	9 82 97
J206	NO_TEST=YES	PCIE_NB_TO_SLOTA_PF<4>	9 82 97
J202	NO_TEST=YES	HT_MB_TO_NB_CTL_N<1>	98
J203	NO_TEST=YES	HT_MB_TO_NB_CTL_P<1>	98
J204	NO_TEST=YES	HT_NB_TO_MB_CTL_N<1>	98
J210	NO_TEST=YES	HT_NB_TO_MB_CTL_P<1>	98
J201	NO_TEST=YES	HT_NB_TO_SB_CTL_N<0>	101
J211	NO_TEST=YES	HT_SB_TO_NB_CTL_P<0>	101
J212	NO_TEST=YES	CLK_KOD_100M_NF<0>	82 97
J213	NO_TEST=YES	CLK_KOD_100M_PF<0>	82 97
J214	NO_TEST=YES	EI_CPU_TO_NB_CLK_N	43 56
J215	NO_TEST=YES	EI_CPU_TO_NB_CLK_P	43 56
J216	NO_TEST=YES	EI_CPU_TO_NB_SR_N<1>	9 43 56
J217	NO_TEST=YES	EI_CPU_TO_NB_SR_P<1>	9 43 56
J218	NO_TEST=YES	EI_NB_TO_CPU_CLK_N	43 56
J219	NO_TEST=YES	EI_NB_TO_CPU_CLK_P	43 56
J220	NO_TEST=YES	EI_NB_TO_CPU_SR_N<0>	9 43 56
J220	NO_TEST=YES	EI_NB_TO_CPU_SR_P<0>	9 43 56

J227	NO_TEST=YES	PLLTESTOUT	43 47
J228	NO_TEST=YES	UATA_DD<13>	127 129
J229	NO_TEST=YES	CPU_SPARE2	43 47
J230	NO_TEST=YES	RFBD<51>	88 89
J240	NO_TEST=YES	TP_CPU_TRIGGER_OUT	56
J260	NO_TEST=YES	UATA_DD<12>	127 129
J261	NO_TEST=YES	EI_CPU_SYSCLK_P	43 56
J262	NO_TEST=YES	EI_CPU_TO_NB_SR_N<1>	9 43 56
J263	NO_TEST=YES	EI_CPU_TO_NB_SR_P<1>	9 43 56
J264	NO_TEST=YES	EI_NB_TO_CPU_SR_N<0>	9 43 56
J265	NO_TEST=YES	EI_NB_TO_CPU_SR_P<0>	9 43 56

JTAG TEST POINTS NEED TO BE ON THE BOTTOM
OF THE BOARD
ADDING FUNC_TEST=TRUE TO THESE NETS

J270	FUNC_TEST=TRUE	TP_JTAG_SB_TCK	20
J272	FUNC_TEST=TRUE	TP_JTAG_SB_TDI	20
J273	FUNC_TEST=TRUE	TP_JTAG_SB_TDO	20
J274	FUNC_TEST=TRUE	TP_JTAG_SB_TMS	20
J280	FUNC_TEST=TRUE	JTAG_SB_TRST_L	20 24

J282	FUNC_TEST=TRUE	JTAG_NB_TCK	20 30
J284	FUNC_TEST=TRUE	JTAG_NB_TDI	20 30
J283	FUNC_TEST=TRUE	JTAG_NB_TDO	20 30
J285	FUNC_TEST=TRUE	JTAG_NB_TMS	20 30
J281	FUNC_TEST=TRUE	JTAG_NB_TRST_L	20

J230	FUNC_TEST=TRUE	TP_JTAG_VESTA_TDI	17
J240	FUNC_TEST=TRUE	TP_JTAG_VESTA_TDO	17
J233	FUNC_TEST=TRUE	TP_JTAG_VESTA_TCK	17
J242	FUNC_TEST=TRUE	TP_JTAG_VESTA_TMS	17
J243	FUNC_TEST=TRUE	TP_JTAG_VESTA_TRST_L	17

J244	FUNC_TEST=TRUE	JTAG_CPU_TCK	30 43
J246	FUNC_TEST=TRUE	JTAG_CPU_TDI	30 43
J245	FUNC_TEST=TRUE	JTAG_CPU_TDO	30 43 47
J248	FUNC_TEST=TRUE	JTAG_CPU_TMS	30 43
J247	FUNC_TEST=TRUE	JTAG_CPU_TRST_L	43 47

ADDING NO_TEST TO ALL PCIE NETS
TO AVOID STUBS
WILL GET COVERAGE IN FCT WITH A DIAG
THAT CHECKS THAT THE BUS IS 16 LANES WIDE

J240	NO_TEST=YES	PCIE_NB_TO_SLOTA_NF<0..15>	9 82 97
J250	NO_TEST=YES	PCIE_NB_TO_SLOTA_PF<0..15>	9 82 97
J251	NO_TEST=YES	PCIE_NB_TO_SLOTA_N<0..15>	9 82 84 97
J252	NO_TEST=YES	PCIE_NB_TO_SLOTA_P<0..15>	9 82 84 97
J253	NO_TEST=YES	PCIE_SLOTA_TO_NB_NF<0..15>	84 97
J254	NO_TEST=YES	PCIE_SLOTA_TO_NB_PF<0..15>	84 97
J255	NO_TEST=YES	PCIE_SLOTA_TO_NB_N<0..15>	9 82 84 97
J256	NO_TEST=YES	PCIE_SLOTA_TO_NB_P<0..15>	9 82 84 97

FUNC TEST 2 OF 2

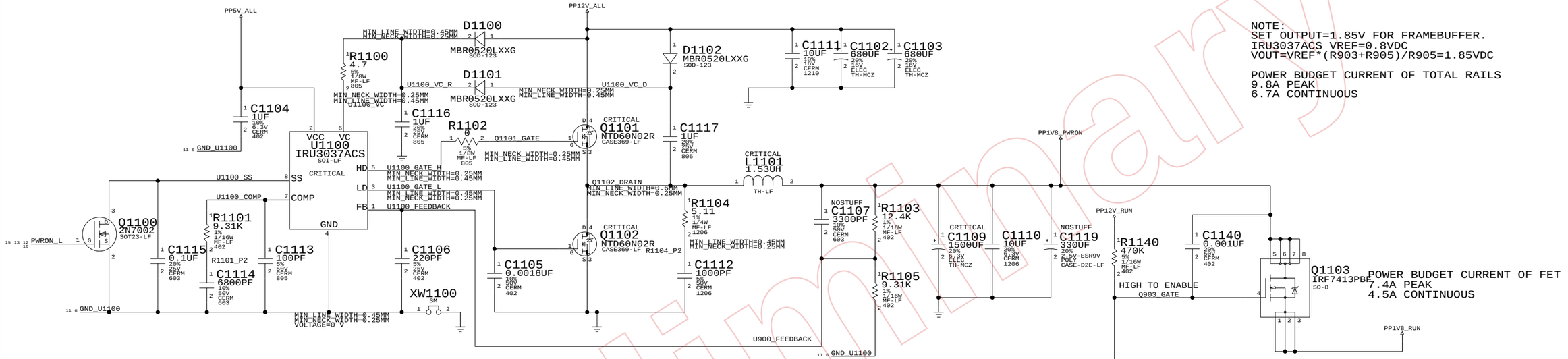
SYNC_MASTER=FINO-ME SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E

SCALE: NONE SHT 9 OF 154

1.8V VOLTAGE REGULATOR

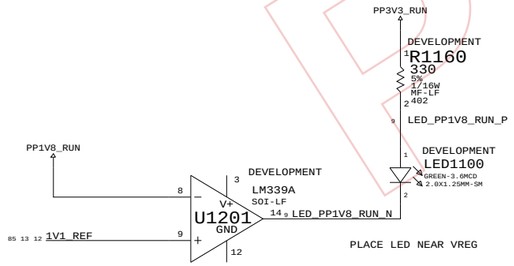


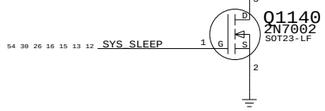
NOTE:
SET OUTPUT=1.85V FOR FRAMEBUFFER.
IRU3037ACS VREF=0.8VDC
VOUT=VREF*(R903+R905)/R905=1.85VDC

POWER BUDGET CURRENT OF TOTAL RAILS
9.8A PEAK
6.7A CONTINUOUS

POWER BUDGET CURRENT OF FET
7.4A PEAK
4.5A CONTINUOUS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0340	376S0388		Q1101,Q1102	





1.8V Vreg

SYNC_MASTER=M23-PC SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E

SCALE: NONE SHT 11 OF 154

KODIAK CORE VOLTAGE REGULATOR

NOTE:

IRU3037ACS VREF=0.8VDC
VOUT=VREF*(R1203+R1205)/R1205=1.25VDC

LOAD FROM POWER BUDGET
8.5A PEAK CURRENT DRAW
7.2A CONTINUOUS CURRENT DRAW

1.35V	R1205=2.87K
1.30V	R1205=3.24K
1.25V	R1205=3.65K

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0340	376S0388		Q1201,Q1202	

PP5V_ALL
PP12V_ALL
PP1V5_PWRON
GND_U1200
U1200_VC
U1200_VC_R
U1200_VC_D
U1200_SS
U1200_COMP
U1200_GATE_H
U1200_GATE_L
U1200_FEEDBACK
Q1201_GATE
Q1202_DRAIN
R2204_P2
R1201_P2
PWRON_L
TURN_ON_PP1V5_L
TURN_ON_PP1V2_L
1V1_REF
SYS_SLEEP
Q1250G
PP1V5_RUN_FOR_LED
LED_PP1V5_RUN_N
LED_PP1V5_RUN_P
PP3V3_RUN
PP1V5_RUN
PP3V3_PWRON
PP12V_RUN
PULSAR_1V5_RUN_SWITCH
SYS_POWERUP_L
U1270_NOISE
U1270_CONT
PP1V5_PWRON_PULSAR
NC_PP1V5_PULSAR

D1200 MBR0520LXXG SOD-123
D1201 MBR0520LXXG SOD-123
D1202 MBR0520LXXG SOD-123
R1200 10 5% 1/8W MF-LF 805
R1202 0 5% 1/8W MF-LF 805
U1200 IRU3037ACS SOI-LF CRITICAL
Q1200 2N7002 SOT23-LF
Q1201 NTD60N02R CASE369-LF CRITICAL
Q1202 NTD60N02R CASE369-LF CRITICAL
L1201 1.53UH SM CRITICAL
R1204 5.11 1% 1/4W MF-LF 1206
R1203 2.05K 1% 1/10W MF-LF 402
R1205 2.87K 1% 1/10W MF-LF 402
R1206 0 5% 1/16W MF-LF 402 NOSTUFF
R1207 0 5% 1/16W MF-LF 402
R1201 15.8K 1% 1/16W MF-LF 402
XW1200 SM
C1201 10UF 10% 16V CERM 1210
C1210 10UF 10% 16V CERM 1210
C1202 680UF 20% 16V ELEC TH-MCZ
C1204 1UF 10% 6.3V CERM 402
C1216 1UF 10% 25V X5R 603
C1217 1UF 20% 25V CERM 805
C1214 0.1UF 20% 16V CERM 603
C1213 56PF 5% 50V CERM 402
C1215 6800PF 10% 50V CERM 603
C1206 220PF 5% 25V CERM 402
C1205 0.0018UF 10% 50V CERM 402
C1212 1000PF 5% 50V CERM 1206
C1207 1UF 20% 10V CERM 603 NOSTUFF
C1208 1500UF 20% 6.3V ELEC TH-MCZ CRITICAL
C1209 1500UF 20% 6.3V ELEC TH-MCZ CRITICAL
C1218 10UF 10% 6.3V X5R 805

MIN_LINE_WIDTH=0.45MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=0 V

TURNING ON PP2V5_PWRON WITH 1V2_PWRON
SO THAT 1.5V IS THE FIRST RAIL UP ON KODIAK

LOAD FROM POWER BUDGET
1.3A PEAK CURRENT DRAW
1.0A CONTINUOUS CURRENT DRAW

PP5V_PWRON
C1250 0.1UF 20% 10V CERM 402
R1250 100K 5% 1/16W MF-LF 402
Q1250 SI3446DV TSOP-LF CRITICAL
Q1251 2N7002 SOT23-LF
RDSON=0.012 OHM @ VGS=3.5 V
R1261 0 5% 1/16W MF-LF 402 DEVELOPMENT
U1201 LM339A SOI-LF DEVELOPMENT
R1260 330 5% 1/16W MF-LF 402 DEVELOPMENT
LED1200 GREEN-3.6MCD 2.0X1.25MM-SM DEVELOPMENT
PLACE LED NEAR VREG

PP1V5_PWRON_PULSAR

U1270 MM1571FN SOT-25A CRITICAL
C1270 1UF 20% 10V CERM 805
R1270 10K 5% 1/16W MF-LF 402
C1271 0.01UF 20% 16V CERM 402
C1272 10UF 10% 6.3V X5R 805
R1273 10K 5% 1/16W MF-LF 402 DEVELOPMENT
C1275 0.01UF 20% 16V CERM 402 DEVELOPMENT
Q1271 IRLM2402PBF SOT23 DEVELOPMENT
R1274 10K 5% 1/16W MF-LF 402 DEVELOPMENT
Q1270 2N7002 SOT23-LF DEVELOPMENT
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.45MM
MIN_NECK_WIDTH=0.25MM
MAKE_BASE=TRUE

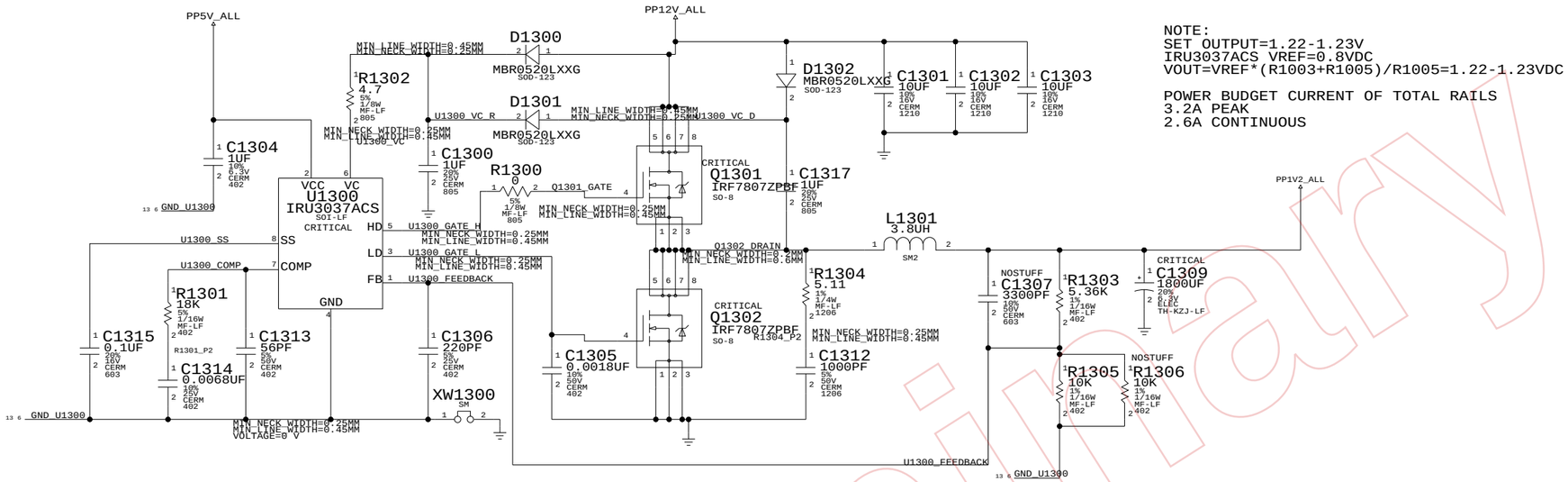
1.5V Vreg

SYNC_MASTER=FINO-PC SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 12 OF 154	

PP1V2_ALL VOLTAGE REGULATOR

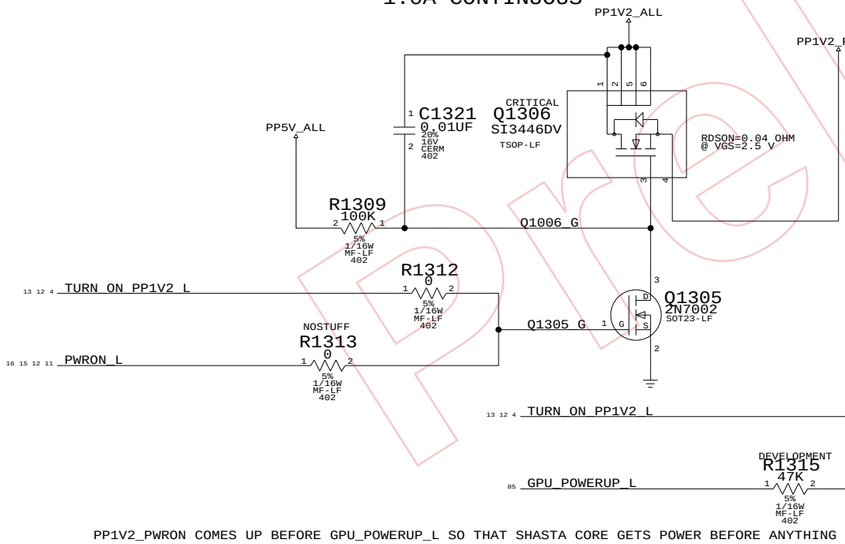


NOTE:
SET OUTPUT=1.22-1.23V
IRU3037ACS VREF=0.8VDC
VOUT=VREF*(R1003+R1005)/R1005=1.22-1.23VDC

POWER BUDGET CURRENT OF TOTAL RAILS
3.2A PEAK
2.6A CONTINUOUS

PP1V2_PWRON FET SWITCH

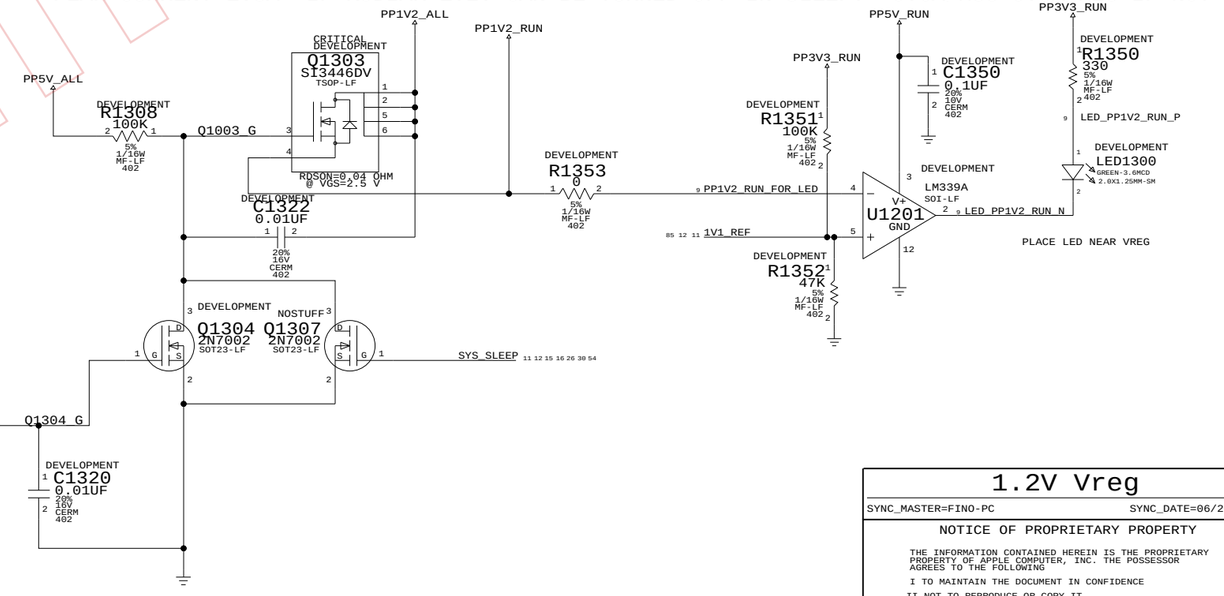
PEAK CURRENT 1.3A
1.0A CONTINUOUS



PP1V2_PWRON COMES UP BEFORE GPU_POWERUP_L SO THAT SHASTA CORE GETS POWER BEFORE ANYTHING ELSE

PP1V2_RUN FET SWITCH

PEAK CURRENT 1.3A IF KODIAK 1.2V CAN BE TURNED OFF IN SLEEP. 0.6A/M33 0.0A/M23 IF NOT

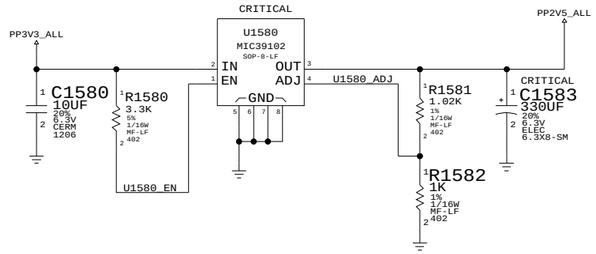


1.2V Vreg	
SYNC_MASTER=FINO-PC	SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 13 OF 154	

PP2V5_ALL VOLTAGE REGULATOR

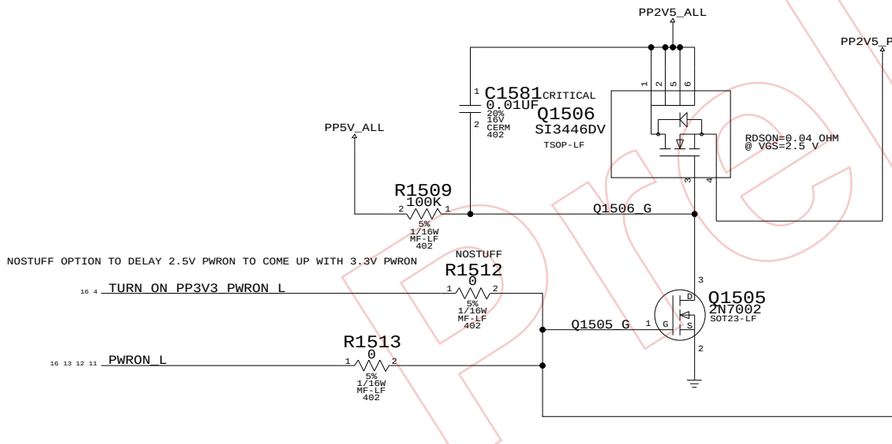


NOTE:
SET OUTPUT=2.5V
IRU3037CS VREF=1.24VDC
VOUT=VREF*(R1581+R1582)+1=5.505VDC

POWER BUDGET CURRENT OF TOTAL RAILS
0.2A PEAK
0.1A CONTINUOUS

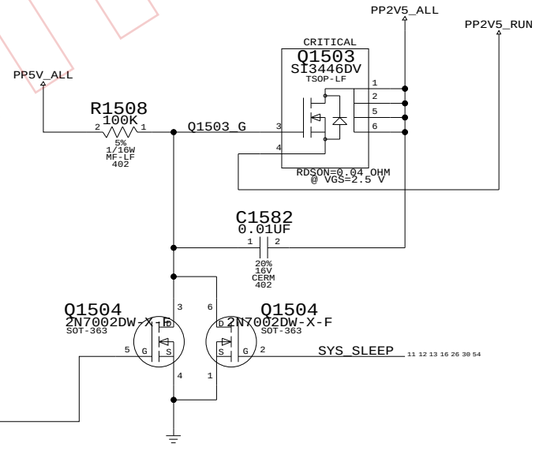
PP2V5_PWRON FET SWITCH

PEAK CURRENT 0.1A



PP2V5_RUN FET SWITCH

PEAK CURRENT 0.1A

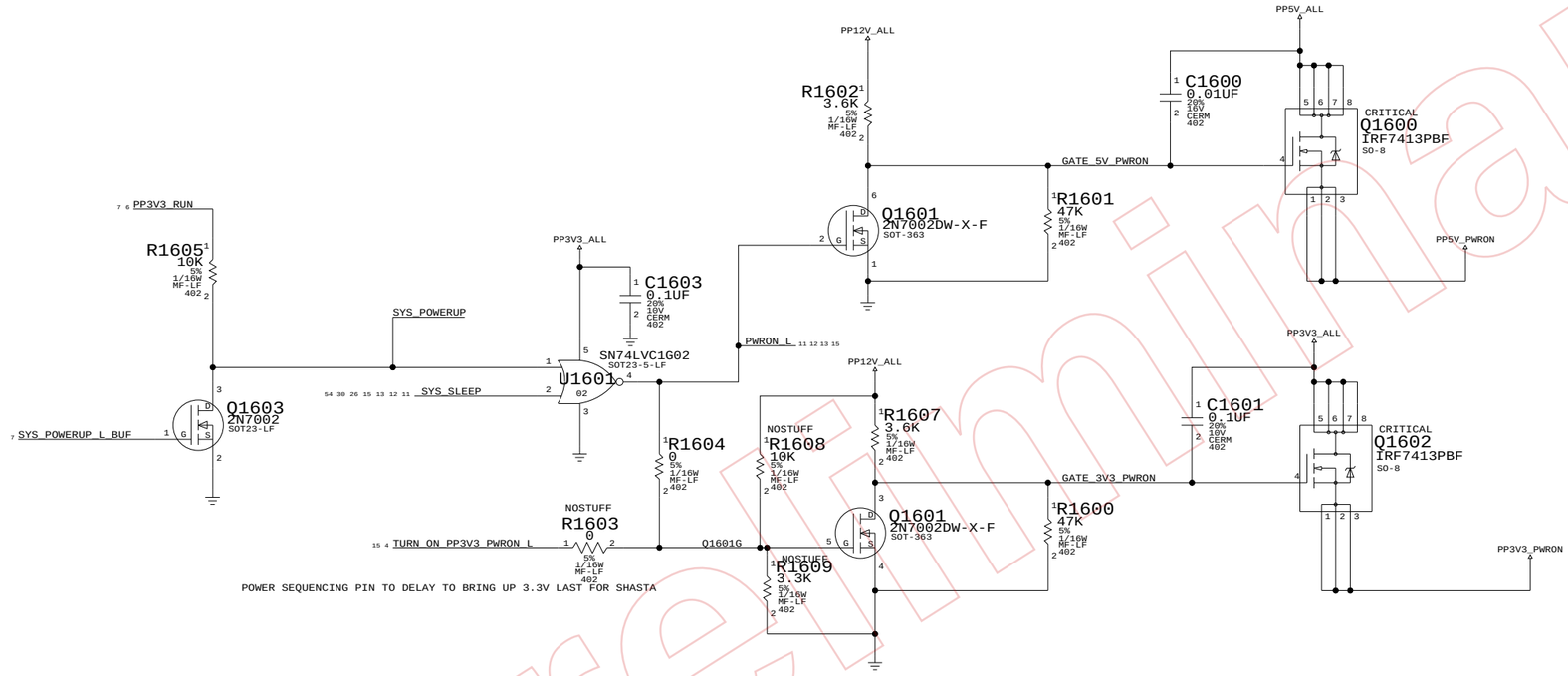


2.5V Vreg

SYNC_MASTER=FINO-PC SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 15 OF 154	



5V & 3.3V Fets

SYNC_MASTER=FINO-PC SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 16 OF 154	

Page Notes

Power aliases required by this page:

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- VESTA1V2_BURST / VESTA1V2_PULSE
  Controls operating mode of Vesta 1.2V regulator. If both options are off the regulator will be in continuous mode.

VESTA JTAG

139 132 17 7 =PP3V3_ENETFW

VESTA HAS INTERNAL PULLUPS. MLB PULLUPS MAY BE NOSTUFFED IN EVT.

R1741 1K 5% 1/16W MF-LF 402
R1742 1K 5% 1/16W MF-LF 402
R1743 1K 5% 1/16W MF-LF 402

9 TP_JTAG_VESTA_TCK	MAKE_BASE=TRUE	=JTAG_VESTA_TCK	17
9 TP_JTAG_VESTA_TDI	MAKE_BASE=TRUE	=JTAG_VESTA_TDI	17
9 TP_JTAG_VESTA_TDO	MAKE_BASE=TRUE	=JTAG_VESTA_TDO	17
9 TP_JTAG_VESTA_TMS	MAKE_BASE=TRUE	=JTAG_VESTA_TMS	17
9 TP_JTAG_VESTA_TRST_L	MAKE_BASE=TRUE	=JTAG_VESTA_TRST_L	

R1740 1K 5% 1/16W MF-LF 402

139 132 7 =PP1V2_ENETFW

L1700 FERR-EMI-600-OHM SM
PP1V2_VESTA_AVDDL
MIN_LINE_WIDTH=0.50 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.2V

C1708 10UF 10% 6.3V X5R 805
C1700 0.1uF 20% 10V CERM 402 (L6/M6)
C1701 0.1uF 20% 10V CERM 402 (L9/M9)
C1702 0.1uF 20% 10V CERM 402 (N5/N6)
C1703 0.1uF 20% 10V CERM 402 (N9/N10)

M23: PP3V3_ENETFW IS AN ALL RAIL
139 132 17 7 =PP3V3_ENETFW

R1750 10K 5% 1/16W MF-LF 402

M23: PP3V3_ENETFW IS AN ALL RAIL
139 132 17 7 =PP3V3_ENETFW

R1751 47K 5% 1/16W MF-LF 402

VESTA_RESET_RC

Q1750 2N7002DW-X-F SOT-363

C1750 1UF 10% 6.3V CERM 402

NOSTUFF
R1720 0 5% 1/16W MF-LF 402
24 ENETFW_RESET

132 VESTA_RESET_H

Q1750 2N7002DW-X-F SOT-363

C1714 10UF 10% 6.3V X5R 805
C1710 0.1uF 20% 10V CERM 402
C1711 0.1uF 20% 10V CERM 402
C1712 0.1uF 20% 10V CERM 402
C1713 0.1uF 20% 10V CERM 402

=PP3V3_ENETFW 7 17 132 139

R1752 10K 5% 1/16W MF-LF 402

RESET ASSERT REQUIREMENT IS 20MS TO 100MS

To keep Vesta from being held in reset when system is off
NOTE: Reset GPIO is active HIGH

VESTA_RESET_L
SCHMITT TRIGGER W/ INTERNAL PULLUP

VESTA MISC

SEE_TABLE
U1701
VESTA-V1.3
FBGA-200-LF
1 OF 3

17 =JTAG_VESTA_TDI	D7	TDI	IPU
17 =JTAG_VESTA_TDO	E10	TDO	
17 =JTAG_VESTA_TCK	E7	TCK	IPU
17 =JTAG_VESTA_TMS	E8	TMS	IPU
17 =JTAG_VESTA_TRST_L	D8	TRST*	IPU
9 TP_VESTA_DNC_C9	C9	DNC	
9 TP_VESTA_DNC_E9	E9	DNC	
NC C3		NC	
NC M13		NC	
	H4	RESET*	IPU

DVDD B1 B15 C15 J1
AVDDL L6 L9 M6 M9 M5 N6 N9 N10
AVDD P4 P5 P10 P11 R3 R12
PVDD A15 N4
OVDD A1 A7 F15 K1
AGND H11 H12 J11 J12 L7 L8 M7 M8 N7 N8 P6 P7 P8 P9
GND A2 B2 B7 C14 F14 J2 K2

IPD 2.5V_EN M3 TP_VESTA_2_5V_EN 9

REGSUP1	E1	TP_VESTA_REGSUP1	9
REGSEN1	F1	TP_VESTA_REGSEN1	9
REGCTL1	G5	TP_VESTA_REGCTL1	9
REGSUP2	E2	TP_VESTA_REGSUP2	9
REGSEN2	F2	TP_VESTA_REGSEN2	9
REGCTL2	G4	TP_VESTA_REGCTL2	9

M23: ADDED C1726 AND C1744 PER BROADCOM RECOMMENDATIONS

C1720 0.1uF 20% 10V CERM 402
C1721 0.1uF 20% 10V CERM 402
C1722 0.1uF 20% 10V CERM 402
C1723 0.1uF 20% 10V CERM 402
C1724 0.1uF 20% 10V CERM 402
C1725 0.1uF 20% 10V CERM 402
C1726 10UF 10% 6.3V X5R 805

=PP2V5_ENETFW 7 132 139

C1730 0.1uF 20% 10V CERM 402
C1731 0.1uF 20% 10V CERM 402

=PP3V3_ENETFW 7 17 132 139

C1740 0.1uF 20% 10V CERM 402
C1741 0.1uF 20% 10V CERM 402
C1742 0.1uF 20% 10V CERM 402
C1743 0.1uF 20% 10V CERM 402
C1744 10UF 10% 6.3V X5R 805

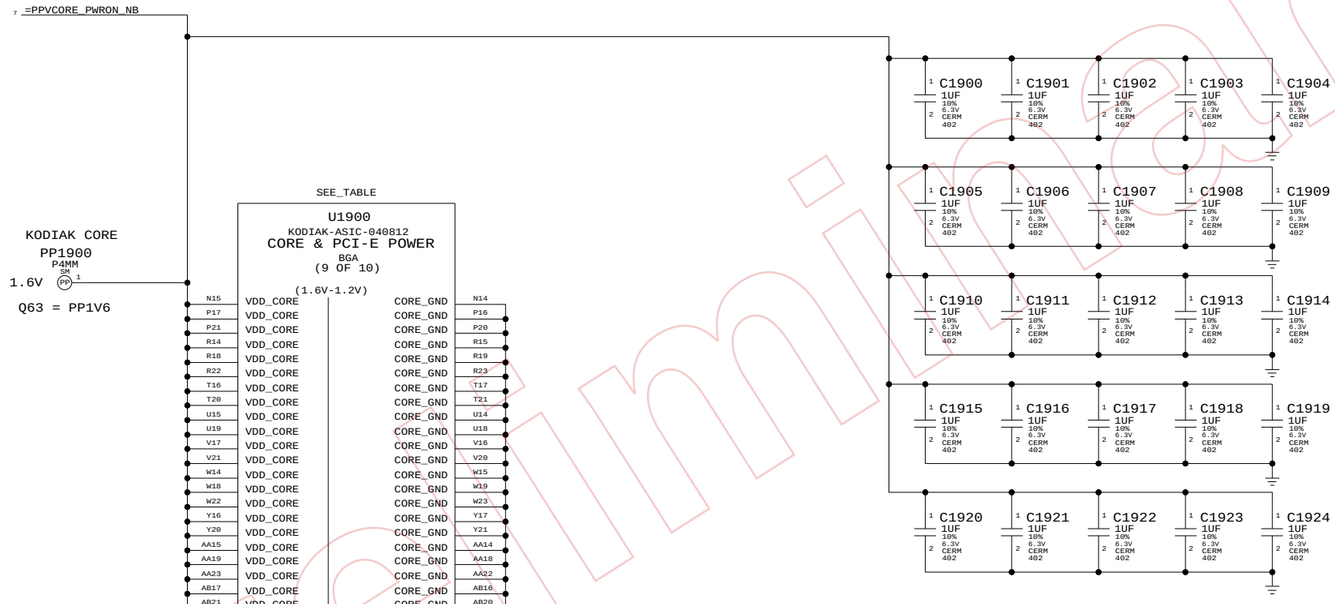
2.5V_EN
0 - OVDD=3.3V
1 - OVDD=2.5V
WHEN OVDD=2.5V GMII PINS ARE NOT 3.3V TOLERANT

Vesta Core / Misc

SYNC_MASTER=FINO-DC SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 17 OF 154	



KODIAK CORE & BYPASS

SYNC_MASTER=Q63 SYNC_DATE=08/01/2005

LAST MODIFIED=Tue Nov 1 14:55:45 2005

PAGE 19

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E

SCALE	SHT	OF
NONE	19	154

DRAWING

SHASTA ALIASES

PCI_RESET_L IS AN 'AND' OF SB_PCI_RESET_L (SB)
AND SYS_IO_RESET_L (SMU)

119 92 PCI_RESET_L — MAKE_BASE=TRUE
- =PCI_AIRPORT_RESET_L 121
- =PCI_ROM_RESET_L 125
- =PCI_USB2_RESET_L 122

24 NB_SLOT_RESET_L — MAKE_BASE=TRUE — =GPU_RESET_L 84

SHASTA JTAG

24 9 JTAG_SB_TRST_L

THESE PINS HAVE INTERNAL PULLUPS OR PULLDOWNS

9 TP_JTAG_SB_TCK	MAKE_BASE=TRUE	JTAG_SB_TCK 24
9 TP_JTAG_SB_TDI	MAKE_BASE=TRUE	JTAG_SB_TDI 24
9 TP_JTAG_SB_TDO	MAKE_BASE=TRUE	JTAG_SB_TDO 24
9 TP_JTAG_SB_TMS	MAKE_BASE=TRUE	JTAG_SB_TMS 24

R2053 4.7K 5% 1/16W MF-LF 402

SHASTA GPIO TERMINATIONS (SOME OF THESE ARE NOSTUFF ON PAGE 24)

119 56 24 23 7 =PP3V3_PWRON_SB

24 RAI_EXP_INTR_L<3>	R2061	10K 5% 1/16W MF-LF 402
24 RAI_EXP_INTR_L<2>	R2062	10K 5% 1/16W MF-LF 402
24 RAI_EXP_INTR_L<1>	R2063	10K 5% 1/16W MF-LF 402
24 RAI_EXP_INTR_L<0>	R2064	10K 5% 1/16W MF-LF 402

=PP1V8_PWRON_NBMEM 7 39 58 59

C2055 1UF 10% 6.3V CERM 402

C2055 ADDED FOR KODIAK RAM DECOUPLING
PAGE 58 IS SHORT ONE CAP

KODIAK JTAG_TRST PULLED HIGH TO ALLOW SMU DEBUG ACCESS

20 9 JTAG_NB_TRST_L

- R2073 4.7K 5% 1/16W MF-LF 402 — =PP2V5_PWRON_NB_MISC 7 20 28 30 39
- NOSTUFF R2074 0 5% 1/16W MF-LF 402 — NB_PU_RST_L 20 30
- NOSTUFF R2054 4.7K 5% 1/16W MF-LF 402

KODIAK ALIASES

6 NC_PMR_CLK_DIS_L — MAKE_BASE=TRUE — PMR_CLK_DIS_L 20

NB_OVERTEMP

30 28 7 =PP3V3_RUN_SMU

R2082 2.2 5% 1/16W MF-LF 402

C2080 1UF 10% 6.3V CERM 402

MIN_LINE_WIDTH=0.38mm
MIN_NECK_WIDTH=0.38mm
TSENSE_NB_VCC

U2080 MAX6690MEE (QSOP)
- STBY 15
- VCC 2 (CRITICAL)
- SMBDATA 12 ← 39 I2C_NB_TEMP_SDA
- SMBCLK 14 ← 39 I2C_NB_TEMP_SCL
- ALERT 11 → TSENSE_NB_OVERTEMP_L
- ADD0 10 ← TSENSE_NB_ADD0
- ADD1 6 ← TSENSE_NB_ADD1
- DXP (SYM_VER2) 3
- DXN 4
- NC_1 1, NC_5 5, NC_9 9, NC_13 13, NC_16 16
- GND 7, 8

R2083 1K 5% 1/16W MF-LF 402
NOSTUFF R2084 1K 5% 1/16W MF-LF 402
NOSTUFF R2086 1K 5% 1/16W MF-LF 402
R2085 1K 5% 1/16W MF-LF 402

NEED TO CHECK ALL I2C ADDRESSES

A0 | A1 | ADDR
0 | 0 | 30/31
0 | hiZ | 32/33
0 | 1 | 34/35
hiZ | 0 | 52/53
hiZ | hiZ | 54/55
hiZ | 1 | 56/57
1 | 0 | 9A/9B
1 | hiZ | 9A/9B
1 | 1 | 9C/9D

NOSTUFF R2087 0 5% 1/16W MF-LF 402 — SYS_OVERTEMP_L 24 28 93

C2081 0.0022UF 10% 50V CERM 402 (PLACE BY IC)

20 NB_THERM_A
MIN_LINE_WIDTH=0.25mm
MIN_NECK_WIDTH=0.25MM
DIFFERENTIAL_PAIR=TSENSE_NB
NET_PHYSICAL_TYPE=10MIL_WIDTH
NET_SPACING_TYPE=TSENSE_DIFPAIR

20 NB_THERM_K
MIN_LINE_WIDTH=0.25mm
MIN_NECK_WIDTH=0.25MM
DIFFERENTIAL_PAIR=TSENSE_NB

NET_SPACING_TYPE=TSENSE_DIFPAIR
NET_PHYSICAL_TYPE=10MIL_WIDTH

U1900 KODIAK-ASIC-040812 BGA (10 OF 10) — POWER/TEST/MISC

30 9 JTAG_NB_TCK	AJ04	CE1_LT_TCK	
30 9 JTAG_NB_TDI	AG07	CE1_MC_TDI	
30 9 JTAG_NB_TDO	AG05	CE1_B_TDO	
30 9 JTAG_NB_TMS	AL02	CE1_DI1_TMS	
20 9 JTAG_NB_TRST_L	AK06	CE1_DI2_TRST	
	AG08	CE0_TEST	
20 NB_THERM_A	F15	SYS_THDIO_D	
20 NB_THERM_K	G15	SYS_THDIO_G	
39 30 28 20 7 =PP2V5_PWRON_NB_MISC	AF02	VD5_0	
	AF05	VD5_1	
	AH01	VD5_2	
	AL01	NORTH_BRIDGE_RESET_L	NB_PU_RST_L 20 30
	AG01	HRESET_L	NB_HRST_L
	AJ03	SUSPENDACK_L	NB_SUSPEND_ACK_L 30 62
	AJ01	SUSPENDREQ_L	NB_SUSPEND_REQ_L 30
	AG04	SYS_ISCA0	I2C_NB_B_SDA 39
	AK03	SYS_ISCL0	I2C_NB_B_SCL 39
	AH06	SYS_ISCA1	I2C_NB_C_SDA 39
	AJ05	SYS_ISCL1	I2C_NB_C_SCL 39
	AG03	API_ISCA	I2C_NB_A_SDA 39
	AH03	API_ISCL	I2C_NB_A_SCL 39
	AE09	PMR_CLK_P	NB_PMR_CLK_P 26 27
	AE10	PMR_CLK_N	NB_PMR_CLK_N 26 27
	AG02	PMR_CLK_STOP_L	

39 30 28 20 7 =PP2V5_PWRON_NB_MISC

P4MM SM (PP) TP2002

R2003 1K 1% 1/16W MF-LF 402

C2050 1UF 10% 6.3V CERM 402
C2051 1UF 10% 6.3V CERM 402
C2052 1UF 10% 6.3V CERM 402

R2000 0 5% 1/16W MF-LF 402

NOSTUFF R2001 60.4 1% 1/16W MF-LF 402
NOSTUFF R2002 60.4 1% 1/16W MF-LF 402

TERM_RC

NOSTUFF C2053 1.5PF +/-0.25PF 50V CERM 402

PLACE TERM R/C CLOSE TO KODIAK

P4MM SM (PP) TP2000 — 1 6 PP_2V5PWRONNBMISC

XW2000

R2013 10K 5% 1/16W MF-LF 402

NOSTUFF R2012 0 5% 1/16W MF-LF 402

20 PMR_CLK_DIS_L — NB_PMR_CLK_STOP_L

NOTE: LOW = DISABLE PMR_CLK

NOTE:
PMR_CLK_STOP CAN BE USED TO STOP ALL CLOCKS IN KODIAK
USED FOR DEBUG
PLACE R2012 IN AN ACCESSIBLE LOCATION

KODIAK & SHASTA MISC

SYNC_MASTER=FINO-ME SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT: 20 OF 154	

Page Notes

Power aliases required by this page:
- =PP3V3_PWRON_SB_PCI64 (VIO1) (TO 5V OR 3.3V)
- =PP3V3_PWRON_SB_PCI32 (VIO2) (TO 5V OR 3.3V)
- =PP3V3_PWRON_SB
- =PP2V5_PWRON_SB
- =PP1V2_PWRON_SB_VCORE

NOTE: PCI pads use the VIO supply to meet different drive timing characteristics required by the PCI spec for 5V vs. 3.3V operation. CONNECT VIO2 TO appropriate PCI bus voltage and VIO1 TO SAME IF 64-BIT PCI, otherwise 3.3V.

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Power Sequencing:
Must power Shasta VCore rail before any other Shasta supplies.

XW2300 P4MM PP_1V2PWRONSBVCORE → PP2300
XW2303 P4MM PP_3V3PWRONSBPCI64 → PP2303
XW2304 P4MM NO_TEST=YES PP_2V5PWRONSB → PP2304

=PP1V2_PWRON_SB_VCORE
C2300–C2314 0.1uF 20% 10V CERM 402

=PP3V3_PWRON_SB
C2320–C2339 0.1uF 20% 10V CERM 402

U2300
SHASTA
V1.1
BGA-LF
(1 OF 8)
POWER
SEE_TABLE

VDDC
VDDO33
VDDO25
VIO1
VIO2
VDDP_KL
GND

Shasta max (est 06/30/03) current:

DIGITAL	1.2V	950 mA (1175 mW)
ANALOG12	1.2V	600 mA (760 mW)
VDDPs	2.5V	100 mA (250 mW)
I/O 2.5	2.5V	20 mA (60 mW)
I/O 3.3	3.3V	220 mA (770 mW)
Total:		3015 mW

=PP2V5_PWRON_SB
C2350 C2351 0.1uF 20% 10V CERM 402

=PP3V3_PWRON_SB_PCI64
C2355 C2356 C2357 0.1uF 20% 10V CERM 402
For PCI_AD<63..32>

=PP3V3_PWRON_SB_PCI32
C2360 C2361 C2362 0.1uF 20% 10V CERM 402
For PCI_AD<31..0>

=PP2V5_PWRON_SB
C2365 0.1uF 20% 10V CERM 402

Shasta Core Power

SYNC_MASTER=Q63 SYNC_DATE=08/01/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E

SCALE: NONE SHT 23 OF 154

LAST_MODIFIED=Tue Nov 1 14:55:47 2005

DRAWING

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
I2S0_TO_SB		
I2S0_TO_DEV		
I2S0_TO_DEV	AUDIO	
I2S0_BIDIR		
I2S0_BIDIR		
I2S1_TO_SB		
I2S1_TO_DEV		
I2S1_TO_DEV	0.25mm SPACING	
I2S1_BIDIR		
I2S1_BIDIR		
I2S2_TO_SB		
I2S2_TO_DEV		
I2S2_TO_DEV	0.25mm SPACING	
I2S2_BIDIR		
I2S2_BIDIR		
SB_CLK18M_XTAL	0.38mm SPACING	
	0.38mm SPACING	
	0.38mm SPACING	
SB_CLK25M_ATA	0.38mm SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	

I2S0_DEV_TO_SB_DTI 24 147
I2S0_SB_TO_DEV_DTO 24 147
I2S0_MCLK 24 154
I2S0_BITCLK 24 147
I2S0_SYNC 24 147

I2S1_DEV_TO_SB_DTI 8 24
I2S1_SB_TO_DEV_DTO 8 24
I2S1_MCLK 8 24
I2S1_BITCLK 8 24
I2S1_SYNC 8 24

I2S2_DEV_TO_SB_DTI 24 154
I2S2_SB_TO_DEV_DTO 24 154
I2S2_MCLK 24 154
I2S2_BITCLK 24 154
I2S2_SYNC 24 154

SB_CLK18M_XTALI 24
SB_CLK18M_XTALO 24
SB_CLK18M_XTALO_R 24
SB_CLK25M_SATA 24 26
NB_TO_SB_INT 24
SB_CPU_A0_INT_L 24
SB_CPU_A1_INT_L 24
SB_CPU_B0_INT_L 24
SB_CPU_B1_INT_L 24
PCI_AIRPORT_INT_L 24 121
PCI_USB2_INT_L 24 122
I2S0_RESET_L 24 147
I2S1_RESET_L 8 24
I2S2_RESET_L 24 154
MB_SLOT_RESET_L 24
NB_SLOT_RESET_L 20 24
SB_CPU_A0_SRESET_L 24 56
SB_CPU_A1_SRESET_L 24 56
SB_CPU_B0_SRESET_L 24 56
SB_CPU_B1_SRESET_L 24 56

Page Notes

Power aliases required by this page:
- _PP3V3_PCI
- _PP3V3_PWRON_SB
- _PP2V5_PWRON_SB
- _PP1V2_PWRON_SB

Signal aliases required by this page: (NONE)

BOM options provided by this page:
- PCI_64BIT: Configures Shasta for 64-bit PCI
  NOTE: XGC required for Shasta GPIOs
- MPIC_NB/MPIC_SB: Selects whether NorthBridge or SouthBridge MPIC will be used for interrupt controller.

NorthBridge / SouthBridge MPIC Routing

Re-pin within each RPAK as necessary
DO NOT swap between RPAKs

SPEC SHOWS LOAD CAPACITANCE OF 16PF FOR 197S0004

AUDIO PAGES IS RESPONSIBLE FOR TERMINATION OF I2S0 AND I2S2
DO NOT ADD PULLUP/DOWN FOR I2S0 AND IS=2S2 IN THIS PAGE

PLACE R2402 CLOSE TO SHASTA

PLACE R2432 CLOSE TO SHASTA

AUDIO GPIOS
NOTE: It is the responsibility of the audio circuit to provide the necessary pull-ups & pull-downs.

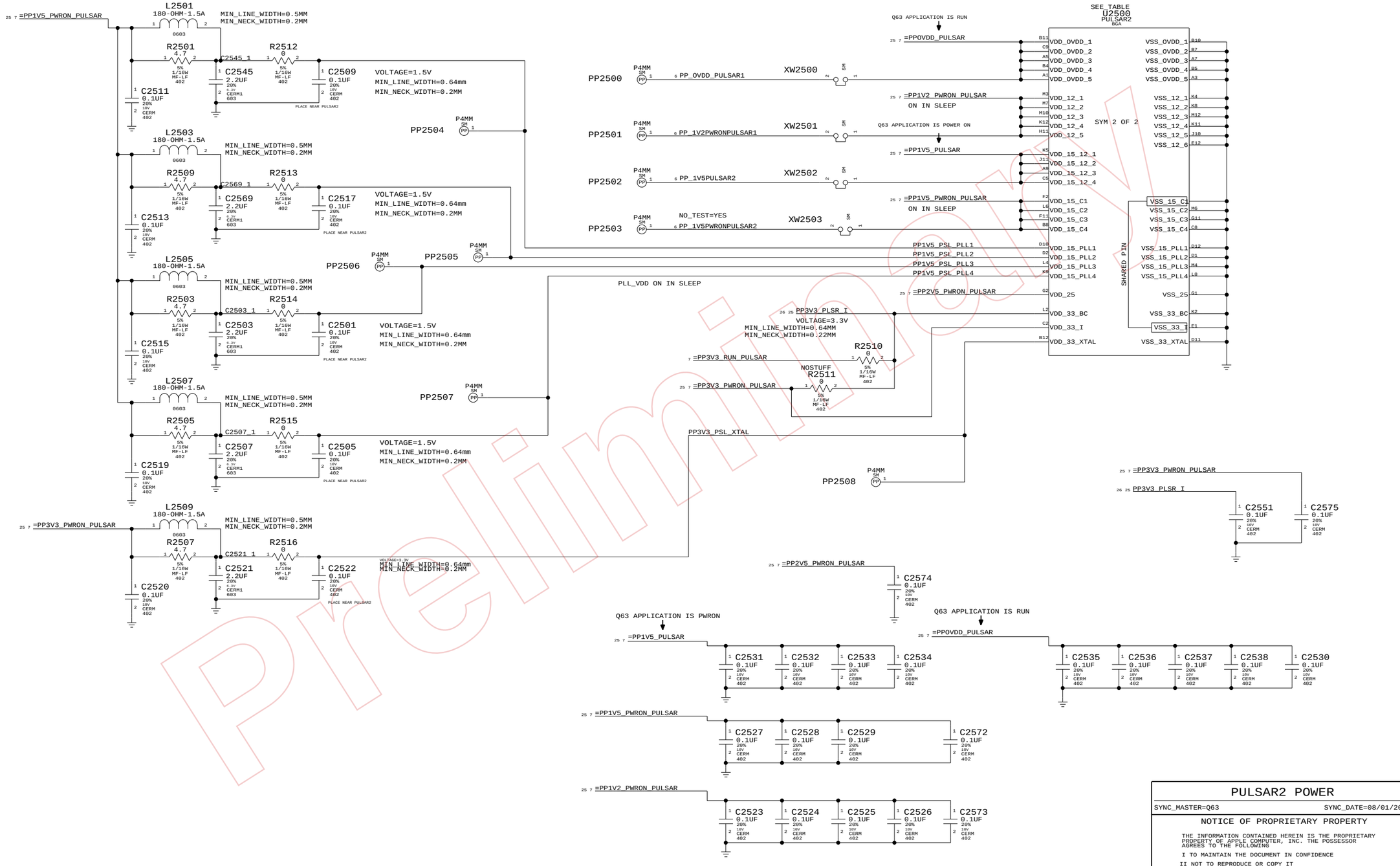
LAST_MODIFIED=Tue Nov 1 14:55:48 2005

Shasta Serial / Misc

SYNC_MASTER=FINO-ME SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 24 OF 154	



PULSAR2 POWER

SYNC_MASTER=Q63 SYNC_DATE=08/01/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 25 OF 154	

LAST_MODIFIED=Tue Nov 1 14:55:49 2005

DRAWING

PLACE ALL 0-OHM SERIES RESISTORSRES
ON THIS PAGE NEAR PULSAR

U2500
PULSAR2
BGA
SYM 1 OF 2

REMOVED R2632 AND R2630
FROM UNUSED CLOCKS FOR EMC

QUASAR CLOCKS ARE RESISTOR DIVIDED DOWN
TO 1.8V ON QUASAR PAGES

LAST MODIFIED: APR 26, 04

PULSAR2 CLOCKS		
SYNC_MASTER=FINO-ME	SYNC_DATE=06/20/2005	

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	E
	SCALE: NONE	SHT: 26	OF: 154

LAST_MODIFIED=Tue Nov 1 14:55:50 2005

DRAWING
TITLE=K31DARWA
ABSREV=SHAWING

N/C ALIASES

N/C RAINIER CLOCKS

6 NC_CLK_RAI_REFCLK_66M ═══ CLK_RAI_REFCLK_66M 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_GIGE_25MHZ ═══ CLK_RAI_GIGE_25MHZ 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_200M_P<0> ═══ CLK_RAI_200M_P<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_200M_N<0> ═══ CLK_RAI_200M_N<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_PCIEA_P<0> ═══ CLK_RAI_PCIEA_P<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_PCIEA_N<0> ═══ CLK_RAI_PCIEA_N<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_PCIEB_P<0> ═══ CLK_RAI_PCIEB_P<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_PCIEB_N<0> ═══ CLK_RAI_PCIEB_N<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_PCIEC_P<0> ═══ CLK_RAI_PCIEC_P<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_PCIEC_N<0> ═══ CLK_RAI_PCIEC_N<0> 26
MAKE_BASE=TRUE

N/C CPUB CLOCKS

6 NC_EI_CPU_B_SYSCLK_P ═══ EI_CPU_B_SYSCLK_P 26
MAKE_BASE=TRUE

6 NC_EI_CPU_B_SYSCLK_N ═══ EI_CPU_B_SYSCLK_N 26
MAKE_BASE=TRUE

6 NC_CPU_B_APSYNC ═══ CPU_B_APSYNC 26
MAKE_BASE=TRUE

N/C QUASAR CLOCKS

6 NC_RAM_ARB0_REF25MHZ ═══ RAM_ARB0_REF25MHZ 26
MAKE_BASE=TRUE

6 NC_RAM_ARB1_REF25MHZ ═══ RAM_ARB1_REF25MHZ 26
MAKE_BASE=TRUE

CLOCK CONSTRAINTS

	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	ELECTRICAL_CONSTAINT_SET	
26 20 NB_PMR_CLK_P	NB_PMR_CLK	NB_PMR_CLK	NB_PMR_CLK_SP	NB_PMR_CLK	167
26 20 NB_PMR_CLK_N	NB_PMR_CLK	NB_PMR_CLK	NB_PMR_CLK_SP	NB_PMR_CLK	168
119 26 PCI_CLK66M_SB_INT		PCI_CLK_SB	P3MM SPACING	PCI_CLK_SB	169
119 26 PCI_CLK33M_SB_EXT_RR		PCI_CLK_SB	PCI_CLK_SB	PCI_CLK_SB_CAP	170

NOTE:
ALL OTHER CLOCK CONTRAINTS ON THEIR
RESPECTIVE BUS PAGES

26 PCI_CLK33M_USB2 ═══ =PCI_CLK33M_USB2 122
MAKE_BASE=TRUE

Pulsar Aliases

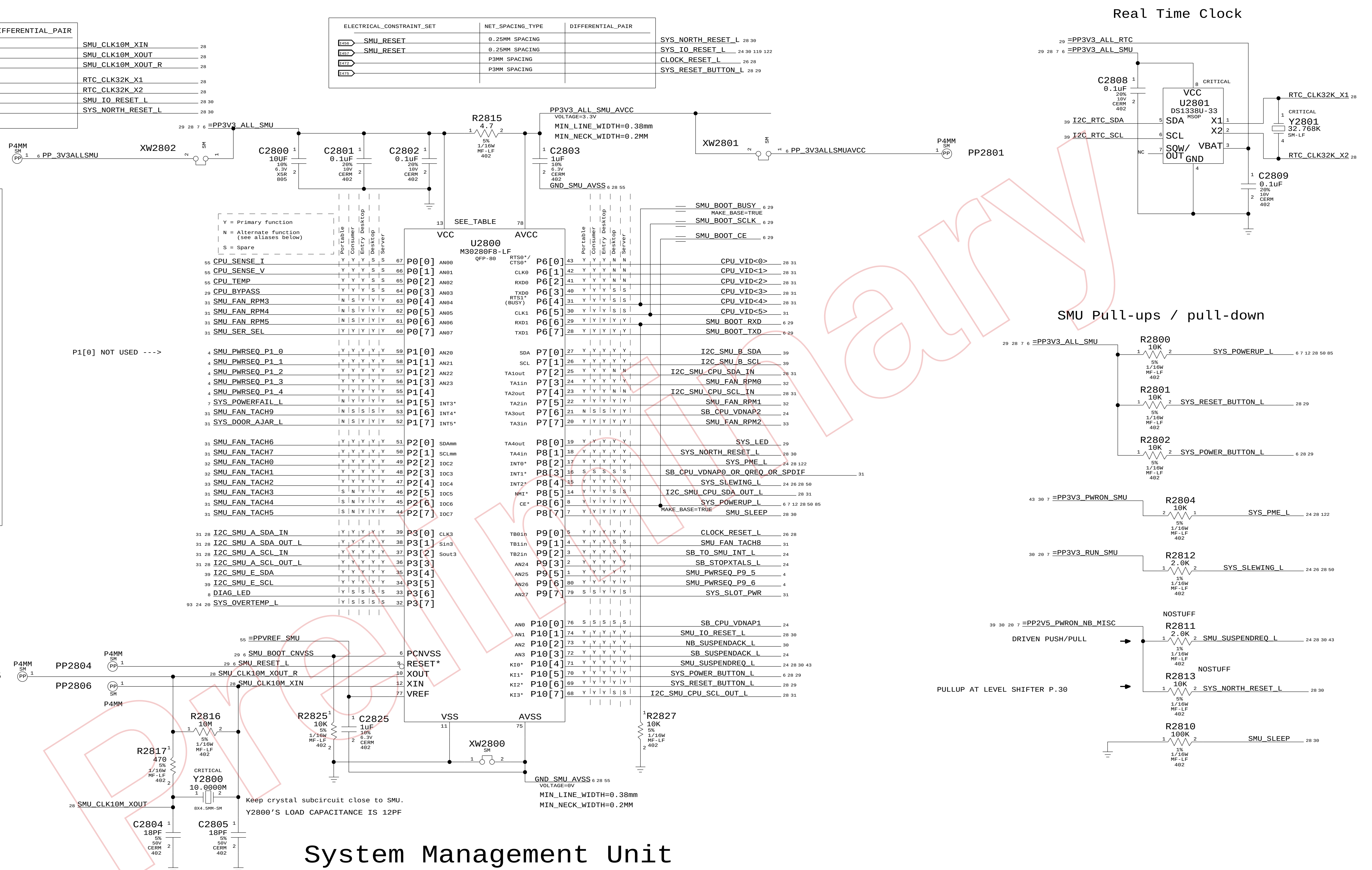
SYNC_MASTER=FINO-ME SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 27 OF 154	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	Net
SMU_CLK10M_XTAL	0.38MM SPACING		SMU_CLK10M_XIN 28
	0.38MM SPACING		SMU_CLK10M_XOUT 28
	0.38MM SPACING		SMU_CLK10M_XOUT_R 28
RTC_CLK32K_XTAL	0.38MM SPACING		RTC_CLK32K_X1 28
	0.38MM SPACING		RTC_CLK32K_X2 28
	P3MM SPACING		SMU_IO_RESET_L 28 30
	0.25MM SPACING		SYS_NORTH_RESET_L 28 30

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	Net
SMU_RESET	0.25MM SPACING		SYS_NORTH_RESET_L 28 30
SMU_RESET	0.25MM SPACING		SYS_IO_RESET_L 24 30 119 122
	P3MM SPACING		CLOCK_RESET_L 26 28
	P3MM SPACING		SYS_RESET_BUTTON_L 28 29



Page Notes

Power aliases required by this page:
- =PP3V3_ALL_SMU
- =PP3V3_ALL_RTC
- =PP3V3_PWRON_SMU
- =PPVREF_SMU (SMU AVCC OR 2.5V REFERENCE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NOTE: CPU current/voltage monitoring (CPU_SENSE_I/CPU_SENSE_V) requires 100K/10uF RC filter at SMU pins. Caps should connect to GND_SMU_AVSS. SMU_VREF should be same signal or reference used by monitoring circuit, but be aware that this will affect other analog inputs such as AC adapter ID.

NOTE: All analog inputs to SMU should have a 100pF capacitor to the SMU AVSS signal (GND_SMU_AVSS). None of those capacitors are provided on this page.

NOTE: Some primary and alternate functions reuire pull-ups that are not. provided on this page. Please. review the latest SMU specification to ensure missing pull-ups are provided on another page.

NOTE: Pinout matches SMU pinout v1.51.

System Management Unit

Alternate Functions

Tower & Server

	Signal	Port	Alternate	
31 28	CPU_VID<0>	6.0	SAT_MRESET_L	
31 28	CPU_VID<1>	6.1	CPU_A_INSERTED_L	
31 28	CPU_VID<2>	6.2	CPU_B_INSERTED_L	
31 28	I2C_SMU_CPU_SDA_IN	7.2	SMU_FAN_PWM8	
31 28	I2C_SMU_CPU_SCL_IN	7.4	SMU_FAN_PWM9	
31 28	I2C_SMU_A_SDA_IN	3.0	I2C_SMU_A_SDA	31 39
31 28	I2C_SMU_A_SDA_OUT_L	3.1	I2C_SMU_A_SCL	31 39

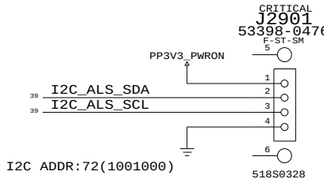
	Signal	Port	Alternate
31 28	CPU_VID<3>	6.3	SMU_FAN_RPM6
31 28	CPU_VID<4>	6.4	SMU_FAN_RPM7
31 28	I2C_SMU_A_SCL_IN	3.2	NB_TDI
31 28	I2C_SMU_A_SCL_OUT_L	3.3	NB_TCK
31 28	I2C_SMU_CPU_SDA_OUT_L	8.5	NB_TMS
31 28	I2C_SMU_CPU_SCL_OUT_L	10.7	NB_TDO_SMU

LAST_MODIFIED=Tue Nov 1 14:55:51 2005

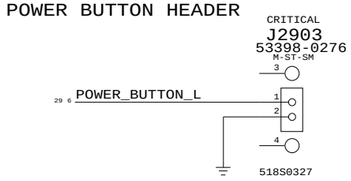
System Management Unit
SYNC_MASTER=Q63 SYNC_DATE=08/01/2005

APPLE COMPUTER INC.
SIZE D — DRAWING NUMBER 051-6790 — REV. E
SCALE NONE — SHT 28 OF 154

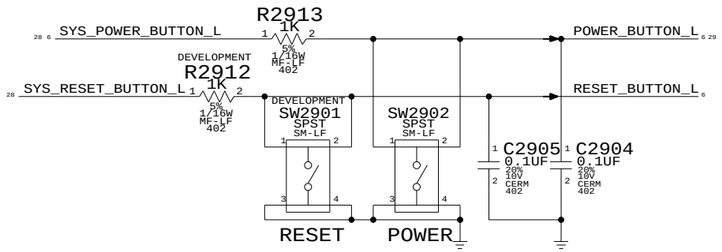
AMBIENT LIGHT SENSOR CONNECTOR



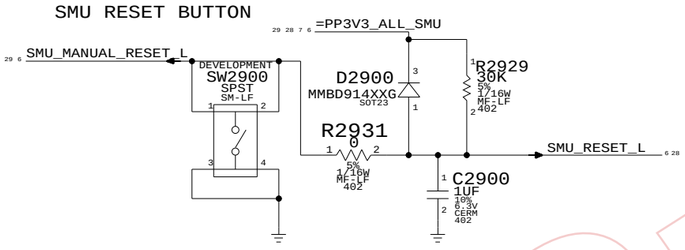
POWER BUTTON HEADER



SYS POWER AND RESET BUTTON

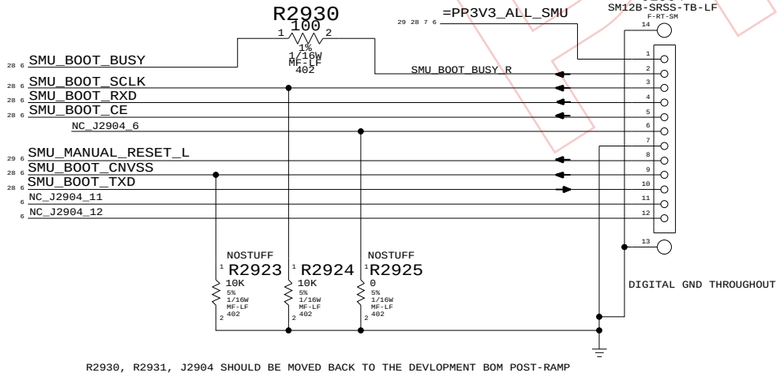


SMU RESET BUTTON



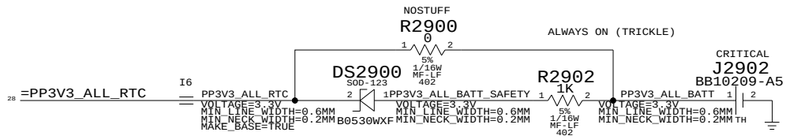
SMU DEBUG/DOWNLOAD CONNECTOR

SAME CONNECTOR AS Q63 CPU CARD FOR SAT

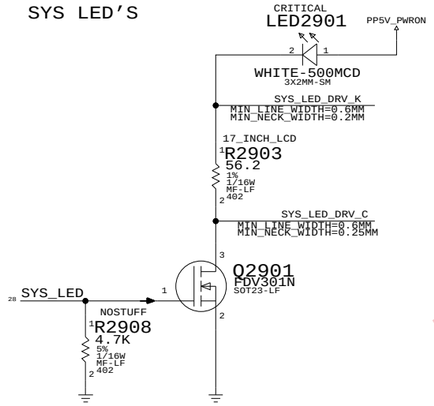


R2930, R2931, J2904 SHOULD BE MOVED BACK TO THE DEVLOPMENT BOM POST-RAMP

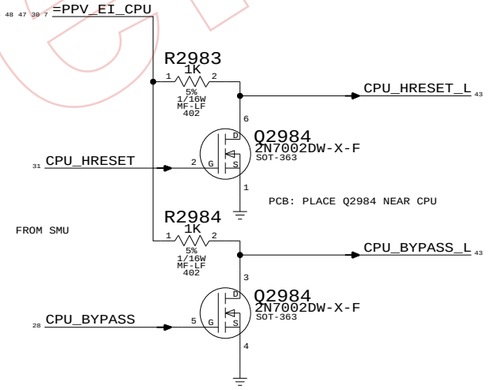
RTC BATTERY



SYS LED'S



DRIVE STRONG HRESET AND BYPASS TO CPU



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0081	1	RES, 39.2 OHM, 1%, 402, LF	R2903	20_INCH_LCD

SMU SUPPLEMENTAL (2)

SYNC_MASTER=FINO-HS SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E

SCALE	SHT	OF
NONE	29	154

SMU TO NB SUSPEND_REQ

SAME AS Q63

=PP3V3_PWRON_SMU — R3000 1K — R3003 4.7K — PMU_SUSPEND_REQ — Q03005 2N7002DW-X-F SOT-363 — SMU_SUSPENDREQ_L

=PP2V5_PWRON_NB_MISC — R3001 100 — Q03000 2N7002DW-X-F SOT-363 — NB_SUSPEND_REQ_L

NOSTUFF R3002 0 — SMU_SUSPENDREQ_L_R — NOSTUFF R3099 0

MISC. SMU BUFFERS

SAME AS (Q63).

=PP3V3_PWRON_SMU — R3021 4.7K — U700 74LC125 14TSSOP — SMU_IO_RESET_L — SYS_IO_RST_L_R — R3022 100 — SYS_IO_RESET_L

U700 IS POWERED BY PP3V3_ALL

U700 74LC125 — SMU_SLEEP — SYS_SLEEP_R — R3023 100 — SYS_SLEEP

NB SUSPEND_ACK_L LEVEL 2.5V TO 3.3V LEVEL SHIFTER

=PP3V3_PWRON_SMU — R3091 1K — R3093 1K — NB_SUSPENDACK — NB_SUSPENDACK_L

NB_SUSPEND_ACK_L_R — R3090 10K — Q03090 2N3904LF SOT23 — NB_SUSPEND_ACK_L

NOSTUFF R3092 0

Q03021 2N7002DW-X-F SOT-363

LEVEL SHIFT SMU TMS TO CPU (BACKUP PLAN)

=PPV_EI_CPU — =PP3V3_PWRON_SMU — R3026 1K — R3027 1K — JTAG_CPU_TMS_2_R — R3028 33 — JTAG_CPU_TMS

JTAG_SMU_TMS_2_R — R3020 10K — Q03030 2N3904LF SOT23 — SMU_CPU_TMS — Q03031 2N7002DW-X-F SOT-363

SMU JTAG TCK TO CPU (BACKUP PLAN)

=PPV_EI_CPU — R3081 1K — R3082 33 — JTAG_CPU_TCK

=PP3V3_RUN_SMU — R3080 4.7K — Q03081 2N7002DW-X-F SOT-363 — SMU_JTAG_TCK_L

Q03080 2N7002DW-X-F SOT-363 — SMU_JTAG_TCK

STUFF IF USING REGISTERED DIMM

=PP3V3_PWRON_SMU — NOSTUFF R3040 1K — SMU_IO_RESET — NOSTUFF Q03040 2N7002 SOT23-LF — SYS_IO_RST_L_R

SYS_NORTH_RESET FROM SMU TO NB_PU_RST

SAME AS Q63

=PP3V3_PWRON_SMU — R3006 10K — R3010 4.7K — NB_PU_RESET — Q03005 2N7002DW-X-F SOT-363 — SYS_NORTH_RESET_L

=PP2V5_PWRON_NB_MISC — R3007 4.7K — Q03000 2N7002DW-X-F SOT-363 — NB_PU_RST_L

NOSTUFF R3008 0 — SYS_NORTH_RESET_L_R — NOSTUFF R3098 0

=PP2V5_PWRON_NB_MISC — R3038 10K — JTAG_NB_TDO

NOSTUFF R3009 0 — SYS_SLEEP — SYS_2SLEEP_R

NOSTUFF Q03006 2N7002 SOT23-LF

CONSIDER COMBINING Q3040 AND Q3006 TO A DUAL PART

SMU_JTAG_TDI — R3030 0

NB JTAG IS A DEVELOPMENT ONLY FEATURE
PLACE 0-OHM R3030 AND R3031 TO AVOID STUBS
R3030,R3031,C3031,U3031,R3032,R3033 SHOULD MOVE TO DEVELOPMENT BOM POST RAMP

SMU_JTAG_TCK — R3031 0

PCB: PLACE U3030 AND U3031 NEAR CPU AND KODIAK.
PCB: PLACE 33 OHM RES NEAR U3030/31 PART.

SHARE CPU AND NB JTAG TDO WITH SMU

SMU DRIVES 3.3V PUSH-PULL ON ALL JTAG-RELATED PINS

=PP3V3_PWRON_SMU — CRITICAL — U3070 SN74LVC2G157 TSSOP — =PP3V3_RUN_SMU

PCB: PLACE U3070 NEAR SMU

JTAG_CPU_TDO_3V3 — JTAG_NB_TDO — SMU_CPU_NB_SEL — VIH=2V — C3070 0.1UF — SMU_JTAG_TDO — NC_JTAGMUX_3

SMU JTAG TDI TO CPU (BACKUP PLAN)

=PPV_EI_CPU — R3084 1K — R3085 33 — JTAG_CPU_TDI_2_R — JTAG_CPU_TDI

R3083 4.7K — Q03081 2N7002DW-X-F SOT-363 — SMU_JTAG_TDI_L

SMU_JTAG_TDI — Q03080 2N7002DW-X-F SOT-363

=PP2V5_PWRON_NB_MISC — C3031 0.1UF — R3034 10K — U3031 SN74AUC2G34 SOT23-6 — JTAG_NB_TDI_R — R3032 33 — JTAG_NB_TDI

VCC RANGE 0.8V - 2.7V

VIH = 2.0V, 3.3V TOLERANT

=PP2V5_PWRON_NB_MISC — SMU_JTAG_NB_TCK — R3035 10K — PULLUP IF KODIAK JTAG IS NOSTUFFED

U3031 — JTAG_NB_TCK_R — R3033 33 — JTAG_NB_TCK

SHARE CPU AND NB JTAG TMS WITH SMU

=PP2V5_PWRON_NB_MISC — C3071 0.1UF

PCB: PLACE U3071 NEAR SMU OR NEAR KODIAK.

CRITICAL

U3071 74LVC1G SC70-6

TO LEVEL SHIFTER — SMU_CPU_TMS

3.3V TOLERANT

SMU_JTAG_TMS — STRAIGHT TO NB — JTAG_NB_TMS

LEVEL SHIFT TDO FROM CPU TO MUX

=PP3V3_PWRON_SMU — R3051 1K — R3052 100 — JTAG_CPU_TDO_L — JTAG_CPU_TDO_3V3

JTAG_CPU_TDO_R — R3050 10K — Q03050 2N3904LF SOT23 — JTAG_CPU_TDO

Q03021 2N7002DW-X-F SOT-363

PCB: PLACE R3050, Q3050, R3051 NEAR CPU. PLACE Q3021, R3052 NEAR SMU.

PULLDOWNS TO BUFFERS/LOGIC GATES

R3036 100K — SMU_JTAG_TDI

R3037 100K — SMU_JTAG_TCK

R3070 100K — SMU_JTAG_TMS

R3071 100K — SMU_CPU_NB_SEL

LEFTOVER FROM UNUSED PRIMARY PLAN - NOT STUFFED

NOSTUFF U5640 SN74AUC1G125 VSSOP — 125

SHARE SMU JTAG TCK WITH CPU AND NB (PRIMARY PLAN)
SHARE SMU JTAG TDI WITH CPU AND NB (PRIMARY PLAN)
NOTE: WE WENT WITH BACKUP PLAN, PRIMARY REMOVED TO AVOID STUBS

SMU SUPPLEMENTAL (3)

SYNC_MASTER=FINO-HS SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 30 OF 154	

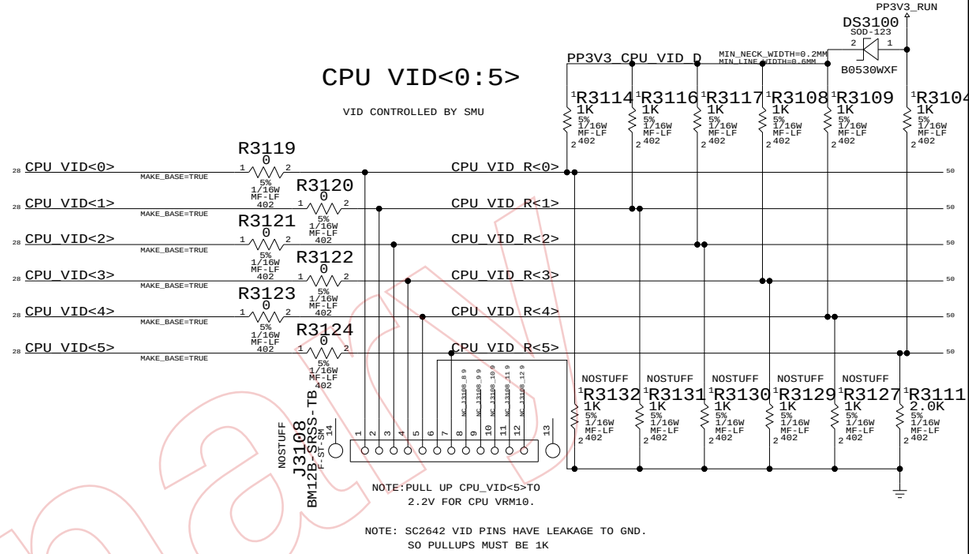
SMU ALIASES

ALIASES ARE ONLY NECESSARY WHERE USE DIFFERS FROM Q63.

COMMENT (ONLY IF USE DIFFERS FROM Q63)	M23 NET NAME	M23 SMU ALLOCATION	Q63 NET NAME (SHARED PAGE)
		CPU_SENSE_I0 P0.0	
		CPU_SENSE_V0 P0.1	
		CPU_TEMP0 P0.2	
Q63 NC'S THESE AS IT USES A SAT.		CPU_BYPASS P0.3	
	9 NC_SMU_FAN_RPM3	FAN_CNTL0_4 P0.4 MAKE_BASE=TRUE	SMU_FAN_RPM3 28
M23/M33 DOESN'T HAVE THOSE FANS.	9 NC_SMU_FAN_RPM4	FAN_CNTL0_5 P0.5 MAKE_BASE=TRUE	SMU_FAN_RPM4 28
	9 NC_SMU_FAN_RPM5	FAN_CNTL0_6 P0.6 MAKE_BASE=TRUE	SMU_FAN_RPM5 28
Q63 USES SMU_SER_SEL FOR SPDIF-SMU-DEBUG. NOT M23/M33 FEATURE.	9 NC_SMU_SER_SEL	SMU_SCCL_SEL P0.7 MAKE_BASE=TRUE	SMU_SER_SEL 28
M23/M33 DOESN'T USE. P1.0 NC ON PG 7.		CPU_SENSE_I1 P1.0	
		CPU_SENSE_V1 P1.1	
SMU USES P1.1, P1.2, P1.3, P9.5, P9.6 FOR PWRSEQ ON PG 7.		CPU_TEMP1 P1.2	
		PS1_3 P1.3	
M23/M33 DOESN'T USE P1.4. NC ON PG 7.		PS1_4 P1.4	
		POWERFAIL* P1.5	
CPU_VID_LE0 FOR Q82. NOT M23/M33 FEATURE.	9 NC_SMU_CPU_VID_LE0	CPU_VID_LE0 P1.6 MAKE_BASE=TRUE	SMU_FAN_TACH9 28
CONSIDER DOOR_AJAR FOR M23/M33 DIMM ACCESS DOOR?	9 NC_SYS_DOOR_AJAR_L	DOOR_AJAR* P1.7 MAKE_BASE=TRUE	SYS_DOOR_AJAR_L 28
CPU_VID_LE1 FOR Q82. NOT M23/M33 FEATURE.	9 NC_SMU_CPU_VID_LE1	CPU_VID_LE1 P2.0 MAKE_BASE=TRUE	SMU_FAN_TACH6 28
M23/M33 DOESN'T HAVE THIS FAN.	9 NC_SMU_FAN_TACH7	FAN_TACH2_1 P2.1 MAKE_BASE=TRUE	SMU_FAN_TACH7 28
		FAN_TACH2_2 P2.2	
		FAN_TACH2_3 P2.3	
		FAN_TACH2_4 P2.4	
M23/M33 DOESN'T HAVE FAN TACHS P2.5, P2.6, P2.7.	9 NC_SMU_FAN_TACH3	FAN_TACH2_5 P2.5 MAKE_BASE=TRUE	SMU_FAN_TACH3 28
M23/M33 USES TACH0 (P2.2), TACH1 (P2.3), TACH2 (P2.4) ONLY.	9 NC_SMU_FAN_TACH4	FAN_TACH2_6 P2.6 MAKE_BASE=TRUE	SMU_FAN_TACH4 28
	9 NC_SMU_FAN_TACH5	FAN_TACH2_7 P2.7 MAKE_BASE=TRUE	SMU_FAN_TACH5 28
M23/M33 ONLY CONNECTS I2C TO KODIAK NOW; CPU HAS PULLUPS ON ITS PG.	39 28 I2C_SMU_A_SDA	IIC_A_DAT P3.0 MAKE_BASE=TRUE	I2C_SMU_A_SDA_IN 28
	39 28 I2C_SMU_A_SCL	IIC_A_CLK P3.1 MAKE_BASE=TRUE	I2C_SMU_A_SDA_OUT_L 28
	30 SMU_JTAG_TDI	TDI P3.2 MAKE_BASE=TRUE	I2C_SMU_A_SCL_IN
	30 SMU_JTAG_TCK	TCK P3.3 MAKE_BASE=TRUE	I2C_SMU_A_SCL_OUT_L 28
		IIC_E_DAT P3.4	
		IIC_E_CLK P3.5	
		DIAG_LED P3.6	
		OVERTEMP* P3.7	
		CPU_VID[0] P6.0	
		CPU_VID[1] P6.1	
		CPU_VID[2] P6.2	
		CPU_VID[3] P6.3	
		CPU_VID[4] P6.4	
		CPU_VID[5] P6.5	
		DEBUG_RXD P6.6	
		DEBUG_TXD P6.7	
		IIC_B_DAT P7.0	
		IIC_B_CLK P7.1	
Q63 USE OF P7.2 IS PWM FAN / SELECT BETWEEN CPU OR NB TMS AND TDO FROM/TO SMU	38 SMU_CPU_NB_SEL	CPU_TMS P7.2 MAKE_BASE=TRUE	I2C_SMU_CPU_SDA_IN 28
		FAN_CNTL7_3 P7.3	
M23/M33 DOESN'T HAVE THIS FAN (P7.4)	9 NC_I2C_SMU_CPU_SCL_IN	FAN_CNTL7_4 P7.4 MAKE_BASE=TRUE	I2C_SMU_CPU_SCL_IN 28
M23/M33 USES FAN_RPM0 (P7.3), FAN_RPM1 (P7.5), FAN_RPM2 (P7.7) ONLY.		FAN_CNTL7_5 P7.5	
		VDNAP2 P7.6	
		FAN_CNTL7_7 P7.7	
		SYSTEM_LED P8.0	
		NB_RESET* P8.1	
		PME* P8.2	
M23/M33 DOESN'T NEED TO MAKE VDNAP0 DO TRIPLE-DUTY.	24 SB_VDNAP0	VDNAP0 P8.3 MAKE_BASE=TRUE	SB_CPU_VDNAP0_OR_QREQ_OR_SPDIF 28
		SLEWING* P8.4	
	30 SMU_JTAG_TMS	NB_TMS P8.5 MAKE_BASE=TRUE	I2C_SMU_CPU_SDA_OUT_L 28
		POWERUP* P8.6	
		SLEEP P8.7	
		CLK_RESET* P9.0	
Q63 USE OF P9.1 IS TACH 8.	29 CPU_HRESET	CPU_HRESET P9.1 MAKE_BASE=TRUE	SMU_FAN_TACH8 28
		SMU_DOORBELL* P9.2	
		STOP_XTAL* P9.3	
		PS9_5 P9.5	
		PS9_6 P9.6	
M23/M33 HAS NO SLOTS.	9 NC_SLOT_TOTAL_PWR	SLOT_TOTAL_PWR P9.7 MAKE_BASE=TRUE	SYS_SLOT_PWR 28
		VDNAP1 P10.0	
		IO_RESET* P10.1	
		SUSPEND_ACK* P10.2	
		SUSPEND_IO_ACK* P10.3	
		SUSPEND_REQ* P10.4	
		PWR_BUTTON* P10.5	
		RST_BUTTON* P10.6	
	30 SMU_JTAG_TDO	TDO P10.7 MAKE_BASE=TRUE	I2C_SMU_CPU_SCL_OUT_L 28

CPU VID<0:5>

VID CONTROLLED BY SMU



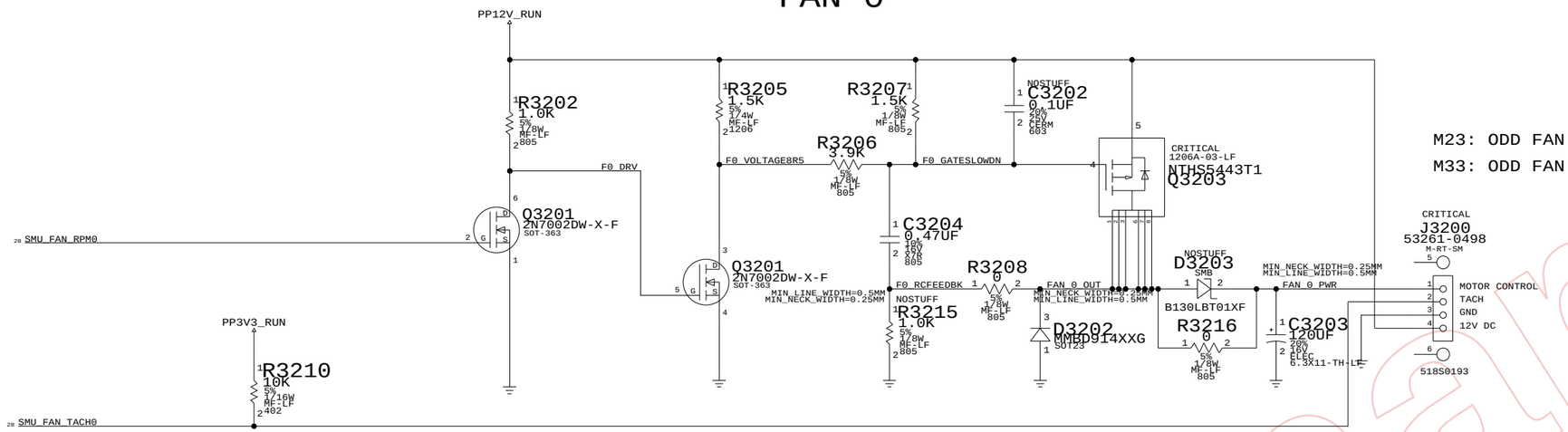
SMU SUPPLEMENTAL (4)

SYNC_MASTER=FINO-HS SYNC_DATE=06/20/2005

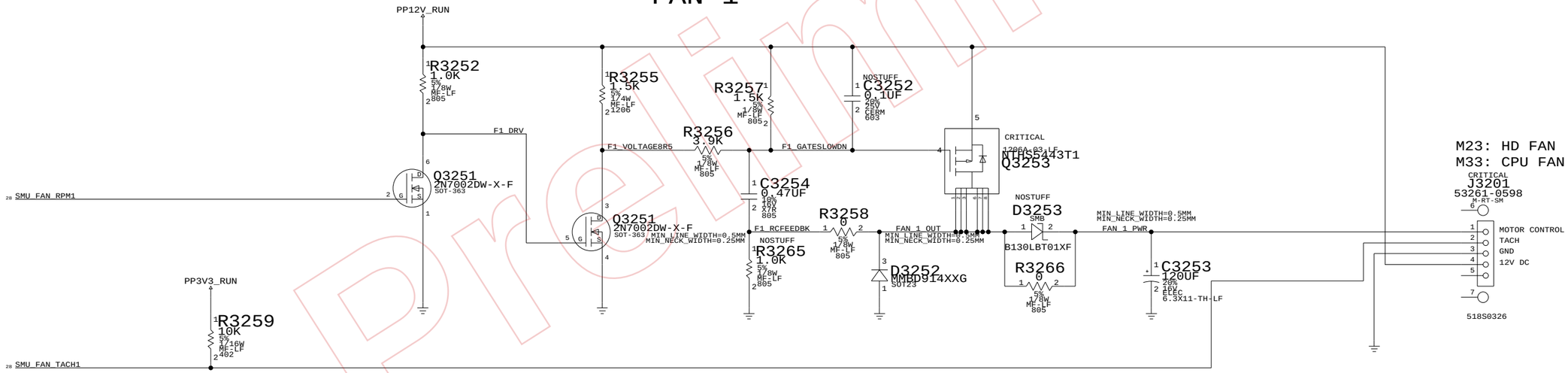
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 31 OF 154	

FAN 0



FAN 1



Fan 0, 1 & System Temp

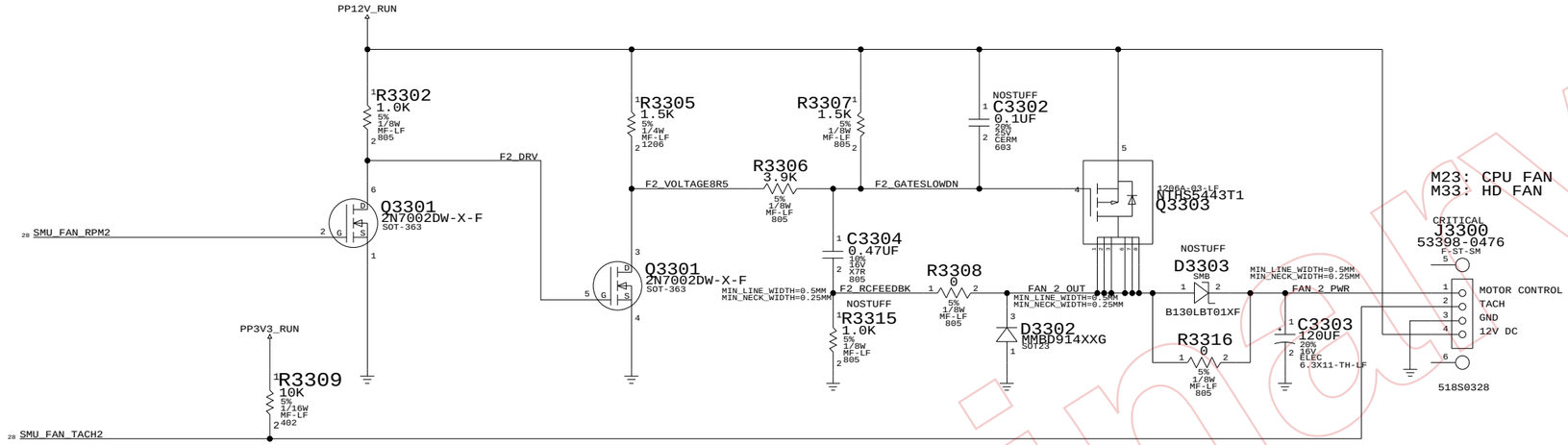
SYNC_MASTER=FINO-HS SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

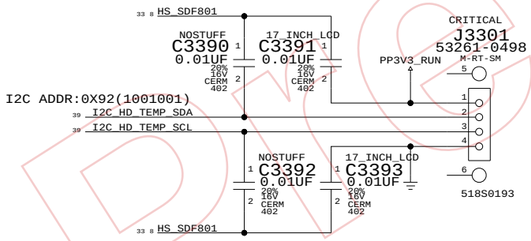
SIZE	DRAWING NUMBER	REV.
D	051-6790	E

SCALE	SHT
NONE	32 OF 154

FAN 2

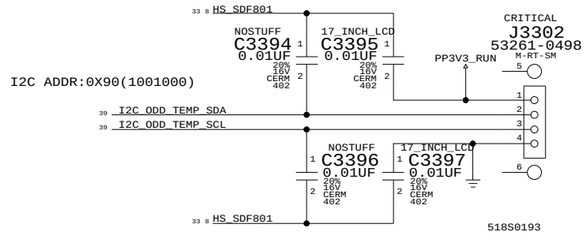


HD TEMP SENSOR



CAPS ARE FOR EMC ON M23 ONLY

ODD TEMP SENSOR



CAPS ARE FOR EMC ON M23 ONLY

Fan 2 & HD Temp

SYNC_MASTER=FINO-HS SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 33 OF 154	

SMU AND NB I2C A BUS

=PP3V3_RUN_I2C

SMU
MASTER
I2C_SMU_A_SDA — NET_SPACING_TYPE=I2C
I2C_SMU_A_SCL — NET_SPACING_TYPE=I2C

R3953 2.0K 5% 1/16W MF-LF 402
R3969 2.0K 5% 1/16W MF-LF 402
VDIV=2.9V
NOSTUFF R3954 15K 5% 1/16W MF-LF 402
NOSTUFF R3955 15K 5% 1/16W MF-LF 402

=PP2V5_RUN_I2C
R3958 2.0K 5% 1/16W MF-LF 402
R3959 2.0K 5% 1/16W MF-LF 402

KODIAK
I2C_NB_A_SDA — NET_SPACING_TYPE=I2C
I2C_NB_A_SCL — NET_SPACING_TYPE=I2C

Q3902 SI2302ADSE3 SOT23-3
Q3902_1 — R3962 0 5% 1/16W MF-LF 402 — =PP2V5_RUN_I2C
Q3901 SI2302ADSE3 SOT23-3
Q3901_1 — R3963 0 5% 1/16W MF-LF 402

SB I2C BUS

PP3V3_RUN

SHASTA
MASTER
U2300
I2C_SB_SDA MAKE_BASE=TRUE
I2C_SB_SCL MAKE_BASE=TRUE
PINS Y9, AB7

R3915 1K 5% 1/16W MF-LF 402
R3914 1K 5% 1/16W MF-LF 402

NET_SPACING_TYPE=AUDIO
NET_SPACING_TYPE=AUDIO

AUDIO
U9500 / AU300
I2C_AUDIO_SDA
I2C_AUDIO_SCL
PINS 18, 19

SMU I2C B BUS

PP3V3_PWRON

R3903 2.0K 5% 1/16W MF-LF 402
R3902 2.0K 5% 1/16W MF-LF 402

SMU
MASTER
U1300
I2C_SMU_B_SDA MAKE_BASE=TRUE
I2C_SMU_B_SCL MAKE_BASE=TRUE
PINS 26, 27

NET_SPACING_TYPE=I2C
NET_SPACING_TYPE=I2C

PULSAR2
U2600
I2C_CLOCK_B_SDA
I2C_CLOCK_B_SCL
NET_SPACING_TYPE=I2C
I2C ADDR:0XD5

R3904 33 5% 1/16W MF-LF 402

ALS HEADER
J2901
I2C_ALS_SDA
I2C_ALS_SCL
NET_SPACING_TYPE=I2C
I2C ADDR:52

R3908 33 5% 1/16W MF-LF 402

SMU I2C E BUS

PP3V3_ALL

R3907 2.0K 5% 1/16W MF-LF 402
R3906 2.0K 5% 1/16W MF-LF 402
R3965 0 5% 1/16W MF-LF 402
R3964 0 5% 1/16W MF-LF 402

SMU 'E'
MASTER
U2800
I2C_SMU_E_SDA — I2C
I2C_SMU_E_SCL — I2C
PINS 34,35

RTC
U2801
I2C_RTC_SDA — I2C
I2C_RTC_SCL — I2C
PINS 5, 6

NB I2C C BUS

=PP2V5_RUN_I2C
R3970 2.0K 5% 1/16W MF-LF 402
R3971 2.0K 5% 1/16W MF-LF 402

KODIAK I2C C
I2C_NB_C_SDA NET_SPACING_TYPE=I2C
I2C_NB_C_SCL NET_SPACING_TYPE=I2C

=PP3V3_RUN_I2C
R3972 2.0K 5% 1/16W MF-LF 402
R3973 2.0K 5% 1/16W MF-LF 402

MAKE_BASE=TRUE I2C_NB_C_3V3_SDA NET_SPACING_TYPE=I2C
MAKE_BASE=TRUE I2C_NB_C_3V3_SCL NET_SPACING_TYPE=I2C

Q3970 SI2302ADSE3 SOT23-3
Q3970_G — R3974 0 5% 1/16W MF-LF 402
Q3971 SI2302ADSE3 SOT23-3
Q3971_G — R3975 0 5% 1/16W MF-LF 402 — =PP2V5_RUN_I2C

ODD TEMP SENSOR HEADER
J3302
I2C_ODD_TEMP_SDA — R3976 33 5% 1/16W MF-LF 402
I2C_ODD_TEMP_SCL — NET_SPACING_TYPE=I2C
I2C ADDR:90

HD TEMP SENSOR HEADER
J3301
I2C_HD_TEMP_SDA — R3977 33 5% 1/16W MF-LF 402
I2C_HD_TEMP_SCL — NET_SPACING_TYPE=I2C
I2C ADDR:92

GPU TEMP SENSOR
U9390
I2C_GPU_DIODE_SDA — R3978 33 5% 1/16W MF-LF 402
I2C_GPU_DIODE_SCL — NET_SPACING_TYPE=I2C
I2C ADDR:9C

KODIAK TEMP SENSOR
U2080
I2C_NB_TEMP_SDA — R3979 33 5% 1/16W MF-LF 402
I2C_NB_TEMP_SCL — NET_SPACING_TYPE=I2C
I2C ADDR:98

NB I2C B BUS

=PP2V5_PWRON_NB_MISC
=PP1V8_PWRON_NBMEM

KODIAK I2C B
MASTER
U1900
I2C_NB_B_SDA NET_SPACING_TYPE=I2C
I2C_NB_B_SCL NET_SPACING_TYPE=I2C
PINS AG04, AK03

R3925 2.0K 5% 1/16W MF-LF 402
R3936 2.0K 5% 1/16W MF-LF 402

Q3903 SI2302ADSE3 SOT23-3
Q3903_G — R3924 0 5% 1/16W MF-LF 402
Q3904 SI2302ADSE3 SOT23-3
Q3904_G — R3937 0 5% 1/16W MF-LF 402

R3931 2.0K 5% 1/16W MF-LF 402
R3938 2.0K 5% 1/16W MF-LF 402

DDR2 DIMMS
I2C_NB_RAM_SDA NET_SPACING_TYPE=I2C
I2C_NB_RAM_SCL NET_SPACING_TYPE=I2C

I2C Connections

SYNC_MASTER=FINO-ME SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 39 OF 154	

Q63 APPLICATION IS PP1V5 PWRON

=PPV_EI_NB 7 41 42 56

XW4100 NO_TEST=YES P4MM PP_VEINB PP4100

U1900 BGA (7 OF 10) PART 0 PWR/GND KODIAK-ASIC-040812

AB01	GND_0	VD2_0	AB02
AB04	GND_1	VD2_1	AB05
AB07	GND_2	VD2_2	AB08
AB10	GND_3	VD2_3	AB11
AB12	GND_4	VD2_4	AB13
AD02	GND_5	VD2_5	AD01
AD05	GND_6	VD2_6	AD04
AD08	GND_7	VD2_7	AD07
AD11	GND_8	VD2_8	AD10
AD13	GND_9	VD2_9	AD12
AD17	GND_10	VD2_10	AD16
AD21	GND_11	VD2_11	AD20
AE15	GND_12	VD2_12	AE14
AE19	GND_13	VD2_13	AE18
AF07	GND_14	VD2_14	AF08
AF10	GND_15	VD2_15	AF11
AF13	GND_16	VD2_16	AF15
AF17	GND_17	VD2_17	AF19
AG11	GND_18	VD2_18	AG13
AG15	GND_19	VD2_19	AG17
AG19	GND_20	VD2_20	AG21
AH02	GND_21	VD2_21	AH04
AH05	GND_22	VD2_22	AH07
AH08	GND_23	VD2_23	AH09
AJ13	GND_24	VD2_24	AJ11
AJ17	GND_25	VD2_25	AJ15
AJ21	GND_26	VD2_26	AJ19
AK01	GND_27	VD2_27	AK02
AK04	GND_28	VD2_28	AK05
AK07	GND_29	VD2_29	AK09
AK11	GND_30	VD2_30	AK13
AK15	GND_31	VD2_31	AK17
AK19	GND_32	VD2_32	AK21
AM02	GND_33	VD2_33	AM01
AM05	GND_34	VD2_34	AM04
AM09	GND_35	VD2_35	AM07
AM13	GND_36	VD2_36	AM11
AM17	GND_37	VD2_37	AM15
AM21	GND_38	VD2_38	AM19
AN04	GND_39	VD2_39	AN05
AN07	GND_40	VD2_40	AN09
AN11	GND_41	VD2_41	AN13
AN15	GND_42	VD2_42	AN17
AN19	GND_43	VD2_43	AN21
AP01	GND_44	VD2_44	AP02
AR05	GND_45	VD2_45	AR03
AR09	GND_46	VD2_46	AR07
AR13	GND_47	VD2_47	AR11
AR17	GND_48	VD2_48	AR15
AR21	GND_49	VD2_49	AR19
AT03	GND_50	VD2_50	AT05
AT07	GND_51	VD2_51	AT09
AT11	GND_52	VD2_52	AT13
AT15	GND_53	VD2_53	AT17
AT19	GND_54	VD2_54	AT21
K01	GND_55	VD2_55	K02
K04	GND_56	VD2_56	K05
M02	GND_57	VD2_57	K08
M05	GND_58	VD2_58	M01
M08	GND_59	VD2_59	M04
P01	GND_60	VD2_60	M07
P04	GND_61	VD2_61	M10
P07	GND_62	VD2_62	P02
P10	GND_63	VD2_63	P05
P12	GND_64	VD2_64	P08
T02	GND_65	VD2_65	P11
T05	GND_66	VD2_66	P13
T08	GND_67	VD2_67	T01
T11	GND_68	VD2_68	T04
T13	GND_69	VD2_69	T07
V01	GND_70	VD2_70	T10
V04	GND_71	VD2_71	T12
V07	GND_72	VD2_72	V02
V10	GND_73	VD2_73	V05
V12	GND_74	VD2_74	V08
Y02	GND_75	VD2_75	V11
Y05	GND_76	VD2_76	V13
Y08	GND_77	VD2_77	Y01
Y11	GND_78	VD2_78	Y04
Y13	GND_79	VD2_79	Y07
AF01	GND_80	VD2_80	Y10
AF04	GND_81	VD2_81	Y12
AF21	GND_82		
AJ08	GND_83		
AJ09	GND_84		

Q63 APPLICATION IS PP1V5 PWRON

56 42 41 7 =PPV_EI_NB

C4168 C4146 C4143 C4139 C4137 C4113 C4112 C4106 C4122 C4100
C4169 C4147 C4145 C4140 C4138 C4114 C4110 C4107 C4133 C4111
C4170 C4149 C4148 C4142 C4141 C4115 C4109 C4108 C4155 C4144
C4171 C4161 C4159 C4152 C4150 C4125 C4118 C4116 C4181 C4166
C4172 C4162 C4160 C4153 C4151 C4126 C4124 C4117 C4101 C4177
C4174 C4165 C4163 C4157 C4154 C4127 C4123 C4104 C4102
C4173 C4167 C4164 C4158 C4156 C4128 C4121 C4120 C4105 C4103
C4180 C4179 C4178 C4176 C4175 C4136 C4135 C4134 C4130 C4129
C4132 C4131

All: 0.22UF 20% 6.3V X5R 402

KODIAK EI PWR & CAPS

SYNC_MASTER=Q63 SYNC_DATE=08/01/2005

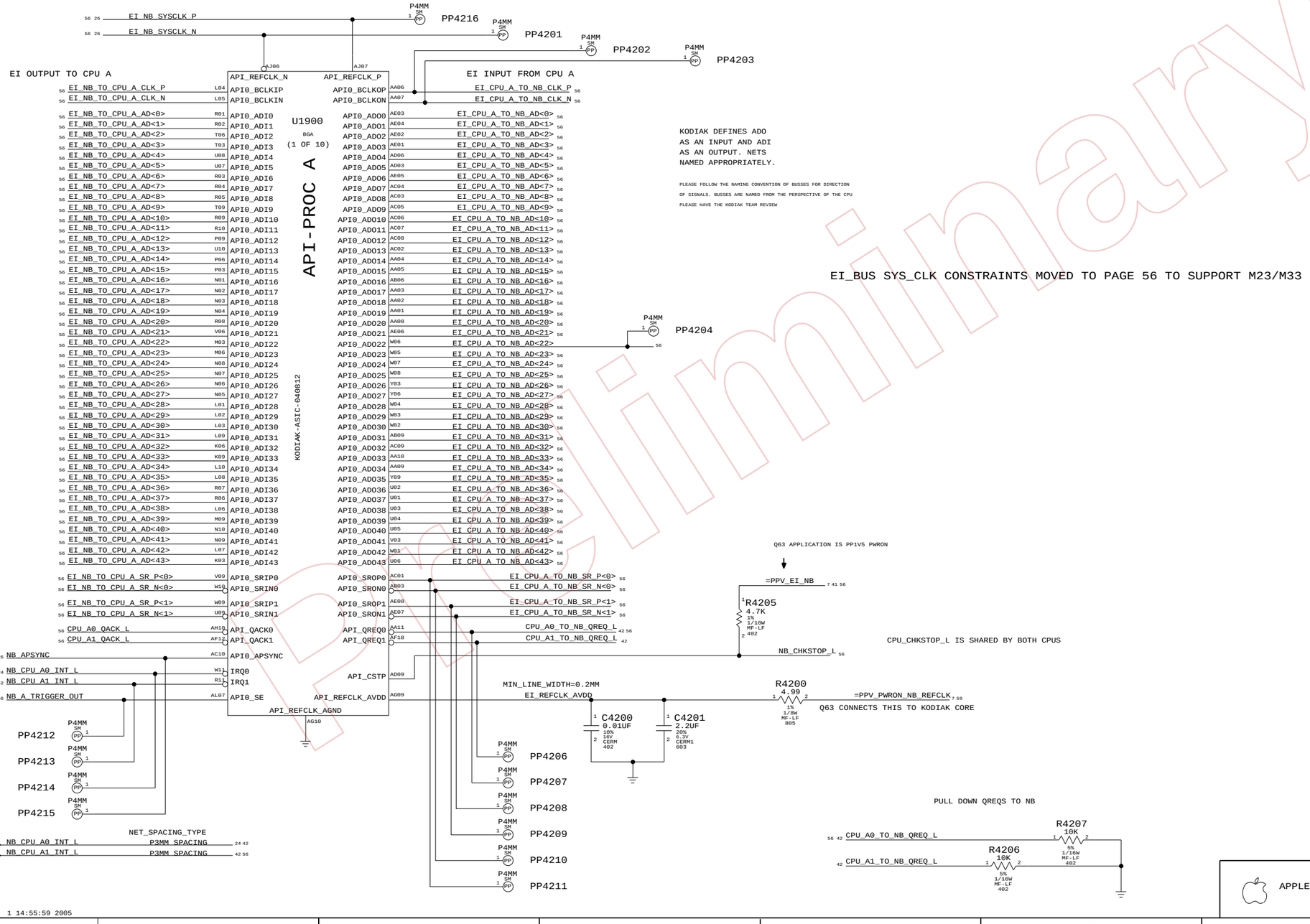
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E

SCALE: NONE SHT: 41 OF: 154

LAST_MODIFIED=Tue Nov 1 14:55:58 2005

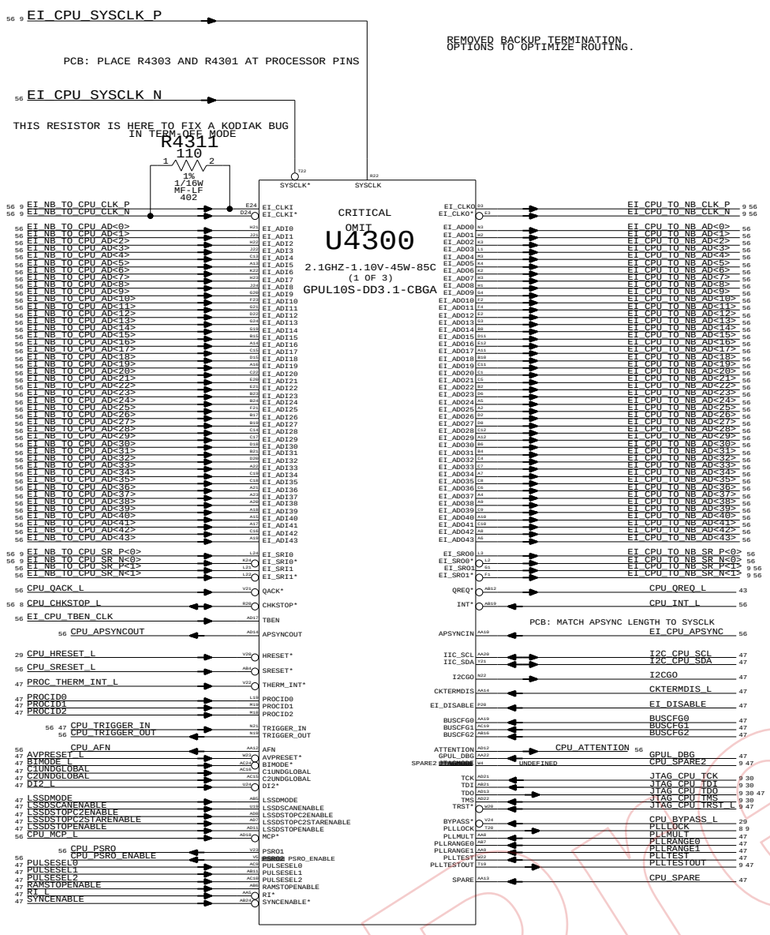
DRAWING

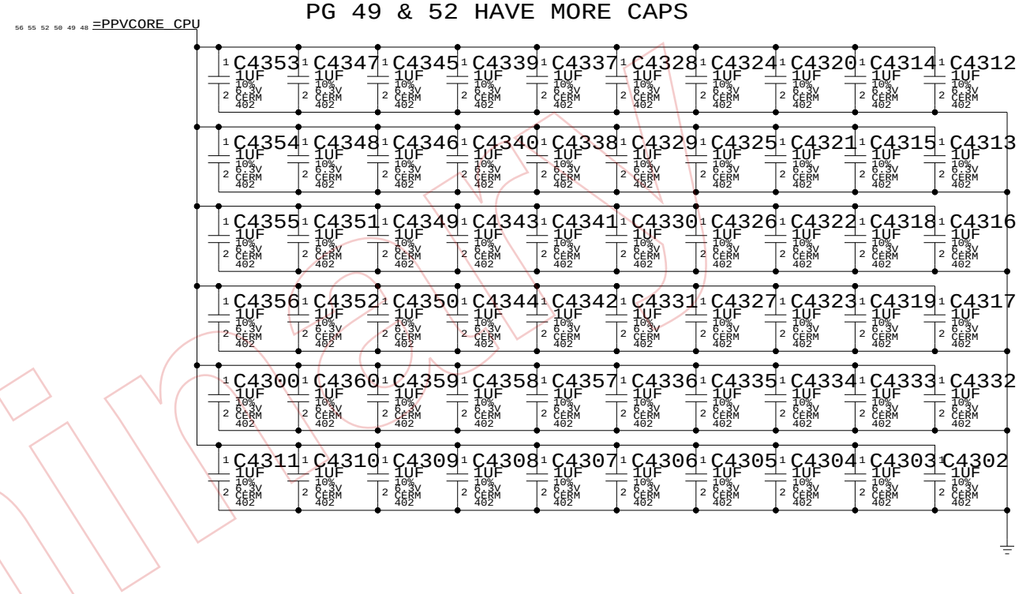


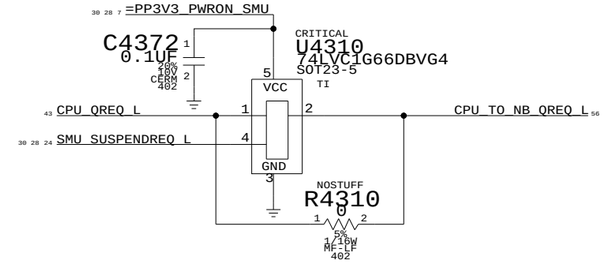
LAST_MODIFIED=Tue Nov 1 14:55:59 2005

DRAWING

KODIAK EI A			
SYNC_MASTER=Q63	SYNC_DATE=08/01/2005		
NOTICE OF PROPRIETARY PROPERTY			
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART			
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6790	REV. E
	SCALE NONE	SHT 42 OF 154	







CPU EI AND IO

SYNC_MASTER=FINO-HS SYNC_DATE=06/20/2005

NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT: 43	OF: 154

PLEASE FOLLOW THE NAMING CONVENTION OF BUSSES FOR DIRECTION
OF SIGNALS. BUSSES ARE NAMED FROM THE PERSPECTIVE OF THE CPU
PLEASE HAVE THE KODIAK TEAM REVIEW

P4MM SM 1 PP → PP4410
P4MM SM 1 PP → PP4411

EI OUTPUT TO CPU B

EI_NB_TO_CPU_B_CLK_P (56) AT08 API1_BCLKIP
EI_NB_TO_CPU_B_CLK_N (56) AR08 API1_BCLKIN

API1_BCLKOP AT16 → EI_CPU_B_TO_NB_CLK_P (56)
API1_BCLKON AR16 → EI_CPU_B_TO_NB_CLK_N (56)

EI INPUT FROM CPU B

U1900
BGA
(2 OF 10)
API-PROC B
KODIAK-ASIC-040812

EI_NB_TO_CPU_B_AD<0> (56)	AM12	API1_ADI0	API1_AD00 AP20	EI_CPU_B_TO_NB_AD<0> (56)
EI_NB_TO_CPU_B_AD<1> (56)	AN12	API1_ADI1	API1_AD01 AN20	EI_CPU_B_TO_NB_AD<1> (56)
EI_NB_TO_CPU_B_AD<2> (56)	AL12	API1_ADI2	API1_AD02 AR20	EI_CPU_B_TO_NB_AD<2> (56)
EI_NB_TO_CPU_B_AD<3> (56)	AK12	API1_ADI3	API1_AD03 AT20	EI_CPU_B_TO_NB_AD<3> (56)
EI_NB_TO_CPU_B_AD<4> (56)	AP11	API1_ADI4	API1_AD04 AL19	EI_CPU_B_TO_NB_AD<4> (56)
EI_NB_TO_CPU_B_AD<5> (56)	AL11	API1_ADI5	API1_AD05 AP19	EI_CPU_B_TO_NB_AD<5> (56)
EI_NB_TO_CPU_B_AD<6> (56)	AP12	API1_ADI6	API1_AD06 AM20	EI_CPU_B_TO_NB_AD<6> (56)
EI_NB_TO_CPU_B_AD<7> (56)	AR12	API1_ADI7	API1_AD07 AM18	EI_CPU_B_TO_NB_AD<7> (56)
EI_NB_TO_CPU_B_AD<8> (56)	AT12	API1_ADI8	API1_AD08 AL18	EI_CPU_B_TO_NB_AD<8> (56)
EI_NB_TO_CPU_B_AD<9> (56)	AH12	API1_ADI9	API1_AD09 AN18	EI_CPU_B_TO_NB_AD<9> (56)
EI_NB_TO_CPU_B_AD<10> (56)	AG12	API1_ADI10	API1_AD010 AP18	EI_CPU_B_TO_NB_AD<10> (56)
EI_NB_TO_CPU_B_AD<11> (56)	AH13	API1_ADI11	API1_AD011 AR18	EI_CPU_B_TO_NB_AD<11> (56)
EI_NB_TO_CPU_B_AD<12> (56)	AJ12	API1_ADI12	API1_AD012 AT18	EI_CPU_B_TO_NB_AD<12> (56)
EI_NB_TO_CPU_B_AD<13> (56)	AG14	API1_ADI13	API1_AD013 AK18	EI_CPU_B_TO_NB_AD<13> (56)
EI_NB_TO_CPU_B_AD<14> (56)	AM10	API1_ADI14	API1_AD014 AP17	EI_CPU_B_TO_NB_AD<14> (56)
EI_NB_TO_CPU_B_AD<15> (56)	AL10	API1_ADI15	API1_AD015 AL17	EI_CPU_B_TO_NB_AD<15> (56)
EI_NB_TO_CPU_B_AD<16> (56)	AN10	API1_ADI16	API1_AD016 AH20	EI_CPU_B_TO_NB_AD<16> (56)
EI_NB_TO_CPU_B_AD<17> (56)	AP10	API1_ADI17	API1_AD017 AJ20	EI_CPU_B_TO_NB_AD<17> (56)
EI_NB_TO_CPU_B_AD<18> (56)	AR10	API1_ADI18	API1_AD018 AK20	EI_CPU_B_TO_NB_AD<18> (56)
EI_NB_TO_CPU_B_AD<19> (56)	AT10	API1_ADI19	API1_AD019 AH19	EI_CPU_B_TO_NB_AD<19> (56)
EI_NB_TO_CPU_B_AD<20> (56)	AK10	API1_ADI20	API1_AD020 AG20	EI_CPU_B_TO_NB_AD<20> (56)
EI_NB_TO_CPU_B_AD<21> (56)	AJ10	API1_ADI21	API1_AD021 AL20	EI_CPU_B_TO_NB_AD<21> (56)
EI_NB_TO_CPU_B_AD<22> (56)	AM08	API1_ADI22	API1_AD022 AM16	EI_CPU_B_TO_NB_AD<22>
EI_NB_TO_CPU_B_AD<23> (56)	AN08	API1_ADI23	API1_AD023 AN16	EI_CPU_B_TO_NB_AD<23> (56)
EI_NB_TO_CPU_B_AD<24> (56)	AL08	API1_ADI24	API1_AD024 AL16	EI_CPU_B_TO_NB_AD<24> (56)
EI_NB_TO_CPU_B_AD<25> (56)	AP07	API1_ADI25	API1_AD025 AK16	EI_CPU_B_TO_NB_AD<25> (56)
EI_NB_TO_CPU_B_AD<26> (56)	AT06	API1_ADI26	API1_AD026 AP15	EI_CPU_B_TO_NB_AD<26> (56)
EI_NB_TO_CPU_B_AD<27> (56)	AR06	API1_ADI27	API1_AD027 AL15	EI_CPU_B_TO_NB_AD<27> (56)
EI_NB_TO_CPU_B_AD<28> (56)	AP08	API1_ADI28	API1_AD028 AP16	EI_CPU_B_TO_NB_AD<28> (56)
EI_NB_TO_CPU_B_AD<29> (56)	AT04	API1_ADI29	API1_AD029 AM14	EI_CPU_B_TO_NB_AD<29> (56)
EI_NB_TO_CPU_B_AD<30> (56)	AR04	API1_ADI30	API1_AD030 AL14	EI_CPU_B_TO_NB_AD<30> (56)
EI_NB_TO_CPU_B_AD<31> (56)	AP05	API1_ADI31	API1_AD031 AN14	EI_CPU_B_TO_NB_AD<31> (56)
EI_NB_TO_CPU_B_AD<32> (56)	AM06	API1_ADI32	API1_AD032 AP14	EI_CPU_B_TO_NB_AD<32> (56)
EI_NB_TO_CPU_B_AD<33> (56)	AN06	API1_ADI33	API1_AD033 AR14	EI_CPU_B_TO_NB_AD<33> (56)
EI_NB_TO_CPU_B_AD<34> (56)	AP06	API1_ADI34	API1_AD034 AT14	EI_CPU_B_TO_NB_AD<34> (56)
EI_NB_TO_CPU_B_AD<35> (56)	AP04	API1_ADI35	API1_AD035 AK14	EI_CPU_B_TO_NB_AD<35> (56)
EI_NB_TO_CPU_B_AD<36> (56)	AM03	API1_ADI36	API1_AD036 AP13	EI_CPU_B_TO_NB_AD<36> (56)
EI_NB_TO_CPU_B_AD<37> (56)	AN01	API1_ADI37	API1_AD037 AL13	EI_CPU_B_TO_NB_AD<37> (56)
EI_NB_TO_CPU_B_AD<38> (56)	AL06	API1_ADI38	API1_AD038 AG16	EI_CPU_B_TO_NB_AD<38> (56)
EI_NB_TO_CPU_B_AD<39> (56)	AL05	API1_ADI39	API1_AD039 AH15	EI_CPU_B_TO_NB_AD<39> (56)
EI_NB_TO_CPU_B_AD<40> (56)	AL04	API1_ADI40	API1_AD040 AJ14	EI_CPU_B_TO_NB_AD<40> (56)
EI_NB_TO_CPU_B_AD<41> (56)	AL03	API1_ADI41	API1_AD041 AH14	EI_CPU_B_TO_NB_AD<41> (56)
EI_NB_TO_CPU_B_AD<42> (56)	AN02	API1_ADI42	API1_AD042 AH16	EI_CPU_B_TO_NB_AD<42> (56)
EI_NB_TO_CPU_B_AD<43> (56)	AN03	API1_ADI43	API1_AD043 AH17	EI_CPU_B_TO_NB_AD<43> (56)

KODIAK DEFINES ADO AS AN INPUT AND ADI AS AN OUTPUT. NETS NAMED APPROPRIATELY.

WE MAY NEED A DIFFERENT ELECTRICAL_CONSTRAINT_SET FOR CPU_A AND CPU_B.

EI_BUS SYS_CLK CONSTRAINTS MOVED TO PAGE 56 TO SUPPORT M23/M33

EI_NB_TO_CPU_B_SR_P<0> (56)	AP09	API1_SRIP0	API1_SROP0 AG18	EI_CPU_B_TO_NB_SR_P<0> (56)
EI_NB_TO_CPU_B_SR_N<0> (56)	AL09	API1_SRIN0	API1_SRON0 AJ16	EI_CPU_B_TO_NB_SR_N<0> (56)
EI_NB_TO_CPU_B_SR_P<1> (56)	AR02	API1_SRIP1	API1_SROP1 AJ18	EI_CPU_B_TO_NB_SR_P<1> (56)
EI_NB_TO_CPU_B_SR_N<1> (56)	AP02	API1_SRIN1	API1_SRON1 AH18	EI_CPU_B_TO_NB_SR_N<1> (56)

CPU_B0_QACK_L (56)	AF12	API_QACK2	API_QREQ2 AF16	CPU_B0_TO_NB_QREQ_L (44)
CPU_B1_QACK_L (56)	AC12	API_QACK3	API_QREQ3 AF20	CPU_B1_TO_NB_QREQ_L (44)

NB_CPU_B0_INT_L (56 44)	N12	IRQ2	
NB_CPU_B1_INT_L (56 44)	U12	IRQ3	
TP_NB_APSYNC (9)	AH11	API1_APSYNC	
NB_B_TRIGGER_OUT (56)	AK08	API1_SE	

WIRE TP_NB_APSYNC TO A TEST POINT

P4MM SM 1 PP → PP4406
P4MM SM 1 PP → PP4407
P4MM SM 1 PP → PP4408

P4MM SM 1 PP → PP4413 (56)

P4MM SM 1 PP → PP4400
P4MM SM 1 PP → PP4401
P4MM SM 1 PP → PP4402
P4MM SM 1 PP → PP4403
P4MM SM 1 PP → PP4404
P4MM SM 1 PP → PP4405

NET_SPACING_TYPE

NB_CPU_B0_INT_L (46)	P3MM_SPACING	(44 56)
NB_CPU_B1_INT_L (49)	P3MM_SPACING	(44 56)

PULL DOWN QREQS TO NB

CPU_B0_TO_NB_QREQ_L (44) — R4407 10K 5% 1/16W MF-LF 402 — 1 2
CPU_B1_TO_NB_QREQ_L (44) — R4406 10K 5% 1/16W MF-LF 402 — 1 2

LAST_MODIFIED=Tue Nov 1 14:56:00 2005

DRAWING

KODIAK EI B	
SYNC_MASTER=Q63	SYNC_DATE=08/01/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 44 OF 154	

=PPV_EI_CPU 7 29 30 47 48 56

PULLUPS

43	C1UNDGLOBAL	NOSTUFF R4777 4.7K	R4743 4.7K
43	C2UNDGLOBAL	NOSTUFF R4779 4.7K	R4769 4.7K
43	PLLTEST	NOSTUFF R4763 4.7K	R4761 4.7K
43	CKTERMDIS_L	NOSTUFF R4775 4.7K	R4773 4.7K
43	GPUL_DBG	R4740 4.7K	NOSTUFF R4742 4.7K

M23/M33 IS JTAG ONLY, NO I2C

43 9	JTAG_CPU_TRST_L	R4709 4.7K
43	BIMODE_L	R4731 4.7K
43	DI2_L	R4733 4.7K
43	RI_L	R4735 4.7K
43	PROC_THERM_INT_L	R4765 4.7K
43	I2CGO	R4787 4.7K
43	I2C_CPU_SCL	R4788 4.7K
43	I2C_CPU_SDA	R4789 4.7K
43 30 9	JTAG_CPU_TDO	R4790 4.7K

PULLDOWNS

43 9	CPU_SPARE2	R4739 0
43	LSSDMODE	R4745 4.7K
43	LSSDSCANENABLE	R4741 4.7K
43	LSSDSTOPC2ENABLE	R4747 4.7K
43	LSSDSTOPC2STARENABLE	R4749 4.7K
43	LSSDSTOPENABLE	R4751 4.7K
43	SYNCENABLE	R4737 4.7K
43	RAMSTOPENABLE	R4755 4.7K
43	CPU_SPARE	NOSTUFF R4767 4.7K
56 43	CPU_TRIGGER_IN	R4781 4.7K
43	PULSESEL0	R4703 4.7K
43	PULSESEL1	R4705 4.7K
43	PULSESEL2	R4707 4.7K
43	PROCID0	R4702 4.7K
43	PROCID1	R4704 4.7K
43	PROCID2	R4706 4.7K
43 9	PLLTESTOUT	NOSTUFF R4771 4.7K

=PPV_EI_CPU 7 29 30 47 48 56

R4768 10K

NOTES

JTAG DRIVEN ON SMU PG 30
QREQ PULLDOWNS ON Q63 SHARED PAGE
SRESET DRIVEN ON PG 56
INT DRIVEN BY KODIAK
R4739 REQUIRED TO ACCESS THE RINGS

4.7K RESISTORS FOR MANUFACTURING-TEST-TYPE PULLUPS OR PULLDOWNS.
1K RESISTORS FOR IMPORTANT USE OR STRAPPING OPTIONS.

SELECT PROCESSOR CLOCK MULTIPLIER. PROCESSOR CLOCK(MHZ)= SYSTCLOCK * PLLMULT.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
*	116S0066	1	RES,1K OHM,1/16W,5%,0402	R4734	EI_3TO1	SYSCLK * 12
	116S0066	1	RES,1K OHM,1/16W,5%,0402	R4718	EI_2TO1	SYSCLK * 8

SELECT EI BUS DIVIDER. BUS DATA RATE(BPS)= (PROCESSOR CLOCK) / BUSCFG.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
*	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4724,R4726,R4728	EI_2TO1	PROC / 2
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4724,R4726,R4712	EI_3TO1	PROC / 3
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4724,R4710,R4728	NOSTUFF	PROC / 4
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4724,R4710,R4712	NOSTUFF	PROC / 6
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4708,R4726,R4728	NOSTUFF	PROC / 8
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4708,R4726,R4712	NOSTUFF	PROC / 12
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4708,R4710,R4728	NOSTUFF	PROC / 16
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4708,R4710,R4712	NOSTUFF	

SELECT ELASTIC MODE OR BYPASS.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
*	116S0066	1	RES,1K OHM,1/16W,5%,0402	R4736		
	116S0066	1	RES,1K OHM,1/16W,5%,0402	R4720	NOSTUFF	BYPASS MODE

SELECT PLL FREQUENCY RANGE.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
	116S0066	2	RES,1K OHM,1/16W,5%,0402	R4730,R4732	CPU_PLL_LOW	>= 1.8 GHZ *
	116S0066	2	RES,1K OHM,1/16W,5%,0402	R4730,R4716	CPU_PLL_HIGH	
	116S0066	2	RES,1K OHM,1/16W,5%,0402	R4714,R4732	CPU_PLL_MEDIUM	
	116S0066	2	RES,1K OHM,1/16W,5%,0402	R4714,R4716	NOSTUFF	RESERVED

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
116S0066	1	RES,1K OHM,1/16W,5%,0402	R4722		AVPRESET OFF
116S0066	1	RES,1K OHM,1/16W,5%,0402	R4738	NOSTUFF	AVPRESET ON

* STUFF THESE ON M23.

PROCESSOR BUS CONFIGURATION

56 48 47 30 29 7 =PPV_EI_CPU

SEE STUFFING OPTIONS ABOVE

BUSCFG0	OMIT R4708 1K	OMIT R4710 1K	OMIT R4712 1K	OMIT R4714 1K	OMIT R4716 1K	OMIT R4718 1K	OMIT R4720 1K	OMIT R4722 1K
BUSCFG1								
BUSCFG2								
PLLRANGE0								
PLLRANGE1								
PLLMULT								
EI_DISABLE								
AVPRESET_L	OMIT R4724 1K	OMIT R4726 1K	OMIT R4728 1K	OMIT R4730 1K	OMIT R4732 1K	OMIT R4734 1K	OMIT R4736 1K	OMIT R4738 1K

CPU STRAPS

SYNC_MASTER=FINO-HS SYNC_DATE=06/20/2005

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	E
	SCALE NONE	SHT 47 OF 154	

=PPVCORE_CPU
VOLTAGE=1.3V
MIN_LINE_WIDTH=0.50MM
MIN_NECK_WIDTH=0.20MM

=PPV_EI_CPU

PPV_RUN_AVDD_CPU

R4832 2.2 5% 1/10W MF-LF 603

PPV_RUN_CPU_AVDD_R
VOLTAGE=2.8V
MIN_LINE_WIDTH=0.60MM
MIN_NECK_WIDTH=0.20MM

L4801 60-OHM-EMI SM 0805

PPV_RUN_CPU_AVDD_R_L
VOLTAGE=2.8V
MIN_LINE_WIDTH=0.60MM
MIN_NECK_WIDTH=0.20MM

C4802 10UF 10% 6.3V X5R 805

C4800 0.1UF 10% 16V X5R 402

NET_PHYSICAL_TYPE=PROC_DIFF
NET_SPACING_TYPE=PROC_DIFF
DIFFERENTIAL_PAIR=P_TDO
MIN_LINE_WIDTH=0.25MM
MIN_NECK_WIDTH=0.20MM

CPU_DIODE_POS

C4817 10UF 10% 6.3V X5R 805
C4816 10UF 10% 6.3V X5R 805
C4815 10UF 10% 6.3V X5R 805
C4814 10UF 10% 6.3V X5R 805

C4811 0.1UF 20% 10V CERM 402
C4806 0.1UF 20% 10V CERM 402
C4805 0.1UF 20% 10V CERM 402
C4803 0.1UF 20% 10V CERM 402
C4812 0.1UF 20% 10V CERM 402
C4809 0.1UF 20% 10V CERM 402
C4807 0.1UF 20% 10V CERM 402
C4804 0.1UF 20% 10V CERM 402
C4813 0.1UF 20% 10V CERM 402
C4810 0.1UF 20% 10V CERM 402
C4808 0.1UF 20% 10V CERM 402
C4826 0.1UF 20% 10V CERM 402
C4820 0.1UF 20% 10V CERM 402
C4818 0.1UF 20% 10V CERM 402
C4827 0.1UF 20% 10V CERM 402
C4821 0.1UF 20% 10V CERM 402
C4819 0.1UF 20% 10V CERM 402
C4828 0.1UF 20% 10V CERM 402
C4824 0.1UF 20% 10V CERM 402
C4822 0.1UF 20% 10V CERM 402
C4829 0.1UF 20% 10V CERM 402
C4825 0.1UF 20% 10V CERM 402
C4823 0.1UF 20% 10V CERM 402
C4836 0.1UF 20% 10V CERM 402
C4831 0.1UF 20% 10V CERM 402
C4830 0.1UF 20% 10V CERM 402
C4837 0.1UF 20% 10V CERM 402
C4834 0.1UF 20% 10V CERM 402
C4832 0.1UF 20% 10V CERM 402
C4838 0.1UF 20% 10V CERM 402
C4835 0.1UF 20% 10V CERM 402
C4833 0.1UF 20% 10V CERM 402
C4845 0.1UF 20% 10V CERM 402
C4841 0.1UF 20% 10V CERM 402
C4839 0.1UF 20% 10V CERM 402
C4846 0.1UF 20% 10V CERM 402
C4842 0.1UF 20% 10V CERM 402
C4840 0.1UF 20% 10V CERM 402
C4847 0.1UF 20% 10V CERM 402
C4844 0.1UF 20% 10V CERM 402
C4843 0.1UF 20% 10V CERM 402

OMIT CRITICAL
U4300
2.1GHZ-1.10V-45W-85C
(2 OF 3)
GPUL10S-DD3.1-CBGA

OMIT CRITICAL
U4300
2.1GHZ-1.10V-45W-85C
(3 OF 3)
GPUL10S-DD3.1-CBGA

AVDD
KPVDD1
KPVDD2
DIODEPOS
DIODENEG
AGND
KPGND2
SPARE_GND

VCORE X105
GND X105
VCORE X100
GND X99

NOSTUFF R4810 100K 5% 1/10W MF-LF 603

PROCESSOR KELVIN POINT PROBE POINT

KPVDD2
DIFFERENTIAL_PAIR=P_KP2
MIN_LINE_WIDTH=0.25MM
MIN_NECK_WIDTH=0.20MM
NET_SPACING_TYPE=PROC_DIFF
NET_PHYSICAL_TYPE=PROC_DIFF

REMEMBER TO CHANGE KPVDD TO NO_TEST ON PG 6.

PCB:PUT R4810 AS CLOSE TO RESPECTIVE PINS AS POSSIBLE.

KPGND2
DIFFERENTIAL_PAIR=P_KP2
MIN_LINE_WIDTH=0.25MM
MIN_NECK_WIDTH=0.20MM
NET_SPACING_TYPE=PROC_DIFF
NET_PHYSICAL_TYPE=PROC_DIFF

OMIT XW4800 SM

GND_CPU_AVDD

CPU_DIODE_NEG
DIFFERENTIAL_PAIR=P_TDO
MIN_LINE_WIDTH=0.25MM
MIN_NECK_WIDTH=0.20MM
NET_SPACING_TYPE=PROC_DIFF
NET_PHYSICAL_TYPE=PROC_DIFF

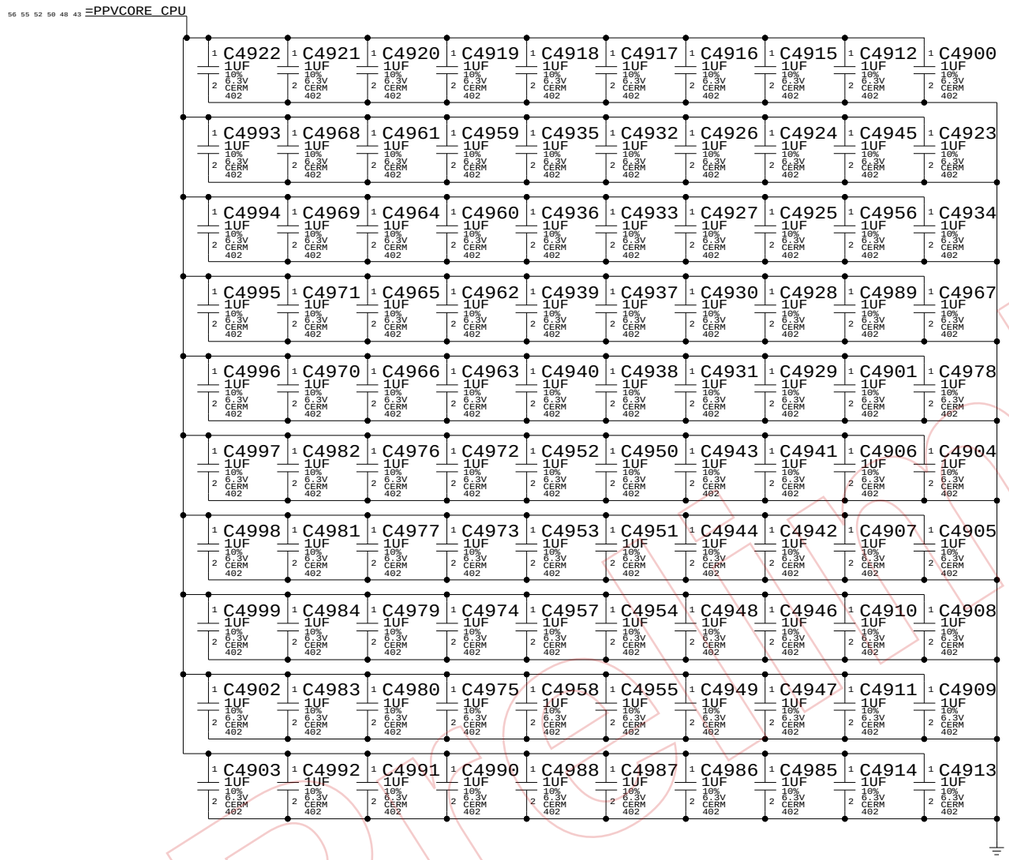
CPU POWER AND BYPASS

SYNC_MASTER=FINO-HS SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E

SCALE	SHT	OF
NONE	48	154



PROC DECOUPLING

SYNC_MASTER=FINO-HS SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 49 OF 154	

VCORE VOLTAGE CONTROLLER (VC)

M23/M33: PP12V_CPU IS AN ALL RAIL

=PP12V_CPU
R5029 10 5% 1/16W MF-LF 402
VC_VCC
C5019 1UF 20% 16V CERM 1206
SYS_POWERUP_L
R5000 1.5K 5% 1/16W MF-LF 402
VRM_EN
Q5012 2N7002 SOT23-LF
C5001 1UF 10% 6.3V CERM 402
VC_AGND
VC_BGOUT
VC_OSCREF
CPU_VID_R<0>
CPU_VID_R<1>
CPU_VID_R<2>
CPU_VID_R<3>
CPU_VID_R<4>
CPU_VID_R<5>
U5000 SC2642 TSSOP
BGOUT OSCREF VID0 VID1 VID2 VID3 VID4 VID5 DACSTEP FB GSENSE OS1 OS2 AGND VCC OUTSEN OUT1 OUT2 PGOOD EROUT
VC_OUTSEN
VC_OUT1
VC_OUT2
VC_PGOOD
PGOOD IS OC
R5030 0 5% 1/16W MF-LF 402
SYS_SLEWING_L
VC_DACSTEP
VC_ERROUT
VC_VCC
R5003 2.7M 5% 1/10W MF-LF 603
R5001 20K 5% 1/16W MF-LF 402
NOSTUFF R5002 0 5% 1/16W MF-LF 402
VC_ERROUT_RC
C5002 470PF 10% 50V CERM 402
OMIT XW5000 SM
VC_OS1
VC_OS2
C5000 0.1UF 20% 10V CERM 402
R5028 221K 1% 1/16W MF-LF 402
VC_AGND

VC_AUX1
VC_AUX2
R5013 20.5K 1% 1/16W MF-LF 402
R5016 20.5K 1% 1/16W MF-LF 402
C5004 0.01UF 10% 16V CERM 402
NOSTUFF R5014 20.5K 1% 1/16W MF-LF 402
C5005 0.01UF 10% 16V CERM 402
NOSTUFF R5015 20.5K 1% 1/16W MF-LF 402

VCORE_SENSE_GND
DIFFERENTIAL PAIR FOR REMOTE SENSE
VCORE_SENSE_VOUT
VC_OUTSEN
R5005 4.99K 1% 1/16W MF-LF 402
VC_VCC
VC_OS_HUB
R5004 261 1% 1/16W MF-LF 402
C5008 0.33UF 10% 6.3V CERM-X5R 402
NOSTUFF R5026 301 1% 1/16W MF-LF 402
AVP ADJUSTMENT
NOSTUFF R5024 330 5% 1/16W MF-LF 402
NOSTUFF R5025 1K 5% 1/16W MF-LF 402
VC_OS_HUB_RC
PCB:PLACE R5025 CLOSE TO INDUCTOR OUTPUT LEAD.
NOSTUFF C5009 0.015UF 10% 16V X7R 402
R5027 1.5K 1% 1/16W MF-LF 402
VC_OUTSEN_R
OMIT XW5002 SM
=PPVCORE_CPU
PCB:CONNECT BETWEEN THE INDUCTOR & BULK CAPS.

VC PROCESSOR VOLTAGE SENSING

CHOICE OF:
1) VCORE PLANE SENSING
2) KELVIN POINT SENSING

PPVCORE_CPU
MIN_NECK_WIDTH=0.20MM
MIN_LINE_WIDTH=0.50MM
UNDER PROCESSOR
R5035 0 5% 1/16W MF-LF 402
R5036 0 5% 1/16W MF-LF 402
VCORE_SENSE_VOUT
VCORE_SENSE_GND
KPVDD2
NOSTUFF R5041 0 5% 1/16W MF-LF 402
CPU SENSE SIDE
KPGND2
NOSTUFF R5042 0 5% 1/16W MF-LF 402

	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
GD1_DRN	0.25 MM	0.25 MM	R836
GD1_BST	0.25 MM	0.25 MM	R837
GD1_VREG	0.25 MM	0.25 MM	R838
GD1_VPN	0.25 MM	0.25 MM	R839
GD1_TG	0.25 MM	0.25 MM	R840
GD1_BG	0.25 MM	0.25 MM	R841
GD1_FET_RC	0.25 MM	0.25 MM	R842
GD1_PN	0.60 MM	0.25 MM	R843
GD1_BST_R	0.25 MM	0.25 MM	R858

	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
GD2_DRN	0.25 MM	0.25 MM	R844
GD2_BST	0.25 MM	0.25 MM	R845
GD2_VREG	0.25 MM	0.25 MM	R846
GD2_VPN	0.25 MM	0.25 MM	R847
GD2_TG	0.25 MM	0.25 MM	R848
GD2_BG	0.25 MM	0.25 MM	R849
GD2_FET_RC	0.25 MM	0.25 MM	R850
GD2_PN	0.60 MM	0.25 MM	R851
GD2_BST_R	0.25 MM	0.25 MM	R852

VCORE SUPPLY PHASE 1 (GD1)

PP12V_CPU_R_L
C5010 1UF 20% 16V CERM 1206
GD1_BST_R
GD1_DRN
CRITICAL U5010 SC1211 VIN SOIC-LF BG CO VREG DRN TG BST VPN THMPAD
GD1_TG
C5029 1UF 20% 16V CERM 1206
VC_OUT1
R5007 4.7 5% 1/10W MF-LF 603
GD1_BST
D5010 BAS16-75V-0.25A SOT23-LF
GD1_VREG
C5013 1UF 20% 16V CERM 1206
GD1_VPN
R5012 200 5% 1/16W MF-LF 402
VC_AUX1
C5014 470PF 10% 50V CERM 402
GD1_PN
C5011 680UF 20% 16V ELEC TH-MCZ
C5035 330UF 20% 16V ELEC SM-LF
C5012 10UF 10% 16V CERM 1210
CRITICAL Q5010 NTD60N02R CASE369-LF
R5050 10K 5% 1/16W MF-LF 402
R5010 1 5% 1/16W MF-LF 402
GD1_BG
CRITICAL Q5011 NTD70N03R CASE369-LF
CRITICAL Q5013 NTD70N03R CASE369-LF
C5015 0.0022UF 10% 50V CERM 402
C5016 3300PF 10% 50V CERM 603
R5011 1.0 5% 1/4W MF-LF 1206
GD1_FET_RC
CRITICAL L5010 0.6UH-24A TH2
=PPVCORE_CPU
PPVCORE_CPU
C5018 1800UF 20% 6.3V ELEC TH-KZJ-LF
C5017 1800UF 20% 6.3V ELEC TH-KZJ-LF
C5032 1800UF 20% 6.3V ELEC TH-KZJ-LF
C5037 1800UF 20% 6.3V ELEC TH-KZJ-LF
C5038 1800UF 20% 6.3V ELEC TH-KZJ-LF
C5039 1800UF 20% 6.3V ELEC TH-KZJ-LF

VCORE SUPPLY PHASE 2 (GD2)

PP12V_CPU_R_L
C5020 1UF 20% 16V CERM 1206
GD2_BST_R
GD2_DRN
CRITICAL U5020 SC1211 VIN SOIC-LF BG CO VREG DRN TG BST VPN THMPAD
GD2_TG
C5030 1UF 20% 16V CERM 1206
VC_OUT2
R5006 4.7 5% 1/10W MF-LF 603
GD2_BST
D5020 BAS16-75V-0.25A SOT23-LF
GD2_VREG
C5023 1UF 20% 16V CERM 1206
GD2_VPN
R5022 200 5% 1/16W MF-LF 402
VC_AUX2
C5024 470PF 10% 50V CERM 402
GD2_PN
C5021 1000UF 20% 16V ELEC TH-KZJ-LF
C5034 1000UF 20% 16V ELEC TH-KZJ-LF
C5022 10UF 10% 16V CERM 1210
CRITICAL Q5020 NTD60N02R CASE369-LF
R5051 10K 5% 1/16W MF-LF 402
R5020 1 5% 1/16W MF-LF 402
GD2_BG
CRITICAL Q5021 NTD70N03R CASE369-LF
CRITICAL Q5023 NTD70N03R CASE369-LF
C5025 0.0022UF 10% 50V CERM 402
C5026 3300PF 10% 50V CERM 603
R5021 1.0 5% 1/4W MF-LF 1206
GD2_FET_RC
CRITICAL L5020 0.6UH-24A TH2
PPVCORE_CPU
C5028 1800UF 20% 6.3V ELEC TH-KZJ-LF
C5033 1800UF 20% 6.3V ELEC TH-KZJ-LF
C5040 1800UF 20% 6.3V ELEC TH-KZJ-LF
C5041 1800UF 20% 6.3V ELEC TH-KZJ-LF
C5042 1800UF 20% 6.3V ELEC TH-KZJ-LF
C5043 1800UF 20% 6.3V ELEC TH-KZJ-LF

PHYSICAL CONSTRAINTS

	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
VC_OSCREF	0.25 MM	0.20 MM	R820
CPU_VID_R<0..5>	0.25 MM	0.20 MM	R830
VC_DACSTEP	0.25 MM	0.20 MM	R821
VC_AGND	0.50 MM	0.20 MM	R822
VC_BGOUT	0.25 MM	0.20 MM	R823
VC_OS1	0.25 MM	0.20 MM	R824
VC_OS2	0.25 MM	0.20 MM	R825
VC_VCC	0.25 MM	0.25 MM	R831
VC_OS_HUB	0.25 MM	0.20 MM	R826
VC_OUTSEN	0.25 MM	0.20 MM	R827
VC_OUTSEN_R	0.25 MM	0.20 MM	R828
VCORE_SENSE_GND	0.25 MM	0.20 MM	R829
VCORE_SENSE_VOUT	0.25 MM	0.20 MM	R832
VC_AUX1	0.25 MM	0.25 MM	R833
VC_AUX2	0.25 MM	0.25 MM	R834
VC_OUT1	0.45 MM	0.25 MM	R835
VC_OUT2	0.45 MM	0.25 MM	R853
VC_ERROUT	0.25 MM	0.20 MM	R855
VC_ERROUT_RC	0.25 MM	0.20 MM	R856
VC_OS_HUB_RC	0.25 MM	0.20 MM	R854

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0340	376S0388		Q5010,Q5020	
376S0341	376S0390		Q5011,Q5013,Q5021,Q5023	

CPU VCORE VREG

SYNC_MASTER=M23-HS SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 50 OF 154	

56 55 50 49 48 43 =PPVCORE_CPU

CRITICAL

C5200 10UF 10% 6.3V X5R 805	C5212 10UF 10% 6.3V X5R 805	C5223 10UF 10% 6.3V X5R 805	C5234 10UF 10% 6.3V X5R 805	C5245 10UF 10% 6.3V X5R 805	C5201 10UF 10% 6.3V X5R 805	C5289 10UF 10% 6.3V X5R 805	C5278 10UF 10% 6.3V X5R 805	C5267 10UF 10% 6.3V X5R 805	C5256 10UF 10% 6.3V X5R 805
C5213 10UF 10% 6.3V X5R 805	C5211 10UF 10% 6.3V X5R 805	C5210 10UF 10% 6.3V X5R 805	C5209 10UF 10% 6.3V X5R 805	C5208 10UF 10% 6.3V X5R 805	C5207 10UF 10% 6.3V X5R 805	C5206 10UF 10% 6.3V X5R 805	C5205 10UF 10% 6.3V X5R 805	C5204 10UF 10% 6.3V X5R 805	C5203 10UF 10% 6.3V X5R 805
C5224 10UF 10% 6.3V X5R 805	C5222 10UF 10% 6.3V X5R 805	C5221 10UF 10% 6.3V X5R 805	C5220 10UF 10% 6.3V X5R 805	C5219 10UF 10% 6.3V X5R 805	C5218 10UF 10% 6.3V X5R 805	C5217 10UF 10% 6.3V X5R 805	C5216 10UF 10% 6.3V X5R 805	C5215 10UF 10% 6.3V X5R 805	C5214 10UF 10% 6.3V X5R 805
C5235 10UF 10% 6.3V X5R 805	C5233 10UF 10% 6.3V X5R 805	C5232 10UF 10% 6.3V X5R 805	C5231 10UF 10% 6.3V X5R 805	C5230 10UF 10% 6.3V X5R 805	C5229 10UF 10% 6.3V X5R 805	C5228 10UF 10% 6.3V X5R 805	C5227 10UF 10% 6.3V X5R 805	C5226 10UF 10% 6.3V X5R 805	C5225 10UF 10% 6.3V X5R 805
C5246 10UF 10% 6.3V X5R 805	C5244 10UF 10% 6.3V X5R 805	C5243 10UF 10% 6.3V X5R 805	C5242 10UF 10% 6.3V X5R 805	C5241 10UF 10% 6.3V X5R 805	C5240 10UF 10% 6.3V X5R 805	C5239 10UF 10% 6.3V X5R 805	C5238 10UF 10% 6.3V X5R 805	C5237 10UF 10% 6.3V X5R 805	C5236 10UF 10% 6.3V X5R 805
C5257 10UF 10% 6.3V X5R 805	C5255 10UF 10% 6.3V X5R 805	C5254 10UF 10% 6.3V X5R 805	C5253 10UF 10% 6.3V X5R 805	C5252 10UF 10% 6.3V X5R 805	C5251 10UF 10% 6.3V X5R 805	C5250 10UF 10% 6.3V X5R 805	C5249 10UF 10% 6.3V X5R 805	C5248 10UF 10% 6.3V X5R 805	C5247 10UF 10% 6.3V X5R 805
C5268 10UF 10% 6.3V X5R 805	C5266 10UF 10% 6.3V X5R 805	C5265 10UF 10% 6.3V X5R 805	C5264 10UF 10% 6.3V X5R 805	C5263 10UF 10% 6.3V X5R 805	C5262 10UF 10% 6.3V X5R 805	C5261 10UF 10% 6.3V X5R 805	C5260 10UF 10% 6.3V X5R 805	C5259 10UF 10% 6.3V X5R 805	C5258 10UF 10% 6.3V X5R 805
C5279 10UF 10% 6.3V X5R 805	C5277 10UF 10% 6.3V X5R 805	C5276 10UF 10% 6.3V X5R 805	C5275 10UF 10% 6.3V X5R 805	C5274 10UF 10% 6.3V X5R 805	C5273 10UF 10% 6.3V X5R 805	C5272 10UF 10% 6.3V X5R 805	C5271 10UF 10% 6.3V X5R 805	C5270 10UF 10% 6.3V X5R 805	C5269 10UF 10% 6.3V X5R 805
C5290 10UF 10% 6.3V X5R 805	C5288 10UF 10% 6.3V X5R 805	C5287 10UF 10% 6.3V X5R 805	C5286 10UF 10% 6.3V X5R 805	C5285 10UF 10% 6.3V X5R 805	C5284 10UF 10% 6.3V X5R 805	C5283 10UF 10% 6.3V X5R 805	C5282 10UF 10% 6.3V X5R 805	C5281 10UF 10% 6.3V X5R 805	C5280 10UF 10% 6.3V X5R 805
C5202 10UF 10% 6.3V X5R 805	C5299 10UF 10% 6.3V X5R 805	C5298 10UF 10% 6.3V X5R 805	C5297 10UF 10% 6.3V X5R 805	C5296 10UF 10% 6.3V X5R 805	C5295 10UF 10% 6.3V X5R 805	C5294 10UF 10% 6.3V X5R 805	C5293 10UF 10% 6.3V X5R 805	C5292 10UF 10% 6.3V X5R 805	C5291 10UF 10% 6.3V X5R 805

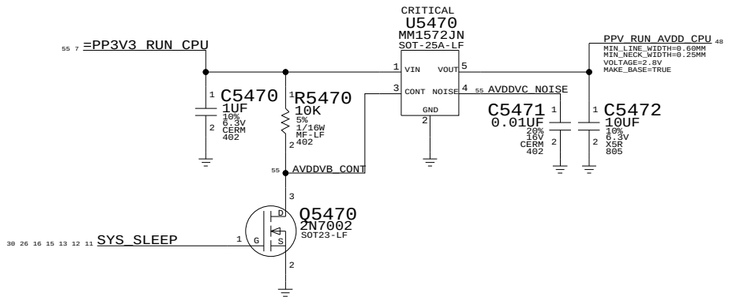
CPU VCORE MORE BYPASS

SYNC_MASTER=FINO-HS SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE NONE	SHT 52 OF 154	

PROCESSOR AVDD VREG



CPU AVDD VREG

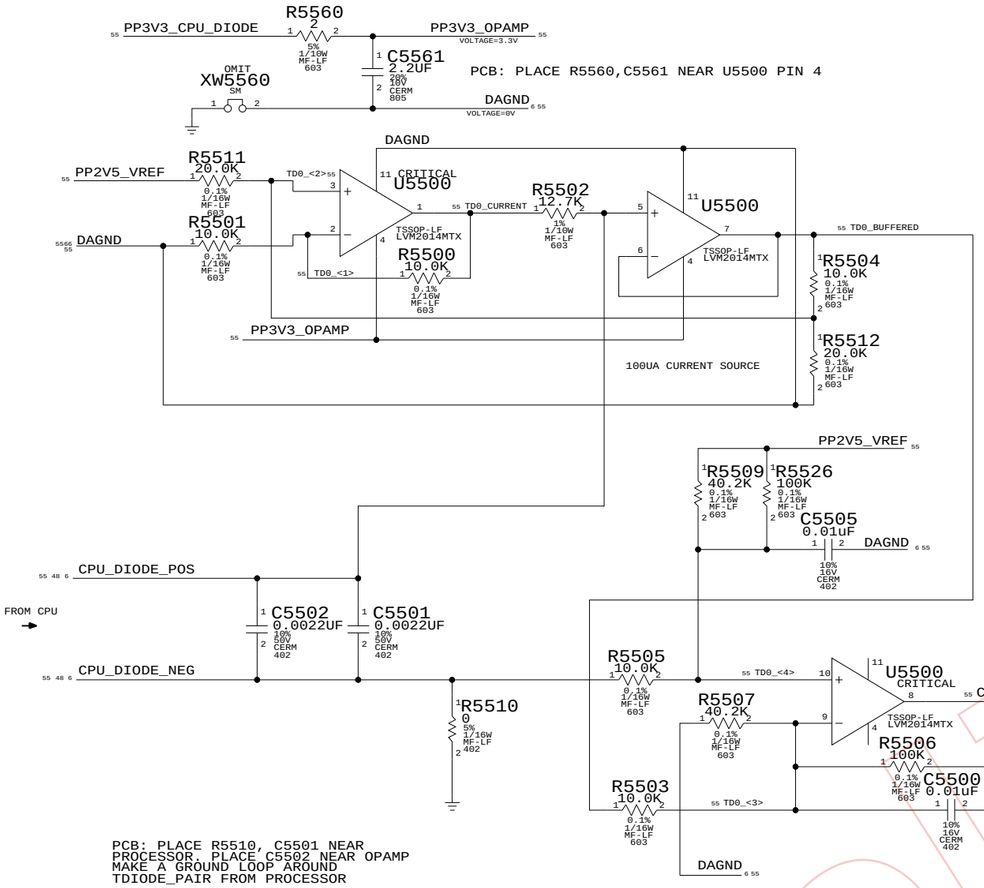
SYNC_MASTER=FINO-HS SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

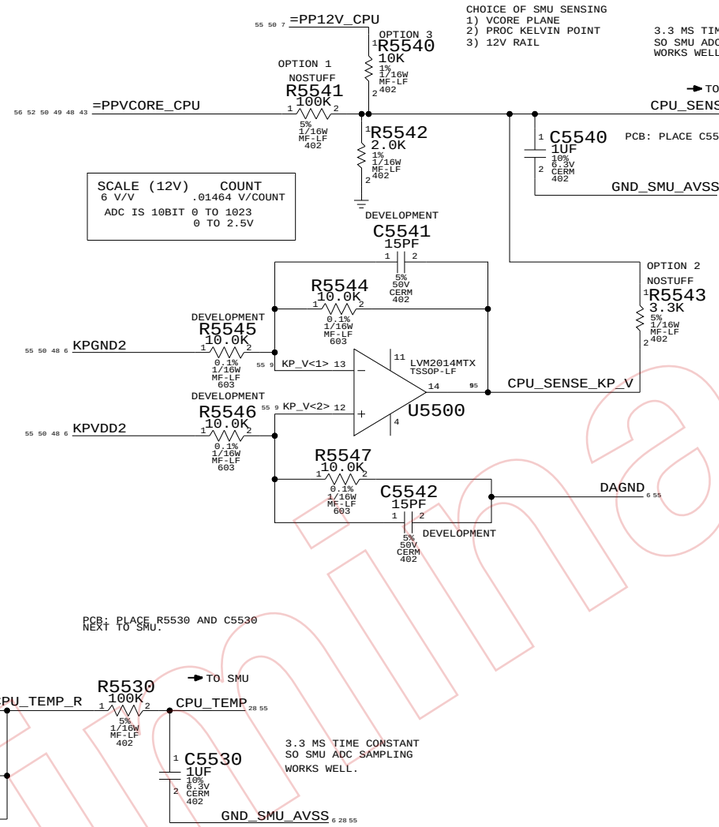
SIZE	DRAWING NUMBER	REV.
D	051-6790	E

SCALE NONE SHT 54 OF 154

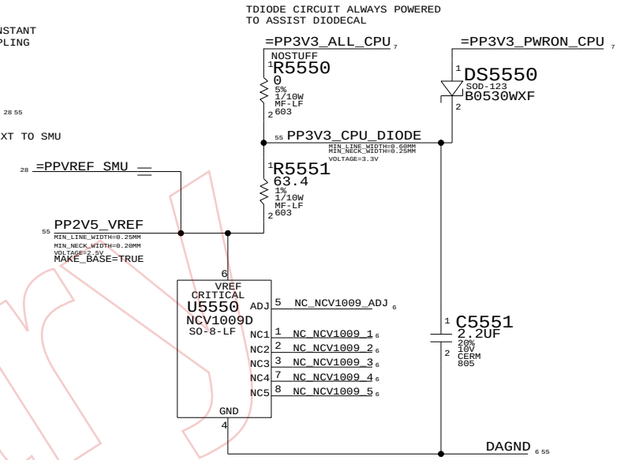
PROCESSOR TEMP SENSE (TDIODE EXCITATION CIRCUIT AND OPAMP)



PROCESSOR VCORE VOLTAGE SENSE



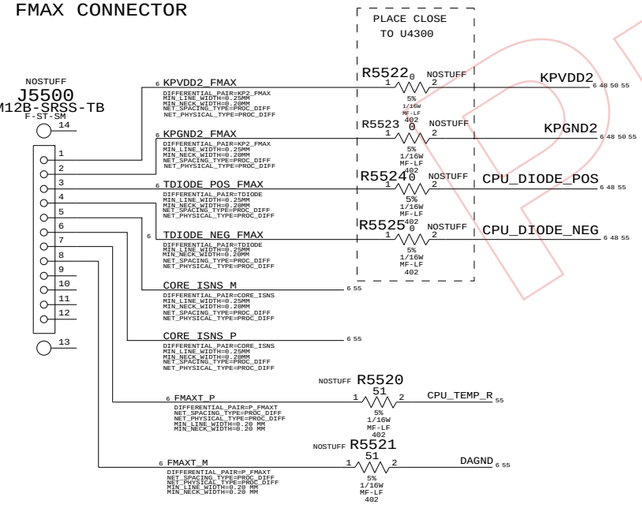
2.5V PRECISION VOLTAGE REFERENCE SOURCE



PHYSICAL CONSTRAINTS

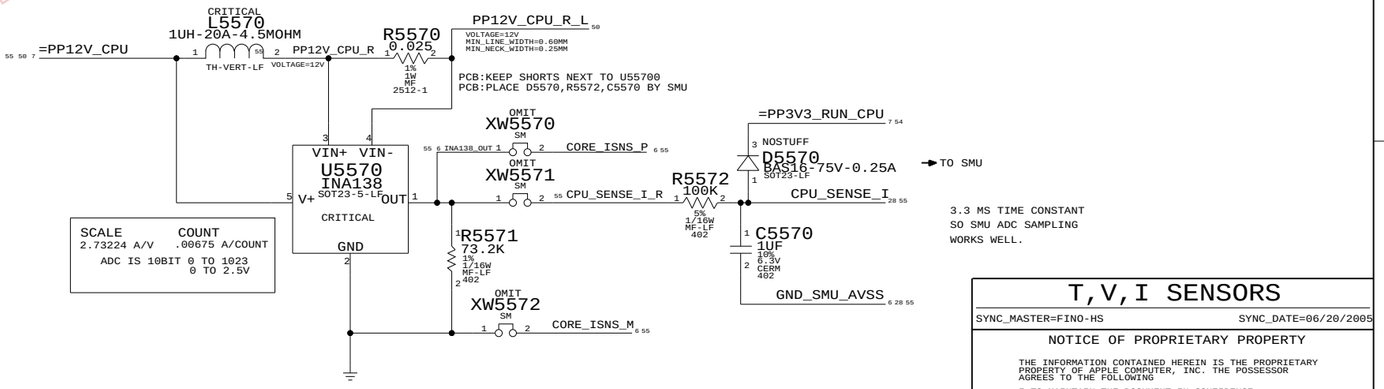
	MIN_LINE_WIDTH	MIN_NECK_WIDTH
TD0_<1..4>	0.25 MM	0.25 MM
PP12V_CPU_R	0.60 MM	0.25 MM
TD0_CURRENT	0.25 MM	0.25 MM
TD0_BUFFERED	0.25 MM	0.25 MM
KP_V<1..2>	0.25 MM	0.25 MM
CPU_SENSE_KP_V	0.25 MM	0.25 MM
PP3V3_OPAMP	0.60 MM	0.25 MM
INA138_OUT	0.25 MM	0.25 MM
CPU_SENSE_I_R	0.25 MM	0.25 MM
CPU_SENSE_I	0.25 MM	0.25 MM
CPU_SENSE_V	0.25 MM	0.25 MM
CPU_TEMP	0.25 MM	0.20 MM
CPU_TEMP_R	0.25 MM	0.20 MM
AVDDVC_NOISE	0.25 MM	0.20 MM
AVDDVB_CONT	0.25 MM	0.20 MM
PP12V_CPU_R	0.60 MM	0.25 MM
DAGND	0.60 MM	0.25 MM

FMAX CONNECTOR



PROCESSOR VCORE CURRENT SENSE

(USING 12V INPUT CURRENT TO DERIVE CPU CURRENT)



T,V,I SENSORS

SYNC_MASTER=FINO-HS SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 55 OF 154	

CONNECT PULSAR CLKS TO CPU/NB

EI_CPU_SYSCLK_P	MAKE_BASE=TRUE	EI_CPU_A_SYSCLK_P	26
EI_CPU_SYSCLK_N	MAKE_BASE=TRUE	EI_CPU_A_SYSCLK_N	26
EI_CPU_APSYNC	MAKE_BASE=TRUE	CPU_A_APSYNC	26
EI_CPU_TBEN_CLK	MAKE_BASE=TRUE	CPU_A_TBEN_CLK_US	26
EI_NB_APSYNC	MAKE_BASE=TRUE	NB_APSYNC	26 42

CONNECT KODIAK EI A TO/FROM CPU

EI_NB_TO_CPU_CLK_P		EI_NB_TO_CPU_A_CLK_P	42
EI_NB_TO_CPU_CLK_N	MAKE_BASE=TRUE	EI_NB_TO_CPU_A_CLK_N	42
EI_NB_TO_CPU_AD<0..43>	MAKE_BASE=TRUE	EI_NB_TO_CPU_A_AD<0..43>	42
EI_NB_TO_CPU_SR_P<0..1>	MAKE_BASE=TRUE	EI_NB_TO_CPU_A_SR_P<0..1>	42
EI_NB_TO_CPU_SR_N<0..1>	MAKE_BASE=TRUE	EI_NB_TO_CPU_A_SR_N<0..1>	42
	MAKE_BASE=TRUE		
EI_CPU_TO_NB_CLK_P		EI_CPU_A_TO_NB_CLK_P	42
EI_CPU_TO_NB_CLK_N	MAKE_BASE=TRUE	EI_CPU_A_TO_NB_CLK_N	42
EI_CPU_TO_NB_AD<0..43>	MAKE_BASE=TRUE	EI_CPU_A_TO_NB_AD<0..43>	42
EI_CPU_TO_NB_SR_P<0..1>	MAKE_BASE=TRUE	EI_CPU_A_TO_NB_SR_P<0..1>	42
EI_CPU_TO_NB_SR_N<0..1>	MAKE_BASE=TRUE	EI_CPU_A_TO_NB_SR_N<0..1>	42
	MAKE_BASE=TRUE		

CONNECT CPU TO KODIAK QREQ A0

CPU_TO_NB_QREQ_L		CPU_A0_TO_NB_QREQ_L	42
	MAKE_BASE=TRUE		

CONNECT CPU TO KODIAK QACK A0, NC OTHERWISE

CPU_QACK_L		CPU_A0_QACK_L	42
NC_CPU_A1_QACK_L	MAKE_BASE=TRUE	CPU_A1_QACK_L	42
NC_CPU_B0_QACK_L	MAKE_BASE=TRUE	CPU_B0_QACK_L	44
NC_CPU_B1_QACK_L	MAKE_BASE=TRUE	CPU_B1_QACK_L	44
	MAKE_BASE=TRUE		

CONNECT CPU TO KODIAK/SHASTA INT A0, NC OTHERWISE

CPU_INT_L		CPU_A0_INT_R_L	24 56
NC_NB_CPU_A1_INT_L	MAKE_BASE=TRUE	NB_CPU_A1_INT_L	42
NC_NB_CPU_B0_INT_L	MAKE_BASE=TRUE	NB_CPU_B0_INT_L	44
NC_NB_CPU_B1_INT_L	MAKE_BASE=TRUE	NB_CPU_B1_INT_L	44
	MAKE_BASE=TRUE		

CONNECT CPU TO SHASTA SRESET A0, NC OTHERWISE

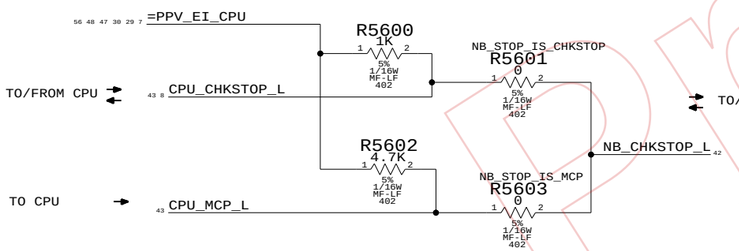
CPU_SRESET_L_R		SB_CPU_A0_SRESET_L	24 56
NOTUSED_CPU_A1_SRESET_L	MAKE_BASE=TRUE	SB_CPU_A1_SRESET_L	24 56
NOTUSED_CPU_B0_SRESET_L	MAKE_BASE=TRUE	SB_CPU_B0_SRESET_L	24 56
NOTUSED_CPU_B1_SRESET_L	MAKE_BASE=TRUE	SB_CPU_B1_SRESET_L	24 56
	MAKE_BASE=TRUE		

WIRE OUT KODIAK AND CPU SIGNALS FOR TP'S

TP_NB_B_TRIGGER_OUT	MAKE_BASE=TRUE	NB_B_TRIGGER_OUT	44
TP_NB_A_TRIGGER_OUT	MAKE_BASE=TRUE	NB_A_TRIGGER_OUT	42
TP_CPU_APSYNCOUT	MAKE_BASE=TRUE	CPU_APSYNCOUT	43
TP_CPU_TRIGGER_IN	MAKE_BASE=TRUE	CPU_TRIGGER_IN	43 47
TP_CPU_TRIGGER_OUT	MAKE_BASE=TRUE	CPU_TRIGGER_OUT	43
NC_PSRO	MAKE_BASE=TRUE	CPU_PSRO	43
NC_PSRO_ENABLE	MAKE_BASE=TRUE	CPU_PSRO_ENABLE	43
TP_CPU_ATTENTION	MAKE_BASE=TRUE	CPU_ATTENTION	43
NC_CPU_AFN	MAKE_BASE=TRUE	CPU_AFN	43
	MAKE_BASE=TRUE		

REMEMBER TO UPDATE NO_TEST PROPERTIES ON PG 6

CPU CHKSTOP OR MCP TO NB



EI BUS AND SYSCLK CONSTRAINT LABELS

	ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR	
56 43 9 EI_CPU_TO_NB_CLK_P	EICNCLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	128
56 43 9 EI_CPU_TO_NB_CLK_N	EICNCLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	127
56 43 EI_CPU_TO_NB_AD<0..21>	EICNCAD	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD		131
56 43 9 EI_CPU_TO_NB_SR_P<0..1>	EICNCSR	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD		134
56 43 9 EI_CPU_TO_NB_SR_N<0..1>	EICNCSR	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD		132
56 43 9 EI_NB_TO_CPU_CLK_P	EINCCLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	129
56 43 9 EI_NB_TO_CPU_CLK_N	EINCCLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	130
56 43 EI_NB_TO_CPU_AD<0..43>	EINCCAD	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD		135
56 43 9 EI_NB_TO_CPU_SR_P<0..1>	EINCCAD	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD		140
56 43 9 EI_NB_TO_CPU_SR_N<0..1>	EINCCAD	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD		137
56 EI_NB_APSYNC	EIPNAPSYNC	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD		
56 43 EI_CPU_APSYNC	EIPCAPSYNC	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD		138
56 43 9 EI_CPU_SYSCLK_P	EIPCSYSCLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_CPU_SYSCLK	139
56 43 EI_CPU_SYSCLK_N	EIPCSYSCLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_CPU_SYSCLK	141
42 26 EI_NB_SYSCLK_P	EIPNSYSCLK_P	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_NB_SYSCLK	136
42 26 EI_NB_SYSCLK_N	EIPNSYSCLK_N	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_NB_SYSCLK	142
56 43 EI_CPU_TO_NB_AD<22>	EICNCAD_PP	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD		1496
56 43 EI_CPU_TO_NB_AD<23..43>	EICNCAD	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD		1496

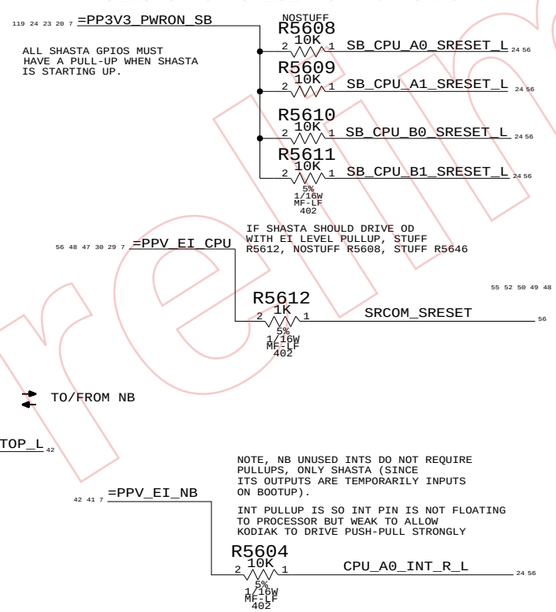
NC KODIAK EI B OUTPUT PORT

NC_EI_NB_TO_CPU_B_CLK_P		EI_NB_TO_CPU_B_CLK_P	44
NC_EI_NB_TO_CPU_B_CLK_N	MAKE_BASE=TRUE	EI_NB_TO_CPU_B_CLK_N	44
NC_EI_NB_TO_CPU_B_AD<0..43>	MAKE_BASE=TRUE	EI_NB_TO_CPU_B_AD<0..43>	44
NC_EI_NB_TO_CPU_B_SR_P<0..1>	MAKE_BASE=TRUE	EI_NB_TO_CPU_B_SR_P<0..1>	44
NC_EI_NB_TO_CPU_B_SR_N<0..1>	MAKE_BASE=TRUE	EI_NB_TO_CPU_B_SR_N<0..1>	44
	MAKE_BASE=TRUE		

NC KODIAK EI B INPUT PORT

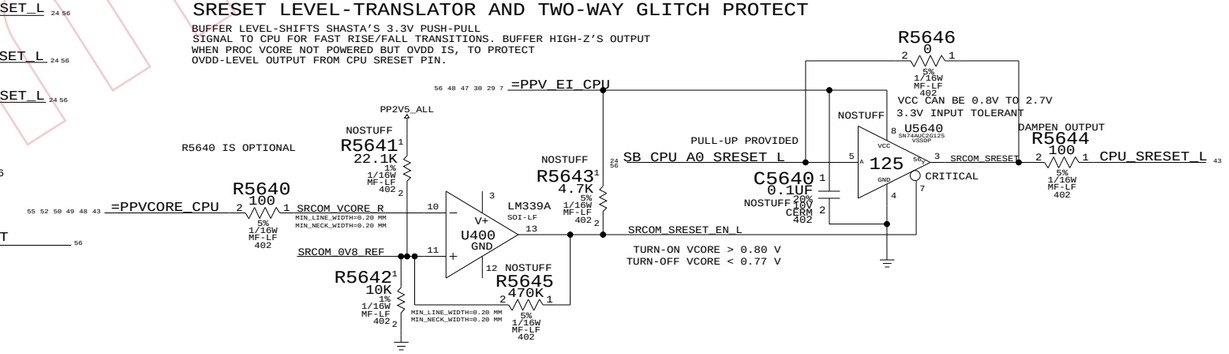
NC_EI_CPU_B_TO_NB_CLK_P		EI_CPU_B_TO_NB_CLK_P	44
NC_EI_CPU_B_TO_NB_CLK_N	MAKE_BASE=TRUE	EI_CPU_B_TO_NB_CLK_N	44
NC_EI_CPU_B_TO_NB_AD<0..43>	MAKE_BASE=TRUE	EI_CPU_B_TO_NB_AD<0..43>	44
NC_EI_CPU_B_TO_NB_SR_P<0..1>	MAKE_BASE=TRUE	EI_CPU_B_TO_NB_SR_P<0..1>	44
NC_EI_CPU_B_TO_NB_SR_N<0..1>	MAKE_BASE=TRUE	EI_CPU_B_TO_NB_SR_N<0..1>	44
	MAKE_BASE=TRUE		

PULLUPS FOR SRESET'S FROM SHASTA



SRESET LEVEL-TRANSLATOR AND TWO-WAY GLITCH PROTECT

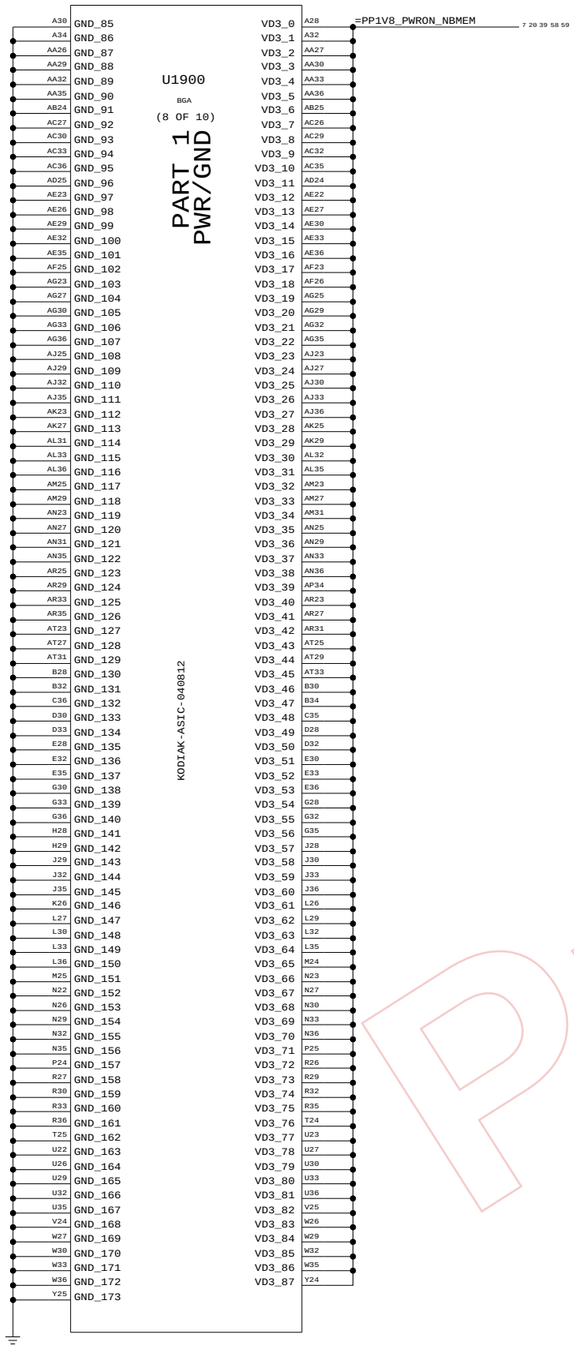
BUFFER LEVEL-SHIFTS SHASTA'S 3.3V PUSH-PULL SIGNAL TO CPU FOR FAST RISE/FALL TRANSITIONS. BUFFER HIGH-Z'S OUTPUT WHEN PROC VCORE NOT POWERED BUT OVDD IS, TO PROTECT OVDD-LEVEL OUTPUT FROM CPU SRESET PIN.



CPU ALIASES & MISC

SYNC_MASTER=FINO-HS SYNC_DATE=06/20/2005

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6790	REV. E
	SCALE NONE	SHT 56 OF 154	



59 58 39 20 7 =PP1V8_PWRON_NBMEM

C5836 C5835 C5834 C5832 C5831 C5830 C5829 C5822 C5811 C5800
C5864 C5859 C5857 C5842 C5840 C5837 C5828 C5801 C5855 C5833
C5863 C5860 C5858 C5843 C5841 C5838 C5827 C5802 C5866 C5844
C5865 C5862 C5861 C5846 C5845 C5839 C5826 C5803 C5887 C5877
C5874 C5869 C5867 C5852 C5850 C5847 C5825 C5810 C5806 C5804
C5873 C5870 C5868 C5853 C5851 C5848 C5824 C5812 C5807 C5805
C5875 C5872 C5871 C5856 C5854 C5849 C5823 C5813 C5809 C5808
C5886 C5885 C5883 C5881 C5879 C5876 C5821 C5818 C5816 C5814
C5884 C5882 C5880 C5878 C5820 C5819 C5817 C5815

1UF 10% 6.3V CERM 402

Q63: SEE P.20 FOR MORE DECOUPLING CAPS FOR THESE PINS.

KODIAC NBMEM PWR & CAPS

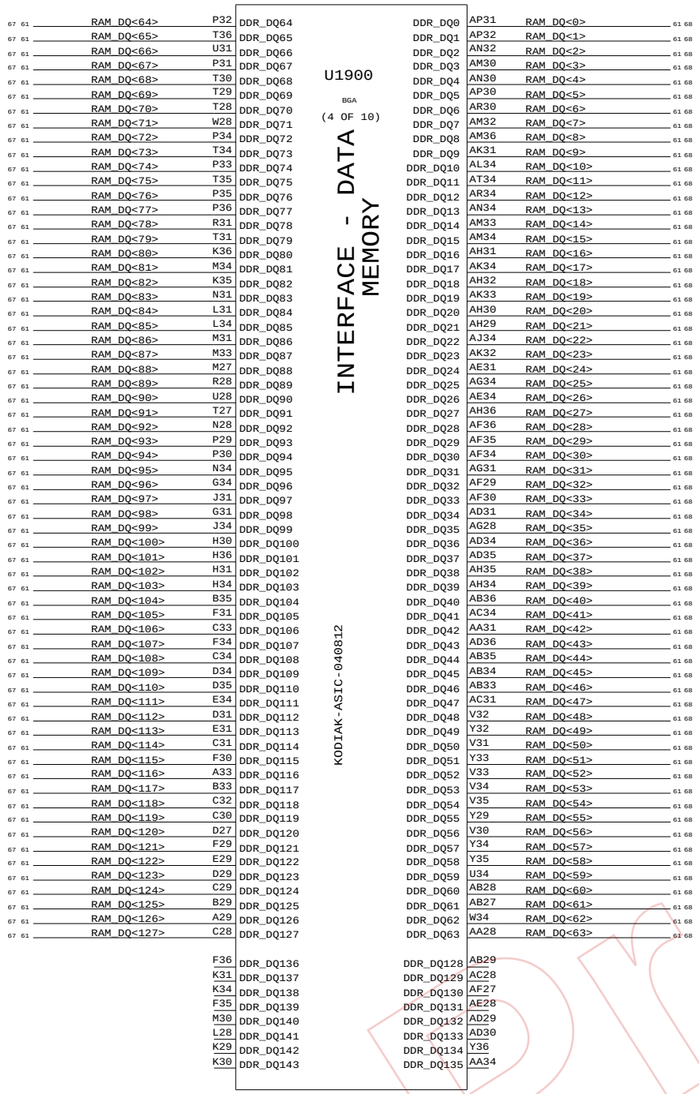
SYNC_MASTER=Q63 SYNC_DATE=08/01/2005

APPLE COMPUTER INC.

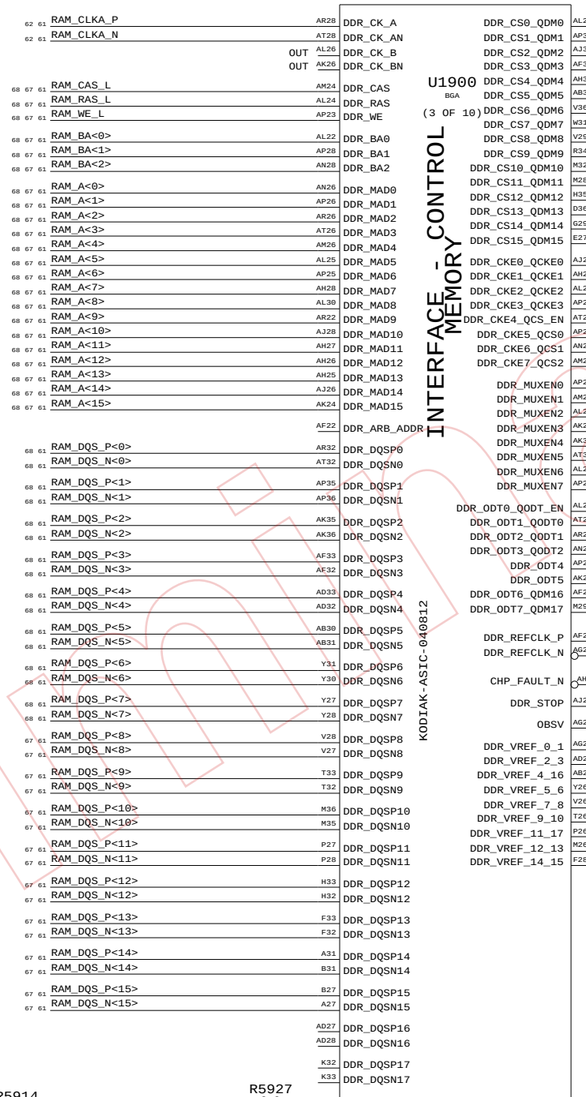
SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 58 OF 154	

LAST_MODIFIED=Tue Nov 1 14:56:09 2005

DRAWING



DQ/DQS OKAY TO TIE TO GROUND FOR THERMALS

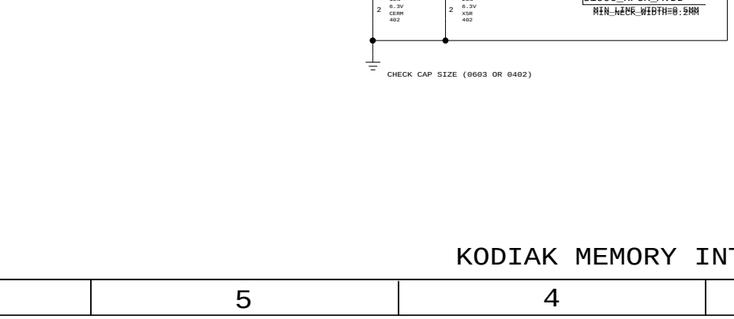


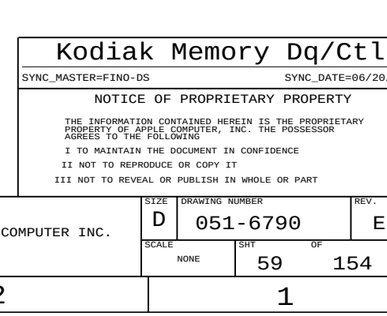
Kodiak 128bit CS/CKE/ODT mapping (Q63 style)

DIMM RANK	CS*	CKE	ODT	M23 Function	D bits
A0	0	0	0	onboard DRAM	0:63
A1	1	1	-	*unused*	0:63
B2	2	0	4	J6700 rank 1	64:127
B3	3	1	-	J6700 rank 2	64:127
C4	2	2	1	*unused*	0:63
C5	3	3	-	*unused*	0:63
D6	10	2	5	*unused*	64:127
D7	11	3	-	*unused*	64:127
E8	4	4	2	*unused*	0:63
E9	5	5	-	*unused*	0:63
F10	12	4	6	*unused*	64:127
F11	13	5	-	*unused*	64:127
G12	6	6	3	*unused*	0:63
G13	7	7	-	*unused*	0:63
H14	14	6	7	*unused*	64:127
H15	15	7	-	*unused*	64:127

Kodiak 128bit CS/CKE/ODT mapping (v1.1 only)

DIMM RANK	CS*	CKE	ODT	M23 Function	D bits
A0	0	0	0	onboard DRAM	0:63
A1	1	1	-	*unused*	0:63
B2	4	4	2	J6700 rank 1	64:127
B3	5	5	-	J6700 rank 2	64:127
C4	2	2	1	*unused*	0:63
C5	3	3	-	*unused*	0:63
D6	6	6	3	*unused*	64:127
D7	7	7	-	*unused*	64:127





PLACE CLOSE TO KODIAK PIN
WITHIN 20MIL FROM VIA FOR EACH VREF

Kodiak Memory Dq/Ctl

SYNC_MASTER=FINO-DS SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 59 OF 154	

KODIAK MEMORY INTERFACE

ALL R PACKS ARE 1/16W 5%

=PP1V8_RUN_RAM

RAM_A<0>
RAM_A<1>
RAM_A<2>
RAM_A<3>
RAM_A<4>
RAM_A<6>
RAM_A<5>
RAM_A<7>

RP6107 RP6106 RP6106 RP6105 RP6105 RP6104 RP6104 RP6103
240 5% 1/16W SM-LF

C6100 0.1UF 20% 10V CERM 402
C6102 0.1UF 20% 10V CERM 402

RPACK/RES NEAR/UNDER CONNECTOR

=PP1V8_RUN_RAM

RAM_A<8>
RAM_A<9>
RAM_A<10>
RAM_A<11>
RAM_A<12>
RAM_A<13>
RAM_A<14>
RAM_A<15>

RP6103 RP6102 RP6108 RP6102 RP6101 RP6110 RP6100 RP6100
240 5% 1/16W SM-LF

C6103 0.1UF 20% 10V CERM 402
C6104 0.1UF 20% 10V CERM 402

RPACK/RES NEAR/UNDER CONNECTOR

=PP1V8_RUN_RAM

1V8_RUN_RAM_CKE

RP6150 RP6152 RP6151 RP6151 RP6150
240 5% 1/16W SM-LF

C6105 0.1UF 20% 10V CERM 402
C6106 0.1UF 20% 10V CERM 402

R6121 10 402 RAM_CS_L<4> — RAM_M23_128 — RAM_CS_DIMM_A
R6161 10 402 RAM_CS_L<8> — RAM_Q63_128
SHARE PIN 2 PADS

R6122 10 402 RAM_CS_L<5> — RAM_M23_128 — RAM_CS_DIMM_B
R6162 10 402 RAM_CS_L<9> — RAM_Q63_128
SHARE PIN 2 PADS

R6123 10 402 RAM_CKE<4> — RAM_M23_128 — RAM_CKE_DIMM_A
R6163 10 402 RAM_CKE<0> — RAM_Q63_128
SHARE PIN 2 PADS

R6124 10 402 RAM_CKE<5> — RAM_M23_128 — RAM_CKE_DIMM_B
R6164 10 402 RAM_CKE<1> — RAM_Q63_128
SHARE PIN 2 PADS

R6125 10 402 RAM_ODT<2> — RAM_M23_128 — RAM_ODT_DIMM_A
R6165 10 402 RAM_ODT<4> — RAM_Q63_128
SHARE PIN 2 PADS

SERIES R NEAR KODIAK

RP6150 RP6152 RP6151 RP6151 RP6150
240 5% 1/16W SM-LF

RPACK/RES NEAR/UNDER CONNECTOR

CS/CKE/ODT TERMINATION FOR DIMM STICK

=PP1V8_RUN_RAM

RAM_RAS_L
RAM_CAS_L
RAM_WE_L

RP6109 RP6110 RP6109
240 5% 1/16W SM-LF

C6108 0.1UF 20% 10V CERM 402

RPACK/RES NEAR/UNDER CONNECTOR

=PP1V8_RUN_RAM

RAM_BA<0>
RAM_BA<1>
RAM_BA<2>

RP6108 RP6107 RP6101
240 5% 1/16W SM-LF

C6109 0.1UF 20% 10V CERM 402

RPACK/RES NEAR/UNDER CONNECTOR

1V8_RUN_RAM_CKE
MIN_LINE_WIDTH=0.0MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.8V
NET_SPACING_TYPE=POWER

=PP1V8_RUN_RAM

SERIES R NEAR KODIAK

RP6170 240 5% 1/16W MF-LF 402

R6173 240 1/16W MF-LF 402
C6107 0.1UF 20% 10V CERM 402

R6172 10 402 RAM_CS_L<0> — RAM_CS_L_R<0>
R6175 10 402 RAM_CKE<0> — RAM_CKE_R<0>
R6178 10 402 RAM_ODT<0> — RAM_ODT_R<0>

R6174 240 1/16W MF-LF 402

RES NEAR BRANCH POINT
CS/CKE/ODT TERMINATION FOR ONBOARD DRAM

RAM_CS_L<0>	RAM_CS_ONBOARD_EC	RAM_CSCKEODT	RAM_CSCKEODT	P245
RAM_CS_L<4>	RAM_CS_DIMM_EC	RAM_CSCKEODT	RAM_CSCKEODT	P487
RAM_CS_L<5>	RAM_CS_DIMM_EC	RAM_CSCKEODT	RAM_CSCKEODT	P242
RAM_CS_L<8>		RAM_CSCKEODT	RAM_CSCKEODT	P244
RAM_CS_L<9>		RAM_CSCKEODT	RAM_CSCKEODT	P244
RAM_CS_L_R<0>		RAM_CSCKEODT	RAM_CSCKEODT	P238
RAM_CS_DIMM_A		RAM_CSCKEODT	RAM_CSCKEODT	P241
RAM_CS_DIMM_B		RAM_CSCKEODT	RAM_CSCKEODT	P675
RAM_CKE<0>	RAM_CKE_DIMM_ONBOARD_EC	RAM_CSCKEODT	RAM_CSCKEODT	P234
RAM_CKE<1>	RAM_CKE_DIMM_EC	RAM_CSCKEODT	RAM_CSCKEODT	P236
RAM_CKE<4>		RAM_CSCKEODT	RAM_CSCKEODT	P235
RAM_CKE<5>		RAM_CSCKEODT	RAM_CSCKEODT	P237
RAM_CKE_R<0>		RAM_CSCKEODT	RAM_CSCKEODT	P239
RAM_CKE_DIMM_B		RAM_CSCKEODT	RAM_CSCKEODT	P1692
RAM_CKE_DIMM_A		RAM_CSCKEODT	RAM_CSCKEODT	P1232
RAM_ODT<0>	RAM_ODT_ONBOARD_EC	RAM_CSCKEODT	RAM_CSCKEODT	P1674
RAM_ODT<2>	RAM_ODT_DIMM_EC	RAM_CSCKEODT	RAM_CSCKEODT	P1676
RAM_ODT<4>		RAM_CSCKEODT	RAM_CSCKEODT	P1677
RAM_ODT_R<0>		RAM_CSCKEODT	RAM_CSCKEODT	P1693
RAM_ODT_DIMM_A		RAM_CSCKEODT	RAM_CSCKEODT	P1694

		ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
RAM_CLKA_P		RAM_KODIAK_CLK_EC	RAM_CLK	RAM_CLK	RAM_KODIAK_CLK_DP	P206
RAM_CLKA_N			RAM_CLK	RAM_CLK	RAM_KODIAK_CLK_DP	P207
RAM_DIMM_A_CLK_P0		RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK0_DP	P230
RAM_DIMM_A_CLK_N0		RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK0_DP	P231
RAM_DIMM_A_CLK_P1		RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK1_DP	P232
RAM_DIMM_A_CLK_N1		RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK1_DP	P233
RAM_DIMM_A_CLK_P2		RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK2_DP	P214
RAM_DIMM_A_CLK_N2		RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK2_DP	P215
RAM_ONBOARD_CLK_P0_1		RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK0_DP	P4416
RAM_ONBOARD_CLK_N0_1		RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK0_DP	P217
RAM_ONBOARD_CLK_P2_3		RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK2_DP	P218
RAM_ONBOARD_CLK_N2_3		RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK2_DP	P219
RAM_ONBOARD_CLK_P4_5		RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK4_DP	P220
RAM_ONBOARD_CLK_N4_5		RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK4_DP	P221
RAM_ONBOARD_CLK_P6_7		RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK6_DP	P222
RAM_ONBOARD_CLK_N6_7		RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK6_DP	P223
RAM_CLK_FBIN_P		RAM_FB_CLK_EC	RAM_CLK	RAM_CLK	RAM_FBIN_CLK_DP	P224
RAM_CLK_FBIN_N			RAM_CLK	RAM_CLK	RAM_FBIN_CLK_DP	P225
RAM_CLK_FBOUT_P			RAM_CLK	RAM_CLK	RAM_FBOUT_CLK_DP	P226
RAM_CLK_FBOUT_N			RAM_CLK	RAM_CLK	RAM_FBOUT_CLK_DP	P227
RAM_DQ<7..0>		RAM_DQS0_EC	RAM_CAD	RAM_CAD		P4428
RAM_DQS_P<0>		RAM_DQS0_EC	RAM_DQS	RAM_DQS	RAM_DQS_0_DP	P4429
RAM_DQS_N<0>		RAM_DQS0_EC	RAM_DQS	RAM_DQS	RAM_DQS_0_DP	P470
RAM_DQ<15..8>		RAM_DQS1_EC	RAM_CAD	RAM_CAD		P4430
RAM_DQS_P<1>		RAM_DQS1_EC	RAM_DQS	RAM_DQS	RAM_DQS_1_DP	P951
RAM_DQS_N<1>		RAM_DQS1_EC	RAM_DQS	RAM_DQS	RAM_DQS_1_DP	P471
RAM_DQ<23..16>		RAM_DQS2_EC	RAM_CAD	RAM_CAD		P4431
RAM_DQS_P<2>		RAM_DQS2_EC	RAM_DQS	RAM_DQS	RAM_DQS_2_DP	P4432
RAM_DQS_N<2>		RAM_DQS2_EC	RAM_DQS	RAM_DQS	RAM_DQS_2_DP	P472
RAM_DQ<31..24>		RAM_DQS3_EC	RAM_CAD	RAM_CAD		P4433
RAM_DQS_P<3>		RAM_DQS3_EC	RAM_DQS	RAM_DQS	RAM_DQS_3_DP	P4555
RAM_DQS_N<3>		RAM_DQS3_EC	RAM_DQS	RAM_DQS	RAM_DQS_3_DP	P473
RAM_DQ<39..32>		RAM_DQS4_EC	RAM_CAD	RAM_CAD		P4434
RAM_DQS_P<4>		RAM_DQS4_EC	RAM_DQS	RAM_DQS	RAM_DQS_4_DP	P4557
RAM_DQS_N<4>		RAM_DQS4_EC	RAM_DQS	RAM_DQS	RAM_DQS_4_DP	P474
RAM_DQ<47..40>		RAM_DQS5_EC	RAM_CAD	RAM_CAD		P4435
RAM_DQS_P<5>		RAM_DQS5_EC	RAM_DQS	RAM_DQS	RAM_DQS_5_DP	P4559
RAM_DQS_N<5>		RAM_DQS5_EC	RAM_DQS	RAM_DQS	RAM_DQS_5_DP	P475
RAM_DQ<55..48>		RAM_DQS6_EC	RAM_CAD	RAM_CAD		P4436
RAM_DQS_P<6>		RAM_DQS6_EC	RAM_DQS	RAM_DQS	RAM_DQS_6_DP	P4561
RAM_DQS_N<6>		RAM_DQS6_EC	RAM_DQS	RAM_DQS	RAM_DQS_6_DP	P476
RAM_DQ<63..56>		RAM_DQS7_EC	RAM_CAD	RAM_CAD		P4545
RAM_DQS_P<7>		RAM_DQS7_EC	RAM_DQS	RAM_DQS	RAM_DQS_7_DP	P4563
RAM_DQS_N<7>		RAM_DQS7_EC	RAM_DQS	RAM_DQS	RAM_DQS_7_DP	P477
RAM_DQ<71..64>		RAM_DQS8_EC	RAM_CAD	RAM_CAD		P4437
RAM_DQS_P<8>		RAM_DQS8_EC	RAM_DQS	RAM_DQS	RAM_DQS_8_DP	P4565
RAM_DQS_N<8>		RAM_DQS8_EC	RAM_DQS	RAM_DQS	RAM_DQS_8_DP	P478
RAM_DQ<79..72>		RAM_DQS9_EC	RAM_CAD	RAM_CAD		P4438
RAM_DQS_P<9>		RAM_DQS9_EC	RAM_DQS	RAM_DQS	RAM_DQS_9_DP	P4566
RAM_DQS_N<9>		RAM_DQS9_EC	RAM_DQS	RAM_DQS	RAM_DQS_9_DP	P479
RAM_DQ<87..80>		RAM_DQS10_EC	RAM_CAD	RAM_CAD		P4439
RAM_DQS_P<10>		RAM_DQS10_EC	RAM_DQS	RAM_DQS	RAM_DQS_10_DP	P4570
RAM_DQS_N<10>		RAM_DQS10_EC	RAM_DQS	RAM_DQS	RAM_DQS_10_DP	P480
RAM_DQ<95..88>		RAM_DQS11_EC	RAM_CAD	RAM_CAD		P4440
RAM_DQS_P<11>		RAM_DQS11_EC	RAM_DQS	RAM_DQS	RAM_DQS_11_DP	P4572
RAM_DQS_N<11>		RAM_DQS11_EC	RAM_DQS	RAM_DQS	RAM_DQS_11_DP	P481
RAM_DQ<103..96>		RAM_DQS12_EC	RAM_CAD	RAM_CAD		P4441
RAM_DQS_P<12>		RAM_DQS12_EC	RAM_DQS	RAM_DQS	RAM_DQS_12_DP	P4574
RAM_DQS_N<12>		RAM_DQS12_EC	RAM_DQS	RAM_DQS	RAM_DQS_12_DP	P482
RAM_DQ<111..104>		RAM_DQS13_EC	RAM_CAD	RAM_CAD		P4442
RAM_DQS_P<13>		RAM_DQS13_EC	RAM_DQS	RAM_DQS	RAM_DQS_13_DP	P4576
RAM_DQS_N<13>		RAM_DQS13_EC	RAM_DQS	RAM_DQS	RAM_DQS_13_DP	P4431
RAM_DQ<119..112>		RAM_DQS14_EC	RAM_CAD	RAM_CAD		P4278
RAM_DQS_P<14>		RAM_DQS14_EC	RAM_DQS	RAM_DQS	RAM_DQS_14_DP	P4276
RAM_DQS_N<14>		RAM_DQS14_EC	RAM_DQS	RAM_DQS	RAM_DQS_14_DP	P4434
RAM_DQ<127..120>		RAM_DQS15_EC	RAM_CAD	RAM_CAD		P4279
RAM_DQS_P<15>		RAM_DQS15_EC	RAM_DQS	RAM_DQS	RAM_DQS_15_DP	P4280
RAM_DQS_N<15>		RAM_DQS15_EC	RAM_DQS	RAM_DQS	RAM_DQS_15_DP	P4435
RAM_DQ_R<127..0>			RAM_CAD	RAM_CAD		P4354
RAM_DQS_P_R<15..0>			RAM_DQS	RAM_DQS		P4356
RAM_DQS_N_R<15..0>			RAM_DQS	RAM_DQS		P4436
RAM_A<15..14>		RAM_A_CTL_EC	RAM_CAD	RAM_CAD		P572
RAM_A<13..0>		RAM_A_CTL_EC	RAM_CAD	RAM_CAD		P2256
RAM_BA<1..0>		RAM_A_CTL_EC	RAM_CAD	RAM_CAD		P2258
RAM_BA<2>		RAM_A_CTL_1_EC	RAM_CAD	RAM_CAD		P574
RAM_RAS_L		RAM_A_CTL_EC	RAM_CAD	RAM_CAD		P2257
RAM_CAS_L		RAM_A_CTL_EC	RAM_CAD	RAM_CAD		P2259
RAM_WE_L		RAM_A_CTL_EC	RAM_CAD	RAM_CAD		P2260
RAM_A_R<15..0>			RAM_CAD	RAM_CAD		P4356
RAM_BA_R<2..0>			RAM_CAD	RAM_CAD		P4354
RAM_RAS_L_R			RAM_CAD	RAM_CAD		P4353
RAM_CAS_L_R			RAM_CAD	RAM_CAD		P4352
RAM_WE_L_R			RAM_CAD	RAM_CAD		P4351

RAM_CLK PRIMARY SPACING SET BASED ON DIFF IMPEDANCE
RAM_CLK LINE-LINE SPACING SET TO 15MIL
TOTAL LENGTH TOLERENCE = 20PS = 2.82MM

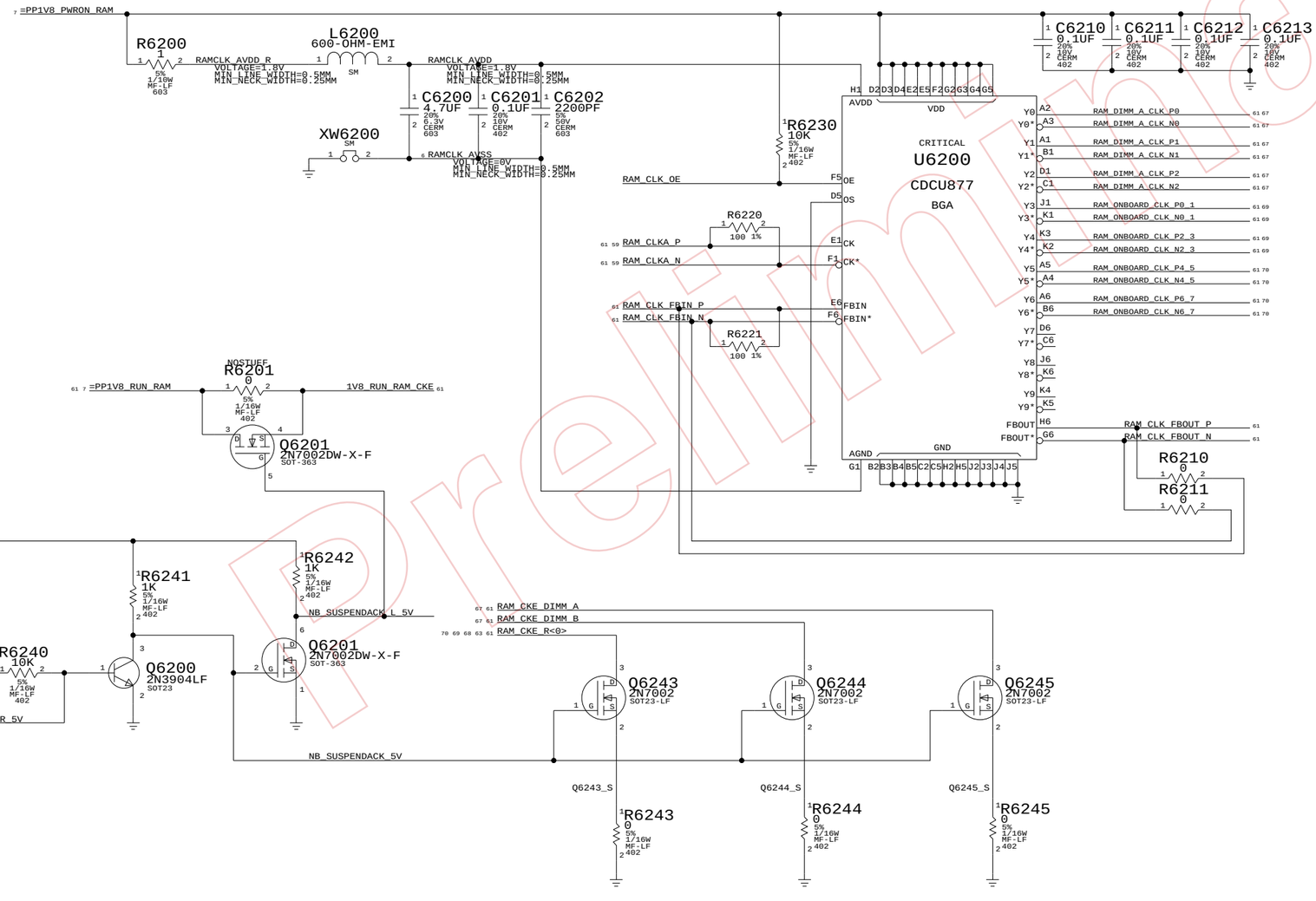
RAM_CAD SPACING IS 10MIL

Parallel Term

SYNC_MASTER=FINO-DS SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 61 OF 154	



Main Memory Clock Buffer

SYNC_MASTER=FINO-DS SYNC_DATE=06/20/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E

SCALE	SHT
NONE	62 OF 154

RAM_A_R<0>
ZTA0
ZTA0_R
ZTA0_RR
ZTA0_RL
ZTA0_L
ZTA0_LR
ZTA0_LL

RAM_A_R<1>
ZTA1
ZTA1_R
ZTA1_RR
ZTA1_RL
ZTA1_L
ZTA1_LR
ZTA1_LL

RAM_A_R<2>
ZTA2
ZTA2_R
ZTA2_RR
ZTA2_RL
ZTA2_L
ZTA2_LR
ZTA2_LL

RAM_A_R<3>
ZTA3
ZTA3_R
ZTA3_RR
ZTA3_RL
ZTA3_L
ZTA3_LR
ZTA3_LL

RAM_A_R<4>
ZTA4
ZTA4_R
ZTA4_RR
ZTA4_RL
ZTA4_L
ZTA4_LR
ZTA4_LL

RAM_A_R<5>
ZTA5
ZTA5_R
ZTA5_RR
ZTA5_RL
ZTA5_L
ZTA5_LR
ZTA5_LL

RAM_A_R<6>
ZTA6
ZTA6_R
ZTA6_RR
ZTA6_RL
ZTA6_L
ZTA6_LR
ZTA6_LL

RAM_A_R<7>
ZTA7
ZTA7_R
ZTA7_RR
ZTA7_RL
ZTA7_L
ZTA7_LR
ZTA7_LL

RAM_A_R<8>
ZTA8
ZTA8_R
ZTA8_RR
ZTA8_RL
ZTA8_L
ZTA8_LR
ZTA8_LL

RAM_A_R<9>
ZTA9
ZTA9_R
ZTA9_RR
ZTA9_RL
ZTA9_L
ZTA9_LR
ZTA9_LL

RAM_A_R<10>
ZTA10
ZTA10_R
ZTA10_RR
ZTA10_RL
ZTA10_L
ZTA10_LR
ZTA10_LL

RAM_A_R<11>
ZTA11
ZTA11_R
ZTA11_RR
ZTA11_RL
ZTA11_L
ZTA11_LR
ZTA11_LL

RAM_A_R<12>
ZTA12
ZTA12_R
ZTA12_RR
ZTA12_RL
ZTA12_L
ZTA12_LR
ZTA12_LL

RAM_A_R<13>
ZTA13
ZTA13_R
ZTA13_RR
ZTA13_RL
ZTA13_L
ZTA13_LR
ZTA13_LL

RAM_A_R<14>
ZTA14
ZTA14_R
ZTA14_RR
ZTA14_RL
ZTA14_L
ZTA14_LR
ZTA14_LL

RAM_A_R<15>
ZTA15
ZTA15_R
ZTA15_RR
ZTA15_RL
ZTA15_L
ZTA15_LR
ZTA15_LL

RAM_BA_R<0>
ZTBA0
ZTBA0_R
ZTBA0_RR
ZTBA0_RL
ZTBA0_L
ZTBA0_LR
ZTBA0_LL

RAM_BA_R<1>
ZTBA1
ZTBA1_R
ZTBA1_RR
ZTBA1_RL
ZTBA1_L
ZTBA1_LR
ZTBA1_LL

RAM_BA_R<2>
ZTBA2
ZTBA2_R
ZTBA2_RR
ZTBA2_RL
ZTBA2_L
ZTBA2_LR
ZTBA2_LL

RAM_RAS_L_R
ZTRAS
ZTRAS_R
ZTRAS_RR
ZTRAS_RL
ZTRAS_L
ZTRAS_LR
ZTRAS_LL

RAM_CAS_L_R
ZTCAS
ZTCAS_R
ZTCAS_RR
ZTCAS_RL
ZTCAS_L
ZTCAS_LR
ZTCAS_LL

RAM_WE_L_R
ZTWE
ZTWE_R
ZTWE_RR
ZTWE_RL
ZTWE_L
ZTWE_LR
ZTWE_LL

RAM_CS_L_R<0>
ZTCS
ZTCS_R
ZTCS_RR
ZTCS_RL
ZTCS_L
ZTCS_LR
ZTCS_LL

RAM_CKE_R<0>
ZTCKE
ZTCKE_R
ZTCKE_RR
ZTCKE_RL
ZTCKE_L
ZTCKE_LR
ZTCKE_LL

RAM_ODT_R<0>
ZTODT
ZTODT_R
ZTODT_RR
ZTODT_RL
ZTODT_L
ZTODT_LR
ZTODT_LL

MEMORY ADDR BRANCHING

SYNC_MASTER=FINO-DS SYNC_DATE=06/20/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

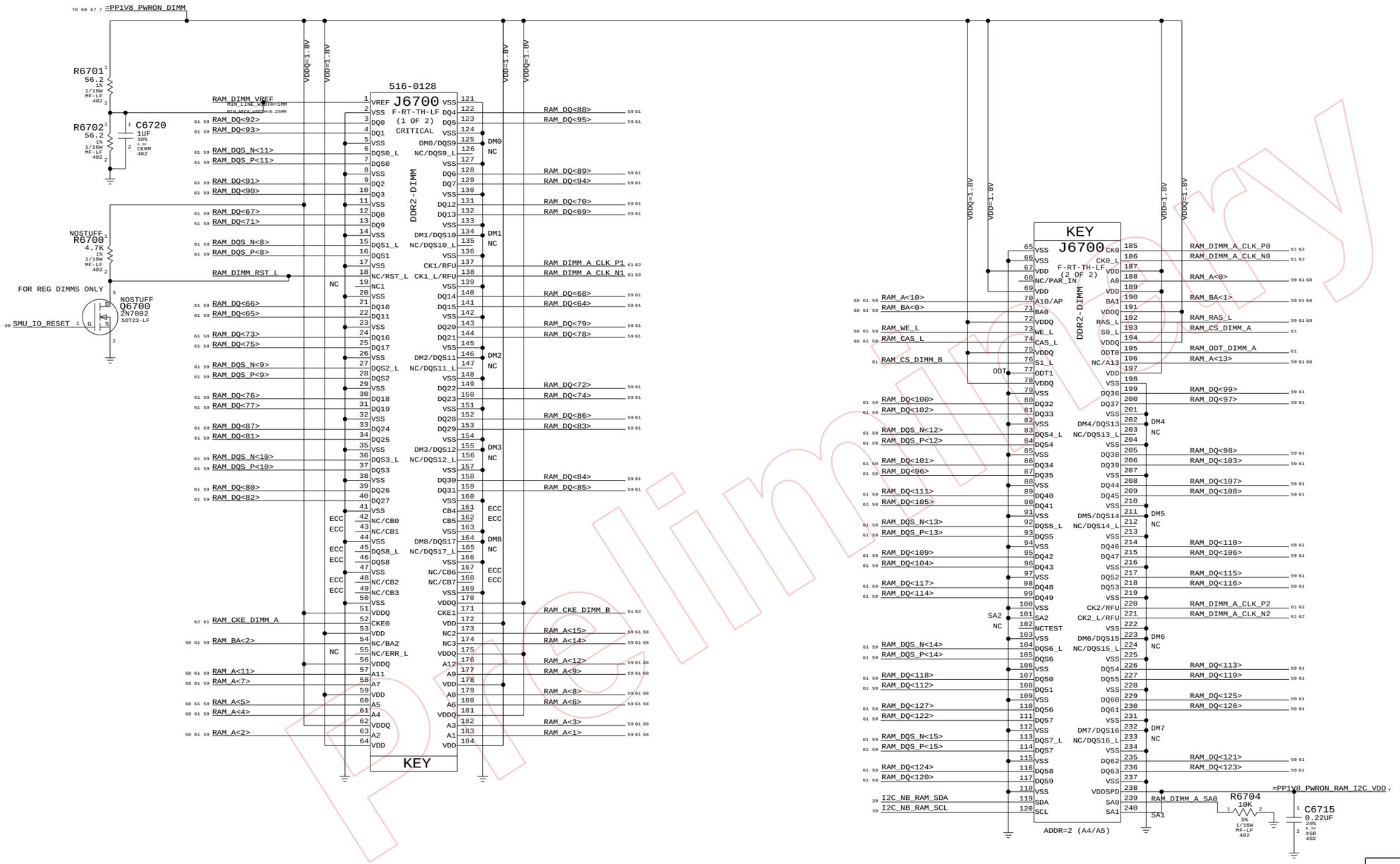
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

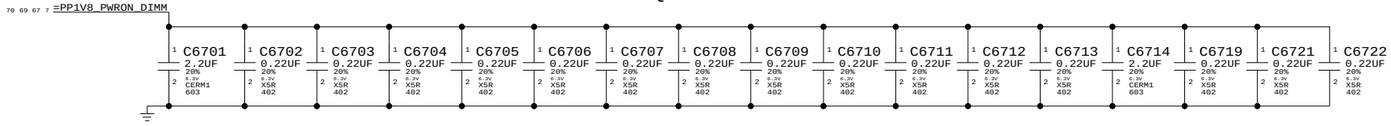
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 63 OF 154	



PLACE CAPS CLOSE TO VDD/VDDQ PINS OF DIMM SOCKET



Memory Dimm A

SYNC_MASTER=FINO-DS SYNC_DATE=06/20/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 67 OF 154	

ONBOARD MEMORY SHOULD FOLLOW SPEC FOR RAW CARD VERSION A

RAM_DQ<0>	22	4	5	RP6800	RAM_DQ_R<0>	61 69
RAM_DQ<1>	22	3	6	RP6800	RAM_DQ_R<1>	6 61 69
RAM_DQ<2>	22	1	8	RP6801	RAM_DQ_R<2>	6 61 69
RAM_DQ<3>	22	3	6	RP6801	RAM_DQ_R<3>	6 61 69
RAM_DQ<4>	22	4	5	RP6801	RAM_DQ_R<4>	61 69
RAM_DQ<5>	22	2	7	RP6800	RAM_DQ_R<5>	6 61 69
RAM_DQ<6>	22	2	7	RP6801	RAM_DQ_R<6>	6 61 69
RAM_DQ<7>	22	1	8	RP6800	RAM_DQ_R<7>	6 61 69
RAM_DQ<8>	22	3	6	RP6802	RAM_DQ_R<8>	6 61 69
RAM_DQ<9>	22	4	5	RP6803	RAM_DQ_R<9>	6 61 69
RAM_DQ<10>	22	1	8	RP6803	RAM_DQ_R<10>	61 69
RAM_DQ<11>	22	4	5	RP6802	RAM_DQ_R<11>	6 61 69
RAM_DQ<12>	22	3	6	RP6803	RAM_DQ_R<12>	6 61 69
RAM_DQ<13>	22	2	7	RP6802	RAM_DQ_R<13>	6 61 69
RAM_DQ<14>	22	2	7	RP6803	RAM_DQ_R<14>	6 61 69
RAM_DQ<15>	22	1	8	RP6802	RAM_DQ_R<15>	61 69
RAM_DQ<16>	22	3	6	RP6805	RAM_DQ_R<16>	6 61 69
RAM_DQ<17>	22	4	5	RP6805	RAM_DQ_R<17>	6 61 69
RAM_DQ<18>	22	1	8	RP6804	RAM_DQ_R<18>	61 69
RAM_DQ<19>	22	2	7	RP6805	RAM_DQ_R<19>	6 61 69
RAM_DQ<20>	22	2	7	RP6804	RAM_DQ_R<20>	6 61 69
RAM_DQ<21>	22	4	5	RP6804	RAM_DQ_R<21>	6 61 69
RAM_DQ<22>	22	3	6	RP6804	RAM_DQ_R<22>	6 61 69
RAM_DQ<23>	22	1	8	RP6805	RAM_DQ_R<23>	61 69
RAM_DQ<24>	22	4	5	RP6807	RAM_DQ_R<24>	6 61 69
RAM_DQ<25>	22	2	7	RP6806	RAM_DQ_R<25>	6 61 69
RAM_DQ<26>	22	4	5	RP6806	RAM_DQ_R<26>	61 69
RAM_DQ<27>	22	1	8	RP6807	RAM_DQ_R<27>	61 69
RAM_DQ<28>	22	3	6	RP6807	RAM_DQ_R<28>	6 61 69
RAM_DQ<29>	22	3	6	RP6806	RAM_DQ_R<29>	6 61 69
RAM_DQ<30>	22	2	7	RP6807	RAM_DQ_R<30>	6 61 69
RAM_DQ<31>	22	1	8	RP6806	RAM_DQ_R<31>	6 61 69
RAM_DQ<32>	22	4	5	RP6809	RAM_DQ_R<32>	6 61 70
RAM_DQ<33>	22	2	7	RP6808	RAM_DQ_R<33>	6 61 70
RAM_DQ<34>	22	3	6	RP6808	RAM_DQ_R<34>	6 61 70
RAM_DQ<35>	22	1	8	RP6809	RAM_DQ_R<35>	61 70
RAM_DQ<36>	22	2	7	RP6809	RAM_DQ_R<36>	6 61 70
RAM_DQ<37>	22	1	8	RP6808	RAM_DQ_R<37>	6 61 70
RAM_DQ<38>	22	3	6	RP6809	RAM_DQ_R<38>	6 61 70
RAM_DQ<39>	22	4	5	RP6808	RAM_DQ_R<39>	61 70
RAM_DQ<40>	22	4	5	RP6810	RAM_DQ_R<40>	6 61 70
RAM_DQ<41>	22	3	6	RP6811	RAM_DQ_R<41>	6 61 70
RAM_DQ<42>	22	1	8	RP6811	RAM_DQ_R<42>	61 70
RAM_DQ<43>	22	2	7	RP6810	RAM_DQ_R<43>	6 61 70
RAM_DQ<44>	22	4	5	RP6811	RAM_DQ_R<44>	6 61 70
RAM_DQ<45>	22	3	6	RP6810	RAM_DQ_R<45>	6 61 70
RAM_DQ<46>	22	2	7	RP6811	RAM_DQ_R<46>	6 61 70
RAM_DQ<47>	22	1	8	RP6810	RAM_DQ_R<47>	61 70
RAM_DQ<48>	22	3	6	RP6812	RAM_DQ_R<48>	6 61 70
RAM_DQ<49>	22	4	5	RP6812	RAM_DQ_R<49>	6 61 70
RAM_DQ<50>	22	2	7	RP6813	RAM_DQ_R<50>	6 61 70
RAM_DQ<51>	22	1	8	RP6813	RAM_DQ_R<51>	61 70
RAM_DQ<52>	22	3	6	RP6813	RAM_DQ_R<52>	6 61 70
RAM_DQ<53>	22	4	5	RP6813	RAM_DQ_R<53>	6 61 70
RAM_DQ<54>	22	2	7	RP6812	RAM_DQ_R<54>	6 61 70
RAM_DQ<55>	22	1	8	RP6812	RAM_DQ_R<55>	61 70
RAM_DQ<56>	22	3	6	RP6814	RAM_DQ_R<56>	6 61 70
RAM_DQ<57>	22	4	5	RP6815	RAM_DQ_R<57>	6 61 70
RAM_DQ<58>	22	2	7	RP6815	RAM_DQ_R<58>	6 61 70
RAM_DQ<59>	22	3	6	RP6815	RAM_DQ_R<59>	6 61 70
RAM_DQ<60>	22	2	7	RP6814	RAM_DQ_R<60>	6 61 70
RAM_DQ<61>	22	1	8	RP6814	RAM_DQ_R<61>	61 70
RAM_DQ<62>	22	1	8	RP6815	RAM_DQ_R<62>	61 70
RAM_DQ<63>	22	4	5	RP6814	RAM_DQ_R<63>	6 61 70

RAM_DQS_P<0>	22	1	2	R6800	RAM_DQS_P_R<0>	61 69
RAM_DQS_N<0>	22	1	2	R6810	RAM_DQS_N_R<0>	61 69
RAM_DQS_P<1>	22	1	2	R6801	RAM_DQS_P_R<1>	61 69
RAM_DQS_N<1>	22	1	2	R6811	RAM_DQS_N_R<1>	61 69
RAM_DQS_P<2>	22	1	2	R6802	RAM_DQS_P_R<2>	61 69
RAM_DQS_N<2>	22	1	2	R6812	RAM_DQS_N_R<2>	61 69
RAM_DQS_P<3>	22	1	2	R6803	RAM_DQS_P_R<3>	61 69
RAM_DQS_N<3>	22	1	2	R6813	RAM_DQS_N_R<3>	61 69
RAM_DQS_P<4>	22	1	2	R6804	RAM_DQS_P_R<4>	61 70
RAM_DQS_N<4>	22	1	2	R6814	RAM_DQS_N_R<4>	61 70
RAM_DQS_P<5>	22	1	2	R6805	RAM_DQS_P_R<5>	61 70
RAM_DQS_N<5>	22	1	2	R6815	RAM_DQS_N_R<5>	61 70
RAM_DQS_P<6>	22	1	2	R6806	RAM_DQS_P_R<6>	61 70
RAM_DQS_N<6>	22	1	2	R6816	RAM_DQS_N_R<6>	61 70
RAM_DQS_P<7>	22	1	2	R6807	RAM_DQS_P_R<7>	61 70
RAM_DQS_N<7>	22	1	2	R6817	RAM_DQS_N_R<7>	61 70

RAM_A<0>	5.1	1	8	RP6824	RAM_A_R<0>	1	ZT6800
RAM_A<1>	5.1	1	8	RP6823	RAM_A_R<1>	1	ZT6801
RAM_A<2>	5.1	2	7	RP6823	RAM_A_R<2>	1	ZT6802
RAM_A<3>	5.1	4	5	RP6822	RAM_A_R<3>	1	ZT6803
RAM_A<4>	5.1	3	6	RP6822	RAM_A_R<4>	1	ZT6804
RAM_A<5>	5.1	2	7	RP6822	RAM_A_R<5>	1	ZT6805
RAM_A<6>	5.1	1	8	RP6822	RAM_A_R<6>	1	ZT6806
RAM_A<7>	5.1	3	6	RP6821	RAM_A_R<7>	1	ZT6807
RAM_A<8>	5.1	4	5	RP6821	RAM_A_R<8>	1	ZT6808
RAM_A<9>	5.1	1	8	RP6821	RAM_A_R<9>	1	ZT6809
RAM_A<10>	5.1	3	6	RP6824	RAM_A_R<10>	1	ZT6810
RAM_A<11>	5.1	2	7	RP6821	RAM_A_R<11>	1	ZT6811
RAM_A<12>	5.1	4	5	RP6820	RAM_A_R<12>	1	ZT6812
RAM_A<13>	5.1	4	5	RP6825	RAM_A_R<13>	1	ZT6813
RAM_A<14>	5.1	2	7	RP6820	RAM_A_R<14>	1	ZT6814
RAM_A<15>	5.1	1	8	RP6820	RAM_A_R<15>	1	ZT6815

VIAS FOR ECC STUB

RAM_BA<0>	5.1	4	5	RP6824	RAM_BA_R<0>	1	ZT6820
RAM_BA<1>	5.1	2	7	RP6824	RAM_BA_R<1>		ZT6821
RAM_BA<2>	5.1	3	6	RP6820	RAM_BA_R<2>	1	ZT6822
RAM_RAS_L	5.1	1	8	RP6825	RAM_RAS_L_R	1	ZT6825
RAM_CAS_L	5.1	3	6	RP6825	RAM_CAS_L_R	1	ZT6826
RAM_WE_L	5.1	2	7	RP6825	RAM_WE_L_R	1	ZT6827

VIAS FOR ECC STUB

PLACE NEAR KODIAK PRIOR TO BRANCH

PLACE AT END POINT TO SIMULATE ECC

C6870	24PF	5% 50V C0G 402	RAM_CS_L_R<0>
C6871	2PF	+/-0.25PF 50V C0G 402-1	
C6880	24PF	5% 50V C0G 402	RAM_CKE_R<0>
C6881	2PF	+/-0.25PF 50V C0G 402-1	
C6890	24PF	5% 50V C0G 402	RAM_ODT_R<0>
C6891	2PF	+/-0.25PF 50V C0G 402-1	

MLB Mem Series Term

SYNC_MASTER=FINO-DS SYNC_DATE=06/20/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

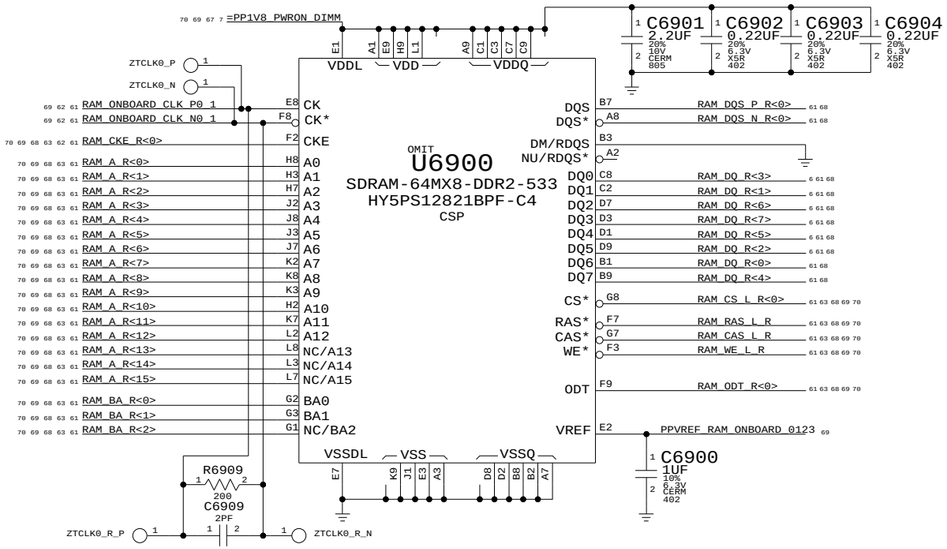
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

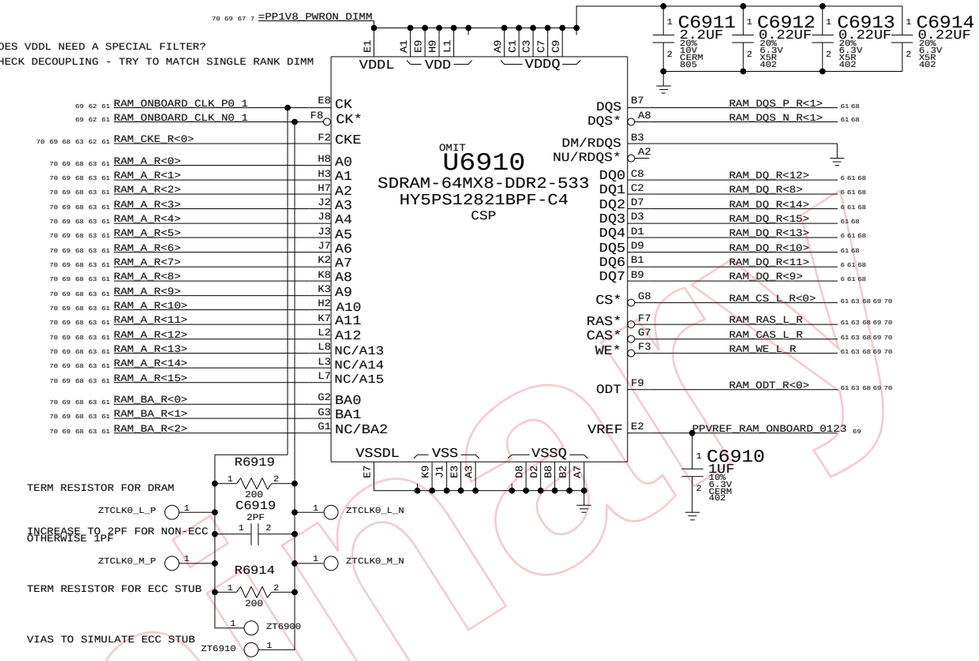
II NOT TO REPRODUCE OR COPY IT

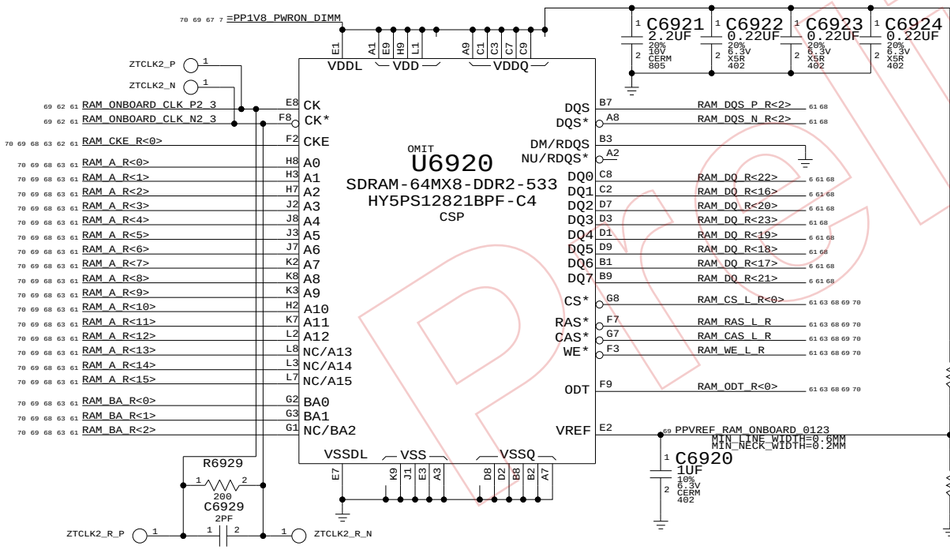
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

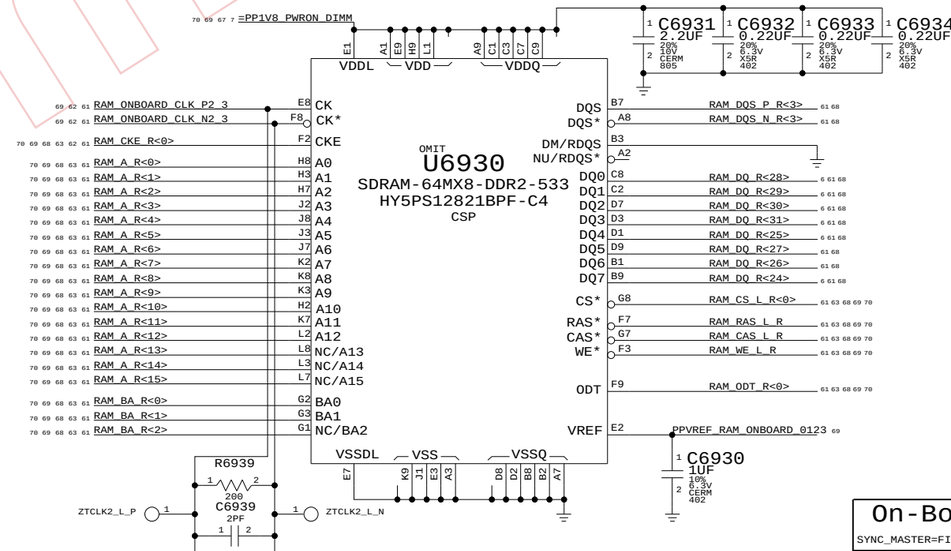
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 68 OF 154	









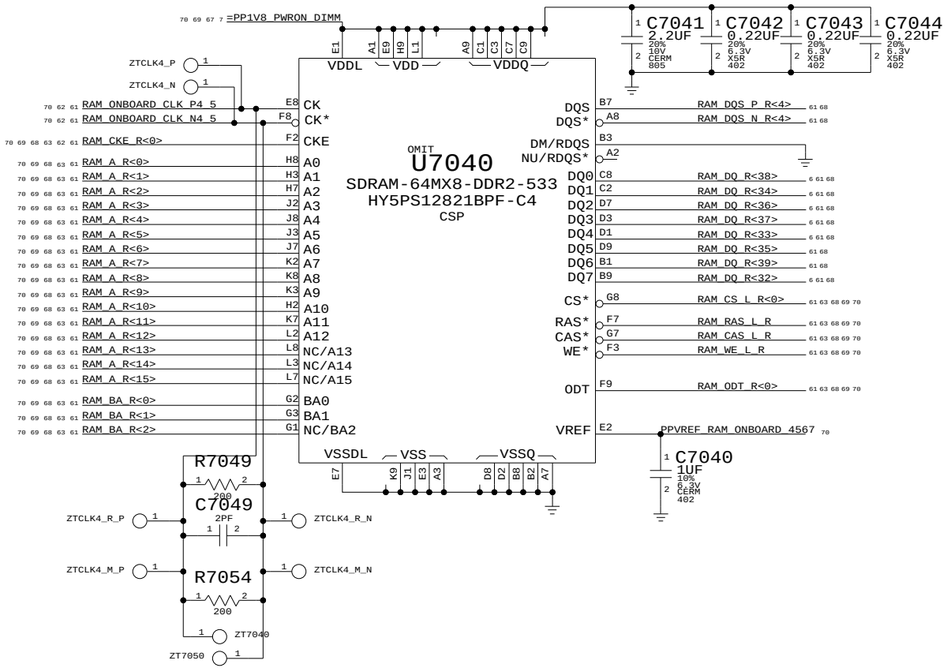
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333T0032	4	IC,SDRAM,DDR2,512MBIT,X8	U6900,U6910,U6920,U6930	CRITICAL	
333T0032	4	IC,SDRAM,DDR2,512MBIT,X8	U7040,U7050,U7060,U7070	CRITICAL	

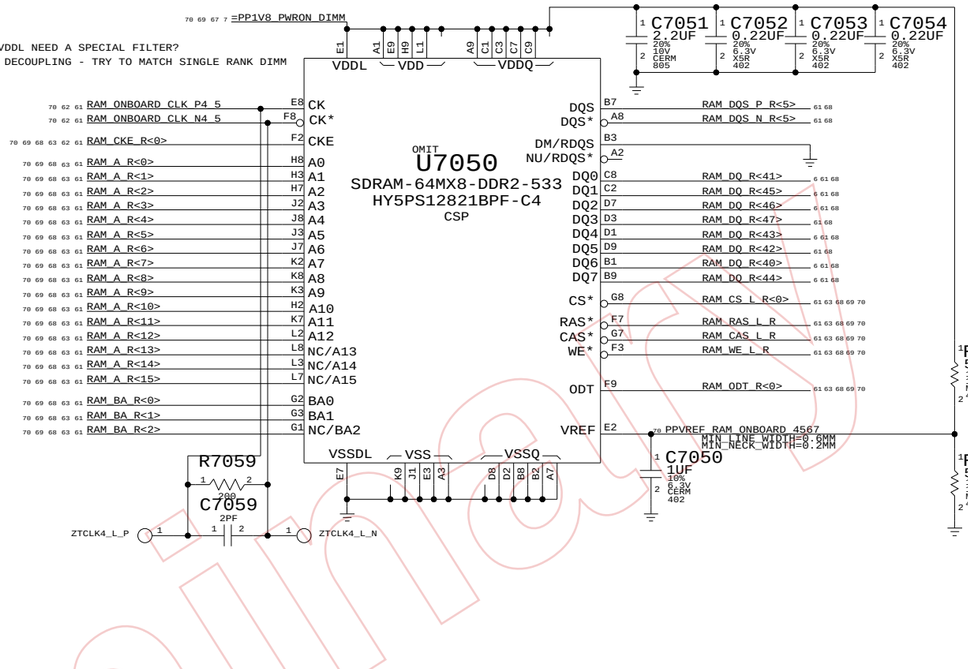
On-Board DDR SDRAM

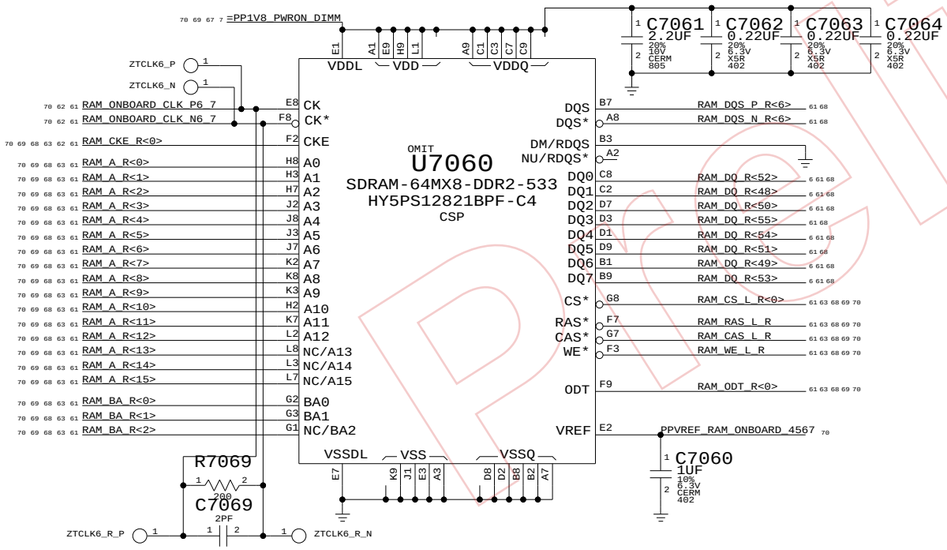
SYNC_MASTER=FINO-DS SYNC_DATE=06/20/2005

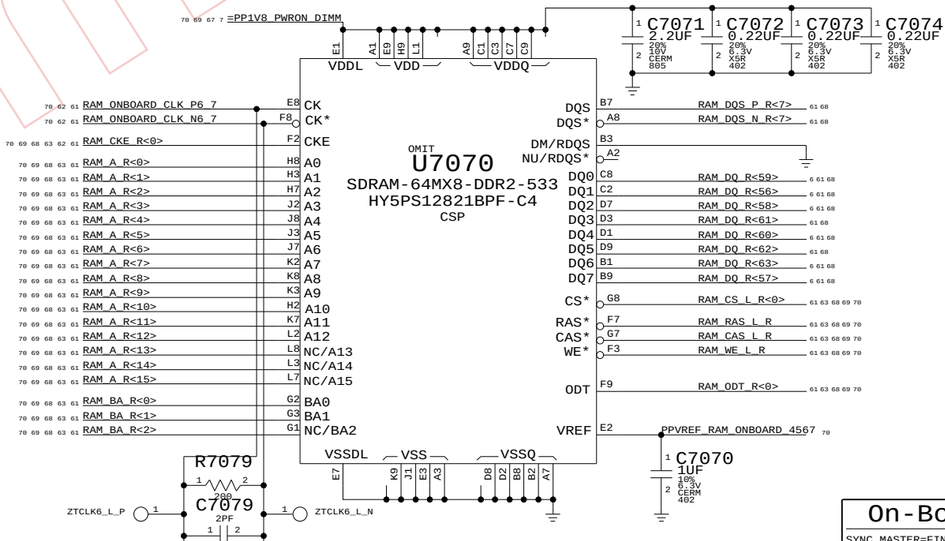
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 69 OF 154	









On-Board DDR SDRAM

SYNC_MASTER=FINO-DS SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE	SHT	OF
NONE	70	154

KODIAK AVDD FILTERING
(LOCATE CLOSE TO POWER AND GROUND PINS)

82 7 =PP2V5_PWRON_NB_PCIE
L8200 0.22UH 0805-1
C8200 0.01UF 10% 16V CERM 402
C8201 10UF 10% 6.3V X5R 805
C8202 1UF 10% 6.3V CERM 402
PWR_PCIE_A_AVDD_2 82 97
97 82 6 KOD_G10_GND (THIS PAGE)

82 7 =PP2V5_PWRON_NB_PCIE
L8201 0.22UH 0805-1
C8203 0.01UF 10% 16V CERM 402
C8204 10UF 10% 6.3V X5R 805
C8205 1UF 10% 6.3V CERM 402
PWR_PCIE_A_AVDD_1 82 97
97 82 6 KOD_K07_GND (THIS PAGE)

82 7 =PP2V5_PWRON_NB_PCIE
L8202 0.22UH 0805-1
C8206 0.01UF 10% 16V CERM 402
C8207 10UF 10% 6.3V X5R 805
C8208 1UF 10% 6.3V CERM 402
PWR_PCIE_A_AVDD_0 82 97
97 82 6 KOD_H05_GND (THIS PAGE)

97 82 PWR_PCIE_A_AVDD_2
97 82 PWR_PCIE_A_AVDD_1
97 82 PWR_PCIE_A_AVDD_0

97 PWR_PCIE_A_AVDD_A
97 PWR_PCIE_A_AVDD_B
97 PWR_PCIE_A_AVDD_C

97 PWR_PCIE_A_AVDD
L8203 0.22UH 0805-1
=PP2V5_PWRON_NB_PCIE 7 82
C8222 1UF 10% 6.3V CERM 402
C8225 1UF 10% 6.3V CERM 402
C8223 10UF 10% 6.3V X5R 805
C8224 0.01UF 10% 16V CERM 402
KOD_L13_GND 6 82 97 (THIS PAGE)
KOD_J13_GND 6 82 97 (THIS PAGE)

L8205 0.22UH 0805-1
=PP2V5_PWRON_NB_PCIE 7 82
C8228 1UF 10% 6.3V CERM 402
C8229 10UF 10% 6.3V X5R 805
C8230 0.01UF 10% 16V CERM 402
KOD_H08_GND 6 82 97 (THIS PAGE)

J06 PCIE_AVDD_0 (1.65V-2.75V) SERDES
J07 PCIE_AVDD_1 (1.65V-2.75V) SERDES
H11 PCIE_AVDD_2 (1.65V-2.75V) SERDES
J12 PCIE_REFCLK_AVDDA (1.65V-2.75V) PLL
K13 PCIE_REFCLK_AVDDB (1.65V-2.75V) PLL
J09 PCIE_REFCLK_AVDD2 (1.65V-2.75V) PLL

U1900
KODIAK-ASIC-040812
PCI-E X16 INTERFACE
BGA
(5 OF 10)
SEE_TABLE

(1.6V-1.2V)
A04 PCIE_VDD
A08 PCIE_VDD
A12 PCIE_VDD
B06 PCIE_VDD
B10 PCIE_VDD
C03 PCIE_VDD
D01 PCIE_VDD
D04 PCIE_VDD
D08 PCIE_VDD
D12 PCIE_VDD
E06 PCIE_VDD
E10 PCIE_VDD
E14 PCIE_VDD
82 7 =PPVCORE_PWRON_NB_PCIE

(1.6V-1.2V)
F02 PCIE_VDD
F05 PCIE_VDD
G08 PCIE_VDD
G12 PCIE_VDD
H01 PCIE_VDD
H04 PCIE_VDD
H07 PCIE_VDD
H10 PCIE_VDD
H14 PCIE_VDD
K12 PCIE_VDD
L11 PCIE_VDD
L14 PCIE_VDD
M12 PCIE_VDD
=PPVCORE_PWRON_NB_PCIE 7 82

KODIAK PCI-E 100MHZ REFCLK
PP8201 P4MM
PP8200 P4MM
97 9 CLK_KOD_100M_PF<0>
97 9 CLK_KOD_100M_NF<0>
J11 PCIE_REFCLK_P
J10 PCIE_REFCLK_N (100MHZ)

97 26 CLK_KOD_100M_P<0>
R8202 20.5 1% 1/10W MF-LF 402 NOSTUFF
97 9 100M_P<0>
C8245 0.01UF 10% 16V CERM 402
C8244 0.01UF 10% 16V CERM 402
100M_G
R8203 29.4 1% 1/10W MF-LF 402
R8204 29.4 1% 1/10W MF-LF 402
C8246 0.01UF 10% 16V CERM 402
97 26 CLK_KOD_100M_N<0>
R8205 20.5 1% 1/10W MF-LF 402
97 9 100M_N<0>

KODIAK PCIE REFCLK TERMINATION
(LOCATE CLOSE TO INPUT PINS)

97 84 9 PCIE_SLOTA_TO_NB_N<0> G05 PCIE_HSIN0
97 84 9 PCIE_SLOTA_TO_NB_P<0> G04 PCIE_HSIP0
97 84 9 PCIE_SLOTA_TO_NB_N<1> G01 PCIE_HSIN1
97 84 9 PCIE_SLOTA_TO_NB_P<1> G02 PCIE_HSIP1
97 84 9 PCIE_SLOTA_TO_NB_N<2> C04 PCIE_HSIN2
97 84 9 PCIE_SLOTA_TO_NB_P<2> C05 PCIE_HSIP2
97 84 9 PCIE_SLOTA_TO_NB_N<3> C07 PCIE_HSIN3
97 84 9 PCIE_SLOTA_TO_NB_P<3> C06 PCIE_HSIP3
97 84 9 PCIE_SLOTA_TO_NB_N<4> E01 PCIE_HSIN4
97 84 9 PCIE_SLOTA_TO_NB_P<4> E02 PCIE_HSIP4
97 84 9 PCIE_SLOTA_TO_NB_N<5> J05 PCIE_HSIN5
97 84 9 PCIE_SLOTA_TO_NB_P<5> J04 PCIE_HSIP5
97 84 9 PCIE_SLOTA_TO_NB_N<6> H06 PCIE_HSIN6
97 84 9 PCIE_SLOTA_TO_NB_P<6> G06 PCIE_HSIP6
97 84 9 PCIE_SLOTA_TO_NB_N<7> E05 PCIE_HSIN7
97 84 9 PCIE_SLOTA_TO_NB_P<7> D05 PCIE_HSIP7
97 84 9 PCIE_SLOTA_TO_NB_N<8> D11 PCIE_HSIN8
97 84 9 PCIE_SLOTA_TO_NB_P<8> E11 PCIE_HSIP8
97 84 9 PCIE_SLOTA_TO_NB_N<9> F12 PCIE_HSIN9
97 84 9 PCIE_SLOTA_TO_NB_P<9> F13 PCIE_HSIP9
97 84 9 PCIE_SLOTA_TO_NB_N<10> H09 PCIE_HSIN10
97 84 9 PCIE_SLOTA_TO_NB_P<10> G09 PCIE_HSIP10
97 84 9 PCIE_SLOTA_TO_NB_N<11> F09 PCIE_HSIN11
97 84 9 PCIE_SLOTA_TO_NB_P<11> F08 PCIE_HSIP11
97 84 9 PCIE_SLOTA_TO_NB_N<12> G13 PCIE_HSIN12
97 84 9 PCIE_SLOTA_TO_NB_P<12> H13 PCIE_HSIP12
97 84 9 PCIE_SLOTA_TO_NB_N<13> C13 PCIE_HSIN13
97 84 9 PCIE_SLOTA_TO_NB_P<13> C12 PCIE_HSIP13
97 84 9 PCIE_SLOTA_TO_NB_N<14> D07 PCIE_HSIN14
97 84 9 PCIE_SLOTA_TO_NB_P<14> E07 PCIE_HSIP14
97 84 9 PCIE_SLOTA_TO_NB_N<15> G07 PCIE_HSIN15
97 84 9 PCIE_SLOTA_TO_NB_P<15> F07 PCIE_HSIP15

82 7 =PP2V5_PWRON_NB_PCIE
R8200 8.2K 5% 1/10W MF-LF 402
84 6 PCIE_SLOTA_PRSNT_L
AJ02 PCIE_PRESENTN

PCIE_VCAL_RES0 F14 PCIE_VCAL_RES0
PCIE_VCAL_RES1 J14 PCIE_VCAL_RES1
R8201 200 1% 1/10W MF-LF 402

A06 PCIE_GND
A10 PCIE_GND
B02 PCIE_GND
B04 PCIE_GND
B08 PCIE_GND
B12 PCIE_GND
D02 PCIE_GND
D06 PCIE_GND
D10 PCIE_GND
D14 PCIE_GND
E08 PCIE_GND
E12 PCIE_GND
F01 PCIE_GND
F04 PCIE_GND
F06 PCIE_GND
G14 PCIE_GND
H02 PCIE_GND
H12 PCIE_GND
K10 PCIE_GND
K14 PCIE_GND
L12 PCIE_GND
M11 PCIE_GND
M13 PCIE_GND

(DNU)
PCIE_AVREG_2 G11 NC_A_AVREG_2 6
PCIE_AVREG_1 J08 NC_A_AVREG_1 6
PCIE_AVREG_0 E04 NC_A_AVREG_0 6

KODIAK PCI-E AC COUPLERS
(LOCATE NEAR SOURCE PINS)

PCIE_HSON0	D03	97 9 PCIE_NB_TO_SLOTA_NF<0>	0.1UF	C8247	PCIE_NB_TO_SLOTA_N<0> 9 84 97
PCIE_HSOP0	E03	97 9 PCIE_NB_TO_SLOTA_PF<0>	0.1UF	C8248	PCIE_NB_TO_SLOTA_P<0> 9 84 97
PCIE_HSON1	J01	97 9 PCIE_NB_TO_SLOTA_NF<1>	0.1UF	C8249	PCIE_NB_TO_SLOTA_N<1> 9 84 97
PCIE_HSOP1	J02	97 9 PCIE_NB_TO_SLOTA_PF<1>	0.1UF	C8250	PCIE_NB_TO_SLOTA_P<1> 9 84 97
PCIE_HSON2	C01	97 9 PCIE_NB_TO_SLOTA_NF<2>	0.1UF	C8251	PCIE_NB_TO_SLOTA_N<2> 9 84 97
PCIE_HSOP2	C02	97 9 PCIE_NB_TO_SLOTA_PF<2>	0.1UF	C8252	PCIE_NB_TO_SLOTA_P<2> 9 84 97
PCIE_HSON3	A07	97 9 PCIE_NB_TO_SLOTA_NF<3>	0.1UF	C8253	PCIE_NB_TO_SLOTA_N<3> 9 84 97
PCIE_HSOP3	B07	97 9 PCIE_NB_TO_SLOTA_PF<3>	0.1UF	C8254	PCIE_NB_TO_SLOTA_P<3> 9 84 97
PCIE_HSON4	F03	97 9 PCIE_NB_TO_SLOTA_NF<4>	0.1UF	C8255	PCIE_NB_TO_SLOTA_N<4> 9 84 97
PCIE_HSOP4	G03	97 9 PCIE_NB_TO_SLOTA_PF<4>	0.1UF	C8256	PCIE_NB_TO_SLOTA_P<4> 9 84 97
PCIE_HSON5	H03	97 9 PCIE_NB_TO_SLOTA_NF<5>	0.1UF	C8257	PCIE_NB_TO_SLOTA_N<5> 9 84 97
PCIE_HSOP5	J03	97 9 PCIE_NB_TO_SLOTA_PF<5>	0.1UF	C8258	PCIE_NB_TO_SLOTA_P<5> 9 84 97
PCIE_HSON6	A03	97 9 PCIE_NB_TO_SLOTA_NF<6>	0.1UF	C8259	PCIE_NB_TO_SLOTA_N<6> 9 84 97
PCIE_HSOP6	B03	97 9 PCIE_NB_TO_SLOTA_PF<6>	0.1UF	C8260	PCIE_NB_TO_SLOTA_P<6> 9 84 97
PCIE_HSON7	A05	97 9 PCIE_NB_TO_SLOTA_NF<7>	0.1UF	C8261	PCIE_NB_TO_SLOTA_N<7> 9 84 97
PCIE_HSOP7	B05	97 9 PCIE_NB_TO_SLOTA_PF<7>	0.1UF	C8262	PCIE_NB_TO_SLOTA_P<7> 9 84 97
PCIE_HSON8	C11	97 9 PCIE_NB_TO_SLOTA_NF<8>	0.1UF	C8263	PCIE_NB_TO_SLOTA_N<8> 9 84 97
PCIE_HSOP8	C10	97 9 PCIE_NB_TO_SLOTA_PF<8>	0.1UF	C8264	PCIE_NB_TO_SLOTA_P<8> 9 84 97
PCIE_HSON9	B11	97 9 PCIE_NB_TO_SLOTA_NF<9>	0.1UF	C8265	PCIE_NB_TO_SLOTA_N<9> 9 84 97
PCIE_HSOP9	A11	97 9 PCIE_NB_TO_SLOTA_PF<9>	0.1UF	C8266	PCIE_NB_TO_SLOTA_P<9> 9 84 97
PCIE_HSON10	F11	97 9 PCIE_NB_TO_SLOTA_NF<10>	0.1UF	C8267	PCIE_NB_TO_SLOTA_N<10> 9 84 97
PCIE_HSOP10	F10	97 9 PCIE_NB_TO_SLOTA_PF<10>	0.1UF	C8268	PCIE_NB_TO_SLOTA_P<10> 9 84 97
PCIE_HSON11	B09	97 9 PCIE_NB_TO_SLOTA_NF<11>	0.1UF	C8269	PCIE_NB_TO_SLOTA_N<11> 9 84 97
PCIE_HSOP11	A09	97 9 PCIE_NB_TO_SLOTA_PF<11>	0.1UF	C8270	PCIE_NB_TO_SLOTA_P<11> 9 84 97
PCIE_HSON12	D13	97 9 PCIE_NB_TO_SLOTA_NF<12>	0.1UF	C8271	PCIE_NB_TO_SLOTA_N<12> 9 84 97
PCIE_HSOP12	E13	97 9 PCIE_NB_TO_SLOTA_PF<12>	0.1UF	C8272	PCIE_NB_TO_SLOTA_P<12> 9 84 97
PCIE_HSON13	B13	97 9 PCIE_NB_TO_SLOTA_NF<13>	0.1UF	C8273	PCIE_NB_TO_SLOTA_N<13> 9 84 97
PCIE_HSOP13	A13	97 9 PCIE_NB_TO_SLOTA_PF<13>	0.1UF	C8274	PCIE_NB_TO_SLOTA_P<13> 9 84 97
PCIE_HSON14	D09	97 9 PCIE_NB_TO_SLOTA_NF<14>	0.1UF	C8275	PCIE_NB_TO_SLOTA_N<14> 9 84 97
PCIE_HSOP14	E09	97 9 PCIE_NB_TO_SLOTA_PF<14>	0.1UF	C8276	PCIE_NB_TO_SLOTA_P<14> 9 84 97
PCIE_HSON15	C08	97 9 PCIE_NB_TO_SLOTA_NF<15>	0.1UF	C8277	PCIE_NB_TO_SLOTA_N<15> 9 84 97
PCIE_HSOP15	C09	97 9 PCIE_NB_TO_SLOTA_PF<15>	0.1UF	C8278	PCIE_NB_TO_SLOTA_P<15> 9 84 97

KODIAK PCI-E DECOUPLING
(LOCATE CLOSE TO POWER AND GROUND PINS)

=PPVCORE_PWRON_NB_PCIE 7 82
C8209 1UF 10% 6.3V CERM 402
C8210 1UF 10% 6.3V CERM 402
C8211 1UF 10% 6.3V CERM 402
C8212 1UF 10% 6.3V CERM 402
C8213 1UF 10% 6.3V CERM 402
C8214 1UF 10% 6.3V CERM 402
C8215 1UF 10% 6.3V CERM 402
C8216 1UF 10% 6.3V CERM 402
C8217 1UF 10% 6.3V CERM 402
C8218 1UF 10% 6.3V CERM 402
C8219 1UF 10% 6.3V CERM 402
C8220 1UF 10% 6.3V CERM 402
C8221 1UF 10% 6.3V CERM 402

=PPVCORE_PWRON_NB_PCIE 7 82
C8231 1UF 10% 6.3V CERM 402
C8232 1UF 10% 6.3V CERM 402
C8233 1UF 10% 6.3V CERM 402
C8234 1UF 10% 6.3V CERM 402
C8235 1UF 10% 6.3V CERM 402
C8236 1UF 10% 6.3V CERM 402
C8241 1UF 10% 6.3V CERM 402
C8242 1UF 10% 6.3V CERM 402
C8243 1UF 10% 6.3V CERM 402
C8237 1UF 10% 6.3V CERM 402
C8238 1UF 10% 6.3V CERM 402
C8239 1UF 10% 6.3V CERM 402
C8240 1UF 10% 6.3V CERM 402

KODIAK PCI-E DECOUPLING
(LOCATE CLOSE TO POWER AND GROUND PINS)

AVDD_0_GND H05 AVDD_1_GND K07 AVDD_2_GND G10
97 82 6 KOD_H05_GND
97 82 6 KOD_K07_GND
97 82 6 KOD_G10_GND
(THIS PAGE, X3)
XW8200 SM
XW8201 SM
XW8202 SM

REFCLK_AGNDA J13 REFCLK_AGNDB L13 REFCLK_AGND2 H08
KOD_H08_GND 6 82 97
KOD_L13_GND 6 82 97
KOD_J13_GND 6 82 97
(THIS PAGE, X3)
XW8203 SM
XW8204 SM
XW8205 SM

KODIAK PCI-E X16

SYNC_MASTER=Q63 SYNC_DATE=08/01/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE	SHT	OF
NONE	82	154

DRAWING

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
338S0239	1	IC,RV370 XT, GRAPHICS CTLR	U8400	RV370XT	CRITICAL
338S0265	1	IC,RV380 XT A23, GRAPHICS CTLR	U8400	RV380XT	CRITICAL

REMOVED COMPLIANCE TEST POINTS
FINO WILL PLACE COUPLING CAPACITORS ON RECEIVING SIDE
(THIS IS ALLOWED FOR CHIP TO CHIP PCIE)
CAP PAD CAN BE USED FOR COMPLIANCE TEST

GROUND VIAS FOR LAYER TRANSITIONS

ZH8400 HOLE-VIA
ZH8401 HOLE-VIA
ZH8402 HOLE-VIA
ZH8403 HOLE-VIA
ZH8404 HOLE-VIA
ZH8405 HOLE-VIA
ZH8406 HOLE-VIA
ZH8407 HOLE-VIA
ZH8408 HOLE-VIA
ZH8409 HOLE-VIA
ZH8410 HOLE-VIA
ZH8411 HOLE-VIA
ZH8412 HOLE-VIA
ZH8413 HOLE-VIA
ZH8414 HOLE-VIA
ZH8415 HOLE-VIA
ZH8416 HOLE-VIA
ZH8417 HOLE-VIA
ZH8418 HOLE-VIA
ZH8419 HOLE-VIA

=PP1V2_GPU_PCIE → L8460 FERR-220-OHM (0805) → PP1V2_GPU_PCIE_VDDR (VOLTAGE=1.2V, MIN_LINE_WIDTH=0.5MM, MIN_NECK_WIDTH=0.25MM)
THIS IS ALIASED TO PPVCORE_GPU ON PAGE 7
L8461 FERR-220-OHM (0805)

C8460 1UF 10% 6.3V CERM 402
C8461 1UF 10% 6.3V CERM 402
C8462 1UF 10% 6.3V CERM 402
C8463 0.1UF 20% 10V CERM 402
C8464 0.1UF 20% 10V CERM 402
C8465 0.1UF 20% 10V CERM 402
C8466 0.1UF 20% 10V CERM 402

PP1V2_GPU_PCIE_PVDD
SYS_POWERUP_L SHOULD CONTROL THE FET ON PP1V2_RUN
C8450 1UF 10% 6.3V CERM 402
C8451 1UF 10% 6.3V CERM 402
C8452 0.1UF 20% 10V CERM 402
C8453 0.1UF 20% 10V CERM 402
C8454 0.1UF 20% 10V CERM 402
C8455 0.1UF 20% 10V CERM 402

=PP1V8_GPU → L8440 FERR-220-OHM (0805) → PP1V8_GPU_PCIE_PVDD (VOLTAGE=1.8V, MIN_LINE_WIDTH=0.5MM, MIN_NECK_WIDTH=0.25MM)
C8440 1UF 10% 6.3V CERM 402
C8441 1UF 10% 6.3V CERM 402
C8442 0.1UF 20% 10V CERM 402
C8443 0.1UF 20% 10V CERM 402
C8444 0.1UF 20% 10V CERM 402
C8445 0.1UF 20% 10V CERM 402

PLACE R8470 CLOSE TO U9670
=GPU_RESET_L → U9670 74LC125 TSSOP → ATI_RESET_L
R8469 8.2K 5% 1/16W MF-LF 402
R8470 33 5% 1/10W MF-LF 402

PP1V2_GPU_PCIE_PVDD
R8471 301 1% 1/16W MF-LF 402
R8472 21 1% 1/16W MF-LF 402
R8473 21 1% 1/16W MF-LF 402
R8474 60.4 1% 1/16W MF-LF 402
R8475 21 1% 1/16W MF-LF 402
R8476 60.4 1% 1/16W MF-LF 402
R8477 21 1% 1/16W MF-LF 402
R8478 301 1% 1/16W MF-LF 402
CKA_P<0> CKA_N<0>
C8472 5PF +/-0.25PF 50V CERM 402
C8473 5PF +/-0.25PF 50V CERM 402
CLK_PCIE_SLOTA_P<0>
CLK_PCIE_SLOTA_N<0>
PP1V2_GPU_PCIE_PVDD

PCI-E SLOTA 100MHZ
REFCLK TERMINATION
(LOCATE CLOSE TO GPU)

U8400 RV370XT BGA (1 OF 5) OMIT PCI-E

CLK_PCIE_SLOTA_PF<0>	AF27	PCIE_REFCLKP
CLK_PCIE_SLOTA_NF<0>	AE27	PCIE_REFCLKN
PCIE_NB_TO_SLOTA_P<0>	AH30	PCIE_RX0P
PCIE_NB_TO_SLOTA_N<0>	AG30	PCIE_RX0N
PCIE_NB_TO_SLOTA_P<1>	AG29	PCIE_RX1P
PCIE_NB_TO_SLOTA_N<1>	AF29	PCIE_RX1N
PCIE_NB_TO_SLOTA_P<2>	AE29	PCIE_RX2P
PCIE_NB_TO_SLOTA_N<2>	AE30	PCIE_RX2N
PCIE_NB_TO_SLOTA_P<3>	AD30	PCIE_RX3P
PCIE_NB_TO_SLOTA_N<3>	AD29	PCIE_RX3N
PCIE_NB_TO_SLOTA_P<4>	AC29	PCIE_RX4P
PCIE_NB_TO_SLOTA_N<4>	AB29	PCIE_RX4N
PCIE_NB_TO_SLOTA_P<5>	AB30	PCIE_RX5P
PCIE_NB_TO_SLOTA_N<5>	AA30	PCIE_RX5N
PCIE_NB_TO_SLOTA_P<6>	AA29	PCIE_RX6P
PCIE_NB_TO_SLOTA_N<6>	Y29	PCIE_RX6N
PCIE_NB_TO_SLOTA_P<7>	W29	PCIE_RX7P
PCIE_NB_TO_SLOTA_N<7>	W30	PCIE_RX7N
PCIE_NB_TO_SLOTA_P<8>	V30	PCIE_RX8P
PCIE_NB_TO_SLOTA_N<8>	V29	PCIE_RX8N
PCIE_NB_TO_SLOTA_P<9>	U29	PCIE_RX9P
PCIE_NB_TO_SLOTA_N<9>	T29	PCIE_RX9N
PCIE_NB_TO_SLOTA_P<10>	T30	PCIE_RX10P
PCIE_NB_TO_SLOTA_N<10>	R30	PCIE_RX10N
PCIE_NB_TO_SLOTA_P<11>	R29	PCIE_RX11P
PCIE_NB_TO_SLOTA_N<11>	P29	PCIE_RX11N
PCIE_NB_TO_SLOTA_P<12>	N29	PCIE_RX12P
PCIE_NB_TO_SLOTA_N<12>	N30	PCIE_RX12N
PCIE_NB_TO_SLOTA_P<13>	M30	PCIE_RX13P
PCIE_NB_TO_SLOTA_N<13>	M29	PCIE_RX13N
PCIE_NB_TO_SLOTA_P<14>	L29	PCIE_RX14P
PCIE_NB_TO_SLOTA_N<14>	K29	PCIE_RX14N
PCIE_NB_TO_SLOTA_P<15>	K30	PCIE_RX15P
PCIE_NB_TO_SLOTA_N<15>	J30	PCIE_RX15N

PCIE_PVDD_18: T23 U23 V23 W23
PCIE_PVDD_12: N23 N24 P23
PCIE_VDDR_12: AG26 AG27 AG28 AJ30 AK29

PERST* AD25 ATI_RESET_L_R

GPU PCI-E AC COUPLERS (PLACE NEAR GPU)

PCIE_TX0P	AF26	C8400 0.1UF	PCIE_SLOTA_TO_NB_PF<0>	PCIE_SLOTA_TO_NB_P<0>	
PCIE_TX0N	AE26	C8401 0.1UF	PCIE_SLOTA_TO_NB_NF<0>	PCIE_SLOTA_TO_NB_N<0>	
PCIE_TX1P	AC25	C8402 0.1UF	PCIE_SLOTA_TO_NB_PF<1>	PCIE_SLOTA_TO_NB_P<1>	
PCIE_TX1N	AB25	C8403 0.1UF	PCIE_SLOTA_TO_NB_NF<1>	PCIE_SLOTA_TO_NB_N<1>	
PCIE_TX2P	AC27	C8404 0.1UF	PCIE_SLOTA_TO_NB_PF<2>	PCIE_SLOTA_TO_NB_P<2>	
PCIE_TX2N	AB27	C8405 0.1UF	PCIE_SLOTA_TO_NB_NF<2>	PCIE_SLOTA_TO_NB_N<2>	
PCIE_TX3P	AC26	C8406 0.1UF	PCIE_SLOTA_TO_NB_PF<3>	PCIE_SLOTA_TO_NB_P<3>	
PCIE_TX3N	AB26	C8407 0.1UF	PCIE_SLOTA_TO_NB_NF<3>	PCIE_SLOTA_TO_NB_N<3>	
PCIE_TX4P	Y25	C8408 0.1UF	PCIE_SLOTA_TO_NB_PF<4>	PCIE_SLOTA_TO_NB_P<4>	
PCIE_TX4N	W25	C8409 0.1UF	PCIE_SLOTA_TO_NB_NF<4>	PCIE_SLOTA_TO_NB_N<4>	
PCIE_TX5P	Y27	C8410 0.1UF	PCIE_SLOTA_TO_NB_PF<5>	PCIE_SLOTA_TO_NB_P<5>	
PCIE_TX5N	W27	C8411 0.1UF	PCIE_SLOTA_TO_NB_NF<5>	PCIE_SLOTA_TO_NB_N<5>	
PCIE_TX6P	Y26	C8412 0.1UF	PCIE_SLOTA_TO_NB_PF<6>	PCIE_SLOTA_TO_NB_P<6>	
PCIE_TX6N	W26	C8413 0.1UF	PCIE_SLOTA_TO_NB_NF<6>	PCIE_SLOTA_TO_NB_N<6>	
PCIE_TX7P	U25	C8414 0.1UF	PCIE_SLOTA_TO_NB_PF<7>	PCIE_SLOTA_TO_NB_P<7>	
PCIE_TX7N	T25	C8415 0.1UF	PCIE_SLOTA_TO_NB_NF<7>	PCIE_SLOTA_TO_NB_N<7>	
PCIE_TX8P	U27	C8416 0.1UF	PCIE_SLOTA_TO_NB_PF<8>	PCIE_SLOTA_TO_NB_P<8>	
PCIE_TX8N	T27	C8417 0.1UF	PCIE_SLOTA_TO_NB_NF<8>	PCIE_SLOTA_TO_NB_N<8>	
PCIE_TX9P	U26	C8418 0.1UF	PCIE_SLOTA_TO_NB_PF<9>	PCIE_SLOTA_TO_NB_P<9>	
PCIE_TX9N	T26	C8419 0.1UF	PCIE_SLOTA_TO_NB_NF<9>	PCIE_SLOTA_TO_NB_N<9>	
PCIE_TX10P	P25	C8420 0.1UF	PCIE_SLOTA_TO_NB_PF<10>	PCIE_SLOTA_TO_NB_P<10>	
PCIE_TX10N	N25	C8421 0.1UF	PCIE_SLOTA_TO_NB_NF<10>	PCIE_SLOTA_TO_NB_N<10>	
PCIE_TX11P	P27	C8422 0.1UF	PCIE_SLOTA_TO_NB_PF<11>	PCIE_SLOTA_TO_NB_P<11>	
PCIE_TX11N	N27	C8423 0.1UF	PCIE_SLOTA_TO_NB_NF<11>	PCIE_SLOTA_TO_NB_N<11>	
PCIE_TX12P	P26	C8424 0.1UF	PCIE_SLOTA_TO_NB_PF<12>	PCIE_SLOTA_TO_NB_P<12>	
PCIE_TX12N	N26	C8425 0.1UF	PCIE_SLOTA_TO_NB_NF<12>	PCIE_SLOTA_TO_NB_N<12>	
PCIE_TX13P	L25	C8426 0.1UF	PCIE_SLOTA_TO_NB_PF<13>	PCIE_SLOTA_TO_NB_P<13>	
PCIE_TX13N	K25	C8427 0.1UF	PCIE_SLOTA_TO_NB_NF<13>	PCIE_SLOTA_TO_NB_N<13>	
PCIE_TX14P	L27	C8428 0.1UF	PCIE_SLOTA_TO_NB_PF<14>	PCIE_SLOTA_TO_NB_P<14>	
PCIE_TX14N	K27	C8429 0.1UF	PCIE_SLOTA_TO_NB_NF<14>	PCIE_SLOTA_TO_NB_N<14>	
PCIE_TX15P	L26	C8430 0.1UF	PCIE_SLOTA_TO_NB_PF<15>	PCIE_SLOTA_TO_NB_P<15>	
PCIE_TX15N	K26	C8431 0.1UF	PCIE_SLOTA_TO_NB_NF<15>	PCIE_SLOTA_TO_NB_N<15>	

PP1V2_GPU_PCIE_VDDR
R8400 100 1% 1/16W MF-LF 402
GPU_PCIE_CALRN AB24 PCIE_CALRN
GPU_PCIE_CALRP AC23 PCIE_CALRP
R8401 150 1% 1/16W MF-LF 402

PCIE_CALI AB23 GPU_PCIE_CALI
PCIE_TEST AE25 GPU_PCIE_TEST
R8402 10K 5% 1/16W MF-LF 402
R8403 10K 1% 1/16W MF-LF 402

PCIE_VSS: K28 L28 M24 M25 M26 M27 M28 N28 P28 R23
PCIE_VSS: AH29 AF28 AE28 AD28 AD27 AD26 AD24 AC28 AB28 AA28
PCIE_VSS: R24 R25 R26 R27 R28 T24 T28 U28 V24 V25 V26 V27 V28 W24 W28 Y28 AA23 AA24 AA25 AA26 AA27

XW8405 SM
PCIE_SLOTA_PRSNT_L

GPU PCIe

SYNC_MASTER=M23-DD SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT: 84 OF: 154	

GPU VCORE VREG

NOTE:
SET OUTPUT = 1.25V +/- 2% FOR RV370 XT
1.30V +/- 2% FOR RV380 XT

IRU3037ACS VREF = 0.8 VDC
VOUT=VREF*(R8503+R8505)/R8505
M23=1.272V
M33=1.332V

PEAK CURRENT OF PPVCORE_GPU
7.2A WITH RV370 XT
8.3A WITH RV380 XT

U700 74LC125 SOT23 TSSOP
SYS_POWERUP_L
GPU_POWERUP_L
D8501 MBR0520LXXG SOD-123
D8502 MBR0520LXXG SOD-123
D8503 MBR0520LXXG SOD-123
U8500 VCC_VC IRU3037ACS SOT-LF
Q8500 2N7002 SOT23-LF
Q8501 IRF7807ZPBF SO-8
Q8502 IRF7805ZPBF SO-8
D8511 MMBD914XXG SOT23
XW8500 SM
U5000_FEEDBACK
D8500 SMB 10BQ040PBF
U8570 MM1572FN SOT-25A-LF
U1201 LM339A SOI-LF

GPU 1.7V VDDC_CT

U8590 FAN2558 SOT23-6-LF
Q8590 2N7002 SOT23-LF
VOUT = 0.59V * [1 + R8590 / R8591]
VOUT = 1.691V

GPU 1.20V PCIE PVDD

U8540 FAN2558 SOT23-6-LF
Q8540 2N7002 SOT23-LF
VOUT = 0.59V * [1 + R8540 / R8541]
VOUT = 1.209V

GPU 1.80V TPVDD

U8560 FAN2558 SOT23-6-LF
Q8560 2N7002 SOT23-LF
VOUT = 0.59V * [1 + R8560 / R8561]
VOUT = 1.802V

GPU 2.5V A2VDD

U8570 MM1572FN SOT-25A-LF
Q8570 2N7002 SOT23-LF

GPU 1.8V VREG

U8580 MIC39102 SOP-8-LF
Q8580 2N7002 SOT23-LF

POWER SEQUENCING FOR RV370/80: =PP3V3_GPU > =PPV_GPU_MEM > VDDC_CT > PPVCORE_GPU
PP2V5_GPU_A2VDD > PP1V8_GPU > PCIE_PVDD

THE ENTIRE SEQUENCE SHOULD TAKE LESS THAN 40 MS (T1+T3 IN DATABOOK)
HOWEVER IDEALLY ALL POWER RAILS SHOULD RAMP TOGETHER
POWER DOWN SEQUENCE SHOULD BE IN REVERSE ORDER

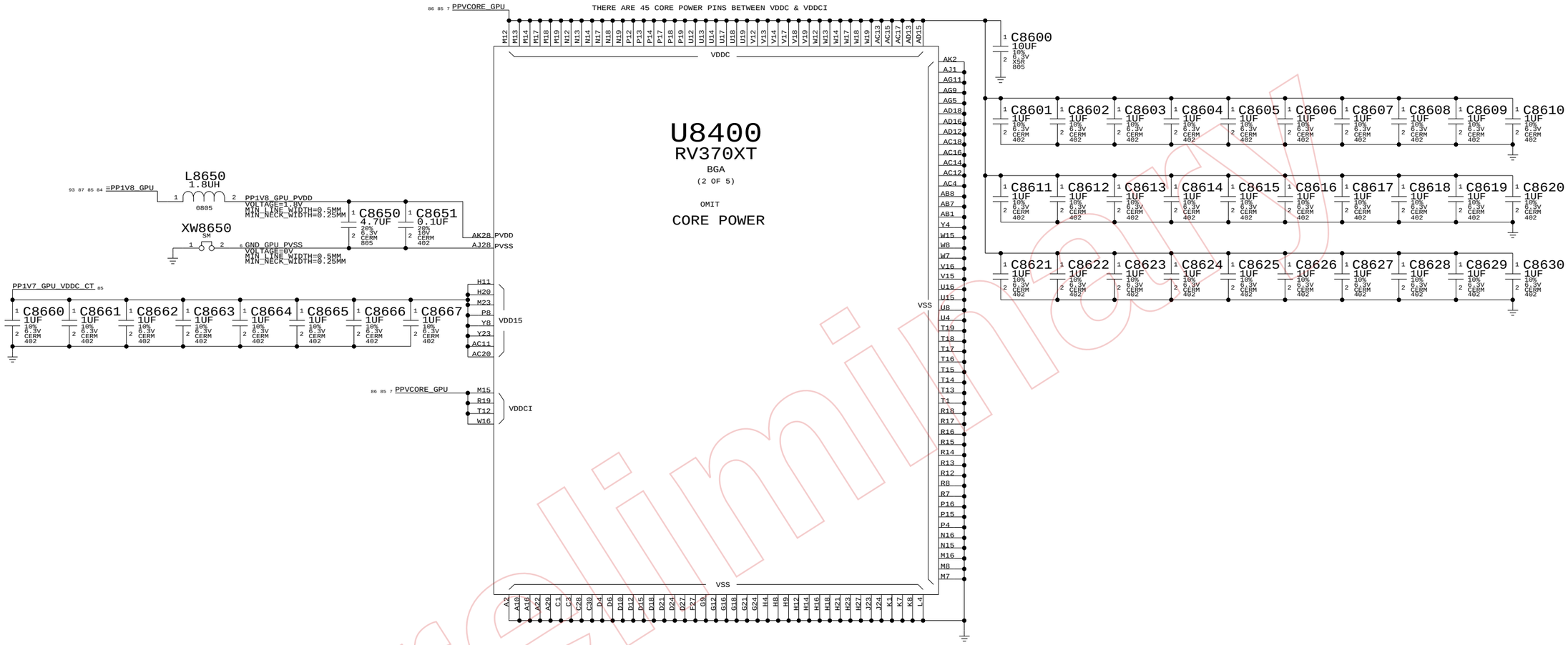
Graphics Vregs

SYNC_MASTER=M23-DD SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E

SCALE: NONE SHT 85 OF 154



GPU Core Power

SYNC_MASTER=FINO-DD SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E

SCALE	SHT	OF
NONE	86	154

=PPV_GPU_MEM

C8700 10UF 10% 6.3V XSR 805
C8701 10UF 10% 6.3V XSR 805
C8702 0.1UF 20% 10V CERM 402
C8703 0.1UF 20% 10V CERM 402
C8704 0.1UF 20% 10V CERM 402
C8705 0.1UF 20% 10V CERM 402
C8706 0.1UF 20% 10V CERM 402
C8707 0.1UF 20% 10V CERM 402
C8708 0.1UF 20% 10V CERM 402
C8709 0.1UF 20% 10V CERM 402
C8710 0.1UF 20% 10V CERM 402
C8711 0.1UF 20% 10V CERM 402
C8712 0.1UF 20% 10V CERM 402
C8713 0.1UF 20% 10V CERM 402
C8714 0.1UF 20% 10V CERM 402
C8715 0.1UF 20% 10V CERM 402
C8716 0.1UF 20% 10V CERM 402
C8717 0.1UF 20% 10V CERM 402
C8718 0.1UF 20% 10V CERM 402
C8719 0.1UF 20% 10V CERM 402

=PP1V8_GPU

L8730 1.8UH 0805
PP1V8_GPU_MPVDD VOLTAGE=1.8V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM

XW8730 SM
GND_GPU_MPVSS VOLTAGE=0V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM

C8730 4.7UF 20% 6.3V CERM 805
C8731 0.1UF 20% 10V CERM 402

VDDR1

OMIT
U8400
RV370XT
BGA
(3 OF 5)

MEMORY INTERFACE A

DQA0	H28	FBD<47>
DQA1	H29	FBD<46>
DQA2	J28	FBD<44>
DQA3	J29	FBD<45>
DQA4	J26	FBD<43>
DQA5	H25	FBD<41>
DQA6	H26	FBD<42>
DQA7	G26	FBD<40>
DQA8	G30	FBD<34>
DQA9	D29	FBD<38>
DQA10	D28	FBD<39>
DQA11	E28	FBD<37>
DQA12	E29	FBD<36>
DQA13	G29	FBD<32>
DQA14	G28	FBD<33>
DQA15	F28	FBD<35>
DQA16	G25	FBD<62>
DQA17	F26	FBD<63>
DQA18	E26	FBD<61>
DQA19	F25	FBD<60>
DQA20	E24	FBD<56>
DQA21	F23	FBD<59>
DQA22	E23	FBD<57>
DQA23	D22	FBD<58>
DQA24	B29	FBD<48>
DQA25	C29	FBD<50>
DQA26	C25	FBD<55>
DQA27	C27	FBD<51>
DQA28	B28	FBD<49>
DQA29	B25	FBD<54>
DQA30	C26	FBD<52>
DQA31	B26	FBD<53>
DQA32	F17	FBD<5>
DQA33	E17	FBD<4>
DQA34	D16	FBD<7>
DQA35	F16	FBD<6>
DQA36	E15	FBD<2>
DQA37	F14	FBD<1>
DQA38	E14	FBD<3>
DQA39	F13	FBD<0>
DQA40	C17	FBD<13>
DQA41	B18	FBD<15>
DQA42	B17	FBD<14>
DQA43	B15	FBD<9>
DQA44	C13	FBD<11>
DQA45	B14	FBD<8>
DQA46	C14	FBD<10>
DQA47	C16	FBD<12>
DQA48	A13	FBD<24>
DQA49	A12	FBD<26>
DQA50	C12	FBD<25>
DQA51	B12	FBD<27>
DQA52	C10	FBD<28>
DQA53	C9	FBD<31>
DQA54	B9	FBD<30>
DQA55	B10	FBD<29>
DQA56	E13	FBD<23>
DQA57	E12	FBD<22>
DQA58	E10	FBD<17>
DQA59	F12	FBD<21>
DQA60	F11	FBD<20>
DQA61	E9	FBD<16>
DQA62	F9	FBD<18>
DQA63	F8	FBD<19>

VDDRH0 F18
VDDRH1 N6
A3 A9 A15 A21 A28 B1 B30 D5 D8 D11 D14 D17 D20 D23 D26 E27 F4 G7 G10 G13 G15 G19 G22 G27 H10 H13 H15 H17

VSSRH0 F19
VSSRH1 M6

MAA0	E22	FBA<0>
MAA1	B22	FBA<1>
MAA2	B23	FBA<2>
MAA3	B24	FBA<3>
MAA4	C23	FBA<4>
MAA5	C22	FBA<5>
MAA6	F22	FBA<6>
MAA7	F21	FBA<7>
MAA8	C21	FBA<8>
MAA9	A24	FBA<9>
MAA10	C24	FBA<10>
MAA11	A25	FBA<11>
MAA12	E21	FBA<12>
MAA13	B20	FBA<13>
MAA14	C19	TP_FBA<14>
DQMA0*	J25	FBDQM<5>
DQMA1*	F29	FBDQM<4>
DQMA2*	E25	FBDQM<7>
DQMA3*	A27	FBDQM<6>
DQMA4*	F15	FBDQM<0>
DQMA5*	C15	FBDQM<1>
DQMA6*	C11	FBDQM<3>
DQMA7*	E11	FBDQM<2>
QSA0	J27	FBDQS<5>
QSA1	F30	FBDQS<4>
QSA2	F24	FBDQS<7>
QSA3	B27	FBDQS<6>
QSA4	E16	FBDQS<0>
QSA5	B16	FBDQS<1>
QSA6	B11	FBDQS<3>
QSA7	F10	FBDQS<2>
RASA*	A19	FBARAS_L
CASA*	E18	FBACAS_L
WEA*	E19	FBAWE_L
CSA0*	E20	FBACS0_L
CSA1*	F20	TP_FBACS1_L
CKEA	B19	FBACKE
CLKA0	B21	FBACLK1
CLKA0*	C20	FBACLK1_L
CLKA1	C18	FBACLK0
CLKA1*	A18	FBACLK0_L
MVREFD	B7	GPU_MVREFD MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM
MVREFS	B8	GPU_MVREFS MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM
DIMA_0	D30	TP_GPU_DIMA_0
DIMA_1	B13	TP_GPU_DIMA_1

R8700 10K 5% 1/16W MF-LF 402
R8720 100 1% 1/16W MF-LF 402
R8721 100 1% 1/16W MF-LF 402
R8722 100 1% 1/16W MF-LF 402
R8723 100 1% 1/16W MF-LF 402
C8721 0.1UF 20% 10V CERM 402
C8723 0.1UF 20% 10V CERM 402

MPVDD	A7	
MPVSS	A6	
DQB0	D7	FBD<124>
DQB1	F7	FBD<127>
DQB2	E7	FBD<125>
DQB3	G6	FBD<121>
DQB4	G5	FBD<120>
DQB5	F5	FBD<123>
DQB6	E5	FBD<122>
DQB7	C4	FBD<126>
DQB8	B5	FBD<113>
DQB9	C5	FBD<112>
DQB10	A4	FBD<114>
DQB11	B4	FBD<115>
DQB12	C2	FBD<117>
DQB13	D3	FBD<119>
DQB14	D1	FBD<116>
DQB15	D2	FBD<118>
DQB16	G4	FBD<111>
DQB17	H6	FBD<110>
DQB18	H5	FBD<109>
DQB19	J6	FBD<108>
DQB20	K5	FBD<104>
DQB21	K4	FBD<105>
DQB22	L6	FBD<107>
DQB23	L5	FBD<106>
DQB24	G2	FBD<103>
DQB25	F3	FBD<99>
DQB26	H2	FBD<102>
DQB27	E2	FBD<97>
DQB28	F2	FBD<98>
DQB29	J3	FBD<100>
DQB30	F1	FBD<96>
DQB31	H3	FBD<101>
DQB32	U6	FBD<86>
DQB33	U5	FBD<84>
DQB34	U3	FBD<85>
DQB35	V6	FBD<87>
DQB36	W5	FBD<82>
DQB37	W4	FBD<83>
DQB38	Y6	FBD<80>
DQB39	Y5	FBD<81>
DQB40	U2	FBD<88>
DQB41	V2	FBD<91>
DQB42	V1	FBD<90>
DQB43	V3	FBD<89>
DQB44	W3	FBD<92>
DQB45	Y2	FBD<93>
DQB46	Y3	FBD<94>
DQB47	AA2	FBD<95>
DQB48	AA6	FBD<71>
DQB49	AA5	FBD<69>
DQB50	AB6	FBD<68>
DQB51	AB5	FBD<70>
DQB52	AD6	FBD<66>
DQB53	AD5	FBD<64>
DQB54	AE5	FBD<65>
DQB55	AE4	FBD<67>
DQB56	AB2	FBD<72>
DQB57	AB3	FBD<73>
DQB58	AC2	FBD<75>
DQB59	AC3	FBD<74>
DQB60	AD3	FBD<78>
DQB61	AE1	FBD<79>
DQB62	AE2	FBD<76>
DQB63	AE3	FBD<77>

H19 H22 J1 J4 J7 J8 K23 K24 L8 L23 M4 M7 M8 R1 R4 T7 T8 V4 V7 V8 AA1 AA4 AA7 AA8 AD4

VDDR1

OMIT
U8400
RV370XT
BGA
(4 OF 5)

MEMORY INTERFACE B

MAB0	N5	FBBA<0>
MAB1	M1	FBBA<1>
MAB2	M3	FBBA<2>
MAB3	L3	FBBA<3>
MAB4	L2	FBBA<4>
MAB5	M2	FBBA<5>
MAB6	M5	FBBA<6>
MAB7	P6	FBBA<7>
MAB8	N3	FBBA<8>
MAB9	K2	FBBA<9>
MAB10	K3	FBBA<10>
MAB11	J2	FBBA<11>
MAB12	P5	FBBA<12>
MAB13	P3	FBBA<13>
MAB14	P2	TP_FBBA<14>
DQMB0*	E6	FBDQM<15>
DQMB1*	B2	FBDQM<14>
DQMB2*	J5	FBDQM<13>
DQMB3*	G3	FBDQM<12>
DQMB4*	W6	FBDQM<10>
DQMB5*	W2	FBDQM<11>
DQMB6*	AC6	FBDQM<8>
DQMB7*	AD2	FBDQM<9>
QSB0	F6	FBDQS<15>
QSB1	B3	FBDQS<14>
QSB2	K6	FBDQS<13>
QSB3	G1	FBDQS<12>
QSB4	V5	FBDQS<10>
QSB5	W1	FBDQS<11>
QSB6	AC5	FBDQS<8>
QSB7	AD1	FBDQS<9>
RASB*	R2	FBBRAS_L
CASB*	T5	FBBCAS_L
WEB*	T6	FBBWE_L
CSB0*	R5	FBBCS0_L
CSB1*	R6	TP_FBBCS1_L
CKEB	R3	FBBCKE
CLKB0	N1	FBBCLK1
CLKB0*	N2	FBBCLK1_L
CLKB1	T2	FBBCLK0
CLKB1*	T3	FBBCLK0_L
MEMVMODE0	C6	GPU_MEMVMODE0
MEMVMODE1	C7	GPU_MEMVMODE1
MEMTEST	C8	GPU_MEMTEST MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM
DIMB_0	E3	TP_GPU_DIMB_0
DIMB_1	AA3	TP_GPU_DIMB_1

R8701 10K 5% 1/16W MF-LF 402
R8724 4.7K 5% 1/16W MF-LF 402 NOSTUFF
R8726 4.7K 5% 1/16W MF-LF 402
R8725 4.7K 5% 1/16W MF-LF 402 NOSTUFF
R8727 4.7K 5% 1/16W MF-LF 402
R8728 47 1% 1/16W MF-LF 402

=PPV_GPU_MEM

MEMVMODE	01
* 1.8V	01
2.5V	10
2.8V	11

GPU Frame Buffer

SYNC_MASTER=FINO-DD SYNC_DATE=06/20/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E

SCALE NONE SHT 87 OF 154

FRAME BUFFER A TERMINATION

PLACE R'S CLOSE TO MEMORY

FBD<31>	22	3	6	RP8820	RFBD<31>
FBD<30>	22	4	5	RP8820	RFBD<30>
FBD<29>	22	1	8	RP8820	RFBD<29>
FBD<28>	22	2	7	RP8820	RFBD<28>
FBD<27>	22	3	6	RP8821	RFBD<27>
FBD<26>	22	4	5	RP8821	RFBD<26>
FBD<25>	22	2	7	RP8821	RFBD<25>
FBD<24>	22	1	8	RP8821	RFBD<24>
FBD<0>	22	1	8	RP8822	RFBD<0>
FBD<1>	22	2	7	RP8822	RFBD<1>
FBD<2>	22	4	5	RP8822	RFBD<2>
FBD<3>	22	3	6	RP8822	RFBD<3>
FBD<17>	22	1	8	RP8823	RFBD<17>
FBD<16>	22	2	7	RP8823	RFBD<16>
FBD<18>	22	3	6	RP8823	RFBD<18>
FBD<19>	22	4	5	RP8823	RFBD<19>
FBD<15>	22	4	5	RP8824	RFBD<15>
FBD<14>	22	3	6	RP8824	RFBD<14>
FBD<13>	22	2	7	RP8824	RFBD<13>
FBD<12>	22	1	8	RP8824	RFBD<12>
FBD<10>	22	3	6	RP8825	RFBD<10>
FBD<11>	22	4	5	RP8825	RFBD<11>
FBD<9>	22	1	8	RP8825	RFBD<9>
FBD<8>	22	2	7	RP8825	RFBD<8>
FBD<5>	22	2	7	RP8826	RFBD<5>
FBD<6>	22	3	6	RP8826	RFBD<6>
FBD<4>	22	1	8	RP8826	RFBD<4>
FBD<7>	22	4	5	RP8826	RFBD<7>
FBD<20>	22	1	8	RP8827	RFBD<20>
FBD<21>	22	2	7	RP8827	RFBD<21>
FBD<22>	22	3	6	RP8827	RFBD<22>
FBD<23>	22	4	5	RP8827	RFBD<23>

FBD<32>	22	3	6	RP8828	RFBD<32>
FBD<33>	22	4	5	RP8828	RFBD<33>
FBD<34>	22	2	7	RP8828	RFBD<34>
FBD<35>	22	1	8	RP8828	RFBD<35>
FBD<36>	22	4	5	RP8816	RFBD<36>
FBD<37>	22	3	6	RP8816	RFBD<37>
FBD<38>	22	2	7	RP8816	RFBD<38>
FBD<39>	22	1	8	RP8816	RFBD<39>
FBD<40>	22	3	6	RP8829	RFBD<40>
FBD<41>	22	4	5	RP8829	RFBD<41>
FBD<42>	22	2	7	RP8829	RFBD<42>
FBD<43>	22	1	8	RP8829	RFBD<43>
FBD<44>	22	4	5	RP8830	RFBD<44>
FBD<45>	22	3	6	RP8830	RFBD<45>
FBD<46>	22	1	8	RP8830	RFBD<46>
FBD<47>	22	2	7	RP8830	RFBD<47>
FBD<48>	22	4	5	RP8831	RFBD<48>
FBD<49>	22	2	7	RP8831	RFBD<49>
FBD<50>	22	3	6	RP8831	RFBD<50>
FBD<51>	22	1	8	RP8831	RFBD<51>
FBD<52>	22	3	6	RP8800	RFBD<52>
FBD<53>	22	4	5	RP8800	RFBD<53>
FBD<54>	22	2	7	RP8800	RFBD<54>
FBD<55>	22	1	8	RP8800	RFBD<55>
FBD<56>	22	4	5	RP8801	RFBD<56>
FBD<57>	22	3	6	RP8801	RFBD<57>
FBD<58>	22	1	8	RP8801	RFBD<58>
FBD<59>	22	2	7	RP8801	RFBD<59>
FBD<60>	22	4	5	RP8802	RFBD<60>
FBD<61>	22	2	7	RP8802	RFBD<61>
FBD<62>	22	3	6	RP8802	RFBD<62>
FBD<63>	22	1	8	RP8802	RFBD<63>

FBDQS<0>	22	R8800	RFBDQS<0>
FBDQS<1>	22	R8801	RFBDQS<1>
FBDQS<2>	22	R8802	RFBDQS<2>
FBDQS<3>	22	R8803	RFBDQS<3>
FBDQS<4>	22	R8804	RFBDQS<4>
FBDQS<5>	22	R8805	RFBDQS<5>
FBDQS<6>	22	R8806	RFBDQS<6>
FBDQS<7>	22	R8807	RFBDQS<7>

FBDQM<0>	22	R8830	RFBDQM<0>
FBDQM<1>	22	R8831	RFBDQM<1>
FBDQM<2>	22	R8832	RFBDQM<2>
FBDQM<3>	22	R8833	RFBDQM<3>
FBDQM<4>	22	R8834	RFBDQM<4>
FBDQM<5>	22	R8835	RFBDQM<5>
FBDQM<6>	22	R8836	RFBDQM<6>
FBDQM<7>	22	R8837	RFBDQM<7>

PLACE CLOCK TERMINATION AFTER MEMORY
GPU -> MEMORY -> TERMINATION

FBACLK0
R8820 56.2 1% 1/10W MF-LF 402
FBACLK0_TERM
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
R8821 56.2 1% 1/10W MF-LF 402
C8821 0.01UF 20% 16V CERM 402
FBACLK0_L

FBACLK1
R8822 56.2 1% 1/10W MF-LF 402
FBACLK1_TERM
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
R8823 56.2 1% 1/10W MF-LF 402
C8823 0.01UF 20% 16V CERM 402
FBACLK1_L

FRAME BUFFER B TERMINATION

FBD<64>	22	1	8	RP8810	RFBD<64>
FBD<65>	22	4	5	RP8810	RFBD<65>
FBD<66>	22	2	7	RP8810	RFBD<66>
FBD<67>	22	3	6	RP8810	RFBD<67>
FBD<84>	22	1	8	RP8809	RFBD<84>
FBD<85>	22	2	7	RP8809	RFBD<85>
FBD<86>	22	3	6	RP8809	RFBD<86>
FBD<87>	22	4	5	RP8809	RFBD<87>
FBD<72>	22	2	7	RP8819	RFBD<72>
FBD<73>	22	1	8	RP8819	RFBD<73>
FBD<75>	22	4	5	RP8819	RFBD<75>
FBD<74>	22	3	6	RP8819	RFBD<74>
FBD<68>	22	1	8	RP8808	RFBD<68>
FBD<70>	22	2	7	RP8808	RFBD<70>
FBD<69>	22	3	6	RP8808	RFBD<69>
FBD<71>	22	4	5	RP8808	RFBD<71>
FBD<80>	22	1	8	RP8807	RFBD<80>
FBD<81>	22	2	7	RP8807	RFBD<81>
FBD<82>	22	3	6	RP8807	RFBD<82>
FBD<83>	22	4	5	RP8807	RFBD<83>
FBD<76>	22	2	7	RP8817	RFBD<76>
FBD<77>	22	1	8	RP8817	RFBD<77>
FBD<78>	22	4	5	RP8817	RFBD<78>
FBD<79>	22	3	6	RP8817	RFBD<79>
FBD<91>	22	3	6	RP8818	RFBD<91>
FBD<90>	22	4	5	RP8818	RFBD<90>
FBD<89>	22	1	8	RP8818	RFBD<89>
FBD<88>	22	2	7	RP8818	RFBD<88>
FBD<95>	22	3	6	RP8803	RFBD<95>
FBD<94>	22	4	5	RP8803	RFBD<94>
FBD<93>	22	1	8	RP8803	RFBD<93>
FBD<92>	22	2	7	RP8803	RFBD<92>

FBD<96>	22	4	5	RP8815	RFBD<96>
FBD<97>	22	3	6	RP8815	RFBD<97>
FBD<98>	22	2	7	RP8815	RFBD<98>
FBD<99>	22	1	8	RP8815	RFBD<99>
FBD<100>	22	4	5	RP8814	RFBD<100>
FBD<101>	22	3	6	RP8814	RFBD<101>
FBD<102>	22	2	7	RP8814	RFBD<102>
FBD<103>	22	1	8	RP8814	RFBD<103>
FBD<104>	22	4	5	RP8812	RFBD<104>
FBD<105>	22	3	6	RP8812	RFBD<105>
FBD<106>	22	2	7	RP8812	RFBD<106>
FBD<107>	22	1	8	RP8812	RFBD<107>
FBD<108>	22	4	5	RP8813	RFBD<108>
FBD<109>	22	3	6	RP8813	RFBD<109>
FBD<110>	22	2	7	RP8813	RFBD<110>
FBD<111>	22	1	8	RP8813	RFBD<111>
FBD<112>	22	3	6	RP8811	RFBD<112>
FBD<113>	22	4	5	RP8811	RFBD<113>
FBD<114>	22	2	7	RP8811	RFBD<114>
FBD<115>	22	1	8	RP8811	RFBD<115>
FBD<116>	22	3	6	RP8806	RFBD<116>
FBD<117>	22	4	5	RP8806	RFBD<117>
FBD<118>	22	2	7	RP8806	RFBD<118>
FBD<119>	22	1	8	RP8806	RFBD<119>
FBD<120>	22	3	6	RP8804	RFBD<120>
FBD<121>	22	4	5	RP8804	RFBD<121>
FBD<122>	22	2	7	RP8804	RFBD<122>
FBD<123>	22	1	8	RP8804	RFBD<123>
FBD<124>	22	4	5	RP8805	RFBD<124>
FBD<125>	22	2	7	RP8805	RFBD<125>
FBD<126>	22	3	6	RP8805	RFBD<126>
FBD<127>	22	1	8	RP8805	RFBD<127>

FBDQS<8>	22	R8808	RFBDQS<8>
FBDQS<9>	22	R8809	RFBDQS<9>
FBDQS<10>	22	R8810	RFBDQS<10>
FBDQS<11>	22	R8811	RFBDQS<11>
FBDQS<12>	22	R8812	RFBDQS<12>
FBDQS<13>	22	R8813	RFBDQS<13>
FBDQS<14>	22	R8814	RFBDQS<14>
FBDQS<15>	22	R8815	RFBDQS<15>

FBDQM<8>	22	R8838	RFBDQM<8>
FBDQM<9>	22	R8839	RFBDQM<9>
FBDQM<10>	22	R8840	RFBDQM<10>
FBDQM<11>	22	R8841	RFBDQM<11>
FBDQM<12>	22	R8842	RFBDQM<12>
FBDQM<13>	22	R8843	RFBDQM<13>
FBDQM<14>	22	R8844	RFBDQM<14>
FBDQM<15>	22	R8845	RFBDQM<15>

FBBCLK0
R8824 56.2 1% 1/10W MF-LF 402
FBBCLK0_TERM
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
R8825 56.2 1% 1/10W MF-LF 402
C8825 0.01UF 20% 16V CERM 402
FBBCLK0_L

FBBCLK1
R8826 56.2 1% 1/10W MF-LF 402
FBBCLK1_TERM
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
R8827 56.2 1% 1/10W MF-LF 402
C8827 0.01UF 20% 16V CERM 402
FBBCLK1_L

	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
FBD<127..0>		GPU_FB	GPU_FB	
RFBD<127..0>		GPU_FB	GPU_FB	
FBA<13..0>		GPU_FB	GPU_FB	
FBBA<13..0>		GPU_FB	GPU_FB	
FBDQM<15..0>		GPU_FB	GPU_FB	
FBDQS<15..0>		GPU_FB	GPU_FBDQS	
FBARAS_L		GPU_FB	GPU_FB	
FBACAS_L		GPU_FB	GPU_FB	
FBAWE_L		GPU_FB	GPU_FB	
FBACS0_L		GPU_FB	GPU_FB	
FBACKE		GPU_FB	GPU_FB	
FBBRAS_L		GPU_FB	GPU_FB	
FBBCAS_L		GPU_FB	GPU_FB	
FBBWE_L		GPU_FB	GPU_FB	
FBBCS0_L		GPU_FB	GPU_FB	
FBBCKE		GPU_FB	GPU_FB	

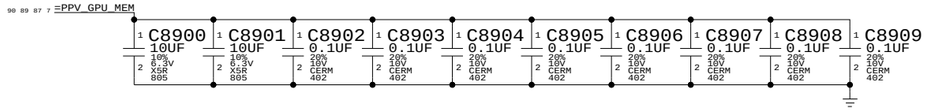
	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
FBACLK0		GPU_FBCLK	GPU_FBCLK	FBACLK0
FBACLK0_L		GPU_FBCLK	GPU_FBCLK	FBACLK0
FBACLK1		GPU_FBCLK	GPU_FBCLK	FBACLK1
FBACLK1_L		GPU_FBCLK	GPU_FBCLK	FBACLK1
FBBCLK0		GPU_FBCLK	GPU_FBCLK	FBBCLK0
FBBCLK0_L		GPU_FBCLK	GPU_FBCLK	FBBCLK0
FBBCLK1		GPU_FBCLK	GPU_FBCLK	FBBCLK1
FBBCLK1_L		GPU_FBCLK	GPU_FBCLK	FBBCLK1

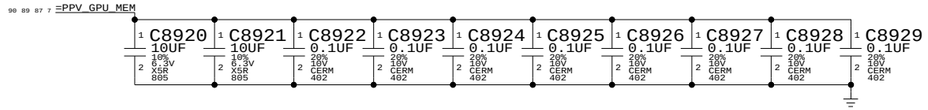
FB Series Termination

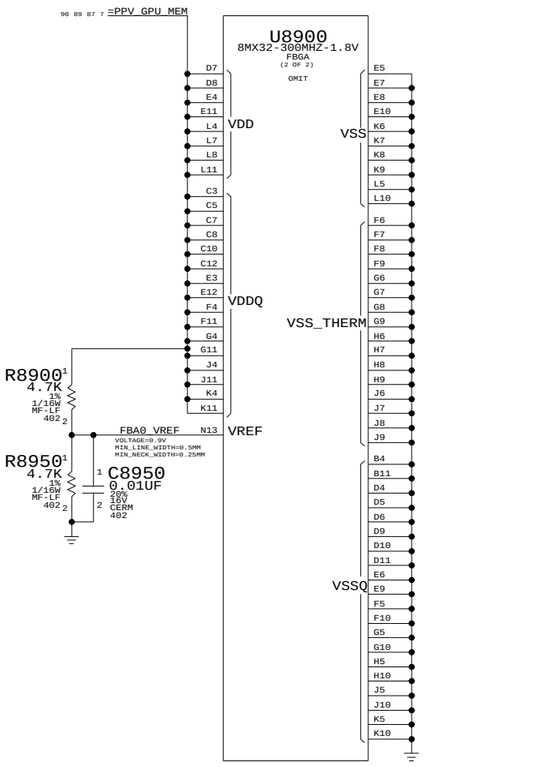
SYNC_MASTER=FINO-DD SYNC_DATE=06/20/2005

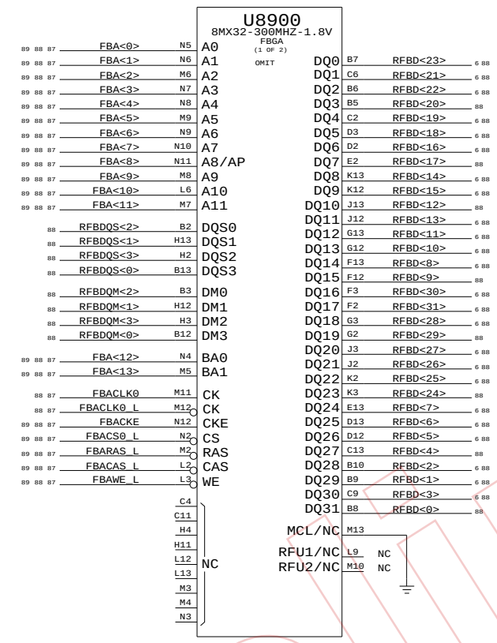
APPLE COMPUTER INC.

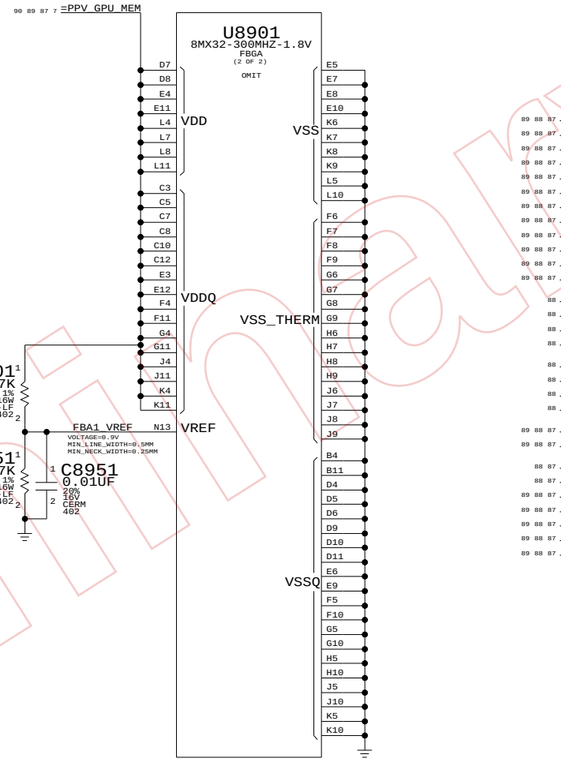
SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 88 OF 154	

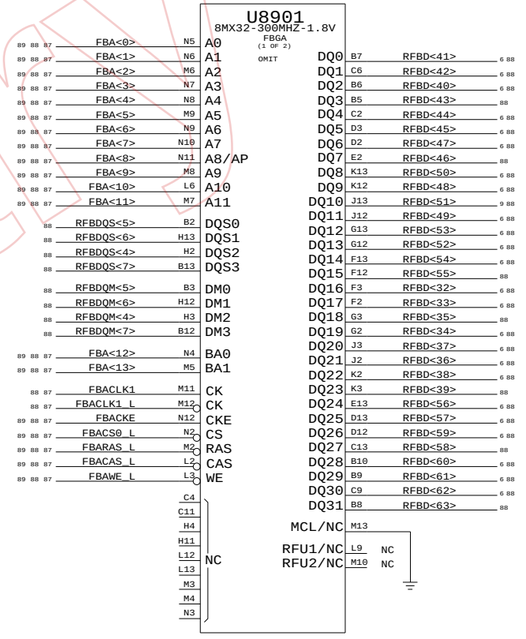


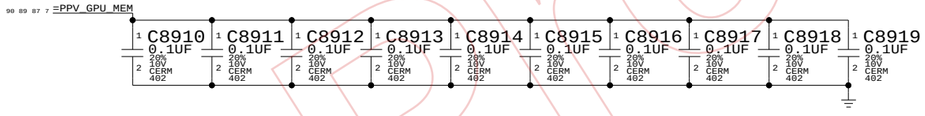


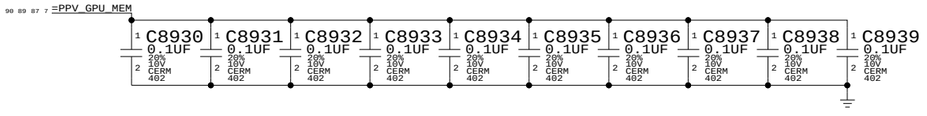


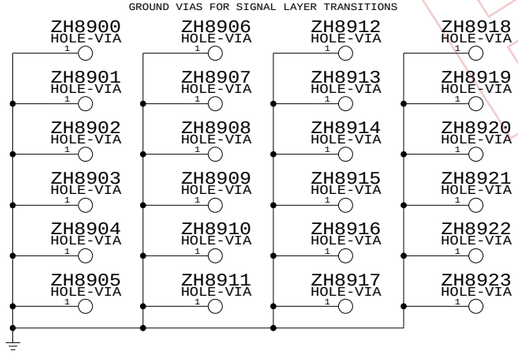












PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
333S0319	2	SDRAM,4MX32,GDDR,300MHZ,1.8V,SAM	U8900,U8901	CRITICAL	FB64MB_300MHZ_SAM	SAMSUNG
333S0311	2	SDRAM,8MX32,GDDR,300MHZ,1.8V,SAM	U8900,U8901	CRITICAL	FB128MB_300MHZ_SAM	
333S0312	2	SDRAM,8MX32,GDDR,350MHZ,1.8V,SAM	U8900,U8901	CRITICAL	FB128MB_350MHZ_SAM	
333S0320	2	SDRAM,4MX32,GDDR,300MHZ,1.8V,HYN	U8900,U8901	CRITICAL	FB64MB_300MHZ_HYN	HYNIX
333S0314	2	SDRAM,8MX32,GDDR,300MHZ,1.8V,HYN	U8900,U8901	CRITICAL	FB128MB_300MHZ_HYN	
333S0315	2	SDRAM,8MX32,GDDR,350MHZ,1.8V,HYN	U8900,U8901	CRITICAL	FB128MB_350MHZ_HYN	

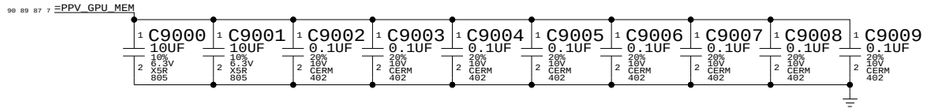
GPU GDDR SDRAM A

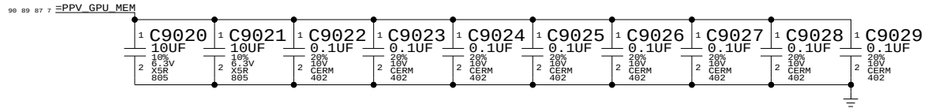
SYNC_MASTER=FINO-DD SYNC_DATE=06/20/2005

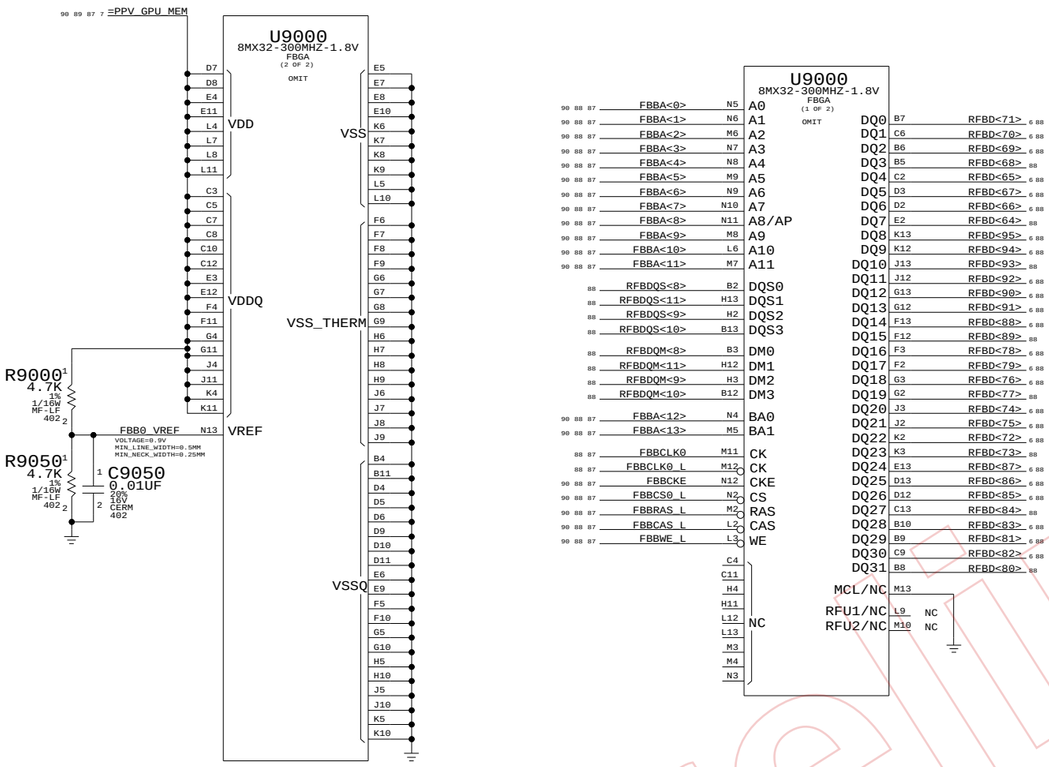
APPLE COMPUTER INC.

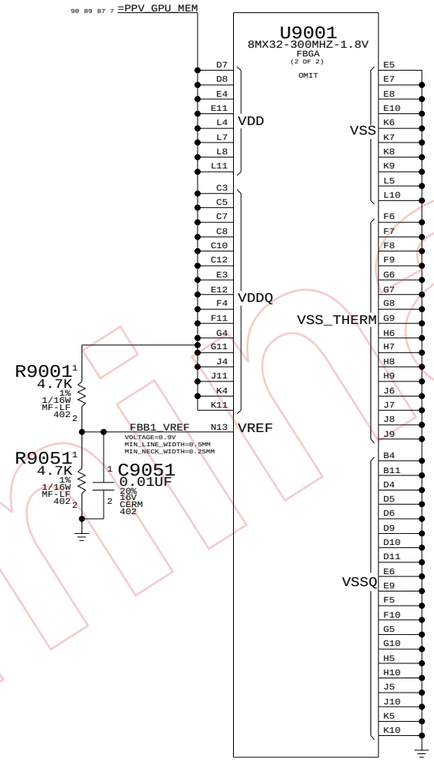
SIZE	DRAWING NUMBER	REV.
D	051-6790	E

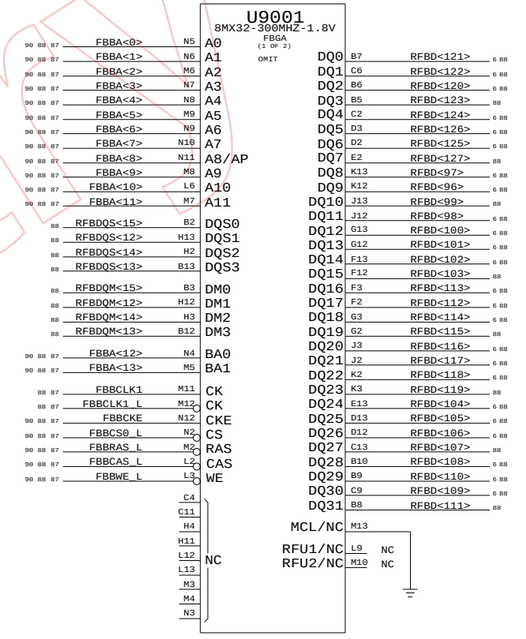
SCALE	SHT	OF
NONE	89	154

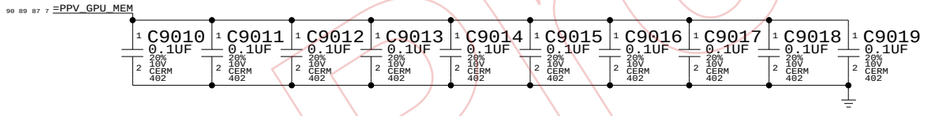


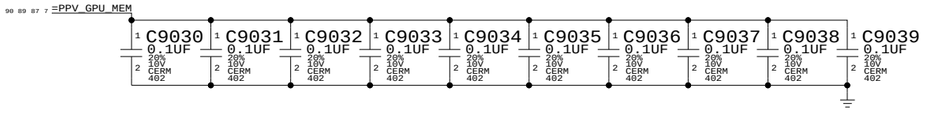


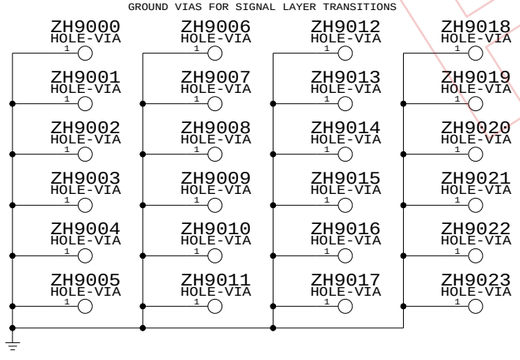












PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
333S0319	2	SDRAM,4MX32,GDDR,300MHZ,1.8V,SAM	U9000,U9001	CRITICAL	FB64MB_300MHZ_SAM	SAMSUNG
333S0311	2	SDRAM,8MX32,GDDR,300MHZ,1.8V,SAM	U9000,U9001	CRITICAL	FB128MB_300MHZ_SAM	
333S0312	2	SDRAM,8MX32,GDDR,350MHZ,1.8V,SAM	U9000,U9001	CRITICAL	FB128MB_350MHZ_SAM	
333S0320	2	SDRAM,4MX32,GDDR,300MHZ,1.8V,HYN	U9000,U9001	CRITICAL	FB64MB_300MHZ_HYN	HYNIX
333S0314	2	SDRAM,8MX32,GDDR,300MHZ,1.8V,HYN	U9000,U9001	CRITICAL	FB128MB_300MHZ_HYN	
333S0315	2	SDRAM,8MX32,GDDR,350MHZ,1.8V,HYN	U9000,U9001	CRITICAL	FB128MB_350MHZ_HYN	

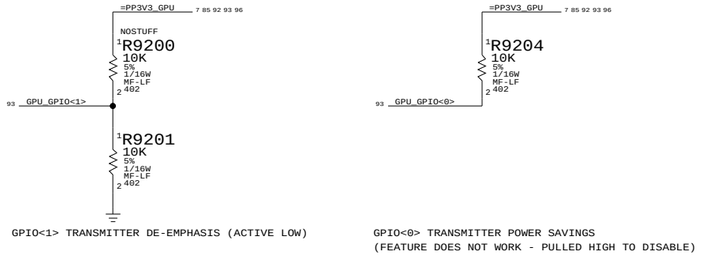
GPU GDDR SDRAM B

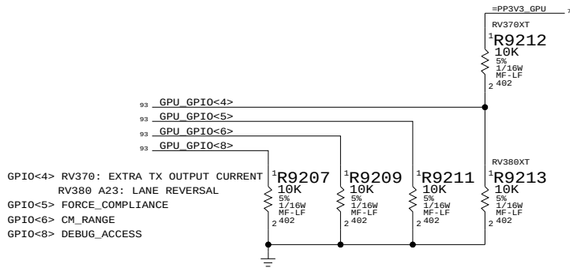
SYNC_MASTER=FINO-DD SYNC_DATE=06/20/2005

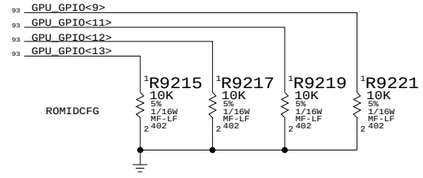
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 90 OF 154	

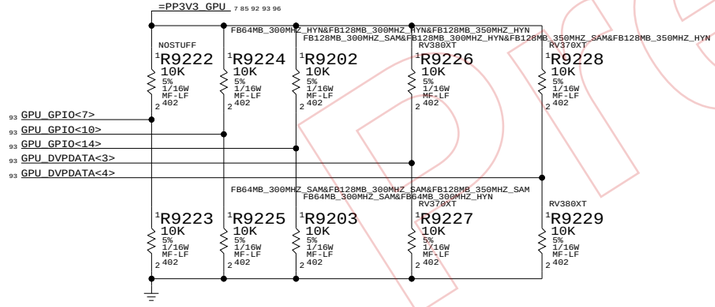
ATI STRAPS





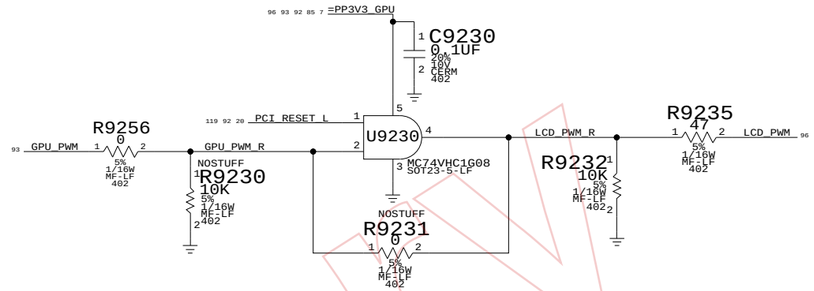


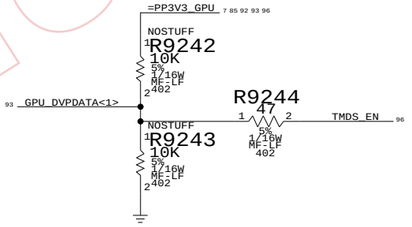
MEMORY STRAPS

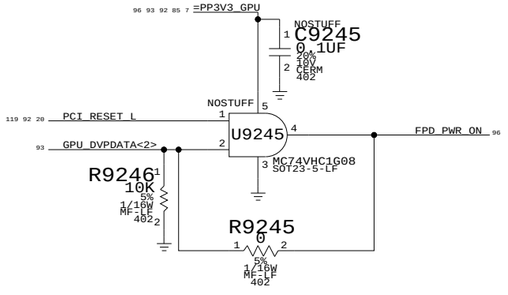


GPIO<7> - MEMORY DIE REVISION
  0 - ORIGINAL DIE REVISION
  1 - NEW (FUTURE) DIE REV
GPIO<10> - MEMORY VENDOR
  0 - SAMSUNG
  1 - HYNIX
GPIO<14> - MEMORY DENSITY
  0 - 4MX32
  1 - 8MX32
DVPDATA<3,4> - SPEED
  00 - 325E / 200M
  01 - 400E / 300M
  10 - 500E / 350M
  11 - RESERVED FOR FUTURE USE

APPLE GPIOS







GPU Straps

SYNC_MASTER=FINO-DD SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 92 OF 154	

SPREAD SPECTRUM SUPPORT

S0=1;S1=M => -1.5% DOWN-SPREAD

27M OSC

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0176	1	OSC, XTAL, 27 MHZ, 30PPM	G9370	CRITICAL	

U8400 RV370XT BGA (5 OF 5)

GPIO	GPIO_0	AJ5	GPU_GPIO<0>
	GPIO_1	AH5	GPU_GPIO<1>
	GPIO_2	AJ4	TP_GPU_GPIO<2>
	GPIO_3	AK4	TP_GPU_GPIO<3>
	GPIO_4	AH4	GPU_GPIO<4>
	GPIO_5	AF4	GPU_GPIO<5>
	GPIO_6	AJ3	GPU_GPIO<6>
	GPIO_7	AK3	GPU_GPIO<7>
	GPIO_8	AH3	GPU_GPIO<8>
	GPIO_9	AJ2	GPU_GPIO<9>
	GPIO_10	AH2	GPU_GPIO<10>
	GPIO_11	AH1	GPU_GPIO<11>
	GPIO_12	AG3	GPU_GPIO<12>
	GPIO_13	AG1	GPU_GPIO<13>
	GPIO_14	AG2	GPU_GPIO<14>
	GPIO+PWRCNTL	AF3	
	GPIO_MEMSSIN	AF2	GPU_MEMSSIN
	VREFG	AG4	GPU_VREFG
CLK	XTALOUT	AJ29	NC
	XTALIN	AH28	GPU_CLK27M_IN
	PLLTEST	AF25	NC
TEST	TESTEN	AH27	GPU_TESTEN
	TEST_YCLK	E8	
	TEST_MCLK	B6	
	DPLUS	AF11	GPU_DIODE_PLUS
	DMINUS	AE11	GPU_DIODE_MINUS
	HPD1	AF12	MON_DETECT_R
NC		AG15	
		AG16	
		AG17	
		AG18	
		AG20	
		AH15	
		AH16	
		AH17	
		AH18	
		AH19	
		AH24	
		AJ16	
		AJ17	
		AJ18	
		AJ19	
		AJ20	
		AJ21	
		AJ23	
		AK18	
TXVDDR		AF13	
		AF14	
TXVSSR		AG13	
		AG14	
		AH14	
TPVDD		AH13	
TPVSS		AH12	
VDD1DI		AE23	
VDD2DI		AE22	
VSS1DI		AE24	
VSS2DI		AE21	
AVDD		AH23	
AVSSQ		AD22	GND_GPU_AVSSQ
AVSSN		AH22	
A2VDD		AE20	
		AF21	
A2VSSN		AG21	
		AH20	
A2VDDQ		AF23	
A2VSSQ		AF22	

EXTERNAL TMDS	DVPDATA_0	AH6	GPU_DVPDATA<0>
	DVPDATA_1	AJ6	GPU_DVPDATA<1>
	DVPDATA_2	AK6	GPU_DVPDATA<2>
	DVPDATA_3	AH7	GPU_DVPDATA<3>
	DVPDATA_4	AK7	GPU_DVPDATA<4>
	DVPDATA_5	AJ7	TP_GPU_DVPDATA<5>
	DVPDATA_6	AH8	TP_GPU_DVPDATA<6>
	DVPDATA_7	AJ8	TP_GPU_DVPDATA<7>
	DVPDATA_8	AH9	TP_GPU_DVPDATA<8>
	DVPDATA_9	AJ9	TP_GPU_DVPDATA<9>
	DVPDATA_10	AK9	TP_GPU_DVPDATA<10>
	DVPDATA_11	AH10	TP_GPU_DVPDATA<11>
	DVPDATA_12	AE6	TP_GPU_DVPDATA<12>
	DVPDATA_13	AG6	TP_GPU_DVPDATA<13>
	DVPDATA_14	AF6	TP_GPU_DVPDATA<14>
	DVPDATA_15	AE7	TP_GPU_DVPDATA<15>
	DVPDATA_16	AF7	TP_GPU_DVPDATA<16>
	DVPDATA_17	AE8	TP_GPU_DVPDATA<17>
	DVPDATA_18	AG8	TP_GPU_DVPDATA<18>
	DVPDATA_19	AF8	TP_GPU_DVPDATA<19>
	DVPDATA_20	AE9	TP_GPU_DVPDATA<20>
	DVPDATA_21	AF9	TP_GPU_DVPDATA<21>
	DVPDATA_22	AG10	TP_GPU_DVPDATA<22>
	DVPDATA_23	AF10	TP_GPU_DVPDATA<23>
DVPCNTL	0	AJ10	GPU_DVPCNTL
	1	AK10	
	2	AJ11	
	3	AH11	
DVOMODE		AE10	
NC		D9	
		D13	
		D19	
		D25	
		E4	
		T4	
		AB4	
		AE12	
		AE15	
		AE16	
		AE17	
		AE18	
		AE19	
		AE15	
		AF16	
		AF17	
		AF18	
		AF19	
		AF20	
	GPU_PWM	AG12	GPU_PWM
TMDS	TXCP	AK12	TMDS_CKP
	TXCM*	AJ12	TMDS_CKM
	TX0P	AJ13	TMDS_D0P
	TX0M*	AK13	TMDS_D0M
	TX1P	AJ15	TMDS_D1P
	TX1M*	AJ14	TMDS_D1M
	TX2P	AK16	TMDS_D2P
	TX2M*	AK15	TMDS_D2M
	DDC3CLK	AG22	I2C_GPU_TMDS_SCL
	DDC3DATA	AG23	I2C_GPU_TMDS_SDA
DAC1	R	AK27	NC
	G	AJ27	NC
	B	AJ26	NC
	HSYNC	AJ25	TP_GPU_HSYNC
	VSYNC	AK25	
	RSET	AH26	
	DDC1CLK	AF24	TP_GPU_DDC1CLK
	DDC1DATA	AG25	TP_GPU_DDC1DATA
	GPIO_AUXWIN	AG24	NC
	STEREOSYNC	AH25	
DAC2	Y_G	AK21	ANALOG_GRN
	C_R	AJ22	ANALOG_RED
	COMP_B	AK22	ANALOG_BLU
	H2SYNC	AJ24	ANALOG_HSYNC
	V2SYNC	AK24	ANALOG_VSYNC
	R2SET	AH21	
	DDC2CLK	AE13	I2C_GPU_MON_SCL
	DDC2DATA	AE14	I2C_GPU_MON_SDA

NO CONNECTS

DIFFERENTIAL IMPEDANCE SHOULD BE 100 OHM

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
TMDS_TCKM	GPU_TMDS	GPU_TMDS	TMDS_CK
	GPU_TMDS	GPU_TMDS	TMDS_CK
TMDS0	GPU_TMDS	GPU_TMDS	TMDS_D0
	GPU_TMDS	GPU_TMDS	TMDS_D0
TMDS0	GPU_TMDS	GPU_TMDS	TMDS_D1
	GPU_TMDS	GPU_TMDS	TMDS_D1
TMDS0	GPU_TMDS	GPU_TMDS	TMDS_D2
	GPU_TMDS	GPU_TMDS	TMDS_D2
	GPU_VGA	GPU_VGA	
	GPU_VGA	GPU_VGA	
	GPU_VGA	GPU_VGA	
	GPU_VGA	GPU_VGA	
	GPU_VGA	GPU_VGA	
		I2C	
		I2C	
		I2C	
		I2C	

GPU THERMAL SENSOR

PLACE C9392 CLOSE TO TEMP SENSOR

PLACE R9321-3 & FL9600-2 NEAR MINI-VGA CONNECTOR

ROUTE GND IN BETWEEN RGB SIGNALS WITH A VIA EVERY INCH

PLACE R9373 CLOSE TO ATI PIN AH28

(PLACE R9371 AND R9372 CLOSE TO OSCILLATOR PIN 8)

(PLACE R9371 CLOSE TO OSC)

GPU DVI & DACs

SYNC_MASTER=FINO-DD SYNC_DATE=06/20/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 93 OF 154	

INTERNAL LCD

	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
TCKP	GPU_TMDS	GPU_TMDS	TCK
TCKM	GPU_TMDS	GPU_TMDS	TCK
TD0P	GPU_TMDS	GPU_TMDS	TD0
TD0M	GPU_TMDS	GPU_TMDS	TD0
TD1P	GPU_TMDS	GPU_TMDS	TD1
TD1M	GPU_TMDS	GPU_TMDS	TD1
TD2P	GPU_TMDS	GPU_TMDS	TD2
TD2M	GPU_TMDS	GPU_TMDS	TD2

PLACE R9600-R9604, C9600 AS CLOSE TO GPU AS POSSIBLE

PLACE FILTER CLOSE TO TMDS CONNECTOR

TMDS_D2M — R9626 NOSTUFF 0 — L9602 90-OHM — TD2M
TMDS_D2P — R9604 332 1% 1/16W MF-LF 402 — R9627 NOSTUFF 0 — TD2P
TMDS_D1M — R9628 NOSTUFF 0 — L9608 90-OHM — TD1M
TMDS_D1P — R9603 332 1% 1/16W MF-LF 402 — R9629 NOSTUFF 0 — TD1P
TMDS_D0M — R9630 NOSTUFF 0 — L9609 90-OHM — TD0M
TMDS_D0P — R9602 332 1% 1/16W MF-LF 402 — R9631 NOSTUFF 0 — TD0P
TMDS_CKM — R9632 NOSTUFF 0 — L9610 90-OHM — TCKM
TMDS_CK_TERM MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM — C9600 22PF 5% 50V CERM 402
TMDS_CKP — R9601 165 1% 1/16W MF-LF 402 — R9633 NOSTUFF 0 — TCKP

PANEL POWER SEQUENCING

=PP3V3_GPU — Q9600 NOSTUFF IRF7410PBF SO-8 — R9634 0 5% 1/4W MF-LF 1206 — =PP3V3_GPU
C9610 NOSTUFF 0.01UF 20% 16V CERM 402
R9625 NOSTUFF 100K 5% 1/16W MF-LF 402
376S0337
C9618 NOSTUFF 0.022UF 20% 16V CERM 402
FPD_PWR_SW_G
R9613 NOSTUFF 10K 5% 1/16W MF-LF 402 — FPD_PWR_ON_D
Q9601 NOSTUFF 2N7002 SOT23-LF — FPD_PWR_ON
D9614 MMBD914XXG SOT23 — TMDS_EN_R
R9614 10K 5% 1/16W MF-LF 402 — TMDS_EN
C9617 10UF 10% 6.3V X5R 805
R9660 NOSTUFF 10K 5% 1/16W MF-LF 402
PPVCC_TMDS
VOLTAGE=3.3V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

=PP3V3_GPU — R9682 0 5% 1/8W MF-LF 805 — PP3V3_DDC
R9605 2.0K 5% 1/16W MF-LF 402 — I2C_GPU_TMDS_SCL
R9607 2.0K 5% 1/16W MF-LF 402
C9601 0.01UF 10% 16V CERM 402
R9608 33 5% 1/16W MF-LF 402 — I2C_TMDS_SCL
R9606 33 5% 1/16W MF-LF 402 — I2C_GPU_TMDS_SDA — I2C_TMDS_SDA

INTERNAL TMDS CONNECTOR

SDF9600 STDOFF-3MMOD4.6MMH-1.35-TH — GND_CHASSIS_TMDS0
(516S0241) CRITICAL
C9620 0.01UF 10% 16V CERM 402
J9602 53307-3072 F-ST-SM
PPVCC_TMDS
PP3V3_DDC VOLTAGE=3.3V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM
TD0M TD0P TD2M TD2P I2C_TMDS_SDA
TCKM TCKP TD1M TD1P I2C_TMDS_SCL
C9616 10UF 10% 6.3V X5R 805
C9615 0.01UF 10% 16V CERM 402
SDF9601 STDOFF-3MMOD4.6MMH-1.35-TH — GND_CHASSIS_TMDS1
C9621 0.01UF 10% 16V CERM 402

U9670 74LC125 — FPD_PWR_ON — LED5900_PWR
R9612 820 5% 1/10W MF-LF 603 — LED5900_P1
LED9600 GREEN-3.6MCD 2.0X1.25MM-SM
SILKSCREEN: 3

INVERTER INTERFACE

=PP12V_GPU — C9642 4.7UF 20% 6.3V CERM 805 — CRITICAL J9601 87437-0443-BLK M-ST-SM
LCD_PWM
INV_CUR_HI
518S0331

EXTERNAL VGA CONNECTOR

	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	
FILT_ANALOG_GRN	GPU_VGA	GPU_VGA	J914
ANALOG_GRN_LC	GPU_VGA	GPU_VGA	J971
ANALOG_GRN_LCL	GPU_VGA	GPU_VGA	J972
FILT_ANALOG_RED	GPU_VGA	GPU_VGA	J916
ANALOG_RED_LC	GPU_VGA	GPU_VGA	J973
ANALOG_RED_LCL	GPU_VGA	GPU_VGA	J974
FILT_ANALOG_BLU	GPU_VGA	GPU_VGA	J915
ANALOG_BLU_LC	GPU_VGA	GPU_VGA	J975
ANALOG_BLU_LCL	GPU_VGA	GPU_VGA	J976
VGA_VSYNC	GPU_VGA	GPU_VGA	J920
VGA_VSYNC_R	GPU_VGA	GPU_VGA	J921
VGA_HSYNC	GPU_VGA	GPU_VGA	J923
VGA_HSYNC_R	GPU_VGA	GPU_VGA	J922

PP5V_USB2 — R9680 0 5% 1/8W MF-LF 805 — PP5V_VGA VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C9602 0.01UF 10% 16V CERM 402 — GND_CHASSIS_VGA

=PP3V3_GPU — C9670 0.1UF 20% 10V CERM 402
U9670 CRITICAL 74LC125 TSSOP
ANALOG_VSYNC — R9671 33 5% 1/16W MF-LF 402 — VGA_VSYNC — VGA_VSYNC_R
U9670 74LC125 TSSOP
ANALOG_HSYNC — R9672 33 5% 1/16W MF-LF 402 — VGA_HSYNC — VGA_HSYNC_R
C9607 NOSTUFF 22PF 5% 50V CERM 402
C9608 NOSTUFF 22PF 5% 50V CERM 402 — GND_CHASSIS_VGA

=PP3V3_GPU — R9673 10K 5% 1/16W MF-LF 402 — R9674 10K 5% 1/16W MF-LF 402
Q9675 2N7002DW-X-F SOT-363
I2C_GPU_MON_SCL — R9675 100 5% 1/16W MF-LF 402 — I2C_MON_SCL_R
Q9675 2N7002DW-X-F SOT-363
I2C_GPU_MON_SDA — R9676 100 5% 1/16W MF-LF 402 — I2C_MON_SDA_R
PP5V_VGA — R9677 4.7K 5% 1/16W MF-LF 402 — R9678 4.7K 5% 1/16W MF-LF 402
C9677 47PF 5% 50V CERM 402
C9678 47PF 5% 50V CERM 402 — GND_CHASSIS_VGA

INDUCTORS SHOULD BE 47 NH
ANY ~8PF CAP SHOULD DO

ANALOG_RED — L9640 47NH-0.20-OHM 0805 — ANALOG_RED_LC — L9641 47NH-0.20-OHM 0805
C9640 8.2PF +/-0.25PF 50V CERM 402
NOSTUFF FL9600 LCFILTER SM-220MHZ-LF — R9640 0 — ANALOG_RED_LCL
R9643 301 1% 1/10W MF-LF 402

ANALOG_GRN — L9642 47NH-0.20-OHM 0805 — ANALOG_GRN_LC — L9643 47NH-0.20-OHM 0805
C9643 8.2PF +/-0.25PF 50V CERM 402
NOSTUFF FL9601 LCFILTER SM-220MHZ-LF — R9641 0 — ANALOG_GRN_LCL
R9644 301 1% 1/10W MF-LF 402

ANALOG_BLU — L9644 47NH-0.20-OHM 0805 — ANALOG_BLU_LC — L9645 47NH-0.20-OHM 0805
C9644 8.2PF +/-0.25PF 50V CERM 402
NOSTUFF FL9602 LCFILTER SM-220MHZ-LF — R9642 0 — ANALOG_BLU_LCL
R9645 301 1% 1/10W MF-LF 402

PLACE R9321-3 & FL9600-2 CLOSE TO J9603

M23: 514S0089

CRITICAL J9603 MINI-VGA F-ST-SM
NC — PIN 15 NC REQUESTED BY EMC
VGA_HSYNC_R — VGA_VSYNC_R
FILT_ANALOG_RED — (RED_RTN)
FILT_ANALOG_GRN — (GRN_RTN)
FILT_ANALOG_BLU — PP5V_VGA
I2C_MON_SCL_R — I2C_MON_SDA_R
MON_DETECT — (BLU_RTN)
C9605 0.01UF 10% 16V CERM 402
C9604 0.01UF 10% 16V CERM 402
C9603 0.01UF 10% 16V CERM 402
GND_CHASSIS_VGA

TMDS/Inverter/ExtVGA

SYNC_MASTER=M23-DD SYNC_DATE=06/20/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 96 OF 154	

KODIAK PCI-E PHYSICAL CONSTRAINT TABLE

SIG_NAME	ELECTRICAL_CONSTRAINT_SET	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE	NET_SPACING_TYPE
100M_N<0>		CLK_100M	PCIE_CLK	PCIE_CLK
100M_P<0>		CLK_100M	PCIE_CLK	PCIE_CLK
CLK_KOD_100M_N<0>		CLK_KODPCIE_100M	PCIE_CLK	PCIE_CLK
CLK_KOD_100M_P<0>		CLK_KODPCIE_100M	PCIE_CLK	PCIE_CLK
CLK_KOD_100M_NF<0>		CLK_KODPCIE_100MF	PCIE_CLK	PCIE_CLK
CLK_KOD_100M_PF<0>		CLK_KODPCIE_100MF	PCIE_CLK	PCIE_CLK
PCIE_NB_TO_SLOTA_NF<0>	PCIE_NB2SA0	PCIE_NB_TO_SLOTA_0_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<0>	PCIE_NB2SA0	PCIE_NB_TO_SLOTA_0_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<1>	PCIE_NB2SA1	PCIE_NB_TO_SLOTA_1_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<1>	PCIE_NB2SA1	PCIE_NB_TO_SLOTA_1_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<2>	PCIE_NB2SA2	PCIE_NB_TO_SLOTA_2_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<2>	PCIE_NB2SA2	PCIE_NB_TO_SLOTA_2_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<3>	PCIE_NB2SA3	PCIE_NB_TO_SLOTA_3_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<3>	PCIE_NB2SA3	PCIE_NB_TO_SLOTA_3_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<4>	PCIE_NB2SA4	PCIE_NB_TO_SLOTA_4_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<4>	PCIE_NB2SA4	PCIE_NB_TO_SLOTA_4_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<5>	PCIE_NB2SA5	PCIE_NB_TO_SLOTA_5_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<5>	PCIE_NB2SA5	PCIE_NB_TO_SLOTA_5_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<6>	PCIE_NB2SA6	PCIE_NB_TO_SLOTA_6_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<6>	PCIE_NB2SA6	PCIE_NB_TO_SLOTA_6_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<7>	PCIE_NB2SA7	PCIE_NB_TO_SLOTA_7_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<7>	PCIE_NB2SA7	PCIE_NB_TO_SLOTA_7_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<8>	PCIE_NB2SA8	PCIE_NB_TO_SLOTA_8_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<8>	PCIE_NB2SA8	PCIE_NB_TO_SLOTA_8_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<9>	PCIE_NB2SA9	PCIE_NB_TO_SLOTA_9_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<9>	PCIE_NB2SA9	PCIE_NB_TO_SLOTA_9_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<10>	PCIE_NB2SA10	PCIE_NB_TO_SLOTA_10_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<10>	PCIE_NB2SA10	PCIE_NB_TO_SLOTA_10_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<11>	PCIE_NB2SA11	PCIE_NB_TO_SLOTA_11_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<11>	PCIE_NB2SA11	PCIE_NB_TO_SLOTA_11_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<12>	PCIE_NB2SA12	PCIE_NB_TO_SLOTA_12_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<12>	PCIE_NB2SA12	PCIE_NB_TO_SLOTA_12_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<13>	PCIE_NB2SA13	PCIE_NB_TO_SLOTA_13_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<13>	PCIE_NB2SA13	PCIE_NB_TO_SLOTA_13_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<14>	PCIE_NB2SA14	PCIE_NB_TO_SLOTA_14_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<14>	PCIE_NB2SA14	PCIE_NB_TO_SLOTA_14_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<15>	PCIE_NB2SA15	PCIE_NB_TO_SLOTA_15_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<15>	PCIE_NB2SA15	PCIE_NB_TO_SLOTA_15_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<0>		PCIE_NB_TO_SLOTA_0	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<0>		PCIE_NB_TO_SLOTA_0	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<1>		PCIE_NB_TO_SLOTA_1	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<1>		PCIE_NB_TO_SLOTA_1	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<2>		PCIE_NB_TO_SLOTA_2	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<2>		PCIE_NB_TO_SLOTA_2	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<3>		PCIE_NB_TO_SLOTA_3	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<3>		PCIE_NB_TO_SLOTA_3	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<4>		PCIE_NB_TO_SLOTA_4	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<4>		PCIE_NB_TO_SLOTA_4	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<5>		PCIE_NB_TO_SLOTA_5	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<5>		PCIE_NB_TO_SLOTA_5	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<6>		PCIE_NB_TO_SLOTA_6	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<6>		PCIE_NB_TO_SLOTA_6	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<7>		PCIE_NB_TO_SLOTA_7	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<7>		PCIE_NB_TO_SLOTA_7	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<8>		PCIE_NB_TO_SLOTA_8	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<8>		PCIE_NB_TO_SLOTA_8	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<9>		PCIE_NB_TO_SLOTA_9	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<9>		PCIE_NB_TO_SLOTA_9	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<10>		PCIE_NB_TO_SLOTA_10	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<10>		PCIE_NB_TO_SLOTA_10	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<11>		PCIE_NB_TO_SLOTA_11	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<11>		PCIE_NB_TO_SLOTA_11	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<12>		PCIE_NB_TO_SLOTA_12	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<12>		PCIE_NB_TO_SLOTA_12	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<13>		PCIE_NB_TO_SLOTA_13	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<13>		PCIE_NB_TO_SLOTA_13	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<14>		PCIE_NB_TO_SLOTA_14	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<14>		PCIE_NB_TO_SLOTA_14	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<15>		PCIE_NB_TO_SLOTA_15	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<15>		PCIE_NB_TO_SLOTA_15	PCIE_DATA	PCIE_DATA

SIG_NAME	ELECTRICAL_CONSTRAINT_SET	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE	NET_SPACING_TYPE
CLK_PCIE_SLOTA_N<0>		KODPCIE_CLK	PCIE_CLK	PCIE_CLK
CLK_PCIE_SLOTA_P<0>		KODPCIE_CLK	PCIE_CLK	PCIE_CLK
CLK_PCIE_SLOTA_NF<0>		KODPCIE_CLKF	PCIE_CLK	PCIE_CLK
CLK_PCIE_SLOTA_PF<0>		KODPCIE_CLKF	PCIE_CLK	PCIE_CLK
CKA_P<0>		CLK_SLOTA_CKA	PCIE_CLK	PCIE_CLK
CKA_N<0>		CLK_SLOTA_CKA	PCIE_CLK	PCIE_CLK
PCIE_SLOTA_TO_NB_NF<0>	PCIE_SA2NB0	PCIE_SLOTA_TO_NB_0_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<0>	PCIE_SA2NB0	PCIE_SLOTA_TO_NB_0_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<1>	PCIE_SA2NB1	PCIE_SLOTA_TO_NB_1_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<1>	PCIE_SA2NB1	PCIE_SLOTA_TO_NB_1_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<2>	PCIE_SA2NB2	PCIE_SLOTA_TO_NB_2_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<2>	PCIE_SA2NB2	PCIE_SLOTA_TO_NB_2_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<3>	PCIE_SA2NB3	PCIE_SLOTA_TO_NB_3_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<3>	PCIE_SA2NB3	PCIE_SLOTA_TO_NB_3_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<4>	PCIE_SA2NB4	PCIE_SLOTA_TO_NB_4_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<4>	PCIE_SA2NB4	PCIE_SLOTA_TO_NB_4_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<5>	PCIE_SA2NB5	PCIE_SLOTA_TO_NB_5_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<5>	PCIE_SA2NB5	PCIE_SLOTA_TO_NB_5_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<6>	PCIE_SA2NB6	PCIE_SLOTA_TO_NB_6_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<6>	PCIE_SA2NB6	PCIE_SLOTA_TO_NB_6_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<7>	PCIE_SA2NB7	PCIE_SLOTA_TO_NB_7_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<7>	PCIE_SA2NB7	PCIE_SLOTA_TO_NB_7_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<8>	PCIE_SA2NB8	PCIE_SLOTA_TO_NB_8_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<8>	PCIE_SA2NB8	PCIE_SLOTA_TO_NB_8_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<9>	PCIE_SA2NB9	PCIE_SLOTA_TO_NB_9_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<9>	PCIE_SA2NB9	PCIE_SLOTA_TO_NB_9_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<10>	PCIE_SA2NB10	PCIE_SLOTA_TO_NB_10_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<10>	PCIE_SA2NB10	PCIE_SLOTA_TO_NB_10_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<11>	PCIE_SA2NB11	PCIE_SLOTA_TO_NB_11_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<11>	PCIE_SA2NB11	PCIE_SLOTA_TO_NB_11_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<12>	PCIE_SA2NB12	PCIE_SLOTA_TO_NB_12_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<12>	PCIE_SA2NB12	PCIE_SLOTA_TO_NB_12_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<13>	PCIE_SA2NB13	PCIE_SLOTA_TO_NB_13_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<13>	PCIE_SA2NB13	PCIE_SLOTA_TO_NB_13_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<14>	PCIE_SA2NB14	PCIE_SLOTA_TO_NB_14_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<14>	PCIE_SA2NB14	PCIE_SLOTA_TO_NB_14_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<15>	PCIE_SA2NB15	PCIE_SLOTA_TO_NB_15_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<15>	PCIE_SA2NB15	PCIE_SLOTA_TO_NB_15_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<0>		PCIE_SLOTA_TO_NB_0	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<0>		PCIE_SLOTA_TO_NB_0	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<1>		PCIE_SLOTA_TO_NB_1	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<1>		PCIE_SLOTA_TO_NB_1	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<2>		PCIE_SLOTA_TO_NB_2	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<2>		PCIE_SLOTA_TO_NB_2	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<3>		PCIE_SLOTA_TO_NB_3	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<3>		PCIE_SLOTA_TO_NB_3	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<4>		PCIE_SLOTA_TO_NB_4	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<4>		PCIE_SLOTA_TO_NB_4	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<5>		PCIE_SLOTA_TO_NB_5	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<5>		PCIE_SLOTA_TO_NB_5	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<6>		PCIE_SLOTA_TO_NB_6	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<6>		PCIE_SLOTA_TO_NB_6	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<7>		PCIE_SLOTA_TO_NB_7	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<7>		PCIE_SLOTA_TO_NB_7	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<8>		PCIE_SLOTA_TO_NB_8	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<8>		PCIE_SLOTA_TO_NB_8	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<9>		PCIE_SLOTA_TO_NB_9	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<9>		PCIE_SLOTA_TO_NB_9	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<10>		PCIE_SLOTA_TO_NB_10	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<10>		PCIE_SLOTA_TO_NB_10	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<11>		PCIE_SLOTA_TO_NB_11	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<11>		PCIE_SLOTA_TO_NB_11	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<12>		PCIE_SLOTA_TO_NB_12	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<12>		PCIE_SLOTA_TO_NB_12	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<13>		PCIE_SLOTA_TO_NB_13	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<13>		PCIE_SLOTA_TO_NB_13	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<14>		PCIE_SLOTA_TO_NB_14	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<14>		PCIE_SLOTA_TO_NB_14	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<15>		PCIE_SLOTA_TO_NB_15	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<15>		PCIE_SLOTA_TO_NB_15	PCIE_DATA	PCIE_DATA

KODIAK PCI-E POWER PHYSICAL CONSTRAINT TABLE

SIG_NAME	MIN_LINE_WIDTH	MIN_NECK_WIDTH	VOLTAGE
KOD_G10_GND	0.3MM	0.25MM	0
KOD_H05_GND	0.3MM	0.25MM	0
KOD_H08_GND	0.3MM	0.25MM	0
KOD_J13_GND	0.3MM	0.25MM	0
KOD_K07_GND	0.3MM	0.25MM	0
KOD_L13_GND	0.3MM	0.25MM	0
PWR_PCIE_A_AVDD	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_2	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_1	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_0	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_A	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_B	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_C	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_2	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_0	0.3MM	0.25MM	1.2

KODIAK PCI-E CONST

SYNC_MASTER=FINO-DD SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E

SCALE	SHT	OF
NONE	97	154

KODIAK HT DECOUPLING
(LOCATE CLOSE TO PINS AS INDICATED)

=PPVCORE_PWRON_NB_HT 7 98

C9806 1UF 10% 6.3V CERM 402
C9807 1UF 10% 6.3V CERM 402
C9808 1UF 10% 6.3V CERM 402
C9809 1UF 10% 6.3V CERM 402
C9810 1UF 10% 6.3V CERM 402
C9811 1UF 10% 6.3V CERM 402
C9812 1UF 10% 6.3V CERM 402
C9813 1UF 10% 6.3V CERM 402
C9814 1UF 10% 6.3V CERM 402
C9815 1UF 10% 6.3V CERM 402

PLANE-SPLIT AC RETURN PATHS
LOCATE EACH CAPACITOR SO THAT
THEY STRADDLE EACH PLANE SPLIT

98 7 =PPVCORE_PWRON_NB_HT — C9834 0.1UF 20% 16V CERM 402 — =PP1V2_PWRON_HT_NBTX 7 98

KODIAK CORES

PP9806 P4MM SM
1.6V
Q63 = PP1V6

98 7 =PP2V5_PWRON_NB_HT — L9800 0.22UH 0805-1 — PWR_HT_AVDD

C9800 0.01UF 10% 16V CERM 402
C9801 10UF 10% 6.3V X5R 805
C9802 1UF 10% 6.3V CERM 402

101 98 6 KOD_L15_GND (THIS PAGE)

98 7 =PPVCORE_PWRON_NB_HT

PP9807 P4MM SM
1.2V
Q63 = PP1V2

=PP1V2_PWRON_HT_NBTX 7 98

L9801 0.22UH 0805-1

101 PWR_HT_AVDD2

C9803 1UF 10% 6.3V CERM 402
C9804 10UF 10% 6.3V X5R 805
C9805 0.01UF 10% 16V CERM 402

=PP2V5_PWRON_NB_HT 7 98

KOD_L15_GND 6 98 101 (THIS PAGE)

98 7 =PP1V2_PWRON_HT_NBTX

C9817 1UF 10% 6.3V CERM 402
C9818 1UF 10% 6.3V CERM 402
C9819 1UF 10% 6.3V CERM 402
C9820 1UF 10% 6.3V CERM 402
C9821 1UF 10% 6.3V CERM 402
C9822 1UF 10% 6.3V CERM 402
C9823 1UF 10% 6.3V CERM 402
C9824 1UF 10% 6.3V CERM 402
C9825 1UF 10% 6.3V CERM 402
C9826 1UF 10% 6.3V CERM 402

KODIAK HT DECOUPLING
(LOCATE CLOSE TO PINS AS INDICATED)
(CAPACITORS ARE DOUBLED-UP WHERE POSSIBL;E)

98 7 =PP1V2_PWRON_HT_NBTX

C9827 1UF 10% 6.3V CERM 402
C9828 1UF 10% 6.3V CERM 402
C9829 1UF 10% 6.3V CERM 402
C9830 1UF 10% 6.3V CERM 402
C9831 1UF 10% 6.3V CERM 402
C9832 1UF 10% 6.3V CERM 402
C9833 1UF 10% 6.3V CERM 402
C9839 1UF 10% 6.3V CERM 402
C9840 1UF 10% 6.3V CERM 402
C9841 1UF 10% 6.3V CERM 402
C9842 1UF 10% 6.3V CERM 402
C9843 1UF 10% 6.3V CERM 402
C9844 1UF 10% 6.3V CERM 402
C9845 1UF 10% 6.3V CERM 402
C9846 1UF 10% 6.3V CERM 402
C9847 1UF 10% 6.3V CERM 402

98 7 =PP1V2_PWRON_HT_NBTX

PP9808 P4MM SM
HTM2NC0-
HTM2NC0+
PP9809 P4MM SM

HT_REFCLK_AVDD
(1.65V-2.75V)
(1.6V-1.2V)

K15

HT_CLK_RXN0 E25
HT_CLK_RXP0 D25
HT_CTL_RXN0 J27
HT_CTL_RXP0 K27
HT_CAD_RXN0 F26
HT_CAD_RXP0 F27
HT_CAD_RXN1 F25
HT_CAD_RXP1 F24
HT_CAD_RXN2 A25
HT_CAD_RXP2 B25
HT_CAD_RXN3 G25
HT_CAD_RXP3 H25
HT_CAD_RXN4 L25
HT_CAD_RXP4 K25
HT_CAD_RXN5 G27
HT_CAD_RXP5 H27
HT_CAD_RXN6 J25
HT_CAD_RXP6 J26
HT_CAD_RXN7 C26
HT_CAD_RXP7 C27
HT_CLK_RXN1 F22
HT_CLK_RXP1 F23
HT_CTL_RXP1 E21
HT_CTL_RXN1 D21
HT_CAD_RXN8 E23
HT_CAD_RXP8 D23
HT_CAD_RXN9 A23
HT_CAD_RXP9 B23
HT_CAD_RXN10 H23
HT_CAD_RXP10 G23
HT_CAD_RXN11 C22
HT_CAD_RXP11 C23
HT_CAD_RXN12 K23
HT_CAD_RXP12 L23
HT_CAD_RXN13 J23
HT_CAD_RXP13 J24
HT_CAD_RXN14 A21
HT_CAD_RXP14 B21
HT_CAD_RXN15 C24
HT_CAD_RXP15 C25
HT_PVTREF0 K19
HT_PVTREF1 L19
HT_PVTREF2_ALT L17
HT_PVTREF3_ALT K17
HT_REFCLK_N J16
HT_REFCLK_P J15
(200MHZ)

HT_RX_VDD A24 B22 B26 D24 E22 E26 G24 H26 K24 L22

HT_REFCLK_AGND

L15

HT_RX_GND A22 A26 B24 D22 D26 E24 G26 H24 K22 L24

HT_REFCLK_AVDD2
(1.65V-2.75V)
(1.6V-1.2V)

H15

HT_VD4 A16 A20 B14 B18 D16 D20 E18 G16 G20 H18 H22 K16 K20 L18 M17 M21 N19

HT_VD4_GND A14 A18 B16 B20 D18 E16 E20 G18 G22 H16 H20 K18 L16 L20 M16 M20 N18

HT_LDTSTOP_L AF06
HT_LDTREQ_L AF09
HT_PWROK AF03
HT_RESET_L AE11

HT_CLK_TXN0 J19
HT_CLK_TXP0 J20
HT_CTL_TXN0 J22
HT_CTL_TXP0 J21
HT_CAD_TXN0 F16
HT_CAD_TXP0 F17
HT_CAD_TXN1 G17
HT_CAD_TXP1 H17
HT_CAD_TXN2 J18
HT_CAD_TXP2 J17
HT_CAD_TXN3 F18
HT_CAD_TXP3 F19
HT_CAD_TXN4 G19
HT_CAD_TXP4 H19
HT_CAD_TXN5 G21
HT_CAD_TXP5 H21
HT_CAD_TXN6 F21
HT_CAD_TXP6 F20
HT_CAD_TXN7 K21
HT_CAD_TXP7 L21
HT_CLK_TXN1 C16
HT_CLK_TXP1 C17
HT_CTL_TXP1 E15
HT_CTL_TXN1 D15
HT_CAD_TXN8 D19
HT_CAD_TXP8 E19
HT_CAD_TXN9 D17
HT_CAD_TXP9 E17
HT_CAD_TXN10 C19
HT_CAD_TXP10 C18
HT_CAD_TXN11 A15
HT_CAD_TXP11 B15
HT_CAD_TXN12 A17
HT_CAD_TXP12 B17
HT_CAD_TXN13 B19
HT_CAD_TXP13 A19
HT_CAD_TXN14 C15
HT_CAD_TXP14 C14
HT_CAD_TXN15 C20
HT_CAD_TXP15 C21

HT_NB_TO_MB_CLK_N<0> 101
HT_NB_TO_MB_CLK_P<0> 101
HT_NB_TO_MB_CTL_N<0> 101
HT_NB_TO_MB_CTL_P<0> 101
HT_NB_TO_MB_CAD_N<0> 101
HT_NB_TO_MB_CAD_P<0> 101
HT_NB_TO_MB_CAD_N<1> 101
HT_NB_TO_MB_CAD_P<1> 101
HT_NB_TO_MB_CAD_N<2> 101
HT_NB_TO_MB_CAD_P<2> 101
HT_NB_TO_MB_CAD_N<3> 101
HT_NB_TO_MB_CAD_P<3> 101
HT_NB_TO_MB_CAD_N<4> 101
HT_NB_TO_MB_CAD_P<4> 101
HT_NB_TO_MB_CAD_N<5> 101
HT_NB_TO_MB_CAD_P<5> 101
HT_NB_TO_MB_CAD_N<6> 101
HT_NB_TO_MB_CAD_P<6> 101
HT_NB_TO_MB_CAD_N<7> 101
HT_NB_TO_MB_CAD_P<7> 101
HT_NB_TO_MB_CLK_N<1> 101
HT_NB_TO_MB_CLK_P<1> 101
9 HT_NB_TO_MB_CTL_P<1>
9 HT_NB_TO_MB_CTL_N<1>
HT_NB_TO_MB_CAD_N<8> 101
HT_NB_TO_MB_CAD_P<8> 101
HT_NB_TO_MB_CAD_N<9> 101
HT_NB_TO_MB_CAD_P<9> 101
HT_NB_TO_MB_CAD_N<10> 101
HT_NB_TO_MB_CAD_P<10> 101
HT_NB_TO_MB_CAD_N<11> 101
HT_NB_TO_MB_CAD_P<11> 101
HT_NB_TO_MB_CAD_N<12> 101
HT_NB_TO_MB_CAD_P<12> 101
HT_NB_TO_MB_CAD_N<13> 101
HT_NB_TO_MB_CAD_P<13> 101
HT_NB_TO_MB_CAD_N<14> 101
HT_NB_TO_MB_CAD_P<14> 101
HT_NB_TO_MB_CAD_N<15> 101
HT_NB_TO_MB_CAD_P<15> 101
HT_LDTSTOP_L 103
HT_LDTREQ_L 103
HT_PWROK 103
HT_LDTRESET_L 103

=PP1V2_PWRON_HT_NBTX 7 98
NOSTUFF R9808 8.2K 5% 1/16W MF-LF 402 2

=PP1V2_PWRON_HT_NBTX 7 98
NOSTUFF R9809 8.2K 5% 1/16W MF-LF 402 2

=PP2V5_PWRON_HT 7 103
R9810 1K 5% 1/16W MF-LF 402
R9811 1K 5% 1/16W MF-LF 402
R9812 1K 5% 1/16W MF-LF 402
R9813 1K 5% 1/16W MF-LF 402

U1900
KODIAK-ASIC-040812
HT X16 INTERFACE
BGA
(6 OF 10)
SEE_TABLE

KODIAK HT RECEIVE CLOCKS

PP9802 P4MM SM
MHT1-
MHT1+
PP9803 P4MM SM

R9806 8.2K 5% 1/16W MF-LF 402 2

HT_MB_TO_NB_CLK_N<1> 101
HT_MB_TO_NB_CLK_P<1> 101

R9807 8.2K 5% 1/16W MF-LF 402 2

HT_MB_TO_NB_CTL_N<1> 9
HT_MB_TO_NB_CTL_P<1> 9

KODIAK HT REFCLK TERMINATION
(LOCATE CLOSE TO INPUT PINS)

HT_NB_REFCLK_P<0> 101 26

R9800 100 1% 1/16W MF-LF 402 2
R9801 200 1% 1/16W MF-LF 402 2

KOD_PVTREF0 K19
KOD_PVTREF1 L19
KOD_PVTREF2_ALT L17
KOD_PVTREF3_ALT K17

R9802 20.5 1% 1/16W MF-LF 402
R9803 29.4 1% 1/16W MF-LF 402
R9804 29.4 1% 1/16W MF-LF 402
R9805 20.5 1% 1/16W MF-LF 402

C9837 0.01UF 10% 16V CERM 402
C9838 0.01UF 10% 16V CERM 402

HT_NB_P<0> 101
HT_NB_N<0> 101

NOSTUFF C9836 0.01UF 10% 16V CERM 402
HT_NB_G 101

HT_NB_REFCLK_N<0> 101 26

HT_NB_REFCLK_PF<0> 101 9
HT_NB_REFCLK_NF<0> 101 9

PP9804 P4MM SM
HREF0-
HREF0+
PP9805 P4MM SM

KODIAK HT REFCLK

101 98 6 KOD_L15_GND (THIS PAGE)

XW9800 SM

PAGE 98

KODIAK HT16

SYNC_MASTER=Q63 SYNC_DATE=08/01/2005

NOTICE OF PROPRIETARY PROPERTY

LAST_MODIFIED=Tue Nov 1 14:56:40 2005

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE	SHT	OF
NONE	98	154

DRAWING

SIG_NAME	MAKE_BASE	DIFFERENTIAL_PAIR	EC_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	
HT_NB_TO_MB_CLK_N<0>	TRUE	HT_NB_TO_SB_CLK	HT_NB_TO_SB_PP	HT_CAD	HT_NB_TO_SB_CLK	HT_MB_TO_SB_CLK_N<0>
HT_NB_TO_MB_CLK_P<0>	TRUE	HT_NB_TO_SB_CLK	HT_NB_TO_SB_PP	HT_CAD	HT_NB_TO_SB_CLK	HT_MB_TO_SB_CLK_P<0>
HT_NB_TO_MB_CAD_N<0>	TRUE	HT_NB_TO_SB_CAD0	HT_NB_TO_SB_PP	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_N<0>
HT_NB_TO_MB_CAD_P<0>	TRUE	HT_NB_TO_SB_CAD0	HT_NB_TO_SB_PP	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_P<0>
HT_NB_TO_MB_CAD_N<1>	TRUE	HT_NB_TO_SB_CAD1	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_N<1>
HT_NB_TO_MB_CAD_P<1>	TRUE	HT_NB_TO_SB_CAD1	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_P<1>
HT_NB_TO_MB_CAD_N<2>	TRUE	HT_NB_TO_SB_CAD2	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_N<2>
HT_NB_TO_MB_CAD_P<2>	TRUE	HT_NB_TO_SB_CAD2	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_P<2>
HT_NB_TO_MB_CAD_N<3>	TRUE	HT_NB_TO_SB_CAD3	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_N<3>
HT_NB_TO_MB_CAD_P<3>	TRUE	HT_NB_TO_SB_CAD3	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_P<3>
HT_NB_TO_MB_CAD_N<4>	TRUE	HT_NB_TO_SB_CAD4	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_N<4>
HT_NB_TO_MB_CAD_P<4>	TRUE	HT_NB_TO_SB_CAD4	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_P<4>
HT_NB_TO_MB_CAD_N<5>	TRUE	HT_NB_TO_SB_CAD5	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_N<5>
HT_NB_TO_MB_CAD_P<5>	TRUE	HT_NB_TO_SB_CAD5	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_P<5>
HT_NB_TO_MB_CAD_N<6>	TRUE	HT_NB_TO_SB_CAD6	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_N<6>
HT_NB_TO_MB_CAD_P<6>	TRUE	HT_NB_TO_SB_CAD6	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_P<6>
HT_NB_TO_MB_CAD_N<7>	TRUE	HT_NB_TO_SB_CAD7	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_N<7>
HT_NB_TO_MB_CAD_P<7>	TRUE	HT_NB_TO_SB_CAD7	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_P<7>
HT_NB_TO_MB_CTL_N<0>	TRUE	HT_NB_TO_SB_CTL0	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CTL_N<0>
HT_NB_TO_MB_CTL_P<0>	TRUE	HT_NB_TO_SB_CTL0	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CTL_P<0>
HT_MB_TO_NB_CLK_N<0>	TRUE	HT_SB_TO_NB_CLK	HT_SB_TO_NB_PP	HT_CAD	HT_SB_TO_NB_CLK	HT_SB_TO_MB_CLK_N<0>
HT_MB_TO_NB_CLK_P<0>	TRUE	HT_SB_TO_NB_CLK	HT_SB_TO_NB_PP	HT_CAD	HT_SB_TO_NB_CLK	HT_SB_TO_MB_CLK_P<0>
HT_MB_TO_NB_CAD_N<0>	TRUE	HT_SB_TO_NB_CAD0	HT_SB_TO_NB_PP	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_N<0>
HT_MB_TO_NB_CAD_P<0>	TRUE	HT_SB_TO_NB_CAD0	HT_SB_TO_NB_PP	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_P<0>
HT_MB_TO_NB_CAD_N<1>	TRUE	HT_SB_TO_NB_CAD1	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_N<1>
HT_MB_TO_NB_CAD_P<1>	TRUE	HT_SB_TO_NB_CAD1	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_P<1>
HT_MB_TO_NB_CAD_N<2>	TRUE	HT_SB_TO_NB_CAD2	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_N<2>
HT_MB_TO_NB_CAD_P<2>	TRUE	HT_SB_TO_NB_CAD2	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_P<2>
HT_MB_TO_NB_CAD_N<3>	TRUE	HT_SB_TO_NB_CAD3	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_N<3>
HT_MB_TO_NB_CAD_P<3>	TRUE	HT_SB_TO_NB_CAD3	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_P<3>
HT_MB_TO_NB_CAD_N<4>	TRUE	HT_SB_TO_NB_CAD4	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_N<4>
HT_MB_TO_NB_CAD_P<4>	TRUE	HT_SB_TO_NB_CAD4	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_P<4>
HT_MB_TO_NB_CAD_N<5>	TRUE	HT_SB_TO_NB_CAD5	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_N<5>
HT_MB_TO_NB_CAD_P<5>	TRUE	HT_SB_TO_NB_CAD5	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_P<5>
HT_MB_TO_NB_CAD_N<6>	TRUE	HT_SB_TO_NB_CAD6	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_N<6>
HT_MB_TO_NB_CAD_P<6>	TRUE	HT_SB_TO_NB_CAD6	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_P<6>
HT_MB_TO_NB_CAD_N<7>	TRUE	HT_SB_TO_NB_CAD7	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_N<7>
HT_MB_TO_NB_CAD_P<7>	TRUE	HT_SB_TO_NB_CAD7	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_P<7>
HT_MB_TO_NB_CTL_N<0>	TRUE	HT_SB_TO_NB_CTL0	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CTL_N<0>
HT_MB_TO_NB_CTL_P<0>	TRUE	HT_SB_TO_NB_CTL0	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CTL_P<0>
NC_HT_MB_TO_NB_CAD_P<8..15>	TRUE					HT_MB_TO_NB_CAD_P<8..15>
NC_HT_MB_TO_NB_CAD_N<8..15>	TRUE					HT_MB_TO_NB_CAD_N<8..15>
TP_HT_MB_TO_NB_CLK_N<1>	TRUE					HT_MB_TO_NB_CLK_N<1>
TP_HT_MB_TO_NB_CLK_P<1>	TRUE					HT_MB_TO_NB_CLK_P<1>
NC_HT_NB_TO_MB_CAD_P<8..15>	TRUE					HT_NB_TO_MB_CAD_P<8..15>
NC_HT_NB_TO_MB_CAD_N<8..15>	TRUE					HT_NB_TO_MB_CAD_N<8..15>
NC_HT_NB_TO_MB_CLK_N<1>	TRUE					HT_NB_TO_MB_CLK_N<1>
NC_HT_NB_TO_MB_CLK_P<1>	TRUE					HT_NB_TO_MB_CLK_P<1>
HT_NB_REFCLK_P<0>		HT_NB_REFCLK0	HT_NB_REFCLK	HT_CLK	HT_CLK	IN
HT_NB_REFCLK_N<0>		HT_NB_REFCLK0		HT_CLK	HT_CLK	IN
HT_NB_P<0>		HT_NB0		HT_CLK	HT_CLK	IN
HT_NB_N<0>		HT_NB0		HT_CLK	HT_CLK	IN
HT_NB_REFCLK_PF<0>		HT_NB_REFCLK_F0		HT_CLK	HT_CLK	IN
HT_NB_REFCLK_NF<0>		HT_NB_REFCLK_F0		HT_CLK	HT_CLK	IN

I97

SIG_NAME	MIN_LINE_WIDTH	MIN_NECK_WIDTH	VOLTAGE	
PWR_HT_AVDD	0.4MM	0.2MM	2.5	IN
PWR_HT_AVDD2	0.4MM	0.2MM	2.5	IN
KOD_L15_GND	0.4MM	0.2MM	0	IN
HT_NB_G KEEP DIFF CLOCK FROM BEING A SINGLE XNET			0	IN

HT ALIASES

FINO-ME 06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E

SCALE NONE SHT 101 OF 154

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	0.38mm SPACING	HT_CLK66M_SB_C
HT_CLK66M_SB	0.38mm SPACING	HT_CLK66M_SB
	P3MM SPACING	HT_LDTRESET_L

Page Notes

Power aliases required by this page:
=PP2V5_PWRON_HT
=PP1V2_PWRON_HT

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- SB_HT_200M
  Stuffs resistor to select 200MHz HT I/F.

RA300 3.3 5% 1/8W MF-LF 805 — PP1V2_PWRON_HT_PLLDVDD (MIN_LINE_WIDTH=0.50mm, MIN_NECK_WIDTH=0.38mm)
CA300 10UF 10% 6.3V X5R 805
CA301 1uF 10% 6.3V CERM 402

RA310 3.3 5% 1/8W MF-LF 805 — PP1V2_PWRON_HT_PLLAVDD (MIN_LINE_WIDTH=0.50mm, MIN_NECK_WIDTH=0.38mm)
CA310 10UF 10% 6.3V X5R 805
CA311 1uF 10% 6.3V CERM 402

=PP1V2_PWRON_SB_HT
=PP2V5_PWRON_HT
CA320 0.1uF 20% 10V CERM 402
CA302 10UF 10% 6.3V X5R 805
CA330 0.1uF 20% 10V CERM 402
CA331 0.1uF 20% 10V CERM 402
CA332 0.1uF 20% 10V CERM 402
CA309 10UF 10% 6.3V X5R 805
CA340 0.1uF 20% 10V CERM 402
CA341 0.1uF 20% 10V CERM 402
CA342 0.1uF 20% 10V CERM 402

HTS2MC0+ PPA300 P4MM SM
HTS2MC0- PPA301 P4MM SM
HTS2MC0+ PPA303 P4MM SM
HTS2MC0- PPA304 P4MM SM

U2300 SHASTA V1.1 BGA-LF (3 OF 8) — HYPERTRANSPORT

Pin	HT_PLL / HT_CLKIN	HT_CADIN	HT_CADOUT	HT_CTL / HT_CLKOUT
D15	HT_CLKIN_P			
C15	HT_CLKIN_N			
B10				HT_CLKOUT_P
A10				HT_CLKOUT_N
D17		HT_CADIN_0_P	HT_CADOUT_0_P	
C17		HT_CADIN_0_N	HT_CADOUT_0_N	
B18		HT_CADIN_1_P	HT_CADOUT_1_P	
A18		HT_CADIN_1_N	HT_CADOUT_1_N	
F15		HT_CADIN_2_P	HT_CADOUT_2_P	
E15		HT_CADIN_2_N	HT_CADOUT_2_N	
D16		HT_CADIN_3_P	HT_CADOUT_3_P	
C16		HT_CADIN_3_N	HT_CADOUT_3_N	
B16		HT_CADIN_4_P	HT_CADOUT_4_P	
A16		HT_CADIN_4_N	HT_CADOUT_4_N	
D14		HT_CADIN_5_P	HT_CADOUT_5_P	
C14		HT_CADIN_5_N	HT_CADOUT_5_N	
E14		HT_CADIN_6_P	HT_CADOUT_6_P	
F14		HT_CADIN_6_N	HT_CADOUT_6_N	
B14		HT_CADIN_7_P	HT_CADOUT_7_P	
A14		HT_CADIN_7_N	HT_CADOUT_7_N	
F13				HT_CTLIN_P
E13				HT_CTLIN_N
E16	HT_PWROK_H			
C18	HT_RESET_L			
E17	HT_LDTSTOP_L			
C8	HT_REFCLK			
D8	HT_S100M66M			
V8	SEL_HT00_H			
A19				HT_LDTREQ_L
E10				HT_R100P
F10				HT_R100N

HT_MB_TO_SB_CLK_P<0>, HT_MB_TO_SB_CLK_N<0>
HT_MB_TO_SB_CAD_P<0>, HT_MB_TO_SB_CAD_N<0>
HT_MB_TO_SB_CAD_P<1>, HT_MB_TO_SB_CAD_N<1>
HT_MB_TO_SB_CAD_P<2>, HT_MB_TO_SB_CAD_N<2>
HT_MB_TO_SB_CAD_P<3>, HT_MB_TO_SB_CAD_N<3>
HT_MB_TO_SB_CAD_P<4>, HT_MB_TO_SB_CAD_N<4>
HT_MB_TO_SB_CAD_P<5>, HT_MB_TO_SB_CAD_N<5>
HT_MB_TO_SB_CAD_P<6>, HT_MB_TO_SB_CAD_N<6>
HT_MB_TO_SB_CAD_P<7>, HT_MB_TO_SB_CAD_N<7>
HT_MB_TO_SB_CTL_P<0>, HT_MB_TO_SB_CTL_N<0>
HT_PWROK, HT_LDTRESET_L, HT_LDTSTOP_L

HT_SB_TO_MB_CLK_P<0>, HT_SB_TO_MB_CLK_N<0>
HT_SB_TO_MB_CAD_P<0>, HT_SB_TO_MB_CAD_N<0>
HT_SB_TO_MB_CAD_P<1>, HT_SB_TO_MB_CAD_N<1>
HT_SB_TO_MB_CAD_P<2>, HT_SB_TO_MB_CAD_N<2>
HT_SB_TO_MB_CAD_P<3>, HT_SB_TO_MB_CAD_N<3>
HT_SB_TO_MB_CAD_P<4>, HT_SB_TO_MB_CAD_N<4>
HT_SB_TO_MB_CAD_P<5>, HT_SB_TO_MB_CAD_N<5>
HT_SB_TO_MB_CAD_P<6>, HT_SB_TO_MB_CAD_N<6>
HT_SB_TO_MB_CAD_P<7>, HT_SB_TO_MB_CAD_N<7>
HT_SB_TO_MB_CTL_P<0>, HT_SB_TO_MB_CTL_N<0>

HT_LDTREQ_SB_L → RA301 0 5% 1/10W MF-LF 402 → HT_LDTREQ_L
SB_HT_R100_P, SB_HT_R100_N → RA350 82.5 1% 1/10W MF-LF 402 → CA350 47pF 5% 50V CERM 402, CA351 47pF 5% 50V CERM 402

PPA302 P4MM SM
RA355 0 5% 1/10W MF-LF 402 — HT_CLK66M_SB
SB_HT_S100M66M, SB_SELHT100
1.0V pk-pk

RA352 4.7K 1% 1/10W MF-LF 402 — NOSTUFF — 1 = 100MHz
RA354 10K 5% 1/10W MF-LF 402 — NOSTUFF — 1 = 100MHz
RA353 4.7K 1% 1/10W MF-LF 402 — 0 = 66MHz
RA351 1K 1% 1/10W MF-LF 402 — 0 = 200MHz

HT Refclk	HT I/F Speed
1 = 100MHz	1 = 100MHz
0 = 66MHz	0 = 200MHz

← DETERMINES THE OPERATING FREQUENCY OF HT CORE
1: THE HT SLAVE, HTGS AND THE HT SIDE OF THE PCI BRIDGES OPERATE AT 100 MHZ
0: THE HT SLAVE, HTGS AND THE HT SIDE OF THE PCI BRIDGES OPERATE AT 200 MHZ

Shasta HyperTransport

SYNC_MASTER=Q63 SYNC_DATE=08/01/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT: 103 OF 154	

LAST_MODIFIED=Tue Nov 1 14:55:22 2005

DRAWING
TITLE=K1LOWARA
ASSEMBLY=SRAWING

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
		PCI_AD<31..28> 120 121 122 125
		PCI_AD<27> 120 121 122 125
		PCI_AD<26..24> 120 121 122 125
		PCI_AD<23> 120 121 122
		PCI_AD<22> 120 121 122
		PCI_AD<21> 120 121 122
		PCI_AD<20> 120 121 122 125
		PCI_AD<19..18> 120 121 122 125
		PCI_AD<17> 120 121 122 125
		PCI_AD<16..0> 120 121 122 125
		PCI_CBE_L<3..0> 120 121 122
		PCI_PAR 120 121 122
		PCI_DEVSEL_L 119 120 121 122
		PCI_FRAME_L 119 120 121 122
		PCI_IRDY_L 119 120 121 122
		PCI_TRDY_L 119 120 121 122
		PCI_STOP_L 119 120 121 122
183	P3MM_SPACING	PCI_CLK66M_SB_INT 26 27 119

Page Notes

Power aliases required by this page:
- =PP3V3_PCI
- =PP3V3_SB_PCI (CAN BE _PP3V3_PCI)
- =PP3V3_PWRON_SB
- =PP2V5_PWRON_SB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD11 - PCI0 (0x106B/0x0053)
AD11 - PCI1 (0x106B/0x0054)
AD11 - PCI2 (0x106B/0x0055)

AD23 - KeyLargo (0x106B/0x004F, PCI1)
AD28 - SATA 150 (0x1166/0x0240, PCI0 or 2)
AD29 - UATA 133 (0x106B/0x0050, PCI0 or 2)
AD30 - FireWire (0x106B/0x0052, PCI0 or 2)
AD31 - Ethernet (0x106B/0x0051, PCI0)

Q63 APPLICATION OF POWER NET "=PP3V3_SB_PCI" IS RUN

PPB905 P4MM SM PP
PP_3V3RUNSB_B9
XWB900 3PK
119 7 PP3V3_RUN_SB
CB910 10UF 10% 6.3V X5R 805
CB900 0.1UF 20% 10V CERM 402
CB901 0.1UF 20% 10V CERM 402
CB902 0.1UF 20% 10V CERM 402
CB903 0.1UF 20% 10V CERM 402
CB904 0.1UF 20% 10V CERM 402
NO STUFF
CB911 10UF 10% 6.3V X5R 805
CB905 0.1UF 20% 10V CERM 402
CB906 0.1UF 20% 10V CERM 402
CB907 0.1UF 20% 10V CERM 402
CB908 0.1UF 20% 10V CERM 402
CB909 0.1UF 20% 10V CERM 402

XWB901 3PK
6 PP_2V5PWRONSB_B9
PPB906 P4MM SM PP
=PP2V5_PWRON_SB 7 23 24 138
CB920 0.1UF 20% 10V CERM 402
CB921 0.1UF 20% 10V CERM 402
CB922 0.1UF 20% 10V CERM 402
CB923 0.1UF 20% 10V CERM 402

PPB900 P4MM SM PP
P3MM_SPACING
119 27 26 PCI_CLK66M_SB_INT
PPB901 P4MM SM PP
27 26 PCI_CLK33M_SB_EXT_RR
NOSTUFF CB912 2PF +/-0.25PF 50V C0G 402-1
STUFF NEAR SHASTA

AA22 B22 E21 H16 J21 M16 N21 R20 U21 V19 B20 J18 N20 U20
VDDOPC PCIVDDP
SEE_TABLE
U2300 SHASTA V1.1 BGA-LF (4 OF 8) PCI

"Slot A" - AD17
121 119 PCI_SLOTA_REQ_L AB18 PCI1REQ_0_L
121 119 PCI_SLOTA_GNT_L AA18 PCI1GNT_0_L
"Slot G" - AD27
122 119 PCI_SLOTG_REQ_L AB20 PCI1REQ_1_L
122 119 PCI_SLOTG_GNT_L AB19 PCI1GNT_1_L
"Slot D" - AD20
119 PCI_SLOTD_REQ_L V17 PCI1REQ_2_L
119 PCI_SLOTD_GNT_L V18 PCI1GNT_2_L
125 121 ROM_CS_L AB8 ROMCS_L
125 121 ROM_OE_L AA9 ROMOE_L
125 121 ROM_WE_L Y10 ROMRW_L

PCI1AD_0_H	L18	PCI_SB_AD<0>	120
PCI1AD_1_H	K19	PCI_SB_AD<1>	120
PCI1AD_2_H	L22	PCI_SB_AD<2>	120
PCI1AD_3_H	M22	PCI_SB_AD<3>	120
PCI1AD_4_H	M18	PCI_SB_AD<4>	120
PCI1AD_5_H	L20	PCI_SB_AD<5>	120
PCI1AD_6_H	M21	PCI_SB_AD<6>	120
PCI1AD_7_H	N16	PCI_SB_AD<7>	120
PCI1AD_8_H	M20	PCI_SB_AD<8>	120
PCI1AD_9_H	P22	PCI_SB_AD<9>	120
PCI1AD_10_H	M17	PCI_SB_AD<10>	120
PCI1AD_11_H	N18	PCI_SB_AD<11>	120
PCI1AD_12_H	M19	PCI_SB_AD<12>	120
PCI1AD_13_H	N19	PCI_SB_AD<13>	120
PCI1AD_14_H	P21	PCI_SB_AD<14>	120
PCI1AD_15_H	R22	PCI_SB_AD<15>	120
PCI1AD_16_H	P20	PCI_SB_AD<16>	120
PCI1AD_17_H	V21	PCI_SB_AD<17>	120
PCI1AD_18_H	P18	PCI_SB_AD<18>	120
PCI1AD_19_H	T20	PCI_SB_AD<19>	120
PCI1AD_20_H	R16	PCI_SB_AD<20>	120
PCI1AD_21_H	R17	PCI_SB_AD<21>	120
PCI1AD_22_H	W21	PCI_SB_AD<22>	120
PCI1AD_23_H	V22	PCI_SB_AD<23>	120
PCI1AD_24_H	R18	PCI_SB_AD<24>	120
PCI1AD_25_H	T19	PCI_SB_AD<25>	120
PCI1AD_26_H	T18	PCI_SB_AD<26>	120
PCI1AD_27_H	Y21	PCI_SB_AD<27>	120
PCI1AD_28_H	W20	PCI_SB_AD<28>	120
PCI1AD_29_H	T16	PCI_SB_AD<29>	120
PCI1AD_30_H	AA21	PCI_SB_AD<30>	120
PCI1AD_31_H	T17	PCI_SB_AD<31>	120
PCI1C_BE_0_L	L19	PCI_SB_CBE_L<0>	120
PCI1C_BE_1_L	P16	PCI_SB_CBE_L<1>	120
PCI1C_BE_2_L	V22	PCI_SB_CBE_L<2>	120
PCI1C_BE_3_L	V20	PCI_SB_CBE_L<3>	120
PCI1DEVSEL_L	T22	PCI_SB_DEVSEL_L	120
PCI1FRAME_L	T21	PCI_SB_FRAME_L	120
PCI1IRDY_L	R21	PCI_SB_IRDY_L	120
PCI1TRDY_L	P19	PCI_SB_TRDY_L	120
PCI1STOP_L	P17	PCI_SB_STOP_L	120
PCI1PAR_H	N17	PCI_SB_PAR	120
PCI1RST_L	U18	SB_PCI_RESET_L	

NET_SPACING_TYPE=P3MM SPACING

=PP3V3_PWRON_SB 7 20 23 24 56
RB955 4.7K 1% 1/16W MF-LF 402
CB950 0.1UF 20% 10V CERM 402
NOSTUFF RB950 4.7K 1% 1/16W MF-LF 402
UB950 MC74VHC1G08 SOT23-5-LF
PCI_RESET_L 20 92
122 30 28 24 SYS_IO_RESET_L
Shasta drives PCI RESET, but its output may not be valid during power-up, so it is ANDed with a reset from the SMU.
RB900 0 NOSTUFF 1/16W MF-LF 402

PP3V3_RUN_SB 7 119
RPB900 4.7K 5% 1/16W SM-LF
PCI_SLOTA_REQ_L 119 121
RPB900 4.7K
PCI_SLOTA_GNT_L 119 121
RPB900 4.7K
PCI_SLOTG_REQ_L 119 122
RPB900 4.7K
PCI_SLOTG_GNT_L 119 122
RPB901 4.7K
PCI_SLOTD_REQ_L 119
RPB901 4.7K
PCI_SLOTD_GNT_L 119

119 7 PP3V3_RUN_SB
RPB902 4.7K
122 121 120 119 PCI_DEVSEL_L
RPB902 4.7K
122 121 120 119 PCI_FRAME_L
RPB902 4.7K
122 121 120 119 PCI_IRDY_L
RPB902 4.7K
122 121 120 119 PCI_TRDY_L
RPB901 4.7K
122 121 120 119 PCI_STOP_L

Shasta PCI Interface

SYNC_MASTER=Q63 SYNC_DATE=08/01/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 119 OF 154	

LAST_MODIFIED=Tue Nov 1 14:55:26 2005
DRAWING
TITLE=KILOWARA
ASSEMBLY=DRAWING

ALL RESISTOR PACKS ARE 47 OHM 1/16W 5%

R PAKS ARE PIN SWAPPABLE ACROSS ALL SIGNALS (EXCEPT IDSELS)

119	PCI_SB_AD<0>	RPC003	4	5	47	PCI_AD<0>	119 121 122 125
119	PCI_SB_AD<1>	RPC003	1	8	47	PCI_AD<1>	119 121 122 125
119	PCI_SB_AD<2>	RPC009	1	8	47	PCI_AD<2>	119 121 122 125
119	PCI_SB_AD<3>	RPC001	3	6	47	PCI_AD<3>	119 121 122 125
119	PCI_SB_AD<4>	RPC000	3	6	47	PCI_AD<4>	119 121 122 125
119	PCI_SB_AD<5>	RPC003	2	7	47	PCI_AD<5>	119 121 122 125
119	PCI_SB_AD<6>	RPC001	4	5	47	PCI_AD<6>	119 121 122 125
119	PCI_SB_AD<7>	RPC000	2	7	47	PCI_AD<7>	119 121 122 125
119	PCI_SB_AD<8>	RPC007	4	5	47	PCI_AD<8>	119 121 122 125
119	PCI_SB_AD<9>	RPC002	1	8	47	PCI_AD<9>	119 121 122 125
119	PCI_SB_AD<10>	RPC000	1	8	47	PCI_AD<10>	119 121 122 125
119	PCI_SB_AD<11>	RPC009	3	6	47	PCI_AD<11>	119 121 122 125
119	PCI_SB_AD<12>	RPC000	4	5	47	PCI_AD<12>	119 121 122 125
119	PCI_SB_AD<13>	RPC009	4	5	47	PCI_AD<13>	119 121 122 125
119	PCI_SB_AD<14>	RPC002	2	7	47	PCI_AD<14>	119 121 122 125
119	PCI_SB_AD<15>	RPC002	4	5	47	PCI_AD<15>	119 121 122 125
119	PCI_SB_AD<16>	RPC002	3	6	47	PCI_AD<16>	119 121 122 125

RC000

119	PCI_SB_AD<17>		1	2	47 5% 1/16W MF-LF 402	PCI_AD<17>	119 121 122 125

119	PCI_SB_AD<18>	RPC007	1	8	47	PCI_AD<18>	119 121 122 125
119	PCI_SB_AD<19>	RPC006	2	7	47	PCI_AD<19>	119 121 122 125
119	PCI_SB_AD<20>	RPC007	2	7	47	PCI_AD<20>	119 121 122 125
119	PCI_SB_AD<21>	RPC008	1	8	47	PCI_AD<21>	119 121 122
119	PCI_SB_AD<22>	RPC004	1	8	47	PCI_AD<22>	119 121 122
119	PCI_SB_AD<23>	RPC006	4	5	47	PCI_AD<23>	119 121 122
119	PCI_SB_AD<24>	RPC008	4	5	47	PCI_AD<24>	119 121 122 125
119	PCI_SB_AD<25>	RPC006	3	6	47	PCI_AD<25>	119 121 122 125
119	PCI_SB_AD<26>	RPC008	3	6	47	PCI_AD<26>	119 121 122 125

RC001

119	PCI_SB_AD<27>		1	2	47 5% 1/16W MF-LF 402	PCI_AD<27>	119 121 122 125

119	PCI_SB_AD<28>	RPC004	4	5	47	PCI_AD<28>	119 121 122 125
119	PCI_SB_AD<29>	RPC008	2	7	47	PCI_AD<29>	119 121 122 125
119	PCI_SB_AD<30>	RPC004	2	7	47	PCI_AD<30>	119 121 122 125
119	PCI_SB_AD<31>	RPC007	3	6	47	PCI_AD<31>	119 121 122 125
119	PCI_SB_CBE_L<0>	RPC003	3	6	47	PCI_CBE_L<0>	119 121 122
119	PCI_SB_CBE_L<1>	RPC001	1	8	47	PCI_CBE_L<1>	119 121 122
119	PCI_SB_CBE_L<2>	RPC006	1	8	47	PCI_CBE_L<2>	119 121 122
119	PCI_SB_CBE_L<3>	RPC004	3	6	47	PCI_CBE_L<3>	119 121 122
119	PCI_SB_DEVSEL_L	RPC005	3	6	47	PCI_DEVSEL_L	119 121 122
119	PCI_SB_FRAME_L	RPC005	4	5	47	PCI_FRAME_L	119 121 122
119	PCI_SB_IRDY_L	RPC005	2	7	47	PCI_IRDY_L	119 121 122
119	PCI_SB_TRDY_L	RPC005	1	8	47	PCI_TRDY_L	119 121 122
119	PCI_SB_STOP_L	RPC001	2	7	47	PCI_STOP_L	119 121 122
119	PCI_SB_PAR	RPC009	2	7	47	PCI_PAR	119 121 122

PLACE CLOSE TO SHASTA

AD<17> IS IDSEL FOR AIRPORT
AD<27> IS IDSEL FOR USB

PCI SERIES TERMINATION

SYNC_MASTER=FINO-MW SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 120 OF 154	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_CLK_AIRPORT	CLOCKS	

PCI_CLK33M_AIRPORT 26 121

Page Notes

Power aliases required by this page:
- _PP3V3_PCI

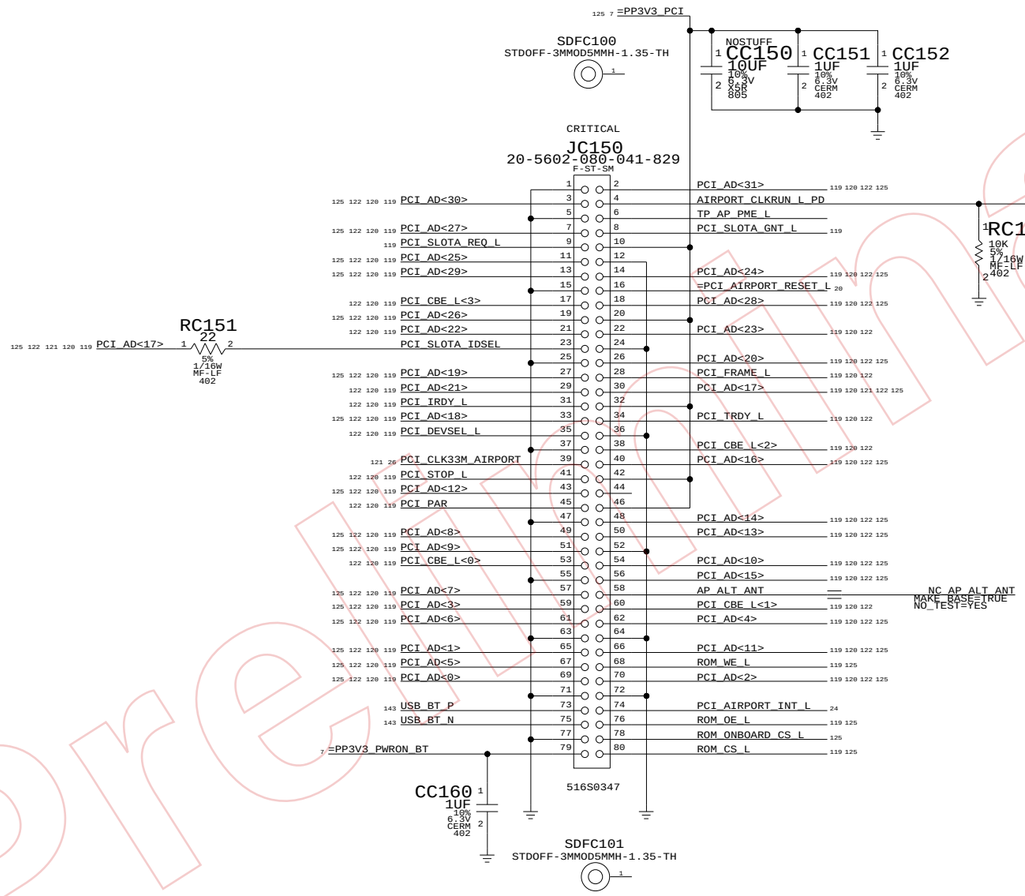
Signal aliases required by this page:
- _PCI_CLK33M_AIRPORT (33MHz PCI clock)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD17 (Slot "A") - AirPort (0x????/0x????)

NOTE: This AirPort implementation does not support PME#.

Q85 WIRELESS CONNECTOR



AIRPORT & BLUETOOTH

SYNC_MASTER=FINO-MW SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 121 OF 154	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	CLOCKS	

=PCI_CLK33M_USB2 27 122

Page Notes

Power aliases required by this page:
- _PPVIO_PCI (to 3.3V or 5V)

Signal aliases required by this page:
- _PCI_CLK33M_USB2 (33MHz PCI clock)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD27 (Slot "G") - USB2 (0x1033/0x0035)

NOTE: This USB2 implementation supports
D3cold.

Q63 APPLICATION OF POWER NET "=PPVIO_PCI_USB2" IS PP3V3_RUN

122 7 =PPVIO_PCI_USB2

CC201 0.1uF 20% 10V CERM 402
CC202 0.1uF 20% 10V CERM 402
CC203 0.1uF 20% 10V CERM 402

XWC200 SM 2 1 6 PP_VIOPCIUSB2_C2 P4MM SM PP 1 PPC203

M3 M4 C8 VDD_PCI

CRITICAL
UC200
NEC_UPD720101_USB2
FBGA-LF

125 121 120 119 PCI_AD<0>	M5	AD0	
125 121 120 119 PCI_AD<1>	P5	AD1	
125 121 120 119 PCI_AD<2>	N5	AD2	
125 121 120 119 PCI_AD<3>	P4	AD3	
125 121 120 119 PCI_AD<4>	N4	AD4	
125 121 120 119 PCI_AD<5>	M3	AD5	
125 121 120 119 PCI_AD<6>	N3	AD6	
125 121 120 119 PCI_AD<7>	M1	AD7	
125 121 120 119 PCI_AD<8>	L2	AD8	
125 121 120 119 PCI_AD<9>	L1	AD9	
125 121 120 119 PCI_AD<10>	K2	AD10	
125 121 120 119 PCI_AD<11>	L3	AD11	
125 121 120 119 PCI_AD<12>	K1	AD12	
125 121 120 119 PCI_AD<13>	K3	AD13	
125 121 120 119 PCI_AD<14>	J2	AD14	
125 121 120 119 PCI_AD<15>	J1	AD15	
125 121 120 119 PCI_AD<16>	F2	AD16	
125 121 120 119 PCI_AD<17>	E1	AD17	
125 121 120 119 PCI_AD<18>	E3	AD18	
125 121 120 119 PCI_AD<19>	D1	AD19	
125 121 120 119 PCI_AD<20>	D3	AD20	
121 120 119 PCI_AD<21>	D2	AD21	
121 120 119 PCI_AD<22>	C1	AD22	
121 120 119 PCI_AD<23>	C2	AD23	
125 121 120 119 PCI_AD<24>	B1	AD24	
125 121 120 119 PCI_AD<25>	A2	AD25	
125 121 120 119 PCI_AD<26>	B3	AD26	
125 121 120 119 PCI_AD<27> (PCI_AD<27>)	C3	AD27	
125 121 120 119 PCI_AD<28>	A3	AD28	
125 121 120 119 PCI_AD<29>	C4	AD29	
125 121 120 119 PCI_AD<30>	B4	AD30	
125 121 120 119 PCI_AD<31>	A4	AD31	
121 120 119 PCI_CBE_L<0>	M2	CBE0	
121 120 119 PCI_CBE_L<1>	J3	CBE1	
121 120 119 PCI_CBE_L<2>	F1	CBE2	
121 120 119 PCI_CBE_L<3>	C5	CBE3	
121 120 119 PCI_PAR	J4	PAR	
121 120 119 PCI_FRAME_L	F3	FRAME	
121 120 119 PCI_IRDY_L	F4	IRDY	
121 120 119 PCI_TRDY_L	G1	TRDY	
121 120 119 PCI_STOP_L	G3	STOP	
PCI_SLOTG_IDSEL	B5	IDSEL	
121 120 119 PCI_DEVSEL_L	G2	DEVSEL	
119 PCI_SLOTG_REQ_L	C6	REQ	
119 PCI_SLOTG_GNT_L	D6	GNT	
NEC_PERR_L_PU	H2	PERR	
NEC_SERR_L_PU	H1	SERR (OD)	
NEC_INTA_L	C7	INTA (OD)	
NEC_INTB_L	B7	INTB (OD)	
NEC_INTC_L	A7	INTC (OD)	
122 27 =PCI_CLK33M_USB2	A8	PCLK	
NEC_VBBRST_L	B8	VBBRST (CHIP RESET)	
NEC_CRUN_L_PD	N6	CRUN	
NEC_PME_L	D5	PME (OD)	
	C5	VCCRST (PCI RESET)	
6 TP_NEC_SMI_L	L6	SMI (OD)	
NEC_LEGC_PD	L7	LEGC	

IPD	NTEST1	M8	TP_NEC_NTEST1 6
IPD	SMC	M7	TP_NEC_SMC 6
IPD	TEB	N7	TP_NEC_TEB
IPD	AMC	P7	TP_NEC_AMC
IPD	TEST	L8	TP_NEC_TEST 6
	NANDTEST	M10	TP_NEC_NANDTEST
	SRCLK	M9	TP_NEC_SRCLK 6
	SRDTA	N9	TP_NEC_SRDATA
IPD	SRMOD	P9	TP_NEC_SRMOD 6

ALL NETS TO FUNCTIONAL TEST PAGE

RC214 22 5% 1/16W MF-LF 402

RC216 10K 5% 1/16W MF-LF 402
RC213 10K 5% 1/16W MF-LF 402

122 7 =PPVIO_PCI_USB2

24 PCI_USB2_INT_L
RPC203 47 5% 1/16W SM-LF (4 5)
RPC203 47 5% 1/16W SM-LF (2 7)
RPC203 47 5% 1/16W SM-LF (3 6)

119 30 28 24 SYS_IO_RESET_L
RC250 47 5% 1/16W MF-LF 402 (1 2)

28 24 SYS_PME_L
RC251 47 5% 1/16W MF-LF 402 (1 2)

20 =PCI_USB2_RESET_L

RC250, RC251 & RPC203 REQUIRED TO facilitate NAND-tree testing

RC215 4.7K 1% 1/16W MF-LF 402
RPC203 47 5% 1/16W SM-LF (8 1)

PPC200 P4MM SM PP 1
PPC201 P4MM SM PP 1

USB 2.0 PCI Interface

SYNC_MASTER=Q63 SYNC_DATE=08/01/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT: 122 OF: 154	

LAST_MODIFIED=Tue Nov 1 14:55:28 2005

DRAWING

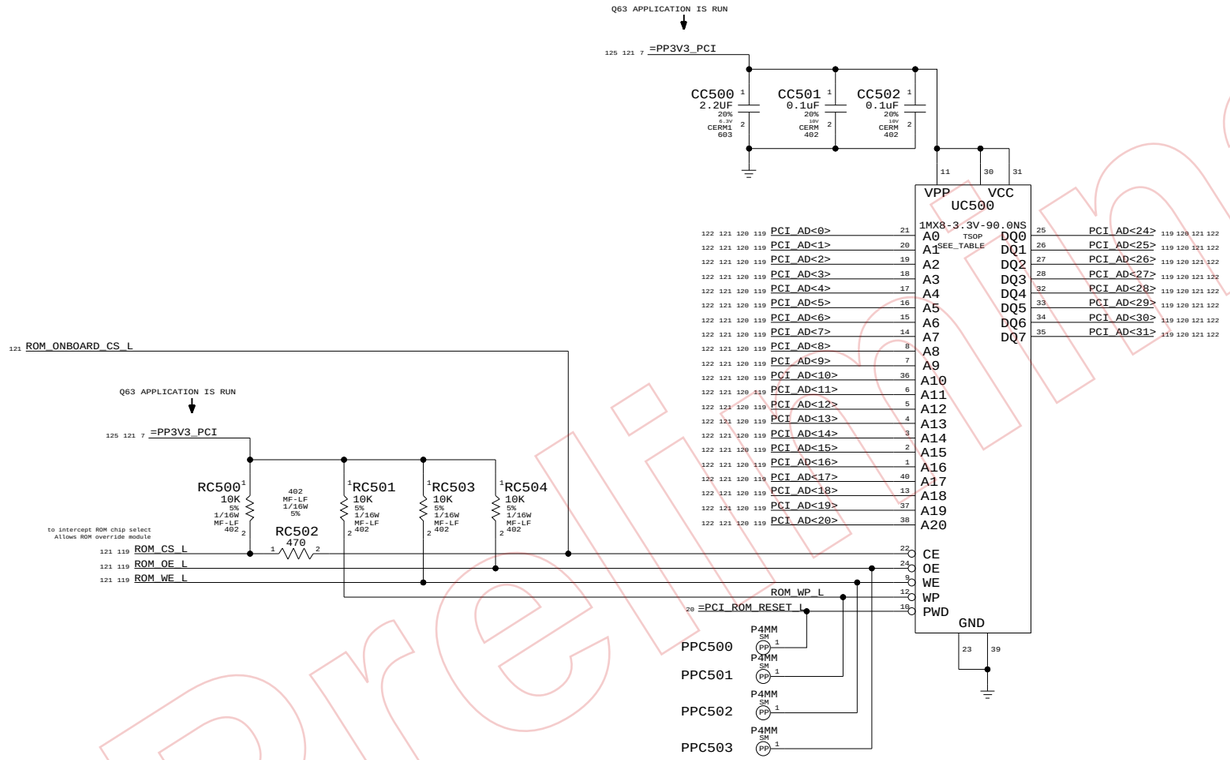
Page Notes

Power aliases required by this page:
- =PP3V3_PCI

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NOTE: This page does not specify a BootROM part number. Must use a TABLE_x_ITEM symbol to declare U7500 part number.



BootROM

SYNC_MASTER=Q63 SYNC_DATE=08/01/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E

SCALE: NONE

SHT 125 OF 154

LAST_MODIFIED=Tue Nov 1 14:55:29 2005

DRAWING

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR	
	SATA	SATA	SATA_RXD1_C	SATA_RXD_P1_C
	SATA	SATA	SATA_RXD1_C	SATA_RXD_N1_C
	SATA	SATA	SATA_TXD1	SATA_TXD_P1
	SATA	SATA	SATA_TXD1	SATA_TXD_N1
	SATA	SATA	SATA_RXD2_C	SATA_RXD_P2_C
	SATA	SATA	SATA_RXD2_C	SATA_RXD_N2_C
	SATA	SATA	SATA_TXD2	SATA_TXD_P2
	SATA	SATA	SATA_TXD2	SATA_TXD_N2
				UATA_DD<15..8>
				UATA_DD<7>
				UATA_DD<6..0>
				UATA_DA<2..0>
				UATA_CS0_L
				UATA_CS1_L
				UATA_HSTROBE
				UATA_STOP
				UATA_DMACK_L
	UATA_NETSPA			UATA_RESET_L
				UATA_DSTROBE
				UATA_DMARQ
				UATA_INTRQ
				UATA_DD_R<15..8>
				UATA_DD_R<7>
				UATA_DD_R<6..0>
				UATA_DA_R<2..0>
				UATA_CS0_L_R
				UATA_CS1_L_R
				UATA_DMACK_L_R
				UATA_HSTROBE_R
				UATA_STOP_R
				UATA_RESET_L_R

Page Notes

Power aliases required by this page:
- _P1V2_PWRON_DISK

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: SATA

Line To Line:	0.38mm
Length Tolerance:	1.27mm
Primary Max Sep:	0.25mm outer
Primary Max Sep:	0.23mm inner
Secondary Max Sep:	2.54mm
Secondary Length:	12.70mm

NOTE: Target differential impedance for SATA data pairs is 100 ohms.

=PP1V2_PWRON_DISK_SB → LC700 600-OHM-1.0A 0805

MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.6MM
PP1V2_SATA_VDD

CC705	2.2UF	20%	6.3V	CERM1	603
CC700	0.1uF	20%	16V	CERM	402
CC701	0.1uF	20%	16V	CERM	402
CC702	0.1uF	20%	16V	CERM	402
CC703	0.1uF	20%	16V	CERM	402
CC704	0.1uF	20%	16V	CERM	402

XWCC00 (SM) → PP_1V2PWRONDISKSB_CC, NO_TEST=YES → P4MM SM PP PPCC00

SATA_VDD x 5 — AB14, AB17, T14, W15, Y18 — SATA_VDD

U2300 SHASTA V1.1 BGA-LF (5 OF 8) SEE_TABLE

UATA

UD_IDEDD_0_H	J6	UATA_DD_R<0>	127 129
UD_IDEDD_1_H	H7	UATA_DD_R<1>	127 129
UD_IDEDD_2_H	H6	UATA_DD_R<2>	127 129
UD_IDEDD_3_H	E2	UATA_DD_R<3>	127 129
UD_IDEDD_4_H	C1	UATA_DD_R<4>	127 129
UD_IDEDD_5_H	C2	UATA_DD_R<5>	127 129
UD_IDEDD_6_H	E3	UATA_DD_R<6>	127 129
UD_IDEDD_7_H	G6	UATA_DD_R<7>	127 129
UD_IDEDD_8_H	G5	UATA_DD_R<8>	127 129
UD_IDEDD_9_H	D4	UATA_DD_R<9>	127 129
UD_IDEDD_10_H	G7	UATA_DD_R<10>	127 129
UD_IDEDD_11_H	F6	UATA_DD_R<11>	127 129
UD_IDEDD_12_H	C3	UATA_DD_R<12>	127 129
UD_IDEDD_13_H	F5	UATA_DD_R<13>	127 129
UD_IDEDD_14_H	E5	UATA_DD_R<14>	127 129
UD_IDEDD_15_H	D5	UATA_DD_R<15>	127 129
UD_IDEDA0_H	E6	UATA_DA_R<0>	127 129
UD_IDEDA1_H	C4	UATA_DA_R<1>	127 129
UD_IDEDA2_H	D6	UATA_DA_R<2>	127 129
UD_IDECS1FX_L	B3	UATA_CS0_L_R	127 129
UD_IDECS3FX_L	B4	UATA_CS1_L_R	127 129
UD_IDEDMACK_L	E8	UATA_DMACK_L_R	127 129
UD_IDERD_L	E4	UATA_HSTROBE_R	127 129
UD_IDEWR_L	D3	UATA_STOP_R	127 129
UD_IDERST_L	E7	UATA_RESET_L_R	127 129
UD_IDECHRDY_H	F9	UATA_DSTROBE	129 127
UD_IDEDMARQ_H	D7	UATA_DMARQ	129 127
UD_IDEINTRQ_H	C5	UATA_INTRQ	129 127

DSTROBE aka: IORDY/HDMARDY*
HSTROBE aka: DIOR*
STOP aka: DIOW*

SATA_RXD_P1_C	Y17	RXDP1	TXDP1 AA16 SATA_TXD_P1
SATA_RXD_N1_C	Y16	RXDN1	TXDN1 AB16 SATA_TXD_N1
		SATA 0	
SATA_RXD_P2_C	AB15	RXDP2	TXDP2 Y15 SATA_TXD_P2
SATA_RXD_N2_C	AA15	RXDN2	TXDN2 Y14 SATA_TXD_N2
		SATA 1	

SATA_GND — AA14, AA17, T13, W18

AC coupling required for any SATA pair used.
Recommend 0.1uF cap placed close to Shasta.
(Caps provided by device page)

P4MM SM PP PPCC01

PLACE TERMINATION RESISTORS AT UATA CONNECTOR JC901

DIOR- :HDMARDY- :HSTROBE >
DIOW- :STOP >

RC706	33	UATA_RESET_L_R	UATA_RESET_L
RC704	22	UATA_DMACK_L_R	UATA_DMACK_L
RC702	22	UATA_HSTROBE_R	UATA_HSTROBE
RC703	22	UATA_STOP_R	UATA_STOP
RC700	33	UATA_CS0_L_R	UATA_CS0_L
RC701	33	UATA_CS1_L_R	UATA_CS1_L

SPARE
RPC704 33 3 6 5% 1/16W SM-LF

RPC704	33	UATA_DA_R<0>	UATA_DA<0>
RPC704	33	UATA_DA_R<1>	UATA_DA<1>
RPC704	33	UATA_DA_R<2>	UATA_DA<2>
RPC700	33	UATA_DD_R<0>	UATA_DD<0>
RPC700	33	UATA_DD_R<1>	UATA_DD<1>
RPC700	33	UATA_DD_R<2>	UATA_DD<2>
RPC703	33	UATA_DD_R<3>	UATA_DD<3>
RPC701	33	UATA_DD_R<4>	UATA_DD<4>
RPC701	33	UATA_DD_R<5>	UATA_DD<5>
RPC703	33	UATA_DD_R<6>	UATA_DD<6>
RPC702	33	UATA_DD_R<7>	UATA_DD<7>
RPC702	33	UATA_DD_R<8>	UATA_DD<8>
RPC703	33	UATA_DD_R<9>	UATA_DD<9>
RPC700	33	UATA_DD_R<10>	UATA_DD<10>
RPC702	33	UATA_DD_R<11>	UATA_DD<11>
RPC701	33	UATA_DD_R<12>	UATA_DD<12>
RPC702	33	UATA_DD_R<13>	UATA_DD<13>
RPC701	33	UATA_DD_R<14>	UATA_DD<14>
RPC703	33	UATA_DD_R<15>	UATA_DD<15>

RC705 10K 5% 1/16W MF-LF 402

Shasta Disk

SYNC_MASTER=M23-DC SYNC_DATE=06/20/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

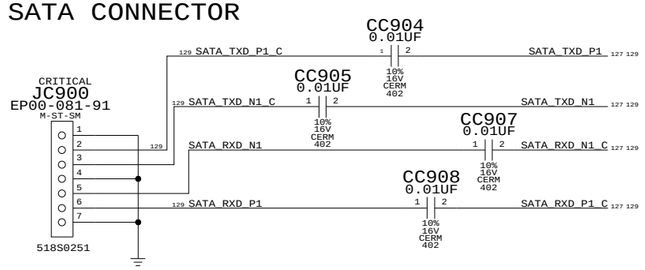
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 127 OF 154	

LAST_MODIFIED=Tue Nov 1 14:55:30 2005

DRAWING TITLE=SCHEMAT ABBREV=SHAHDWG

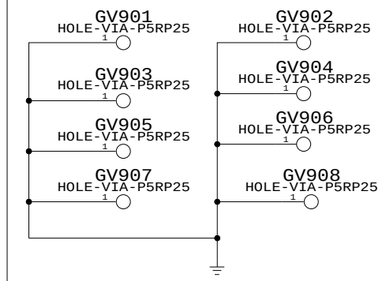
SATA CONNECTOR



SATA PORT1 IS NOT USED IN M23/M33:NO TEST

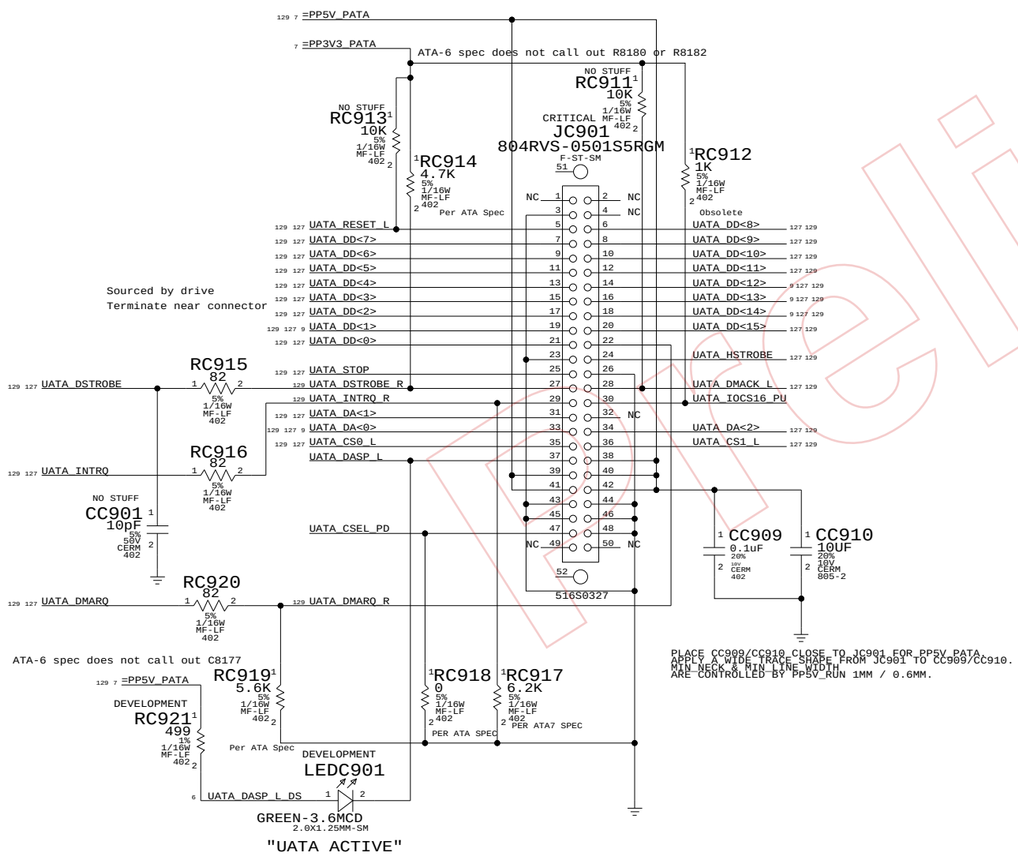
SATA_TXD_P2	NC_SATA_TXD_P2	MAKE_BASE=TRUE
SATA_TXD_N2	NC_SATA_TXD_N2	MAKE_BASE=TRUE
SATA_RXD_N2_C	NC_SATA_RXD_N2_C	MAKE_BASE=TRUE
SATA_RXD_P2_C	NC_SATA_RXD_P2_C	MAKE_BASE=TRUE

SATA DIFF PAIR GND VIAS



4-12-05
ADD THESE GROUND VIAS NEAR
EACH LAYER JUMP FOR THE SATA
DIFF PAIRS. ONE GND VIA PER
SIGNAL VIA, AND PLACE GND VIA
NO CLOSER THAN 0.152MM TO
SIGNAL VIA.

PATA CONNECTOR



ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	NO_TEST
UATA_DD<15..8>	UATA_DD	UATA_NETPH	UATA_NETSPA	
UATA_DD<7>	UATA_DD7	UATA_NETPH	UATA_NETSPA	
UATA_DD<6..0>	UATA_DD	UATA_NETPH	UATA_NETSPA	
UATA_DA<2..0>	UATA_HOST	UATA_NETPH	UATA_NETSPA	
UATA_CS0_L	UATA_HOST	UATA_NETPH	UATA_NETSPA	
UATA_CS1_L	UATA_HOST	UATA_NETPH	UATA_NETSPA	
UATA_HSTROBE	UATA_HOST	UATA_NETPH	UATA_NETSPA	
UATA_STOP	UATA_HOST	UATA_NETPH	UATA_NETSPA	
UATA_DMACK_L	UATA_HOST_R	UATA_NETPH	UATA_NETSPA	
UATA_RESET_L	UATA_RESET_L	UATA_NETPH	UATA_NETSPA	
UATA_DSTROBE_R	UATA_DEV_R_C	UATA_NETPH	UATA_NETSPA	
UATA_DMARQ_R	UATA_DEV_R	UATA_NETPH	UATA_NETSPA	
UATA_INTRQ_R	UATA_DEV_R	UATA_NETPH	UATA_NETSPA	

UATA FROM RPAKS TO JC901

UATA_DD_R<15..8>	UATA_NETPH	UATA_NETSPA		R392
UATA_DD_R<7>	UATA_NETPH	UATA_NETSPA		R383
UATA_DD_R<6..0>	UATA_NETPH	UATA_NETSPA		R384
UATA_DA_R<2..0>	UATA_NETPH	UATA_NETSPA		R385
UATA_CS0_L_R	UATA_NETPH	UATA_NETSPA		R386
UATA_CS1_L_R	UATA_NETPH	UATA_NETSPA		R387
UATA_HSTROBE_R	UATA_NETPH	UATA_NETSPA		R388
UATA_STOP_R	UATA_NETPH	UATA_NETSPA		R389
UATA_DMACK_L_R	UATA_NETPH	UATA_NETSPA		R390
UATA_RESET_L_R	UATA_NETPH	UATA_NETSPA		R391
UATA_DSTROBE	UATA_NETPH	UATA_NETSPA		R382
UATA_DMARQ	UATA_NETPH	UATA_NETSPA		R393
UATA_INTRQ	UATA_NETPH	UATA_NETSPA		R394

UATA FROM SHASTA U2300 TO RPAKS

SATA_TXD_P1	SATA_TXD1	SATA	SATA		TRUE
SATA_TXD_N1	SATA_TXD1	SATA	SATA		TRUE
SATA_TXD_P1_C	SATA_TXD1	SATA	SATA	TX1C	TRUE
SATA_TXD_N1_C	SATA_TXD1	SATA	SATA	TX1C	TRUE
SATA_RXD_N1_C	SATA_RXD1	SATA	SATA		TRUE
SATA_RXD_P1_C	SATA_RXD1	SATA	SATA		TRUE
SATA_RXD_N1	SATA_RXD1	SATA	SATA	RX1C	TRUE
SATA_RXD_P1	SATA_RXD1	SATA	SATA	RX1C	TRUE

4-11-05: BOARD FILE HAS PHYSICAL/SPACING NAME ASSIGMENT ALREADY FOR SATA DIFF PAIRS (CAP TO SHASTA).
BUT NOT FOR THE SATA CAP TO CONNECTOR ROUTES, WHICH THE ABOVE ARE ADDED FOR THIS PURPOSE.

UATA TRACE IMPEDANCE ROUTE TO 50 OHMS

4-8-05
NOTES FOR SHARED PAGE 127
FOR M23/M33 CREATE A WIDE SHAPE
FOR PP1V2_SATA_VDD AND THEN NECK DOWN
TO THE DEFAULT VALUE WHEN NECESSARY.
THE WIDTH/NECK PROPERTIES ON PAGE 127
ARE SET BY Q63 FOR SCHEMATIC SHARING.

LC700 CHANGED TO 155S0240 (600 OHM,0.2 OHM DCR,1A)
PREVIOUS ONE WAS 155S0031 (600 OHM,0.6 OHM DCR,0.2A)
PER TOKIN AMERICA PN: N2012Z601.

4-11-05.
PP1V2_ALL REG. IS SET TO BE 1.22V TO 1.23V
AS NOTED ON THE 1.2 REG PAGE 13. THIS WILL
HELP MITIGATE THE LOSS ACROSS THE Q1306 FET
SI3326DV.

4-12-05.
UPDATED AC COUPLING CAPS FOR SATA JC900.
ADDED DECOUPLING CAPS FOR JC901 PP5V_PATA NET.

Disk Connectors

SYNC_MASTER=M23-DC SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 129 OF 154	

PLACE THESE SERIES TERM CLOSE TO DRIVER: SB/SHASTA

SHASTA -> VESTA

131 9	ENET_TXD_R<0>	I59	MAKE_BASE=TRUE	ENET_TXD<0>	9 131 132
131 9	ENET_TXD_R<1>	I60	MAKE_BASE=TRUE	ENET_TXD<1>	9 131 132
131 9	ENET_TXD_R<2>	I61	MAKE_BASE=TRUE	ENET_TXD<2>	9 131 132
131 9	ENET_TXD_R<3>	I62	MAKE_BASE=TRUE	ENET_TXD<3>	9 131 132
131 9	ENET_TXD_R<4>	I63	MAKE_BASE=TRUE	ENET_TXD<4>	9 131 132
131 9	ENET_TXD_R<5>	I64	MAKE_BASE=TRUE	ENET_TXD<5>	9 131 132
131 9	ENET_TXD_R<6>	I65	MAKE_BASE=TRUE	ENET_TXD<6>	9 131 132
131 9	ENET_TXD_R<7>	I66	MAKE_BASE=TRUE	ENET_TXD<7>	9 131 132
131 9	ENET_TX_EN_R	I67	MAKE_BASE=TRUE	ENET_TX_EN	9 131 132
131 9	ENET_TX_ER_R	I68	MAKE_BASE=TRUE	ENET_TX_ER	9 131 132
131	ENET_CLK125M_GTX_R	I69	MAKE_BASE=TRUE	ENET_CLK125M_GTX	131 132
131	ENET_MDIO_R		MAKE_BASE=TRUE	ENET_MDIO	131 132

PLACE THESE SERIES TERM CLOSE TO DRIVER: VESTA

VESTA -> SHASTA

132	ENET_CLK125M_GBE_REF_R	I84	MAKE_BASE=TRUE	ENET_CLK125M_GBE_REF	131
132	ENET_CLK25M_TX_R	I70	MAKE_BASE=TRUE	ENET_CLK25M_TX	131
132	ENET_CLK125M_RX_R	I71	MAKE_BASE=TRUE	ENET_CLK125M_RX	131
132 131 9	ENET_RXD_R<0>	I72	MAKE_BASE=TRUE	ENET_RXD<0>	9 131
132 131 9	ENET_RXD_R<1>	I73	MAKE_BASE=TRUE	ENET_RXD<1>	9 131
132 131 9	ENET_RXD_R<2>	I74	MAKE_BASE=TRUE	ENET_RXD<2>	9 131
132 131 9	ENET_RXD_R<3>	I75	MAKE_BASE=TRUE	ENET_RXD<3>	9 131
132 131 9	ENET_RXD_R<4>	I76	MAKE_BASE=TRUE	ENET_RXD<4>	9 131
132 131 9	ENET_RXD_R<5>	I77	MAKE_BASE=TRUE	ENET_RXD<5>	9 131
132 131 9	ENET_RXD_R<6>	I78	MAKE_BASE=TRUE	ENET_RXD<6>	9 131
132 131 9	ENET_RXD_R<7>	I79	MAKE_BASE=TRUE	ENET_RXD<7>	9 131
132 131	ENET_RX_DV_R	I80	MAKE_BASE=TRUE	ENET_RX_DV	131
132 131	ENET_RX_ER_R	I81	MAKE_BASE=TRUE	ENET_RX_ER	131
132 131	ENET_COL_R	I82	MAKE_BASE=TRUE	ENET_COL	131
132 131	ENET_CRS_R	I83	MAKE_BASE=TRUE	ENET_CRS	131

ENET SERIES TERM

SYNC_MASTER=FINO-DC SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E

SCALE	SHT	OF
NONE	130	154

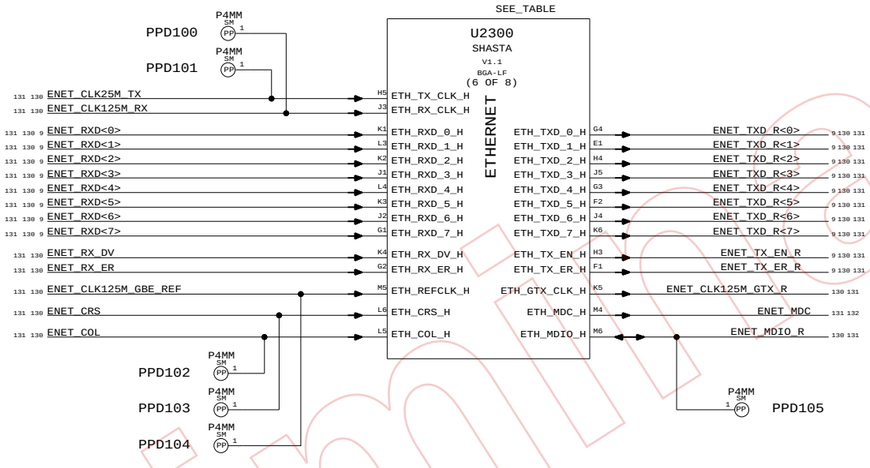
ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
I47		0.38mm SPACING	ENET_CLK25M_TX 130 131
I46		0.38mm SPACING	ENET_CLK125M_RX 130 131
I49		0.38mm SPACING	ENET_CLK125M_GBE_REF 130 131
I22		0.38mm SPACING	ENET_CLK125M_GTX 130 132
I50		0.38mm SPACING	ENET_CLK125M_GTX_R 130 131
I51	ENET_FW_2X		ENET_RXD_R<7..0> 9 130 132
I52	ENET_FW_3X		ENET_RX_DV_R 130 132
I53	ENET_FW_3X		ENET_RX_ER_R 130 132
I54	ENET_FW_2X		ENET_RXD<7..0> 9 130 131
I55	ENET_FW_3X		ENET_RX_DV 130 131
I56	ENET_FW_3X		ENET_RX_ER 130 131
I58	ENET_FW_2X		ENET_TXD_R<7..0> 9 130 131
I57	ENET_FW_3X		ENET_TX_EN_R 9 130 131
I59	ENET_FW_3X		ENET_TX_ER_R 9 130 131
I60	ENET_FW_2X		ENET_TXD<7..0> 9 130 132
I61	ENET_FW_3X		ENET_TX_EN 9 130 132
I62	ENET_FW_3X		ENET_TX_ER 9 130 132
I63	ENET_FW_3X		ENET_CRS_R 130 132
I64	ENET_FW_3X		ENET_COL_R 130 132
I65	ENET_FW_3X		ENET_CRS 130 131
I66	ENET_FW_3X		ENET_COL 130 131
I68	ENET_FW_3X		ENET_MDC 131 132
I41	ENET_FW_3X		ENET_MDIO 130 131 132
I42	ENET_FW_3X		ENET_MDIO_R 130 131
I43	ENET_FW_3X		R8405_1 131
I45	ENET_FW_3X		R8405_2 131
I44	ENET_FW_3X		R8407_2 131

Page Notes

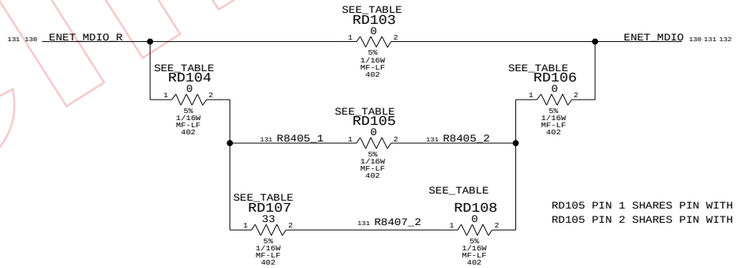
Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



RD103 PIN 1 SHARES PIN WITH RD104 PIN 1
RD103 PIN 2 SHARES PIN WITH RD106 PIN 2



RD105 PIN 1 SHARES PIN WITH RD107 PIN 1
RD105 PIN 2 SHARES PIN WITH RD108 PIN 2

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,0-OHM,402,5%	RD103		ENET_MDIO_DELAY_0
116S0004	3	RES,0-OHM,402,5%	RD104,RD105,RD106		ENET_MDIO_DELAY_2NS
116S0004	3	RES,0-OHM,402,5%	RD104,RD108,RD106		ENET_MDIO_DELAY_4NS
116S0030	1	RES,33-OHM,402,5%	RD107		ENET_MDIO_DELAY_4NS

*

Shasta Ethernet

SYNC_MASTER=Q63 SYNC_DATE=08/01/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 131 OF 154	

LAST_MODIFIED=Tue Nov 1 13:56:12 2005

DRAWING

TITLE=KILOHANA

ABBREV=SMDRAWING

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
	0.38mm_SPACING		ENET_CLK125M_GBE_REF_R 130 132
	0.38mm_SPACING		ENET_CLK125M_RX_R 130 132
	0.38mm_SPACING		ENET_CLK25M_TX_R 130 132
	ENET	ENET_MDI0	ENET_MDI_P<0> 132 136
	ENET	ENET_MDI0	ENET_MDI_N<0> 132 136
	ENET	ENET_MDI1	ENET_MDI_P<1> 132 136
	ENET	ENET_MDI1	ENET_MDI_N<1> 132 136
	ENET	ENET_MDI2	ENET_MDI_P<2> 132 136
	ENET	ENET_MDI2	ENET_MDI_N<2> 132 136
	ENET	ENET_MDI3	ENET_MDI_P<3> 132 136
	ENET	ENET_MDI3	ENET_MDI_N<3> 132 136
	0.38mm_SPACING		VESTA_CLK25M_XTALI 132
	0.38mm_SPACING		VESTA_CLK25M_XTALO 132
	0.38mm_SPACING		VESTA_CLK25M_XTALO_R 132

Page Notes

Power aliases required by this page:
- =PP3V3_ENET
- =PP2V5_ENETFW
- =PP1V2_ENETFW

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: ENET

Line To Line: 0.38mm
Length Tolerance: 1.27mm
Primary Max Sep: 0.13mm
Secondary Max Sep: 2.54mm
Secondary Length: 12.70mm

NOTE: Target differential impedance for ENET data pairs is 100 ohms.

Q63 APPLICATION IS ALL
139 17 7 =PP2V5_ENETFW
LD200 FERR-EMI-600-OHM SM
PP2V5_VESTA_BIASVDD1 6 VOLTAGE=2.5V MIN_LINE_WIDTH=0.50mm MIN_NECK_WIDTH=0.38mm
CD201 0.1uF 20% 10V CERM 402
LD201 FERR-EMI-600-OHM SM
PP2V5_VESTA_XTALVDD1 6 VOLTAGE=2.5V MIN_LINE_WIDTH=0.50mm MIN_NECK_WIDTH=0.38mm
CD202 10UF 10% 6.3V X5R 805
CD203 0.001uF 20% 50V CERM 402
XWD200 SM OMIT TP_VESTA_BIASVDD1 P4MM SM PPD239
XWD201 SM OMIT TP_VESTA_XTALVDD1 P4MM SM PPD201
XWD202 SM OMIT TP_VESTA_PLLVDD1 P4MM SM PPD238
PP1V2_VESTA_PLLVDD1 6 VOLTAGE=1.2V MIN_LINE_WIDTH=0.50mm MIN_NECK_WIDTH=0.38mm
CD204 0.001uF 20% 50V CERM 402
CD205 10UF 10% 6.3V X5R 805
Q63 APPLICATION IS ALL
LD202 FERR-EMI-600-OHM SM
=PP1V2_ENETFW 7 17 139
VESTA SPEC CALLS FOR 2.2UF, LOW ESR CAP
ESR < 0.5 ohms
PPD200 P4MM SM
131 130 ENET_CLK125M_GTX
XTALVDD1 BIASVDD1 PLLVDD1
SEE_TABLE
VESTA ENET
U1701
VESTA-V1.3
FBGA-200-LF
2 OF 3
GTXCLK A4 IPD
CLK125 D1 ENET_CLK125M_GBE_REF_R 130 132
TXC A6 ENET_CLK25M_TX_R 130 132
RXC C1 ENET_CLK125M_RX_R 130 132
131 130 9 ENET_TXD<0> B6 TXD[0] IPD
131 130 9 ENET_TXD<1> C6 TXD[1] IPD
131 130 9 ENET_TXD<2> C7 TXD[2] IPD
131 130 9 ENET_TXD<3> D6 TXD[3] IPD
131 130 9 ENET_TXD<4> E6 TXD[4] IPD
131 130 9 ENET_TXD<5> C5 TXD[5] IPD
131 130 9 ENET_TXD<6> B5 TXD[6] IPD
131 130 9 ENET_TXD<7> A5 TXD[7] IPD
RXD[0] F4 ENET_RXD_R<0> 9 130 131
RXD[1] F5 ENET_RXD_R<1> 9 130 131
RXD[2] E5 ENET_RXD_R<2> 9 130 131
RXD[3] E4 ENET_RXD_R<3> 9 130 131
RXD[4] E3 ENET_RXD_R<4> 9 130 131
RXD[5] D5 ENET_RXD_R<5> 9 130 131
RXD[6] D4 ENET_RXD_R<6> 9 130 131
RXD[7] D3 ENET_RXD_R<7> 9 130 131
131 130 9 ENET_TX_EN B4 TX_EN IPD
131 130 9 ENET_TX_ER C4 TX_ER IPD
RX_DV D2 ENET_RX_DV_R 130 131
RX_ER C2 ENET_RX_ER_R 130 131
131 ENET_MDC G1 MDC IPD
131 130 ENET_MDIO G2 MDIO IPU
COL F3 ENET_COL_R 130 131
CRS G3 ENET_CRS_R 130 131
VESTA_ENET_LOWPWR H5 LOWPWR IPD
IPD=INTERNAL PULL-DOWN
IPU=INTERNAL PULL-UP
RBC0 A3 TP_VESTA_RBC0 9
RBC1 B3 TP_VESTA_RBC1 9
9 TP_VESTA_PHYA<0> L5 PHYA[0] IPD
9 TP_VESTA_PHYA<1> L4 PHYA[1] IPD
9 TP_VESTA_PHYA<2> L3 PHYA[2] IPD
9 TP_VESTA_PHYA<3> L2 PHYA[3] IPD
9 TP_VESTA_PHYA<4> L1 PHYA[4] IPD
TRD+[0] R4 ENET_MDI_P<0> 132 136
TRD-[0] R5 ENET_MDI_N<0> 132 136
TRD+[1] R7 ENET_MDI_P<1> 132 136
TRD-[1] R6 ENET_MDI_N<1> 132 136
TRD+[2] R8 ENET_MDI_P<2> 132 136
TRD-[2] R9 ENET_MDI_N<2> 132 136
TRD+[3] R11 ENET_MDI_P<3> 132 136
TRD-[3] R10 ENET_MDI_N<3> 132 136
9 TP_VESTA_EN_10B K3 EN_10B IPD
9 TP_VESTA_RGMIIEN B8 RGMIIEN IPD
9 TP_VESTA_FDX C8 FDX IPU
9 TP_VESTA_F1000 K4 F1000 IPU
9 TP_VESTA_SPD0 K5 SPD0 IPD
9 TP_VESTA_MANMS D9 MANMS IPD
9 TP_VESTA_HUB A9 HUB IPD
9 TP_VESTA_ER H3 ER IPD
INTR*/ENERGYDET D10 ENET_ENERGYDET 24
IPU SLAVE*/AN_EN C10 TP_VESTA_AN_EN 9
QUALITY*/TXC_RXC_DELAY A8 TP_VESTA_TXC_RXC_DELAY 9
IPD LINK1* A10 TP_VESTA_LINK1_L 9
IPD LINK2* B11 TP_VESTA_LINK2_L 9
IPD FDXLED* B10 TP_VESTA_FDXLED_L 9
IPU XMTLED* B12 TP_VESTA_XMTLED_L 136
IPU ACTLED* A11 TP_VESTA_ACTLED_L 136
9 TP_VESTA_TEST<0> M4 TEST[0]
9 TP_VESTA_TEST<1> M5 TEST[1]
9 TP_VESTA_TVCO N3 TVCO
RDAC1 R1 VESTA_RDAC1_PD
XTALGND BIASGND PLLGND1
P3 P2 P1
RD213 1.24K 1% 1/16W MF-LF 402
TERMINATION OFF PAGE
Put crystal circuit close to PHY
132 VESTA_CLK25M_XTALI N2 XTALI
132 VESTA_CLK25M_XTALO_R P2 XTALO
RD209 0 5% 1/16W MF-LF 402
CRITICAL
YD200 25.0000M 8X4.5MM-SM2
VESTA_CLK25M_XTALO 132
CD218 33pF 5% 50V CERM 402
CD219 33pF 5% 50V CERM 402
CRYSTAL LOAD CAPACITANCE IS 20PF
Q63 APPLICATION IS ALL
139 17 7 =PP3V3_ENETFW
RD204 1K 1% 1/16W MF-LF 402
QD200 2N7002DW-X-F SOT-363
136 132 7 =PP3V3_ENET
CD206 1UF 10% 6.3V CERM 402
QD200 2N7002DW-X-F SOT-363
17 VESTA_RESET_H
136 132 7 =PP3V3_ENET
RD250 1.5K 5% 1/16W MF-LF 402
131 ENET_MDC
131 130 ENET_MDIO

Vesta Config Straps:

PHYA<4..0> - PHY Address Select
(Internal Pull-downs)

EN_10B - TBI Interface Select
1 - TBI/RTBI Mode
0 - GMII/RGMII Mode
(Internal Pull-down)

RGMIIEN - RGMII Enable
1 - RGMII/RTBI Mode
0 - GMII/TBI Mode
(Internal Pull-down)

FDX - Full-Duplex Select
Sets manual duplex mode bit
(Internal Pull-up)

F1000 - Speed Select
See table below
(Internal Pull-up)

SPD0 - Speed Select
See table below
(Internal Pull-down)

MANMS - Manual Master/Slave Configuration Select
Sets manual master/slave configuration enable bit
(Internal Pull-down)

HUB - Repeater Select
Sets Hub/DTE bit and master/slave configuration value bit
(Internal Pull-down)

ER - Edge Rate Select
1 - Rise time approx. 5 ns
0 - Rise time approx. 4 ns
(Internal Pull-down)

AN_EN - Auto-Negotiation Select
1 - Auto-negotiation enabled
0 - Auto-negotiation disabled
(Internal Pull-up)

TXC_RXC_DELAY
1 - If RGMII Mode enabled, RXC clock and GTXCLK are delayed by 1.9 ns
0 - No clock delay
(Internal Pull-down)

AN_EN	F1000	SPD0	Description
0	0	0	Force 10BASE-T
0	0	1	Force 100BASE-TX
0	1	X	Force 1000BASE-T (test use only)
1	0	0	Auto-negotiate advertise 10BASE-T
1	0	1	Auto-negotiate advertise 10/100BASE-TX
1	1	0	Auto-negotiate advertise 10/100/1000BASE-T
1	1	1	Auto-negotiate advertise 1000BASE-T

Vesta Ethernet PHY

SYNC_MASTER=Q63 SYNC_DATE=08/01/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 132 OF 154	

LAST_MODIFIED=Tue Nov 1 14:55:32 2005
DRAWING
TITLE=SCHEMAT
ABBREV=SMAGNG

EXTRA CONSTRAINTS TO SUPPLEMENT THE THE MISSING NET PHYSICAL FROM EARLIER PAGE

NET_PHYSICAL_TYPE

P292	ENET	ENET_MDI_P<0>	132 136
P296	ENET	ENET_MDI_N<0>	132 136
P297	ENET	ENET_MDI_P<1>	132 136
P298	ENET	ENET_MDI_N<1>	132 136
P299	ENET	ENET_MDI_P<2>	132 136
P300	ENET	ENET_MDI_N<2>	132 136
P301	ENET	ENET_MDI_P<3>	132 136
P302	ENET	ENET_MDI_N<3>	132 136

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0253	1	CON,RJ-45 7 DEGRESS	JD600	CRITICAL	17_INCH_LCD
514-0254	1	CON,RJ-45 7 DEGRESS	JD600	CRITICAL	20_INCH_LCD

PUT DEVELOPMENT LEDS ON TOP SIDE OF BOARD

136 132 7 =PP3V3_ENET
DEVELOPMENT
RD601 330 5% 1/10W MF-LF 603
LED8700_P
DEVELOPMENT
LEDD600
GREEN-3.6MCD 2.0X1.25MM-SM

LD600
FERR-EMI-600-OHM
SM

7 =PP2V5_ENET
PP2V5_ENET_CTAP
MIN_LINE_WIDTH=0.58mm
MIN_NECK_WIDTH=0.38mm
VOLTAGE=2.5V
CD600 0.1UF 20% 10V CERM 402
CD601 0.1UF 20% 10V CERM 402

7 GND_CHASSIS_RJ45
CD604 0.001UF 10% 50V CERM 402

ENET TERMINATION

PLACE THESE PARTS NEAR VESTA

136 132 ENET_MDI_P<0>
136 132 ENET_MDI_N<0>
RD604 49.9 1% 1/16W MF-LF 402
RD605 49.9 1% 1/16W MF-LF 402
ENET_MDI0

136 132 ENET_MDI_P<1>
136 132 ENET_MDI_N<1>
CD606 0.01UF 20% 16V CERM 402
RD606 49.9 1% 1/16W MF-LF 402
RD607 49.9 1% 1/16W MF-LF 402
ENET_MDI1

136 132 ENET_MDI_P<2>
136 132 ENET_MDI_N<2>
RD608 49.9 1% 1/16W MF-LF 402
RD609 49.9 1% 1/16W MF-LF 402
CD607 0.01UF 20% 16V CERM 402
ENET_MDI2

136 132 ENET_MDI_P<3>
136 132 ENET_MDI_N<3>
CD608 0.01UF 20% 16V CERM 402
RD610 49.9 1% 1/16W MF-LF 402
RD611 49.9 1% 1/16W MF-LF 402
ENET_MDI3
CD609 0.01UF 20% 16V CERM 402

CD605 0.001UF 10% 50V CERM 402

(514-0253)
OMIT
JD600
JFM38V10-0112-4F
F-ANG-TH

PRIMARY
13
11
5 ENET_CTAP
6 ENET_CTAP
1 MDI_0+
2 MDI_0-
3 MDI_1+
4 MDI_1-
7 MDI_2+
8 MDI_2-
9 MDI_3+
10 MDI_3-
12
RJ45 CHIP SIDE

1CT:1CT
75 OHM
SECONDARY
J1
J2
J3
J4
J5
J6
J7
J8
RJ45 CABLE SIDE
SHIELD
1000PF, 2000V

132 TP_VESTA_XMTLED_L
VESTA_XMTLED_L
MAKE_BASE=TRUE

132 TP_VESTA_ACTLED_L
VESTA_ACTLED_L
MAKE_BASE=TRUE

136 132 7 =PP3V3_ENET
DEVELOPMENT
RD603 330 5% 1/10W MF-LF 603
LED8701_P
DEVELOPMENT
LEDD601
GREEN-3.6MCD 2.0X1.25MM-SM

SPARE GND VIAS FOR LAYER TRAVERSALS DURING ROUTING

ZHD690 HOLE-VIA
ZHD691 HOLE-VIA
ZHD692 HOLE-VIA
ZHD693 HOLE-VIA

ETHERNET CONNECTOR

SYNC_MASTER=FINO-DC SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 136 OF 154	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	ENET_FW_2X	
	ENET_FW_3X	
	ENET_FW_3X	
	ENET_FW_2X	
	ENET_FW_3X	
	ENET_FW_3X	
	ENET_FW_3X	
	ENET_FW_3X	
	0.38mm_SPACING	
	0.38mm_SPACING	
	0.38mm_SPACING	

Page Notes

Power aliases required by this page:
- _PP2V5_PWRON_SB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

119 24 23 7 =PP2V5_PWRON_SB

CD800 0.1uF 20% 10V CERM 402
CD801 0.1uF 20% 10V CERM 402
CD802 0.1uF 20% 10V CERM 402

FWVDDP
U2300
SHASTA
V1.1
BGA-LF
SEE TABLE (7 OF 8)

FIREWIRE

PHY_DATA_0_H	N4	FW_DATA<0>	138 139
PHY_DATA_1_H	P5	FW_DATA<1>	138 139
PHY_DATA_2_H	N1	FW_DATA<2>	138 139
PHY_DATA_3_H	M7	FW_DATA<3>	138 139
PHY_DATA_4_H	N6	FW_DATA<4>	138 139
PHY_DATA_5_H	L1	FW_DATA<5>	138 139
PHY_DATA_6_H	M3	FW_DATA<6>	138 139
PHY_DATA_7_H	L2	FW_DATA<7>	138 139
PHY_CTL_0_H	N2	139 138 FW_CTL_S<0>	RD801 0 5% 1/16W MF-LF 402 FW_CTL<0> 138 139
PHY_CTL_1_H	N3	139 138 FW_CTL_S<1>	RD802 0 5% 1/16W MF-LF 402 FW_CTL<1> 138 139
PHY_LPS_H	P6	FW_LPS	138 139
PHY_LREQ_H	P1	FW_LREQ	138 139
PHY_SCLK_H	P2	139 138 FW_CLK98M_PCLK	
PHY_PINT_L	P3	139 138 FW_PINT	
PHY_LCLK_H	R1	138 FW_CLK98M_LCLK_R	RD800 22 5% 1/16W MF-LF 402 FW_CLK98M_LCLK 138 139
PHY_LINKON_L	N7	FW_LINKON	139

Shasta FireWire

SYNC_MASTER=Q63 SYNC_DATE=08/01/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E

SCALE: NONE SHT 138 OF 154

LAST_MODIFIED=Tue Nov 1 14:55:34 2005

DRAWING

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
(PROVIDED BY LINK PAGE)		0.38mm SPACING		FW_CLK98M_PCLK_R 139
	FW	FW	FW_TPA0	FW_TPA_P<0> 139 140
	FW	FW	FW_TPA0	FW_TPA_N<0> 139 140
	FW	FW	FW_TPB0	FW_TPB_P<0> 139 140
	FW	FW	FW_TPB0	FW_TPB_N<0> 139 140
	FW	FW	FW_TPA1	FW_TPA_P<1> 139 140
	FW	FW	FW_TPA1	FW_TPA_N<1> 139 140
	FW	FW	FW_TPB1	FW_TPB_P<1> 139 140
	FW	FW	FW_TPB1	FW_TPB_N<1> 139 140
ETHERNET SPACING TO ROUTE ON LAYER 6	FW	FW	FW_TPA2	FW_TPA_P<2> 139 140
	FW	FW	FW_TPA2	FW_TPA_N<2> 139 140
	FW	FW	FW_TPB2	FW_TPB_P<2> 139 140
	FW	FW	FW_TPB2	FW_TPB_N<2> 139 140
		0.38mm SPACING		VESTA_CLK24M_XTALI 139
		0.38mm SPACING		VESTA_CLK24M_XTALO 139
		0.38mm SPACING		VESTA_CLK24M_XTALO_R 139
100V	FW_CTL			FW_CTL_S<1..0> 138
140V	FW_CTL			FW_CTL<1..0> 138 139
141V	FW_CTL			FW_CTL_R<1..0> 138 139

Page Notes

Power aliases required by this page:
- =PPFW_PHY
- =PP3V3_FW
- =PP3V3_ENETFW
- =PP2V5_ENETFW
- =PP1V2_ENETFW

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- VESTA_DS_ONLY_EN0
  If stuffed, adds external pull-up to counter internal pull-down in Vesta.
  See straps table for more information.
- VESTA_PWR_CLASS_0
  If stuffed, adds external pull-down to counter internal pull-up in Vesta.
  See straps table for more information.

Net Spacing Type: FW

NOTE: Target differential impedance for FW data pairs is 110 ohms.

VESTA CONFIG STRAPS:

FW_PWR_CLASS_MSB - FIREWIRE POWER CLASS
1 - Sets Power Class to 0x4
0 - Sets Power Class to 0x0
(Internal Pull-up)

FW_DS_ONLY_P0 - PORT 0 DATA/STROBE
1 - Port 0 Data/Strobe mode only
0 - Port 0 Bilingual mode
(Internal Pull-down)

ESDET[0]
1=PORTS 1 AND 2 DS ONLY
0=PARTS 1 AND 2 BI-LINGUAL
ESDET[1]
1=PORT 1 PRESENT
0=PORT 1 NOT PRESENT
ESDET[2]
1=PORT 2 PRESENT
0=PORT 2 NOT PRESENT

CRYSTAL LOAD CAPACITANCE IS 12PF

IPD=INTERNAL PULL-DOWN
IPU=INTERNAL PULL-UP

SEE_TABLE
VESTA FW
U1701
VESTA-V1.3
FBGA-200-LF
3 OF 3

Q63 PORT ALOCATION
800 REAR PORT
400 REAR PORT
400 FNT PNL PORT

Vesta FireWire PHY		
SYNC_MASTER=Q63	SYNC_DATE=08/01/2005	
NOTICE OF PROPRIETARY PROPERTY		
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART		
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6790 REV. E
	SCALE NONE	SHT 139 OF 154

LAST_MODIFIED=Tue Nov 1 14:55:35 2005

NET_TYPE SPACING	PHYSICAL	DIFFERENTIAL_PAIR		
FW	FW	FW_TPA0_FL	FW_PORT0_TPA_P_FL	140
FW	FW	FW_TPA0_FL	FW_PORT0_TPA_N_FL	140
FW	FW	FW_TPB0_FL	FW_PORT0_TPB_P_FL	140
FW	FW	FW_TPB0_FL	FW_PORT0_TPB_N_FL	140
FW	FW	FW_TPA1_FL	FW_PORT1_TPA_P_FL	140
FW	FW	FW_TPA1_FL	FW_PORT1_TPA_N_FL	140
FW	FW	FW_TPB1_FL	FW_PORT1_TPB_P_FL	140
FW	FW	FW_TPB1_FL	FW_PORT1_TPB_N_FL	140

=PP12V_ALL_FW

8 WATTS MAX
12 VOLTS

RE056 1.3 20% 1W FF 2512 — PP12V_FW (MIN_LINE_WIDTH=0.8MM, MIN_NECK_WIDTH=0.25MM, VOLTAGE=12V, MAKE_BASE=TRUE)

I443 =PPFW_PHY 139 — TO FW CDS PIN (CABLE POWER DETECT)

DE000 MURS320XXG SMC — FW_VP_R (MIN_LINE_WIDTH=0.8MM, MIN_NECK_WIDTH=0.25MM, MAKE_BASE=TRUE, VOLTAGE=24V)

CE009 0.1UF 10% 50V X7R 603-1 — FW_VP MAX IS 24V

CRITICAL
RE002 1.3 20% 1W FF 2512 — FW_VP (MIN_LINE_WIDTH=0.8MM, MIN_NECK_WIDTH=0.25MM, VOLTAGE=24V)

FE002 0.75AMP-13.2V MINISMD-LF — PPFW_PORT0_VP (MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=24V)

DESIGNED WITH INTENTION TO RESIZE FUSE LIMITS EQUAL FW SPEC 1.5A LIMIT

FE000 1.5AMP-33V SM-LF — PPFW_PORT1_VP (MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=24V)

POSSIBLE CURRENT SHARING SCENARIO
KCL = CABLE POWER + SYSTEM POWER = > 1.5 AMPS

Termination

Place close to FireWire PHY

VOLTAGE=1.86V
FW_TPBIAS<1> 139
FW_TPBIAS<0> 139 VOLTAGE=1.86V

CE050 1UF 10% 6.3V CERM 402
CE060 1UF 10% 6.3V CERM 402

RE050 56.2 1% 1/10W MF-LF 402
RE051 56.2 1% 1/16W MF-LF 402
RE060 56.2 1% 1/16W MF-LF 402
RE061 56.2 1% 1/10W MF-LF 402

FW_TPA_P<0> 139	MAKE_BASE=TRUE	FW_PORT0_TPA_P 140
FW_TPA_N<0> 139	MAKE_BASE=TRUE	FW_PORT0_TPA_N 140
FW_TPB_P<0> 139	MAKE_BASE=TRUE	FW_PORT0_TPB_P 140
FW_TPB_N<0> 139	MAKE_BASE=TRUE	FW_PORT0_TPB_N 140
FW_TPA_P<1> 139	MAKE_BASE=TRUE	FW_PORT1_TPA_P 140
FW_TPA_N<1> 139	MAKE_BASE=TRUE	FW_PORT1_TPA_N 140
FW_TPB_P<1> 139	MAKE_BASE=TRUE	FW_PORT1_TPB_P 140
FW_TPB_N<1> 139	MAKE_BASE=TRUE	FW_PORT1_TPB_N 140

RE052 56.2 1% 1/10W MF-LF 402
RE053 56.2 1% 1/16W MF-LF 402
RE062 56.2 1% 1/16W MF-LF 402
RE063 56.2 1% 1/10W MF-LF 402

FW_TPA_C<0> VOLTAGE=0V — RE054 4.99K 1% 1/16W MF-LF 402 — CE054 270pF 5% 25V CERM 402
FW_TPA_C<1> VOLTAGE=0V — RE064 4.99K 1% 1/16W MF-LF 402 — CE064 270pF 5% 25V CERM 402

3rd TPA/TPB pair unused

FW_TPBIAS<2> 139	NC_FW_TPBIAS2	MAKE_BASE=TRUE, NO_TEST=YES
FW_TPA_P<2> 139	NC_FW_TPA_P2	MAKE_BASE=TRUE, NO_TEST=YES
FW_TPA_N<2> 139	NC_FW_TPA_N2	MAKE_BASE=TRUE, NO_TEST=YES
FW_TPB_P<2> 139	FW_TPB2_PD	MAKE_BASE=TRUE, NO_TEST=YES
FW_TPB_N<2> 139		

RE070 1K 5% 1/10W MF-LF 402

ESD Rail

CALCULATION = 220 OHMS, THERE'S ALREADY A 215 IN THE DESIGN, SO I'M USING 215 INSTEAD

=PP3V3_FW — RE090 215 1% 1/10W MF-LF 402 — PP3V3_FW_ESD_F (VOLTAGE=3.3V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm) — LE090 400-OHM-EMI SM-1 — PP3V3_FW_ESD 140 (VOLTAGE=3.3V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm)

DE090 SOT23 BZX84C2V7-X-F

[LATE VG NOTES]
CURRENT THROUGH THE BIAS RESISTOR SHOULD BE 5MA FOR A VOLTAGE DROP TO 2.2V
IT IS 2.2V INSTEAD OF 2.7V BECAUSE THE SNAPBACK ESD DIODES HAVE A .5V DROP

ZHE090 HOLE-VIA
ZHE091 HOLE-VIA
ZHE092 HOLE-VIA
ZHE093 HOLE-VIA

SPARE GND VIAS FOR LAYER TRAVERSALS DURING ROUTING

"Snapback" & "Late VG" Protection

PP3V3_FW_ESD 140

DPE010 BAV99DW-X-F SOT-363
CE010 0.001UF 10% 50V CERM 402
CE011 0.001UF 10% 50V CERM 402

FW_PORT0_TPA_P 140
FW_PORT0_TPA_N 140
FW_PORT0_TPB_P 140
FW_PORT0_TPB_N 140

FLE010 120-OHM 2012 SYM_VER-1
FLE011 120-OHM 2012 SYM_VER-1

DPE011 BAV99DW-X-F SOT-363
CE012 0.001UF 10% 50V CERM 402
CE013 0.001UF 10% 50V CERM 402

LE010 FERR-160-OHM 1206-LF

PORT 0
1394A
OMIT

JE000 UF01613-M33-4F F-ST-TH

FW_PORT0_TPA_P_FL 140	TPO	(TPA+)
FW_PORT0_TPA_N_FL 140	TPO#	(TPA-)
FW_PORT0_TPB_P_FL 140	TPI	(TPB+)
FW_PORT0_TPB_N_FL 140	TPI#	(TPB-)
PPFW_PORT0_VP_FL	VP	
VOLTAGE=24V, MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm	VGND	

7 8 9 10

FW_VP MAX IS 24V
CE015 0.1UF 10% 50V X7R 603-1
CE016 0.01UF 20% 16V CERM 402

514-0251 20_INCH_VERSION SHOWN

GND_CHASSIS_FIREWIRE 7 140

"Snapback" & "Late VG" Protection

PP3V3_FW_ESD 140

DPE020 BAV99DW-X-F SOT-363
CE020 0.001UF 10% 50V CERM 402
CE021 0.001UF 10% 50V CERM 402

FW_PORT1_TPA_P 140
FW_PORT1_TPA_N 140
FW_PORT1_TPB_P 140
FW_PORT1_TPB_N 140

FLE020 120-OHM 2012 SYM_VER-1
FLE021 120-OHM 2012 SYM_VER-1

DPE021 BAV99DW-X-F SOT-363
CE022 0.001UF 10% 50V CERM 402
CE023 0.001UF 10% 50V CERM 402

PPFW_PORT1_VP 140

LE020 FERR-160-OHM 1206-LF

PORT 1
1394A
OMIT

JE001 UF01613-M33-4F F-ST-TH

FW_PORT1_TPA_P_FL 140	TPO	(TPA+)
FW_PORT1_TPA_N_FL 140	TPO#	(TPA-)
FW_PORT1_TPB_P_FL 140	TPI	(TPB+)
FW_PORT1_TPB_N_FL 140	TPI#	(TPB-)
PPFW_PORT1_VP_FL	VP	
MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=24V	VGND	

7 8 9 10

CE025 0.1UF 10% 50V X7R 603-1
CE026 0.01UF 20% 16V CERM 402

514-0251 20_INCH_VERSION SHOWN

GND_CHASSIS_FIREWIRE 7 140

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0248	1	CON,1394A 7 DEGREES	JE000	CRITICAL	17_INCH_LCD
514-0248	1	CON,1394A 7 DEGREES	JE001	CRITICAL	17_INCH_LCD
514-0251	1	CON,1394A 7 DEGREES	JE000	CRITICAL	20_INCH_LCD
514-0251	1	CON,1394A 7 DEGREES	JE001	CRITICAL	20_INCH_LCD

FIREWIRE CONNECTORS

SYNC_MASTER=FINO-DC SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 140 OF 154	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR	
	USB2	USB2_S	USB2_0	USB2_P<0>
	USB2	USB2_S	USB2_0	USB2_N<0>
	USB2	USB2_S	USB2_1	USB2_P<1>
	USB2	USB2_S	USB2_1	USB2_N<1>
	USB2	USB2_S	USB2_2	USB2_P<2>
	USB2	USB2_S	USB2_2	USB2_N<2>
	USB2	USB2	USB2_3	USB2_P<3>
	USB2	USB2	USB2_3	USB2_N<3>
	USB2	USB2	USB2_4	USB2_P<4>
	USB2	USB2	USB2_4	USB2_N<4>
	0.38mm SPACING			NEC_CLK30M_XT1
	0.38mm SPACING			NEC_CLK30M_XT2
	0.38mm SPACING			NEC_CLK30M_XT2_R

Page Notes

Power aliases required by this page:
- =PP3V3_PWRON_USB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: USB2

Line To Line: 0.50mm
Length Tolerance: 1.27mm
Primary Max Sep: 0.19mm
Secondary Max Sep: 2.54mm
Secondary Length: 12.70mm

NOTE: Target differential impedance for USB2 data pairs is 90 ohms.

Q63 USB PORT ALLOCATION
REAR USB (PORT #0)
FRONT PANEL USB (PORT #1)
REAR USB (PORT #2)
REAR USB (PORT #3)

U2300 SHASTA V1.1 BGA-LF (8 OF 8)

NC0	P7	TP_SB<0>
NC1	P8	TP_SB<1>
NC2	R3	TP_SB<2>
NC3	R4	TP_SB<3>
NC4	R5	TP_SB<4>
NC5	R6	TP_SB<5>
NC6	R7	TP_SB<6>
NC7	R8	TP_SB<7>
NC8	T1	TP_SB<8>
NC9	T2	TP_SB<9>
NC10	T3	TP_SB<10>
NC11	T4	TP_SB<11>
NC12	T5	TP_SB<12>
NC13	T6	TP_SB<13>
NC14	T7	TP_SB<14>
NC15	T8	TP_SB<15>
NC16	U1	TP_SB<16>
NC17	U2	TP_SB<17>
NC18	U3	TP_SB<18>
NC19	U4	TP_SB<19>
NC20	U5	TP_SB<20>
NC21	U6	TP_SB<21>
NC22	V1	TP_SB<22>
NC23	V2	TP_SB<23>
NC24	V3	TP_SB<24>
NC25	V4	TP_SB<25>
NC26	W1	TP_SB<26>
NC27	W3	TP_SB<27>
NC28	Y1	TP_SB<28>
NC29	Y3	TP_SB<29>

LE235 FERR-EMI-100-OHM SM
PP3V3_PWRON_NEC_AVDD (VOLTAGE=3.3V)
MIN_LINE_WIDTH=0.50mm
MIN_NECK_WIDTH=0.2MM
XWE200 SM OMIT
P4MM SM PPE2000
TP_NEC_AVDD
MINIMIZE TRACE LENGTH OF CAPS FROM AVDD TO AVSS PINS
RE235 4.7 5% 1/10W MF-LF 603
CE235 10UF 10% 6.3V X5R 805
CE236 0.1uF 20% 10V CERM 402
CE237 0.1uF 20% 10V CERM 402
GND_NEC_AVSS_R
145 144 142 7 =PP3V3_PWRON_USB
CE220 10UF 10% 6.3V X5R 805
CE221–CE225 0.1uF 20% 10V CERM 402
CE226–CE230 0.1uF 20% 10V CERM 402
VDD
AVDD

CRITICAL
UC200
NEC_UPD720101_USB2
FBGA-LF

RE200–RE209 36 1% 1/16W MF-LF 402

RSDM1	M14	USB_NEC_N<0>	USB2_N<0>
DM1	M13		USB2_N<0>
DP1	L14		USB2_P<0>
RSDP1	K13	USB_NEC_P<0>	USB2_P<0>
RSDM2	K14	USB_NEC_N<1>	USB2_N<1>
DM2	K12		USB2_N<1>
DP2	J14		USB2_P<1>
RSDP2	J12	USB_NEC_P<1>	USB2_P<1>
RSDM3	H11	USB_NEC_N<2>	USB2_N<2>
DM3	G11		USB2_N<2>
DP3	G13		USB2_P<2>
RSDP3	G14	USB_NEC_P<2>	USB2_P<2>
RSDM4	F12	USB_NEC_N<3>	USB2_N<3>
DM4	F14		USB2_N<3>
DP4	E12		USB2_P<3>
RSDP4	E14	USB_NEC_P<3>	USB2_P<3>
RSDM5	E13	USB_NEC_N<4>	USB2_N<4>
DM5	D14		USB2_N<4>
DP5	C13		USB2_P<4>
RSDP5	C14	USB_NEC_P<4>	USB2_P<4>

P4MM SM PPE2002
P4MM SM PPE2001

40.2 OHM RESISTORS ON PORT 2 FOR EVALUATION

BLUTOOTH CONNECTOR,(PORT #4)

145 144 142 7 =PP3V3_PWRON_USB
RE210 33K 5% 1/16W MF-LF 402
RPE210 10K 5% 1/16W SM-LF

USB2_OC<0>	B12	(USB2_OC<0>)	OCI1
USB2_OC<1>	B11	(USB2_OC<1>)	OCI2
USB2_OC<2>	B10	(USB2_OC<2>)	OCI3
USB2_OC<3>	A10	(USB2_OC<3>)	OCI4
USB2_OC<4>	B9	(USB2_OC<4>)	OCI5

USB2_PWREN<0>	C12	PPON1
USB2_PWREN<1>	A11	PPON2
USB2_PWREN<2>	C11	PPON3
USB2_PWREN<3>	C10	PPON4
USB2_PWREN<4>	A9	PPON5

145 144 142 7 =PP3V3_PWRON_USB
RE240 1.5K 5% 1/16W MF-LF 402
RE241 1.5K 5% 1/16W MF-LF 402
NEC_NC1_PU — P6 NC1
NEC_NC2_PU — M6 NC2

NEC_CLK30M_XT1	L9	XT1/SCLK
NEC_CLK30M_XT2_R	P8	XT2

RE245 100 1% 1/16W MF-LF 402
CRITICAL
YE245 30.0000M 8X4.5MM-SM1
NEC_CLK30M_XT2
CE245 22pF 5% 50V CERM 402
CE246 22pF 5% 50V CERM 402
SPEC SHOWS LOAD CAPACITANCE OF 16PF

VSS
XWE201 SM OMIT
AVSS
AVSS(R)
RREF — P11 NEC_RREF_PD
RE238 9.09K 1% 1/16W MF-LF 402
MINIMIZE TRACE LENGTH TO PINS
Tie to GND at ball N11
GND_NEC_AVSS_R (VOLTAGE=0V)
MIN_LINE_WIDTH=0.50mm
MIN_NECK_WIDTH=0.2MM

USB Host Interfaces

SYNC_MASTER=FINO-PC SYNC_DATE=07/05/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 142 OF 154	

LAST_MODIFIED=Tue Nov 1 14:55:37 2005
DRAWING
TITLE=KILOHANA
ABBREV=SMAWING

Page Notes

Power aliases required by this page:
- _PP5V_PWRON_USB
- _PP5V_PWRON_UDASH
- _PP3V3_PWRON_UDASH
- _PP3V3_PWRON_BT

Signal aliases required by this page:
(NONE)
NOTE: This page is expected to contain the necessary aliases to map the USB pairs to their appropriate destinations and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: USB pairs are NOT constrained on this page. It is assumed that the USB Host Controller page will provide the appropriate constraints to apply to entire USB D+/D- XNets.

neoBorg Implementation

NOTE: This design does not provide power control on USB ports 2-4. Rename USB controller outputs to indicate single-pin connections.

142 USB2_PWREN<0> — TP_USB2_PWREN<0> 6 MAKE_BASE=TRUE
142 USB2_PWREN<1> — TP_USB2_PWREN<1> 6 MAKE_BASE=TRUE
142 USB2_PWREN<2> — TP_USB2_PWREN<2> 6 MAKE_BASE=TRUE
142 USB2_PWREN<3> — TP_USB2_PWREN<3> 6 MAKE_BASE=TRUE
142 USB2_PWREN<4> — TP_USB2_PWREN<4> 6 MAKE_BASE=TRUE

External USB Ports

PORT 1

96 PP5V_USB2 — VOLTAGE=5V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM
LE310 FERR-250-OHM SM
NOSTUFF CE310 150UF 20% 6.3V POLY SMD2
RE336 0 805 1/8W MF-LF 5%
VOLTAGE=0V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM
CE312 0.01UF 20% 16V CERM 402
CE313 0.01UF 20% 16V CERM 402
GND_USB_PORT1
PP5V_USB2_PORT1_F — VOLTAGE=5V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM

142 USB2_N<0> — USB2_PORT1_N MAKE_BASE=TRUE
142 USB2_P<0> — USB2_PORT1_P MAKE_BASE=TRUE
LE312 120-OHM 2012 SYM_VER-1
NOSTUFF RE312 0 402
NOSTUFF RE313 0 402
143 USB2_PORT1_N_F
143 USB2_PORT1_P_F
RE310 15K 5% 1/16W MF-LF 402
RE311 15K 5% 1/16W MF-LF 402

OMIT JE310 UB01123M23-4F F-ST-TH
VDD, D-, D+, GND
PORT 1
514-0247
GND_CHASSIS_USB
MIN_NECK_WIDTH=0.2MM, MIN_LINE_WIDTH=0.6MM, VOLTAGE=0 — 7,143

PORT 2

LE320 FERR-250-OHM SM
NOSTUFF CE320 330UF 20% 6.3V POLY SMD
RE335 0 805 1/8W MF-LF 5%
VOLTAGE=0V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM
CE322 0.01UF 20% 16V CERM 402
CE323 0.01UF 20% 16V CERM 402
GND_USB_PORT2
PP5V_USB2_PORT2_F — VOLTAGE=5V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM

142 USB2_N<1> — USB2_PORT2_N MAKE_BASE=TRUE
142 USB2_P<1> — USB2_PORT2_P MAKE_BASE=TRUE
LE322 120-OHM 2012 SYM_VER-1
NOSTUFF RE322 0 402
NOSTUFF RE323 0 402
143 USB2_PORT2_N_F
143 USB2_PORT2_P_F
RE320 15K 5% 1/16W MF-LF 402
RE321 15K 5% 1/16W MF-LF 402

OMIT JE320 UB01123M23-4F F-ST-TH
VDD, D-, D+, GND
PORT 2
514-0247
GND_CHASSIS_USB — 7,143

PORT 3

LE330 FERR-250-OHM SM
PP5V_USB2_PORT3_F — VOLTAGE=5V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM
RE334 0 805 1/8W MF-LF 5%
VOLTAGE=0V, MIN_NECK_WIDTH=0.25MM, MIN_LINE_WIDTH=0.6MM
CE332 0.01UF 20% 16V CERM 402
CE333 0.01UF 20% 16V CERM 402
GND_USB_PORT3

142 USB2_N<2> — USB2_PORT3_N MAKE_BASE=TRUE
142 USB2_P<2> — USB2_PORT3_P MAKE_BASE=TRUE
LE332 120-OHM 2012 SYM_VER-1
NOSTUFF RE332 0 402
NOSTUFF RE333 0 402
143 USB2_PORT3_N_F
143 USB2_PORT3_P_F
RE330 15K 5% 1/16W MF-LF 402
RE331 15K 5% 1/16W MF-LF 402

OMIT JE330 UB01123M23-4F F-ST-TH
VDD, D-, D+, GND
PORT 3
514-0247
GND_CHASSIS_USB — 7,143

FE301 / LE340 / CE344 / RE346 / CE342 / CE343

FE301 0.75AMP-13.2V MINISMD-LF 740S0509 CRITICAL
LE340 FERR-250-OHM SM
=PP5V_PWRON_BNDI — VOLTAGE=5V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM
PP5V_BNDI_LE340
CE344 10UF 20% 10V CERM 805-2
RE346 0 805 1/8W MF-LF 5%
VOLTAGE=0V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM
CE342 0.01UF 20% 16V CERM 402
CE343 0.01UF 20% 16V CERM 402
GND_BNDI
PP5V_PWRON_BNDI — VOLTAGE=5V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM
GND_CHASSIS_BNDI

FHB CONNECTOR

518S0324
JE350 53261-1498 M-RT-SM

USB_HUB IMPLIMENTS 15K PULLDOWNS INTERNAL SO THEY ARE NOT NEEDED HERE

144 USB2_HUB_P<2> — NOSTUFF RE343 0 402 — LE342 120-OHM 2012 — NOSTUFF RE342 0 402 — 144 USB2_HUB_N<2>
144 USB2_HUB_P<3> — NOSTUFF RE354 0 402 — LE352 120-OHM 2012 — NOSTUFF RE355 0 402 — 144 USB2_HUB_N<3>

153 AUD_MIC_IN_P_CONN
153 GND_AUDIO_MIC_CONN
153 AUD_MIC_IN_N_CONN
143,7 GND_CHASSIS_BNDI
143,7 GND_CHASSIS_BNDI
143 USB2_HUB_P_L<2>
143 USB2_HUB_N_L<2>
143 GND_BNDI
143 USB2_P_L<3>
143 USB2_N_L<3>
24 SB_GPIO14
143 PP5V_PWRON_BNDI

4-14-05
PLACE CE343, CE344 & LE340 NEAR JE350 PIN 14 IN THE ORDER LISTED, AND NOT ON BOTH SIDES OF THE PIN.

UE300 USB Controller

CRITICAL
UE300 TPS2024 SOI-LF
=PP5V_PWRON_USB
IN_0, IN_1, EN*, OUT_0, OUT_1, OUT_2, OC*, GND

142 USB2_OC<0> — USB_OC MAKE_BASE=TRUE
142 USB2_OC<1>
142 USB2_OC<2>

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0294	3	USB RECEPTACLE,4P,UB1123-M23B-4F	JE310,JE320,JE330	CRITICAL	17_INCH_LCD
514-0295	3	USB RECEPTACLE,4P,UB1123-M33B-4F	JE310,JE320,JE330	CRITICAL	20_INCH_LCD

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE	
PROVIDED BY USB CONTROLLER	USB2	USB2_PORT1_F	USB2	USB2_PORT1_P_F 143
	USB2	USB2_PORT1_F	USB2	USB2_PORT1_N_F 143
	USB2	USB2_PORT2_F	USB2	USB2_PORT2_P_F 143
	USB2	USB2_PORT2_F	USB2	USB2_PORT2_N_F 143
	USB2	USB2_PORT3_F	USB2	USB2_PORT3_P_F 143
	USB2	USB2_PORT3_F	USB2	USB2_PORT3_N_F 143
	USB2	USB2_HUB_F	USB2	USB2_HUB_P_L<2> 143
	USB2	USB2_HUB_F	USB2	USB2_HUB_N_L<2> 143
	USB2	USB2_BNDI_F	USB2	USB2_P_L<3> 143
	USB2	USB2_BNDI_F	USB2	USB2_N_L<3> 143
	USB2	USB2_0_IC	USB2	USB_NEC_P<0> 142
	USB2	USB2_0_IC	USB2	USB_NEC_N<0> 142
	USB2	USB2_1_IC	USB2	USB_NEC_P<1> 142
	USB2	USB2_1_IC	USB2	USB_NEC_N<1> 142
	USB2	USB2_2_IC	USB2	USB_NEC_P<2> 142
	USB2	USB2_2_IC	USB2	USB_NEC_N<2> 142
	USB2	USB2_3_IC	USB2	USB_NEC_P<3> 142
	USB2	USB2_3_IC	USB2	USB_NEC_N<3> 142
	USB2	USB2_4_IC	USB2	USB_NEC_P<4> 142
	USB2	USB2_4_IC	USB2	USB_NEC_N<4> 142

DUE TO THESE NETS ARE ON A Q63 SHARED PAGE 124, THESE PROPERTIES FOR M23/M33 WERE PLACED ON THIS PAGE.

SENDS NEC USB PORT 3 TO BLUETOOTH MODULE

121 USB_BT_P — MAKE_BASE=TRUE — USB2_P<3> 142
121 USB_BT_N — MAKE_BASE=TRUE — USB2_N<3> 142
RE350 15K 5% 1/16W MF-LF 402
RE351 15K 5% 1/16W MF-LF 402

SENDS NEC CONTROLLER PORT 4 TO USB HUB UPSTREAM PORT

142 USB2_P<4> — MAKE_BASE=TRUE — USB2_HUB_P<0> 144
142 USB2_N<4> — MAKE_BASE=TRUE — USB2_HUB_N<0> 144
RE352 15K 5% 1/16W MF-LF 402
RE353 15K 5% 1/16W MF-LF 402

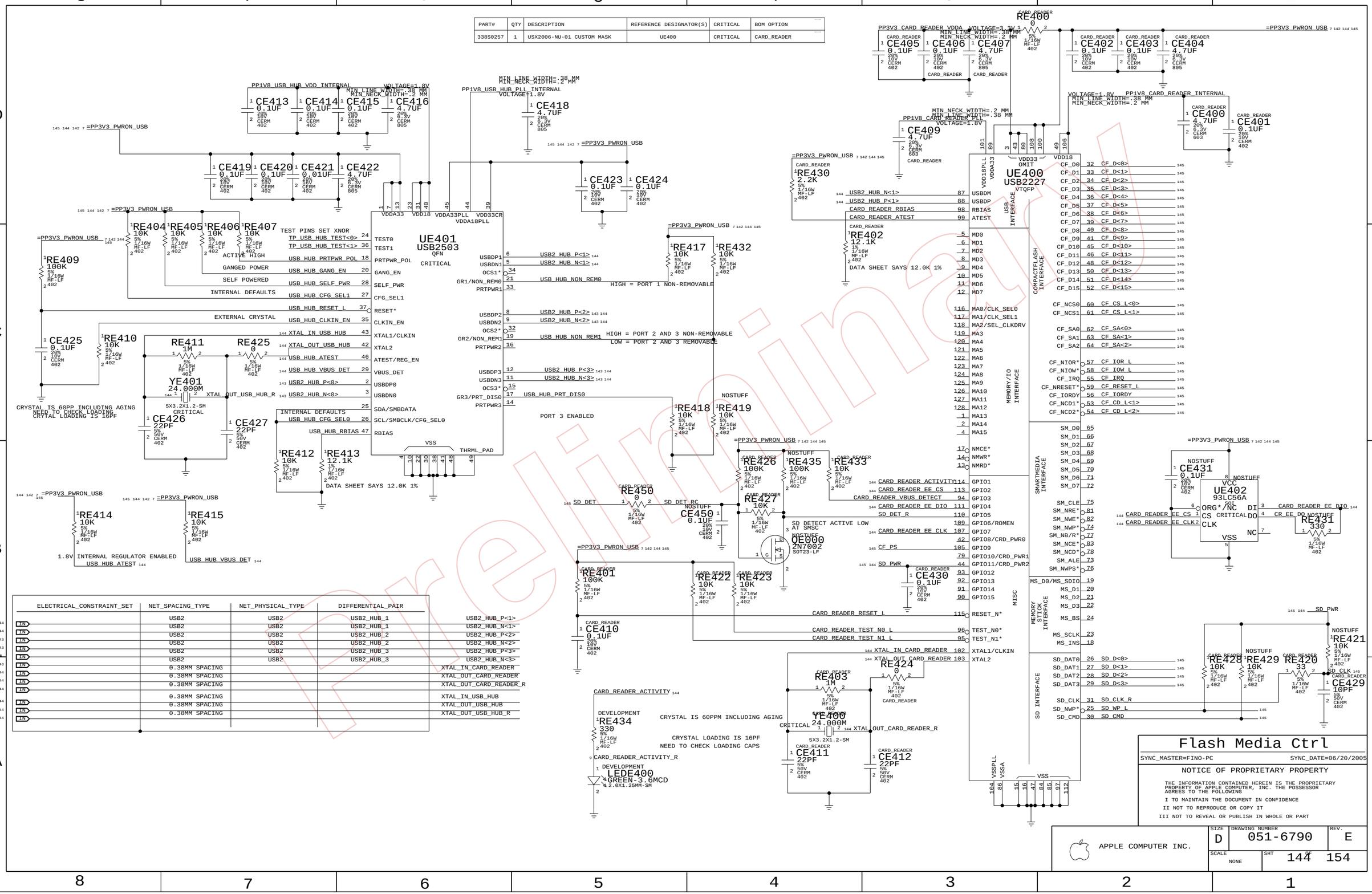
USB Device Interfaces

SYNC_MASTER=FINO-PC SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

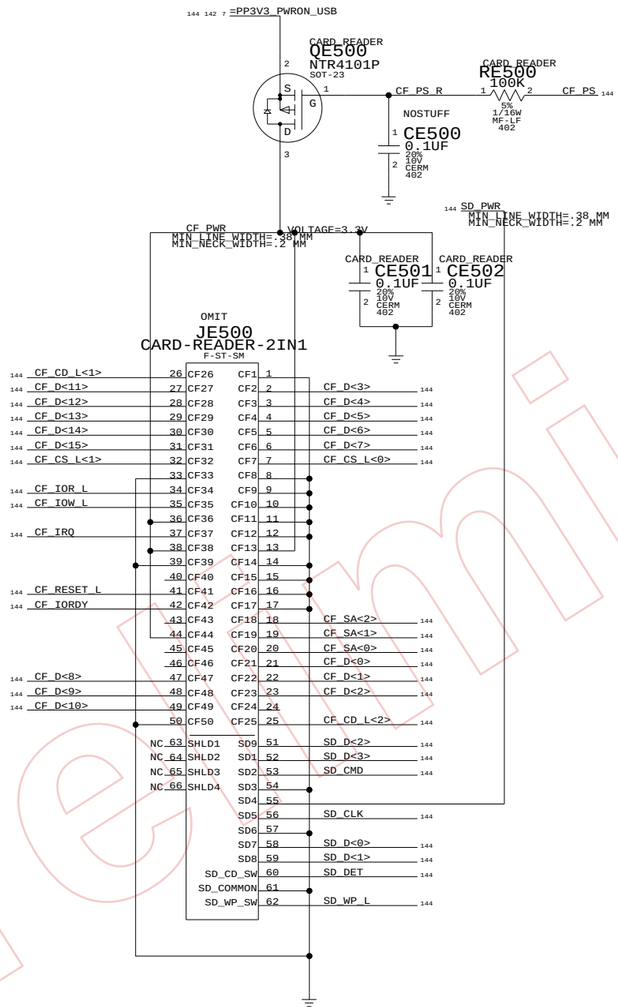
SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 143 OF 154	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0257	1	USX2006-NU-01 CUSTOM MASK	UE400	CRITICAL	CARD_READER



IF USING THE CARD READER, MUST CHANGE THESE BOM OPTIONS TO:

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION	
512S0010	1	CONN, MEDIA CARD M23	JE500	CRITICAL	CARD_READER	17_INCH_LCD
512S0012	1	CONN, MEDIA CARD M33	JE500	CRITICAL	CARD_READER	20_INCH_LCD



WRITE PROTECT AND CARD DETECT SWITCHES

CARD STATUS	WRITE PROTECT	WRITE ENABLE	CARD DETECT
NOT INSERTED	OPEN	OPEN	OPEN
FULLY INSERTED	OPEN	CLOSE	CLOSE

Flash Connector

SYNC_MASTER=FINO-PC SYNC_DATE=06/20/2005

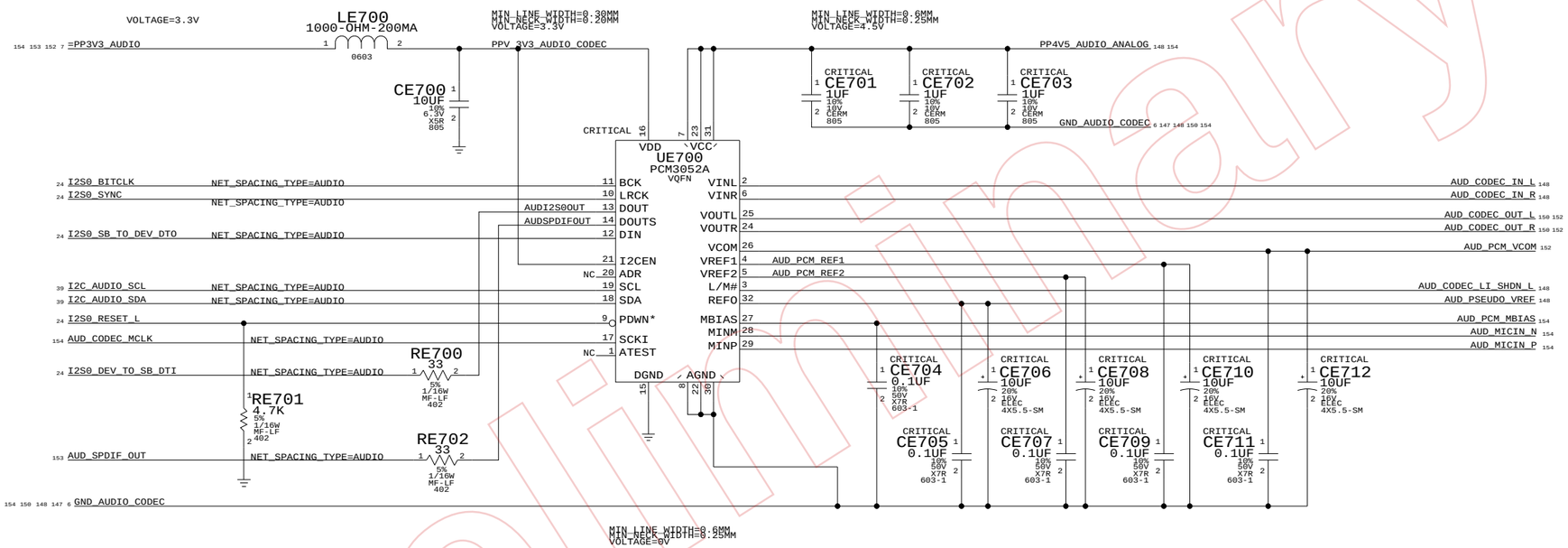
APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6790 | REV. E

SCALE NONE | SHT 145 OF 154

AUDIO CODEC

APPLE P/N 353S0933



AUDIO: CODEC

SYNC_MASTER=FINO-SO SYNC_DATE=10/07/2005

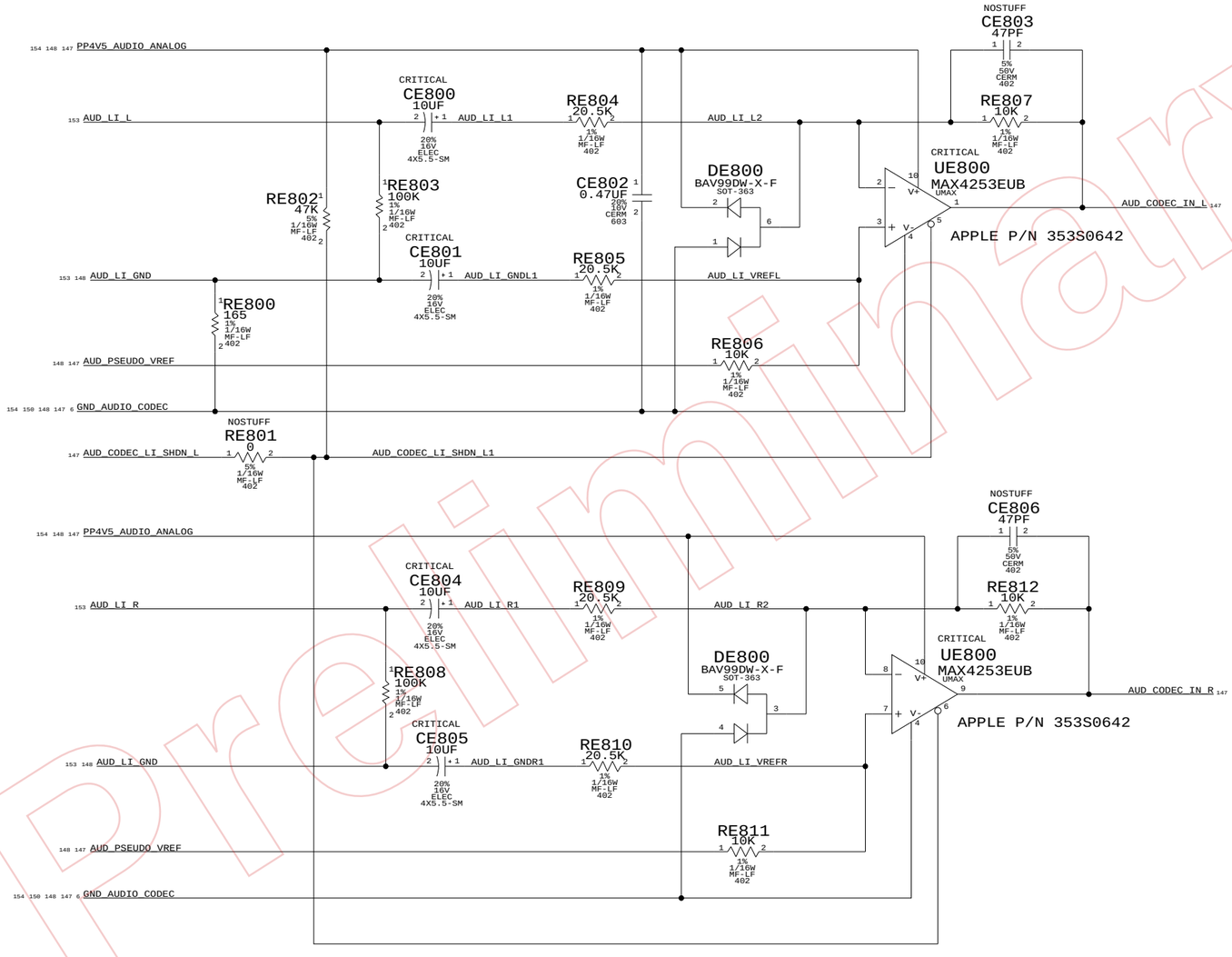
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E

SCALE	SHT	OF
NONE	147	154

LINE IN PSEUDO-DIFFERENTIAL AMP

AV= 0.49



AUDIO: LINE INPUT AMP

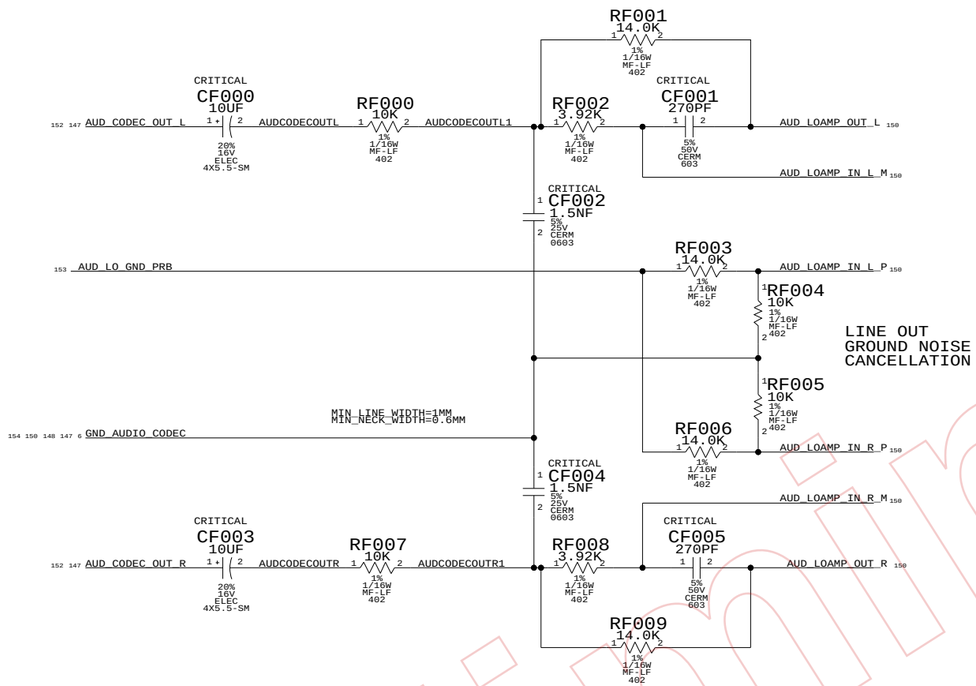
SYNC_MASTER=FINO-SO SYNC_DATE=10/07/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 148 OF 154	

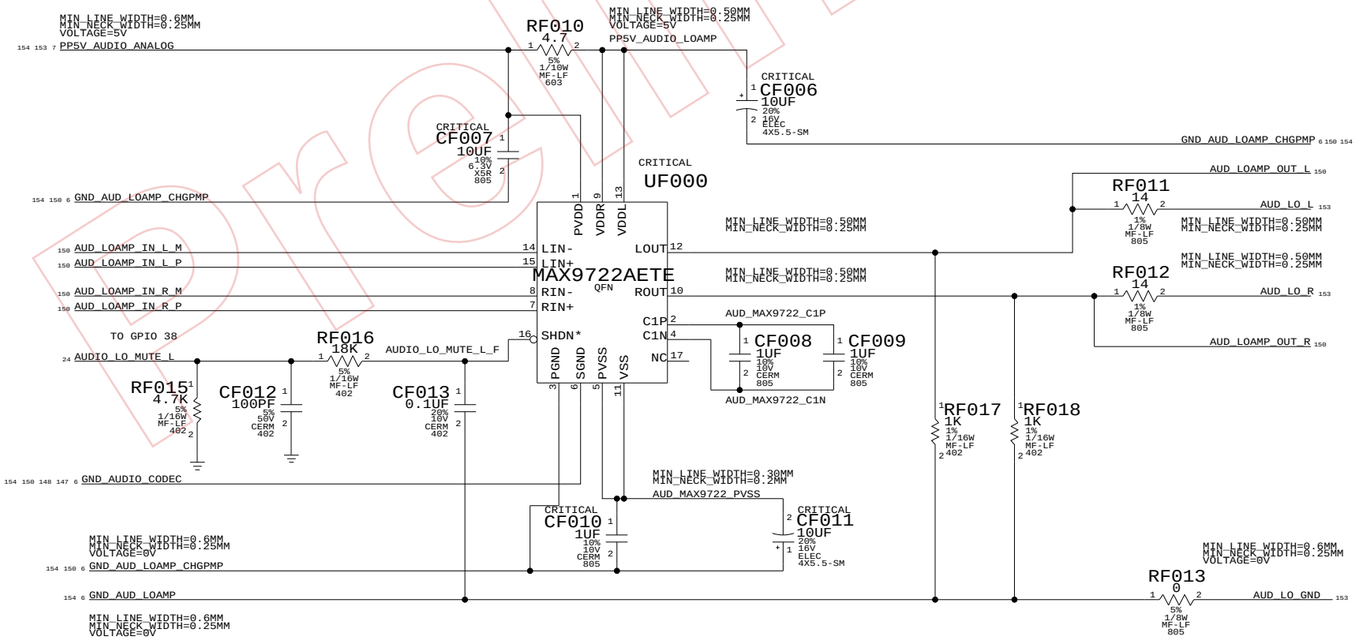
LINE OUT LOW-PASS FILTER

FC = 37 KHZ, HO = -1.4



LINE OUT AMP

APPLE P/N 353S0687



AUDIO: LINE OUT AMP

SYNC_MASTER=FINO-SO SYNC_DATE=10/07/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E

SCALE: NONE SHT OF: 150 154

SPEAKER AMP

APPLE P/N 353S0680

NET_SPACING_TYPE=AUDIO
DIFFERENTIAL_PAIR=AUD_SPKRAMP_PWR
MIN_LINE_WIDTH=1MM
MIN_NECK_WIDTH=0.30MM
VOLTAGE=12V

PP12V_AUDIO_SPKRAMP

LF200 FERR-250-OHM SM-1

NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=1MM
MIN_NECK_WIDTH=0.30MM
VOLTAGE=12V

PP12V_AUD_SPKRAMP_PLANE

CRITICAL CF217 220UF 20% 16V ELEC 6.3X8-SM
CRITICAL CF200 220UF 20% 16V ELEC 6.3X8-SM
CF201 10UF 10% 16V CERM 1210
CF218 0.1UF 20% 16V CERM 603
CF202 1UF 20% 16V CERM 1206
CF219 0.1UF 20% 16V CERM 603
CF203 10UF 10% 16V CERM 1210
CF223 10UF 10% 16V CERM 1210

GND_AUDIO_SPKRAMP_PLANE

=PP3V3_AUDIO

RF214 10K 1% 1/16W MF-LF 402

AUD_CODEC_OUT_L
LF205 1000-OHM-200MA 0603
CRITICAL CF204 0.47UF 10% 16V X7R 805
AUDSAMPINLN
CRITICAL CF215 100PF 5% 50V CERM 402
LF206 1000-OHM-200MA 0603
CRITICAL CF205 0.47UF 10% 16V X7R 805
AUDSAMPINLP

AUD_PCM_VCOM

AUD_CODEC_OUT_R
LF207 1000-OHM-200MA 0603
CRITICAL CF206 0.47UF 10% 16V X7R 805
AUDSAMPINRP
CRITICAL CF216 100PF 5% 50V CERM 402
LF208 1000-OHM-200MA 0603
CRITICAL CF207 0.47UF 10% 16V X7R 805
AUDSAMPINRN

UF200 MAX9714 QFN-LF

AUD_SAMP_INL_N	9	INL-
AUD_SAMP_INL_P	10	INL+
AUD_SAMP_INR_P	16	INR+
AUD_SAMP_INR_N	15	INR-
AUD_SAMP_G1	17	G1
AUD_SAMP_G2	18	G2
AUD_SAMP_FS1	19	FS1
AUD_SAMP_FS2	20	FS2
AUD_SAMP_SHDN_L	11	SHDN*
	8	NC
AUD_MAX9714_VREG	14	REG
	3,4,21,22	VDD
	7	CHOLD
	31,32	OUTL+
	29,30	OUTL-
	6	C1+
	5	C1-
	27,28	OUTR+
	25,26	OUTR-
	13,33,1,2,23,24	PGND
	12	SS

MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.15MM
AUD_MAX9714_VREG

AUD_MAX9714_CHOLD
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.2MM

NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.3MM
AUDSAMPOUTLP
AUDSAMPOUTLN
AUDSAMPOUTRP
AUDSAMPOUTRN

MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.15MM
AUDSAMPCPP
AUDSAMPCPN
CRITICAL CF208 0.1UF 10% 50V X7R 603-1
AUDSAMPCSS

LF201 180-OHM-1.5A 0603
LF202 180-OHM-1.5A 0603
LF203 180-OHM-1.5A 0603
LF204 180-OHM-1.5A 0603

AUD_SPKR_OUTL_P
AUD_SPKR_OUTL_N
AUD_SPKR_OUTR_P
AUD_SPKR_OUTR_N

CRITICAL CF210 1000PF 5% 25V CERM 603
CRITICAL CF211 1000PF 5% 25V CERM 603
CRITICAL CF212 1000PF 5% 25V CERM 603
CRITICAL CF213 1000PF 5% 25V CERM 603

CF209 0.47UF 10% 16V X7R 805

RF215 10K 1% 1/16W MF-LF 402
=PP3V3_AUDIO
AUDIO_SPKR_MUTE_L_INV

TIE TO GPIO 40
AUDIO_SPKR_MUTE_L
RF213 47K 5% 1/16W MF-LF 402
AUDIO_SPKR_MUTE_L_F

QF200 2N7002DW-X-F SOT-363
QF200 2N7002DW-X-F SOT-363

RF212 4.7K 5% 1/16W MF-LF 402
CF220 100PF 5% 50V CERM 402
CF221 100PF 5% 50V CERM 402

CF214 0.47UF 10% 16V X7R 805

XCF200 50MIL28

NET_SPACING_TYPE=AUDIO
DIFFERENTIAL_PAIR=AUD_SPKRAMP_PWR
MIN_LINE_WIDTH=1MM
MIN_NECK_WIDTH=0.25MM

XWF201 SM SMT

NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=1MM
MIN_NECK_WIDTH=0.25MM

GND_AUDIO_SPKRAMP
GND_AUDIO_SPKRAMP_PLANE

GAIN SETTINGS: +19DB

MODULATION SETTING: LOW EMI

GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

=PP3V3_AUDIO

RPF200 47K 5% 1/16W SM-LF

AUD_SAMP_FS2
AUD_SAMP_FS1
AUD_SAMP_G2
AUD_SAMP_G1

RF208 0 5% 1/16W MF-LF 402

GND_AUDIO_SPKRAMP_PLANE

AUDIO: SPEAKER AMP

SYNC_MASTER=FINO-SO SYNC_DATE=10/07/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E

SCALE	SHT	OF
NONE	152	154

LINE IN JACK

APPLE P/N 514-0246 (M23) APPLE P/N 514-0249 (M33)

OMIT
JF300
JA03333-M23-4F
F-ST-TH

LF300 FERR-EMI-100-OHM SM — AUD_LI_L_JACK → AUD_LI_L_EMI
LF301 FERR-EMI-100-OHM SM — AUD_LI_DET_JACK → AUD_LI_DET_EMI
LF302 FERR-EMI-100-OHM SM — AUD_LI_R_JACK → AUD_LI_R_EMI
LF303 FERR-EMI-100-OHM SM — AUD_LI_GND_JACK → AUD_LI_GND_EMI
LF304 FERR-EMI-100-OHM SM — AUD_LI_L_EMI → AUD_LI_L
LF305 FERR-EMI-100-OHM SM — AUD_LI_DET_EMI → AUD_LI_DET_H
LF306 FERR-EMI-100-OHM SM — AUD_LI_R_EMI → AUD_LI_R
LF307 FERR-EMI-100-OHM SM — AUD_LI_GND_EMI → AUD_LI_GND

MIN_LINE_WIDTH=0.2MM MIN_NECK_WIDTH=0.15MM
MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.3MM
MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.4MM

154 153 7 GND_CHASSIS_AUDIO_EXTERNAL

CF300 100PF 5% 50V CERM 402
CF301 100PF 5% 50V CERM 402
CF302 100PF 5% 50V CERM 402
CF303 100PF 5% 50V CERM 402

DZF300 14V-15A 0405

154 153 7 GND_CHASSIS_AUDIO_EXTERNAL

SPEAKER CABLE CONNECTOR

APPLE P/N 518S0249

JF301
53261-0798
M-RT-SM

MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.3MM NET_SPACING_TYPE=AUDIO

152 AUD_SPKR_OUTR_N → LF333 180-OHM-1.5A 0603 → AUD_SPKR_OUTR_N_CONN
152 AUD_SPKR_OUTR_P → LF330 180-OHM-1.5A 0603 → AUD_SPKR_OUTR_P_CONN
LF332 1000-OHM-200MA 0603 — AUDIO_SPKR_ID
152 AUD_SPKR_OUTL_N → LF331 180-OHM-1.5A 0603 → AUD_SPKR_OUTL_N_CONN
152 AUD_SPKR_OUTL_P → LF334 180-OHM-1.5A 0603 → AUD_SPKR_OUTL_P_CONN

NET_SPACING_TYPE=AUDIO MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.3MM

154 153 152 147 7 =PP3V3_AUDIO
RF313 47K 5% 1/16W MF-LF 402
24 AUDIO_SPKR_ID

SPEAKER TYPE DETECT TO GPIO 43

CF326 1000PF 5% 25V CERM 603
CF319 1000PF 5% 25V CERM 603
CF325 1000PF 5% 25V CERM 603
CF327 1000PF 5% 25V CERM 603

LINE IN PLUG DETECT

AUDIO_IN_DET0_L = LOW: PLUG INSERTED
AUDIO_IN_DET0_L = HIGH: PLUG NOT INSERTED

154 153 152 147 7 =PP3V3_AUDIO
RF300 100K 5% 1/16W MF-LF 402
RF301 47K 5% 1/16W MF-LF 402 — TO GPIO 34 → AUDIO_LI_DET_L 24
153 AUD_LI_DET_H
RF302 47K 5% 1/16W MF-LF 402 — AUDLINDETH
QF300 2N7002 SOT23-LF
CF308 0.1UF 20% 10V CERM 402

154 150 7 PP5V_AUDIO_ANALOG
152 147 7 =PP3V3_AUDIO 154 153
RF311 0 5% 1/16W MF-LF 402
RF310 0 NOSTUFF 5% 1/16W MF-LF 402
AUDIO_SPDIF_PWR

6 GND_AUDIO_MIC → LF308 FERR-EMI-100-OHM SM → GND_AUDIO_MIC_EMI
154 AUD_MIC_IN_P → LF309 FERR-EMI-100-OHM SM → AUD_MIC_IN_P_EMI
154 AUD_MIC_IN_N → LF310 FERR-EMI-100-OHM SM → AUD_MIC_IN_N_EMI
LF311 FERR-EMI-100-OHM SM — GND_AUDIO_MIC_EMI → GND_AUDIO_MIC_CONN
LF312 FERR-EMI-100-OHM SM — AUD_MIC_IN_P_EMI → AUD_MIC_IN_P_CONN
LF313 FERR-EMI-100-OHM SM — AUD_MIC_IN_N_EMI → AUD_MIC_IN_N_CONN

NET_SPACING_TYPE=AUDIO
DIFFERENTIAL_PAIR=AUDIO_MIC
DIFFERENTIAL_PAIR=MIC_IN

CF320 1000PF 10% 25V X7R 402
CF321 1000PF 10% 25V X7R 402
CF322 1000PF 10% 25V X7R 402

7 GND_CHASSIS_AUDIO_INTERNAL

DZF302 14V-15A 0405
DZF303 14V-15A 0405
NC

CRITICAL	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
CRITICAL	514-0246	1	LINE IN CONNECTOR, 5.5 DEG	JF300	17_INCH_LCD
CRITICAL	514-0260	1	COMBO OUT CONN, 4.5 DEG	JF303	17_INCH_LCD
CRITICAL	514-0249	1	LINE IN CONNECTOR, 5.5 DEG	JF300	20_INCH_LCD
CRITICAL	514-0261	1	COMBO OUT CONN, 4.5 DEG	JF303	20_INCH_LCD

LINE OUT PLUG DETECTS

AUDIO_LO_DET_L = LOW: PLUG INSERTED
AUDIO_LO_DET_L = HIGH: PLUG NOT INSERTED

AUDIO_LO_OPTICAL_PLUG_L = LOW: OPTICAL DIGITAL AUDIO PLUG INSERTED
AUDIO_LO_OPTICAL_PLUG_L = HIGH: ANALOG AUDIO PLUG INSERTED

154 153 152 147 7 =PP3V3_AUDIO
RF303 100K 5% 1/16W MF-LF 402
RF304 47K 5% 1/16W MF-LF 402 — TO GPIO 32 → AUDIO_LO_DET_L 24
153 AUD_LO_DET2
RF305 47K 5% 1/16W MF-LF 402 — AUD_LO_DET2_1
QF301 2N7002DW-X-F SOT-363
CF309 0.1UF 20% 10V CERM 402

154 153 152 147 7 =PP3V3_AUDIO
RF306 100K 5% 1/16W MF-LF 402
RF307 47K 5% 1/16W MF-LF 402 — TO GPIO 33 → AUDIO_LO_OPTICAL_PLUG_L 24
153 AUD_LO_DET1
RF308 47K 5% 1/16W MF-LF 402 — AUD_LO_DET1_1
NOSTUFF RF309 100K 5% 1/16W MF-LF 402
QF301 2N7002DW-X-F SOT-363
CF310 0.1UF 20% 10V CERM 402

LINE OUT JACK

APPLE P/N 514-0260 (M23)
APPLE P/N 514-0261 (M33)
OMIT
JF303
UCNT2052E007-0
F-ANG-TH

AUD_LO_DET1_JACK
AUD_LO_L_JACK
AUD_LO_DET2_JACK
AUD_LO_R_JACK
AUD_LO_GND_JACK
TYPE_DET
TIP
TIP_DET
RING
GND_1
GND_2
VIN
VCC
GND
LED

MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.4MM
MIN_LINE_WIDTH=0.5MM

RF312 0 5% 1/16W MF-LF 402
MIN_LINE_WIDTH=0.25MM MIN_NECK_WIDTH=0.2MM
AUD_SPDIF_GND

LF314 FERR-EMI-100-OHM SM — AUD_SPDIF_OUT → AUD_SPDIF_OUT_EMI
LF315 FERR-EMI-100-OHM SM — AUDIO_SPDIF_PWR → PP5V_AUDIO_SPDIF_EMI
LF316 FERR-EMI-100-OHM SM — AUD_LO_DET1 → AUD_LO_DET1_EMI
LF318 FERR-EMI-100-OHM SM — AUD_LO_L → AUD_LO_L_EMI
LF319 FERR-EMI-100-OHM SM — AUD_LO_DET2 → AUD_LO_DET2_EMI
LF317 FERR-EMI-100-OHM SM — AUD_LO_R → AUD_LO_R_EMI
LF320 FERR-EMI-100-OHM SM — AUD_LO_GND → AUD_LO_GND_EMI
LF321 FERR-EMI-100-OHM SM — AUD_LO_GND_PRB → AUD_LO_GND_PRB_EMI
LF322 FERR-EMI-100-OHM SM — AUD_SPDIF_OUT_EMI → AUD_SPDIF_OUT_JACK
LF323 FERR-EMI-100-OHM SM — PP5V_AUDIO_SPDIF_EMI → PP5V_AUDIO_SPDIF_JACK
LF324 FERR-EMI-100-OHM SM — AUD_LO_DET1_EMI
LF326 FERR-EMI-100-OHM SM — AUD_LO_L_EMI → AUD_LO_L_JACK
LF327 FERR-EMI-100-OHM SM — AUD_LO_DET2_EMI → AUD_LO_DET2_JACK
LF325 FERR-EMI-100-OHM SM — AUD_LO_R_EMI → AUD_LO_R_JACK
LF328 FERR-EMI-100-OHM SM — AUD_LO_GND_EMI → AUD_LO_GND_JACK
LF329 FERR-EMI-100-OHM SM — AUD_LO_GND_PRB_EMI

MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.5MM

CF311 100PF 5% 50V CERM 402
CF312 100PF 5% 50V CERM 402
CF315 100PF 5% 50V CERM 402
CF324 100PF 5% 50V CERM 402
CF316 0.01UF 10% 16V CERM 402
CF314 100PF 5% 50V CERM 402
CF313 100PF 5% 50V CERM 402
CF323 100PF 5% 50V CERM 402

AUD_LI_GND_EMI 153
DZF301 15V SOT23LF MMBZ15DLT1

154 153 7 GND_CHASSIS_AUDIO_EXTERNAL

AUDIO: CONNECTORS

SYNC_MASTER=FINO-SO SYNC_DATE=10/07/2005

NOTICE OF PROPRIETARY PROPERTY

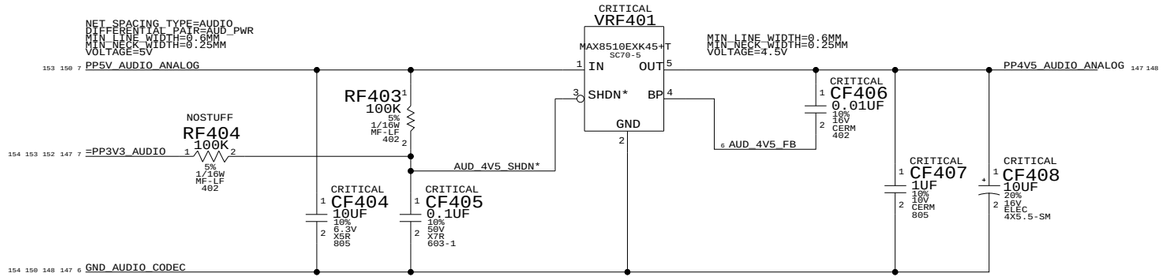
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

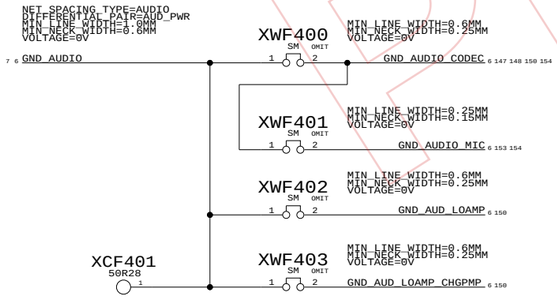
SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 153 OF 154	

4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP

APPLE P/N 353S0733



AUDIO GROUND RETURNS



PLACE ACROSS GROUND SPLIT

NOSTUFF
RF416
0
5%
1/8W
MF-LF
805
152 6 GND_AUDIO_SPKRAMP_PLANE
GND_AUDIO_CODEC 6 147 148 150 154

PLACE NEAR ENTRY TO SPEAKER AMP GROUND PLANE

NOSTUFF
RF417
0
5%
1/8W
MF-LF
805
152 7 6 GND_AUDIO_SPKRAMP

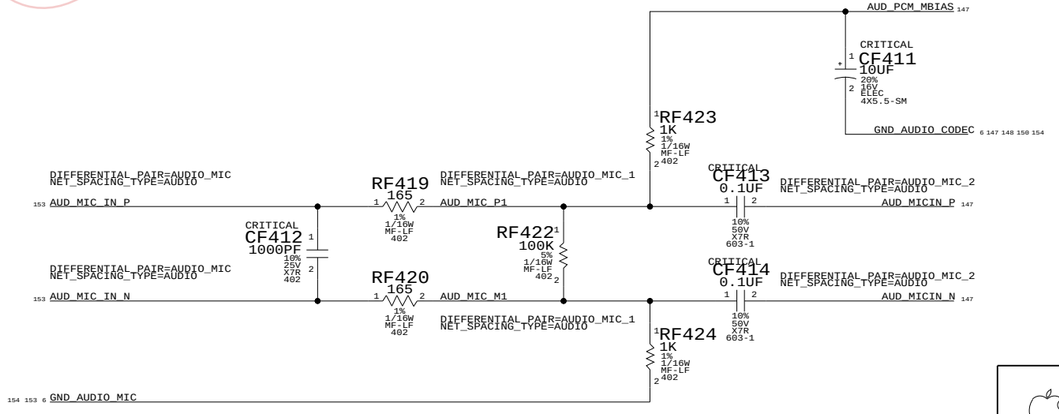
PLACE ACROSS GROUND SPLIT AT CODEC UE700

RF405
0
5%
1/8W
MF-LF
805
154 150 148 147 6 GND_AUDIO_CODEC

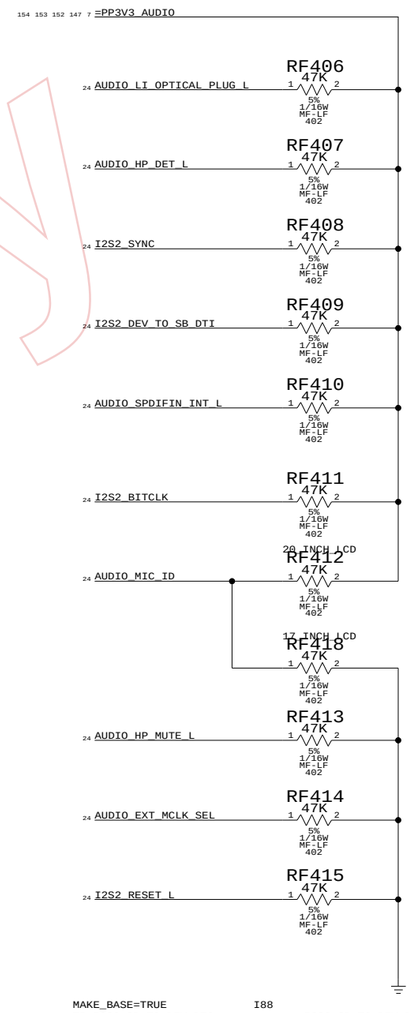
PLACE AT JF303

RF429
0
5%
1/8W
MF-LF
805
153 7 GND_CHASSIS_AUDIO_EXTERNAL

MICROPHONE IMPEDANCE MATCHING CIRCUIT



UNUSED GPIO TERMINATIONS



MAKE_BASE=TRUE I88
9 TP_I2S2_SB_TO_DEV_DTO — I2S2_SB_TO_DEV_DTO 24

MAKE_BASE=TRUE I89
6 NC_I2S2_MCLK — I2S2_MCLK 24

MAKE_BASE=TRUE I116
24 I2S0_MCLK — AUD_CODEC_MCLK 147

AUDIO: POWER SUPPLIES

SYNC_MASTER=FINO-SO SYNC_DATE=10/07/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE: NONE	SHT 154 OF 154	