1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

IMG5 20" REV F
11/01/05

REV	ZONE	ECN	DESC
F		408133	PRODUCTION RELEASED 11/01/05 ?

PDF	CSA	CONTENTS	SYNC	MASTER	DATE
2	2	System Block Diagram		FINO-M23	08/26/2005
3	4	Power Block Diagram		FINO-M23	08/26/2005
4	5	Table Items		FINO-M23	10/07/2005
5	6	FUNC TEST 1 OF 2		FINO-M23	08/26/2005
6	7	POWER CONN / ALIAS		M33-PC	06/20/2005
7	8	Signal Alias		FINO-M23	08/29/2005
8	9	FUNC TEST 2 OF 2		FINO-M23	08/26/2005
9	11	1.8V VREG		M33-PC	06/20/2005
10	12	1.5V Vreg		FINO-M23	10/07/2005
11	13	1.2V Vreg		FINO-M23	08/26/2005
12	15	2.5V Vreg		FINO-M23	08/26/2005
13	16	5V & 3.3V Fets		FINO-M23	08/26/2005
14	17	Vesta Core / Misc		FINO-M23	08/26/2005
15	19	KODIAK CORE & BYPASS		Q63	08/26/2005
16	20	KODIAK & SHASTA MISC		FINO-M23	08/26/2005
17	23	Shasta Core Power		Q63	08/26/2005
18	24	Shasta Serial / Misc		FINO-M23	08/26/2005
19	25	PULSAR2 POWER		Q63	08/26/2005
20	26	PULSAR2 CLOCKS		FINO-M23	08/26/2005
21	27	Pulsar Aliases		FINO-M23	08/26/2005
22	28	System Management Unit		Q63	08/26/2005
23	29	SMU SUPPLEMENTAL (2)		FINO-M23	09/20/2005
24	30	SMU SUPPLEMENTAL (3)		FINO-M23	09/20/2005
25	31	SMU SUPPLEMENTAL (4)		FINO-M23	08/26/2005
26	32	Fan 0, 1 & System Temp		FINO-M23	08/26/2005
27	33	Fan 2 & HD Temp		M33-HS	08/04/2005
28	39	I2C Connections		FINO-M23	08/26/2005
29	41	KODIAK EI PWR & CAPS		Q63	08/26/2005
30	42	KODIAK EI A		Q63	08/26/2005
31	43	CPU EI AND IO		FINO-M23	08/26/2005
32	44	KODIAK EI B		Q63	08/26/2005
33	47	CPU STRAPS		FINO-M23	08/26/2005
34	48	CPU POWER AND BYPASS		FINO-M23	08/26/2005
35	49	PROC DECOUPLING		FINO-M23	08/26/2005
36	50	CPU VCORE VREG		M33-HS	06/20/2005
37	52	CPU VCORE MORE BYPASS		FINO-M23	08/26/2005
38	54	CPU AVDD VREG		FINO-M23	10/07/2005
39	55	T,V,I SENSORS		FINO-M23	08/29/2005
40	56	CPU ALIASES & MISC		FINO-M23	08/26/2005
41	58	KODIAC NBMEM PWR & CAPS		Q63	08/26/2005
42	59	Kodiak Memory Dq/Ctl		FINO-M23	08/26/2005
43	61	Parallel Term		FINO-M23	08/26/2005
44	62	Main Memory Clock Buffer		FINO-M23	08/26/2005
45	63	MEMORY ADDR BRANCHING		FINO-M23	08/26/2005
46	67	Memory Dimm A		FINO-M23	08/26/2005
47	68	MLB Mem Series Term		FINO-M23	08/26/2005
48	69	On-Board DDR SDRAM		FINO-M23	08/26/2005
49	70	On-Board DDR SDRAM		FINO-M23	08/26/2005
50	82	KODIAK PCI-E X16		Q63	08/26/2005
51	84	GPU PCIe		FINO-M23	08/18/2005
52	85	Graphics Vregs		M33-DD	06/20/2005
53	86	GPU Core Power		FINO-M23	10/07/2005
54	87	GPU Frame Buffer		FINO-M23	10/07/2005
55	88	FB Series Termination		FINO-M23	08/26/2005
56	89	GPU GDDR SDRAM A		FINO-M23	10/07/2005
57	90	GPU GDDR SDRAM B		FINO-M23	10/07/2005
58	91	FB Parallel Termination		M33-DD	06/20/2005
59	92	GPU Straps		FINO-M23	08/26/2005
60	93	GPU DVI & DACs		FINO-M23	10/07/2005
61	96	TMDS / ExtVGA		M33-DD	06/20/2005
62	97	KODIAK PCI-E CONST		FINO-M23	08/26/2005
63	98	KODIAK HT16		Q63	08/26/2005
64	101	HT ALIASES		FINO-M23	08/26/2005
65	103	Shasta HyperTransport		Q63	08/26/2005
66	119	Shasta PCI Interface		Q63	08/26/2005
67	120	PCI SERIES TERMINATION		FINO-M23	08/26/2005
68	121	AIRPORT & BLUETOOTH		FINO-M23	08/26/2005
69	122	USB 2.0 PCI Interface		Q63	08/26/2005
70	125	BootROM		Q63	08/26/2005
71	127	Shasta Disk		M33-DC	06/20/2005
72	129	Disk Connectors		M33-DC	06/20/2005
73	130	ENET SERIES TERM		FINO-M23	08/26/2005
74	131	Shasta Ethernet		Q63	08/26/2005
75	132	Vesta Ethernet PHY		Q63	08/26/2005
76	136	ETHERNET CONNECTOR		FINO-M23	08/26/2005
77	138	Shasta FireWire		Q63	08/26/2005
78	139	Vesta FireWire PHY		Q63	08/26/2005
79	140	FIREWIRE CONNECTORS		FINO-M23	08/26/2005
80	142	USB Host Interfaces		FINO-M23	08/26/2005
81	143	USB Device Interfaces		FINO-M23	09/20/2005
82	144	Flash Media Ctrl		FINO-M23	09/27/2005
83	145	Flash Connector		FINO-M23	09/27/2005
84	147	AUDIO: CODEC		FINO-SO	10/07/2005
85	148	AUDIO: LINE INPUT AMP		FINO-SO	10/07/2005
86	150	AUDIO: LINE OUT AMP		FINO-SO	10/07/2005
87	152	AUDIO: SPEAKER AMP		FINO-SO	10/07/2005
88	153	AUDIO: CONNECTORS		FINO-SO	10/07/2005
89	154	AUDIO: POWER SUPPLIES		FINO-SO	10/07/2005

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

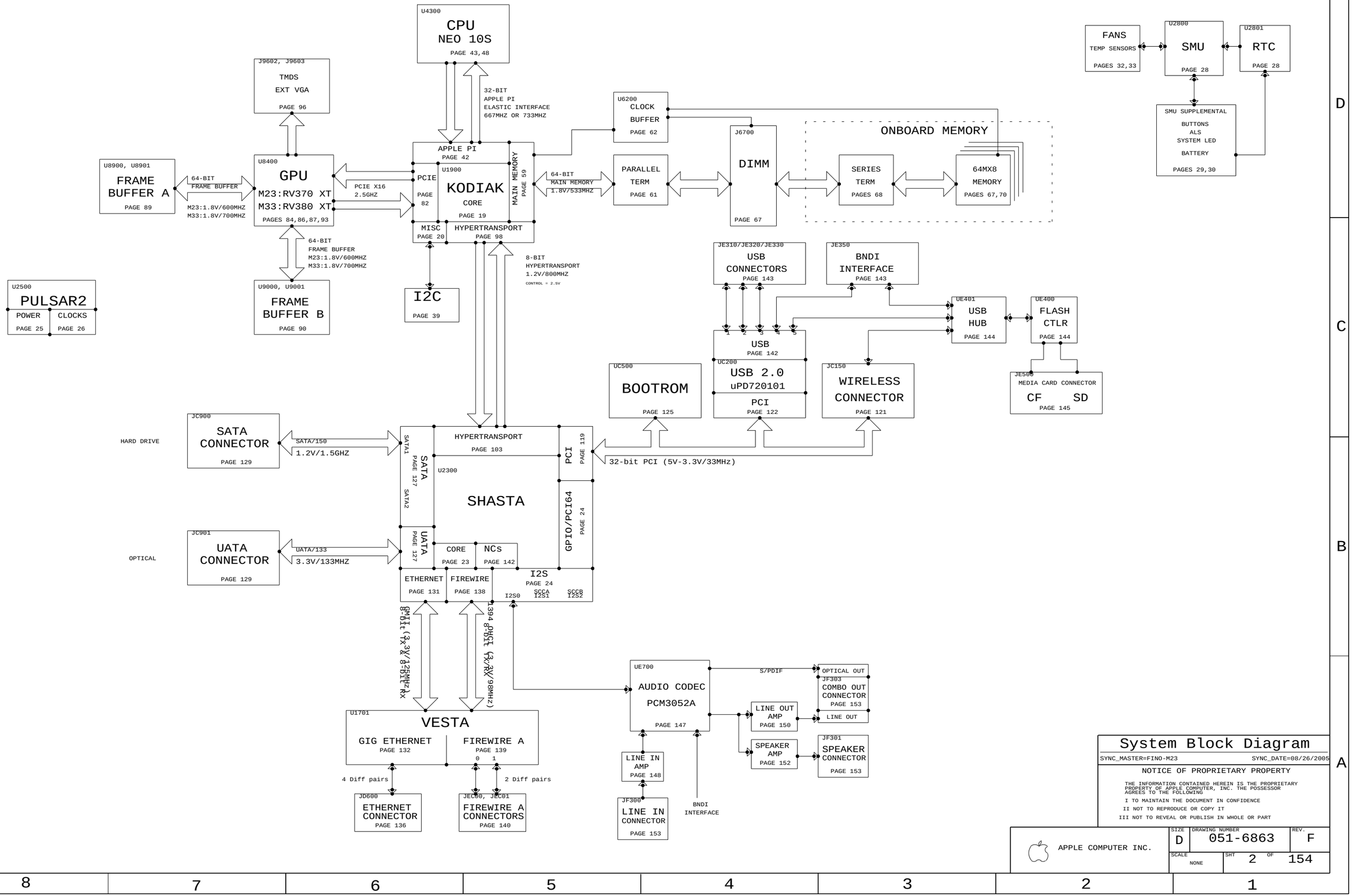
SIZE D

Apple Computer Inc.

TITLE
SCH,MLB,IMG5,20

DRAWING NUMBER 051-6863 REV. F

SHT 1 OF 154



System Block Diagram

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 2 OF 154	

POWER CONNECTOR

J700
PAGE 7

SYS_POWERUP_L

PP12V_ALL — FW CONN

PP12V_RUN — 20" PANEL POWER, 17" LCD INVERTER

PP5V_RUN — OPTICAL

PP5V_ALL

PP3V3_ALL

PP3V3_RUN — PCI BUS, AUDIO CODEC

SMU

POWER SEQUENCE PIN

- NC_SMU_PWRSEQ_P1_0 — SMU_PWRSEQ_P1_0
- NC_SMU_PWRSEQ_P1_4 — SMU_PWRSEQ_P1_4
- TURN_ON_PP1V2_L — SMU_PWRSEQ_P1_1
- PP3V3_PWRON: PWR_GOOD_PP1V5 — SMU_PWRSEQ_P9_5; PWR_GOOD_PP1V8 — SMU_PWRSEQ_P9_6
- TURN_ON_PP3V3_PWRON_L — SMU_PWRSEQ_P1_2
- SMU_PWRSEQ_P1_3

PP1V5_PWRON SWITCHER
PAGE 12
→ PULSAR, KODIAK CORE

PP1V5_RUN FET SWITCH
PAGE 12
→ EI

GPU CORE SWITCHER
PAGE 85

CPU CORE SWITCHER
PAGE 50

PP1V8_PWRON SWITCHER
PAGE 11
→ MAIN MEMORY

PP1V8_RUN POWER SW
PAGE 11
→ GPU MEMORY

PP0V9_GPU_VTT LINEAR
PAGE 91

PP4V5_RUN_AUDIO LINEAR
PAGE 154
→ AUDIO CODEC

PP5V_PWRON FET SWITCH
PAGE 16
→ USB CONN

PP2V5_ALL LINEAR
PAGE 15
→ VESTA

PP2V5_PWRON FET SWITCH
PAGE 15

PP2V5_RUN FET SWITCH
PAGE 15

PP3V3_PWRON FET SWITCH
PAGE 16
→ MODEM & BT, USB2 HOST

PP1V8_TPVDD LINEAR
PAGE 85

PP1V5_VDDC_CT LINEAR
PAGE 85

PP1V8_GPU LINEAR
PAGE 85

PP2V5_RUN_CPU_AVDD LINEAR
PAGE 54

PP2V5_GPU_A2VDD LINEAR
PAGE 85

PP1V2_TPVDD LINEAR
PAGE 85

PP1V2_PWRON FET SWITCH
PAGE 13
→ SHASTA CORE

PP1V2_RUN FET SWITCH
PAGE 13
→ HT BUS

PP1V2_ALL SWITCHER
PAGE 13
→ VESTA CORE

PP2V5_ALL
R431 10K 5% 1/16W MF-LF 402

PP1V5_PWRON
R430 100K 5% 1/10W MF-LF 402 — PS_1V_REF — COMPARE_PP1V5
C430 0.01UF 20% 16V CERM 402
U400 LM339A SOI-LF (V+, GND)

PP2V5_ALL
R442 150K 5% 1/16W MF-LF 402 — PS_1V_REF
PP5V_ALL
R443 100K 1% 1/10W MF-LF 402
R440 100K 5% 1/16W MF-LF 402 — COMPARE_PP1V8
C440 0.01UF 20% 16V CERM 402
U400 LM339A SOI-LF (V+, GND)
PP2V5_ALL
R441 10K 5% 1/16W MF-LF 402
C441 0.1UF 20% 16V CERM 402

PP2V5_ALL
U400P2
U400 LM339A SOI-LF (V+, GND)

Power Block Diagram

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 4 OF 154	

PROCESSORS

NEED TO UPDATED BIN CODES AS NOTES

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION	
337S3224	1	PROCESSOR	CBGA-576-1MM	IC,GPUL,DD3.1,1.9G,85C	1.9GHZ	1.10V	45W	50MV	U4300	17_INCH_LCD	CRITICAL
337S3220	1	PROCESSOR	CBGA-576-1MM	IC,GPUL,DD3.1,2.1G,85C	2.1GHZ	1.10V	45W	50MV	U4300	20_INCH_LCD	CRITICAL

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
337S3225	337S3224	17_INCH_LCD	U4300	IC,DD3.1,1.9G,1.15V
337S3226	337S3224	17_INCH_LCD	U4300	IC,DD3.1,1.9G,1.20V
337S3227	337S3224	17_INCH_LCD	U4300	IC,DD3.1,1.9G,1.25V
337S3228	337S3224	17_INCH_LCD	U4300	IC,DD3.0X,1.9G,1.15V
337S3229	337S3224	17_INCH_LCD	U4300	IC,DD3.0X,1.9G,1.20V
337S3230	337S3224	17_INCH_LCD	U4300	IC,DD3.0X,1.9G,1.25V
337S3231	337S3224	17_INCH_LCD	U4300	IC,DD3.0X,1.9G,1.30V
337S3221	337S3220	20_INCH_LCD	U4300	IC,DD3.1,2.1G,1.15V
337S3222	337S3220	20_INCH_LCD	U4300	IC,DD3.1,2.1G,1.20V
337S3223	337S3220	20_INCH_LCD	U4300	IC,DD3.1,2.1G,1.25V

ASICS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
343S0379	1	IC,KODIAK,V1.2,PBGA,200MM	U1900		CRITICAL
343S0377	1	IC,ASIC,SHASTA,V1.1,PBGA,LF	U2300		CRITICAL
343S0356	1	IC,ASIC,VESTA,V1.3,LF	U1701		CRITICAL
343S0319	1	IC,PULSAR2,100P,P8MM,BGA	U2500		CRITICAL

MISC PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION		
051-6790	1	PCB,SCHEM,MLB,M23	SCH1	17_INCH_LCD		
051-6863	1	PCB,SCHEM,MLB,M33	SCH1	20_INCH_LCD		
820-1783	1	PCB,FAB,MLB,M23	MLB1	17_INCH_LCD	CRITICAL	
820-1766	1	PCB,FAB,MLB,M33	MLB1	20_INCH_LCD	CRITICAL	
062-2082	1	SPEC,VENDOR PACKAGING PROCEDURE	VPP1			
825-6447	1	BARCODE LABEL, MLB	LBL1			
341T1751	1	IC,FLASH,1MX8,3.3V,90NS	UC500		CRITICAL	
341T1752	1	PURCH ASSY, SMU BIG	U2800		CRITICAL	
603-7318	1	M23 CPU HEATSINK	MECH1	OMIT	CRITICAL	
603-7321	1	M33 CPU HEATSINK	MECH1	OMIT	CRITICAL	
603-7319	1	M23 GPU HEATSINK	MECH2	OMIT	CRITICAL	HEATSINKS ARE NOW ON THE PD BOM
603-7322	1	M33 GPU HEATSINK	MECH2	OMIT	CRITICAL	
603-7320	1	M23 NB HEATSINK	MECH3	OMIT	CRITICAL	
603-7323	1	M33 NB HEATSINK	MECH3	OMIT	CRITICAL	
875-1905	1	CPU GAP FILLER	GAP1			
875-2429	1	LED COVER TAPE	TAPE1	17_INCH_LCD		

ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
378S0140	378S0141		LED700,LED702	KINGBRIGHT LED
343S0388	343S0356		U1701	VESTA A4
126S0078	126S0086		C722	EL CAP
126S0068	126S0088		CF000	EL CAP
353S1321	353S1105		U400	LM339
138S0558	138S0547			10UF CAP ALL LOC.
124-0338	124-0333			PANASONIC CAPS

Table Items

SYNC_MASTER=FINO-M23 SYNC_DATE=10/07/2005

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6863 | REV. F

SCALE NONE | SHT 5 OF 154

NO TEST XW NETS

U97	NO_TEST=YES	GND_U1100	11
U98	NO_TEST=YES	GND_U1200	12
U99	NO_TEST=YES	GND_U1300	13
U90	NO_TEST=YES	PP_2V5PWRONNBMISC	20
U91	NO_TEST=YES	PP_1V2PWRONSBVCORE	23
U92	NO_TEST=YES	PP_3V3PWRONSBPCI64	23
U93	NO_TEST=YES	PP_2V5PWRONSB	23
U95	NO_TEST=YES	PP_1V2PWRONSBPLL45VDD	24
U96	NO_TEST=YES	PP_OVDD_PULSAR1	25
U96	NO_TEST=YES	PP_1V2PWRONPULSAR1	25
U96	NO_TEST=YES	PP_1V5PULSAR2	25
U97	NO_TEST=YES	PP_1V5PWRONPULSAR2	25
U98	NO_TEST=YES	GND_SMU_AVSS	28 55
U98	NO_TEST=YES	PP_3V3ALLSMUAVCC	28
U99	NO_TEST=YES	PP_3V3ALLSMU	28
U91	NO_TEST=YES	PP_VEINB	41
U92	NO_TEST=YES	GND_CPU_AVDD	48
U93	NO_TEST=YES	VC_AGND	50
U93	NO_TEST=YES	VC_OUTSEN_R	50
U90	NO_TEST=YES	KPVDD2_FMAX	55
U90	NO_TEST=YES	GND_GPU_PVSS	86
U97	NO_TEST=YES	GND_GPU_MPVSS	87
U96	NO_TEST=YES	GND_AUDIO_MIC	153 154

U90	NO_TEST=YES	GND_GPU_TPVSS	93
U90	NO_TEST=YES	GND_GPU_TXVSSR	93
U92	NO_TEST=YES	GND_GPU_VSSDI	93
U90	NO_TEST=YES	GND_GPU_AVSSN	93
U90	NO_TEST=YES	GND_GPU_AVSSQ	93
U90	NO_TEST=YES	GND_GPU_A2VSSN	93
U90	NO_TEST=YES	GND_GPU_A2VSSQ	93
U90	NO_TEST=YES	KOD_L15_GND	98 101
U90	NO_TEST=YES	PP_3V3SBPCI_B9	
U90	NO_TEST=YES	PP_2V5PWRONSB_B9	119
U90	NO_TEST=YES	PP_VIOPCIUSB2_C2	122
U91	NO_TEST=YES	PP_1V2PWRONDISKSB_CC	127
U90	NO_TEST=YES	PP2V5_VESTA_BIASVDD1	132
U91	NO_TEST=YES	PP2V5_VESTA_XTALVDD1	132
U92	NO_TEST=YES	PP1V2_VESTA_PLLVDD1	132
U92	NO_TEST=YES	PP1V2_VESTA_PLLVDD2	139
U90	NO_TEST=YES	PP2V5_VESTA_BIASVDD2	139
U90	NO_TEST=YES	PP2V5_VESTA_XTALVDD2	139
U91	NO_TEST=YES	PP1V2_VESTA_FAVDDL	139
U90	NO_TEST=YES	PP2V5_VESTA_FAVDDM	139
U90	NO_TEST=YES	PP3V3_VESTA_FAVDDH	139
U90	NO_TEST=YES	PP3V3_PWRON_NEC_AVDD	142
U90	NO_TEST=YES	GND_AUD_LOAMP	150 154

U91	NO_TEST=YES	GND_NEC_AVSS_R	142
U90	NO_TEST=YES	GND_AUDIO_SPKRAMP_PLANE	152 154
U91	NO_TEST=YES	GND_AUDIO_CODEC	147 148 150 154
U91	NO_TEST=YES	KPGND2_FMAX	55
U91	NO_TEST=YES	TDIODE_POS_FMAX	55
U91	NO_TEST=YES	TDIODE_NEG_FMAX	55
U91	NO_TEST=YES	DAGND	55
U91	NO_TEST=YES	INA138_OUT	55
U90	NO_TEST=YES	RAMCLK_AVSS	62
U90	NO_TEST=YES	PP12V_AUDIO_SPKRAMP	7 152
U90	NO_TEST=YES	GND_AUDIO	7 154
U90	NO_TEST=YES	GND_AUDIO_SPKRAMP	7 152 154
U91	NO_TEST=YES	KOD_H05_GND	82 97
U91	NO_TEST=YES	KOD_K07_GND	82 97
U91	NO_TEST=YES	KOD_G10_GND	82 97
U91	NO_TEST=YES	KOD_J13_GND	82 97
U91	NO_TEST=YES	KOD_L13_GND	82 97
U91	NO_TEST=YES	KOD_H08_GND	82 97
U91	NO_TEST=YES	PCIE_SLOTA_PRSNT_L	82 84
U91	NO_TEST=YES	U8500_GND	85
U91	NO_TEST=YES	GND_AUD_LOAMP_CHGPMP	150 154

EE IDENTIFIED NO TEST NETS

U95	NO_TEST=YES	NC_EI_NB_TO_CPU_B_CLK_P	56
U95	NO_TEST=YES	NC_EI_NB_TO_CPU_B_CLK_N	56
U95	NO_TEST=YES	NC_EI_NB_TO_CPU_B_AD<0..43>	56
U95	NO_TEST=YES	NC_EI_NB_TO_CPU_B_SR_P<0..1>	56
U96	NO_TEST=YES	NC_EI_NB_TO_CPU_B_SR_N<0..1>	56
U96	NO_TEST=YES	NC_EI_CPU_B_TO_NB_CLK_P	56
U96	NO_TEST=YES	NC_EI_CPU_B_TO_NB_CLK_N	56
U96	NO_TEST=YES	NC_EI_CPU_B_TO_NB_AD<0..43>	56
U96	NO_TEST=YES	NC_EI_CPU_B_TO_NB_SR_P<0..1>	56
U96	NO_TEST=YES	NC_EI_CPU_B_TO_NB_SR_N<0..1>	56

U96	NO_TEST=YES	NC_NB_CPU_A1_INT_L	56
U97	NO_TEST=YES	NC_NB_CPU_B0_INT_L	56
U97	NO_TEST=YES	NC_NB_CPU_B1_INT_L	56
U97	NO_TEST=YES	NC_CPU_A1_QACK_L	56
U97	NO_TEST=YES	NC_CPU_B0_QACK_L	56
U97	NO_TEST=YES	NC_CPU_B1_QACK_L	56
U97	NO_TEST=YES	NC_HT_MB_TO_NB_CAD_P<8..15>	101
U97	NO_TEST=YES	NC_HT_MB_TO_NB_CAD_N<8..15>	101
U97	NO_TEST=YES	NC_HT_NB_TO_MB_CAD_P<8..15>	101
U98	NO_TEST=YES	NC_HT_NB_TO_MB_CAD_N<8..15>	101
U10	NO_TEST=YES	NC_CLK_RAI_200M_N<0>	27
U10	NO_TEST=YES	NC_CLK_RAI_200M_P<0>	27
U10	NO_TEST=YES	NC_CLK_RAI_PCIEA_N<0>	27
U10	NO_TEST=YES	NC_CLK_RAI_PCIEA_P<0>	27
U10	NO_TEST=YES	NC_CLK_RAI_PCIEB_N<0>	27
U10	NO_TEST=YES	NC_CLK_RAI_PCIEB_P<0>	27
U10	NO_TEST=YES	NC_CLK_RAI_PCIEC_N<0>	27
U10	NO_TEST=YES	NC_CLK_RAI_PCIEC_P<0>	27
U10	NO_TEST=YES	NC_A_AVREG_0	82
U10	NO_TEST=YES	NC_A_AVREG_1	82
U10	NO_TEST=YES	NC_A_AVREG_2	82
U10	NO_TEST=YES	NC_CPU_B_APSYNC	27
U10	NO_TEST=YES	NC_EI_CPU_B_SYSCLK_N	27
U10	NO_TEST=YES	NC_EI_CPU_B_SYSCLK_P	27
U10	NO_TEST=YES	NC_HT_NB_TO_MB_CLK_N<1>	101
U10	NO_TEST=YES	NC_HT_NB_TO_MB_CLK_P<1>	101
U10	NO_TEST=YES	NC_J2904_11	29
U10	NO_TEST=YES	NC_J2904_12	29
U10	NO_TEST=YES	NC_NCV1009_1	55
U10	NO_TEST=YES	NC_NCV1009_2	55
U10	NO_TEST=YES	NC_NCV1009_3	55
U10	NO_TEST=YES	NC_NCV1009_4	55
U10	NO_TEST=YES	NC_NCV1009_5	55
U10	NO_TEST=YES	NC_NCV1009_ADJ	55
U10	NO_TEST=YES	NC_RAM_ARB0_REF25MHZ	27
U10	NO_TEST=YES	NC_RAM_ARB1_REF25MHZ	27
U10	NO_TEST=YES	NC_SMU_PWRSEQ_P1_0	4
U10	NO_TEST=YES	NC_SMU_PWRSEQ_P1_4	4

U11	NO_TEST=YES	RFBD<38>	88 89
U11	NO_TEST=YES	RFBD<37>	88 89
U11	NO_TEST=YES	RFBD<36>	88 89
U11	NO_TEST=YES	RFBD<34>	88 89
U11	NO_TEST=YES	RFBD<33>	88 89
U11	NO_TEST=YES	RFBD<32>	88 89
U11	NO_TEST=YES	RFBD<31>	88 89
U11	NO_TEST=YES	RFBD<30>	88 89
U11	NO_TEST=YES	RFBD<28>	88 89
U11	NO_TEST=YES	RFBD<27>	88 89
U11	NO_TEST=YES	RFBD<26>	88 89
U11	NO_TEST=YES	RFBD<25>	88 89
U11	NO_TEST=YES	RFBD<23>	88 89
U11	NO_TEST=YES	RFBD<22>	88 89
U11	NO_TEST=YES	RFBD<21>	88 89

U10	NO_TEST=YES	KPVDD2	48 50 55
U10	NO_TEST=YES	KPGND2	48 50 55
U10	NO_TEST=YES	CPU_DIODE_POS	48 55
U10	NO_TEST=YES	CPU_DIODE_NEG	48 55
U11	NO_TEST=YES	FMAXT_P	55
U11	NO_TEST=YES	FMAXT_M	55
U11	NO_TEST=YES	CORE_ISNS_P	55
U11	NO_TEST=YES	CORE_ISNS_M	55
U11	NO_TEST=YES	PPV_RUN_CPU_AVDD_R_L	48
U11	NO_TEST=YES	NC_CLK_RAI_GIGE_25MHZ	27
U11	NO_TEST=YES	NC_CLK_RAI_REFCLK_66M	27
U11	NO_TEST=YES	NC_CPU_B_TBEN_CLK_US	26
U11	NO_TEST=YES	NC_PMR_CLK_DIS_L	20
U11	NO_TEST=YES	NC_I2S2_MCLK	154
U11	NO_TEST=YES	NC_SATA_RXD_N2_C	129
U11	NO_TEST=YES	NC_SATA_RXD_P2_C	129
U11	NO_TEST=YES	NC_SATA_TXD_N2	129
U11	NO_TEST=YES	NC_SATA_TXD_P2	129
U11	NO_TEST=YES	TP_SB<29>	142
U11	NO_TEST=YES	TP_SB<28>	142
U11	NO_TEST=YES	TP_SB<27>	142
U11	NO_TEST=YES	TP_SB<26>	142
U11	NO_TEST=YES	TP_SB<25>	142
U11	NO_TEST=YES	TP_SB<24>	142
U11	NO_TEST=YES	TP_SB<23>	142
U11	NO_TEST=YES	TP_SB<22>	142
U11	NO_TEST=YES	TP_SB<21>	142
U11	NO_TEST=YES	TP_SB<20>	142
U11	NO_TEST=YES	TP_SB<19>	142
U11	NO_TEST=YES	TP_SB<18>	142
U11	NO_TEST=YES	TP_SB<17>	142
U11	NO_TEST=YES	TP_SB<16>	142
U11	NO_TEST=YES	TP_SB<15>	142
U11	NO_TEST=YES	TP_SB<14>	142
U11	NO_TEST=YES	TP_SB<13>	142
U11	NO_TEST=YES	TP_SB<12>	142
U11	NO_TEST=YES	TP_SB<11>	142
U11	NO_TEST=YES	TP_SB<10>	142
U11	NO_TEST=YES	TP_SB<9>	142
U11	NO_TEST=YES	TP_SB<8>	142
U11	NO_TEST=YES	TP_SB<7>	142
U11	NO_TEST=YES	TP_SB<6>	142
U11	NO_TEST=YES	TP_SB<5>	142
U11	NO_TEST=YES	TP_SB<4>	142
U11	NO_TEST=YES	TP_SB<3>	142
U11	NO_TEST=YES	TP_SB<2>	142
U11	NO_TEST=YES	TP_SB<1>	142
U11	NO_TEST=YES	TP_SB<0>	142
U11	NO_TEST=YES	RFBD<61>	88 89
U11	NO_TEST=YES	RFBD<60>	88 89
U11	NO_TEST=YES	RFBD<59>	88 89
U11	NO_TEST=YES	RFBD<57>	88 89
U11	NO_TEST=YES	RFBD<56>	88 89
U11	NO_TEST=YES	RFBD<54>	88 89
U11	NO_TEST=YES	RFBD<53>	88 89
U11	NO_TEST=YES	RFBD<52>	88 89
U11	NO_TEST=YES	RFBD<50>	88 89
U11	NO_TEST=YES	RFBD<49>	88 89
U11	NO_TEST=YES	RFBD<48>	88 89
U11	NO_TEST=YES	RFBD<47>	88 89
U11	NO_TEST=YES	RFBD<45>	88 89
U11	NO_TEST=YES	RFBD<44>	88 89
U11	NO_TEST=YES	RFBD<42>	88 89
U11	NO_TEST=YES	RFBD<41>	88 89
U11	NO_TEST=YES	RFBD<40>	88 89

U11	NO_TEST=YES	RFBD<126>	88 90
U12	NO_TEST=YES	RFBD<125>	88 90
U11	NO_TEST=YES	RFBD<124>	88 90
U12	NO_TEST=YES	RFBD<122>	88 90
U12	NO_TEST=YES	RFBD<121>	88 90
U12	NO_TEST=YES	RFBD<120>	88 90
U12	NO_TEST=YES	RFBD<118>	88 90
U12	NO_TEST=YES	RFBD<117>	88 90
U12	NO_TEST=YES	RFBD<116>	88 90
U12	NO_TEST=YES	RFBD<114>	88 90
U12	NO_TEST=YES	RFBD<113>	88 90
U12	NO_TEST=YES	RFBD<112>	88 90
U12	NO_TEST=YES	RFBD<110>	88 90
U12	NO_TEST=YES	RFBD<109>	88 90
U12	NO_TEST=YES	RFBD<108>	88 90
U12	NO_TEST=YES	RFBD<106>	88 90
U12	NO_TEST=YES	RFBD<105>	88 90
U12	NO_TEST=YES	RFBD<104>	88 90
U12	NO_TEST=YES	RFBD<102>	88 90
U12	NO_TEST=YES	RFBD<101>	88 90
U12	NO_TEST=YES	RFBD<100>	88 90
U12	NO_TEST=YES	RFBD<98>	88 90
U12	NO_TEST=YES	RFBD<97>	88 90
U12	NO_TEST=YES	RFBD<96>	88 90
U12	NO_TEST=YES	RFBD<95>	88 90
U12	NO_TEST=YES	RFBD<94>	88 90
U12	NO_TEST=YES	RFBD<92>	88 90
U12	NO_TEST=YES	RFBD<91>	88 90
U12	NO_TEST=YES	RFBD<90>	88 90
U12	NO_TEST=YES	RFBD<88>	88 90
U12	NO_TEST=YES	RFBD<87>	88 90
U12	NO_TEST=YES	RFBD<86>	88 90
U12	NO_TEST=YES	RFBD<85>	88 90
U12	NO_TEST=YES	RFBD<83>	88 90
U12	NO_TEST=YES	RFBD<82>	88 90
U12	NO_TEST=YES	RFBD<81>	88 90
U12	NO_TEST=YES	RFBD<79>	88 90
U12	NO_TEST=YES	RFBD<78>	88 90
U12	NO_TEST=YES	RFBD<76>	88 90
U12	NO_TEST=YES	RFBD<75>	88 90
U12	NO_TEST=YES	RFBD<74>	88 90
U12	NO_TEST=YES	RFBD<72>	88 90
U12	NO_TEST=YES	RFBD<71>	88 90
U12	NO_TEST=YES	RFBD<70>	88 90
U12	NO_TEST=YES	RFBD<69>	88 90
U12	NO_TEST=YES	RFBD<67>	88 90
U12	NO_TEST=YES	RFBD<66>	88 90
U12	NO_TEST=YES	RFBD<65>	88 90
U12	NO_TEST=YES	RFBD<62>	88 90

U80	NO_TEST=YES	TP_FBBCS1_L	87
U82	NO_TEST=YES	AUD_4V5_FB	154
U83	NO_TEST=YES	ITS_RUNNING	7
U83	NO_TEST=YES	LED801_1	8
U83	NO_TEST=YES	LED802_1	8
U84	NO_TEST=YES	PCI_CLK66M_SB_INT_R	26
U84	NO_TEST=YES	Q800_D	8
U84	NO_TEST=YES	Q800_G	8
U84	NO_TEST=YES	Q801_B	8
U84	NO_TEST=YES	Q802_B	8
U85	NO_TEST=YES	Q802_E	8
U85	NO_TEST=YES	Q803_B	8
U42	NO_TEST=YES	TP_USB2_PWREN<0>	143
U42	NO_TEST=YES	TP_USB2_PWREN<1>	143
U87	NO_TEST=YES	TP_SB_FSTEST	24
U87	NO_TEST=YES	TP_SB_PLLTEST	24
U84	NO_TEST=YES	TP_USB2_PWREN<2>	143
U84	NO_TEST=YES	TP_USB2_PWREN<3>	143
U84	NO_TEST=YES	TP_USB2_PWREN<4>	143
U83	NO_TEST=YES	TP_NEC_NTEST1	122
U83	NO_TEST=YES	TP_NEC_SMC	122
U83	NO_TEST=YES	TP_NEC_SMI_L	122
U84	NO_TEST=YES	TP_NEC_SRCLK	122
U83	NO_TEST=YES	TP_NEC_SRMOD	122
U83	NO_TEST=YES	TP_NEC_TEST	122
U88	NO_TEST=YES	UATA_DASP_L_DS	129
U12	NO_TEST=YES	RFBD<19>	88 89
U12	NO_TEST=YES	RFBD<18>	88 89
U12	NO_TEST=YES	RFBD<16>	88 89
U12	NO_TEST=YES	RFBD<15>	88 89
U12	NO_TEST=YES	RFBD<14>	88 89
U12	NO_TEST=YES	RFBD<13>	88 89
U12	NO_TEST=YES	RFBD<11>	88 89
U12	NO_TEST=YES	RFBD<10>	88 89
U12	NO_TEST=YES	RFBD<8>	88 89
U12	NO_TEST=YES	RFBD<7>	88 89
U12	NO_TEST=YES	RFBD<6>	88 89
U12	NO_TEST=YES	RFBD<5>	88 89
U12	NO_TEST=YES	RFBD<3>	88 89
U12	NO_TEST=YES	RFBD<2>	88 89
U12	NO_TEST=YES	RFBD<1>	88 89
U12	NO_TEST=YES	RAM_DQ_R<63>	61 68 70
U12	NO_TEST=YES	RAM_DQ_R<60>	61 68 70
U12	NO_TEST=YES	RAM_DQ_R<59>	61 68 70
U12	NO_TEST=YES	RAM_DQ_R<58>	61 68 70
U12	NO_TEST=YES	RAM_DQ_R<57>	61 68 70
U12	NO_TEST=YES	RAM_DQ_R<56>	61 68 70
U12	NO_TEST=YES	RAM_DQ_R<54>	61 68 70
U12	NO_TEST=YES	RAM_DQ_R<53>	61 68 70
U12	NO_TEST=YES	RAM_DQ_R<52>	61 68 70
U12	NO_TEST=YES	RAM_DQ_R<50>	61 68 70
U12	NO_TEST=YES	RAM_DQ_R<49>	61 68 70
U12	NO_TEST=YES	RAM_DQ_R<48>	61 68 70
U12	NO_TEST=YES	RAM_DQ_R<46>	61 68 70
U13	NO_TEST=YES	RAM_DQ_R<45>	61 68 70
U13	NO_TEST=YES	RAM_DQ_R<44>	61 68 70
U13	NO_TEST=YES	RAM_DQ_R<43>	61 68 70
U13	NO_TEST=YES	RAM_DQ_R<41>	61 68 70
U13	NO_TEST=YES	RAM_DQ_R<40>	61 68 70
U13	NO_TEST=YES	RAM_DQ_R<37>	61 68 70
U13	NO_TEST=YES	RAM_DQ_R<38>	61 68 70
U13	NO_TEST=YES	RAM_DQ_R<36>	61 68 70
U13	NO_TEST=YES	RAM_DQ_R<34>	61 68 70
U13	NO_TEST=YES	RAM_DQ_R<33>	61 68 70
U13	NO_TEST=YES	RAM_DQ_R<32>	61 68 70
U13	NO_TEST=YES	RAM_DQ_R<30>	61 68 69
U13	NO_TEST=YES	RAM_DQ_R<29>	61 68 69
U13	NO_TEST=YES	RAM_DQ_R<28>	61 68 69
U13	NO_TEST=YES	RAM_DQ_R<31>	61 68 69
U13	NO_TEST=YES	RAM_DQ_R<25>	61 68 69
U13	NO_TEST=YES	RAM_DQ_R<24>	61 68 69
U13	NO_TEST=YES	RAM_DQ_R<22>	61 68 69
U13	NO_TEST=YES	RAM_DQ_R<21>	61 68 69
U13	NO_TEST=YES	RAM_DQ_R<20>	61 68 69
U13	NO_TEST=YES	RAM_DQ_R<19>	61 68 69
U13	NO_TEST=YES	RAM_DQ_R<17>	61 68 69
U13	NO_TEST=YES	RAM_DQ_R<16>	61 68 69
U13	NO_TEST=YES	RAM_DQ_R<14>	61 68 69
U13	NO_TEST=YES	RAM_DQ_R<13>	61 68 69
U13	NO_TEST=YES	RAM_DQ_R<12>	61 68 69
U13	NO_TEST=YES	RAM_DQ_R<11>	61 68 69

U13	NO_TEST=YES	RAM_DQ_R<9>	61 68 69
U13	NO_TEST=YES	RAM_DQ_R<8>	61 68 69
U13	NO_TEST=YES	RAM_DQ_R<7>	61 68 69
U13	NO_TEST=YES	RAM_DQ_R<6>	61 68 69
U13	NO_TEST=YES	RAM_DQ_R<5>	61 68 69
U13	NO_TEST=YES	RAM_DQ_R<3>	61 68 69
U13	NO_TEST=YES	RAM_DQ_R<2>	61 68 69
U13	NO_TEST=YES	RAM_DQ_R<1>	61 68 69

FUNC TEST NETS

NOTES FROM TOM FUSSELMAN

PLACE TWO TEST POINTS ON TOP SIDE
FOR PP3V3_ALL AND GND
PLACE WITHIN 1 INCH OF EACH OTHER
USE FAT TRACES

U10	FUNC_TEST=TRUE	PPVCORE_CPU	50
U10	FUNC_TEST=TRUE	=PP3V3_ALL_SMU	7 28 29
U10	FUNC_TEST=TRUE	=PP5V_RUN_CPU	7 8
U10	FUNC_TEST=TRUE	SYS_POWER_BUTTON_L	28 29
U10	FUNC_TEST=TRUE	POWER_BUTTON_L	29
U10	FUNC_TEST=TRUE	RESET_BUTTON_L	29
U10	FUNC_TEST=TRUE	SMU_RESET_L	28 29
U10	FUNC_TEST=TRUE	SYS_POWERUP_L	7 12 28 50 85

TOP SIDE ONLY

U10	FUNC_TEST=TRUE	SMU_BOOT_SCLK	28 29
U10	FUNC_TEST=TRUE	SMU_BOOT_RXD	28 29
U10	FUNC_TEST=TRUE	SMU_BOOT_CE	28 29
U10	FUNC_TEST=TRUE	SMU_BOOT_CNVSS	28 29
U10	FUNC_TEST=TRUE	SMU_BOOT_TXD	28 29
U10	FUNC_TEST=TRUE	SMU_BOOT_BUSY	28 29
U10	FUNC_TEST=TRUE	SMU_MANUAL_RESET_L	29

PP1V2_ALL PP3V3_ALL PP5V_ALL

7 PP1V2_ALL FUNC_TEST=TRUE
7 PP3V3_ALL FUNC_TEST=TRUE
7 PP5V_ALL FUNC_TEST=TRUE

PP1V8_RUN PP2V5_RUN PP3V3_RUN PP12V_RUN

7 PP1V8_RUN FUNC_TEST=TRUE
7 PP2V5_RUN FUNC_TEST=TRUE
16 7 PP3V3_RUN FUNC_TEST=TRUE
7 PP12V_RUN FUNC_TEST=TRUE

PP1V5_PWRON

7 PP1V5_PWRON FUNC_TEST=TRUE

GND FUNC_TEST=TRUE

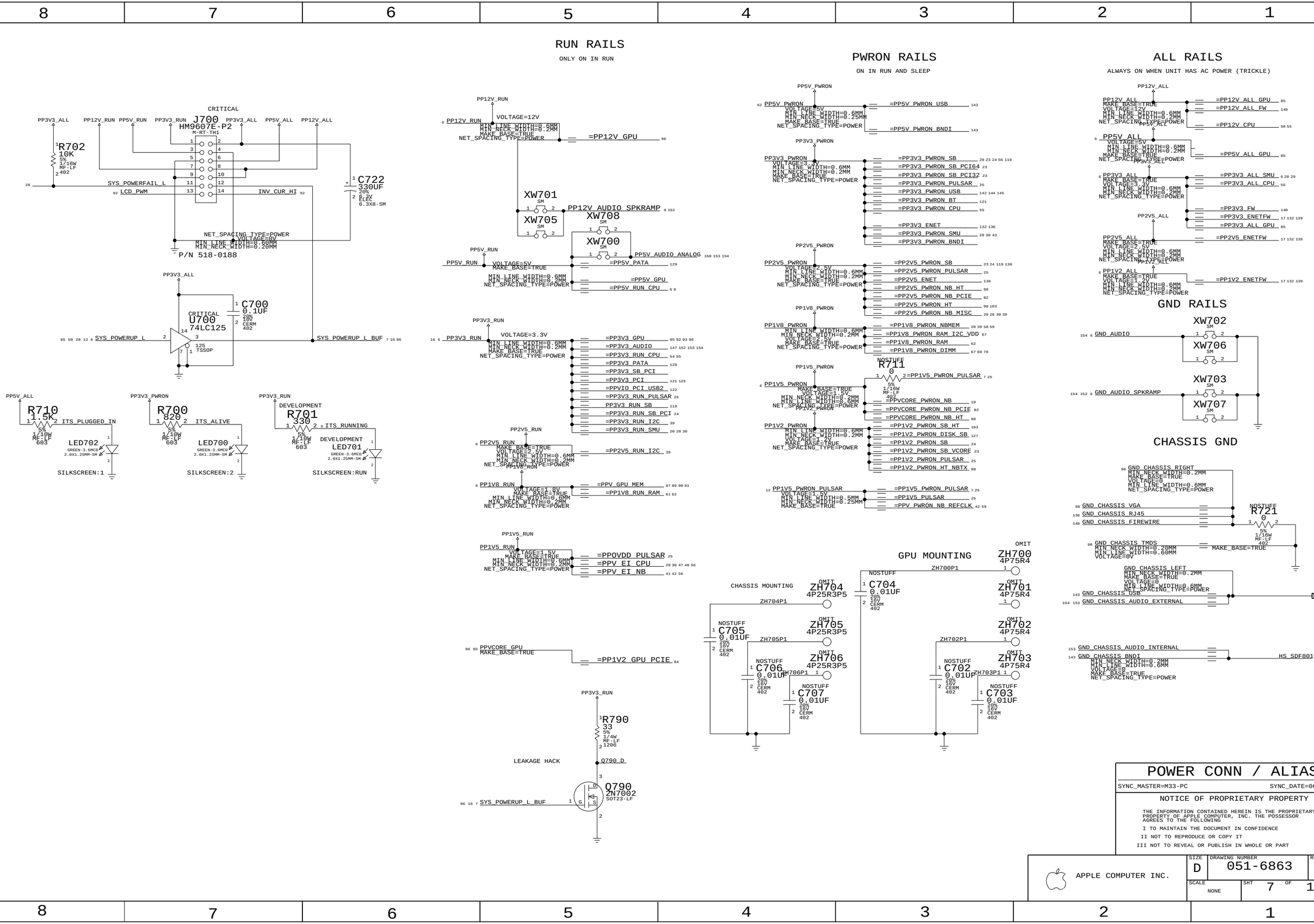
FUNC TEST 1 OF 2

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE COMPUTER INC.

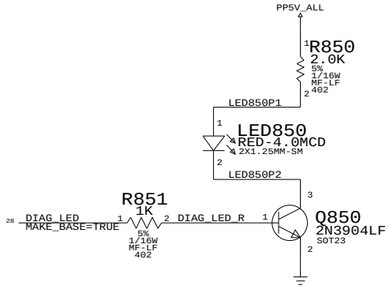
SIZE	DRAWING NUMBER	REV.
D	051-6863	F

SCALE NONE SHT 6 OF 154

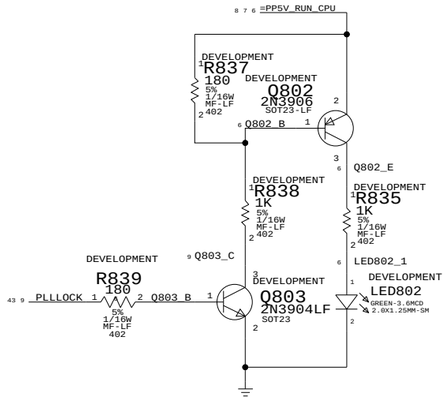

RUN RAILS
ONLY ON IN RUN
PWRON RAILS
ON IN RUN AND SLEEP
ALL RAILS
ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)
GND RAILS
CHASSIS GND
CRITICAL
J700
HM9607E-P2
M-RT-TH1
R702
10K
C722
330UF
C700
0.1UF
U700
74LC125
SYS_POWERFAIL_L
LCD_PWM
INV_CUR_HI
SYS_POWERUP_L
SYS_POWERUP_L_BUF
P/N 518-0188
R710
1.5K
LED702
ITS_PLUGGED_IN
SILKSCREEN:1
R700
820
LED700
ITS_ALIVE
SILKSCREEN:2
DEVELOPMENT
R701
330
LED701
ITS_RUNNING
SILKSCREEN:RUN
XW701
XW705
XW708
XW700
PP12V_AUDIO_SPKRAMP
PP5V_AUDIO_ANALOG
=PP12V_GPU
=PP5V_PATA
=PP5V_GPU
=PP5V_RUN_CPU
=PP3V3_GPU
=PP3V3_AUDIO
=PP3V3_RUN_CPU
=PP3V3_PATA
=PP3V3_SB_PCI
=PP3V3_PCI
=PPVIO_PCI_USB2
=PP3V3_RUN_PULSAR
PP3V3_RUN_SB
=PP3V3_RUN_SB_PCI
=PP3V3_RUN_I2C
=PP3V3_RUN_SMU
=PP2V5_RUN_I2C
=PPV_GPU_MEM
=PP1V8_RUN_RAM
=PPOVDD_PULSAR
=PPV_EI_CPU
=PPV_EI_NB
=PP1V2_GPU_PCIE
LEAKAGE HACK
R790
33
Q790
2N7002
Q790_D
SYS_POWERUP_L_BUF
PP5V_PWRON
=PP5V_PWRON_USB
=PP5V_PWRON_BNDI
PP3V3_PWRON
=PP3V3_PWRON_SB
=PP3V3_PWRON_SB_PCI64
=PP3V3_PWRON_SB_PCI32
=PP3V3_PWRON_PULSAR
=PP3V3_PWRON_USB
=PP3V3_PWRON_BT
=PP3V3_PWRON_CPU
=PP3V3_ENET
=PP3V3_PWRON_SMU
=PP3V3_PWRON_BNDI
PP2V5_PWRON
=PP2V5_PWRON_SB
=PP2V5_PWRON_PULSAR
=PP2V5_ENET
=PP2V5_PWRON_NB_HT
=PP2V5_PWRON_NB_PCIE
=PP2V5_PWRON_HT
=PP2V5_PWRON_NB_MISC
PP1V8_PWRON
=PP1V8_PWRON_NBMEM
=PP1V8_PWRON_RAM_I2C_VDD
=PP1V8_PWRON_RAM
=PP1V8_PWRON_DIMM
NOSTUFF
R711
0
=PP1V5_PWRON_PULSAR
PP1V5_PWRON
=PPVCORE_PWRON_NB
=PPVCORE_PWRON_NB_PCIE
=PPVCORE_PWRON_NB_HT
PP1V2_PWRON
=PP1V2_PWRON_SB_HT
=PP1V2_PWRON_DISK_SB
=PP1V2_PWRON_SB
=PP1V2_PWRON_SB_VCORE
=PP1V2_PWRON_PULSAR
=PP1V2_PWRON_HT_NBTX
=PP1V5_PWRON_PULSAR
=PP1V5_PULSAR
=PPV_PWRON_NB_REFCLK
PP12V_ALL
=PP12V_ALL_GPU
=PP12V_ALL_FW
=PP12V_CPU
PP5V_ALL
=PP5V_ALL_GPU
PP3V3_ALL
=PP3V3_ALL_SMU
=PP3V3_ALL_CPU
=PP3V3_FW
PP2V5_ALL
=PP3V3_ENETFW
=PP3V3_ALL_GPU
=PP2V5_ENETFW
PP1V2_ALL
=PP1V2_ENETFW
GND_AUDIO
GND_AUDIO_SPKRAMP
XW702
XW706
XW703
XW707
GND_CHASSIS_RIGHT
GND_CHASSIS_VGA
GND_CHASSIS_RJ45
GND_CHASSIS_FIREWIRE
R721
GND_CHASSIS_TMDS
GND_CHASSIS_LEFT
GND_CHASSIS_USB
GND_CHASSIS_AUDIO_EXTERNAL
GND_CHASSIS_AUDIO_INTERNAL
GND_CHASSIS_BNDI
HS_SDF801
GPU MOUNTING
CHASSIS MOUNTING
ZH700
ZH704
ZH705
ZH706
ZH701
ZH702
ZH703
C704
C705
C706
C707
C702
C703
0.01UF
POWER CONN / ALIAS
SYNC_MASTER=M33-PC
SYNC_DATE=06/20/2005
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
APPLE COMPUTER INC.
SIZE
D
DRAWING NUMBER
051-6863
REV.
F
SCALE
NONE
SHT
7
OF
154

DIAG LED

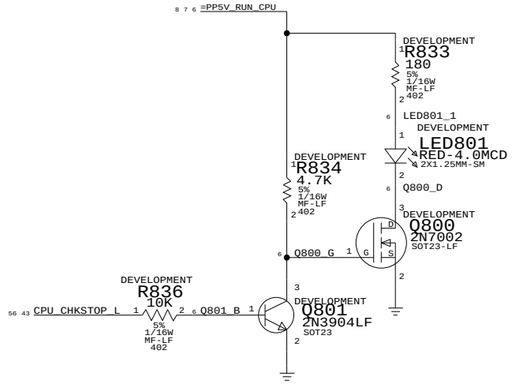
(OVERTEMP LED)



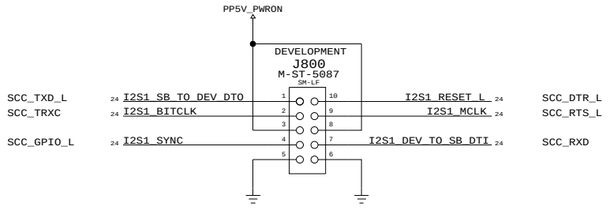
PLL LOCK LED



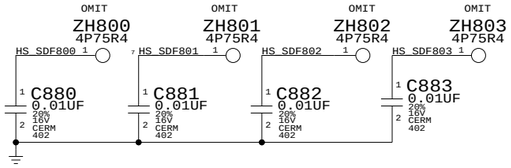
CHKSTOP LED



SERIAL DEBUG



CPU HEATSINK MOUNTING HOLES



Signal Alias

SYNC_MASTER=FINO-M23 SYNC_DATE=08/29/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 8 OF 154	

8	7	6	5	4	3	2	1	
D								D
C								C
B								B
A								A
8	7	6	5	4	3	2	1	

I1	NO_TEST=YES	ENET_TXD_R<7>	130 131
I2	NO_TEST=YES	ENET_TXD_R<6>	130 131
I3	NO_TEST=YES	ENET_TXD_R<5>	130 131
I4	NO_TEST=YES	ENET_TXD_R<4>	130 131
I5	NO_TEST=YES	ENET_TXD_R<3>	130 131
I6	NO_TEST=YES	ENET_TXD_R<2>	130 131
I7	NO_TEST=YES	ENET_TXD_R<1>	130 131
I8	NO_TEST=YES	ENET_TXD_R<0>	130 131
I9	NO_TEST=YES	ENET_TXD<7>	130 131 132
I10	NO_TEST=YES	ENET_TXD<6>	130 131 132
I12	NO_TEST=YES	ENET_TXD<5>	130 131 132
I11	NO_TEST=YES	ENET_TXD<4>	130 131 132
I13	NO_TEST=YES	ENET_TXD<3>	130 131 132
I14	NO_TEST=YES	ENET_TXD<2>	130 131 132
I15	NO_TEST=YES	ENET_TXD<1>	130 131 132
I16	NO_TEST=YES	ENET_TXD<0>	130 131 132
I18	NO_TEST=YES	ENET_RXD_R<7>	130 131 132
I17	NO_TEST=YES	ENET_RXD_R<6>	130 131 132
I19	NO_TEST=YES	ENET_RXD_R<5>	130 131 132
I20	NO_TEST=YES	ENET_RXD_R<4>	130 131 132
I21	NO_TEST=YES	ENET_RXD_R<3>	130 131 132
I22	NO_TEST=YES	ENET_RXD_R<2>	130 131 132
I24	NO_TEST=YES	ENET_RXD_R<1>	130 131 132
I23	NO_TEST=YES	ENET_RXD_R<0>	130 131 132
I25	NO_TEST=YES	ENET_RXD<7>	130 131
I26	NO_TEST=YES	ENET_RXD<6>	130 131
I27	NO_TEST=YES	ENET_RXD<5>	130 131
I28	NO_TEST=YES	ENET_RXD<4>	130 131
I30	NO_TEST=YES	ENET_RXD<3>	130 131
I29	NO_TEST=YES	ENET_RXD<2>	130 131
I31	NO_TEST=YES	ENET_RXD<1>	130 131
I32	NO_TEST=YES	ENET_RXD<0>	130 131
I33	NO_TEST=YES	ENET_TX_EN_R	130 131
I34	NO_TEST=YES	ENET_TX_ER_R	130 131
I36	NO_TEST=YES	ENET_TX_EN	130 131 132
I35	NO_TEST=YES	ENET_TX_ER	130 131 132
I37	NO_TEST=YES	TP_HT_MB_TO_NB_CLK_N<1>	101
I38	NO_TEST=YES	TP_HT_MB_TO_NB_CLK_P<1>	101
I39	NO_TEST=YES	NC_CPU_AFN	56
I40	NO_TEST=YES	NC_I2C_SMU_CPU_SCL_IN	31
I42	NO_TEST=YES	NC_PSRO	56
I41	NO_TEST=YES	NC_PSRO_ENABLE	56
I43	NO_TEST=YES	NC_SLOT_TOTAL_PWR	31
I44	NO_TEST=YES	NC_SMU_CPU_VID_LE0	31
I45	NO_TEST=YES	NC_SMU_CPU_VID_LE1	31
I46	NO_TEST=YES	NC_SMU_FAN_RPM3	31
I48	NO_TEST=YES	NC_SMU_FAN_RPM4	31
I47	NO_TEST=YES	NC_SMU_FAN_RPM5	31
I49	NO_TEST=YES	NC_SMU_FAN_TACH3	31
I50	NO_TEST=YES	NC_SMU_FAN_TACH4	31
I51	NO_TEST=YES	NC_SMU_FAN_TACH5	31
I52	NO_TEST=YES	NC_SMU_FAN_TACH7	31
I54	NO_TEST=YES	NC_SMU_SER_SEL	31
I53	NO_TEST=YES	NC_SYS_DOOR_AJAR_L	31
I55	NO_TEST=YES	TP_VESTA_2_5V_EN	17
I56	NO_TEST=YES	TP_VESTA_AN_EN	132
I57	NO_TEST=YES	TP_VESTA_DNC_C9	17
I58	NO_TEST=YES	TP_VESTA_DNC_E9	17
I60	NO_TEST=YES	TP_VESTA_EN_10B	132
I59	NO_TEST=YES	TP_VESTA_ER	132
I61	NO_TEST=YES	TP_VESTA_F1000	132
I62	NO_TEST=YES	TP_VESTA_FDX	132
I63	NO_TEST=YES	TP_VESTA_FDXLED_L	132
I64	NO_TEST=YES	TP_VESTA_HUB	132
I66	NO_TEST=YES	TP_VESTA_LINK1_L	132
I65	NO_TEST=YES	TP_VESTA_LINK2_L	132
I67	NO_TEST=YES	TP_VESTA_MANMS	132
I68	NO_TEST=YES	TP_VESTA_PHYA<0>	132
I69	NO_TEST=YES	TP_VESTA_PHYA<1>	132
I70	NO_TEST=YES	TP_VESTA_PHYA<2>	132
I72	NO_TEST=YES	TP_VESTA_PHYA<3>	132
I71	NO_TEST=YES	TP_VESTA_PHYA<4>	132
I73	NO_TEST=YES	TP_VESTA_RBC0	132
I74	NO_TEST=YES	TP_VESTA_RBC1	132
I76	NO_TEST=YES	TP_VESTA_REGCTL1	17
I76	NO_TEST=YES	TP_VESTA_REGCTL2	17
I78	NO_TEST=YES	TP_VESTA_REGSEN1	17
I77	NO_TEST=YES	TP_VESTA_REGSEN2	17
I79	NO_TEST=YES	TP_VESTA_REGSUP1	17
I80	NO_TEST=YES	TP_VESTA_REGSUP2	17
I81	NO_TEST=YES	TP_VESTA_RGMIIEN	132
I82	NO_TEST=YES	TP_VESTA_SPD0	132
I84	NO_TEST=YES	TP_VESTA_TDBL<0>	139
I83	NO_TEST=YES	TP_VESTA_TDBL<1>	139
I85	NO_TEST=YES	TP_VESTA_TDBL<2>	139
I86	NO_TEST=YES	TP_VESTA_TEST<0>	132
I87	NO_TEST=YES	TP_VESTA_TEST<1>	132
I88	NO_TEST=YES	TP_VESTA_TEST_1394<0>	139
I90	NO_TEST=YES	TP_VESTA_TEST_1394<1>	139
I89	NO_TEST=YES	TP_VESTA_TVCO	132
I222	NO_TEST=YES	CARD_READER_ACTIVITY_R	144
I223	NO_TEST=YES	TP_VESTA_FAVDDL	139
I224	NO_TEST=YES	TP_NB_A_TRIGGER_OUT	56
I225	NO_TEST=YES	TP_NB_B_TRIGGER_OUT	56

I91	NO_TEST=YES	TP_VESTA_TVCO_24	139
I92	NO_TEST=YES	TP_VESTA_TXC_RXC_DELAY	132
I93	NO_TEST=YES	TP_I2S2_SB_TO_DEV_DTO	154
I94	NO_TEST=YES	TP_NB_APSYNC	44
I95	NO_TEST=YES	TP_SB_WATCHDOG	24
I96	NO_TEST=YES	NC_CPU_TBEN_CLK	
I97	NO_TEST=YES	NC_J3108_10	31
I98	NO_TEST=YES	NC_J3108_11	31
I99	NO_TEST=YES	NC_J3108_12	31
I100	NO_TEST=YES	NC_J3108_8	31
I101	NO_TEST=YES	NC_J3108_9	31
I102	NO_TEST=YES	NC_JTAGMUX_3	30
I103	NO_TEST=YES	NC_PP1V5_PULSAR	12

THE FOLLOWING NETS ARE USED ONLY
WHEN THE DEVELOPMENT BOM OPTION IS ENABLED

I109	NO_TEST=YES	Q803_C	8
I108	NO_TEST=YES	PLLLOCK	8 43

I113	NO_TEST=YES	LED_PP1V8_RUN_P	11
I117	NO_TEST=YES	LED_PP1V8_RUN_N	11
I118	NO_TEST=YES	PP1V5_RUN_FOR_LED	12
I115	NO_TEST=YES	LED_PP1V5_RUN_N	12
I116	NO_TEST=YES	LED_PP1V5_RUN_P	12
I119	NO_TEST=YES	PULSAR_1V5_RUN_SWITCH	12
I120	NO_TEST=YES	PP1V2_RUN_FOR_LED	13
I121	NO_TEST=YES	LED_PP1V2_RUN_N	13
I122	NO_TEST=YES	LED_PP1V2_RUN_P	13
I123	NO_TEST=YES	KP_V<1>	55
I124	NO_TEST=YES	KP_V<2>	55
I125	NO_TEST=YES	CPU_SENSE_KP_V	55
I126	NO_TEST=YES	NB_PLL_OUT_TRG_R	
I127	NO_TEST=YES	NB_PLL_OUT_TRG	59
I128	NO_TEST=YES	PP5V_T555	
I131	NO_TEST=YES	T555_DISC	
I130	NO_TEST=YES	T555_THRES	
I129	NO_TEST=YES	T555_OUT	
I132	NO_TEST=YES	T555_PWM	
I133	NO_TEST=YES	PP3V3_GPU_TSENSE	93
I134	NO_TEST=YES	TSENSE_GPU_OVERTEMP_L	93
I135	NO_TEST=YES	TSENSE_GPU_ADD0	93
I136	NO_TEST=YES	TSENSE_GPU_ADD1	93
I137	NO_TEST=YES	GPU_DIODE_PLUS	93
I138	NO_TEST=YES	GPU_DIODE_MINUS	93
I139	NO_TEST=YES	LED8700_P	136
I140	NO_TEST=YES	LED8701_P	136

THE FOLLOWING PULSAR NETS WILL BE
TESTED VIA TEST JET

I143	NO_TEST=YES	CPU_A_TBEN_CLK_R	26
I144	NO_TEST=YES	CPU_B_TBEN_CLK_R	26
I145	NO_TEST=YES	CPU_A_APSYNC_R	26
I146	NO_TEST=YES	CPU_B_APSYNC_R	26
I147	NO_TEST=YES	NB_APSYNC_R	26
I148	NO_TEST=YES	HT_SB_REFCLK_R	26
I149	NO_TEST=YES	HT_NB_REFCLK_H0_R	26
I150	NO_TEST=YES	HT_NB_REFCLK_L0_R	26
I151	NO_TEST=YES	CLK_RAIREF_200M_P_R	26
I152	NO_TEST=YES	CLK_RAIREF_200M_N_R	26
I153	NO_TEST=YES	NB_PMR_CLK_P_R	26
I155	NO_TEST=YES	NB_PMR_CLK_N_R	26
I154	NO_TEST=YES	NB_PCIE_REFCLK_P_C	26
I156	NO_TEST=YES	NB_PCIE_REFCLK_N_C	26
I158	NO_TEST=YES	GFX_SLOT_PCIE_REFCLK_P_C	26
I159	NO_TEST=YES	GFX_SLOT_PCIE_REFCLK_N_C	26
I157	NO_TEST=YES	PCIE_A_REFCLKIN_P_C	26
I160	NO_TEST=YES	PCIE_A_REFCLKIN_N_C	26
I161	NO_TEST=YES	PCIE_B_REFCLKIN_P_C	26
I162	NO_TEST=YES	PCIE_B_REFCLKIN_N_C	26
I163	NO_TEST=YES	PCIE_C_REFCLKIN_P_C	26
I164	NO_TEST=YES	PCIE_C_REFCLKIN_N_C	26
I165	NO_TEST=YES	NB_DDR_REFCLK_P_R	26
I166	NO_TEST=YES	NB_DDR_REFCLK_N_R	26
I167	NO_TEST=YES	CLK_RAI_GIGE_25MHZ_R	26
I168	NO_TEST=YES	QUA0_REF_25MHZ_R	26
I169	NO_TEST=YES	SB_CLK25M_SATA_R	26
I170	NO_TEST=YES	QUA1_REF_25MHZ_R	26
I171	NO_TEST=YES	PCI_CLK33M_SB_EXT_R	26
I172	NO_TEST=YES	SB_AIRPRT_CLK_33MHZ_R	26
I173	NO_TEST=YES	CLK_RAI_REFCLK_66M_R	26
I174	NO_TEST=YES	SB_USB2_CLK_33MHZ_R	26

THE FOLLOWING NETS DO NOT HAVE
TEST POINT BECAUSE OF ROUTING DENSITY
AND SIGNAL INTEGRITY.
TEST COVERAGE WILL BE BY FCT
NOTE FOR SHARING: DO NOT INCLUDE THIS LIST UNTIL
PCB LAYOUT ADDS TEST POINTS. THIS LIST IS A RESULT OF PCB
LAYOUT HAVING DIFFICULTY PLACING TEST POINTS ON THESE NETS

I177	NO_TEST=YES	100M_N<0>	82 97
I178	NO_TEST=YES	100M_P<0>	82 97
I179	NO_TEST=YES	CKA_N<0>	84 97
I180	NO_TEST=YES	CKA_P<0>	84 97
I177	NO_TEST=YES	HT_NB_N<0>	98 101
I178	NO_TEST=YES	HT_NB_P<0>	98 101
I179	NO_TEST=YES	HT_NB_REFCLK_NF<0>	98 101
I180	NO_TEST=YES	HT_NB_REFCLK_PF<0>	98 101
I185	NO_TEST=YES	HT_NB_TO_SB_CAD_N<0..7>	101
I187	NO_TEST=YES	HT_NB_TO_SB_CAD_P<0..7>	101
I186	NO_TEST=YES	HT_NB_TO_SB_CLK_P<0>	101
I188	NO_TEST=YES	HT_NB_TO_SB_CLK_N<0>	101
I189	NO_TEST=YES	HT_SB_TO_NB_CAD_N<0..7>	101
I190	NO_TEST=YES	HT_SB_TO_NB_CAD_P<0..7>	101
I187	NO_TEST=YES	HT_SB_TO_NB_CLK_P<0>	101
I189	NO_TEST=YES	HT_SB_TO_NB_CLK_N<0>	101
I188	NO_TEST=YES	PCIE_SLOTA_TO_NB_N<0..15>	9 82 84 97
I191	NO_TEST=YES	PCIE_SLOTA_TO_NB_P<0..15>	9 82 84 97
I192	NO_TEST=YES	UATA_DA<0>	127 129
I193	NO_TEST=YES	UATA_DD<1>	127 129
I194	NO_TEST=YES	UATA_DD<14>	127 129
I195	NO_TEST=YES	PCIE_NB_TO_SLOTA_N<0>	9 82 84 97
I196	NO_TEST=YES	PCIE_NB_TO_SLOTA_N<3>	9 82 84 97
I197	NO_TEST=YES	PCIE_NB_TO_SLOTA_NF<13>	9 82 97
I198	NO_TEST=YES	PCIE_NB_TO_SLOTA_NF<7>	9 82 97
I199	NO_TEST=YES	PCIE_NB_TO_SLOTA_P<1>	9 82 84 97
I200	NO_TEST=YES	PCIE_NB_TO_SLOTA_P<10>	9 82 84 97
I207	NO_TEST=YES	PCIE_NB_TO_SLOTA_PF<13>	9 82 97
I207	NO_TEST=YES	PCIE_NB_TO_SLOTA_PF<14>	9 82 97
I208	NO_TEST=YES	PCIE_NB_TO_SLOTA_NF<12>	9 82 97
I208	NO_TEST=YES	PCIE_NB_TO_SLOTA_PF<10>	9 82 97
I208	NO_TEST=YES	PCIE_NB_TO_SLOTA_PF<4>	9 82 97
I208	NO_TEST=YES	HT_MB_TO_NB_CTL_N<1>	98
I208	NO_TEST=YES	HT_NB_TO_MB_CTL_P<1>	98
I208	NO_TEST=YES	HT_NB_TO_MB_CTL_N<1>	98
I211	NO_TEST=YES	HT_NB_TO_MB_CTL_P<1>	98
I209	NO_TEST=YES	HT_NB_TO_SB_CTL_N<0>	101
I210	NO_TEST=YES	HT_SB_TO_NB_CTL_P<0>	101
I213	NO_TEST=YES	CLK_KOD_100M_NF<0>	82 97
I212	NO_TEST=YES	CLK_KOD_100M_PF<0>	82 97
I214	NO_TEST=YES	EI_CPU_TO_NB_CLK_N	43 56
I215	NO_TEST=YES	EI_CPU_TO_NB_CLK_P	43 56
I216	NO_TEST=YES	EI_CPU_TO_NB_SR_N<1>	9 43 56
I218	NO_TEST=YES	EI_CPU_TO_NB_SR_P<1>	9 43 56
I217	NO_TEST=YES	EI_NB_TO_CPU_CLK_N	43 56
I219	NO_TEST=YES	EI_NB_TO_CPU_CLK_P	43 56
I221	NO_TEST=YES	EI_NB_TO_CPU_SR_N<0>	9 43 56
I220	NO_TEST=YES	EI_NB_TO_CPU_SR_P<0>	9 43 56

I257	NO_TEST=YES	PLLTESTOUT	43 47
I258	NO_TEST=YES	UATA_DD<13>	127 129
I259	NO_TEST=YES	CPU_SPARE2	43 47
I260	NO_TEST=YES	RFBD<51>	88 89
I261	NO_TEST=YES	TP_CPU_TRIGGER_OUT	56
I262	NO_TEST=YES	UATA_DD<12>	127 129
I263	NO_TEST=YES	EI_CPU_SYSCLK_P	43 56
I264	NO_TEST=YES	EI_CPU_TO_NB_SR_N<1>	9 43 56
I265	NO_TEST=YES	EI_CPU_TO_NB_SR_P<1>	9 43 56
I266	NO_TEST=YES	EI_NB_TO_CPU_SR_N<0>	9 43 56
I267	NO_TEST=YES	EI_NB_TO_CPU_SR_P<0>	9 43 56

JTAG TEST POINTS NEED TO BE ON THE BOTTOM
OF THE BOARD
ADDING FUNC_TEST=TRUE TO THESE NETS

I820	FUNC_TEST=TRUE	TP_JTAG_SB_TCK	20
I822	FUNC_TEST=TRUE	TP_JTAG_SB_TDI	20
I822	FUNC_TEST=TRUE	TP_JTAG_SB_TDO	20
I824	FUNC_TEST=TRUE	TP_JTAG_SB_TMS	20
I830	FUNC_TEST=TRUE	JTAG_SB_TRST_L	20 24

I832	FUNC_TEST=TRUE	JTAG_NB_TCK	20 30
I834	FUNC_TEST=TRUE	JTAG_NB_TDI	20 30
I833	FUNC_TEST=TRUE	JTAG_NB_TDO	20 30
I836	FUNC_TEST=TRUE	JTAG_NB_TMS	20 30
I831	FUNC_TEST=TRUE	JTAG_NB_TRST_L	20

I838	FUNC_TEST=TRUE	TP_JTAG_VESTA_TDI	17
I840	FUNC_TEST=TRUE	TP_JTAG_VESTA_TDO	17
I839	FUNC_TEST=TRUE	TP_JTAG_VESTA_TCK	17
I842	FUNC_TEST=TRUE	TP_JTAG_VESTA_TMS	17
I843	FUNC_TEST=TRUE	TP_JTAG_VESTA_TRST_L	17

I844	FUNC_TEST=TRUE	JTAG_CPU_TCK	30 43
I846	FUNC_TEST=TRUE	JTAG_CPU_TDI	30 43
I845	FUNC_TEST=TRUE	JTAG_CPU_TDO	30 43 47
I848	FUNC_TEST=TRUE	JTAG_CPU_TMS	30 43
I847	FUNC_TEST=TRUE	JTAG_CPU_TRST_L	43 47

ADDING NO_TEST TO ALL PCIE NETS
TO AVOID STUBS
WILL GET COVERAGE IN FCT WITH A DIAG
THAT CHECKS THAT THE BUS IS 16 LANES WIDE

I240	NO_TEST=YES	PCIE_NB_TO_SLOTA_NF<0..15>	9 82 97
I250	NO_TEST=YES	PCIE_NB_TO_SLOTA_PF<0..15>	9 82 97
I251	NO_TEST=YES	PCIE_NB_TO_SLOTA_N<0..15>	9 82 84 97
I252	NO_TEST=YES	PCIE_NB_TO_SLOTA_P<0..15>	9 82 84 97
I253	NO_TEST=YES	PCIE_SLOTA_TO_NB_NF<0..15>	84 97
I254	NO_TEST=YES	PCIE_SLOTA_TO_NB_PF<0..15>	84 97
I255	NO_TEST=YES	PCIE_SLOTA_TO_NB_N<0..15>	9 82 84 97
I256	NO_TEST=YES	PCIE_SLOTA_TO_NB_P<0..15>	9 82 84 97

FUNC TEST 2 OF 2

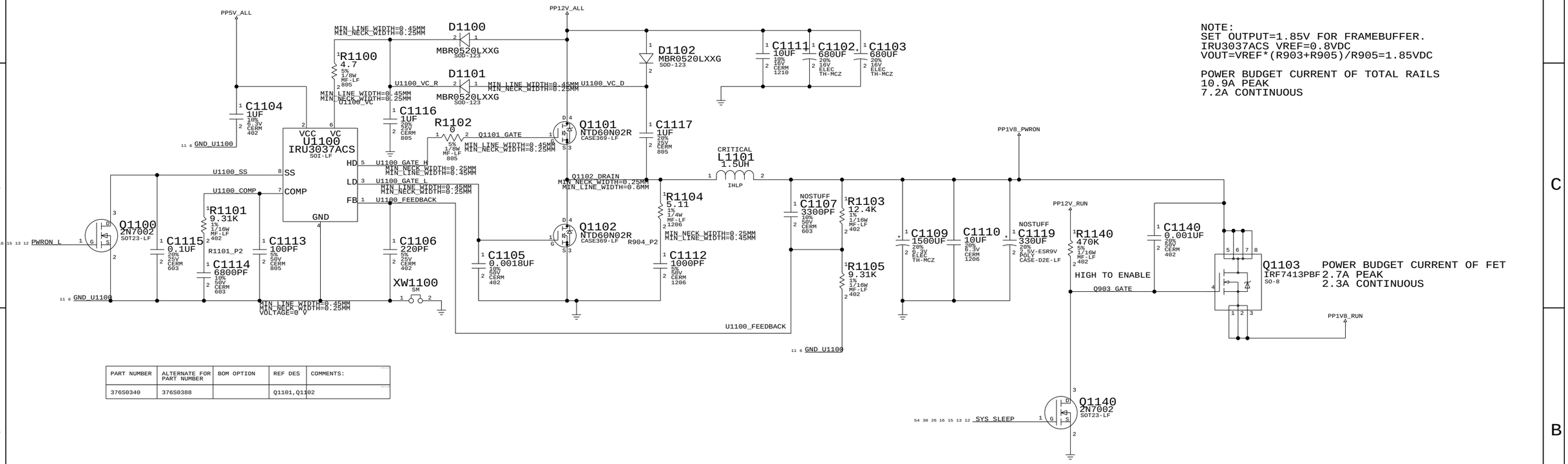
SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F

SCALE	SHT	OF
NONE	9	154

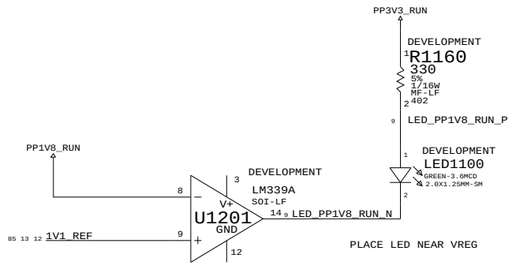
1.8V VOLTAGE REGULATOR



NOTE:
SET OUTPUT=1.85V FOR FRAMEBUFFER.
IRU3037ACS VREF=0.8VDC
VOUT=VREF*(R903+R905)/R905=1.85VDC

POWER BUDGET CURRENT OF TOTAL RAILS
10.9A PEAK
7.2A CONTINUOUS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0340	376S0388		Q1101,Q1102	



1.8V VREG	
SYNC_MASTER=M33-PC	SYNC_DATE=06/20/2005

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	F
	SCALE: NONE	SHT 11 OF 154	

KODIAK CORE VOLTAGE REGULATOR

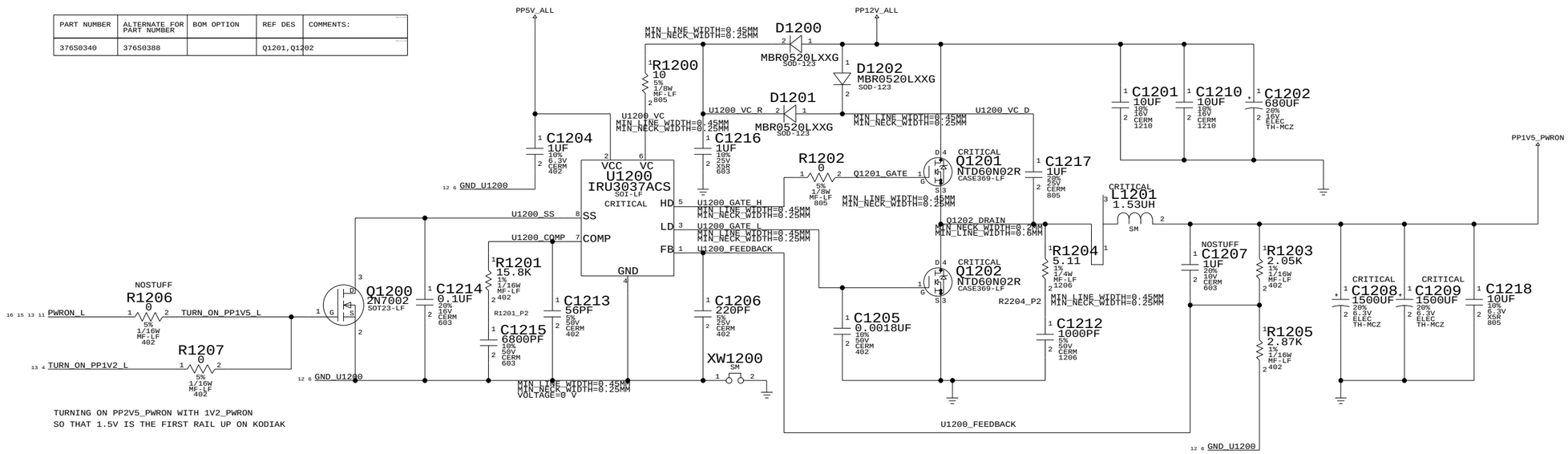
NOTE:

IRU3037ACS VREF=0.8VDC
VOUT=VREF*(R1203+R1205)/R1205=1.25VDC

LOAD FROM POWER BUDGET
8.5A PEAK CURRENT DRAW
7.2A CONTINUOUS CURRENT DRAW

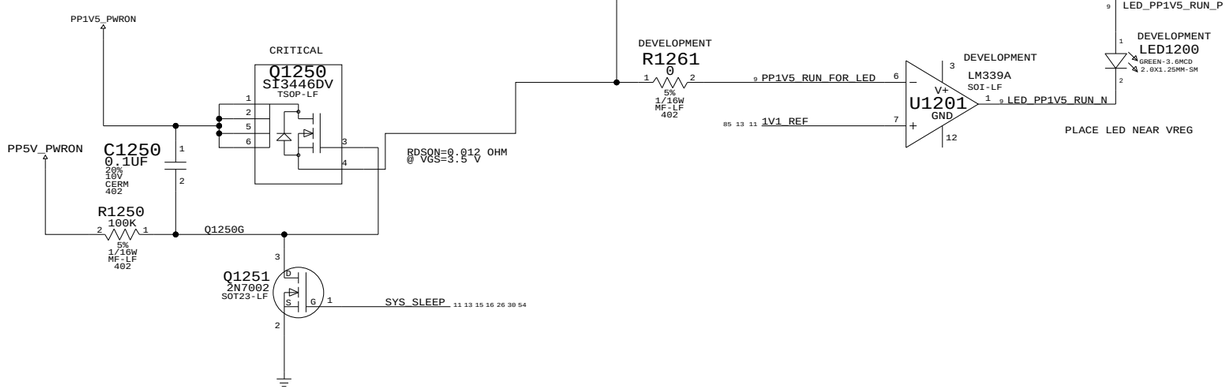
1.35V	R1205=2.87K
1.30V	R1205=3.24K
1.25V	R1205=3.65K

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0340	376S0388		Q1201,Q1202	

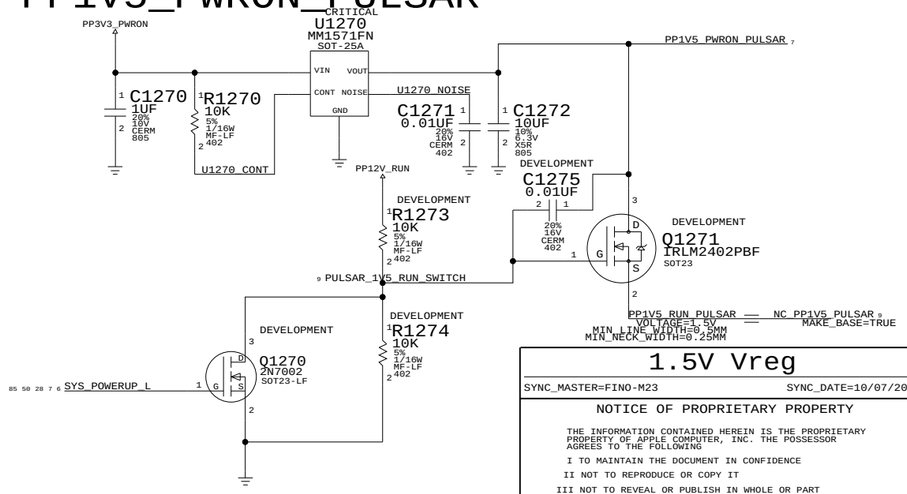


TURNING ON PP2V5_PWRON WITH 1V2_PWRON
SO THAT 1.5V IS THE FIRST RAIL UP ON KODIAK

LOAD FROM POWER BUDGET
1.3A PEAK CURRENT DRAW
1.0A CONTINUOUS CURRENT DRAW



PP1V5_PWRON_PULSAR



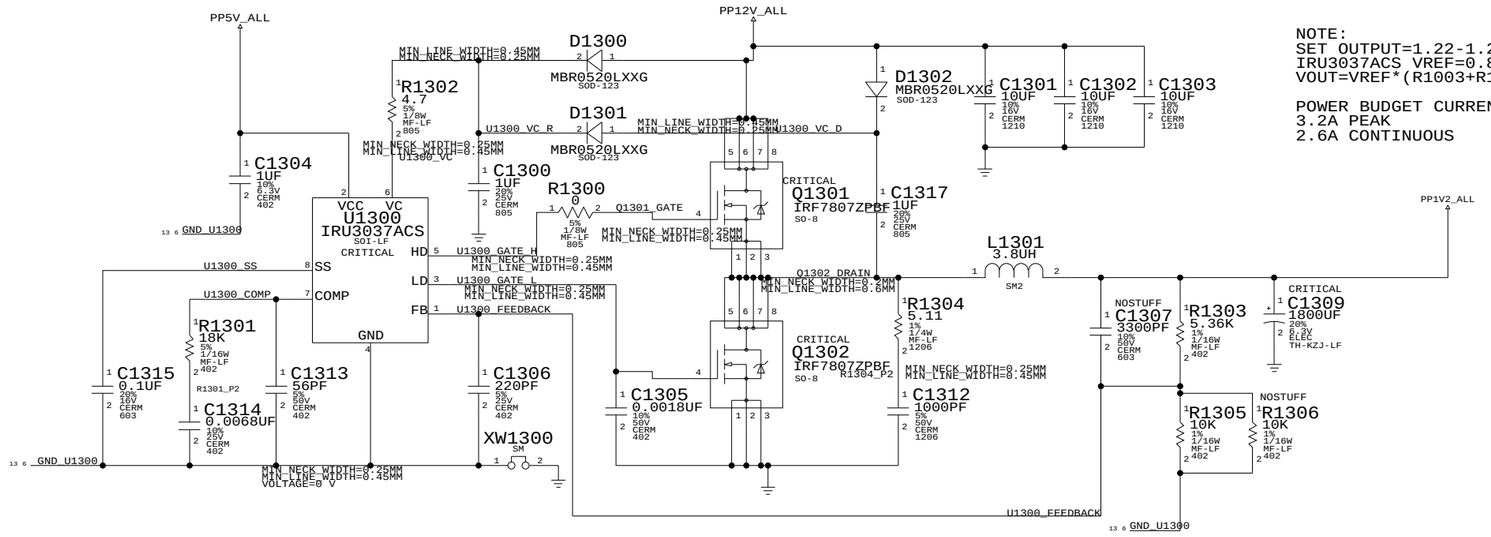
1.5V Vreg

SYNC_MASTER=FINO-M23 SYNC_DATE=10/07/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 12 OF 154	

PP1V2_ALL VOLTAGE REGULATOR

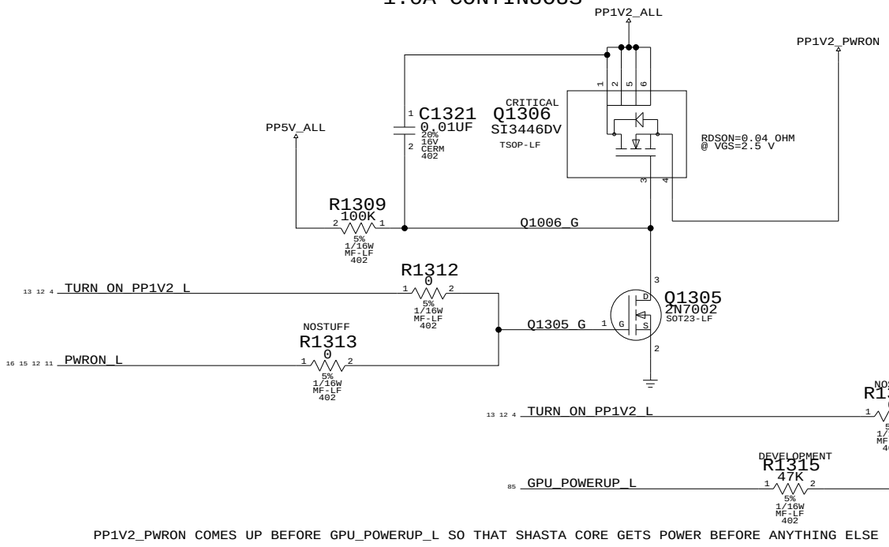


NOTE:
SET OUTPUT=1.22-1.23V
IRU3037ACS VREF=0.8VDC
VOUT=VREF*(R1003+R1005)/R1005=1.22-1.23VDC

POWER BUDGET CURRENT OF TOTAL RAILS
3.2A PEAK
2.6A CONTINUOUS

PP1V2_PWRON FET SWITCH

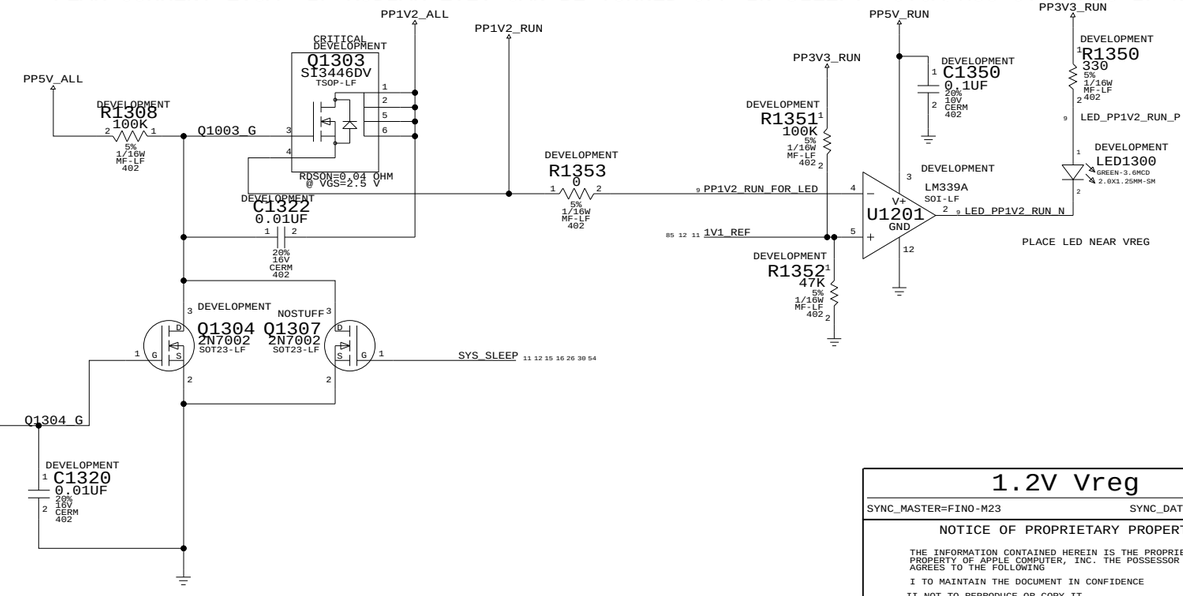
PEAK CURRENT 1.3A
1.0A CONTINUOUS



PP1V2_PWRON COMES UP BEFORE GPU_POWERUP_L SO THAT SHASTA CORE GETS POWER BEFORE ANYTHING ELSE

PP1V2_RUN FET SWITCH

PEAK CURRENT 1.3A IF KODIAK 1.2V CAN BE TURNED OFF IN SLEEP. 0.6A/M33 0.0A/M23 IF NOT



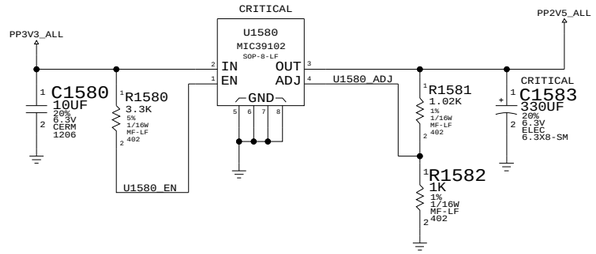
1.2V Vreg

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 13 OF 154	

PP2V5_ALL VOLTAGE REGULATOR

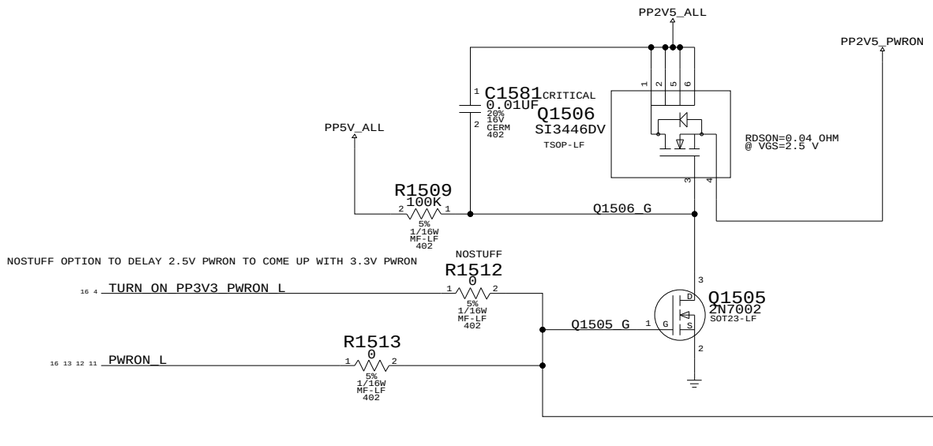


NOTE:
SET OUTPUT=2.5V
IRU3037CS VREF=1.24VDC
VOUT=VREF*(R1581+R1582)+1=5.505VDC

POWER BUDGET CURRENT OF TOTAL RAILS
0.2A PEAK
0.1A CONTINUOUS

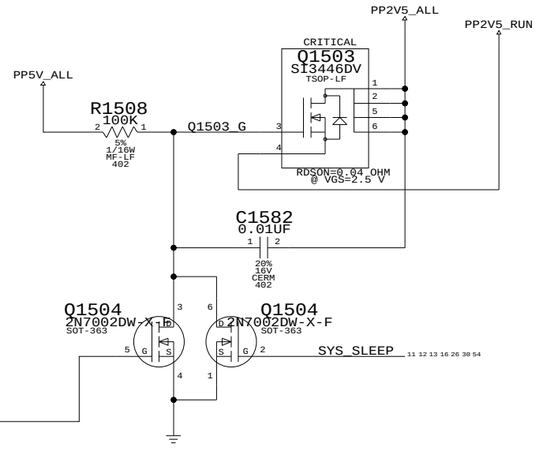
PP2V5_PWRON FET SWITCH

PEAK CURRENT 0.1A



PP2V5_RUN FET SWITCH

PEAK CURRENT 0.1A

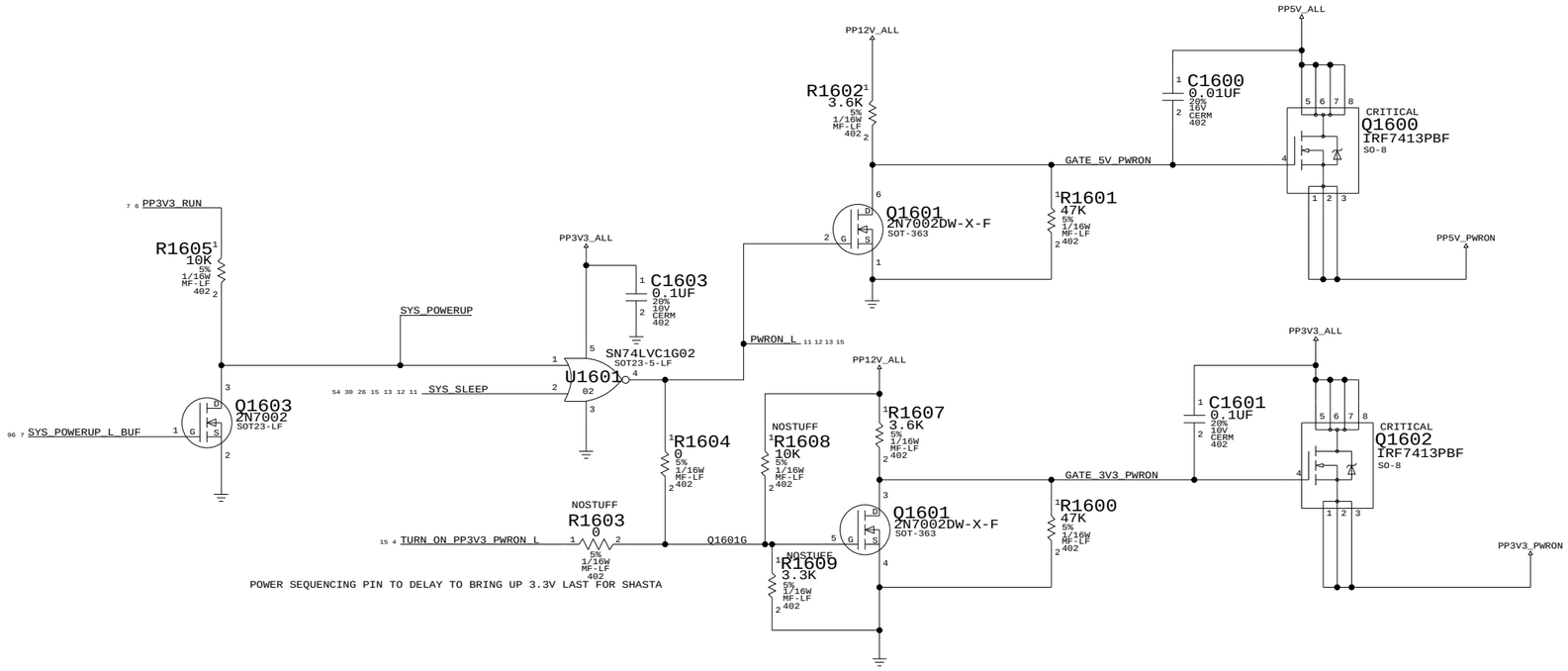


2.5V Vreg

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 15 OF 154	



5V & 3.3V Fets

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F

SCALE	SHT
NONE	16 OF 154

Page Notes

Power aliases required by this page:

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- VESTA1V2_BURST / VESTA1V2_PULSE
  Controls operating mode of Vesta 1.2V regulator. If both options are off the regulator will be in continuous mode.

VESTA JTAG

139 132 17 7 =PP3V3_ENETFW

VESTA HAS INTERNAL PULLUPS. MLB PULLUPS MAY BE NOSTUFFED IN EVT.

R1741 1K 5% 1/16W MF-LF 402
R1742 1K 5% 1/16W MF-LF 402
R1743 1K 5% 1/16W MF-LF 402

9 TP_JTAG_VESTA_TCK — MAKE_BASE=TRUE — =JTAG_VESTA_TCK 17
9 TP_JTAG_VESTA_TDI — MAKE_BASE=TRUE — =JTAG_VESTA_TDI 17
9 TP_JTAG_VESTA_TDO — MAKE_BASE=TRUE — =JTAG_VESTA_TDO 17
9 TP_JTAG_VESTA_TMS — MAKE_BASE=TRUE — =JTAG_VESTA_TMS 17
9 TP_JTAG_VESTA_TRST_L — MAKE_BASE=TRUE — =JTAG_VESTA_TRST_L

R1740 1K 5% 1/16W MF-LF 402

139 132 7 =PP1V2_ENETFW

L1700 FERR-EMI-600-OHM SM
PP1V2_VESTA_AVDDL
MIN_LINE_WIDTH=0.50 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.2V

C1708 10UF 10% 6.3V X5R 805 — L6/M6
C1700 0.1uF 20% 10V CERM 402 — L9/M9
C1701 0.1uF 20% 10V CERM 402 — N5/N6
C1702 0.1uF 20% 10V CERM 402
C1703 0.1uF 20% 10V CERM 402 — N9/N10

M23: PP3V3_ENETFW IS AN ALL RAIL
139 132 17 7 =PP3V3_ENETFW

R1750 10K 5% 1/16W MF-LF 402

M23: PP3V3_ENETFW IS AN ALL RAIL
139 132 17 7 =PP3V3_ENETFW

R1751 47K 5% 1/16W MF-LF 402

VESTA_RESET_RC

Q1750 2N7002DW-X-F SOT-363

C1750 1UF 10% 6.3V CERM 402

C1714 10UF 10% 6.3V X5R 805
C1710 0.1uF 20% 10V CERM 402
C1711 0.1uF 20% 10V CERM 402
C1712 0.1uF 20% 10V CERM 402
C1713 0.1uF 20% 10V CERM 402

=PP3V3_ENETFW 7 17 132 139

R1752 10K 5% 1/16W MF-LF 402

VESTA_RESET_L
SCHMITT TRIGGER W/ INTERNAL PULLUP

RESET ASSERT REQUIREMENT IS 20MS TO 100MS

NOSTUFF
R1720 0 5% 1/16W MF-LF 402
24 ENETFW_RESET

Q1750 2N7002DW-X-F SOT-363
132 VESTA_RESET_H

To keep Vesta from being held in reset when system is off
NOTE: Reset GPIO is active HIGH

VESTA MISC

SEE_TABLE

U1701
VESTA-V1.3
FBGA-200-LF
1 OF 3

		H4	RESET* IPU
17	=JTAG_VESTA_TDI	D7	TDI IPU
17	=JTAG_VESTA_TDO	E10	TDO
17	=JTAG_VESTA_TCK	E7	TCK IPU
17	=JTAG_VESTA_TMS	E8	TMS IPU
17	=JTAG_VESTA_TRST_L	D8	TRST* IPU
9	TP_VESTA_DNC_C9	C9	DNC
9	TP_VESTA_DNC_E9	E9	DNC
NC	C3		NC
NC	M13		NC

DVDD B1 B15 C15 J1
AVDDL L6 L9 M6 M9 M5 N6 N9 N10
AVDD P4 P5 P10 P11 R3 R12
PVDD A15 N4
OVDD A1 A7 F15 K1
AGND H11 H12 J11 J12 L7 L8 M7 M8 N7 N8 P6 P7 P8 P9
GND A2 B2 B7 C14 F14 J2 K2

IPD 2.5V_EN M3 — TP_VESTA_2_5V_EN 9

REGSUP1 E1 — TP_VESTA_REGSUP1 9
REGSEN1 F1 — TP_VESTA_REGSEN1 9
REGCTL1 G5 — TP_VESTA_REGCTL1 9

REGSUP2 E2 — TP_VESTA_REGSUP2 9
REGSEN2 F2 — TP_VESTA_REGSEN2 9
REGCTL2 G4 — TP_VESTA_REGCTL2 9

M23: ADDED C1726 AND C1744 PER BROADCOM RECOMMENDATIONS

C1720 0.1uF 20% 10V CERM 402
C1721 0.1uF 20% 10V CERM 402
C1722 0.1uF 20% 10V CERM 402
C1723 0.1uF 20% 10V CERM 402
C1724 0.1uF 20% 10V CERM 402
C1725 0.1uF 20% 10V CERM 402
C1726 10UF 10% 6.3V X5R 805

=PP2V5_ENETFW 7 132 139

C1730 0.1uF 20% 10V CERM 402
C1731 0.1uF 20% 10V CERM 402

=PP3V3_ENETFW 7 17 132 139

C1740 0.1uF 20% 10V CERM 402
C1741 0.1uF 20% 10V CERM 402
C1742 0.1uF 20% 10V CERM 402
C1743 0.1uF 20% 10V CERM 402
C1744 10UF 10% 6.3V X5R 805

2.5V_EN
0 - OVDD=3.3V
1 - OVDD=2.5V
WHEN OVDD=2.5V GMII PINS ARE NOT 3.3V TOLERANT

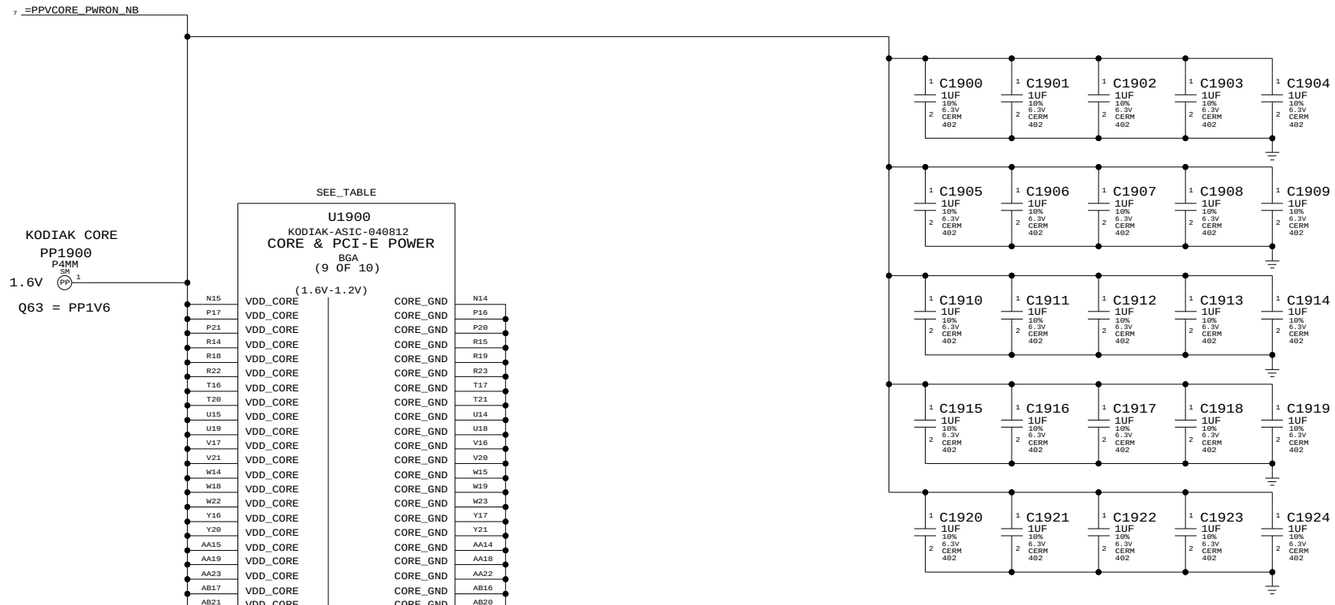
Vesta Core / Misc

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6863 | REV. F

SCALE NONE | SHT 17 OF 154



KODIAK CORE & BYPASS

SYNC_MASTER=Q63 SYNC_DATE=08/26/2005

LAST MODIFIED=Tue Nov 1 13:46:17 2005

APPLE COMPUTER INC.

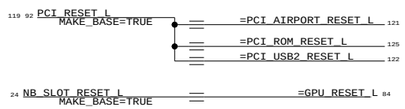
SIZE	DRAWING NUMBER	REV.
D	051-6863	F

SCALE	SHT	OF
NONE	19	154

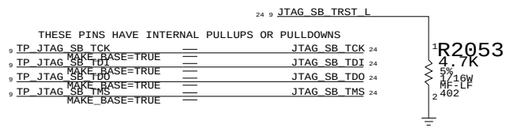
DRAWING

SHASTA ALIASES

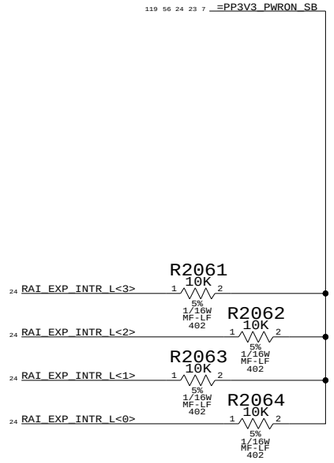
PCI_RESET_L IS AN 'AND' OF SB_PCI_RESET_L (SB)
AND SYS_IO_RESET_L (SMU)



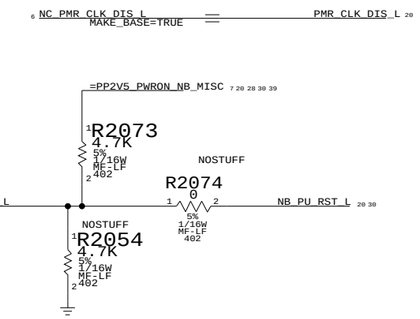
SHASTA JTAG



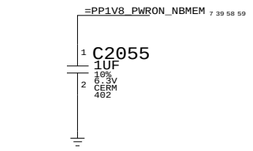
SHASTA GPIO TERMINATIONS (SOME OF THESE ARE NOSTUFF ON PAGE 24)



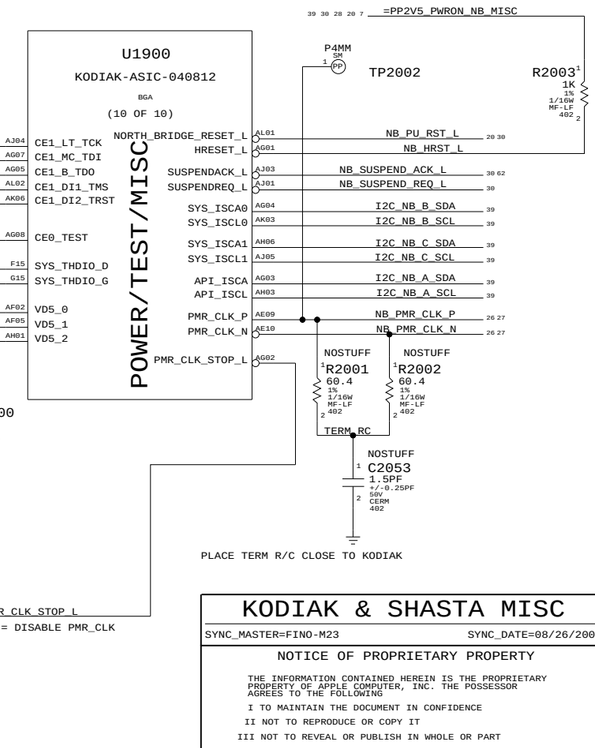
KODIAK ALIASES



KODIAK JTAG_TRST PULLED HIGH
TO ALLOW SMU DEBUG ACCESS

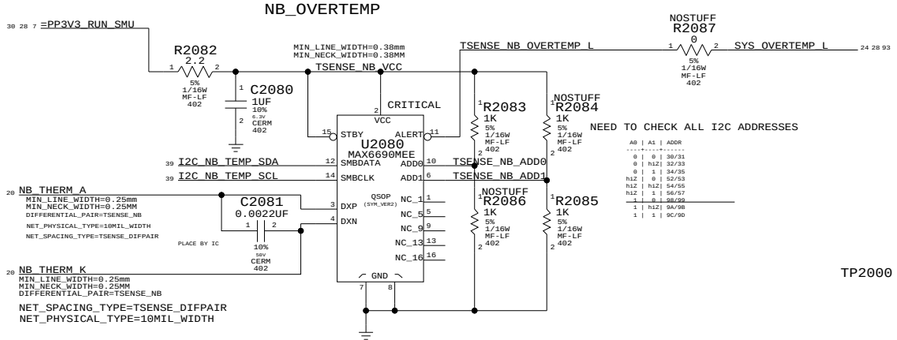


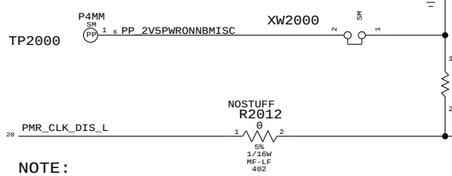
C2055 ADDED FOR KODIAK RAM DECOUPLING
PAGE 58 IS SHORT ONE CAP



PLACE TERM R/C CLOSE TO KODIAK

NB_OVERTEMP





NOTE: LOW = DISABLE PMR_CLK

NOTE:
PMR_CLK_STOP CAN BE USED TO STOP ALL CLOCKS IN KODIAK
USED FOR DEBUG
PLACE R2012 IN AN ACCESSIBLE LOCATION

KODIAK & SHASTA MISC

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT: 20 OF 154	

Page Notes

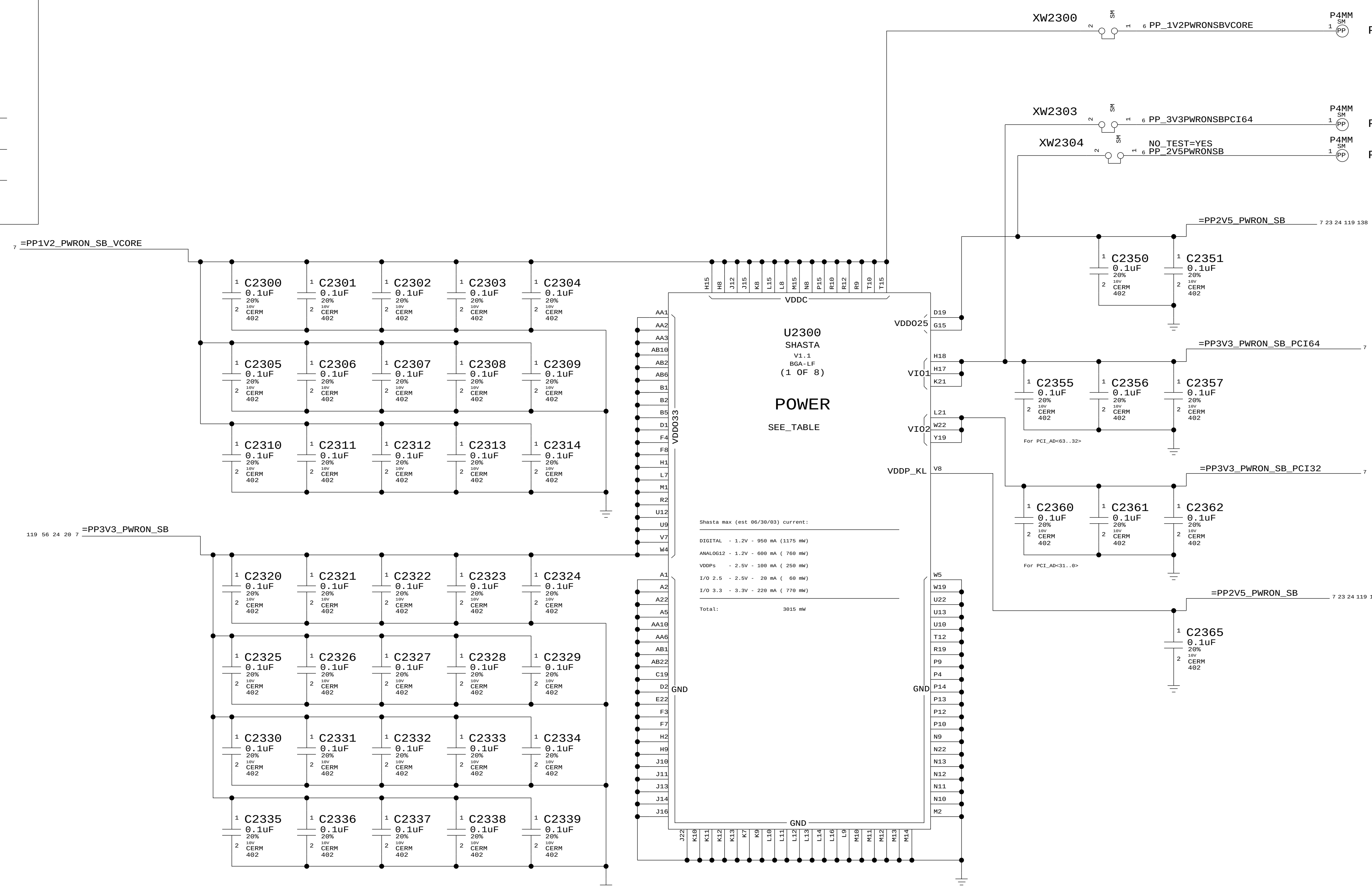
Power aliases required by this page:
- =PP3V3_PWRON_SB_PCI64 (VIO1) (TO 5V OR 3.3V)
- =PP3V3_PWRON_SB_PCI32 (VIO2) (TO 5V OR 3.3V)
- =PP3V3_PWRON_SB
- =PP2V5_PWRON_SB
- =PP1V2_PWRON_SB_VCORE

NOTE: PCI pads use the VIO supply to meet different drive timing characteristics required by the PCI spec for 5V vs. 3.3V operation. CONNECT VIO2 TO appropriate PCI bus voltage and VIO1 TO SAME IF 64-BIT PCI, otherwise 3.3V.

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Power Sequencing:
Must power Shasta VCore rail before any other Shasta supplies.



Shasta max (est 06/30/03) current:

DIGITAL	1.2V	950 mA	(1175 mW)
ANALOG12	1.2V	600 mA	(760 mW)
VDDPs	2.5V	100 mA	(250 mW)
I/O 2.5	2.5V	20 mA	(60 mW)
I/O 3.3	3.3V	220 mA	(770 mW)
Total:			3015 mW

Shasta Core Power

SYNC_MASTER=Q63 SYNC_DATE=08/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE NONE	SHT 23	OF 154

LAST_MODIFIED=Tue Nov 1 13:46:20 2005

DRAWING

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
I2S0_TO_SB		
I2S0_TO_DEV		
I2S0_TO_DEV	AUDIO	
I2S0_BIDIR		
I2S0_BIDIR		
I2S1_TO_SB		
I2S1_TO_DEV		
I2S1_TO_DEV	0.25mm SPACING	
I2S1_BIDIR		
I2S1_BIDIR		
I2S2_TO_SB		
I2S2_TO_DEV		
I2S2_TO_DEV	0.25mm SPACING	
I2S2_BIDIR		
I2S2_BIDIR		
SB_CLK18M_XTAL	0.38mm SPACING	
	0.38mm SPACING	
	0.38mm SPACING	
SB_CLK25M_ATA	0.38mm SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	

I2S0_DEV_TO_SB_DTI 24 147
I2S0_SB_TO_DEV_DTO 24 147
I2S0_MCLK 24 154
I2S0_BITCLK 24 147
I2S0_SYNC 24 147
I2S1_DEV_TO_SB_DTI 8 24
I2S1_SB_TO_DEV_DTO 8 24
I2S1_MCLK 8 24
I2S1_BITCLK 8 24
I2S1_SYNC 8 24
I2S2_DEV_TO_SB_DTI 24 154
I2S2_SB_TO_DEV_DTO 24 154
I2S2_MCLK 24 154
I2S2_BITCLK 24 154
I2S2_SYNC 24 154
SB_CLK18M_XTALI 24
SB_CLK18M_XTALO 24
SB_CLK18M_XTALO_R 24
SB_CLK25M_SATA 24 26
NB_TO_SB_INT 24
SB_CPU_A0_INT_L 24
SB_CPU_A1_INT_L 24
SB_CPU_B0_INT_L 24
SB_CPU_B1_INT_L 24
PCI_AIRPORT_INT_L 24 121
PCI_USB2_INT_L 24 122
I2S0_RESET_L 24 147
I2S1_RESET_L 8 24
I2S2_RESET_L 24 154
MB_SLOT_RESET_L 24
NB_SLOT_RESET_L 20 24
SB_CPU_A0_SRESET_L 24 56
SB_CPU_A1_SRESET_L 24 56
SB_CPU_B0_SRESET_L 24 56
SB_CPU_B1_SRESET_L 24 56

Page Notes

Power aliases required by this page:
- _PP3V3_PCI
- _PP3V3_PWRON_SB
- _PP2V5_PWRON_SB
- _PP1V2_PWRON_SB

Signal aliases required by this page: (NONE)

BOM options provided by this page:
- PCI_64BIT: Configures Shasta for 64-bit PCI
  NOTE: XGC required for Shasta GPIOs
- MPIC_NB/MPIC_SB: Selects whether NorthBridge or SouthBridge MPIC will be used for interrupt controller.

AUDIO PAGES IS RESPONSIBLE FOR TERMINATION OF I2S0 AND I2S2
DO NOT ADD PULLUP/DOWN FOR I2S0 AND IS=2S2 IN THIS PAGE

Re-pin within each RPAK as necessary
DO NOT swap between RPAKs

NorthBridge / SouthBridge MPIC Routing

PLACE R2402 CLOSE TO SHASTA

PLACE R2432 CLOSE TO SHASTA

SPEC SHOWS LOAD CAPACITANCE OF 16PF FOR 197S0004

AUDIO GPIOS
NOTE: It is the responsibility of the audio circuit to provide the necessary pull-ups & pull-downs.

LAST_MODIFIED=Tue Nov 1 13:46:21 2005

Shasta Serial / Misc

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

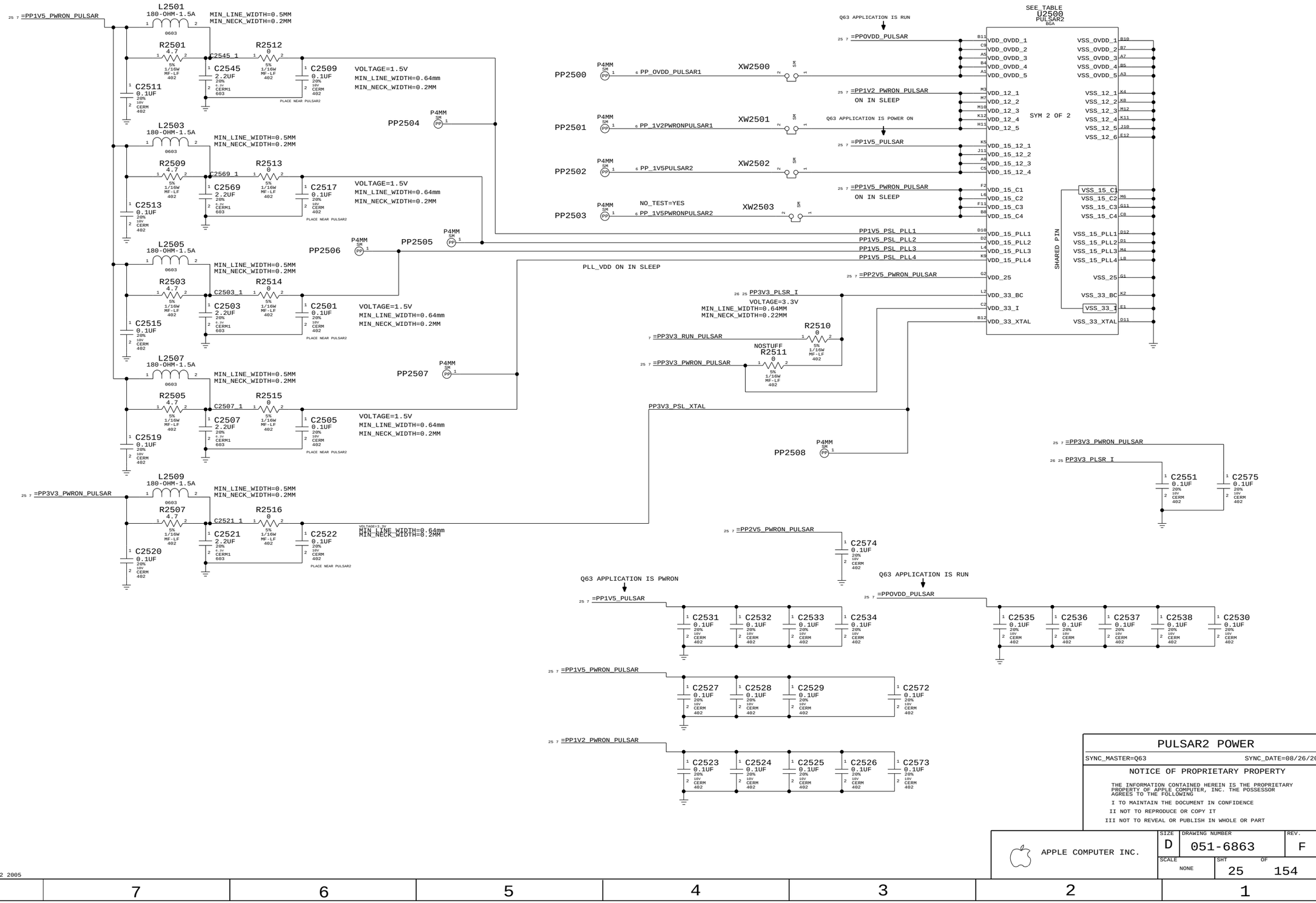
NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 24 OF 154	

DRAWING
TITLE=SCHEMATIC
ABBREV=SCHEMATIC


=PP1V5_PWRON_PULSAR
L2501
180-OHM-1.5A
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
R2501 4.7
R2512 0
C2545 2.2UF
C2509 0.1UF
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.64mm
MIN_NECK_WIDTH=0.2MM
C2511 0.1UF
PP2504
L2503
R2509 4.7
R2513 0
C2569 2.2UF
C2517 0.1UF
C2513 0.1UF
L2505
R2503 4.7
R2514 0
C2503 2.2UF
C2501 0.1UF
C2515 0.1UF
PP2506
PP2505
L2507
R2505 4.7
R2515 0
C2507 2.2UF
C2505 0.1UF
C2519 0.1UF
PP2507
L2509
R2507 4.7
R2516 0
C2521 2.2UF
C2522 0.1UF
C2520 0.1UF
=PP3V3_PWRON_PULSAR
PLACE NEAR PULSAR2
PP2508
PP2500
PP2501
PP2502
PP2503
PP_OVDD_PULSAR1
PP_1V2PWRONPULSAR1
PP_1V5PULSAR2
PP_1V5PWRONPULSAR2
XW2500
XW2501
XW2502
XW2503
NO_TEST=YES
Q63 APPLICATION IS RUN
Q63 APPLICATION IS POWER ON
=PPOVDD_PULSAR
=PP1V2_PWRON_PULSAR
ON IN SLEEP
=PP1V5_PULSAR
=PP1V5_PWRON_PULSAR
=PP2V5_PWRON_PULSAR
PP1V5_PSL_PLL1
PP1V5_PSL_PLL2
PP1V5_PSL_PLL3
PP1V5_PSL_PLL4
PLL_VDD ON IN SLEEP
PP3V3_PLSR_I
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.64MM
MIN_NECK_WIDTH=0.22MM
=PP3V3_RUN_PULSAR
NOSTUFF
R2511 0
R2510 0
=PP3V3_PWRON_PULSAR
PP3V3_PSL_XTAL
SEE_TABLE
U2500
PULSAR2
BGA
SYM 2 OF 2
SHARED PIN
VDD_OVDD_1
VDD_OVDD_2
VDD_OVDD_3
VDD_OVDD_4
VDD_OVDD_5
VDD_12_1
VDD_12_2
VDD_12_3
VDD_12_4
VDD_12_5
VDD_15_12_1
VDD_15_12_2
VDD_15_12_3
VDD_15_12_4
VDD_15_C1
VDD_15_C2
VDD_15_C3
VDD_15_C4
VDD_15_PLL1
VDD_15_PLL2
VDD_15_PLL3
VDD_15_PLL4
VDD_25
VDD_33_BC
VDD_33_I
VDD_33_XTAL
VSS_OVDD_1
VSS_OVDD_2
VSS_OVDD_3
VSS_OVDD_4
VSS_OVDD_5
VSS_12_1
VSS_12_2
VSS_12_3
VSS_12_4
VSS_12_5
VSS_12_6
VSS_15_C1
VSS_15_C2
VSS_15_C3
VSS_15_C4
VSS_15_PLL1
VSS_15_PLL2
VSS_15_PLL3
VSS_15_PLL4
VSS_25
VSS_33_BC
VSS_33_I
VSS_33_XTAL
=PP3V3_PWRON_PULSAR
=PP3V3_PLSR_I
C2551 0.1UF
C2575 0.1UF
=PP2V5_PWRON_PULSAR
C2574 0.1UF
Q63 APPLICATION IS PWRON
Q63 APPLICATION IS RUN
=PP1V5_PULSAR
=PPOVDD_PULSAR
C2531 0.1UF
C2532 0.1UF
C2533 0.1UF
C2534 0.1UF
C2535 0.1UF
C2536 0.1UF
C2537 0.1UF
C2538 0.1UF
C2530 0.1UF
=PP1V5_PWRON_PULSAR
C2527 0.1UF
C2528 0.1UF
C2529 0.1UF
C2572 0.1UF
=PP1V2_PWRON_PULSAR
C2523 0.1UF
C2524 0.1UF
C2525 0.1UF
C2526 0.1UF
C2573 0.1UF
PULSAR2 POWER
SYNC_MASTER=Q63
SYNC_DATE=08/26/2005
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-6863
REV. F
SCALE NONE
SHT 25 OF 154
LAST_MODIFIED=Tue Nov 1 13:46:22 2005
DRAWING

PLACE ALL 0-OHM SERIES RESISTORSRES
ON THIS PAGE NEAR PULSAR

REMOVED R2632 AND R2630
FROM UNUSED CLOCKS FOR EMC

QUASAR CLOCKS ARE RESISTOR DIVIDED DOWN
TO 1.8V ON QUASAR PAGES

LAST MODIFIED: APR 26, 04

PULSAR2 CLOCKS

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F

SCALE: NONE SHT: 26 OF: 154

LAST_MODIFIED=Tue Nov 1 13:46:22 2005

N/C ALIASES

N/C RAINIER CLOCKS

6 NC_CLK_RAI_REFCLK_66M — MAKE_BASE=TRUE — CLK_RAI_REFCLK_66M 26

6 NC_CLK_RAI_GIGE_25MHZ — MAKE_BASE=TRUE — CLK_RAI_GIGE_25MHZ 26

6 NC_CLK_RAI_200M_P<0> — MAKE_BASE=TRUE — CLK_RAI_200M_P<0> 26

6 NC_CLK_RAI_200M_N<0> — MAKE_BASE=TRUE — CLK_RAI_200M_N<0> 26

6 NC_CLK_RAI_PCIEA_P<0> — MAKE_BASE=TRUE — CLK_RAI_PCIEA_P<0> 26

6 NC_CLK_RAI_PCIEA_N<0> — MAKE_BASE=TRUE — CLK_RAI_PCIEA_N<0> 26

6 NC_CLK_RAI_PCIEB_P<0> — MAKE_BASE=TRUE — CLK_RAI_PCIEB_P<0> 26

6 NC_CLK_RAI_PCIEB_N<0> — MAKE_BASE=TRUE — CLK_RAI_PCIEB_N<0> 26

6 NC_CLK_RAI_PCIEC_P<0> — MAKE_BASE=TRUE — CLK_RAI_PCIEC_P<0> 26

6 NC_CLK_RAI_PCIEC_N<0> — MAKE_BASE=TRUE — CLK_RAI_PCIEC_N<0> 26

N/C CPUB CLOCKS

6 NC_EI_CPU_B_SYSCLK_P — MAKE_BASE=TRUE — EI_CPU_B_SYSCLK_P 26

6 NC_EI_CPU_B_SYSCLK_N — MAKE_BASE=TRUE — EI_CPU_B_SYSCLK_N 26

6 NC_CPU_B_APSYNC — MAKE_BASE=TRUE — CPU_B_APSYNC 26

N/C QUASAR CLOCKS

6 NC_RAM_ARB0_REF25MHZ — MAKE_BASE=TRUE — RAM_ARB0_REF25MHZ 26

6 NC_RAM_ARB1_REF25MHZ — MAKE_BASE=TRUE — RAM_ARB1_REF25MHZ 26

CLOCK CONSTRAINTS

	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	ELECTRICAL_CONSTAINT_SET
26 20 NB_PMR_CLK_P	NB_PMR_CLK	NB_PMR_CLK	NB_PMR_CLK_SP	NB_PMR_CLK
25 20 NB_PMR_CLK_N	NB_PMR_CLK	NB_PMR_CLK	NB_PMR_CLK_SP	NB_PMR_CLK
119 26 PCI_CLK66M_SB_INT		PCI_CLK_SB	P3MM SPACING	PCI_CLK_SB
119 26 PCI_CLK33M_SB_EXT_RR		PCI_CLK_SB	PCI_CLK_SB	PCI_CLK_SB_CAP

167 168 169 170

NOTE:
ALL OTHER CLOCK CONTRAINTS ON THEIR
RESPECTIVE BUS PAGES

26 PCI_CLK33M_USB2 — MAKE_BASE=TRUE — =PCI_CLK33M_USB2 122

Pulsar Aliases

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F

SCALE NONE SHT 27 OF 154

System Management Unit

Page Notes

Power aliases required by this page:
- =PP3V3_ALL_SMU
- =PP3V3_ALL_RTC
- =PP3V3_PWRON_SMU
- =PPVREF_SMU (SMU AVCC OR 2.5V REFERENCE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NOTE: CPU current/voltage monitoring (CPU_SENSE_I/CPU_SENSE_V) requires 100K/10uF RC filter at SMU pins. Caps should connect to GND_SMU_AVSS. SMU_VREF should be same signal or reference used by monitoring circuit, but be aware that this will affect other analog inputs such as AC adapter ID.

NOTE: All analog inputs to SMU should have a 100pF capacitor to the SMU AVSS signal (GND_SMU_AVSS). None of those capacitors are provided on this page.

NOTE: Some primary and alternate functions reuire pull-ups that are not. provided on this page. Please. review the latest SMU specification to ensure missing pull-ups are provided on another page.

NOTE: Pinout matches SMU pinout v1.51.

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
SMU_CLK10M_XTAL	0.38MM SPACING		SMU_CLK10M_XIN 28
	0.38MM SPACING		SMU_CLK10M_XOUT 28
	0.38MM SPACING		SMU_CLK10M_XOUT_R 28
RTC_CLK32K_XTAL	0.38MM SPACING		RTC_CLK32K_X1 28
	0.38MM SPACING		RTC_CLK32K_X2 28
A475	P3MM SPACING		SMU_IO_RESET_L 28 30
A476	0.25MM SPACING		SYS_NORTH_RESET_L 28 30

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
A456 SMU_RESET	0.25MM SPACING		SYS_NORTH_RESET_L 28 30
A457 SMU_RESET	0.25MM SPACING		SYS_IO_RESET_L 24 30 119 122
A472	P3MM SPACING		CLOCK_RESET_L 26 28
A475	P3MM SPACING		SYS_RESET_BUTTON_L 28 29

PP2800 P4MM SM 1 6 PP_3V3ALLSMU — XW2802 SM 2 1 — 29 28 7 6 =PP3V3_ALL_SMU

C2800 10UF 10% 6.3V XSR 805 — C2801 0.1uF 20% 10V CERM 402 — C2802 0.1uF 20% 10V CERM 402

R2815 4.7 5% 1/16W MF-LF 402 — 13 SEE_TABLE 78

PP3V3_ALL_SMU_AVCC
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.38mm
MIN_NECK_WIDTH=0.2MM

C2803 1uF 10% 6.3V CERM 402

XW2801 SM 2 1 — P4MM SM 1 6 PP_3V3ALLSMUAVCC — PP2801 P4MM SM 1

GND_SMU_AVSS 6 28 55

Y = Primary function
N = Alternate function (see aliases below)
S = Spare

U2800 M30280F8-LF QFP-80

VCC 13 — VSS 11 — AVCC 75

	Portable	Consumer	Entry Desktop	Desktop	Server				Portable	Consumer	Entry Desktop	Desktop	Server	
55 CPU_SENSE_I	Y	Y	Y	S	S	67	P0[0]	AN00	RTS0*/CTS0*	P6[0]	43	Y	Y	Y	N	N	SMU_BOOT_BUSY 6 29 (MAKE_BASE=TRUE)
55 CPU_SENSE_V	Y	Y	Y	S	S	66	P0[1]	AN01	CLK0	P6[1]	42	Y	Y	Y	N	N	SMU_BOOT_SCLK 6 29 (MAKE_BASE=TRUE)
55 CPU_TEMP	Y	Y	Y	S	S	65	P0[2]	AN02	RXD0	P6[2]	41	Y	Y	Y	N	N	SMU_BOOT_CE 6 29 (MAKE_BASE=TRUE)
29 CPU_BYPASS	Y	Y	Y	S	S	64	P0[3]	AN03	TXD0	P6[3]	40	Y	Y	Y	S	S	CPU_VID<0> 28 31
31 SMU_FAN_RPM3	N	S	Y	Y	Y	63	P0[4]	AN04	RTS1* (BUSY)	P6[4]	31	Y	Y	Y	S	S	CPU_VID<1> 28 31
31 SMU_FAN_RPM4	N	S	Y	Y	Y	62	P0[5]	AN05	CLK1	P6[5]	30	Y	Y	Y	S	S	CPU_VID<2> 28 31
31 SMU_FAN_RPM5	N	S	Y	Y	Y	61	P0[6]	AN06	RXD1	P6[6]	29	Y	Y	Y	Y	Y	CPU_VID<3> 28 31
31 SMU_SER_SEL	Y	Y	Y	Y	Y	60	P0[7]	AN07	TXD1	P6[7]	28	Y	Y	Y	Y	Y	CPU_VID<4> 28 31
P1[0] NOT USED --->																	SMU_BOOT_RXD 6 29
4 SMU_PWRSEQ_P1_0	Y	Y	Y	Y	Y	59	P1[0]	AN20									SMU_BOOT_TXD 6 29
4 SMU_PWRSEQ_P1_1	Y	Y	Y	Y	Y	58	P1[1]	AN21	SDA	P7[0]	27	Y	Y	Y	Y	Y	I2C_SMU_B_SDA 39
4 SMU_PWRSEQ_P1_2	Y	Y	Y	Y	Y	57	P1[2]	AN22	SCL	P7[1]	26	Y	Y	Y	Y	Y	I2C_SMU_B_SCL 39
4 SMU_PWRSEQ_P1_3	Y	Y	Y	Y	Y	56	P1[3]	AN23	TA1out	P7[2]	25	Y	Y	Y	N	N	I2C_SMU_CPU_SDA_IN 28 31
4 SMU_PWRSEQ_P1_4	Y	Y	Y	Y	Y	55	P1[4]		TA1in	P7[3]	24	Y	Y	Y	Y	Y	SMU_FAN_RPM0 32
7 SYS_POWERFAIL_L	N	Y	Y	Y	Y	54	P1[5]	INT3*	TA2out	P7[4]	23	Y	Y	Y	N	N	I2C_SMU_CPU_SCL_IN 28 31
31 SMU_FAN_TACH9	N	S	S	S	Y	53	P1[6]	INT4*	TA2in	P7[5]	22	Y	Y	Y	Y	Y	SMU_FAN_RPM1 32
31 SYS_DOOR_AJAR_L	N	S	Y	Y	Y	52	P1[7]	INT5*	TA3out	P7[6]	21	N	S	S	Y	Y	SB_CPU_VDNAP2 24
									TA3in	P7[7]	20	Y	Y	Y	Y	Y	SMU_FAN_RPM2 33
31 SMU_FAN_TACH6	Y	Y	Y	Y	Y	51	P2[0]	SDAmm	TA4out	P8[0]	19	Y	Y	Y	Y	Y	SYS_LED 29
31 SMU_FAN_TACH7	Y	Y	Y	Y	Y	50	P2[1]	SCLmm	TA4in	P8[1]	18	Y	Y	Y	Y	Y	SYS_NORTH_RESET_L 28 30
32 SMU_FAN_TACH0	Y	Y	Y	Y	Y	49	P2[2]	IOC2	INT0*	P8[2]	17	Y	Y	Y	Y	Y	SYS_PME_L 24 28 122
32 SMU_FAN_TACH1	Y	Y	Y	Y	Y	48	P2[3]	IOC3	INT1*	P8[3]	16	S	S	S	S	S	SB_CPU_VDNAP0_OR_QREQ_OR_SPDIF 31
33 SMU_FAN_TACH2	Y	Y	Y	Y	Y	47	P2[4]	IOC4	INT2*	P8[4]	15	Y	Y	Y	Y	Y	SYS_SLEWING_L 24 26 28 50
31 SMU_FAN_TACH3	S	N	Y	Y	Y	46	P2[5]	IOC5	NMI*	P8[5]	14	Y	Y	Y	S	S	I2C_SMU_CPU_SDA_OUT_L 28 31
31 SMU_FAN_TACH4	S	N	Y	Y	Y	45	P2[6]	IOC6	CE*	P8[6]	8	Y	Y	Y	Y	Y	SYS_POWERUP_L 6 7 12 28 50 85 (MAKE_BASE=TRUE)
31 SMU_FAN_TACH5	S	N	Y	Y	Y	44	P2[7]	IOC7		P8[7]	7	Y	Y	Y	Y	Y	SMU_SLEEP 28 30
31 28 I2C_SMU_A_SDA_IN	Y	Y	Y	Y	Y	39	P3[0]	CLK3	TB0in	P9[0]	5	Y	Y	Y	Y	Y	CLOCK_RESET_L 26 28
31 28 I2C_SMU_A_SDA_OUT_L	Y	Y	Y	Y	Y	38	P3[1]	Sin3	TB1in	P9[1]	4	Y	Y	Y	S	S	SMU_FAN_TACH8 31
31 28 I2C_SMU_A_SCL_IN	Y	Y	Y	Y	Y	37	P3[2]	Sout3	TB2in	P9[2]	3	Y	Y	Y	Y	Y	SB_TO_SMU_INT_L 24
31 28 I2C_SMU_A_SCL_OUT_L	Y	Y	Y	Y	Y	36	P3[3]		AN24	P9[3]	2	Y	Y	Y	Y	Y	SB_STOPXTALS_L 24
39 I2C_SMU_E_SDA	Y	Y	Y	Y	Y	35	P3[4]		AN25	P9[5]	1	Y	Y	Y	Y	Y	SMU_PWRSEQ_P9_5 4
39 I2C_SMU_E_SCL	Y	Y	Y	Y	Y	34	P3[5]		AN26	P9[6]	80	Y	Y	Y	Y	Y	SMU_PWRSEQ_P9_6 4
8 DIAG_LED	Y	S	S	S	S	33	P3[6]		AN27	P9[7]	79	S	S	S	Y	S	SYS_SLOT_PWR 31
93 24 20 SYS_OVERTEMP_L	Y	S	S	S	S	32	P3[7]										
									AN0	P10[0]	76	S	S	S	S	S	SB_CPU_VDNAP1 24
									AN1	P10[1]	74	Y	Y	Y	Y	Y	SMU_IO_RESET_L 28 30
									AN2	P10[2]	73	Y	Y	Y	Y	Y	NB_SUSPENDACK_L 30
									AN3	P10[3]	72	Y	Y	Y	Y	Y	SB_SUSPENDACK_L 24
									KI0*	P10[4]	71	Y	Y	Y	Y	Y	SMU_SUSPENDREQ_L 24 28 30 43
									KI1*	P10[5]	70	Y	Y	Y	Y	Y	SYS_POWER_BUTTON_L 6 28 29
									KI2*	P10[6]	69	Y	Y	Y	Y	Y	SYS_RESET_BUTTON_L 28 29
									KI3*	P10[7]	68	Y	Y	Y	S	S	I2C_SMU_CPU_SCL_OUT_L 28 31

55 =PPVREF_SMU

29 6 SMU_BOOT_CNVSS — 6 PCNVSS
29 6 SMU_RESET_L — 9 RESET*
28 SMU_CLK10M_XOUT_R — 10 XOUT
28 SMU_CLK10M_XIN — 12 XIN
77 VREF

PP2804 P4MM SM 1 — PP2805 P4MM SM 1 — PP2806 P4MM SM 1

R2816 10M 5% 1/16W MF-LF 402

R2817 470 5% 1/16W MF-LF 402

CRITICAL Y2800 10.0000M 8X4.5MM-SM

28 SMU_CLK10M_XOUT

C2804 18PF 5% 50V CERM 402 — C2805 18PF 5% 50V CERM 402

R2825 10K 5% 1/16W MF-LF 402 — C2825 1uF 10% 6.3V CERM 402

XW2800 SM 1 2

R2827 10K 5% 1/16W MF-LF 402

GND_SMU_AVSS 6 28 55
VOLTAGE=0V
MIN_LINE_WIDTH=0.38mm
MIN_NECK_WIDTH=0.2MM

Keep crystal subcircuit close to SMU.
Y2800'S LOAD CAPACITANCE IS 12PF

Real Time Clock

29 =PP3V3_ALL_RTC
29 28 7 6 =PP3V3_ALL_SMU

C2808 0.1uF 20% 10V CERM 402

U2801 DS1338U-33 MSOP
VCC 8 CRITICAL
SDA 5 — 39 I2C_RTC_SDA
SCL 6 — 39 I2C_RTC_SCL
SQW/OUT 7
GND 4
X1 1 — RTC_CLK32K_X1 28
X2 2
VBAT 3
NC 1

CRITICAL Y2801 32.768K SM-LF — RTC_CLK32K_X2 28

C2809 0.1uF 20% 10V CERM 402

SMU Pull-ups / pull-down

29 28 7 6 =PP3V3_ALL_SMU
R2800 10K 5% 1/16W MF-LF 402 — SYS_POWERUP_L 6 7 12 28 50 85
R2801 10K 5% 1/16W MF-LF 402 — SYS_RESET_BUTTON_L 28 29
R2802 10K 5% 1/16W MF-LF 402 — SYS_POWER_BUTTON_L 6 28 29

43 30 7 =PP3V3_PWRON_SMU
R2804 10K 5% 1/16W MF-LF 402 — SYS_PME_L 24 28 122

30 20 7 =PP3V3_RUN_SMU
R2812 2.0K 1% 1/16W MF-LF 402 — SYS_SLEWING_L 24 26 28 50

NOSTUFF
39 30 20 7 =PP2V5_PWRON_NB_MISC
DRIVEN PUSH/PULL
R2811 2.0K 1% 1/16W MF-LF 402 — SMU_SUSPENDREQ_L 24 28 30 43

NOSTUFF
PULLUP AT LEVEL SHIFTER P.30
R2813 10K 5% 1/16W MF-LF 402 — SYS_NORTH_RESET_L 28 30

R2810 100K 1% 1/16W MF-LF 402 — SMU_SLEEP 28 30

Alternate Functions

Tower & Server

	Port		
31 28 CPU_VID<0>	6.0	—	SAT_MRESET_L
31 28 CPU_VID<1>	6.1	—	CPU_A_INSERTED_L
31 28 CPU_VID<2>	6.2	—	CPU_B_INSERTED_L
31 28 I2C_SMU_CPU_SDA_IN	7.2	—	SMU_FAN_PWM8
31 28 I2C_SMU_CPU_SCL_IN	7.4	—	SMU_FAN_PWM9
31 28 I2C_SMU_A_SDA_IN	3.0	—	I2C_SMU_A_SDA 31 39
31 28 I2C_SMU_A_SDA_OUT_L	3.1	—	I2C_SMU_A_SCL 31 39

	Port		
31 28 CPU_VID<3>	6.3	—	SMU_FAN_RPM6
31 28 CPU_VID<4>	6.4	—	SMU_FAN_RPM7
31 28 I2C_SMU_A_SCL_IN	3.2	—	NB_TDI
31 28 I2C_SMU_A_SCL_OUT_L	3.3	—	NB_TCK
31 28 I2C_SMU_CPU_SDA_OUT_L	8.5	—	NB_TMS
31 28 I2C_SMU_CPU_SCL_OUT_L	10.7	—	NB_TDO_SMU

System Management Unit		
SYNC_MASTER=Q63	SYNC_DATE=08/26/2005	

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

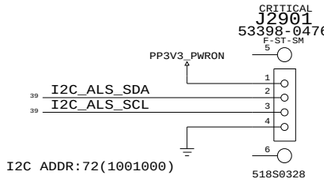
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 28 OF 154	

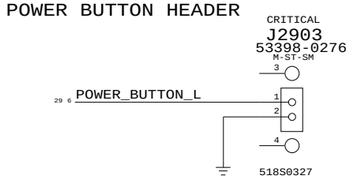
LAST_MODIFIED=Tue Nov 1 13:46:23 2005

DRAWING TITLE=KILOHANA ASSEMBLY=DRAWING

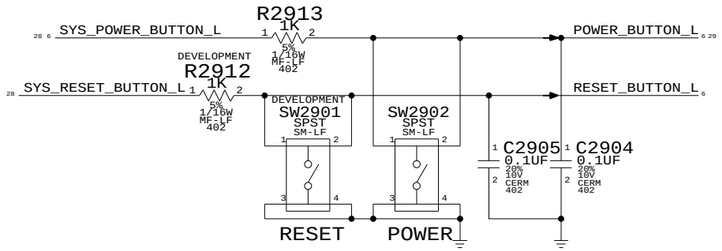
AMBIENT LIGHT SENSOR CONNECTOR



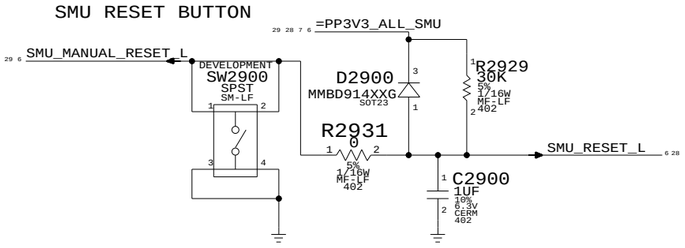
POWER BUTTON HEADER



SYS POWER AND RESET BUTTON

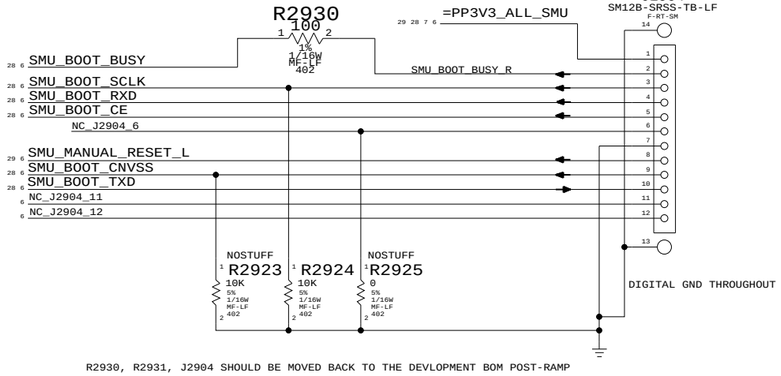


SMU RESET BUTTON



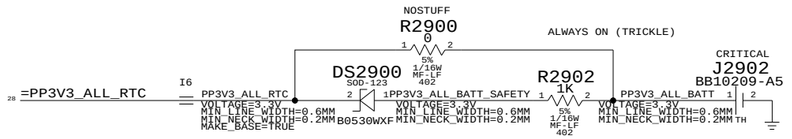
SMU DEBUG/DOWNLOAD CONNECTOR

SAME CONNECTOR AS Q63 CPU CARD FOR SAT

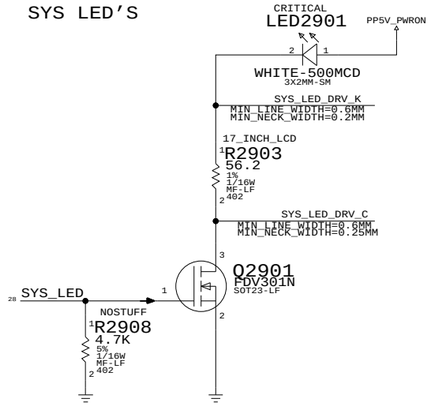


R2930, R2931, J2904 SHOULD BE MOVED BACK TO THE DEVLOPMENT BOM POST-RAMP

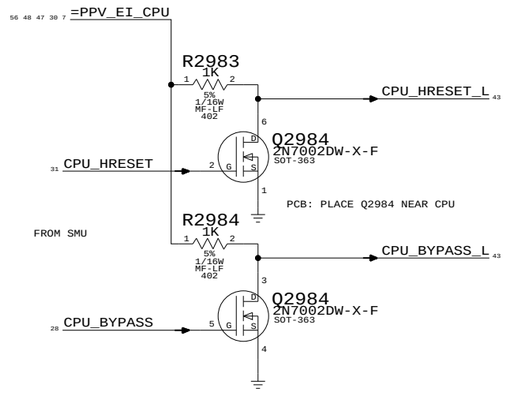
RTC BATTERY



SYS LED'S



DRIVE STRONG HRESET AND BYPASS TO CPU



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0081	1	RES, 39.2 OHM, 1%, 402, LF	R2903	20_INCH_LCD

SMU SUPPLEMENTAL (2)

SYNC_MASTER=FINO-M23 SYNC_DATE=09/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F

SCALE	SHT	OF
NONE	29	154

SMU TO NB SUSPEND_REQ

SAME AS Q63

=PP3V3_PWRON_SMU

R3000 1K 5% 1/16W MF-LF 402

R3003 4.7K 5% 1/16W MF-LF 402

PMU_SUSPEND_REQ

=PP2V5_PWRON_NB_MISC

R3001 100 5% 1/16W MF-LF 402

NB_SUSPEND_REQ_L

SMU_SUSPENDREQ_L

Q3005 2N7002DW-X-F SOT-363

Q3000 2N7002DW-X-F SOT-363

NOSTUFF R3002 0 5% 1/16W MF-LF 402

SMU_SUSPENDREQ_L_R

NOSTUFF R3099 0 5% 1/16W MF-LF 402

=PP2V5_PWRON_NB_MISC

R3038 10K 5% 1/16W MF-LF 402

JTAG_NB_TDO

SYS_NORTH_RESET FROM SMU TO NB_PU_RST

SAME AS Q63

=PP3V3_PWRON_SMU

R3006 10K 5% 1/16W MF-LF 402

R3010 4.7K 5% 1/16W MF-LF 402

NB_PU_RESET

=PP2V5_PWRON_NB_MISC

R3007 4.7K 5% 1/16W MF-LF 402

NB_PU_RST_L

SYS_NORTH_RESET_L

Q3005 2N7002DW-X-F SOT-363

Q3000 2N7002DW-X-F SOT-363

NOSTUFF R3008 0 5% 1/16W MF-LF 402

SYS_NORTH_RESET_L_R

NOSTUFF R3098 0 5% 1/16W MF-LF 402

NOSTUFF Q3006 2N7002 SOT23-LF

SYS_SLEEP

NOSTUFF R3009 0 5% 1/16W MF-LF 402

SYS_2SLEEP_R

CONSIDER COMBINING Q3040 AND Q3006 TO A DUAL PART

SHARE CPU AND NB JTAG TDO WITH SMU

=PP3V3_PWRON_SMU

SMU DRIVES 3.3V PUSH-PULL ON ALL JTAG-RELATED PINS

CRITICAL

U3070 SN74LVC2G157 TSSOP

PCB: PLACE U3070 NEAR SMU

JTAG_CPU_TDO_3V3

JTAG_NB_TDO

SMU_CPU_NB_SEL

VIH=2V

SMU_JTAG_TDO

NC_JTAGMUX_3

C3070 0.1UF 20% 16V CERM 402

SMU JTAG TDI TO CPU (BACKUP PLAN)

=PPV_EI_CPU

R3084 1K 5% 1/16W MF-LF 402

R3085 33 5% 1/16W MF-LF 402

JTAG_CPU_TDI

=PP3V3_RUN_SMU

R3083 4.7K 5% 1/16W MF-LF 402

Q3081 2N7002DW-X-F SOT-363

SMU_JTAG_TDI_L

Q3080 2N7002DW-X-F SOT-363

SMU_JTAG_TDI

SHARE CPU AND NB JTAG TMS WITH SMU

=PP2V5_PWRON_NB_MISC

C3071 0.1UF 20% 16V CERM 402

PCB: PLACE U3071 NEAR SMU OR NEAR KODIAK.

CRITICAL

U3071 74LVC1G SC70-6

TO LEVEL SHIFTER

SMU_CPU_TMS

3.3V TOLERANT

STRAIGHT TO NB

JTAG_NB_TMS

SMU_JTAG_TMS

LEVEL SHIFT TDO FROM CPU TO MUX

=PP3V3_PWRON_SMU

R3051 1K 5% 1/16W MF-LF 402

R3052 100 5% 1/16W MF-LF 402

JTAG_CPU_TDO_L

JTAG_CPU_TDO_3V3

JTAG_CPU_TDO_R

R3050 10K 5% 1/16W MF-LF 402

Q3050 2N3904LF SOT23

Q3021 2N7002DW-X-F SOT-363

JTAG_CPU_TDO

PCB: PLACE R3050, Q3050, R3051 NEAR CPU. PLACE Q3021, R3052 NEAR SMU.

MISC. SMU BUFFERS

SAME AS (Q63).

=PP3V3_PWRON_SMU

R3021 4.7K 5% 1/16W MF-LF 402

U700 IS POWERED BY PP3V3_ALL

U700 74LC125 TSSOP

SMU_IO_RESET_L

SYS_IO_RST_L_R

R3022 100 5% 1/16W MF-LF 402

SYS_IO_RESET_L

U700 74LC125 TSSOP

SMU_SLEEP

SYS_SLEEP_R

R3023 100 5% 1/16W MF-LF 402

SYS_SLEEP

SMU JTAG TCK TO CPU (BACKUP PLAN)

=PPV_EI_CPU

R3081 1K 5% 1/16W MF-LF 402

R3082 33 5% 1/16W MF-LF 402

JTAG_CPU_TCK

JTAG_CPU_TCK_2_R

=PP3V3_RUN_SMU

R3080 4.7K 5% 1/16W MF-LF 402

Q3081 2N7002DW-X-F SOT-363

SMU_JTAG_TCK_L

Q3080 2N7002DW-X-F SOT-363

SMU_JTAG_TCK

STUFF IF USING REGISTERED DIMM

=PP3V3_PWRON_SMU

NOSTUFF R3040 1K 5% 1/16W MF-LF 402

SMU_IO_RESET

NOSTUFF Q3040 2N7002 SOT23-LF

SYS_IO_RST_L_R

SHARE SMU JTAG TCK WITH CPU AND NB (PRIMARY PLAN)
SHARE SMU JTAG TDI WITH CPU AND NB (PRIMARY PLAN)
NOTE: WE WENT WITH BACKUP PLAN, PRIMARY REMOVED TO AVOID STUBS

NB JTAG IS A DEVELOPMENT ONLY FEATURE
PLACE O-OHM R3030 AND R3031 TO AVOID STUBS
R3030,R3031,C3031,U3031,R3032,R3033 SHOULD MOVE TO DEVELOPMENT BOM POST RAMP

SMU_JTAG_TDI

R3030 0 5% 1/16W MF-LF 402

=PP2V5_PWRON_NB_MISC

C3031 0.1UF 20% 16V CERM 402

VCC RANGE 0.8V - 2.7V

U3031 SN74AUC2G34 SOT23-6

R3034 10K 5% 1/16W MF-LF 402

VIH = 2.0V, 3.3V TOLERANT

SMU_JTAG_NB_TDI

R3032 33 5% 1/16W MF-LF 402

JTAG_NB_TDI_R

JTAG_NB_TDI

PCB: PLACE U3030 AND U3031 NEAR CPU AND KODIAK.
PCB: PLACE 33 OHM RES NEAR U3030/31 PART.

SMU_JTAG_TCK

R3031 0 5% 1/16W MF-LF 402

=PP2V5_PWRON_NB_MISC

SMU_JTAG_NB_TCK

VCC RANGE 0.8V - 2.7V

U3031 SN74AUC2G34 SOT23-6

VIH = 2.0V, 3.3V TOLERANT

R3033 33 5% 1/16W MF-LF 402

JTAG_NB_TCK_R

R3035 10K 5% 1/16W MF-LF 402

PULLUP IF KODIAK JTAG IS NOSTUFFED

JTAG_NB_TCK

PULLDOWNS TO BUFFERS/LOGIC GATES

R3036 100K 5% 1/16W MF-LF 402

SMU_JTAG_TDI

R3037 100K 5% 1/16W MF-LF 402

SMU_JTAG_TCK

R3070 100K 5% 1/16W MF-LF 402

SMU_JTAG_TMS

R3071 100K 5% 1/16W MF-LF 402

SMU_CPU_NB_SEL

NB SUSPEND_ACK_L LEVEL 2.5V TO 3.3V LEVEL SHIFTER

=PP3V3_PWRON_SMU

R3091 1K 5% 1/16W MF-LF 402

R3093 1K 5% 1/16W MF-LF 402

NB_SUSPEND_ACK_L_R

NB_SUSPENDACK

NB_SUSPENDACK_L

R3090 10K 5% 1/16W MF-LF 402

Q3090 2N3904LF SOT23

Q3021 2N7002DW-X-F SOT-363

NB_SUSPEND_ACK_L

NOSTUFF R3092 0 5% 1/16W MF-LF 402

LEVEL SHIFT SMU TMS TO CPU (BACKUP PLAN)

=PPV_EI_CPU

=PP3V3_PWRON_SMU

R3026 1K 5% 1/16W MF-LF 402

R3027 1K 5% 1/16W MF-LF 402

R3028 33 5% 1/16W MF-LF 402

JTAG_CPU_TMS_2_L

JTAG_CPU_TMS_2_R

JTAG_CPU_TMS

JTAG_SMU_TMS_2_R

R3020 10K 5% 1/16W MF-LF 402

Q3030 2N3904LF SOT23

Q3031 2N7002DW-X-F SOT-363

SMU_CPU_TMS

LEFTOVER FROM UNUSED PRIMARY PLAN - NOT STUFFED

NOSTUFF U5640 SN74AUC1G125 SSOP

125

SMU SUPPLEMENTAL (3)

SYNC_MASTER=FINO-M23 SYNC_DATE=09/20/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 30 OF 154	

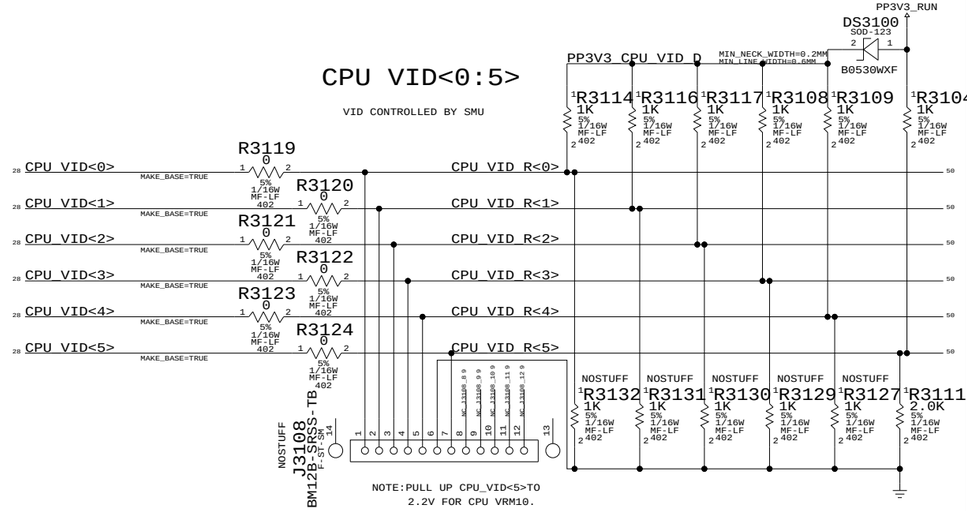
SMU ALIASES

ALIASES ARE ONLY NECESSARY WHERE USE DIFFERS FROM Q63.

COMMENT (ONLY IF USE DIFFERS FROM Q63)	M23 NET NAME	M23 SMU ALLOCATION		Q63 NET NAME (SHARED PAGE)
		CPU_SENSE_I0	P0.0	
		CPU_SENSE_V0	P0.1	
		CPU_TEMP0	P0.2	
Q63 NC'S THESE AS IT USES A SAT.		CPU_BYPASS	P0.3	
	9 NC_SMU_FAN_RPM3	FAN_CNTL0_4	P0.4	SMU_FAN_RPM3 28
M23/M33 DOESN'T HAVE THOSE FANS.	9 NC_SMU_FAN_RPM4	FAN_CNTL0_5	P0.5	SMU_FAN_RPM4 28
	9 NC_SMU_FAN_RPM5	FAN_CNTL0_6	P0.6	SMU_FAN_RPM5 28
Q63 USES SMU_SER_SEL FOR SPDIF-SMU-DEBUG. NOT M23/M33 FEATURE.	9 NC_SMU_SER_SEL	SMU_SCCL_SEL	P0.7	SMU_SER_SEL 28
M23/M33 DOESN'T USE. P1.0 NC ON PG 7.		CPU_SENSE_I1	P1.0	
		CPU_SENSE_V1	P1.1	
SMU USES P1.1, P1.2, P1.3, P9.5, P9.6 FOR PWRSEQ ON PG 7.		CPU_TEMP1	P1.2	
		PS1_3	P1.3	
M23/M33 DOESN'T USE P1.4. NC ON PG 7.		PS1_4	P1.4	
		POWERFAIL*	P1.5	
CPU_VID_LE0 FOR Q82. NOT M23/M33 FEATURE.	9 NC_SMU_CPU_VID_LE0	CPU_VID_LE0	P1.6	SMU_FAN_TACH9 28
CONSIDER DOOR_AJAR FOR M23/M33 DIMM ACCESS DOOR?	9 NC_SYS_DOOR_AJAR_L	DOOR_AJAR*	P1.7	SYS_DOOR_AJAR_L 28
CPU_VID_LE1 FOR Q82. NOT M23/M33 FEATURE.	9 NC_SMU_CPU_VID_LE1	CPU_VID_LE1	P2.0	SMU_FAN_TACH6 28
M23/M33 DOESN'T HAVE THIS FAN.	9 NC_SMU_FAN_TACH7	FAN_TACH2_1	P2.1	SMU_FAN_TACH7 28
		FAN_TACH2_2	P2.2	
		FAN_TACH2_3	P2.3	
		FAN_TACH2_4	P2.4	
M23/M33 DOESN'T HAVE FAN TACHS P2.5, P2.6, P2.7.	9 NC_SMU_FAN_TACH3	FAN_TACH2_5	P2.5	SMU_FAN_TACH3 28
M23/M33 USES TACH0 (P2.2), TACH1 (P2.3), TACH2 (P2.4) ONLY.	9 NC_SMU_FAN_TACH4	FAN_TACH2_6	P2.6	SMU_FAN_TACH4 28
	9 NC_SMU_FAN_TACH5	FAN_TACH2_7	P2.7	SMU_FAN_TACH5 28
M23/M33 ONLY CONNECTS I2C TO KODIAK NOW; CPU HAS PULLUPS ON ITS PG.	39 28 I2C_SMU_A_SDA	IIC_A_DAT	P3.0	I2C_SMU_A_SDA_IN 28
	39 28 I2C_SMU_A_SCL	IIC_A_CLK	P3.1	I2C_SMU_A_SDA_OUT_L 28
	30 SMU_JTAG_TDI	TDI	P3.2	I2C_SMU_A_SCL_IN 28
	30 SMU_JTAG_TCK	TCK	P3.3	I2C_SMU_A_SCL_OUT_L 28
		IIC_E_DAT	P3.4	
		IIC_E_CLK	P3.5	
		DIAG_LED	P3.6	
		OVERTEMP*	P3.7	
		CPU_VID[0]	P6.0	
		CPU_VID[1]	P6.1	
		CPU_VID[2]	P6.2	
		CPU_VID[3]	P6.3	
		CPU_VID[4]	P6.4	
		CPU_VID[5]	P6.5	
		DEBUG_RXD	P6.6	
		DEBUG_TXD	P6.7	
		IIC_B_DAT	P7.0	
		IIC_B_CLK	P7.1	
Q63 USE OF P7.2 IS PWM FAN — SELECT BETWEEN CPU OR NB TMS AND TDO FROM/TO SMU	30 SMU_CPU_NB_SEL	CPU_TMS	P7.2	I2C_SMU_CPU_SDA_IN 28
		FAN_CNTL7_3	P7.3	
M23/M33 DOESN'T HAVE THIS FAN (P7.4)	9 NC_I2C_SMU_CPU_SCL_IN	FAN_CNTL7_4	P7.4	I2C_SMU_CPU_SCL_IN 28
M23/M33 USES FAN_RPM0 (P7.3), FAN_RPM1 (P7.5), FAN_RPM2 (P7.7) ONLY.		FAN_CNTL7_5	P7.5	
		VDNAP2	P7.6	
		FAN_CNTL7_7	P7.7	
		SYSTEM_LED	P8.0	
		NB_RESET*	P8.1	
		PME*	P8.2	
M23/M33 DOESN'T NEED TO MAKE VDNAP0 DO TRIPLE-DUTY.	24 SB_VDNAP0	VDNAP0	P8.3	SB_CPU_VDNAP0_OR_QREQ_OR_SPDIF 28
		SLEWING*	P8.4	
	30 SMU_JTAG_TMS	NB_TMS	P8.5	I2C_SMU_CPU_SDA_OUT_L 28
		POWERUP*	P8.6	
		SLEEP	P8.7	
		CLK_RESET*	P9.0	
Q63 USE OF P9.1 IS TACH 8.	29 CPU_HRESET	CPU_HRESET	P9.1	SMU_FAN_TACH8 28
		SMU_DOORBELL*	P9.2	
		STOP_XTAL*	P9.3	
SMU USES P1.1, P1.2, P1.3, P9.5, P9.6 FOR PWRSEQ ON PG 7.		PS9_5	P9.5	
		PS9_6	P9.6	
M23/M33 HAS NO SLOTS.	9 NC_SLOT_TOTAL_PWR	SLOT_TOTAL_PWR	P9.7	SYS_SLOT_PWR 28
		VDNAP1	P10.0	
		IO_RESET*	P10.1	
		SUSPEND_ACK*	P10.2	
		SUSPEND_IO_ACK*	P10.3	
		SUSPEND_REQ*	P10.4	
		PWR_BUTTON*	P10.5	
		RST_BUTTON*	P10.6	
	30 SMU_JTAG_TDO	TDO	P10.7	I2C_SMU_CPU_SCL_OUT_L 28

CPU VID<0:5>

VID CONTROLLED BY SMU



NOTE:PULL UP CPU_VID<5>TO 2.2V FOR CPU VRM10.

NOTE: SC2642 VID PINS HAVE LEAKAGE TO GND. SO PULLUPS MUST BE 1K

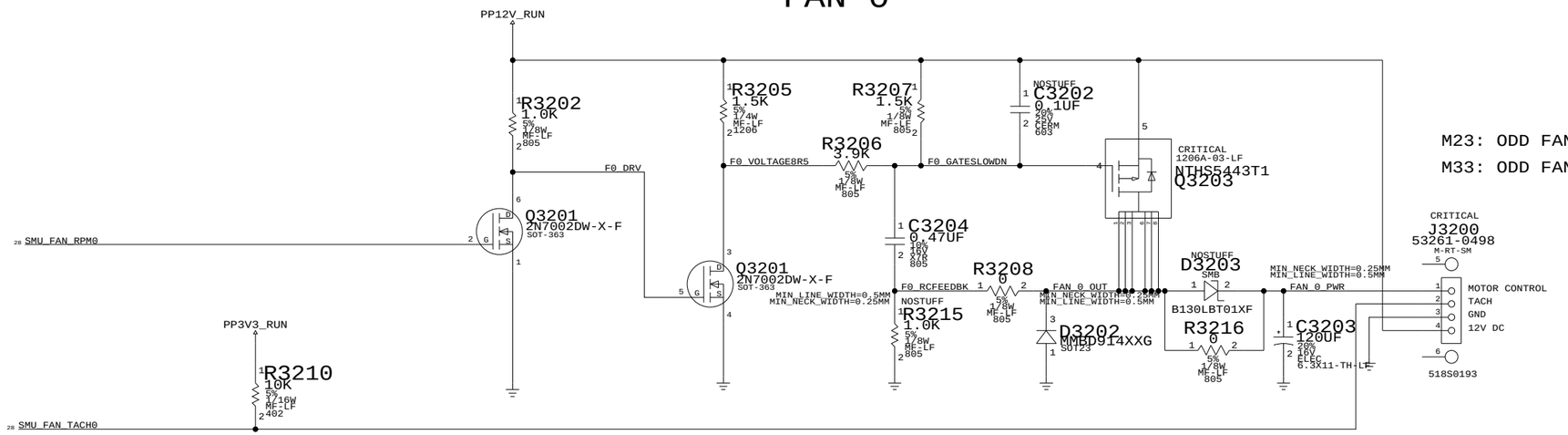
SMU SUPPLEMENTAL (4)

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE COMPUTER INC.

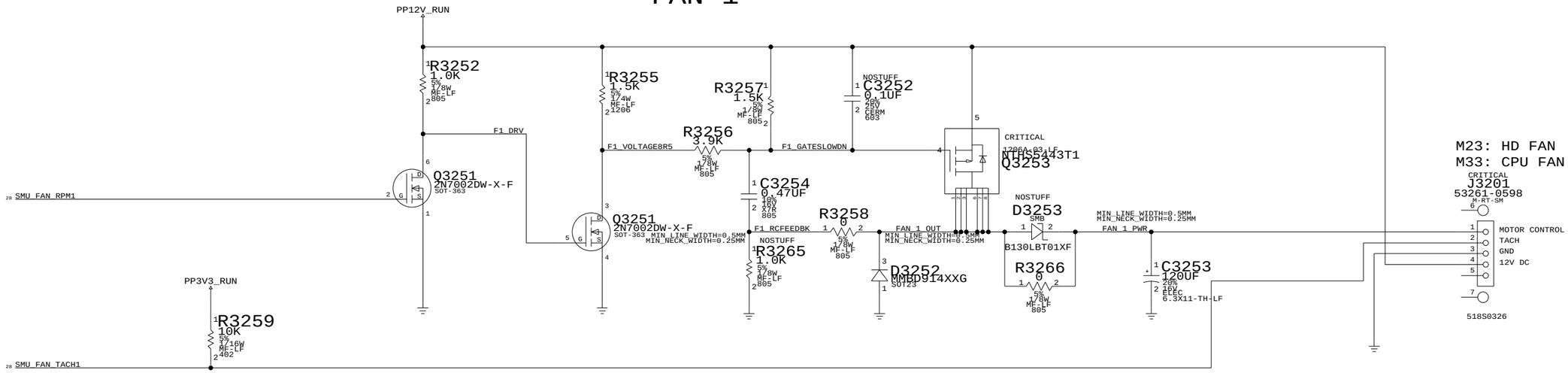
SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 31 OF 154	

FAN 0



M23: ODD FAN
M33: ODD FAN

FAN 1



M23: HD FAN
M33: CPU FAN

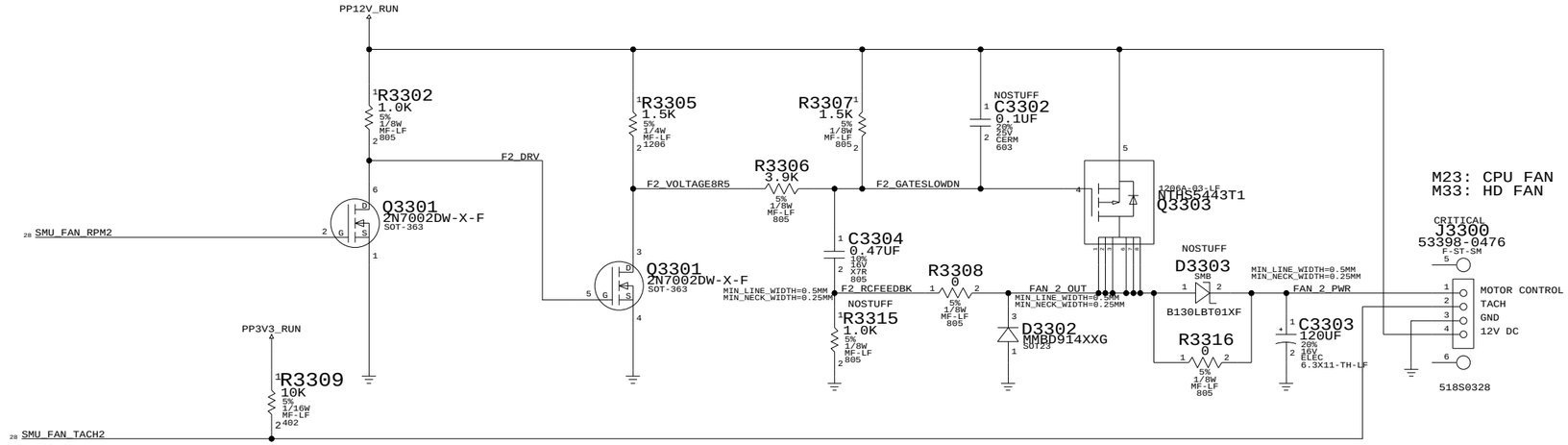
Fan 0, 1 & System Temp

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

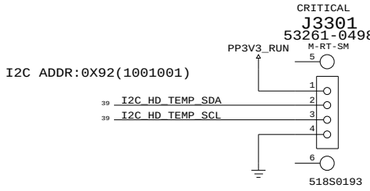
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 32 OF 154	

FAN 2

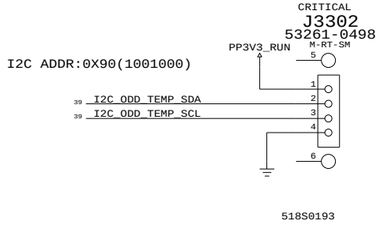


HD TEMP SENSOR



NOTE: BROKE SYNC ON THIS PAGE
TO ALLOW EMC CAPS ON M23 ONLY

ODD TEMP SENSOR



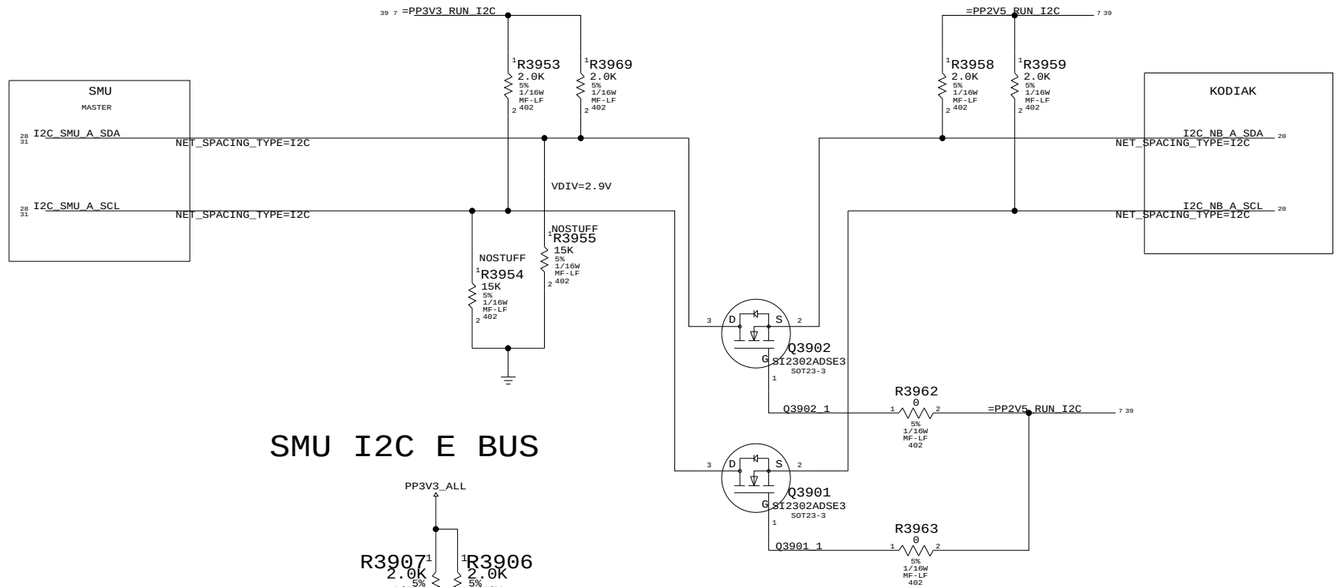
Fan 2 & HD Temp

SYNC_MASTER=M33-HS SYNC_DATE=08/04/2005

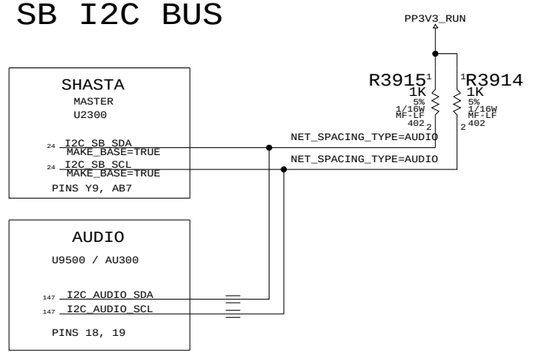
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 33 OF 154	

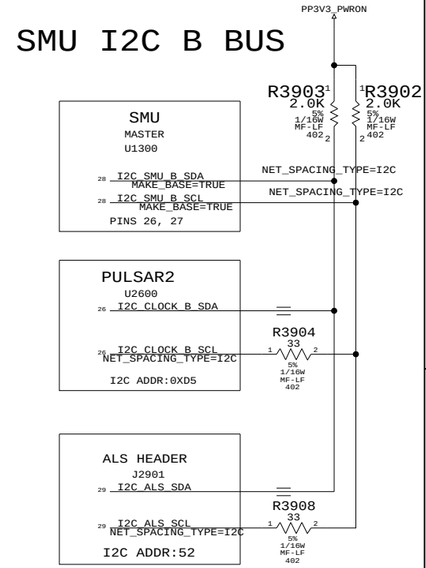
SMU AND NB I2C A BUS



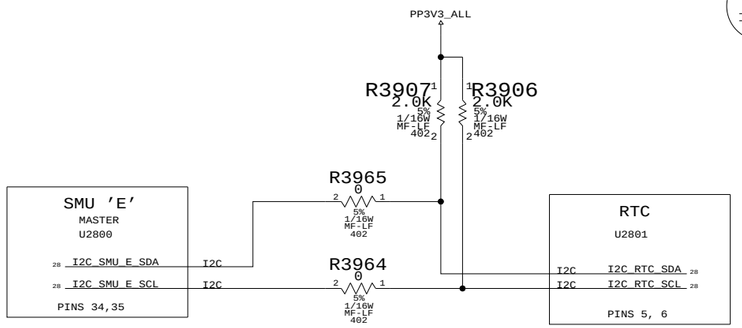
SB I2C BUS



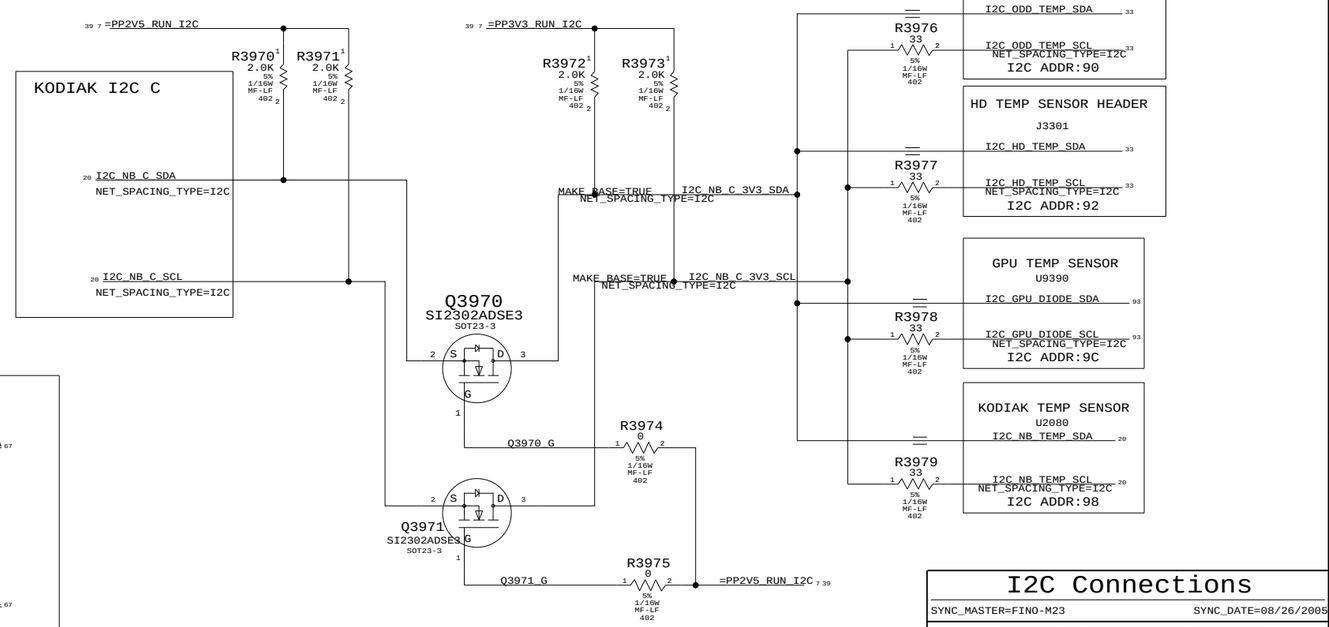
SMU I2C B BUS



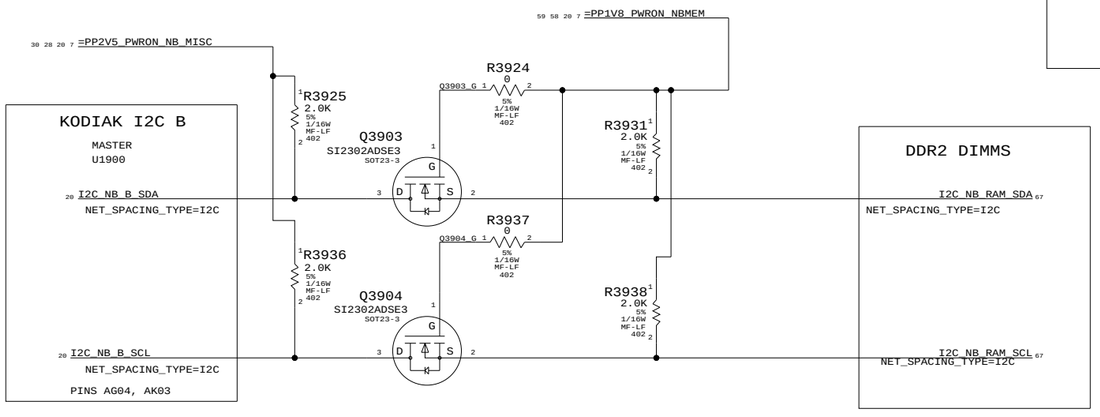
SMU I2C E BUS



NB I2C C BUS



NB I2C B BUS

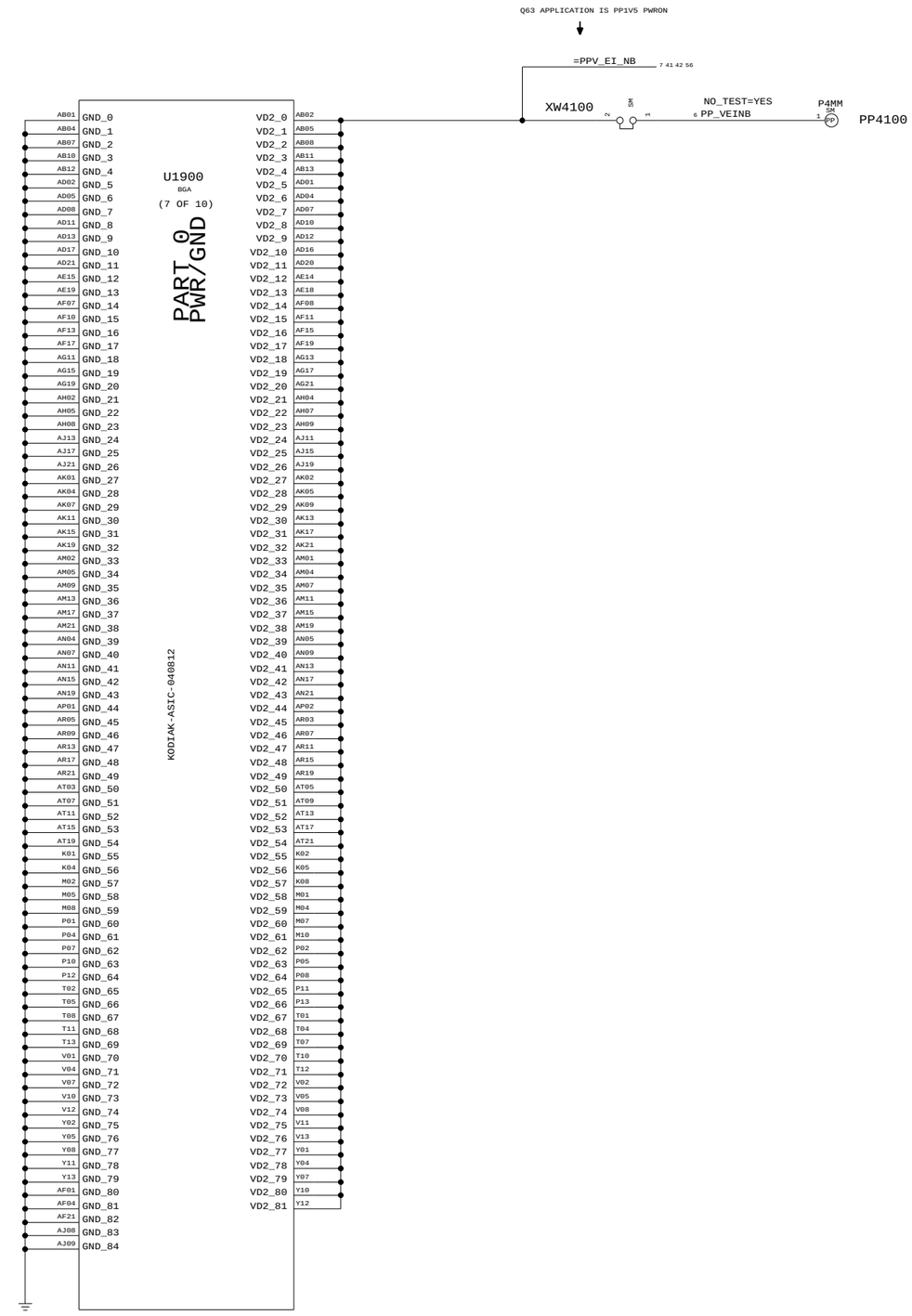


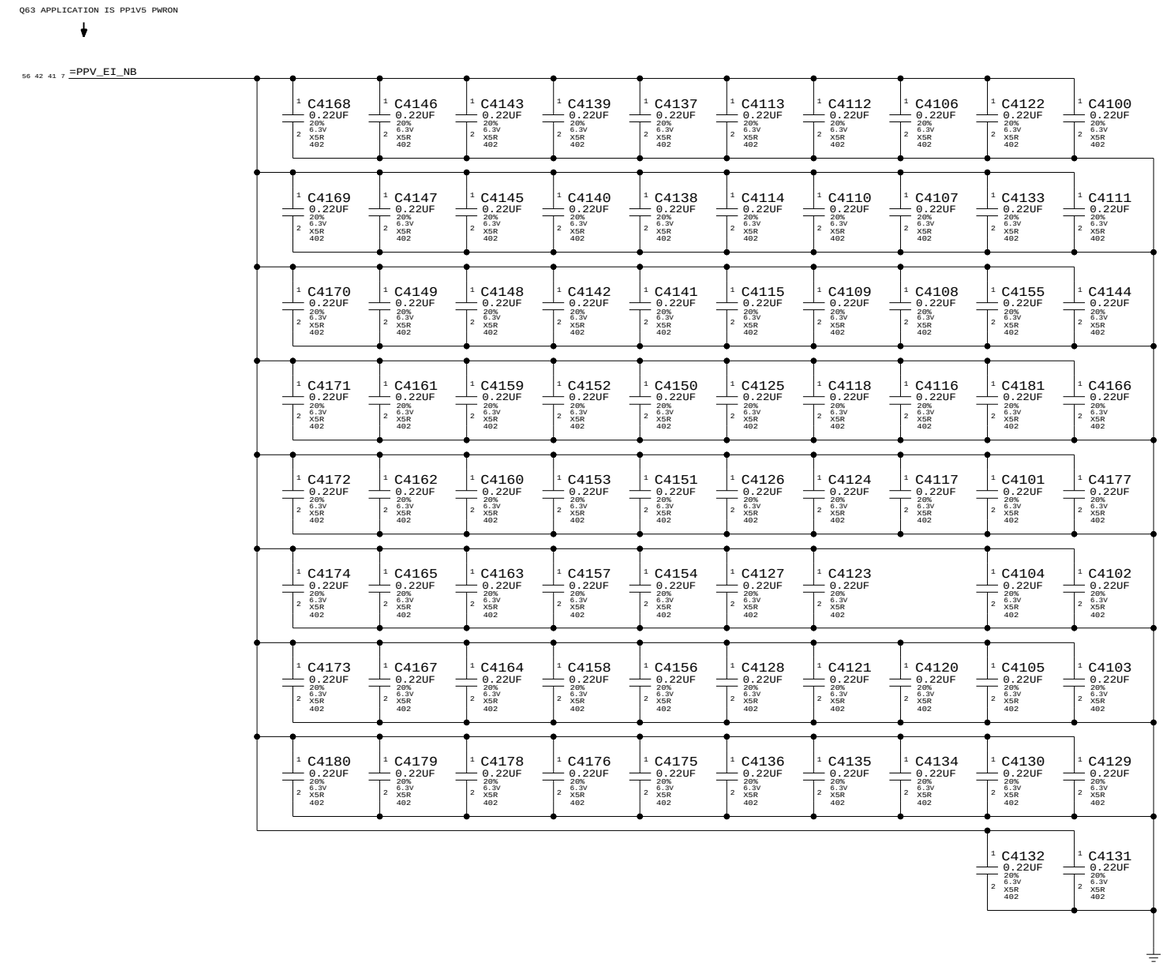
I2C Connections

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 39 OF 154	





LAST_MODIFIED=Tue Nov 1 13:46:30 2005

DRAWING

TITLE=KILOHMA

ABORDEV=SHAWING

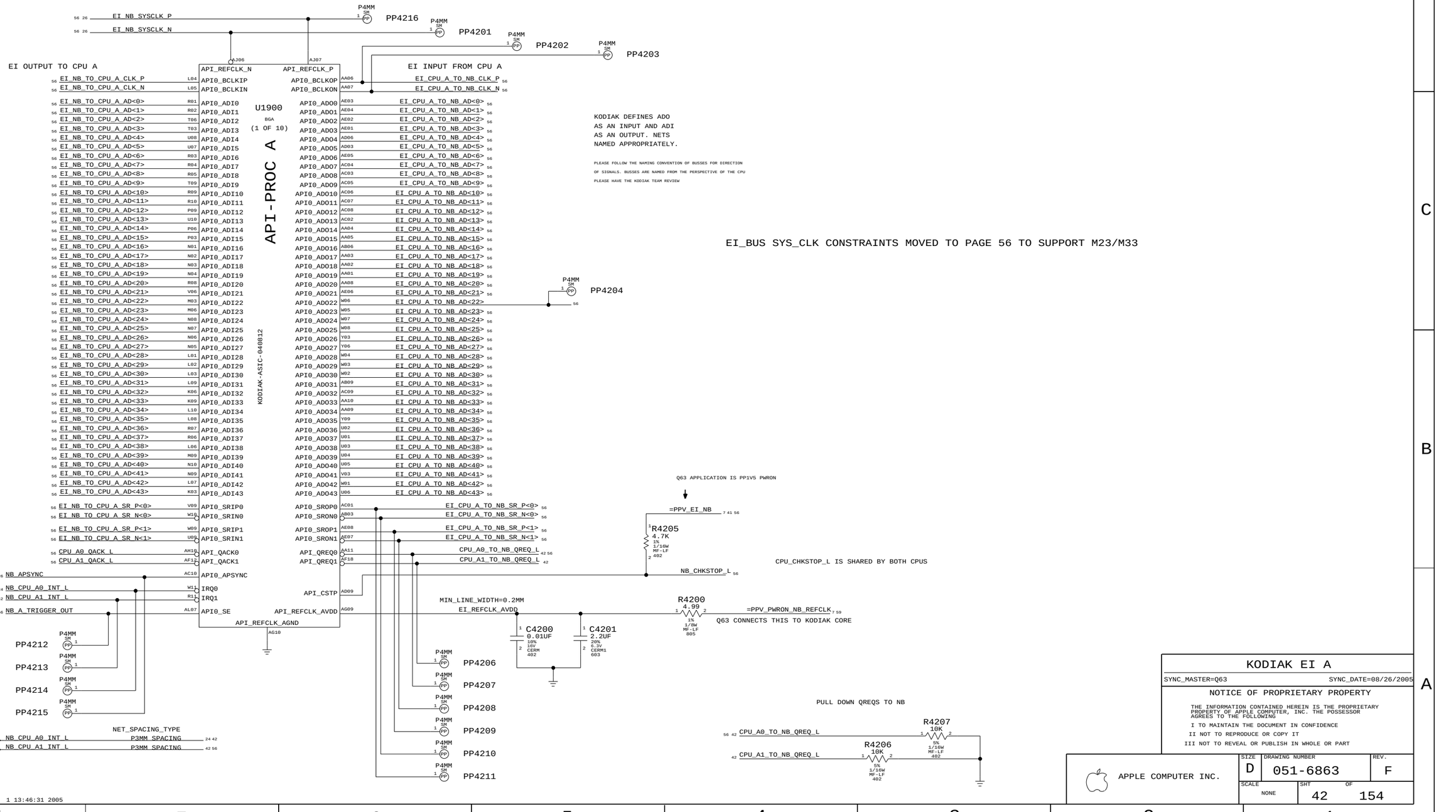
KODIAK EI PWR & CAPS

SYNC_MASTER=Q63 SYNC_DATE=08/26/2005

APPLE COMPUTER INC.

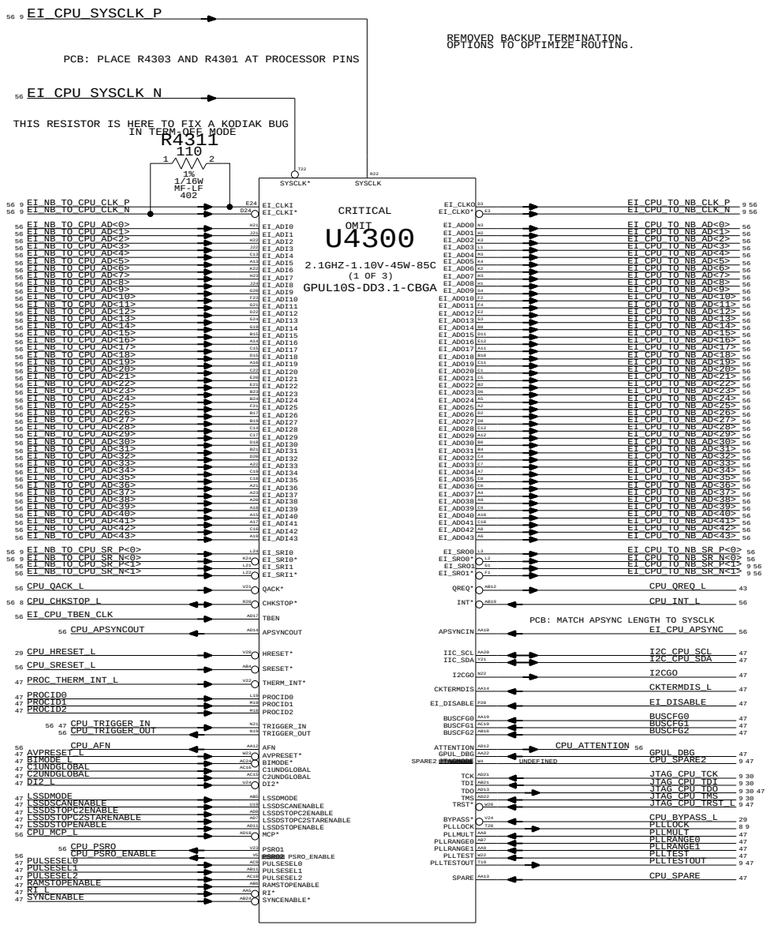
SIZE	DRAWING NUMBER	REV.
D	051-6863	F

SCALE	SHT	OF
NONE	41	154



KODIAK EI A			
SYNC_MASTER=Q63	SYNC_DATE=08/26/2005		
NOTICE OF PROPRIETARY PROPERTY			
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART			
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6863	REV. F
	SCALE NONE	SHT 42 OF 154	

DRAWING



PG 49 & 52 HAVE MORE CAPS

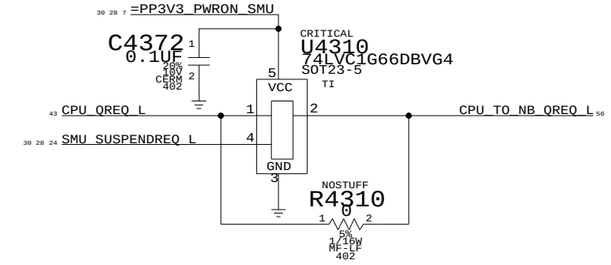
=PPVCORE_CPU

C4353 C4347 C4345 C4339 C4337 C4328 C4324 C4320 C4314 C4312
C4354 C4348 C4346 C4340 C4338 C4329 C4325 C4321 C4315 C4313
C4355 C4351 C4349 C4343 C4341 C4330 C4326 C4322 C4318 C4316
C4356 C4352 C4350 C4344 C4342 C4331 C4327 C4323 C4319 C4317
C4300 C4360 C4359 C4358 C4357 C4336 C4335 C4334 C4333 C4332
C4311 C4310 C4309 C4308 C4307 C4306 C4305 C4304 C4303 C4302

1UF 10% 6.3V CERM 402

QREQ_L AND SUSPENDREQ_L AND HACK

SAME AS Q45



CPU EI AND IO

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT: 43 OF 154	

PLEASE FOLLOW THE NAMING CONVENTION OF BUSSES FOR DIRECTION
OF SIGNALS. BUSSES ARE NAMED FROM THE PERSPECTIVE OF THE CPU
PLEASE HAVE THE KODIAK TEAM REVIEW

EI OUTPUT TO CPU B

EI INPUT FROM CPU B

U1900
BGA
(2 OF 10)
API-PROC B
KODIAK-ASIC-040812

EI_NB_TO_CPU_B_CLK_P	AT08	API1_BCLKIP	API1_BCLKOP	AT16	EI_CPU_B_TO_NB_CLK_P
EI_NB_TO_CPU_B_CLK_N	AR08	API1_BCLKIN	API1_BCLKON	AR16	EI_CPU_B_TO_NB_CLK_N
EI_NB_TO_CPU_B_AD<0>	AM12	API1_ADI0	API1_AD00	AP20	EI_CPU_B_TO_NB_AD<0>
EI_NB_TO_CPU_B_AD<1>	AN12	API1_ADI1	API1_AD01	AN20	EI_CPU_B_TO_NB_AD<1>
EI_NB_TO_CPU_B_AD<2>	AL12	API1_ADI2	API1_AD02	AR20	EI_CPU_B_TO_NB_AD<2>
EI_NB_TO_CPU_B_AD<3>	AK12	API1_ADI3	API1_AD03	AT20	EI_CPU_B_TO_NB_AD<3>
EI_NB_TO_CPU_B_AD<4>	AP11	API1_ADI4	API1_AD04	AL19	EI_CPU_B_TO_NB_AD<4>
EI_NB_TO_CPU_B_AD<5>	AL11	API1_ADI5	API1_AD05	AP19	EI_CPU_B_TO_NB_AD<5>
EI_NB_TO_CPU_B_AD<6>	AP12	API1_ADI6	API1_AD06	AM20	EI_CPU_B_TO_NB_AD<6>
EI_NB_TO_CPU_B_AD<7>	AR12	API1_ADI7	API1_AD07	AM18	EI_CPU_B_TO_NB_AD<7>
EI_NB_TO_CPU_B_AD<8>	AT12	API1_ADI8	API1_AD08	AL18	EI_CPU_B_TO_NB_AD<8>
EI_NB_TO_CPU_B_AD<9>	AH12	API1_ADI9	API1_AD09	AN18	EI_CPU_B_TO_NB_AD<9>
EI_NB_TO_CPU_B_AD<10>	AG12	API1_ADI10	API1_AD010	AP18	EI_CPU_B_TO_NB_AD<10>
EI_NB_TO_CPU_B_AD<11>	AH13	API1_ADI11	API1_AD011	AR18	EI_CPU_B_TO_NB_AD<11>
EI_NB_TO_CPU_B_AD<12>	AJ12	API1_ADI12	API1_AD012	AT18	EI_CPU_B_TO_NB_AD<12>
EI_NB_TO_CPU_B_AD<13>	AG14	API1_ADI13	API1_AD013	AK18	EI_CPU_B_TO_NB_AD<13>
EI_NB_TO_CPU_B_AD<14>	AM10	API1_ADI14	API1_AD014	AP17	EI_CPU_B_TO_NB_AD<14>
EI_NB_TO_CPU_B_AD<15>	AL10	API1_ADI15	API1_AD015	AL17	EI_CPU_B_TO_NB_AD<15>
EI_NB_TO_CPU_B_AD<16>	AN10	API1_ADI16	API1_AD016	AH20	EI_CPU_B_TO_NB_AD<16>
EI_NB_TO_CPU_B_AD<17>	AP10	API1_ADI17	API1_AD017	AJ20	EI_CPU_B_TO_NB_AD<17>
EI_NB_TO_CPU_B_AD<18>	AR10	API1_ADI18	API1_AD018	AK20	EI_CPU_B_TO_NB_AD<18>
EI_NB_TO_CPU_B_AD<19>	AT10	API1_ADI19	API1_AD019	AH19	EI_CPU_B_TO_NB_AD<19>
EI_NB_TO_CPU_B_AD<20>	AK10	API1_ADI20	API1_AD020	AG20	EI_CPU_B_TO_NB_AD<20>
EI_NB_TO_CPU_B_AD<21>	AJ10	API1_ADI21	API1_AD021	AL20	EI_CPU_B_TO_NB_AD<21>
EI_NB_TO_CPU_B_AD<22>	AM08	API1_ADI22	API1_AD022	AM16	EI_CPU_B_TO_NB_AD<22>
EI_NB_TO_CPU_B_AD<23>	AN08	API1_ADI23	API1_AD023	AN16	EI_CPU_B_TO_NB_AD<23>
EI_NB_TO_CPU_B_AD<24>	AL08	API1_ADI24	API1_AD024	AL16	EI_CPU_B_TO_NB_AD<24>
EI_NB_TO_CPU_B_AD<25>	AP07	API1_ADI25	API1_AD025	AK16	EI_CPU_B_TO_NB_AD<25>
EI_NB_TO_CPU_B_AD<26>	AT06	API1_ADI26	API1_AD026	AP15	EI_CPU_B_TO_NB_AD<26>
EI_NB_TO_CPU_B_AD<27>	AR06	API1_ADI27	API1_AD027	AL15	EI_CPU_B_TO_NB_AD<27>
EI_NB_TO_CPU_B_AD<28>	AP08	API1_ADI28	API1_AD028	AP16	EI_CPU_B_TO_NB_AD<28>
EI_NB_TO_CPU_B_AD<29>	AT04	API1_ADI29	API1_AD029	AM14	EI_CPU_B_TO_NB_AD<29>
EI_NB_TO_CPU_B_AD<30>	AR04	API1_ADI30	API1_AD030	AL14	EI_CPU_B_TO_NB_AD<30>
EI_NB_TO_CPU_B_AD<31>	AP05	API1_ADI31	API1_AD031	AN14	EI_CPU_B_TO_NB_AD<31>
EI_NB_TO_CPU_B_AD<32>	AM06	API1_ADI32	API1_AD032	AP14	EI_CPU_B_TO_NB_AD<32>
EI_NB_TO_CPU_B_AD<33>	AN06	API1_ADI33	API1_AD033	AR14	EI_CPU_B_TO_NB_AD<33>
EI_NB_TO_CPU_B_AD<34>	AP06	API1_ADI34	API1_AD034	AT14	EI_CPU_B_TO_NB_AD<34>
EI_NB_TO_CPU_B_AD<35>	AP04	API1_ADI35	API1_AD035	AK14	EI_CPU_B_TO_NB_AD<35>
EI_NB_TO_CPU_B_AD<36>	AM03	API1_ADI36	API1_AD036	AP13	EI_CPU_B_TO_NB_AD<36>
EI_NB_TO_CPU_B_AD<37>	AN01	API1_ADI37	API1_AD037	AL13	EI_CPU_B_TO_NB_AD<37>
EI_NB_TO_CPU_B_AD<38>	AL06	API1_ADI38	API1_AD038	AG16	EI_CPU_B_TO_NB_AD<38>
EI_NB_TO_CPU_B_AD<39>	AL05	API1_ADI39	API1_AD039	AH15	EI_CPU_B_TO_NB_AD<39>
EI_NB_TO_CPU_B_AD<40>	AL04	API1_ADI40	API1_AD040	AJ14	EI_CPU_B_TO_NB_AD<40>
EI_NB_TO_CPU_B_AD<41>	AL03	API1_ADI41	API1_AD041	AH14	EI_CPU_B_TO_NB_AD<41>
EI_NB_TO_CPU_B_AD<42>	AN02	API1_ADI42	API1_AD042	AH16	EI_CPU_B_TO_NB_AD<42>
EI_NB_TO_CPU_B_AD<43>	AN03	API1_ADI43	API1_AD043	AH17	EI_CPU_B_TO_NB_AD<43>
EI_NB_TO_CPU_B_SR_P<0>	AP09	API1_SRIP0	API1_SROP0	AG18	EI_CPU_B_TO_NB_SR_P<0>
EI_NB_TO_CPU_B_SR_N<0>	AL09	API1_SRIN0	API1_SRON0	AJ16	EI_CPU_B_TO_NB_SR_N<0>
EI_NB_TO_CPU_B_SR_P<1>	AR02	API1_SRIP1	API1_SROP1	AJ18	EI_CPU_B_TO_NB_SR_P<1>
EI_NB_TO_CPU_B_SR_N<1>	AP02	API1_SRIN1	API1_SRON1	AH18	EI_CPU_B_TO_NB_SR_N<1>
CPU_B0_QACK_L	AF12	API_QACK2	API_QREQ2	AF16	CPU_B0_TO_NB_QREQ_L
CPU_B1_QACK_L	AC12	API_QACK3	API_QREQ3	AF20	CPU_B1_TO_NB_QREQ_L
NB_CPU_B0_INT_L	N12	IRQ2			
NB_CPU_B1_INT_L	U12	IRQ3			
TP_NB_APSYNC	AH11	API1_APSYNC			
NB_B_TRIGGER_OUT	AK08	API1_SE			

KODIAK DEFINES ADO
AS AN INPUT AND ADI
AS AN OUTPUT. NETS
NAMED APPROPRIATELY.

WE MAY NEED A DIFFERENT
ELECTRICAL_CONSTRAINT_SET
FOR CPU_A AND CPU_B.

EI_BUS SYS_CLK CONSTRAINTS MOVED TO PAGE 56 TO SUPPORT M23/M33

WIRE TP_NB_APSYNC TO A TEST POINT

P4MM SM
PP4410
PP4411
PP4413
PP4400
PP4401
PP4402
PP4403
PP4404
PP4405
PP4406
PP4407
PP4408

NET_SPACING_TYPE

NB_CPU_B0_INT_L	P3MM_SPACING	44 56
NB_CPU_B1_INT_L	P3MM_SPACING	44 56

PULL DOWN QREQS TO NB

CPU_B0_TO_NB_QREQ_L — R4407 10K 5% 1/16W MF-LF 402
CPU_B1_TO_NB_QREQ_L — R4406 10K 5% 1/16W MF-LF 402

KODIAK EI B

SYNC_MASTER=Q63 SYNC_DATE=08/26/2005

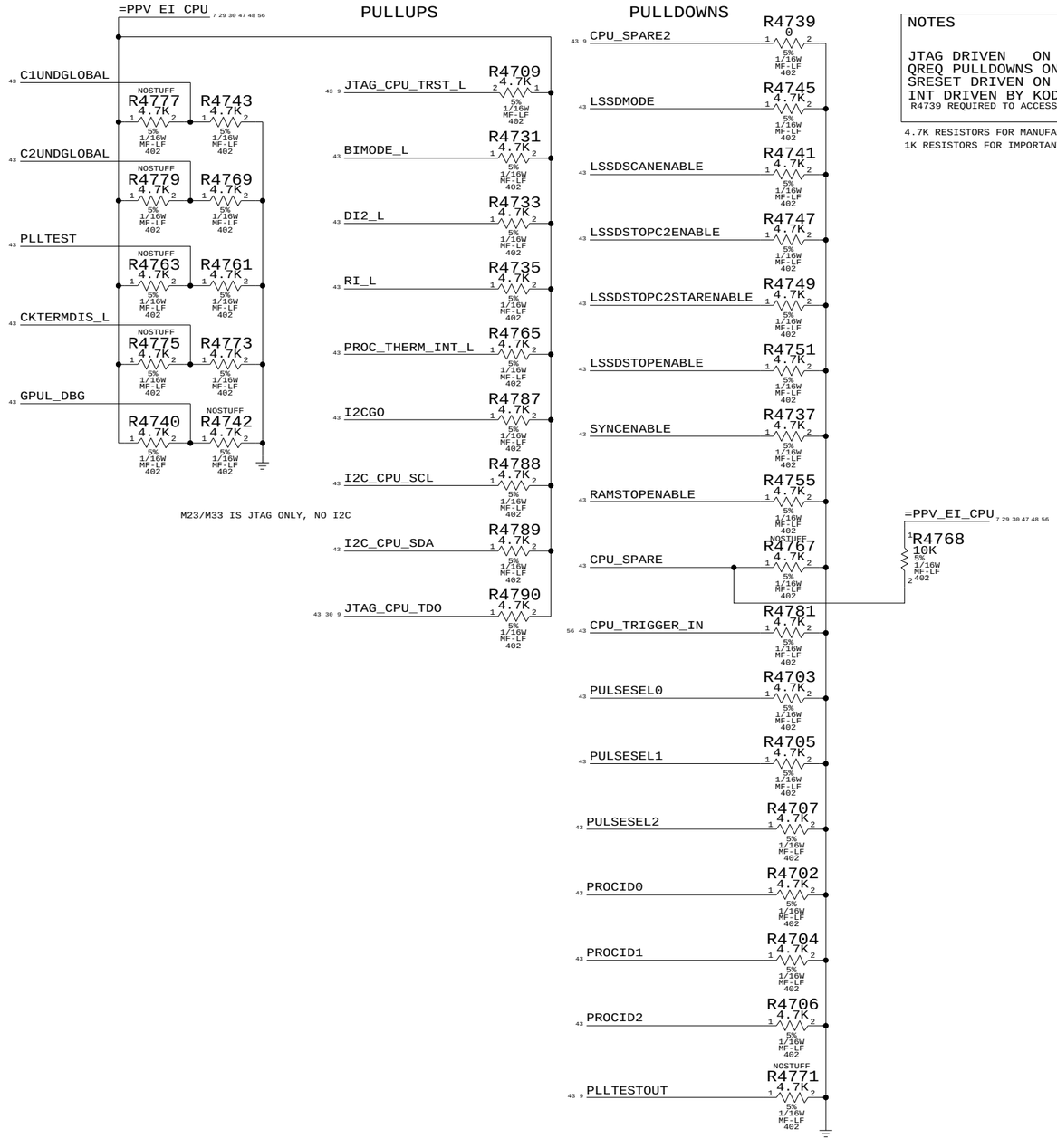
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F

SCALE: NONE SHT 44 OF 154

LAST_MODIFIED=Tue Nov 1 13:46:32 2005

DRAWING



NOTES

JTAG DRIVEN ON SMU PG 30
QREQ PULLDOWNS ON Q63 SHARED PAGE
SRESET DRIVEN ON PG 56
INT DRIVEN BY KODIAK
R4739 REQUIRED TO ACCESS THE RINGS

4.7K RESISTORS FOR MANUFACTURING-TEST-TYPE PULLUPS OR PULLDOWNS.
1K RESISTORS FOR IMPORTANT USE OR STRAPPING OPTIONS.

SELECT PROCESSOR CLOCK MULTIPLIER. PROCESSOR CLOCK(MHZ)= SYSTCLOCK * PLLMULT.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
*	116S0066	1	RES,1K OHM,1/16W,5%,0402	R4734	EI_3TO1	SYSCLK * 12
	116S0066	1	RES,1K OHM,1/16W,5%,0402	R4718	EI_2TO1	SYSCLK * 8

SELECT EI BUS DIVIDER. BUS DATA RATE(BPS)= (PROCESSOR CLOCK) / BUSCFG.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4724,R4726,R4728	EI_2TO1	PROC / 2
*	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4724,R4726,R4712	EI_3TO1	PROC / 3
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4724,R4710,R4728	NOSTUFF	PROC / 4
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4724,R4710,R4712	NOSTUFF	PROC / 6
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4708,R4726,R4728	NOSTUFF	PROC / 8
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4708,R4726,R4712	NOSTUFF	PROC / 12
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4708,R4710,R4728	NOSTUFF	PROC / 16
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4708,R4710,R4712	NOSTUFF	

SELECT ELASTIC MODE OR BYPASS.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
*	116S0066	1	RES,1K OHM,1/16W,5%,0402	R4736		
	116S0066	1	RES,1K OHM,1/16W,5%,0402	R4720	NOSTUFF	BYPASS MODE

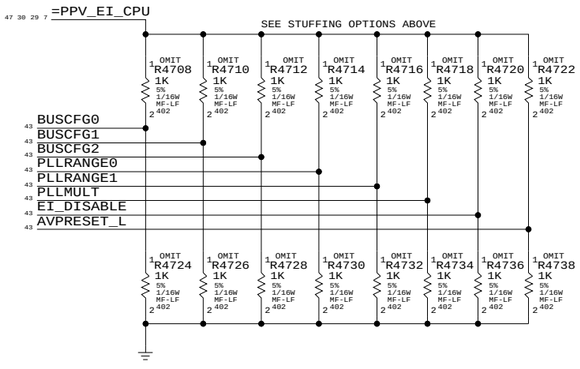
SELECT PLL FREQUENCY RANGE.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
>= 1.8 GHZ *	116S0066	2	RES,1K OHM,1/16W,5%,0402	R4730,R4732	CPU_PLL_LOW	
	116S0066	2	RES,1K OHM,1/16W,5%,0402	R4730,R4716	CPU_PLL_HIGH	
	116S0066	2	RES,1K OHM,1/16W,5%,0402	R4714,R4732	CPU_PLL_MEDIUM	
	116S0066	2	RES,1K OHM,1/16W,5%,0402	R4714,R4716	NOSTUFF	RESERVED

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
116S0066	1	RES,1K OHM,1/16W,5%,0402	R4722		AVPRESET OFF
116S0066	1	RES,1K OHM,1/16W,5%,0402	R4738	NOSTUFF	AVPRESET ON

* STUFF THESE ON M23.

PROCESSOR BUS CONFIGURATION



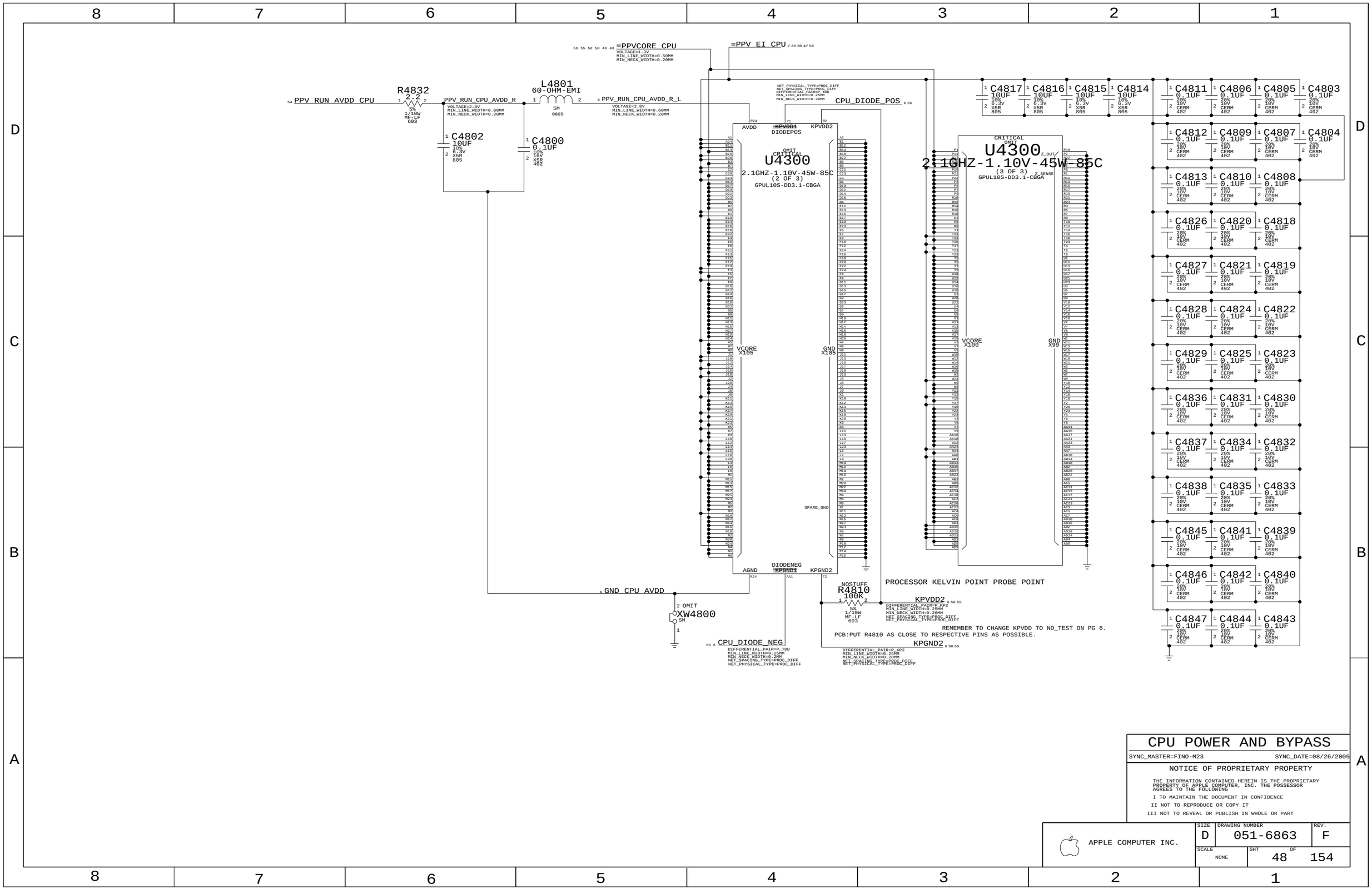
CPU STRAPS

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F

SCALE	SHT	OF
NONE	47	154



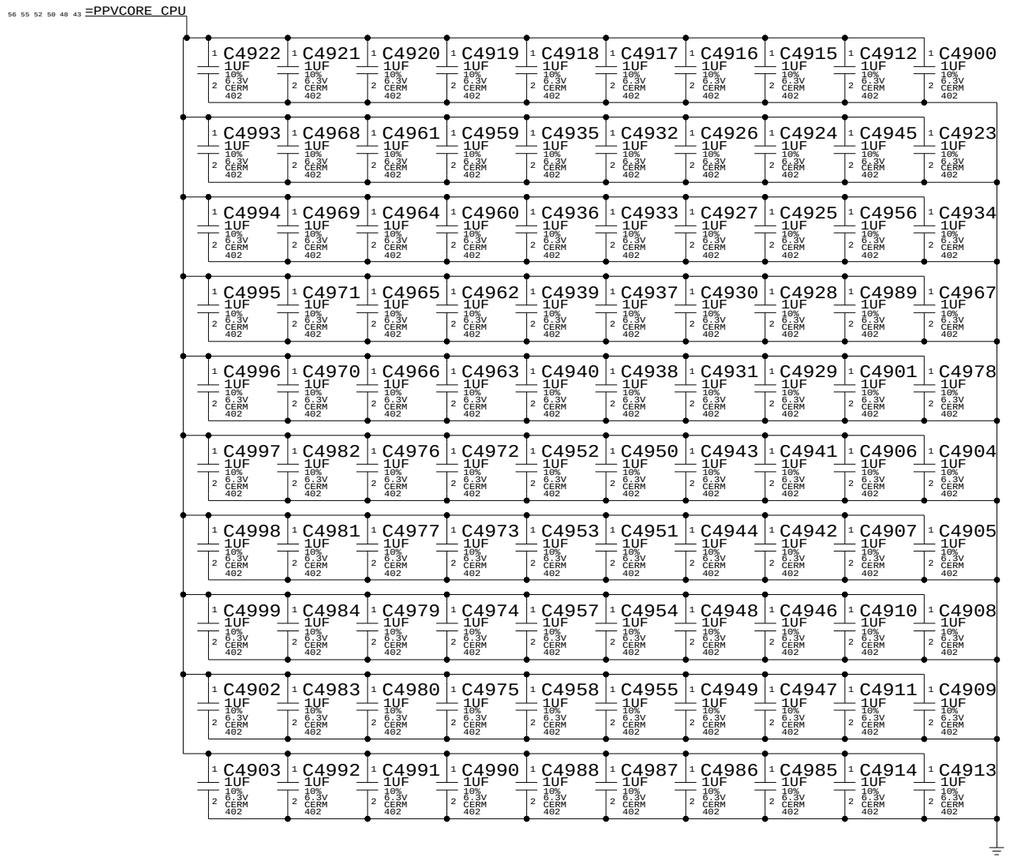
CPU POWER AND BYPASS

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F

SCALE	SHT	OF
NONE	48	154



PROC DECOUPLING

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 49 OF 154	

VCORE VOLTAGE CONTROLLER (VC)

M23/M33: PP12V_CPU IS AN ALL RAIL

=PP12V_CPU
R5029 10 5% 1/16W MF-LF 402
VC_VCC
C5019 1UF 20% 16V CERM 1206
SYS_POWERUP_L
R5000 1.5K 5% 1/16W MF-LF 402
VRM_EN
Q5012 2N7002 SOT23-LF
C5001 1UF 10% 6.3V CERM 402
VC_AGND
VC_BGOUT
VC_OSCREF
CPU_VID_R<0>
CPU_VID_R<1>
CPU_VID_R<2>
CPU_VID_R<3>
CPU_VID_R<4>
CPU_VID_R<5>
U5000 SC2642 TSSOP (CRITICAL)
BGOUT, OSCREF, VID0, VID1, VID2, VID3, VID4, VID5, DACSTEP, FB, GSENSE, OS1, OS2, AGND, VCC, OUTSEN, OUT1, OUT2, PGOOD, EROUT
VC_OUTSEN
VC_OUT1
VC_OUT2
VC_PGOOD
PGOOD IS OC
R5030 0 5% 1/10W MF-LF 402
SYS_SLEWING_L
NOSTUFF R5003 2.7M 5% 1/10W MF-LF 603
VC_EROUT
VC_VCC
R5001 20K 5% 1/16W MF-LF 402
NOSTUFF R5002 0 5% 1/16W MF-LF 402
VC_EROUT_RC
C5002 470PF 10% 50V CERM 402
OMIT XW5000 SM
C5000 0.1UF 20% 10V CERM 402
R5028 221K 1% 1/16W MF-LF 402
VC_OS1
VC_OS2
VC_AUX1
VC_AUX2
R5013 20.5K 1% 1/16W MF-LF 402
R5016 20.5K 1% 1/16W MF-LF 402
C5004 0.01UF 10% 16V CERM 402
NOSTUFF R5014 20.5K 1% 1/16W MF-LF 402
C5005 0.01UF 10% 16V CERM 402
NOSTUFF R5015 20.5K 1% 1/16W MF-LF 402
VCORE_SENSE_GND
DIFFERENTIAL PAIR FOR REMOTE SENSE
VCORE_SENSE_VOUT
R5005 4.99K 1% 1/16W MF-LF 402
VC_OS_HUB
R5004 261 1% 1/16W MF-LF 402
C5008 0.33UF 10% 6.3V CERM-XSR 402
NOSTUFF R5026 301 1% 1/16W MF-LF 402
AVP ADJUSTMENT
NOSTUFF R5024 330 5% 1/16W MF-LF 402
NOSTUFF R5025 1K 5% 1/16W MF-LF 402
VC_OS_HUB_RC
PCB:PLACE R5025 CLOSE TO INDUCTOR OUTPUT LEAD.
NOSTUFF C5009 0.015UF 10% 16V X7R 402
R5027 1.5K 1% 1/16W MF-LF 402
VC_OUTSEN_R
OMIT XW5002 SM
=PPVCORE_CPU
PCB:CONNECT BETWEEN THE INDUCTOR & BULK CAPS.

VC PROCESSOR VOLTAGE SENSING

CHOICE OF:
1) VCORE PLANE SENSING
2) KELVIN POINT SENSING

PPVCORE_CPU
R5035 0 5% 1/10W MF-LF 402
MIN_NECK_WIDTH=0.20MM
MIN_LINE_WIDTH=0.50MM
UNDER PROCESSOR
R5036 0 5% 1/10W MF-LF 402
VCORE_SENSE_VOUT
VCORE_SENSE_GND
NOSTUFF R5041 0 5% 1/10W MF-LF 402
KPVDD2
CPU SENSE SIDE
NOSTUFF R5042 0 5% 1/10W MF-LF 402
KPGND2

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
GD1_DRN	0.25 MM	0.25 MM
GD1_BST	0.25 MM	0.25 MM
GD1_VREG	0.25 MM	0.25 MM
GD1_VPN	0.25 MM	0.25 MM
GD1_TG	0.25 MM	0.25 MM
GD1_BG	0.25 MM	0.25 MM
GD1_FET_RC	0.25 MM	0.25 MM
GD1_PN	0.60 MM	0.25 MM
GD1_BST_R	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
GD2_DRN	0.25 MM	0.25 MM
GD2_BST	0.25 MM	0.25 MM
GD2_VREG	0.25 MM	0.25 MM
GD2_VPN	0.25 MM	0.25 MM
GD2_TG	0.25 MM	0.25 MM
GD2_BG	0.25 MM	0.25 MM
GD2_FET_RC	0.25 MM	0.25 MM
GD2_PN	0.60 MM	0.25 MM
GD2_BST_R	0.25 MM	0.25 MM

VCORE SUPPLY PHASE 1 (GD1)

PP12V_CPU_R_L
C5010 1UF 20% 16V CERM 1206
GD1_BST_R
GD1_DRN
U5010 SC1211 VIN SOIC-LF (CRITICAL)
BG, VREG, TG, VPN, CO, DRN, BST, THMPAD
VC_OUT1
C5029 1UF 20% 16V CERM 1206
R5007 4.7 5% 1/10W MF-LF 603
GD1_BST
D5010 BAS16-75V-0.25A SOT23-LF
GD1_VREG
C5013 1UF 20% 16V CERM 1206
GD1_TG
Q5010 IRLR7821PBF TO-252AA (CRITICAL)
R5050 10K 5% 1/16W MF-LF 402
R5010 1 2% 1/10W MF-LF 402
C5011 330UF 20% 16V ELEC SM-LF
C5035 330UF 20% 16V ELEC SM-LF
C5012 10UF 10% 16V CERM 1210
L5010 0.36UH-30A-0.80MOHM SM (CRITICAL)
=PPVCORE_CPU
PPVCORE_CPU
C5018 330UF 20% 2.5V-ESR9V POLY CASE-D2E-LF (CRITICAL)
C5017 330UF 20% 2.5V-ESR9V POLY CASE-D2E-LF
C5032 1500UF 20% 0.3V ELEC TH-MCZ
C5038 330UF 20% 2.5V-ESR9V POLY CASE-D2E-LF
GD1_PN
R5011 1.0 5% 1/4W MF-LF 1206
GD1_FET_RC
R5012 200 5% 1/16W MF-LF 402
VC_AUX1
C5014 470PF 10% 50V CERM 402
GD1_BG1
Q5011 IRLR7843PBF TO-252AA (CRITICAL)
Q5013 IRLR7843PBF TO-252AA (CRITICAL)
C5015 0.0022UF 10% 50V CERM 402
C5016 3300PF 10% 50V CERM 603
NEED TO CHANGE TO 10MOHM CAPS - 8 PCS

VCORE SUPPLY PHASE 2 (GD2)

PP12V_CPU_R_L
C5020 1UF 20% 16V CERM 1206
GD2_BST_R
GD2_DRN
U5020 SC1211 VIN SOIC-LF (CRITICAL)
BG, VREG, TG, VPN, CO, DRN, BST, THMPAD
VC_OUT2
C5030 1UF 20% 16V CERM 1206
R5006 4.7 5% 1/10W MF-LF 603
GD2_BST
D5020 BAS16-75V-0.25A SOT23-LF
GD2_VREG
C5023 1UF 20% 16V CERM 1206
GD2_TG
Q5020 IRLR7821PBF TO-252AA (CRITICAL)
R5051 10K 5% 1/16W MF-LF 402
R5020 1 2% 1/10W MF-LF 402
C5021 1000UF 20% 16V ELEC TH-KZJ-LF
C5022 10UF 10% 16V CERM 1210
L5020 0.36UH-30A-0.80MOHM SM (CRITICAL)
PPVCORE_CPU
C5028 1800UF 20% 0.3V ELEC TH-KZJ-LF (CRITICAL)
C5033 1800UF 20% 0.3V ELEC TH-KZJ-LF
C5040 1500UF 20% 0.3V ELEC TH-MCZ
GD2_PN
R5021 1.0 5% 1/4W MF-LF 1206
GD2_FET_RC
R5022 200 5% 1/16W MF-LF 402
VC_AUX2
C5024 470PF 10% 50V CERM 402
GD2_BG1
Q5021 IRLR7843PBF TO-252AA (CRITICAL)
Q5023 IRLR7843PBF TO-252AA (CRITICAL)
C5025 0.0022UF 10% 50V CERM 402
C5026 3300PF 10% 50V CERM 603
C5041 330UF 20% 2.5V-ESR9V POLY CASE-D2E-LF (CRITICAL)
C5042 330UF 20% 2.5V-ESR9V POLY CASE-D2E-LF
NEED TO CHANGE TO 10MOHM CAPS - 8 PCS

PHYSICAL CONSTRAINTS

	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
VC_OSCREF	0.25 MM	0.20 MM	4376
CPU_VID_R<0..5>	0.25 MM	0.20 MM	4377
VC_DACSTEP	0.25 MM	0.20 MM	4378
VC_AGND	0.50 MM	0.20 MM	4379
VC_BGOUT	0.25 MM	0.20 MM	4380
VC_OS1	0.25 MM	0.20 MM	4381
VC_OS2	0.25 MM	0.20 MM	4382
VC_VCC	0.25 MM	0.25 MM	4383
VC_OS_HUB	0.25 MM	0.20 MM	4384
VC_OUTSEN	0.25 MM	0.20 MM	4385
VC_OUTSEN_R	0.25 MM	0.20 MM	4386
VCORE_SENSE_GND	0.25 MM	0.20 MM	4387
VCORE_SENSE_VOUT	0.25 MM	0.20 MM	4388
VC_AUX1	0.25 MM	0.25 MM	4389
VC_AUX2	0.25 MM	0.25 MM	4390
VC_OUT1	0.45 MM	0.25 MM	4391
VC_OUT2	0.45 MM	0.25 MM	4392
VC_EROUT	0.25 MM	0.20 MM	4393
VC_EROUT_RC	0.25 MM	0.20 MM	4394
VC_OS_HUB_RC	0.25 MM	0.20 MM	4395

CPU VCORE VREG

SYNC_MASTER=M33-HS SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6863 | REV. F

SCALE NONE | SHT 50 OF 154

56 55 50 49 48 43 =PPVCORE_CPU

CRITICAL

C5200 10UF 10% 6.3V X5R 805	C5212 10UF 10% 6.3V X5R 805	C5223 10UF 10% 6.3V X5R 805	C5234 10UF 10% 6.3V X5R 805	C5245 10UF 10% 6.3V X5R 805	C5201 10UF 10% 6.3V X5R 805	C5289 10UF 10% 6.3V X5R 805	C5278 10UF 10% 6.3V X5R 805	C5267 10UF 10% 6.3V X5R 805	C5256 10UF 10% 6.3V X5R 805
C5213 10UF 10% 6.3V X5R 805	C5211 10UF 10% 6.3V X5R 805	C5210 10UF 10% 6.3V X5R 805	C5209 10UF 10% 6.3V X5R 805	C5208 10UF 10% 6.3V X5R 805	C5207 10UF 10% 6.3V X5R 805	C5206 10UF 10% 6.3V X5R 805	C5205 10UF 10% 6.3V X5R 805	C5204 10UF 10% 6.3V X5R 805	C5203 10UF 10% 6.3V X5R 805
C5224 10UF 10% 6.3V X5R 805	C5222 10UF 10% 6.3V X5R 805	C5221 10UF 10% 6.3V X5R 805	C5220 10UF 10% 6.3V X5R 805	C5219 10UF 10% 6.3V X5R 805	C5218 10UF 10% 6.3V X5R 805	C5217 10UF 10% 6.3V X5R 805	C5216 10UF 10% 6.3V X5R 805	C5215 10UF 10% 6.3V X5R 805	C5214 10UF 10% 6.3V X5R 805
C5235 10UF 10% 6.3V X5R 805	C5233 10UF 10% 6.3V X5R 805	C5232 10UF 10% 6.3V X5R 805	C5231 10UF 10% 6.3V X5R 805	C5230 10UF 10% 6.3V X5R 805	C5229 10UF 10% 6.3V X5R 805	C5228 10UF 10% 6.3V X5R 805	C5227 10UF 10% 6.3V X5R 805	C5226 10UF 10% 6.3V X5R 805	C5225 10UF 10% 6.3V X5R 805
C5246 10UF 10% 6.3V X5R 805	C5244 10UF 10% 6.3V X5R 805	C5243 10UF 10% 6.3V X5R 805	C5242 10UF 10% 6.3V X5R 805	C5241 10UF 10% 6.3V X5R 805	C5240 10UF 10% 6.3V X5R 805	C5239 10UF 10% 6.3V X5R 805	C5238 10UF 10% 6.3V X5R 805	C5237 10UF 10% 6.3V X5R 805	C5236 10UF 10% 6.3V X5R 805
C5257 10UF 10% 6.3V X5R 805	C5255 10UF 10% 6.3V X5R 805	C5254 10UF 10% 6.3V X5R 805	C5253 10UF 10% 6.3V X5R 805	C5252 10UF 10% 6.3V X5R 805	C5251 10UF 10% 6.3V X5R 805	C5250 10UF 10% 6.3V X5R 805	C5249 10UF 10% 6.3V X5R 805	C5248 10UF 10% 6.3V X5R 805	C5247 10UF 10% 6.3V X5R 805
C5268 10UF 10% 6.3V X5R 805	C5266 10UF 10% 6.3V X5R 805	C5265 10UF 10% 6.3V X5R 805	C5264 10UF 10% 6.3V X5R 805	C5263 10UF 10% 6.3V X5R 805	C5262 10UF 10% 6.3V X5R 805	C5261 10UF 10% 6.3V X5R 805	C5260 10UF 10% 6.3V X5R 805	C5259 10UF 10% 6.3V X5R 805	C5258 10UF 10% 6.3V X5R 805
C5279 10UF 10% 6.3V X5R 805	C5277 10UF 10% 6.3V X5R 805	C5276 10UF 10% 6.3V X5R 805	C5275 10UF 10% 6.3V X5R 805	C5274 10UF 10% 6.3V X5R 805	C5273 10UF 10% 6.3V X5R 805	C5272 10UF 10% 6.3V X5R 805	C5271 10UF 10% 6.3V X5R 805	C5270 10UF 10% 6.3V X5R 805	C5269 10UF 10% 6.3V X5R 805
C5290 10UF 10% 6.3V X5R 805	C5288 10UF 10% 6.3V X5R 805	C5287 10UF 10% 6.3V X5R 805	C5286 10UF 10% 6.3V X5R 805	C5285 10UF 10% 6.3V X5R 805	C5284 10UF 10% 6.3V X5R 805	C5283 10UF 10% 6.3V X5R 805	C5282 10UF 10% 6.3V X5R 805	C5281 10UF 10% 6.3V X5R 805	C5280 10UF 10% 6.3V X5R 805
C5202 10UF 10% 6.3V X5R 805	C5299 10UF 10% 6.3V X5R 805	C5298 10UF 10% 6.3V X5R 805	C5297 10UF 10% 6.3V X5R 805	C5296 10UF 10% 6.3V X5R 805	C5295 10UF 10% 6.3V X5R 805	C5294 10UF 10% 6.3V X5R 805	C5293 10UF 10% 6.3V X5R 805	C5292 10UF 10% 6.3V X5R 805	C5291 10UF 10% 6.3V X5R 805

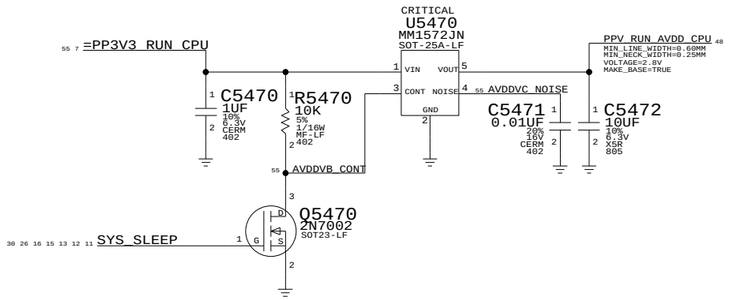
CPU VCORE MORE BYPASS

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE NONE	SHT 52 OF 154	

PROCESSOR AVDD VREG



ZH5400 HOLE-VIA
ZH5401 HOLE-VIA
ZH5402 HOLE-VIA
ZH5403 HOLE-VIA
ZH5404 HOLE-VIA
ZH5405 HOLE-VIA
ZH5406 HOLE-VIA
ZH5407 HOLE-VIA
ZH5408 HOLE-VIA
ZH5409 HOLE-VIA
ZH5410 HOLE-VIA
ZH5411 HOLE-VIA
ZH5412 HOLE-VIA
ZH5413 HOLE-VIA
ZH5414 HOLE-VIA
ZH5415 HOLE-VIA
ZH5416 HOLE-VIA
ZH5417 HOLE-VIA
ZH5418 HOLE-VIA
ZH5419 HOLE-VIA
ZH5420 HOLE-VIA
ZH5421 HOLE-VIA
ZH5422 HOLE-VIA
ZH5423 HOLE-VIA
ZH5424 HOLE-VIA
ZH5425 HOLE-VIA
ZH5426 HOLE-VIA
ZH5427 HOLE-VIA
ZH5428 HOLE-VIA
ZH5429 HOLE-VIA
ZH5430 HOLE-VIA
ZH5431 HOLE-VIA
ZH5432 HOLE-VIA
ZH5433 HOLE-VIA
ZH5434 HOLE-VIA
ZH5435 HOLE-VIA
ZH5436 HOLE-VIA
ZH5437 HOLE-VIA
ZH5438 HOLE-VIA
ZH5439 HOLE-VIA
ZH5440 HOLE-VIA
ZH5441 HOLE-VIA
ZH5442 HOLE-VIA
ZH5443 HOLE-VIA
ZH5444 HOLE-VIA
ZH5445 HOLE-VIA
ZH5446 HOLE-VIA
ZH5447 HOLE-VIA
ZH5448 HOLE-VIA
ZH5449 HOLE-VIA
ZH5450 HOLE-VIA
ZH5451 HOLE-VIA
ZH5452 HOLE-VIA
ZH5453 HOLE-VIA
ZH5454 HOLE-VIA
ZH5455 HOLE-VIA
ZH5456 HOLE-VIA
ZH5457 HOLE-VIA
ZH5458 HOLE-VIA
ZH5459 HOLE-VIA
ZH5460 HOLE-VIA
ZH5461 HOLE-VIA
ZH5462 HOLE-VIA
ZH5463 HOLE-VIA
ZH5464 HOLE-VIA
ZH5465 HOLE-VIA
ZH5466 HOLE-VIA
ZH5467 HOLE-VIA
ZH5468 HOLE-VIA
ZH5469 HOLE-VIA
ZH5470 HOLE-VIA
ZH5471 HOLE-VIA

CPU AVDD VREG

SYNC_MASTER=FINO-M23 SYNC_DATE=10/07/2005

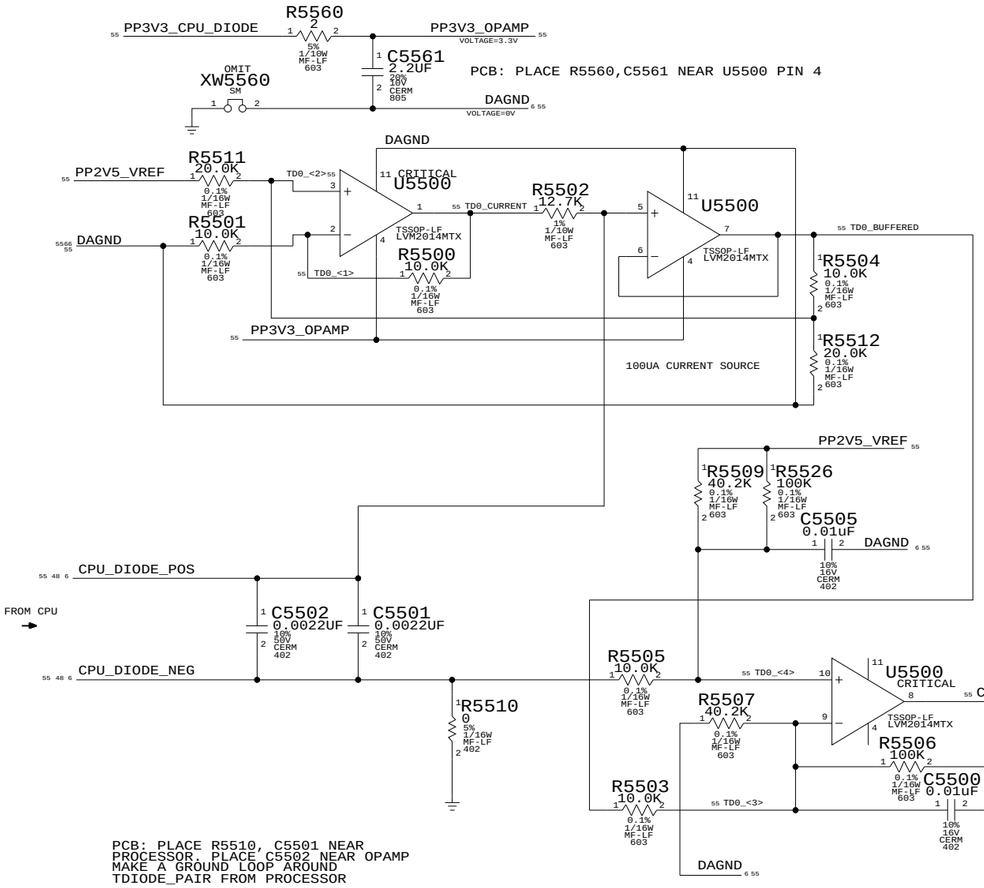
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F

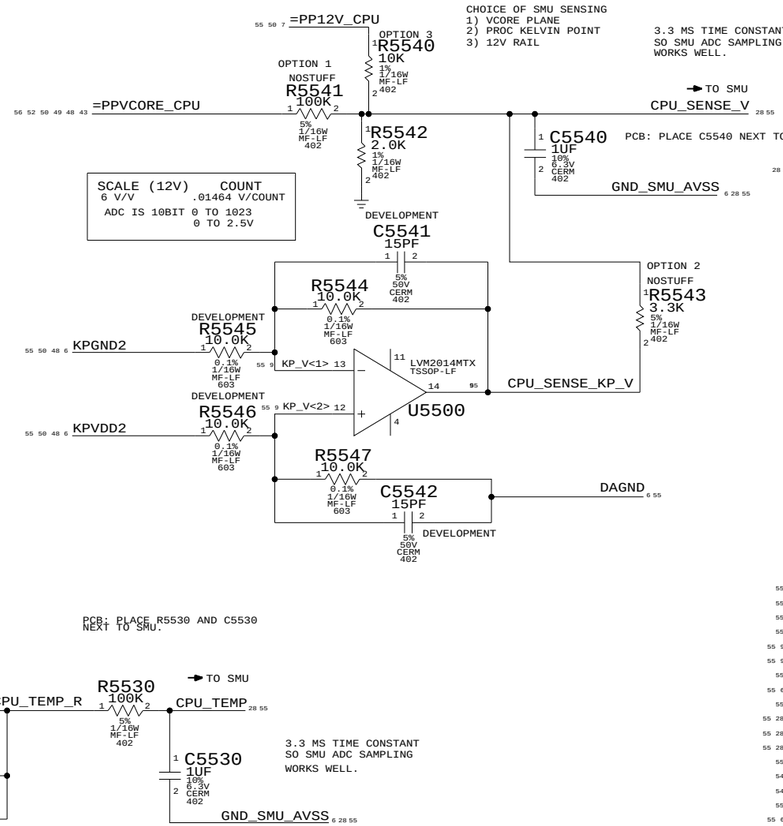
SCALE: NONE

SHT 54 OF 154

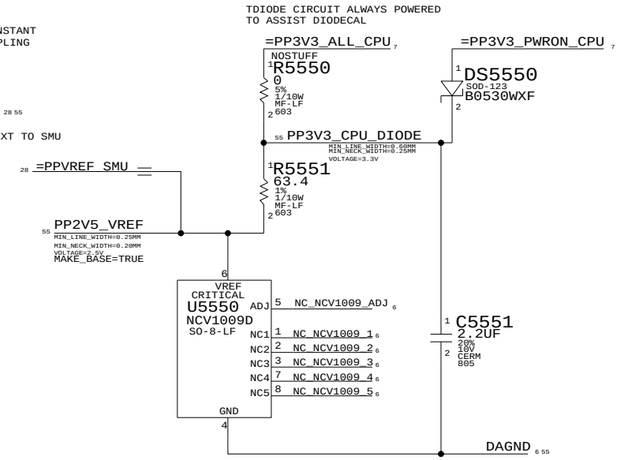
PROCESSOR TEMP SENSE (TDIODE EXCITATION CIRCUIT AND OPAMP)



PROCESSOR VCORE VOLTAGE SENSE



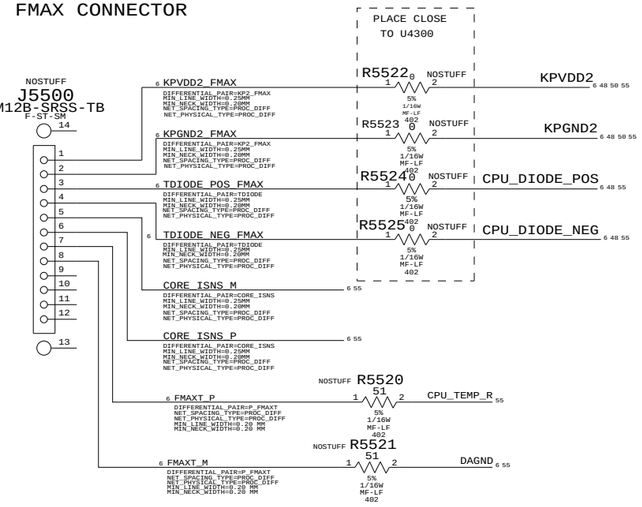
2.5V PRECISION VOLTAGE REFERENCE SOURCE



PHYSICAL CONSTRAINTS

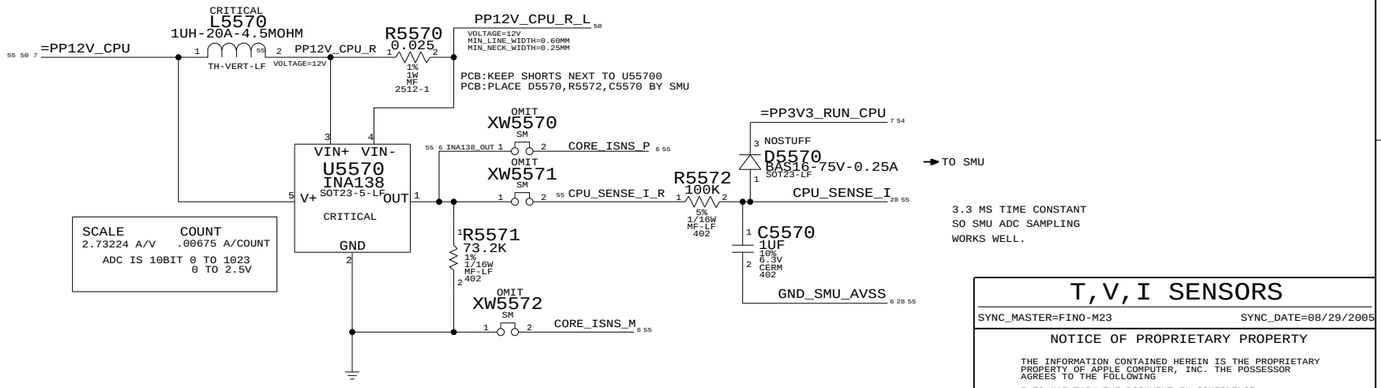
	MIN_LINE_WIDTH	MIN_NECK_WIDTH
TD0_<1..4>	0.25 MM	0.25 MM
PP12V_CPU_R	0.60 MM	0.25 MM
TD0_CURRENT	0.25 MM	0.25 MM
TD0_BUFFERED	0.25 MM	0.25 MM
KP_V<1..2>	0.25 MM	0.25 MM
CPU_SENSE_KP_V	0.25 MM	0.25 MM
PP3V3_OPAMP	0.60 MM	0.25 MM
INA138_OUT	0.25 MM	0.25 MM
CPU_SENSE_I_R	0.25 MM	0.25 MM
CPU_SENSE_I	0.25 MM	0.25 MM
CPU_SENSE_V	0.25 MM	0.25 MM
CPU_TEMP	0.25 MM	0.20 MM
CPU_TEMP_R	0.25 MM	0.20 MM
AVDDVC_NOISE	0.25 MM	0.20 MM
AVDDVB_CONT	0.25 MM	0.20 MM
PP12V_CPU_R	0.60 MM	0.25 MM
DAGND	0.60 MM	0.25 MM

FMAX CONNECTOR



PROCESSOR VCORE CURRENT SENSE

(USING 12V INPUT CURRENT TO DERIVE CPU CURRENT)



T,V,I SENSORS

SYNC_MASTER=FINO-M23 SYNC_DATE=08/29/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 55 OF 154	

CONNECT PULSAR CLKS TO CPU/NB

56 43 9	EI_CPU_SYSCLK_P	EI_CPU_A_SYSCLK_P	26
56 43	EI_CPU_SYSCLK_N	EI_CPU_A_SYSCLK_N	26
56 43	EI_CPU_APSYNC	CPU_A_APSYNC	26
43	EI_CPU_TBEN_CLK	CPU_A_TBEN_CLK_US	26
56	EI_NB_APSYNC	NB_APSYNC	26 42

MAKE_BASE=TRUE

CONNECT KODIAK EI A TO/FROM CPU

56 43 9	EI_NB_TO_CPU_CLK_P	EI_NB_TO_CPU_A_CLK_P	42
56 43 9	EI_NB_TO_CPU_CLK_N	EI_NB_TO_CPU_A_CLK_N	42
56 43	EI_NB_TO_CPU_AD<0..43>	EI_NB_TO_CPU_A_AD<0..43>	42
56 43 9	EI_NB_TO_CPU_SR_P<0..1>	EI_NB_TO_CPU_A_SR_P<0..1>	42
56 43 9	EI_NB_TO_CPU_SR_N<0..1>	EI_NB_TO_CPU_A_SR_N<0..1>	42
56 43 9	EI_CPU_TO_NB_CLK_P	EI_CPU_A_TO_NB_CLK_P	42
56 43 9	EI_CPU_TO_NB_CLK_N	EI_CPU_A_TO_NB_CLK_N	42
56 43	EI_CPU_TO_NB_AD<0..43>	EI_CPU_A_TO_NB_AD<0..43>	42
56 43 9	EI_CPU_TO_NB_SR_P<0..1>	EI_CPU_A_TO_NB_SR_P<0..1>	42
56 43 9	EI_CPU_TO_NB_SR_N<0..1>	EI_CPU_A_TO_NB_SR_N<0..1>	42

MAKE_BASE=TRUE

CONNECT CPU TO KODIAK QREQ A0

43	CPU_TO_NB_QREQ_L	CPU_A0_TO_NB_QREQ_L	42

MAKE_BASE=TRUE

CONNECT CPU TO KODIAK QACK A0, NC OTHERWISE

43	CPU_QACK_L	CPU_A0_QACK_L	42
9	NC_CPU_A1_QACK_L	CPU_A1_QACK_L	42
9	NC_CPU_B0_QACK_L	CPU_B0_QACK_L	44
6	NC_CPU_B1_QACK_L	CPU_B1_QACK_L	44

MAKE_BASE=TRUE

CONNECT CPU TO KODIAK/SHASTA INT A0, NC OTHERWISE

43	CPU_INT_L	CPU_A0_INT_R_L	24 56
9	NC_NB_CPU_A1_INT_L	NB_CPU_A1_INT_L	42
9	NC_NB_CPU_B0_INT_L	NB_CPU_B0_INT_L	44
6	NC_NB_CPU_B1_INT_L	NB_CPU_B1_INT_L	44

MAKE_BASE=TRUE

CONNECT CPU TO SHASTA SRESET A0, NC OTHERWISE

	CPU_SRESET_L_R	SB_CPU_A0_SRESET_L	24 56
	NOTUSED_CPU_A1_SRESET_L	SB_CPU_A1_SRESET_L	24 56
	NOTUSED_CPU_B0_SRESET_L	SB_CPU_B0_SRESET_L	24 56
	NOTUSED_CPU_B1_SRESET_L	SB_CPU_B1_SRESET_L	24 56

MAKE_BASE=TRUE

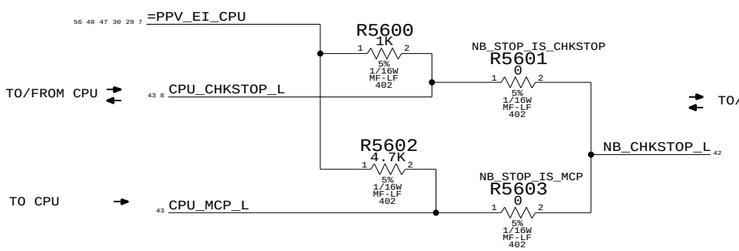
WIRE OUT KODIAK AND CPU SIGNALS FOR TP'S

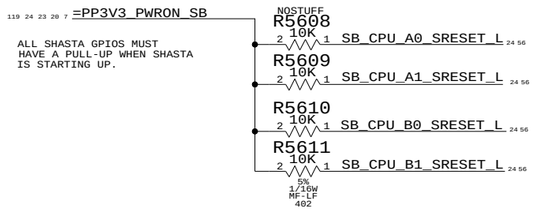
9	TP_NB_B_TRIGGER_OUT	NB_B_TRIGGER_OUT	44
9	TP_NB_A_TRIGGER_OUT	NB_A_TRIGGER_OUT	42
9	TP_CPU_APSYNCOUT	CPU_APSYNCOUT	43
9	TP_CPU_TRIGGER_IN	CPU_TRIGGER_IN	43 47
9	TP_CPU_TRIGGER_OUT	CPU_TRIGGER_OUT	43
9	NC_PSRO	CPU_PSRO	43
9	NC_PSRO_ENABLE	CPU_PSRO_ENABLE	43
9	TP_CPU_ATTENTION	CPU_ATTENTION	43
9	NC_CPU_AFN	CPU_AFN	43

MAKE_BASE=TRUE

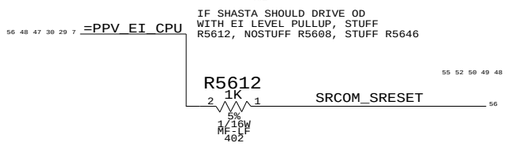
REMEMBER TO UPDATE NO_TEST PROPERTIES ON PG 6

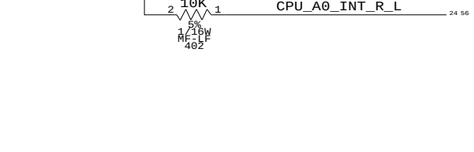
CPU CHKSTOP OR MCP TO NB





ALL SHASTA GPIOS MUST HAVE A PULL-UP WHEN SHASTA IS STARTING UP.





EI BUS AND SYSCLK CONSTRAINT LABELS

	ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR	
56 43 9 EI_CPU_TO_NB_CLK_P	EICNCLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	128
56 43 9 EI_CPU_TO_NB_CLK_N	EICNCLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	127
56 43 EI_CPU_TO_NB_AD<0..21>	EICNCAD	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD		131
56 43 9 EI_CPU_TO_NB_SR_P<0..1>	EICNCSR	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD		134
56 43 9 EI_CPU_TO_NB_SR_N<0..1>	EICNCSR	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD		132
56 43 9 EI_NB_TO_CPU_CLK_P	EINCCLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	129
56 43 9 EI_NB_TO_CPU_CLK_N	EINCCLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	130
56 43 EI_NB_TO_CPU_AD<0..43>	EINCCAD	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD		135
56 43 9 EI_NB_TO_CPU_SR_P<0..1>	EINCCAD	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD		140
56 43 9 EI_NB_TO_CPU_SR_N<0..1>	EINCCAD	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD		137
56 EI_NB_APSYNC	EIPNAPSYNC	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD		138
56 43 EI_CPU_APSYNC	EIPCAPSYNC	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD		139
56 43 9 EI_CPU_SYSCLK_P	EIPCSYSCLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_CPU_SYSCLK	140
56 43 EI_CPU_SYSCLK_N	EIPCSYSCLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_CPU_SYSCLK	141
42 26 EI_NB_SYSCLK_P	EIPNSYSCLK_P	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_NB_SYSCLK	136
42 26 EI_NB_SYSCLK_N	EIPNSYSCLK_N	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_NB_SYSCLK	142
56 43 EI_CPU_TO_NB_AD<22>	EICNCAD_PP	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD		1496
56 43 EI_CPU_TO_NB_AD<23..43>	EICNCAD	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD		1496

NC KODIAK EI B OUTPUT PORT

6	NC_EI_NB_TO_CPU_B_CLK_P	EI_NB_TO_CPU_B_CLK_P	44
6	NC_EI_NB_TO_CPU_B_CLK_N	EI_NB_TO_CPU_B_CLK_N	44
6	NC_EI_NB_TO_CPU_B_AD<0..43>	EI_NB_TO_CPU_B_AD<0..43>	44
6	NC_EI_NB_TO_CPU_B_SR_P<0..1>	EI_NB_TO_CPU_B_SR_P<0..1>	44
6	NC_EI_NB_TO_CPU_B_SR_N<0..1>	EI_NB_TO_CPU_B_SR_N<0..1>	44

MAKE_BASE=TRUE

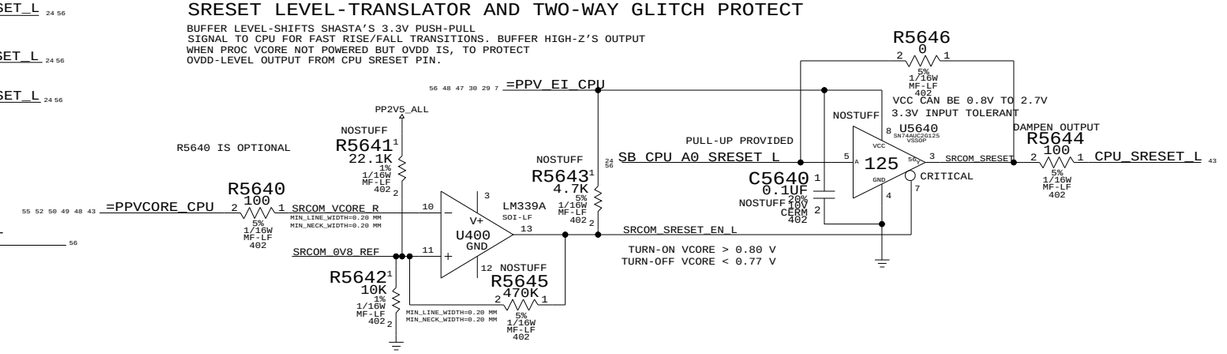
NC KODIAK EI B INPUT PORT

6	NC_EI_CPU_B_TO_NB_CLK_P	EI_CPU_B_TO_NB_CLK_P	44
6	NC_EI_CPU_B_TO_NB_CLK_N	EI_CPU_B_TO_NB_CLK_N	44
6	NC_EI_CPU_B_TO_NB_AD<0..43>	EI_CPU_B_TO_NB_AD<0..43>	44
6	NC_EI_CPU_B_TO_NB_SR_P<0..1>	EI_CPU_B_TO_NB_SR_P<0..1>	44
6	NC_EI_CPU_B_TO_NB_SR_N<0..1>	EI_CPU_B_TO_NB_SR_N<0..1>	44

MAKE_BASE=TRUE

SRESET LEVEL-TRANSLATOR AND TWO-WAY GLITCH PROTECT

BUFFER LEVEL-SHIFTS SHASTA'S 3.3V PUSH-PULL SIGNAL TO CPU FOR FAST RISE/FALL TRANSITIONS. BUFFER HIGH-Z'S OUTPUT WHEN PROC VCORE NOT POWERED BUT OVDD IS, TO PROTECT OVDD-LEVEL OUTPUT FROM CPU SRESET PIN.

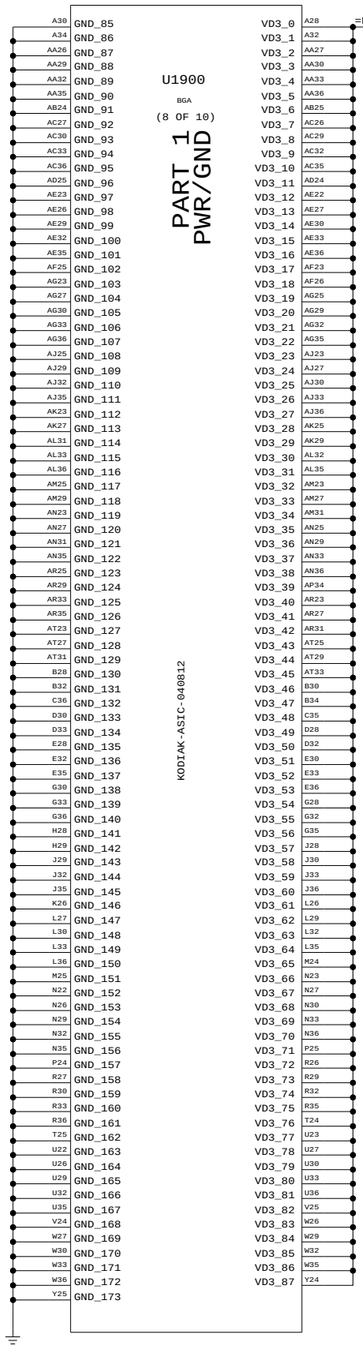


CPU ALIASES & MISC

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT: 56 OF 154	



59 58 39 20 7 =PP1V8_PWRON_NBMEM

C5836 C5835 C5834 C5832 C5831 C5830 C5829 C5822 C5811 C5800
C5864 C5859 C5857 C5842 C5840 C5837 C5828 C5801 C5855 C5833
C5863 C5860 C5858 C5843 C5841 C5838 C5827 C5802 C5866 C5844
C5865 C5862 C5861 C5846 C5845 C5839 C5826 C5803 C5887 C5877
C5874 C5869 C5867 C5852 C5850 C5847 C5825 C5810 C5806 C5804
C5873 C5870 C5868 C5853 C5851 C5848 C5824 C5812 C5807 C5805
C5875 C5872 C5871 C5856 C5854 C5849 C5823 C5813 C5809 C5808
C5886 C5885 C5883 C5881 C5879 C5876 C5821 C5818 C5816 C5814
C5884 C5882 C5880 C5878 C5820 C5819 C5817 C5815

1UF 10% 6.3V CERM 402

Q63: SEE P.20 FOR MORE DECOUPLING CAPS FOR THESE PINS.

KODIAC NBMEM PWR & CAPS

SYNC_MASTER=Q63 SYNC_DATE=08/26/2005

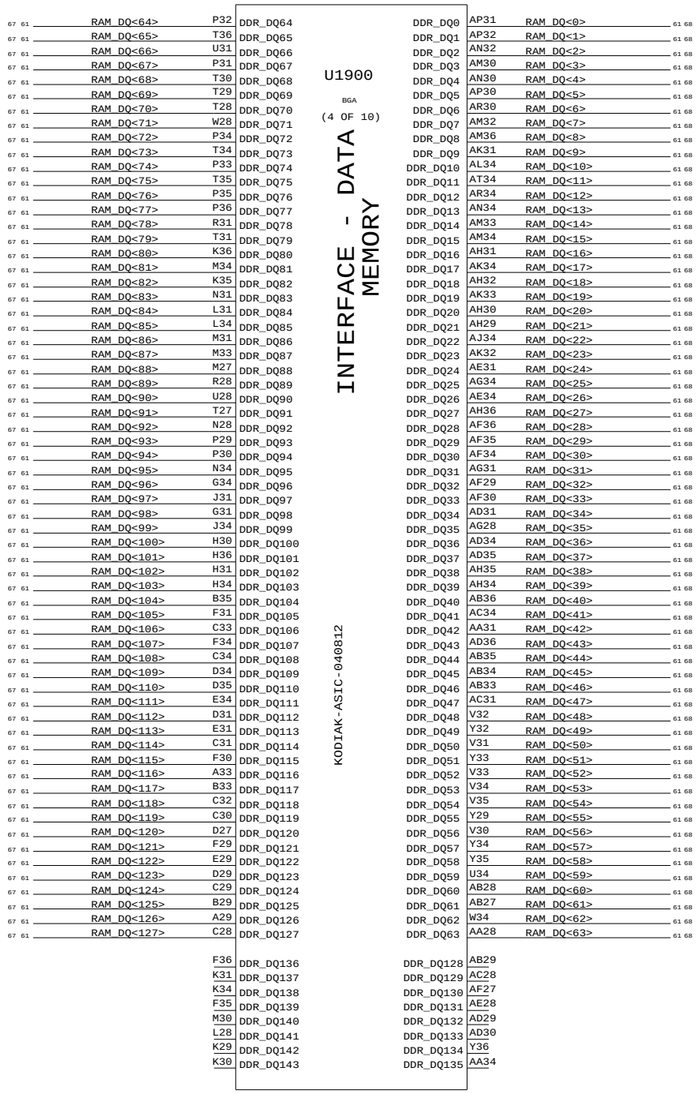
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F

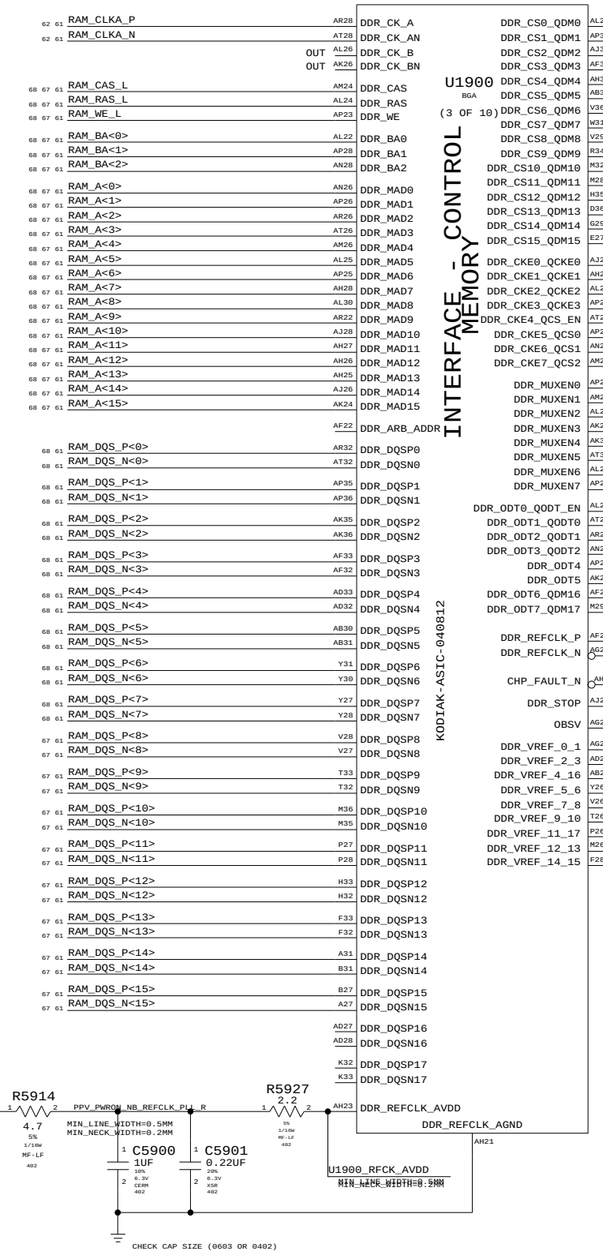
SCALE	SHT	OF
NONE	58	154

LAST_MODIFIED=Tue Nov 1 13:46:44 2005

DRAWING



DQ/DQS OKAY TO TIE TO GROUND FOR THERMALS



Kodiak 128bit CS/CKE/ODT mapping (Q63 style)

DIMM RANK	CS*	CKE	ODT	M23 Function	D bits
A0	0	0	0	onboard DRAM	0:63
A1	1	1	-	*unused*	0:63
B2	2	0	4	J6700 rank 1	64:127
B3	3	1	-	J6700 rank 2	64:127
C4	2	2	1	*unused*	0:63
C5	3	3	-	*unused*	0:63
D6	10	2	5	*unused*	64:127
D7	11	3	-	*unused*	64:127
E8	4	4	2	*unused*	0:63
E9	5	5	-	*unused*	0:63
F10	12	4	6	*unused*	64:127
F11	13	5	-	*unused*	64:127
G12	6	6	3	*unused*	0:63
G13	7	7	-	*unused*	0:63
H14	14	6	7	*unused*	64:127
H15	15	7	-	*unused*	64:127

Kodiak 128bit CS/CKE/ODT mapping (v1.1 only)

DIMM RANK	CS*	CKE	ODT	M23 Function	D bits
A0	0	0	0	onboard DRAM	0:63
A1	1	1	-	*unused*	0:63
B2	4	4	2	J6700 rank 1	64:127
B3	5	5	-	J6700 rank 2	64:127
C4	2	2	1	*unused*	0:63
C5	3	3	-	*unused*	0:63
D6	6	6	3	*unused*	64:127
D7	7	7	-	*unused*	64:127

Kodiak Memory Dq/Ctl

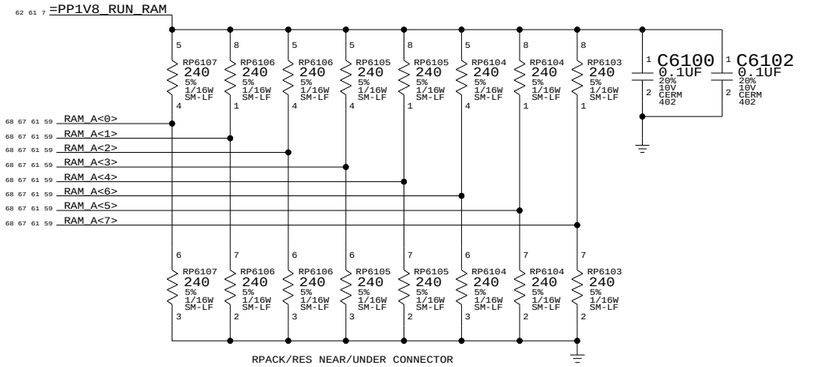
SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

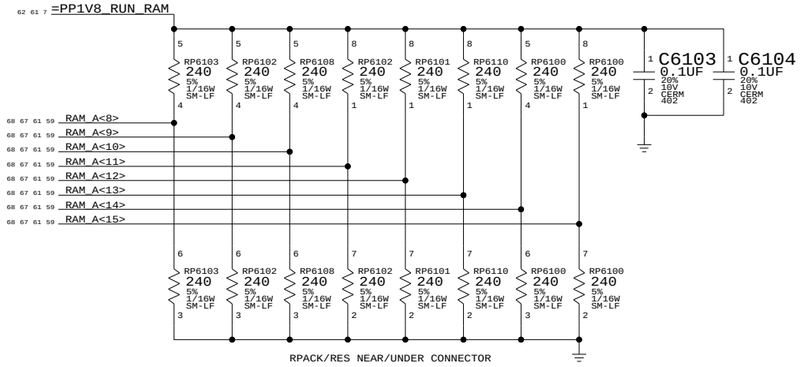
APPLE COMPUTER INC.

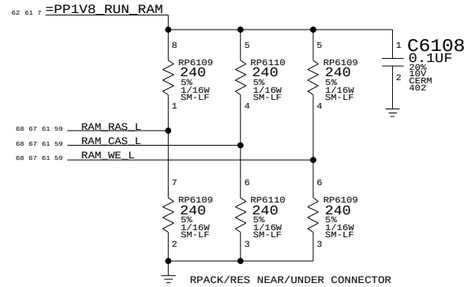
SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 59 OF 154	

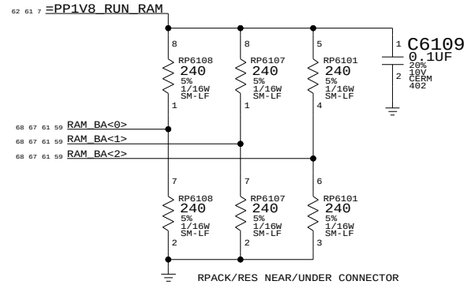
KODIAK MEMORY INTERFACE

ALL R PACKS ARE 1/16W 5%









RAM_CS_L<0>	RAM_CS_ONBOARD_EC	RAM_CSCKEODT	RAM_CSCKEODT	245
RAM_CS_L<4>	RAM_CS_DIMM_EC	RAM_CSCKEODT	RAM_CSCKEODT	487
RAM_CS_L<5>	RAM_CS_DIMM_EC	RAM_CSCKEODT	RAM_CSCKEODT	242
RAM_CS_L<8>		RAM_CSCKEODT	RAM_CSCKEODT	246
RAM_CS_L<9>		RAM_CSCKEODT	RAM_CSCKEODT	244
RAM_CS_L_R<0>		RAM_CSCKEODT	RAM_CSCKEODT	238
RAM_CS_DIMM_A		RAM_CSCKEODT	RAM_CSCKEODT	241
RAM_CS_DIMM_B		RAM_CSCKEODT	RAM_CSCKEODT	675
RAM_CKE<0>	RAM_CKE_DIMM_ONBOARD_EC	RAM_CSCKEODT	RAM_CSCKEODT	234
RAM_CKE<1>	RAM_CKE_DIMM_EC	RAM_CSCKEODT	RAM_CSCKEODT	236
RAM_CKE<4>		RAM_CSCKEODT	RAM_CSCKEODT	235
RAM_CKE<5>		RAM_CSCKEODT	RAM_CSCKEODT	237
RAM_CKE_R<0>		RAM_CSCKEODT	RAM_CSCKEODT	239
RAM_CKE_DIMM_B		RAM_CSCKEODT	RAM_CSCKEODT	1592
RAM_CKE_DIMM_A		RAM_CSCKEODT	RAM_CSCKEODT	232
RAM_ODT<0>	RAM_ODT_ONBOARD_EC	RAM_CSCKEODT	RAM_CSCKEODT	1674
RAM_ODT<2>	RAM_ODT_DIMM_EC	RAM_CSCKEODT	RAM_CSCKEODT	1676
RAM_ODT<4>		RAM_CSCKEODT	RAM_CSCKEODT	1677
RAM_ODT_R<0>		RAM_CSCKEODT	RAM_CSCKEODT	1593
RAM_ODT_DIMM_A		RAM_CSCKEODT	RAM_CSCKEODT	1594

	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
RAM_CLKA_P	RAM_KODIAK_CLK_EC	RAM_CLK	RAM_CLK	RAM_KODIAK_CLK_DP	206
RAM_CLKA_N		RAM_CLK	RAM_CLK	RAM_KODIAK_CLK_DP	207
RAM_DIMM_A_CLK_P0	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK0_DP	210
RAM_DIMM_A_CLK_N0	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK0_DP	211
RAM_DIMM_A_CLK_P1	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK1_DP	212
RAM_DIMM_A_CLK_N1	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK1_DP	213
RAM_DIMM_A_CLK_P2	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK2_DP	214
RAM_DIMM_A_CLK_N2	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK2_DP	215
RAM_ONBOARD_CLK_P0_1	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK0_DP	1648
RAM_ONBOARD_CLK_N0_1	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK0_DP	1647
RAM_ONBOARD_CLK_P2_3	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK2_DP	2218
RAM_ONBOARD_CLK_N2_3	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK2_DP	2219
RAM_ONBOARD_CLK_P4_5	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK4_DP	2220
RAM_ONBOARD_CLK_N4_5	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK4_DP	2221
RAM_ONBOARD_CLK_P6_7	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK6_DP	2222
RAM_ONBOARD_CLK_N6_7	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK6_DP	2223
RAM_CLK_FBIN_P	RAM_FB_CLK_EC	RAM_CLK	RAM_CLK	RAM_FBIN_CLK_DP	2224
RAM_CLK_FBIN_N		RAM_CLK	RAM_CLK	RAM_FBIN_CLK_DP	2225
RAM_CLK_FBOUT_P		RAM_CLK	RAM_CLK	RAM_FBOUT_CLK_DP	2226
RAM_CLK_FBOUT_N		RAM_CLK	RAM_CLK	RAM_FBOUT_CLK_DP	2227
RAM_DQ<7..0>	RAM_DQS0_EC	RAM_CAD	RAM_CAD		2428
RAM_DQS_P<0>	RAM_DQS0_EC	RAM_DQS	RAM_DQS	RAM_DQS_0_DP	2429
RAM_DQS_N<0>	RAM_DQS0_EC	RAM_DQS	RAM_DQS	RAM_DQS_0_DP	1470
RAM_DQ<15..8>	RAM_DQS1_EC	RAM_CAD	RAM_CAD		2430
RAM_DQS_P<1>	RAM_DQS1_EC	RAM_DQS	RAM_DQS	RAM_DQS_1_DP	2431
RAM_DQS_N<1>	RAM_DQS1_EC	RAM_DQS	RAM_DQS	RAM_DQS_1_DP	1471
RAM_DQ<23..16>	RAM_DQS2_EC	RAM_CAD	RAM_CAD		2454
RAM_DQS_P<2>	RAM_DQS2_EC	RAM_DQS	RAM_DQS	RAM_DQS_2_DP	2455
RAM_DQS_N<2>	RAM_DQS2_EC	RAM_DQS	RAM_DQS	RAM_DQS_2_DP	1472
RAM_DQ<31..24>	RAM_DQS3_EC	RAM_CAD	RAM_CAD		2456
RAM_DQS_P<3>	RAM_DQS3_EC	RAM_DQS	RAM_DQS	RAM_DQS_3_DP	2457
RAM_DQS_N<3>	RAM_DQS3_EC	RAM_DQS	RAM_DQS	RAM_DQS_3_DP	1473
RAM_DQ<39..32>	RAM_DQS4_EC	RAM_CAD	RAM_CAD		2458
RAM_DQS_P<4>	RAM_DQS4_EC	RAM_DQS	RAM_DQS	RAM_DQS_4_DP	2459
RAM_DQS_N<4>	RAM_DQS4_EC	RAM_DQS	RAM_DQS	RAM_DQS_4_DP	1474
RAM_DQ<47..40>	RAM_DQS5_EC	RAM_CAD	RAM_CAD		2460
RAM_DQS_P<5>	RAM_DQS5_EC	RAM_DQS	RAM_DQS	RAM_DQS_5_DP	2461
RAM_DQS_N<5>	RAM_DQS5_EC	RAM_DQS	RAM_DQS	RAM_DQS_5_DP	1475
RAM_DQ<55..48>	RAM_DQS6_EC	RAM_CAD	RAM_CAD		2462
RAM_DQS_P<6>	RAM_DQS6_EC	RAM_DQS	RAM_DQS	RAM_DQS_6_DP	2463
RAM_DQS_N<6>	RAM_DQS6_EC	RAM_DQS	RAM_DQS	RAM_DQS_6_DP	1476
RAM_DQ<63..56>	RAM_DQS7_EC	RAM_CAD	RAM_CAD		2464
RAM_DQS_P<7>	RAM_DQS7_EC	RAM_DQS	RAM_DQS	RAM_DQS_7_DP	2465
RAM_DQS_N<7>	RAM_DQS7_EC	RAM_DQS	RAM_DQS	RAM_DQS_7_DP	1477
RAM_DQ<71..64>	RAM_DQS8_EC	RAM_CAD	RAM_CAD		2207
RAM_DQS_P<8>	RAM_DQS8_EC	RAM_DQS	RAM_DQS	RAM_DQS_8_DP	2466
RAM_DQS_N<8>	RAM_DQS8_EC	RAM_DQS	RAM_DQS	RAM_DQS_8_DP	1478
RAM_DQ<79..72>	RAM_DQS9_EC	RAM_CAD	RAM_CAD		2688
RAM_DQS_P<9>	RAM_DQS9_EC	RAM_DQS	RAM_DQS	RAM_DQS_9_DP	2689
RAM_DQS_N<9>	RAM_DQS9_EC	RAM_DQS	RAM_DQS	RAM_DQS_9_DP	1479
RAM_DQ<87..80>	RAM_DQS10_EC	RAM_CAD	RAM_CAD		2690
RAM_DQS_P<10>	RAM_DQS10_EC	RAM_DQS	RAM_DQS	RAM_DQS_10_DP	2691
RAM_DQS_N<10>	RAM_DQS10_EC	RAM_DQS	RAM_DQS	RAM_DQS_10_DP	1480
RAM_DQ<95..88>	RAM_DQS11_EC	RAM_CAD	RAM_CAD		2692
RAM_DQS_P<11>	RAM_DQS11_EC	RAM_DQS	RAM_DQS	RAM_DQS_11_DP	2693
RAM_DQS_N<11>	RAM_DQS11_EC	RAM_DQS	RAM_DQS	RAM_DQS_11_DP	1481
RAM_DQ<103..96>	RAM_DQS12_EC	RAM_CAD	RAM_CAD		2270
RAM_DQS_P<12>	RAM_DQS12_EC	RAM_DQS	RAM_DQS	RAM_DQS_12_DP	2271
RAM_DQS_N<12>	RAM_DQS12_EC	RAM_DQS	RAM_DQS	RAM_DQS_12_DP	1482
RAM_DQ<111..104>	RAM_DQS13_EC	RAM_CAD	RAM_CAD		2272
RAM_DQS_P<13>	RAM_DQS13_EC	RAM_DQS	RAM_DQS	RAM_DQS_13_DP	2273
RAM_DQS_N<13>	RAM_DQS13_EC	RAM_DQS	RAM_DQS	RAM_DQS_13_DP	1483
RAM_DQ<119..112>	RAM_DQS14_EC	RAM_CAD	RAM_CAD		2274
RAM_DQS_P<14>	RAM_DQS14_EC	RAM_DQS	RAM_DQS	RAM_DQS_14_DP	2275
RAM_DQS_N<14>	RAM_DQS14_EC	RAM_DQS	RAM_DQS	RAM_DQS_14_DP	1484
RAM_DQ<127..120>	RAM_DQS15_EC	RAM_CAD	RAM_CAD		2276
RAM_DQS_P<15>	RAM_DQS15_EC	RAM_DQS	RAM_DQS	RAM_DQS_15_DP	2277
RAM_DQS_N<15>	RAM_DQS15_EC	RAM_DQS	RAM_DQS	RAM_DQS_15_DP	1485
RAM_DQ_R<127..0>		RAM_CAD	RAM_CAD		2254
RAM_DQS_P_R<15..0>		RAM_DQS	RAM_DQS		2255
RAM_DQS_N_R<15..0>		RAM_DQS	RAM_DQS		1486
RAM_A<15..14>	RAM_A_CTL_EC	RAM_CAD	RAM_CAD		1572
RAM_A<13..0>	RAM_A_CTL_EC	RAM_CAD	RAM_CAD		2256
RAM_BA<1..0>	RAM_A_CTL_EC	RAM_CAD	RAM_CAD		2258
RAM_BA<2>	RAM_A_CTL_1_EC	RAM_CAD	RAM_CAD		1571
RAM_RAS_L	RAM_A_CTL_EC	RAM_CAD	RAM_CAD		2257
RAM_CAS_L	RAM_A_CTL_EC	RAM_CAD	RAM_CAD		2688
RAM_WE_L	RAM_A_CTL_EC	RAM_CAD	RAM_CAD		2689
RAM_A_R<15..0>		RAM_CAD	RAM_CAD		2686
RAM_BA_R<2..0>		RAM_CAD	RAM_CAD		2684
RAM_RAS_L_R		RAM_CAD	RAM_CAD		2683
RAM_CAS_L_R		RAM_CAD	RAM_CAD		2682
RAM_WE_L_R		RAM_CAD	RAM_CAD		1681

RAM_CLK PRIMARY SPACING SET BASED ON DIFF IMPEDANCE
RAM_CLK LINE-LINE SPACING SET TO 15MIL
TOTAL LENGTH TOLERENCE = 20PS = 2.82MM

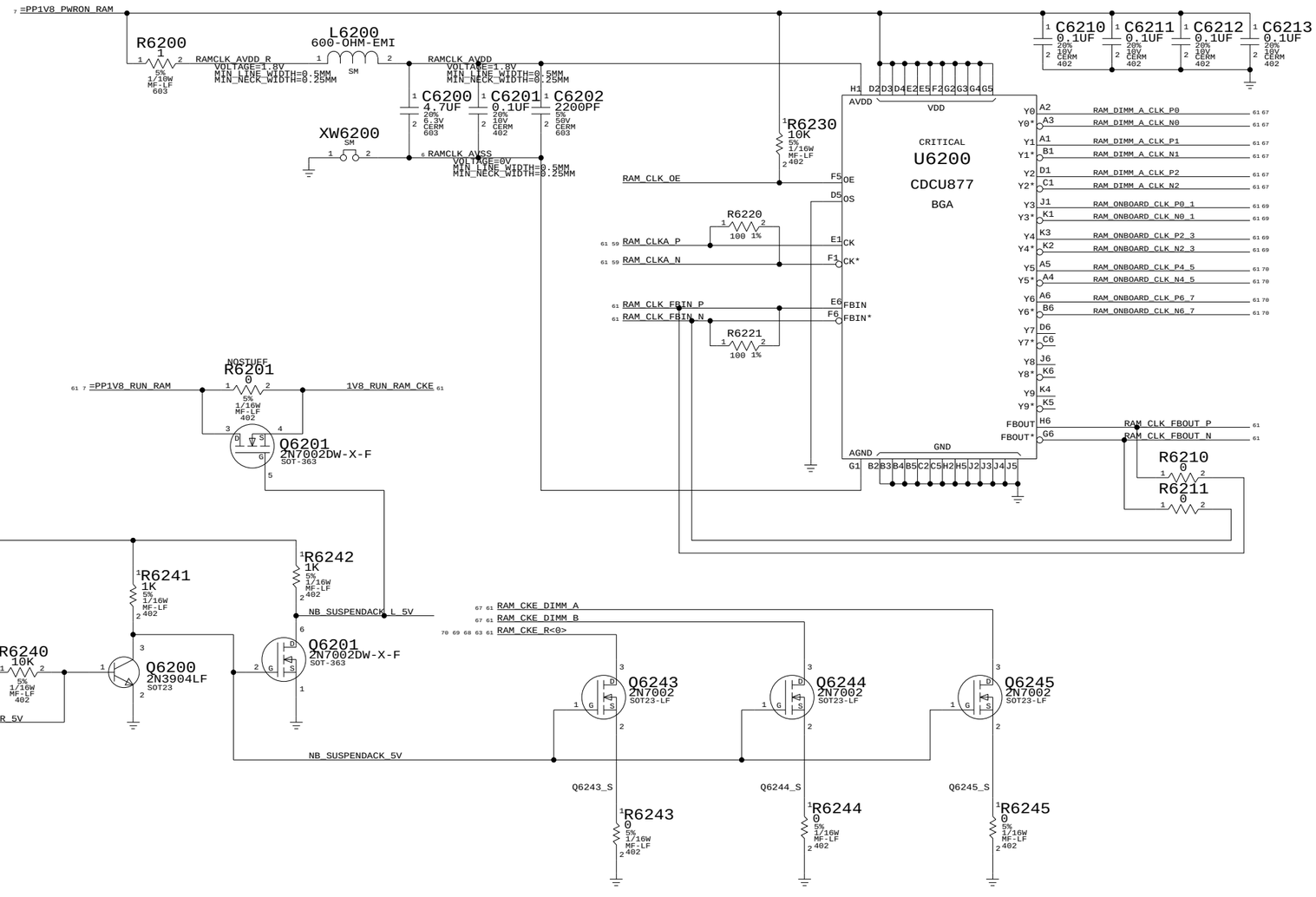
RAM_CAD SPACING IS 10MIL

Parallel Term

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 61 OF 154	

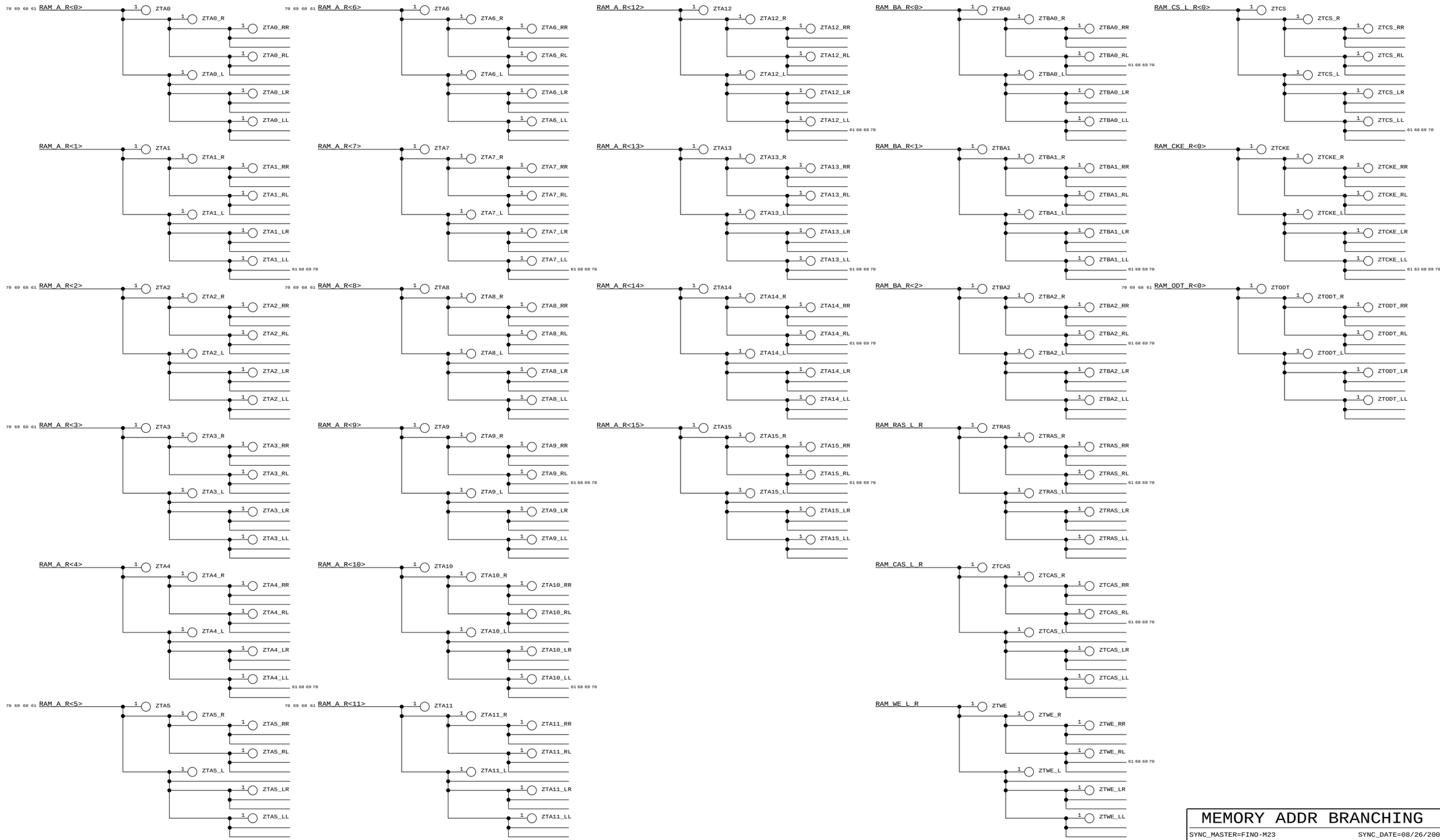


Main Memory Clock Buffer

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 62 OF 154	



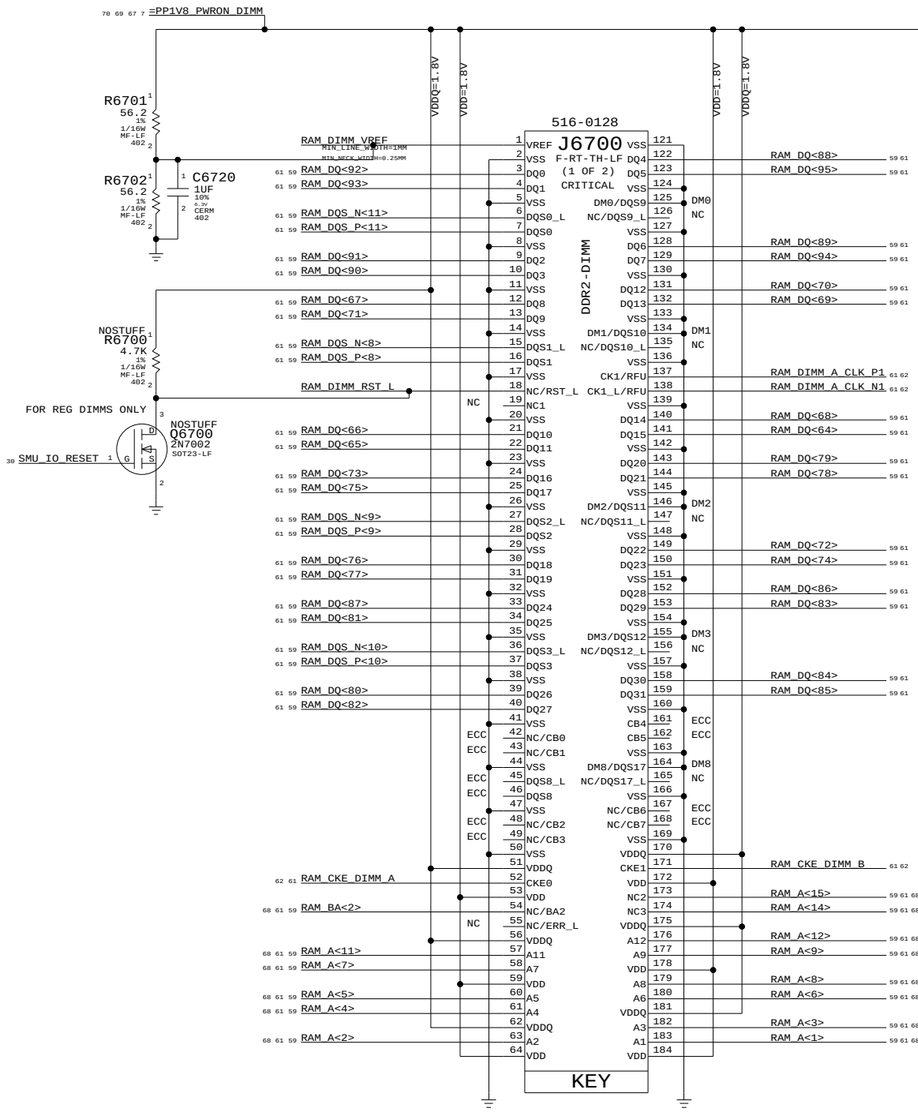
MEMORY ADDR BRANCHING

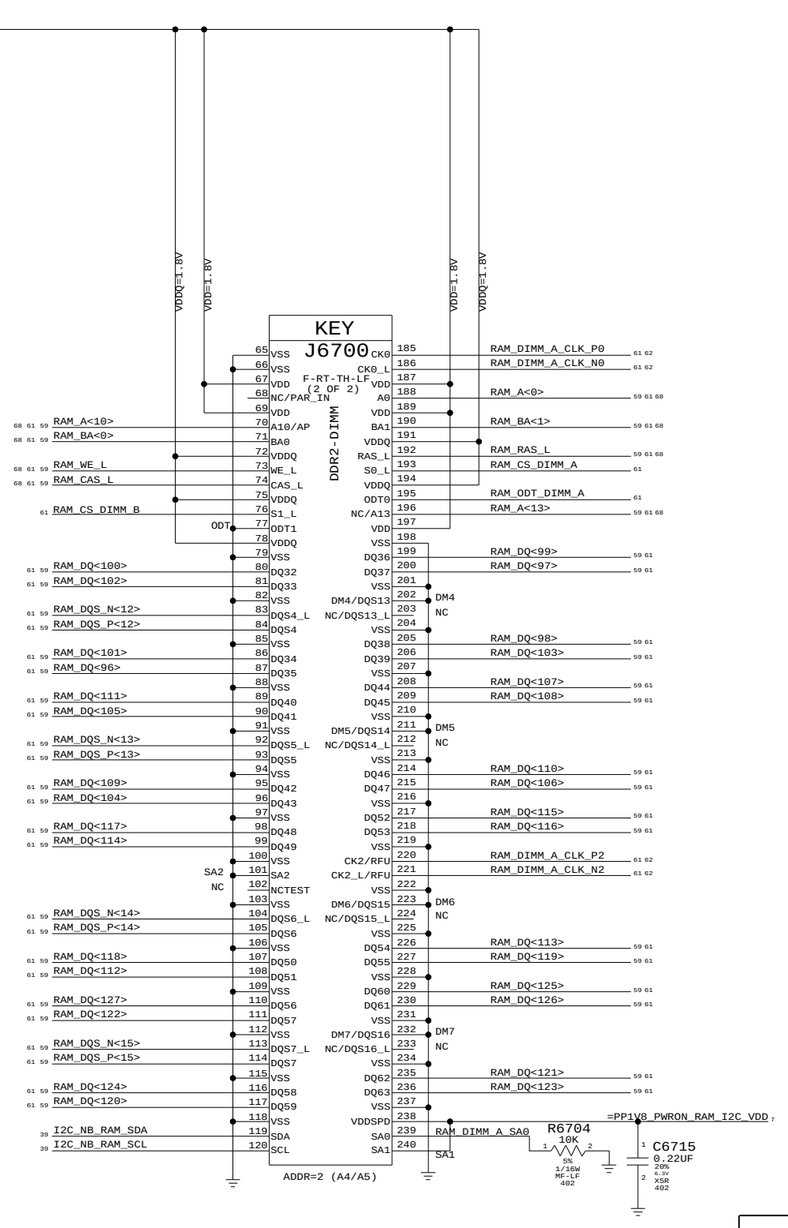
SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE COMPUTER INC.

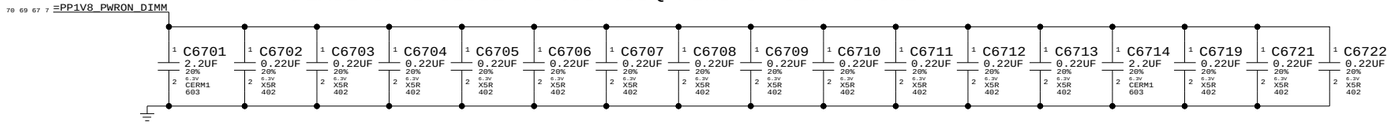
SIZE	DRAWING NUMBER	REV.
D	051-6863	F

SCALE NONE SHT 63 OF 154





PLACE CAPS CLOSE TO VDD/VDDQ PINS OF DIMM SOCKET



Memory Dimm A

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE	SHT	OF
NONE	67	154

ONBOARD MEMORY SHOULD FOLLOW SPEC FOR RAW CARD VERSION A

RAM_DQ<0>	22	4	5	RP6800 RAM_DQ_R<0>
RAM_DQ<1>	22	3	6	RP6800 RAM_DQ_R<1>
RAM_DQ<2>	22	1	8	RP6801 RAM_DQ_R<2>
RAM_DQ<3>	22	3	6	RP6801 RAM_DQ_R<3>
RAM_DQ<4>	22	4	5	RP6801 RAM_DQ_R<4>
RAM_DQ<5>	22	2	7	RP6800 RAM_DQ_R<5>
RAM_DQ<6>	22	2	7	RP6801 RAM_DQ_R<6>
RAM_DQ<7>	22	1	8	RP6800 RAM_DQ_R<7>
RAM_DQ<8>	22	3	6	RP6802 RAM_DQ_R<8>
RAM_DQ<9>	22	4	5	RP6803 RAM_DQ_R<9>
RAM_DQ<10>	22	1	8	RP6803 RAM_DQ_R<10>
RAM_DQ<11>	22	4	5	RP6802 RAM_DQ_R<11>
RAM_DQ<12>	22	3	6	RP6803 RAM_DQ_R<12>
RAM_DQ<13>	22	2	7	RP6802 RAM_DQ_R<13>
RAM_DQ<14>	22	2	7	RP6803 RAM_DQ_R<14>
RAM_DQ<15>	22	1	8	RP6802 RAM_DQ_R<15>
RAM_DQ<16>	22	3	6	RP6805 RAM_DQ_R<16>
RAM_DQ<17>	22	4	5	RP6805 RAM_DQ_R<17>
RAM_DQ<18>	22	1	8	RP6804 RAM_DQ_R<18>
RAM_DQ<19>	22	2	7	RP6805 RAM_DQ_R<19>
RAM_DQ<20>	22	2	7	RP6804 RAM_DQ_R<20>
RAM_DQ<21>	22	4	5	RP6804 RAM_DQ_R<21>
RAM_DQ<22>	22	3	6	RP6804 RAM_DQ_R<22>
RAM_DQ<23>	22	1	8	RP6805 RAM_DQ_R<23>
RAM_DQ<24>	22	4	5	RP6807 RAM_DQ_R<24>
RAM_DQ<25>	22	2	7	RP6806 RAM_DQ_R<25>
RAM_DQ<26>	22	4	5	RP6806 RAM_DQ_R<26>
RAM_DQ<27>	22	1	8	RP6807 RAM_DQ_R<27>
RAM_DQ<28>	22	3	6	RP6807 RAM_DQ_R<28>
RAM_DQ<29>	22	3	6	RP6806 RAM_DQ_R<29>
RAM_DQ<30>	22	2	7	RP6807 RAM_DQ_R<30>
RAM_DQ<31>	22	1	8	RP6806 RAM_DQ_R<31>
RAM_DQ<32>	22	4	5	RP6809 RAM_DQ_R<32>
RAM_DQ<33>	22	2	7	RP6808 RAM_DQ_R<33>
RAM_DQ<34>	22	3	6	RP6808 RAM_DQ_R<34>
RAM_DQ<35>	22	1	8	RP6809 RAM_DQ_R<35>
RAM_DQ<36>	22	2	7	RP6809 RAM_DQ_R<36>
RAM_DQ<37>	22	1	8	RP6808 RAM_DQ_R<37>
RAM_DQ<38>	22	3	6	RP6809 RAM_DQ_R<38>
RAM_DQ<39>	22	4	5	RP6808 RAM_DQ_R<39>
RAM_DQ<40>	22	4	5	RP6810 RAM_DQ_R<40>
RAM_DQ<41>	22	3	6	RP6811 RAM_DQ_R<41>
RAM_DQ<42>	22	1	8	RP6811 RAM_DQ_R<42>
RAM_DQ<43>	22	2	7	RP6810 RAM_DQ_R<43>
RAM_DQ<44>	22	4	5	RP6811 RAM_DQ_R<44>
RAM_DQ<45>	22	3	6	RP6810 RAM_DQ_R<45>
RAM_DQ<46>	22	2	7	RP6811 RAM_DQ_R<46>
RAM_DQ<47>	22	1	8	RP6810 RAM_DQ_R<47>
RAM_DQ<48>	22	3	6	RP6812 RAM_DQ_R<48>
RAM_DQ<49>	22	4	5	RP6812 RAM_DQ_R<49>
RAM_DQ<50>	22	2	7	RP6813 RAM_DQ_R<50>
RAM_DQ<51>	22	1	8	RP6813 RAM_DQ_R<51>
RAM_DQ<52>	22	3	6	RP6813 RAM_DQ_R<52>
RAM_DQ<53>	22	4	5	RP6813 RAM_DQ_R<53>
RAM_DQ<54>	22	2	7	RP6812 RAM_DQ_R<54>
RAM_DQ<55>	22	1	8	RP6812 RAM_DQ_R<55>
RAM_DQ<56>	22	3	6	RP6814 RAM_DQ_R<56>
RAM_DQ<57>	22	4	5	RP6815 RAM_DQ_R<57>
RAM_DQ<58>	22	2	7	RP6815 RAM_DQ_R<58>
RAM_DQ<59>	22	3	6	RP6815 RAM_DQ_R<59>
RAM_DQ<60>	22	2	7	RP6814 RAM_DQ_R<60>
RAM_DQ<61>	22	1	8	RP6814 RAM_DQ_R<61>
RAM_DQ<62>	22	1	8	RP6815 RAM_DQ_R<62>
RAM_DQ<63>	22	4	5	RP6814 RAM_DQ_R<63>

RAM_DQS_P<0>	22	1	2	R6800 RAM_DQS_P_R<0>
RAM_DQS_N<0>	22	1	2	R6810 RAM_DQS_N_R<0>
RAM_DQS_P<1>	22	1	2	R6801 RAM_DQS_P_R<1>
RAM_DQS_N<1>	22	1	2	R6811 RAM_DQS_N_R<1>
RAM_DQS_P<2>	22	1	2	R6802 RAM_DQS_P_R<2>
RAM_DQS_N<2>	22	1	2	R6812 RAM_DQS_N_R<2>
RAM_DQS_P<3>	22	1	2	R6803 RAM_DQS_P_R<3>
RAM_DQS_N<3>	22	1	2	R6813 RAM_DQS_N_R<3>
RAM_DQS_P<4>	22	1	2	R6804 RAM_DQS_P_R<4>
RAM_DQS_N<4>	22	1	2	R6814 RAM_DQS_N_R<4>
RAM_DQS_P<5>	22	1	2	R6805 RAM_DQS_P_R<5>
RAM_DQS_N<5>	22	1	2	R6815 RAM_DQS_N_R<5>
RAM_DQS_P<6>	22	1	2	R6806 RAM_DQS_P_R<6>
RAM_DQS_N<6>	22	1	2	R6816 RAM_DQS_N_R<6>
RAM_DQS_P<7>	22	1	2	R6807 RAM_DQS_P_R<7>
RAM_DQS_N<7>	22	1	2	R6817 RAM_DQS_N_R<7>

RAM_A<0>	5.1	1	8	RP6824 RAM_A_R<0> ZT6800
RAM_A<1>	5.1	1	8	RP6823 RAM_A_R<1> ZT6801
RAM_A<2>	5.1	2	7	RP6823 RAM_A_R<2> ZT6802
RAM_A<3>	5.1	4	5	RP6822 RAM_A_R<3> ZT6803
RAM_A<4>	5.1	3	6	RP6822 RAM_A_R<4> ZT6804
RAM_A<5>	5.1	2	7	RP6822 RAM_A_R<5> ZT6805
RAM_A<6>	5.1	1	8	RP6822 RAM_A_R<6> ZT6806
RAM_A<7>	5.1	3	6	RP6821 RAM_A_R<7> ZT6807
RAM_A<8>	5.1	4	5	RP6821 RAM_A_R<8> ZT6808
RAM_A<9>	5.1	1	8	RP6821 RAM_A_R<9> ZT6809
RAM_A<10>	5.1	3	6	RP6824 RAM_A_R<10> ZT6810
RAM_A<11>	5.1	2	7	RP6821 RAM_A_R<11> ZT6811
RAM_A<12>	5.1	4	5	RP6820 RAM_A_R<12> ZT6812
RAM_A<13>	5.1	4	5	RP6825 RAM_A_R<13> ZT6813
RAM_A<14>	5.1	2	7	RP6820 RAM_A_R<14> ZT6814
RAM_A<15>	5.1	1	8	RP6820 RAM_A_R<15> ZT6815

VIAS FOR ECC STUB

RAM_BA<0>	5.1	4	5	RP6824 RAM_BA_R<0> ZT6820
RAM_BA<1>	5.1	2	7	RP6824 RAM_BA_R<1> ZT6821
RAM_BA<2>	5.1	3	6	RP6820 RAM_BA_R<2> ZT6822
RAM_RAS_L	5.1	1	8	RP6825 RAM_RAS_L_R ZT6825
RAM_CAS_L	5.1	3	6	RP6825 RAM_CAS_L_R ZT6826
RAM_WE_L	5.1	2	7	RP6825 RAM_WE_L_R ZT6827

VIAS FOR ECC STUB

PLACE NEAR KODIAK PRIOR TO BRANCH

PLACE AT END POINT TO SIMULATE ECC

C6870 24PF 5% 50V C0G 402	C6871 2PF +/-0.25PF 50V C0G 402-1	RAM_CS_L_R<0>
C6880 24PF 5% 50V C0G 402	C6881 2PF +/-0.25PF 50V C0G 402-1	RAM_CKE_R<0>
C6890 24PF 5% 50V C0G 402	C6891 2PF +/-0.25PF 50V C0G 402-1	RAM_ODT_R<0>

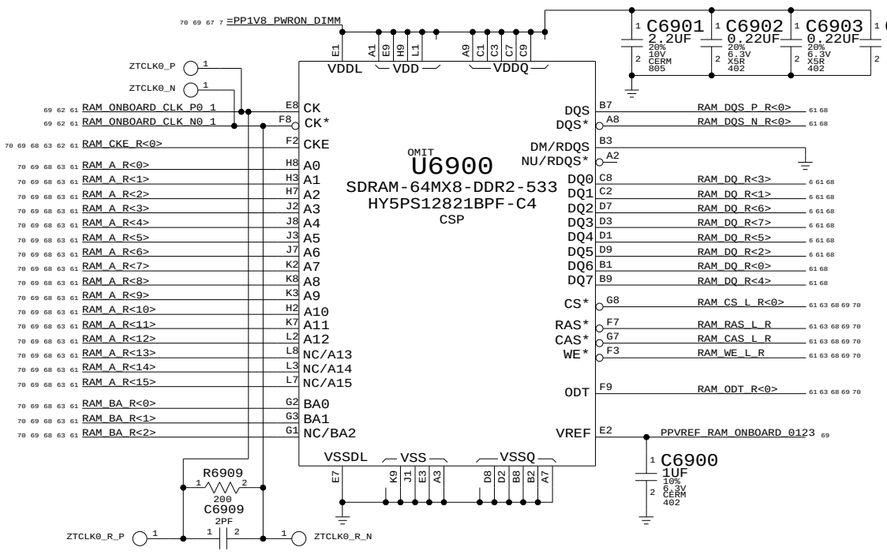
MLB Mem Series Term

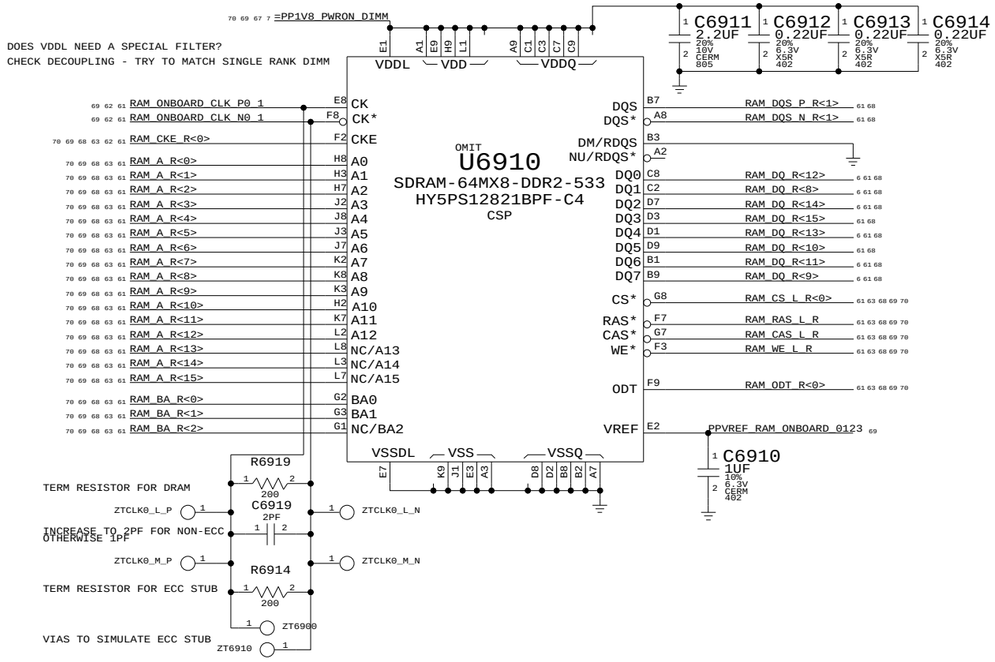
SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

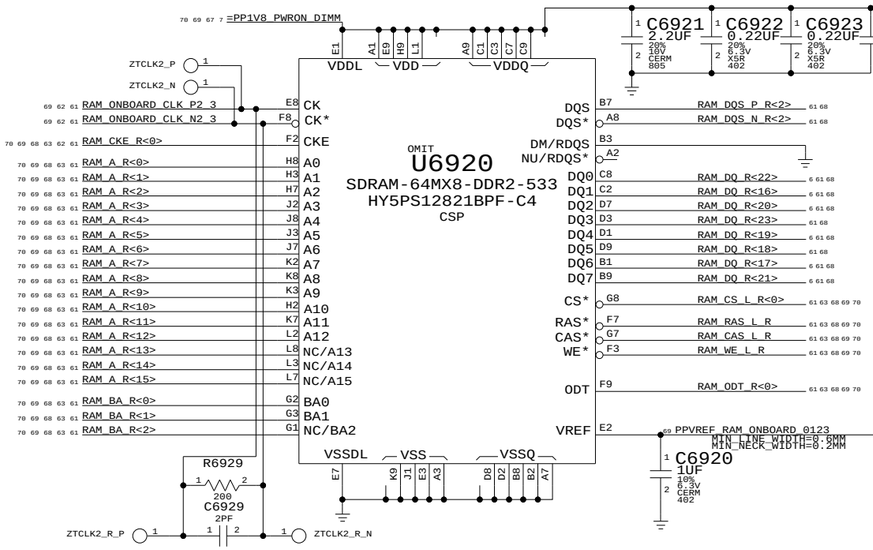
NOTICE OF PROPRIETARY PROPERTY

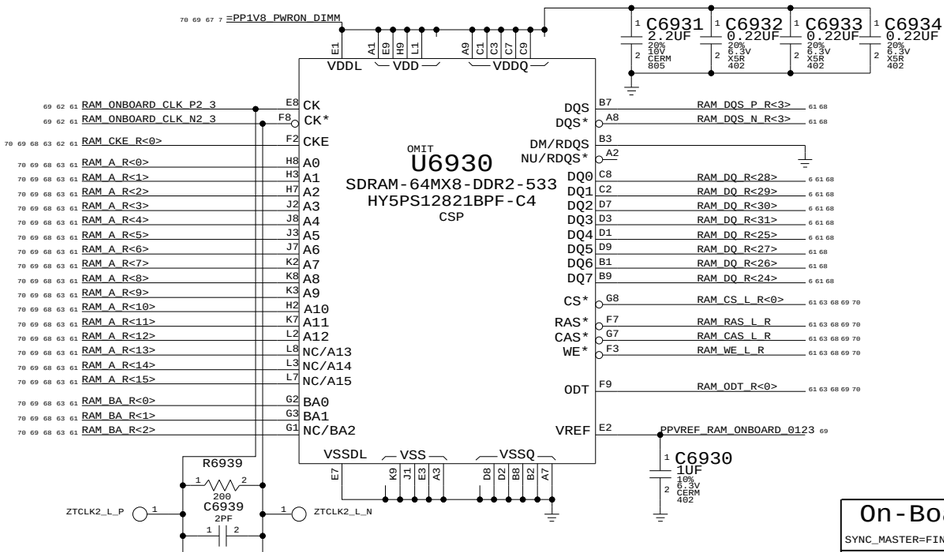
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 68 OF 154	









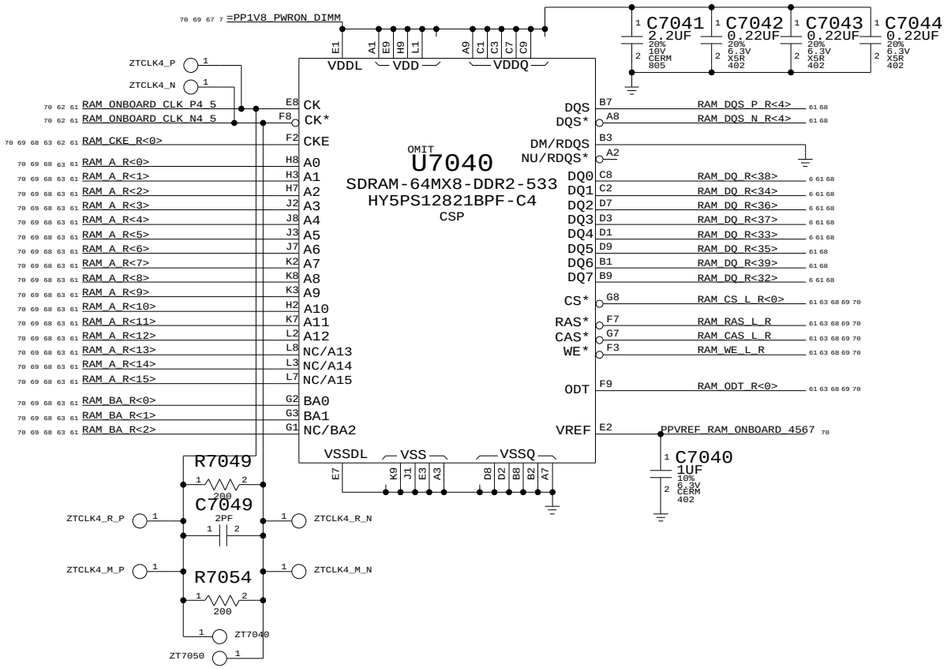
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333T0032	4	IC,SDRAM,DDR2,512MBIT,X8	U6900,U6910,U6920,U6930	CRITICAL	
333T0032	4	IC,SDRAM,DDR2,512MBIT,X8	U7040,U7050,U7060,U7070	CRITICAL	

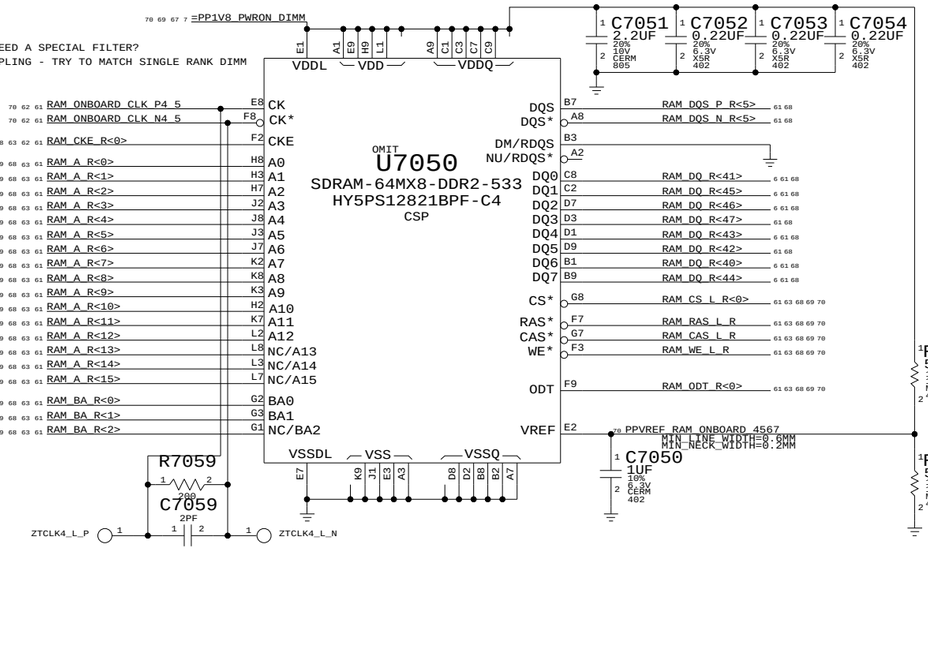
On-Board DDR SDRAM

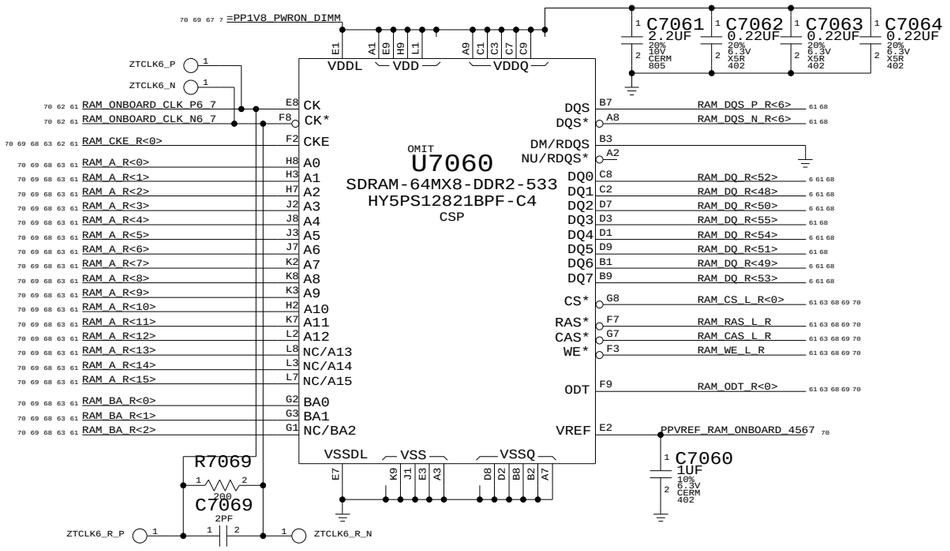
SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

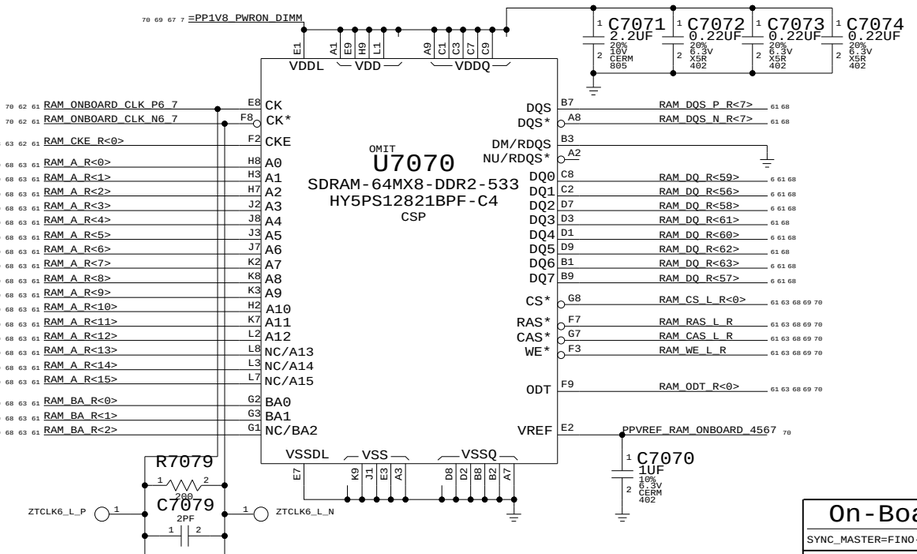
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 69 OF 154	









On-Board DDR SDRAM

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 70 OF 154	

KODIAK AVDD FILTERING
(LOCATE CLOSE TO POWER AND GROUND PINS)

L8200 0.22UH 0805-1 — =PP2V5_PWRON_NB_PCIE → PWR_PCIE_A_AVDD_2
C8200 0.01UF 10% 16V CERM 402
C8201 10UF 10% 6.3V X5R 805
C8202 1UF 10% 6.3V CERM 402
KOD_G10_GND (THIS PAGE)

L8201 0.22UH 0805-1 — =PP2V5_PWRON_NB_PCIE → PWR_PCIE_A_AVDD_1
C8203 0.01UF 10% 16V CERM 402
C8204 10UF 10% 6.3V X5R 805
C8205 1UF 10% 6.3V CERM 402
KOD_K07_GND (THIS PAGE)

L8202 0.22UH 0805-1 — =PP2V5_PWRON_NB_PCIE → PWR_PCIE_A_AVDD_0
C8206 0.01UF 10% 16V CERM 402
C8207 10UF 10% 6.3V X5R 805
C8208 1UF 10% 6.3V CERM 402
KOD_H05_GND (THIS PAGE)

PWR_PCIE_A_AVDD_2 (J06) PWR_PCIE_A_AVDD_1 (J07) PWR_PCIE_A_AVDD_0 (H11)
PWR_PCIE_A_AVDD_A (J12) PWR_PCIE_A_AVDD_B (K13) PWR_PCIE_A_AVDD_C (J09)

L8203 0.22UH 0805-1 — =PP2V5_PWRON_NB_PCIE
PWR_PCIE_A_AVDD → C8222 1UF, C8225 1UF, C8223 10UF, C8224 0.01UF
KOD_L13_GND (THIS PAGE)
KOD_J13_GND (THIS PAGE)

L8205 0.22UH 0805-1 — =PP2V5_PWRON_NB_PCIE
C8228 1UF, C8229 10UF, C8230 0.01UF
KOD_H08_GND (THIS PAGE)

KODIAK PCI-E 100MHZ REFCLK
PP8201 P4MM SM
100+ CLK_KOD_100M_PF<0>
100- CLK_KOD_100M_NF<0>
PP8200 P4MM SM

R8202 20.5 1% 1/16W MF-LF 402 — CLK_KOD_100M_P<0> → 100M_P<0>
C8245 0.01UF 10% 16V CERM 402
R8203 29.4 1% 1/16W MF-LF 402 — NOSTUFF
C8244 0.01UF 10% 16V CERM 402 — 100M_G
R8204 29.4 1% 1/16W MF-LF 402
R8205 20.5 1% 1/16W MF-LF 402 — CLK_KOD_100M_N<0> → 100M_N<0>
C8246 0.01UF 10% 16V CERM 402

KODIAK PCIE REFCLK TERMINATION
(LOCATE CLOSE TO INPUT PINS)

=PP2V5_PWRON_NB_PCIE
R8200 8.2K 5% 1/10W MF-LF 402
PCIE_SLOTA_PRSNT_L
R8201 200 1% 1/10W MF-LF 402

KODIAK PCI-E DECOUPLING
(LOCATE CLOSE TO POWER AND GROUND PINS)
=PPVCORE_PWRON_NB_PCIE
C8209 C8210 C8211 C8212 C8213 C8214 C8215 C8216 C8217 C8218 C8219 C8220 C8221
1UF 10% 6.3V CERM 402

U1900
KODIAK-ASIC-040812
PCI-E X16 INTERFACE
BGA
(5 OF 10)
SEE_TABLE

PCIE_AVDD_0 (1.65V-2.75V) SERDES	PCIE_AVDD_1 (1.65V-2.75V) SERDES	PCIE_AVDD_2 (1.65V-2.75V) SERDES	PCIE_REFCLK_AVDDA (1.65V-2.75V) PLL
PCIE_REFCLK_AVDDB (1.65V-2.75V) PLL	PCIE_REFCLK_AVDD2 (1.65V-2.75V) PLL		

(1.6V-1.2V)
PCIE_VDD: A04 A08 A12 B06 B10 C03 D01 D04 D08 D12 E06 E10 E14
PCIE_VDD: F02 F05 G08 G12 H01 H04 H07 H10 H14 K12 L11 L14 M12
=PPVCORE_PWRON_NB_PCIE

PCIE_REFCLK_P J11
PCIE_REFCLK_N J10 (100MHZ)

PCIE_HSIN0 G05 … PCIE_HSIN15 F07
PCIE_HSIP0 G04 … PCIE_HSIP15 F08
PCIE_PRESENTN AJ02
PCIE_UCAL_RES0 F14
PCIE_UCAL_RES1 J14

(DNU) PCIE_AVREG_2 G11 — NC_A_AVREG_2
PCIE_AVREG_1 J08 — NC_A_AVREG_1
PCIE_AVREG_0 E04 — NC_A_AVREG_0

PCIE_GND: A06 A10 B02 B04 B08 B12 D02 D06 D10 D14 E08 E12 F01
PCIE_GND: F04 F06 G14 H02 H12 K10 K14 L12 M11 M13

AVDD_0_GND H05 — KOD_H05_GND
AVDD_1_GND K07 — KOD_K07_GND
AVDD_2_GND G10 — KOD_G10_GND
(THIS PAGE, X3)
XW8200 XW8201 XW8202 SM

REFCLK_AGNDA J13 — KOD_H08_GND
REFCLK_AGNDB L13 — KOD_L13_GND
REFCLK_AGND2 H08 — KOD_J13_GND
(THIS PAGE, X3)
XW8203 XW8204 XW8205 SM

KODIAK PCI-E AC COUPLERS
(LOCATE NEAR SOURCE PINS)

PCIE_HSON0	D03	PCIE_NB_TO_SLOTA_NF<0>	0.1UF	C8247	PCIE_NB_TO_SLOTA_N<0>
PCIE_HSOP0	E03	PCIE_NB_TO_SLOTA_PF<0>	0.1UF	C8248	PCIE_NB_TO_SLOTA_P<0>
PCIE_HSON1	J01	PCIE_NB_TO_SLOTA_NF<1>	0.1UF	C8249	PCIE_NB_TO_SLOTA_N<1>
PCIE_HSOP1	J02	PCIE_NB_TO_SLOTA_PF<1>	0.1UF	C8250	PCIE_NB_TO_SLOTA_P<1>
PCIE_HSON2	C01	PCIE_NB_TO_SLOTA_NF<2>	0.1UF	C8251	PCIE_NB_TO_SLOTA_N<2>
PCIE_HSOP2	C02	PCIE_NB_TO_SLOTA_PF<2>	0.1UF	C8252	PCIE_NB_TO_SLOTA_P<2>
PCIE_HSON3	A07	PCIE_NB_TO_SLOTA_NF<3>	0.1UF	C8253	PCIE_NB_TO_SLOTA_N<3>
PCIE_HSOP3	B07	PCIE_NB_TO_SLOTA_PF<3>	0.1UF	C8254	PCIE_NB_TO_SLOTA_P<3>
PCIE_HSON4	F03	PCIE_NB_TO_SLOTA_NF<4>	0.1UF	C8255	PCIE_NB_TO_SLOTA_N<4>
PCIE_HSOP4	G03	PCIE_NB_TO_SLOTA_PF<4>	0.1UF	C8256	PCIE_NB_TO_SLOTA_P<4>
PCIE_HSON5	H03	PCIE_NB_TO_SLOTA_NF<5>	0.1UF	C8257	PCIE_NB_TO_SLOTA_N<5>
PCIE_HSOP5	J03	PCIE_NB_TO_SLOTA_PF<5>	0.1UF	C8258	PCIE_NB_TO_SLOTA_P<5>
PCIE_HSON6	A03	PCIE_NB_TO_SLOTA_NF<6>	0.1UF	C8259	PCIE_NB_TO_SLOTA_N<6>
PCIE_HSOP6	B03	PCIE_NB_TO_SLOTA_PF<6>	0.1UF	C8260	PCIE_NB_TO_SLOTA_P<6>
PCIE_HSON7	A05	PCIE_NB_TO_SLOTA_NF<7>	0.1UF	C8261	PCIE_NB_TO_SLOTA_N<7>
PCIE_HSOP7	B05	PCIE_NB_TO_SLOTA_PF<7>	0.1UF	C8262	PCIE_NB_TO_SLOTA_P<7>
PCIE_HSON8	C11	PCIE_NB_TO_SLOTA_NF<8>	0.1UF	C8263	PCIE_NB_TO_SLOTA_N<8>
PCIE_HSOP8	C10	PCIE_NB_TO_SLOTA_PF<8>	0.1UF	C8264	PCIE_NB_TO_SLOTA_P<8>
PCIE_HSON9	B11	PCIE_NB_TO_SLOTA_NF<9>	0.1UF	C8265	PCIE_NB_TO_SLOTA_N<9>
PCIE_HSOP9	A11	PCIE_NB_TO_SLOTA_PF<9>	0.1UF	C8266	PCIE_NB_TO_SLOTA_P<9>
PCIE_HSON10	F11	PCIE_NB_TO_SLOTA_NF<10>	0.1UF	C8267	PCIE_NB_TO_SLOTA_N<10>
PCIE_HSOP10	F10	PCIE_NB_TO_SLOTA_PF<10>	0.1UF	C8268	PCIE_NB_TO_SLOTA_P<10>
PCIE_HSON11	B09	PCIE_NB_TO_SLOTA_NF<11>	0.1UF	C8269	PCIE_NB_TO_SLOTA_N<11>
PCIE_HSOP11	A09	PCIE_NB_TO_SLOTA_PF<11>	0.1UF	C8270	PCIE_NB_TO_SLOTA_P<11>
PCIE_HSON12	D13	PCIE_NB_TO_SLOTA_NF<12>	0.1UF	C8271	PCIE_NB_TO_SLOTA_N<12>
PCIE_HSOP12	E13	PCIE_NB_TO_SLOTA_PF<12>	0.1UF	C8272	PCIE_NB_TO_SLOTA_P<12>
PCIE_HSON13	B13	PCIE_NB_TO_SLOTA_NF<13>	0.1UF	C8273	PCIE_NB_TO_SLOTA_N<13>
PCIE_HSOP13	A13	PCIE_NB_TO_SLOTA_PF<13>	0.1UF	C8274	PCIE_NB_TO_SLOTA_P<13>
PCIE_HSON14	D09	PCIE_NB_TO_SLOTA_NF<14>	0.1UF	C8275	PCIE_NB_TO_SLOTA_N<14>
PCIE_HSOP14	E09	PCIE_NB_TO_SLOTA_PF<14>	0.1UF	C8276	PCIE_NB_TO_SLOTA_P<14>
PCIE_HSON15	C08	PCIE_NB_TO_SLOTA_NF<15>	0.1UF	C8277	PCIE_NB_TO_SLOTA_N<15>
PCIE_HSOP15	C09	PCIE_NB_TO_SLOTA_PF<15>	0.1UF	C8278	PCIE_NB_TO_SLOTA_P<15>

=PPVCORE_PWRON_NB_PCIE
C8231 C8232 C8233 C8234 C8235 C8236 C8241 C8242 C8243 C8237 C8238 C8239 C8240
1UF 10% 6.3V CERM 402

KODIAK PCI-E DECOUPLING
(LOCATE CLOSE TO POWER AND GROUND PINS)

KODIAK PCI-E X16

SYNC_MASTER=Q63 SYNC_DATE=08/26/2005

NOTICE OF PROPRIETARY PROPERTY
LAST_MODIFIED=Tue Nov 1 13:47:03 2005
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

PAGE 82

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 82 OF 154	

DRAWING

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
338S0239	1	IC,RV370 XT, GRAPHICS CTLR	U8400	RV370XT	CRITICAL
338S0265	1	IC,RV380 XT A23, GRAPHICS CTLR	U8400	RV380XT	CRITICAL

REMOVED COMPLIANCE TEST POINTS
FINO WILL PLACE COUPLING CAPACITORS ON RECEIVING SIDE
(THIS IS ALLOWED FOR CHIP TO CHIP PCIE)
CAP PAD CAN BE USED FOR COMPLIANCE TEST

7 =PP1V2_GPU_PCIE
THIS IS ALIASED TO
PPVCORE_GPU ON PAGE 7

R8460 0.300 5% 1/8W MF 805
R8461 0.300 5% 1/8W MF 805
R8460 BRINGS VDDR FROM CORE (1.35) TO 1.2

PP1V2_GPU_PCIE_VDDR 84
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM

C8460 1UF 10% 6.3V CERM 402
C8461 1UF 10% 6.3V CERM 402
C8462 1UF 10% 6.3V CERM 402
C8463 0.1UF 20% 10V CERM 402
C8464 0.1UF 20% 10V CERM 402
C8465 0.1UF 20% 10V CERM 402
C8466 0.1UF 20% 10V CERM 402

85 84 PP1V2_GPU_PCIE_PVDD

SYS_POWERUP_L SHOULD CONTROL THE FET ON PP1V2_RUN

C8450 1UF 10% 6.3V CERM 402
C8451 1UF 10% 6.3V CERM 402
C8452 0.1UF 20% 10V CERM 402
C8453 0.1UF 20% 10V CERM 402
C8454 0.1UF 20% 10V CERM 402
C8455 0.1UF 20% 10V CERM 402

93 87 86 85 =PP1V8_GPU
L8440 FERR-220-OHM 0805
PP1V8_GPU_PCIE_PVDD
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM

C8440 1UF 10% 6.3V CERM 402
C8441 1UF 10% 6.3V CERM 402
C8442 0.1UF 20% 10V CERM 402
C8443 0.1UF 20% 10V CERM 402
C8444 0.1UF 20% 10V CERM 402
C8445 0.1UF 20% 10V CERM 402

PLACE R8470 CLOSE TO U9670

20 =GPU_RESET_L
U9670 74LC125 TSSOP
R8469 8.2K 5% 1/16W MF-LF 402
R8470 33 5% 1/10W MF-LF 402
ATI_RESET_L

GROUND VIAS FOR LAYER TRANSITIONS

ZH8400 HOLE-VIA
ZH8401 HOLE-VIA
ZH8402 HOLE-VIA
ZH8403 HOLE-VIA
ZH8404 HOLE-VIA
ZH8405 HOLE-VIA
ZH8406 HOLE-VIA
ZH8407 HOLE-VIA
ZH8408 HOLE-VIA
ZH8409 HOLE-VIA
ZH8410 HOLE-VIA
ZH8411 HOLE-VIA
ZH8412 HOLE-VIA
ZH8413 HOLE-VIA
ZH8414 HOLE-VIA
ZH8415 HOLE-VIA
ZH8416 HOLE-VIA
ZH8417 HOLE-VIA
ZH8418 HOLE-VIA
ZH8419 HOLE-VIA

PP1V2_GPU_PCIE_PVDD 84 85
R8471 301 1% 1/16W MF-LF 402
R8472 21 1% 1/16W MF-LF 402
R8473 21 1% 1/16W MF-LF 402
R8474 60.4 1% 1/16W MF-LF 402
R8475 21 1% 1/16W MF-LF 402
R8476 60.4 1% 1/16W MF-LF 402
R8477 21 1% 1/16W MF-LF 402
R8478 301 1% 1/16W MF-LF 402
PP1V2_GPU_PCIE_PVDD 84 85

CKA_PCIE<0>
C8472 5PF +/-0.25PF 50V CERM 402
C8473 5PF +/-0.25PF 50V CERM 402
CKA_PCIE_N<0>

97 26 CLK_PCIE_SLOTA_P<0>
97 26 CLK_PCIE_SLOTA_N<0>

PCI-E SLOTA 100MHZ
REFCLK TERMINATION
(LOCATE CLOSE TO GPU)

97 CLK_PCIE_SLOTA_PF<0> AF27 PCIE_REFCLKP
97 CLK_PCIE_SLOTA_NF<0> AF27 PCIE_REFCLKN

97 82 9 PCIE_NB_TO_SLOTA_P<0>	AH30	PCIE_RX0P
97 82 9 PCIE_NB_TO_SLOTA_N<0>	AG30	PCIE_RX0N
97 82 9 PCIE_NB_TO_SLOTA_P<1>	AG29	PCIE_RX1P
97 82 9 PCIE_NB_TO_SLOTA_N<1>	AF29	PCIE_RX1N
97 82 9 PCIE_NB_TO_SLOTA_P<2>	AE29	PCIE_RX2P
97 82 9 PCIE_NB_TO_SLOTA_N<2>	AE30	PCIE_RX2N
97 82 9 PCIE_NB_TO_SLOTA_P<3>	AD30	PCIE_RX3P
97 82 9 PCIE_NB_TO_SLOTA_N<3>	AD29	PCIE_RX3N
97 82 9 PCIE_NB_TO_SLOTA_P<4>	AC29	PCIE_RX4P
97 82 9 PCIE_NB_TO_SLOTA_N<4>	AB29	PCIE_RX4N
97 82 9 PCIE_NB_TO_SLOTA_P<5>	AB30	PCIE_RX5P
97 82 9 PCIE_NB_TO_SLOTA_N<5>	AA30	PCIE_RX5N
97 82 9 PCIE_NB_TO_SLOTA_P<6>	AA29	PCIE_RX6P
97 82 9 PCIE_NB_TO_SLOTA_N<6>	Y29	PCIE_RX6N
97 82 9 PCIE_NB_TO_SLOTA_P<7>	W29	PCIE_RX7P
97 82 9 PCIE_NB_TO_SLOTA_N<7>	W30	PCIE_RX7N
97 82 9 PCIE_NB_TO_SLOTA_P<8>	V30	PCIE_RX8P
97 82 9 PCIE_NB_TO_SLOTA_N<8>	V29	PCIE_RX8N
97 82 9 PCIE_NB_TO_SLOTA_P<9>	U29	PCIE_RX9P
97 82 9 PCIE_NB_TO_SLOTA_N<9>	T29	PCIE_RX9N
97 82 9 PCIE_NB_TO_SLOTA_P<10>	T30	PCIE_RX10P
97 82 9 PCIE_NB_TO_SLOTA_N<10>	R30	PCIE_RX10N
97 82 9 PCIE_NB_TO_SLOTA_P<11>	R29	PCIE_RX11P
97 82 9 PCIE_NB_TO_SLOTA_N<11>	P29	PCIE_RX11N
97 82 9 PCIE_NB_TO_SLOTA_P<12>	N29	PCIE_RX12P
97 82 9 PCIE_NB_TO_SLOTA_N<12>	N30	PCIE_RX12N
97 82 9 PCIE_NB_TO_SLOTA_P<13>	M30	PCIE_RX13P
97 82 9 PCIE_NB_TO_SLOTA_N<13>	M29	PCIE_RX13N
97 82 9 PCIE_NB_TO_SLOTA_P<14>	L29	PCIE_RX14P
97 82 9 PCIE_NB_TO_SLOTA_N<14>	K29	PCIE_RX14N
97 82 9 PCIE_NB_TO_SLOTA_P<15>	K30	PCIE_RX15P
97 82 9 PCIE_NB_TO_SLOTA_N<15>	J30	PCIE_RX15N

T23 U23 V23 W23 N23 N24 P23 AG26 AG27 AG28 AJ30 AK29
PCIE_PVDD_18 PCIE_PVDD_12 PCIE_VDDR_12

U8400 RV370XT BGA (1 OF 5) OMIT PCI-E

PERST* AD25 ATI_RESET_L_R

GPU PCI-E AC COUPLERS (PLACE NEAR GPU)

PCIE_TX0P	AF26	97 9 PCIE_SLOTA_TO_NB_PF<0>	0.1UF	C8400	PCIE_SLOTA_TO_NB_P<0>	9 82 97
PCIE_TX0N	AE26	97 9 PCIE_SLOTA_TO_NB_NF<0>	0.1UF	C8401	PCIE_SLOTA_TO_NB_N<0>	9 82 97
PCIE_TX1P	AC25	97 9 PCIE_SLOTA_TO_NB_PF<1>	0.1UF	C8402	PCIE_SLOTA_TO_NB_P<1>	9 82 97
PCIE_TX1N	AB25	97 9 PCIE_SLOTA_TO_NB_NF<1>	0.1UF	C8403	PCIE_SLOTA_TO_NB_N<1>	9 82 97
PCIE_TX2P	AC27	97 9 PCIE_SLOTA_TO_NB_PF<2>	0.1UF	C8404	PCIE_SLOTA_TO_NB_P<2>	9 82 97
PCIE_TX2N	AB27	97 9 PCIE_SLOTA_TO_NB_NF<2>	0.1UF	C8405	PCIE_SLOTA_TO_NB_N<2>	9 82 97
PCIE_TX3P	AC26	97 9 PCIE_SLOTA_TO_NB_PF<3>	0.1UF	C8406	PCIE_SLOTA_TO_NB_P<3>	9 82 97
PCIE_TX3N	AB26	97 9 PCIE_SLOTA_TO_NB_NF<3>	0.1UF	C8407	PCIE_SLOTA_TO_NB_N<3>	9 82 97
PCIE_TX4P	Y25	97 9 PCIE_SLOTA_TO_NB_PF<4>	0.1UF	C8408	PCIE_SLOTA_TO_NB_P<4>	9 82 97
PCIE_TX4N	W25	97 9 PCIE_SLOTA_TO_NB_NF<4>	0.1UF	C8409	PCIE_SLOTA_TO_NB_N<4>	9 82 97
PCIE_TX5P	Y27	97 9 PCIE_SLOTA_TO_NB_PF<5>	0.1UF	C8410	PCIE_SLOTA_TO_NB_P<5>	9 82 97
PCIE_TX5N	W27	97 9 PCIE_SLOTA_TO_NB_NF<5>	0.1UF	C8411	PCIE_SLOTA_TO_NB_N<5>	9 82 97
PCIE_TX6P	Y26	97 9 PCIE_SLOTA_TO_NB_PF<6>	0.1UF	C8412	PCIE_SLOTA_TO_NB_P<6>	9 82 97
PCIE_TX6N	W26	97 9 PCIE_SLOTA_TO_NB_NF<6>	0.1UF	C8413	PCIE_SLOTA_TO_NB_N<6>	9 82 97
PCIE_TX7P	U25	97 9 PCIE_SLOTA_TO_NB_PF<7>	0.1UF	C8414	PCIE_SLOTA_TO_NB_P<7>	9 82 97
PCIE_TX7N	T25	97 9 PCIE_SLOTA_TO_NB_NF<7>	0.1UF	C8415	PCIE_SLOTA_TO_NB_N<7>	9 82 97
PCIE_TX8P	U27	97 9 PCIE_SLOTA_TO_NB_PF<8>	0.1UF	C8416	PCIE_SLOTA_TO_NB_P<8>	9 82 97
PCIE_TX8N	T27	97 9 PCIE_SLOTA_TO_NB_NF<8>	0.1UF	C8417	PCIE_SLOTA_TO_NB_N<8>	9 82 97
PCIE_TX9P	U26	97 9 PCIE_SLOTA_TO_NB_PF<9>	0.1UF	C8418	PCIE_SLOTA_TO_NB_P<9>	9 82 97
PCIE_TX9N	T26	97 9 PCIE_SLOTA_TO_NB_NF<9>	0.1UF	C8419	PCIE_SLOTA_TO_NB_N<9>	9 82 97
PCIE_TX10P	P25	97 9 PCIE_SLOTA_TO_NB_PF<10>	0.1UF	C8420	PCIE_SLOTA_TO_NB_P<10>	9 82 97
PCIE_TX10N	N25	97 9 PCIE_SLOTA_TO_NB_NF<10>	0.1UF	C8421	PCIE_SLOTA_TO_NB_N<10>	9 82 97
PCIE_TX11P	P27	97 9 PCIE_SLOTA_TO_NB_PF<11>	0.1UF	C8422	PCIE_SLOTA_TO_NB_P<11>	9 82 97
PCIE_TX11N	N27	97 9 PCIE_SLOTA_TO_NB_NF<11>	0.1UF	C8423	PCIE_SLOTA_TO_NB_N<11>	9 82 97
PCIE_TX12P	P26	97 9 PCIE_SLOTA_TO_NB_PF<12>	0.1UF	C8424	PCIE_SLOTA_TO_NB_P<12>	9 82 97
PCIE_TX12N	N26	97 9 PCIE_SLOTA_TO_NB_NF<12>	0.1UF	C8425	PCIE_SLOTA_TO_NB_N<12>	9 82 97
PCIE_TX13P	L25	97 9 PCIE_SLOTA_TO_NB_PF<13>	0.1UF	C8426	PCIE_SLOTA_TO_NB_P<13>	9 82 97
PCIE_TX13N	K25	97 9 PCIE_SLOTA_TO_NB_NF<13>	0.1UF	C8427	PCIE_SLOTA_TO_NB_N<13>	9 82 97
PCIE_TX14P	L27	97 9 PCIE_SLOTA_TO_NB_PF<14>	0.1UF	C8428	PCIE_SLOTA_TO_NB_P<14>	9 82 97
PCIE_TX14N	K27	97 9 PCIE_SLOTA_TO_NB_NF<14>	0.1UF	C8429	PCIE_SLOTA_TO_NB_N<14>	9 82 97
PCIE_TX15P	L26	97 9 PCIE_SLOTA_TO_NB_PF<15>	0.1UF	C8430	PCIE_SLOTA_TO_NB_P<15>	9 82 97
PCIE_TX15N	K26	97 9 PCIE_SLOTA_TO_NB_NF<15>	0.1UF	C8431	PCIE_SLOTA_TO_NB_N<15>	9 82 97

84 PP1V2_GPU_PCIE_VDDR
R8400 100 1% 1/16W MF-LF 402
PCIE_CALRN AB24
PCIE_CALRP AC23
R8401 150 1% 1/16W MF-LF 402

PCIE_CALI AB23 GPU_PCIE_CALI
PCIE_TEST AE25 GPU_PCIE_TEST
R8402 10K 5% 1/16W MF-LF 402
R8403 10K 1% 1/16W MF-LF 402

K28 L28 M24 M25 M26 M27 M28 N28 P28 R23 PCIE_VSS
AH29 AF28 AE28 AD28 AD27 AD26 AD24 AC28 AB28 AA28 PCIE_VSS
PCIE_VSS
R24 R25 R26 R27 R28 T24 T28 U28 V24 V25 V26 V27 V28 W24 W28 Y28 AA23 AA24 AA25 AA26 AA27

XW8405 SM
82 6 PCIE_SLOTA_PRSNT_L

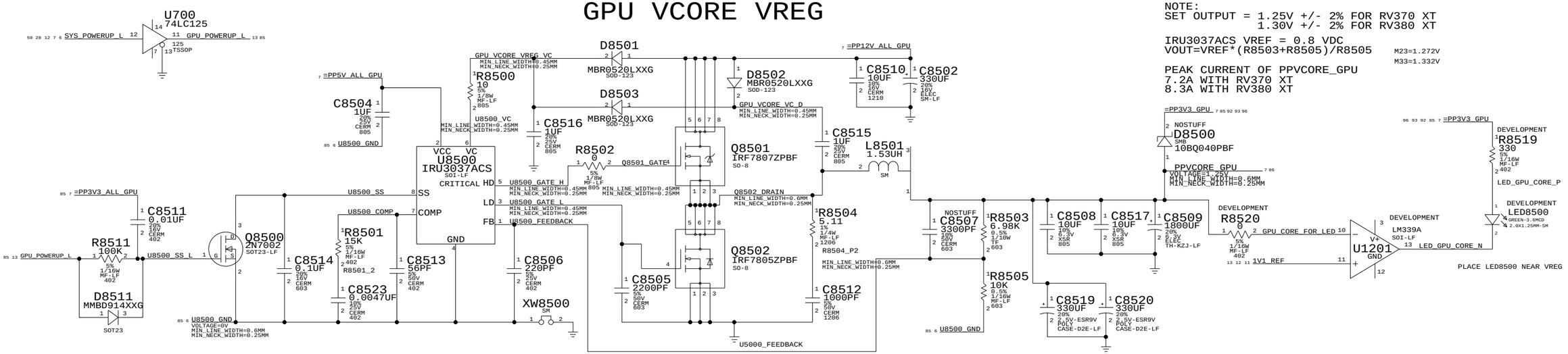
GPU PCIe

SYNC_MASTER=FINO-M23 SYNC_DATE=08/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT: 84 OF 154	

GPU VCORE VREG

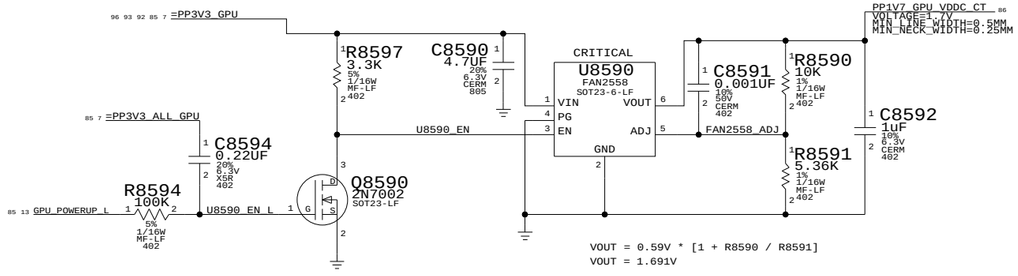


NOTE:
SET OUTPUT = 1.25V +/- 2% FOR RV370 XT
1.30V +/- 2% FOR RV380 XT

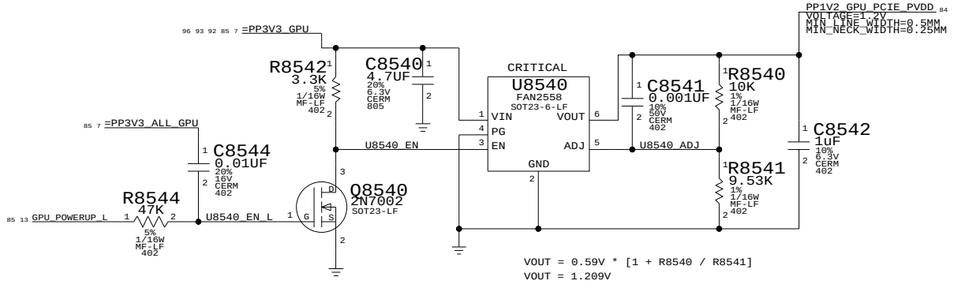
IRU3037ACS VREF = 0.8 VDC
VOUT=VREF*(R8503+R8505)/R8505 M23=1.272V M33=1.332V

PEAK CURRENT OF PPVCORE_GPU
7.2A WITH RV370 XT
8.3A WITH RV380 XT

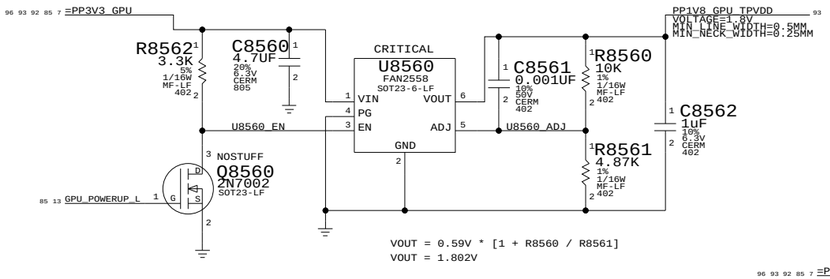
GPU 1.7V VDDC_CT



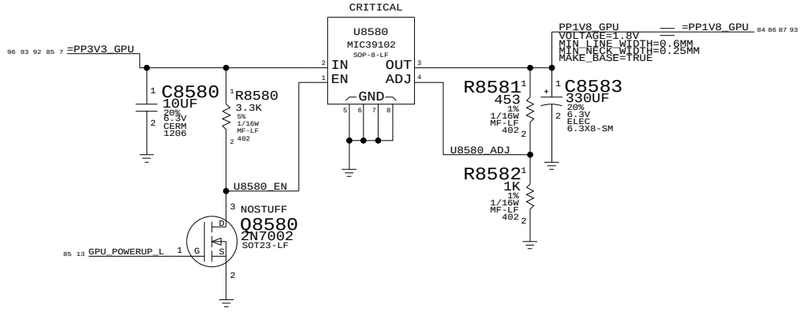
GPU 1.20V PCIE PVDD



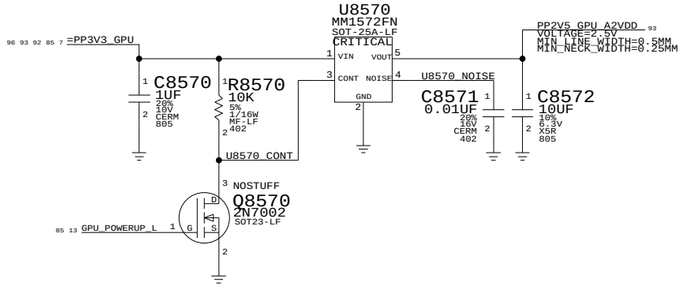
GPU 1.80V TPVDD



GPU 1.8V VREG



GPU 2.5V A2VDD



POWER SEQUENCING FOR RV370/80: =PP3V3_GPU > =PPV_GPU_MEM > VDDC_CT > PPVCORE_GPU
PP2V5_GPU_A2VDD > PP1V8_GPU > PCIE_PVDD

THE ENTIRE SEQUENCE SHOULD TAKE LESS THAN 40 MS (T1+T3 IN DATABOOK)
HOWEVER IDEALLY ALL POWER RAILS SHOULD RAMP TOGETHER
POWER DOWN SEQUENCE SHOULD BE IN REVERSE ORDER

Graphics Vregs

SYNC_MASTER=M33-DD SYNC_DATE=06/20/2005

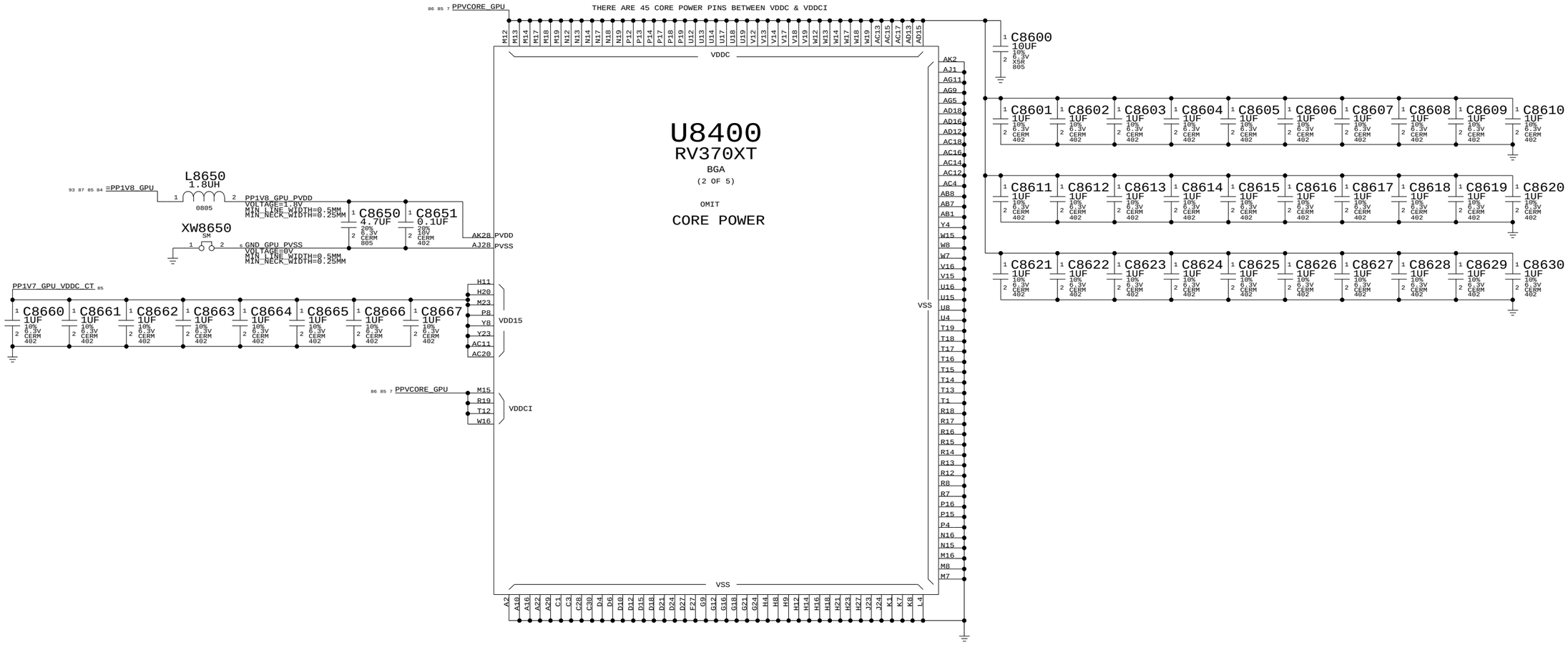
NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 85 OF 154	

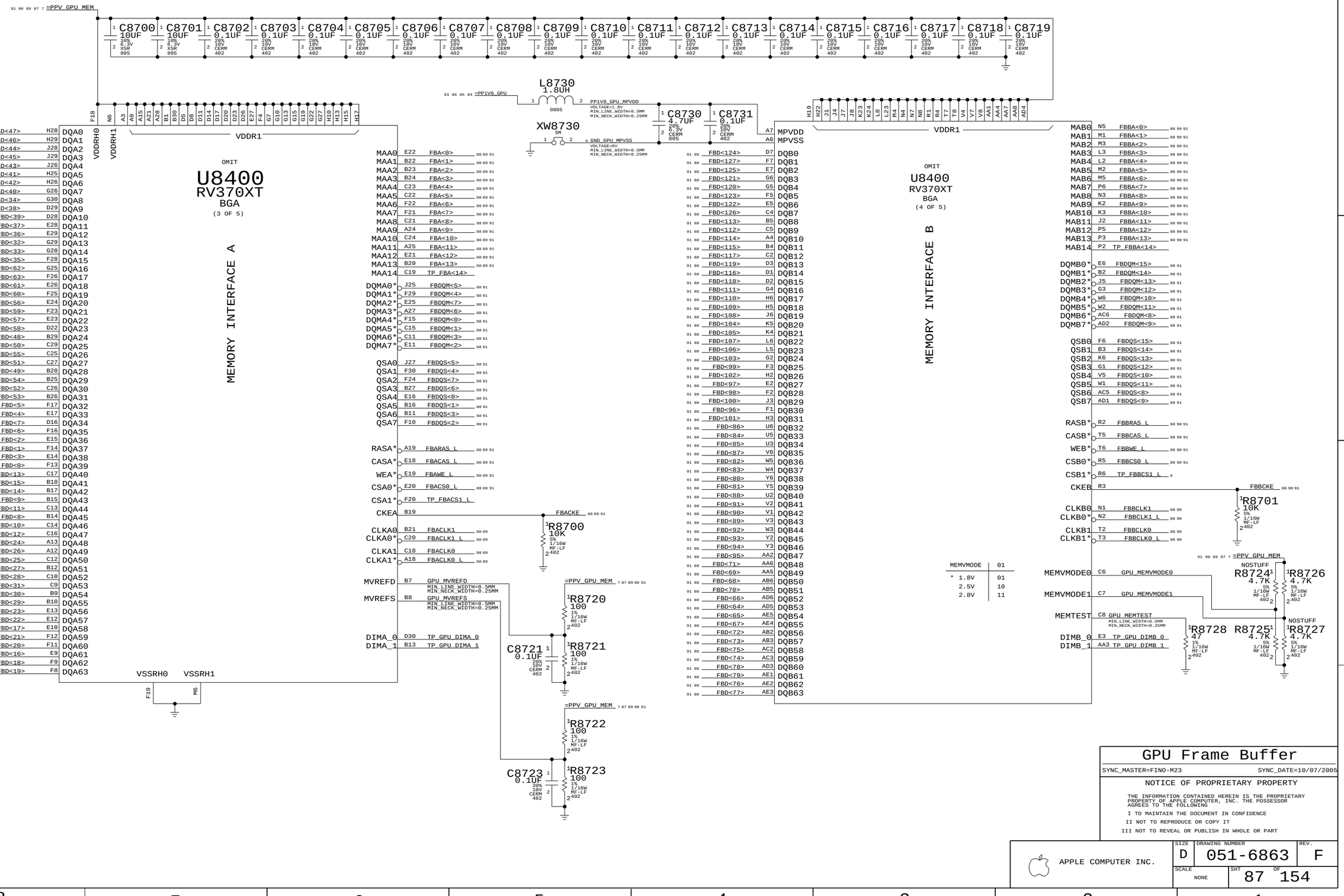


GPU Core Power

SYNC_MASTER=FINO-M23 SYNC_DATE=10/07/2005

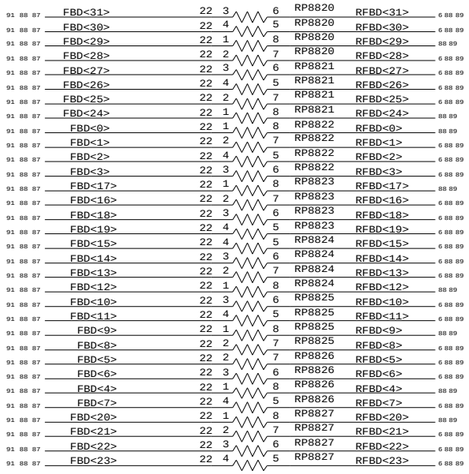
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 86 OF 154	


=PPV_GPU_MEM
C8700 10UF 10% 6.3V XSR 805
C8701 10UF 10% 6.3V XSR 805
C8702 0.1UF 20% 10V CERM 402
C8703 0.1UF 20% 10V CERM 402
C8704 0.1UF 20% 10V CERM 402
C8705 0.1UF 20% 10V CERM 402
C8706 0.1UF 20% 10V CERM 402
C8707 0.1UF 20% 10V CERM 402
C8708 0.1UF 20% 10V CERM 402
C8709 0.1UF 20% 10V CERM 402
C8710 0.1UF 20% 10V CERM 402
C8711 0.1UF 20% 10V CERM 402
C8712 0.1UF 20% 10V CERM 402
C8713 0.1UF 20% 10V CERM 402
C8714 0.1UF 20% 10V CERM 402
C8715 0.1UF 20% 10V CERM 402
C8716 0.1UF 20% 10V CERM 402
C8717 0.1UF 20% 10V CERM 402
C8718 0.1UF 20% 10V CERM 402
C8719 0.1UF 20% 10V CERM 402
L8730 1.8UH 0805
=PP1V8_GPU
PP1V8_GPU_MPVDD
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
C8730 4.7UF 20% 6.3V CERM 805
C8731 0.1UF 20% 10V CERM 402
XW8730 SM
GND_GPU_MPVSS
VOLTAGE=0V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VDDR1
OMIT
U8400
RV370XT
BGA
(3 OF 5)
MEMORY INTERFACE A
DQA0 DQA1 DQA2 DQA3 DQA4 DQA5 DQA6 DQA7 DQA8 DQA9 DQA10 DQA11 DQA12 DQA13 DQA14 DQA15 DQA16 DQA17 DQA18 DQA19 DQA20 DQA21 DQA22 DQA23 DQA24 DQA25 DQA26 DQA27 DQA28 DQA29 DQA30 DQA31 DQA32 DQA33 DQA34 DQA35 DQA36 DQA37 DQA38 DQA39 DQA40 DQA41 DQA42 DQA43 DQA44 DQA45 DQA46 DQA47 DQA48 DQA49 DQA50 DQA51 DQA52 DQA53 DQA54 DQA55 DQA56 DQA57 DQA58 DQA59 DQA60 DQA61 DQA62 DQA63
VDDRH0 VDDRH1
VSSRH0 VSSRH1
MAA0 MAA1 MAA2 MAA3 MAA4 MAA5 MAA6 MAA7 MAA8 MAA9 MAA10 MAA11 MAA12 MAA13 MAA14
DQMA0* DQMA1* DQMA2* DQMA3* DQMA4* DQMA5* DQMA6* DQMA7*
QSA0 QSA1 QSA2 QSA3 QSA4 QSA5 QSA6 QSA7
RASA* CASA* WEA* CSA0* CSA1*
CKEA
CLKA0 CLKA0* CLKA1 CLKA1*
MVREFD MVREFS
DIMA_0 DIMA_1
R8700 10K 5% 1/16W MF-LF 402
R8720 100 1% 1/16W MF-LF 402
R8721 100 1% 1/16W MF-LF 402
R8722 100 1% 1/16W MF-LF 402
R8723 100 1% 1/16W MF-LF 402
C8721 0.1UF 20% 10V CERM 402
C8723 0.1UF 20% 10V CERM 402
MPVDD MPVSS
DQB0 DQB1 DQB2 DQB3 DQB4 DQB5 DQB6 DQB7 DQB8 DQB9 DQB10 DQB11 DQB12 DQB13 DQB14 DQB15 DQB16 DQB17 DQB18 DQB19 DQB20 DQB21 DQB22 DQB23 DQB24 DQB25 DQB26 DQB27 DQB28 DQB29 DQB30 DQB31 DQB32 DQB33 DQB34 DQB35 DQB36 DQB37 DQB38 DQB39 DQB40 DQB41 DQB42 DQB43 DQB44 DQB45 DQB46 DQB47 DQB48 DQB49 DQB50 DQB51 DQB52 DQB53 DQB54 DQB55 DQB56 DQB57 DQB58 DQB59 DQB60 DQB61 DQB62 DQB63
VDDR1
OMIT
U8400
RV370XT
BGA
(4 OF 5)
MEMORY INTERFACE B
MAB0 MAB1 MAB2 MAB3 MAB4 MAB5 MAB6 MAB7 MAB8 MAB9 MAB10 MAB11 MAB12 MAB13 MAB14
DQMB0* DQMB1* DQMB2* DQMB3* DQMB4* DQMB5* DQMB6* DQMB7*
QSB0 QSB1 QSB2 QSB3 QSB4 QSB5 QSB6 QSB7
RASB* CASB* WEB* CSB0* CSB1*
CKEB
CLKB0 CLKB0* CLKB1 CLKB1*
R8701 10K 5% 1/16W MF-LF 402
MEMVMODE
* 1.8V 01
2.5V 10
2.8V 11
MEMVMODE0 MEMVMODE1 MEMTEST
DIMB_0 DIMB_1
R8728 47 1% 1/16W MF-LF 402
R8724 4.7K 5% 1/16W MF-LF 402
R8725 4.7K 5% 1/16W MF-LF 402
R8726 4.7K 5% 1/16W MF-LF 402
R8727 4.7K 5% 1/16W MF-LF 402
NOSTUFF
GPU Frame Buffer
SYNC_MASTER=FINO-M23
SYNC_DATE=10/07/2005
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-6863
REV. F
SCALE NONE
SHT 87 OF 154

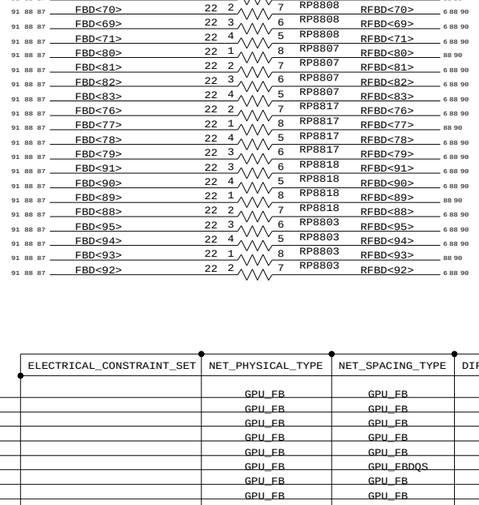
FRAME BUFFER A TERMINATION

PLACE R'S CLOSE TO MEMORY



PLACE CLOCK TERMINATION AFTER MEMORY
GPU -> MEMORY -> TERMINATION

FRAME BUFFER B TERMINATION



ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
FBD<127..0>	GPU_FB	GPU_FB		4425
RFBD<127..0>	GPU_FB	GPU_FB		4425
FBA<13..0>	GPU_FB	GPU_FB		4426
FBBA<13..0>	GPU_FB	GPU_FB		4427
FBDQM<15..0>	GPU_FB	GPU_FB		4428
FBDQS<15..0>	GPU_FB	GPU_FBDQS		4429
FBARAS_L	GPU_FB	GPU_FB		4430
FBACAS_L	GPU_FB	GPU_FB		4470
FBAWE_L	GPU_FB	GPU_FB		4471
FBACS0_L	GPU_FB	GPU_FB		4472
FBACKE	GPU_FB	GPU_FB		4473
FBBRAS_L	GPU_FB	GPU_FB		4474
FBBCAS_L	GPU_FB	GPU_FB		4475
FBBWE_L	GPU_FB	GPU_FB		4476
FBBCS0_L	GPU_FB	GPU_FB		4477
FBBCKE	GPU_FB	GPU_FB		4478

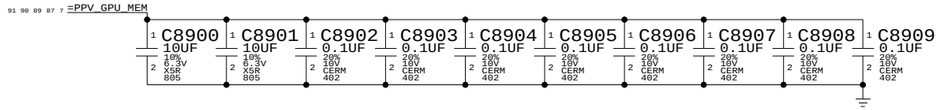
ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
FBACLK0	GPU_FBCLK	GPU_FBCLK	FBACLK0	4483
FBACLK0_L	GPU_FBCLK	GPU_FBCLK	FBACLK0	4484
FBACLK1	GPU_FBCLK	GPU_FBCLK	FBACLK1	4485
FBACLK1_L	GPU_FBCLK	GPU_FBCLK	FBACLK1	4486
FBBCLK0	GPU_FBCLK	GPU_FBCLK	FBBCLK0	4491
FBBCLK0_L	GPU_FBCLK	GPU_FBCLK	FBBCLK0	4487
FBBCLK1	GPU_FBCLK	GPU_FBCLK	FBBCLK1	4488
FBBCLK1_L	GPU_FBCLK	GPU_FBCLK	FBBCLK1	4492

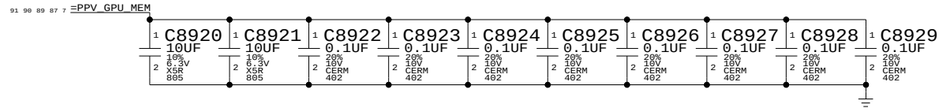
FB Series Termination

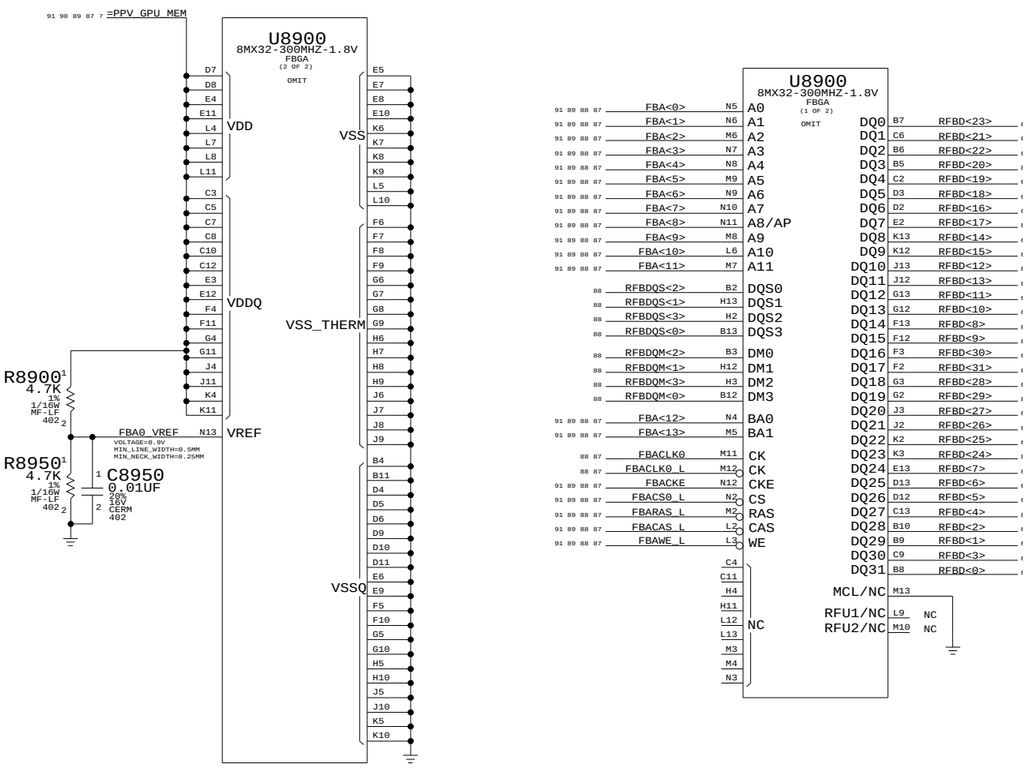
SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

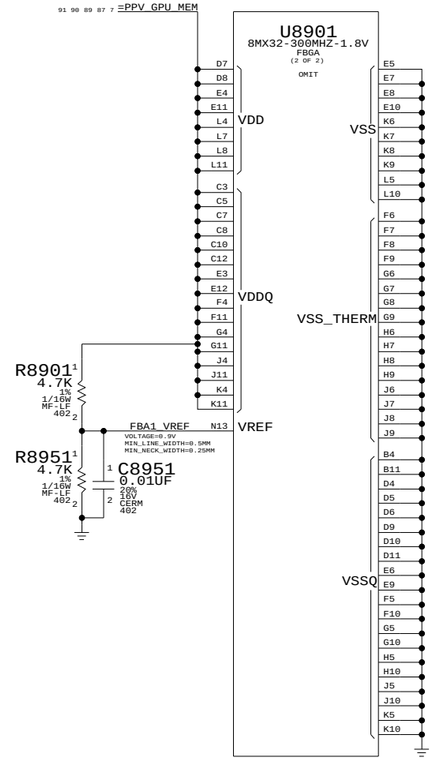
APPLE COMPUTER INC.

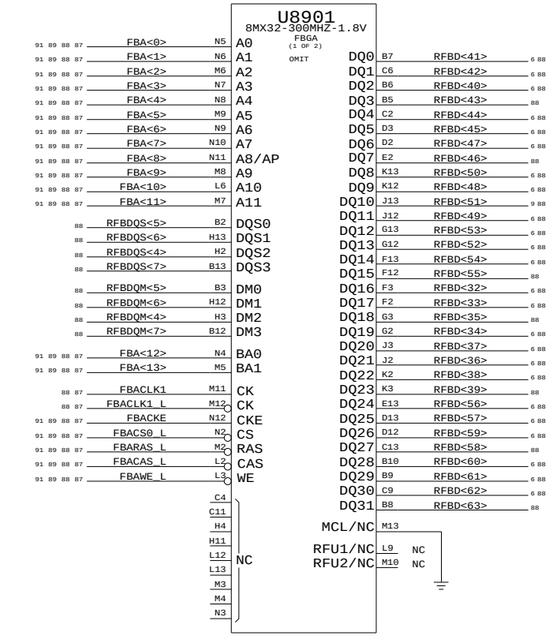
SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 88 OF 154	

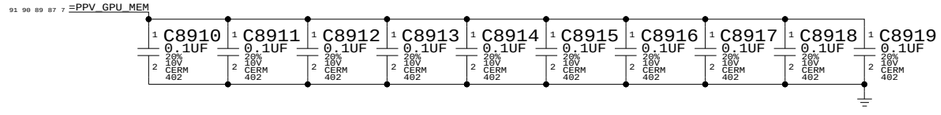


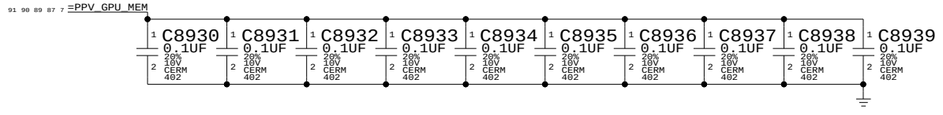




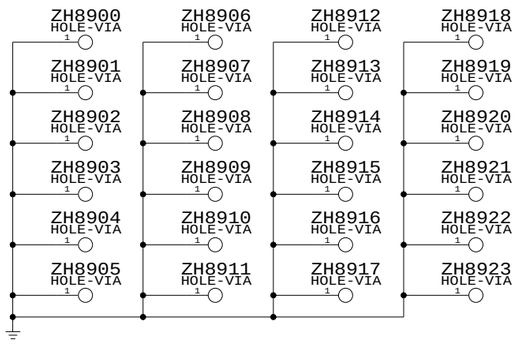








GROUND VIAS FOR SIGNAL LAYER TRANSITIONS



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
333S0319	2	SDRAM,4MX32,GDDR,300MHZ,1.8V,SAM	U8900,U8901	CRITICAL	FB64MB_300MHZ_SAM	SAMSUNG
333S0311	2	SDRAM,8MX32,GDDR,300MHZ,1.8V,SAM	U8900,U8901	CRITICAL	FB128MB_300MHZ_SAM	
333S0312	2	SDRAM,8MX32,GDDR,350MHZ,1.8V,SAM	U8900,U8901	CRITICAL	FB128MB_350MHZ_SAM	
333S0320	2	SDRAM,4MX32,GDDR,300MHZ,1.8V,HYN	U8900,U8901	CRITICAL	FB64MB_300MHZ_HYN	HYNIX
333S0314	2	SDRAM,8MX32,GDDR,300MHZ,1.8V,HYN	U8900,U8901	CRITICAL	FB128MB_300MHZ_HYN	
333S0315	2	SDRAM,8MX32,GDDR,350MHZ,1.8V,HYN	U8900,U8901	CRITICAL	FB128MB_350MHZ_HYN	

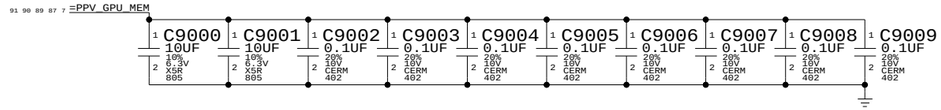
GPU GDDR SDRAM A

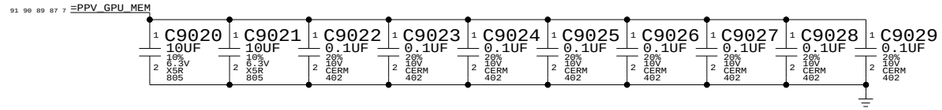
SYNC_MASTER=FINO-M23 SYNC_DATE=10/07/2005

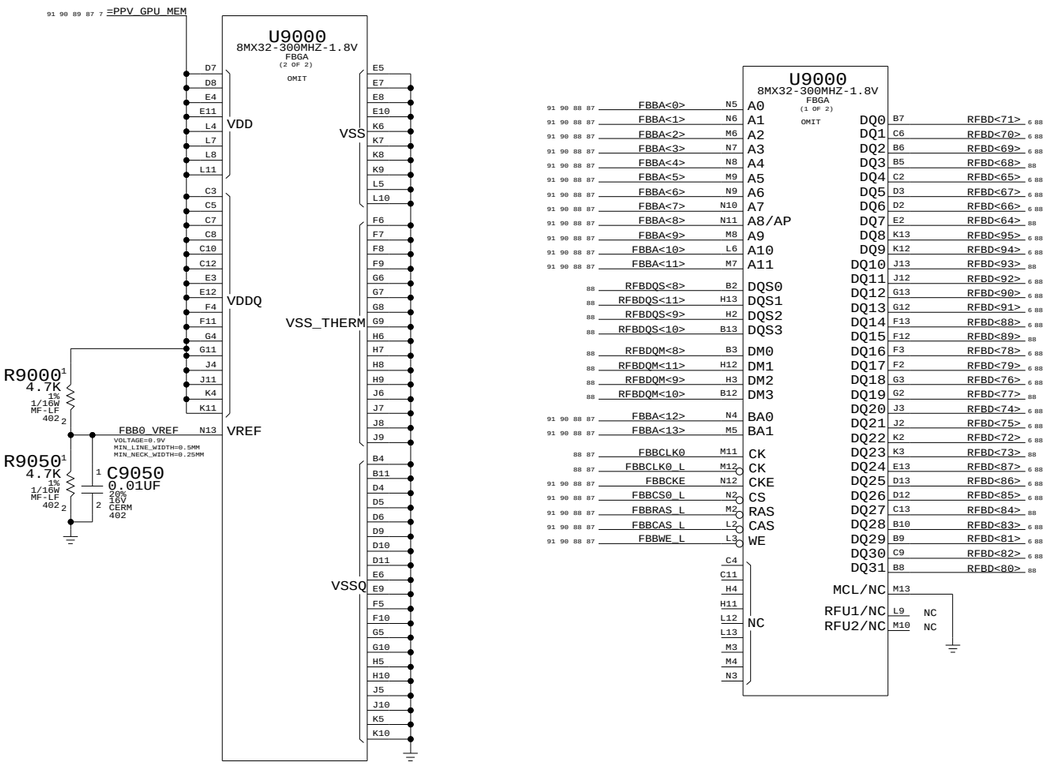
APPLE COMPUTER INC.

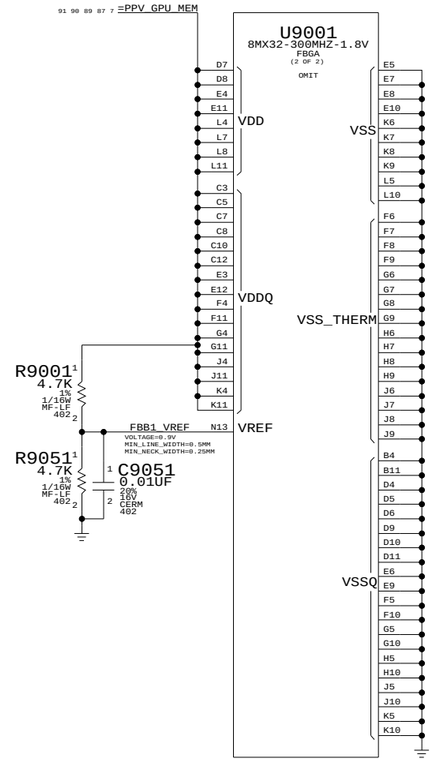
SIZE	DRAWING NUMBER	REV.
D	051-6863	F

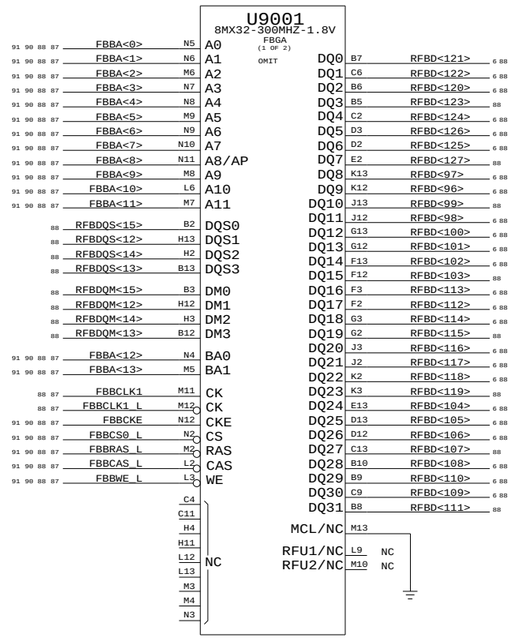
SCALE	SHT	OF
NONE	89	154

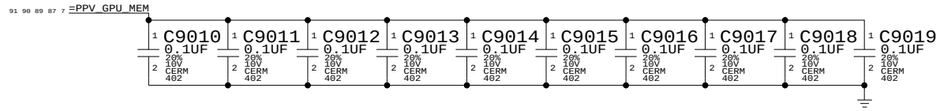


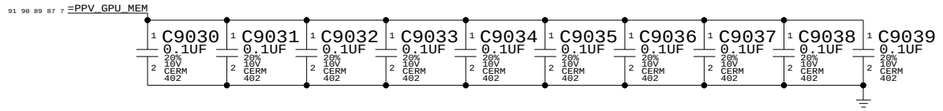


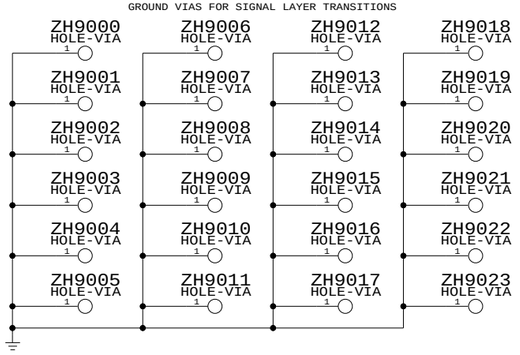












PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
333S0319	2	SDRAM,4MX32,GDDR,300MHZ,1.8V,SAM	U9000,U9001	CRITICAL	FB64MB_300MHZ_SAM	SAMSUNG
333S0311	2	SDRAM,8MX32,GDDR,300MHZ,1.8V,SAM	U9000,U9001	CRITICAL	FB128MB_300MHZ_SAM	
333S0312	2	SDRAM,8MX32,GDDR,350MHZ,1.8V,SAM	U9000,U9001	CRITICAL	FB128MB_350MHZ_SAM	
333S0320	2	SDRAM,4MX32,GDDR,300MHZ,1.8V,HYN	U9000,U9001	CRITICAL	FB64MB_300MHZ_HYN	HYNIX
333S0314	2	SDRAM,8MX32,GDDR,300MHZ,1.8V,HYN	U9000,U9001	CRITICAL	FB128MB_300MHZ_HYN	
333S0315	2	SDRAM,8MX32,GDDR,350MHZ,1.8V,HYN	U9000,U9001	CRITICAL	FB128MB_350MHZ_HYN	

GPU GDDR SDRAM B

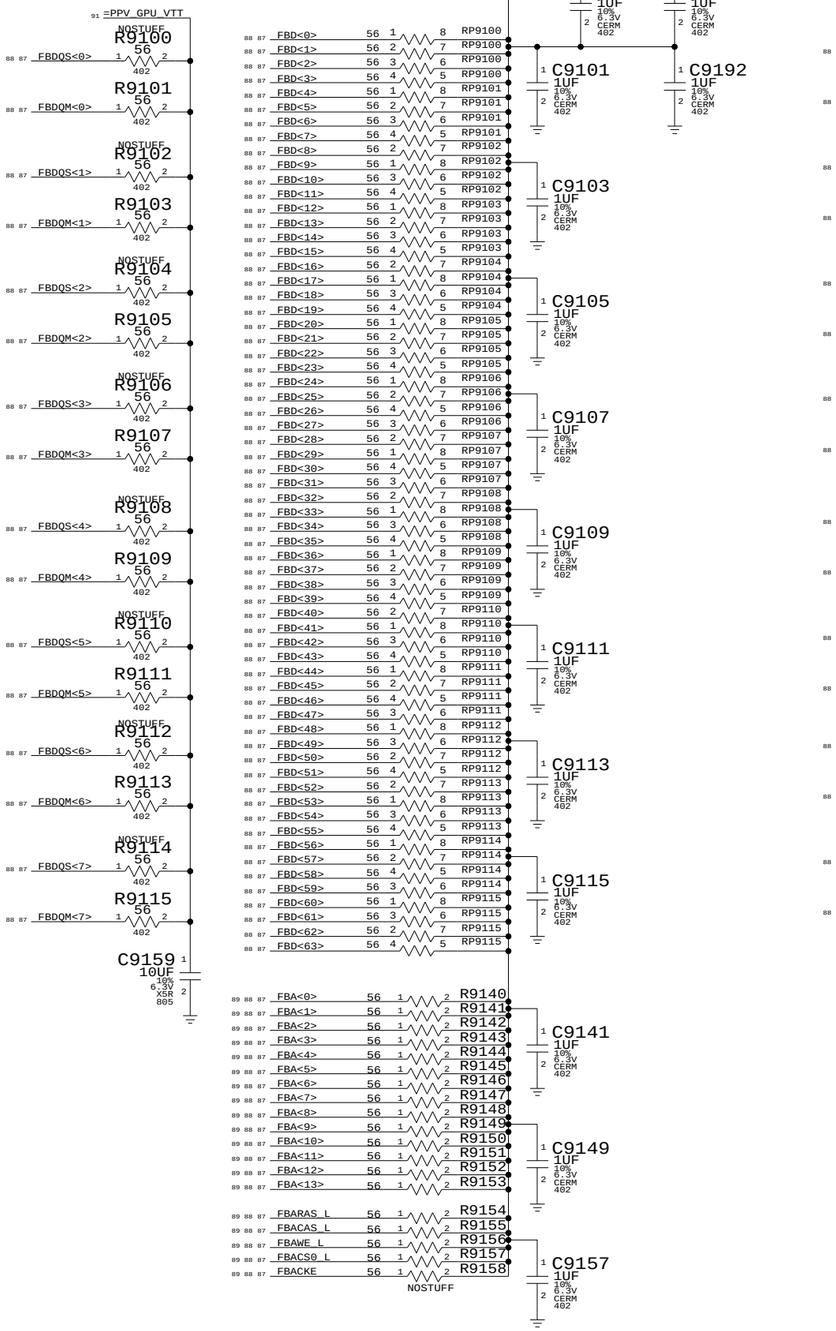
SYNC_MASTER=FINO-M23 SYNC_DATE=10/07/2005

APPLE COMPUTER INC.

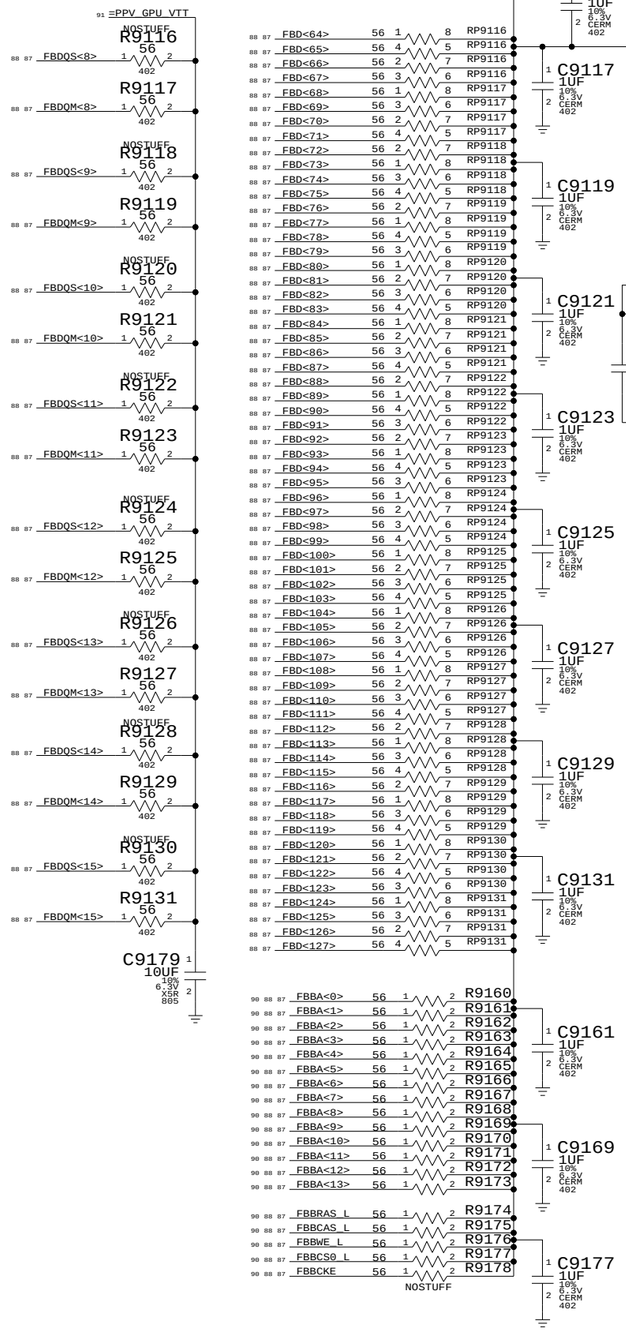
SIZE	DRAWING NUMBER	REV.
D	051-6863	F

SCALE	SHT	OF
NONE	90	154

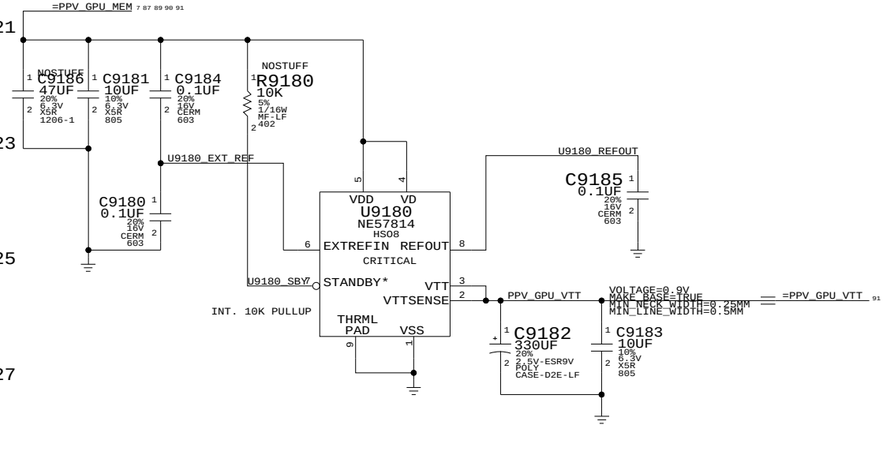
FRAME BUFFER A TERMINATION



FRAME BUFFER B TERMINATION



GPU VTT VREG



FB Parallel Termination

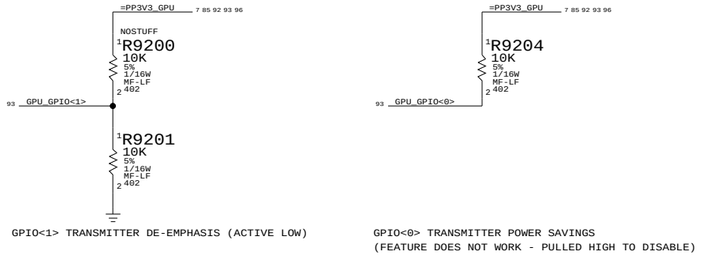
SYNC_MASTER=M33-DD SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F

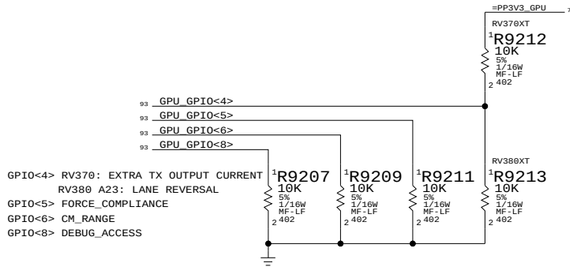
SCALE	SHT	OF
NONE	91	154

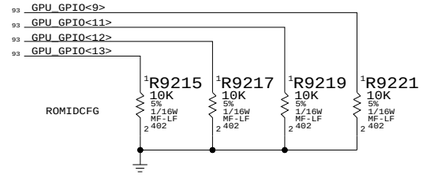
ATI STRAPS



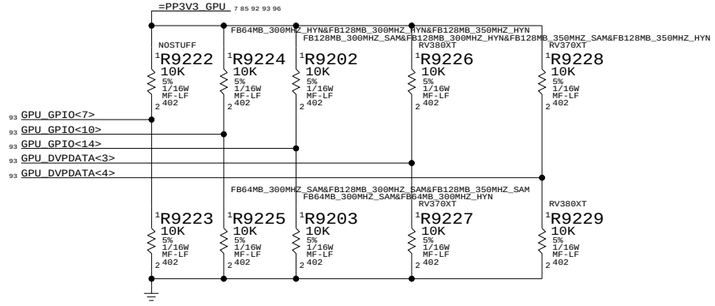
GPIO<1> TRANSMITTER DE-EMPHASIS (ACTIVE LOW)

GPIO<0> TRANSMITTER POWER SAVINGS
(FEATURE DOES NOT WORK - PULLED HIGH TO DISABLE)



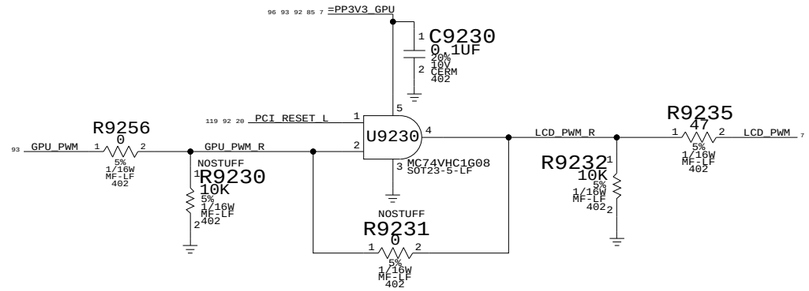


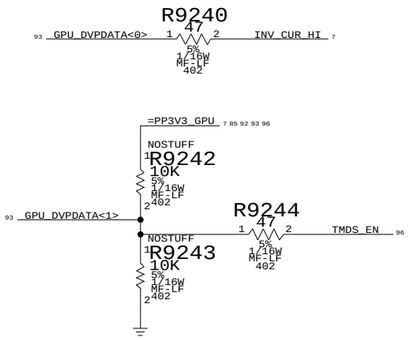
MEMORY STRAPS

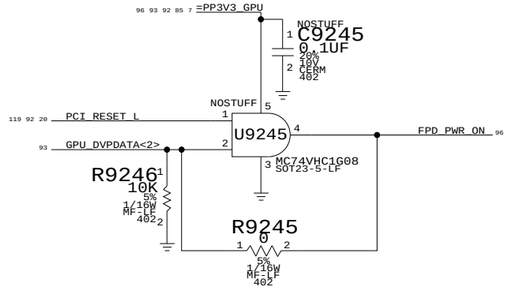


GPIO<7> - MEMORY DIE REVISION
  0 - ORIGINAL DIE REVISION
  1 - NEW (FUTURE) DIE REV
GPIO<10> - MEMORY VENDOR
  0 - SAMSUNG
  1 - HYNIX
GPIO<14> - MEMORY DENSITY
  0 - 4MX32
  1 - 8MX32
DVPDATA<3,4> - SPEED
  00 - 325E / 200M
  01 - 400E / 300M
  10 - 500E / 350M
  11 - RESERVED FOR FUTURE USE

APPLE GPIOS







GPU Straps

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 92 OF 154	

SPREAD SPECTRUM SUPPORT

S0=1;S1=M => -1.5% DOWN-SPREAD

27M OSC

(PLACE R9371 AND R9372 CLOSE TO OSCILLATOR PIN 8)

PLACE R9373 CLOSE TO ATI PIN AH28

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0176	1	OSC, 27MHZ, 30PPM	G9370	CRITICAL	

DIFFERENTIAL IMPEDANCE SHOULD BE 100 OHM

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
TMDS_TCKM	GPU_TMDS	GPU_TMDS	TMDS_CK
	GPU_TMDS	GPU_TMDS	TMDS_CK
TMDS0	GPU_TMDS	GPU_TMDS	TMDS_D0
	GPU_TMDS	GPU_TMDS	TMDS_D0
TMDS0	GPU_TMDS	GPU_TMDS	TMDS_D1
	GPU_TMDS	GPU_TMDS	TMDS_D1
TMDS0	GPU_TMDS	GPU_TMDS	TMDS_D2
	GPU_TMDS	GPU_TMDS	TMDS_D2
	GPU_VGA	GPU_VGA	
	GPU_VGA	GPU_VGA	
	GPU_VGA	GPU_VGA	
	GPU_VGA	GPU_VGA	
	GPU_VGA	GPU_VGA	
		I2C	
		I2C	
		I2C	
		I2C	

GPU THERMAL SENSOR

PLACE C9392 CLOSE TO TEMP SENSOR

PLACE R9321-3 & FL9600-2 NEAR MINI-VGA CONNECTOR
ROUTE GND IN BETWEEN RGB SIGNALS WITH A VIA EVERY INCH

GPU DVI & DACs

SYNC_MASTER=FINO-M23 SYNC_DATE=10/07/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 93 OF 154	

INTERNAL LCD

NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
GPU_TMDS	GPU_TMDS	TCK
GPU_TMDS	GPU_TMDS	TCK
GPU_TMDS	GPU_TMDS	TD0
GPU_TMDS	GPU_TMDS	TD0
GPU_TMDS	GPU_TMDS	TD1
GPU_TMDS	GPU_TMDS	TD1
GPU_TMDS	GPU_TMDS	TD2
GPU_TMDS	GPU_TMDS	TD2

TCKP, TCKM, TD0P, TD0M, TD1P, TD1M, TD2P, TD2M

PLACE R9600-R9604, C9600 AS CLOSE TO GPU AS POSSIBLE

PLACE FILTER CLOSE TO TMDS CONNECTOR

TMDS_D2M, TMDS_D2P, TMDS_D1M, TMDS_D1P, TMDS_D0M, TMDS_D0P, TMDS_CKM, TMDS_CKP

R9626 0 NOSTUFF; R9604 130 1% 1/16W MF-LF 402; L9602 90-OHM SYM_VER-1 SM; R9627 0 NOSTUFF; R9628 0 NOSTUFF; R9603 130 1% 1/16W MF-LF 402; L9608 90-OHM SYM_VER-1 SM; R9629 0 NOSTUFF; R9630 0 NOSTUFF; R9602 130 1% 1/16W MF-LF 402; L9609 90-OHM SYM_VER-1 SM; R9631 0 NOSTUFF; R9632 0 NOSTUFF; R9601 165 1% 1/16W MF-LF 402; L9610 90-OHM SYM_VER-1 SM; R9633 0 NOSTUFF

TMDS_CK_TERM
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.2MM

C9600 22PF 5% 50V CERM 402; R9600 165 1% 1/16W MF-LF 402

TD1M, TD1P, TD0M, TD0P, TCKM, TCKP

=PP3V3_GPU

R9605 2.0K 5% 1/16W MF-LF 402; R9607 2.0K 5% 1/16W MF-LF 402; R9682 0 5% 1/8W MF-LF 805; C9601 0.01UF 10% 16V CERM 402

I2C_GPU_TMDS_SCL → R9608 33 5% 1/16W MF-LF 402 → I2C_TMDS_SCL

I2C_GPU_TMDS_SDA → R9606 33 5% 1/16W MF-LF 402 → I2C_TMDS_SDA

INTERNAL TMDS CONNECTOR

SDF9600
STDOFF-3MMOD4.6MMH-1.35-TH
(516S0241)
J9602
53307-3072
F-ST-SM
CRITICAL

TD0M, TD0P, TD2M, TD2P, I2C_TMDS_SDA

PPVCC_TMDS
PP3V3_DDC
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM

TCKM, TCKP, TD1M, TD1P, I2C_TMDS_SCL

C9616 10UF 10% 16V CERM 1210; C9615 0.01UF 10% 16V CERM 402

GND_CHASSIS_TMDS

SDF9601
STDOFF-3MMOD4.6MMH-1.35-TH

PANEL POWER SEQUENCING

=PP12V_GPU

Q9600 IRF7416BF SOI NOSTUFF
S3 S2 S1 GATE D4 D3 D2 D1
376S0385

R9634 0 5% 1/4W MF-LF 1206

C9619 0.01UF 20% 16V CERM 402 NOSTUFF
R9625 100K 5% 1/16W MF-LF 402 NOSTUFF
C9618 0.022UF 20% 16V CERM 402 NOSTUFF

FPD_PWR_SW_G

D9614 MMBD914XXG SOT23

C9617 10UF 10% 16V CERM 1210

R9660 10K 5% 1/16W MF-LF 402 NOSTUFF

PPVCC_TMDS
VOLTAGE=12V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM

R9613 100K 5% 1/16W MF-LF 402

FPD_PWR_ON_D

Q9601 2N7002 SOT23-LF NOSTUFF

FPD_PWR_ON

TMDS_EN_R

R9614 10K 5% 1/16W MF-LF 402

TMDS_EN

DZ9600 MMBZ5227B SOT23

U9670 74LC125 TSSOP

FPD_PWR_ON → LED5900_PWR

R9612 820 5% 1/10W MF-LF 603

LED9600 GREEN-3.6MCD 2.0X1.25MM-SM

LED5900_P1

SILKSCREEN: 3

=PP12V_GPU

R9690 300 5% 1/8W MF-LF 805; R9691 300 5% 1/8W MF-LF 805

Q9690_D

Q9690 2N7002 SOT23-LF

SYS_POWERUP_L_BUF

FOR PANEL VCC FALL TIME SPEC

EXTERNAL VGA CONNECTOR

NET_PHYSICAL_TYPE	NET_SPACING_TYPE
GPU_VGA	GPU_VGA
GPU_VGA	GPU_VGA
GPU_VGA	GPU_VGA
GPU_VGA	GPU_VGA
GPU_VGA	GPU_VGA
GPU_VGA	GPU_VGA
GPU_VGA	GPU_VGA
GPU_VGA	GPU_VGA
GPU_VGA	GPU_VGA
GPU_VGA	GPU_VGA
GPU_VGA	GPU_VGA
GPU_VGA	GPU_VGA

FILT_ANALOG_GRN, ANALOG_GRN_LC, ANALOG_GRN_LCL, FILT_ANALOG_RED, ANALOG_RED_LC, ANALOG_RED_LCL, FILT_ANALOG_BLU, ANALOG_BLU_LC, ANALOG_BLU_LCL, VGA_VSYNC, VGA_VSYNC_R, VGA_HSYNC, VGA_HSYNC_R

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
152S0316	3	INDUCTOR, 47NH, 0.20 OHM	FL9600,FL9601,FL9602	

PP5V_USB2 → R9680 0 5% 1/8W MF-LF 805 → PP5V_VGA
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM

C9602 0.01UF 10% 16V CERM 402

GND_CHASSIS_VGA

=PP3V3_GPU

U9670 74LC125 TSSOP CRITICAL

ANALOG_VSYNC → R9671 33 5% 1/16W MF-LF 402 → VGA_VSYNC_R

C9670 0.1UF 20% 10V CERM 402

ANALOG_HSYNC → R9672 33 5% 1/16W MF-LF 402 → VGA_HSYNC_R

C9607 22PF 5% 50V CERM 402 NOSTUFF; C9608 22PF 5% 50V CERM 402 NOSTUFF

GND_CHASSIS_VGA

=PP3V3_GPU

R9673 10K 5% 1/16W MF-LF 402; R9674 10K 5% 1/16W MF-LF 402

Q9675 2N7002DW-X-F SOT-363

I2C_GPU_MON_SCL → R9675 100 5% 1/16W MF-LF 402 → I2C_MON_SCL_R

I2C_GPU_MON_SDA → R9676 100 5% 1/16W MF-LF 402 → I2C_MON_SDA_R

PP5V_VGA

R9677 4.7K 5% 1/16W MF-LF 402; R9678 4.7K 5% 1/16W MF-LF 402

C9677 47PF 5% 50V CERM 402; C9678 47PF 5% 50V CERM 402

GND_CHASSIS_VGA

INDUCTORS SHOULD BE 47 NH
ANY ~8PF CAP SHOULD DO

L9640 0 5% 1/8W MF-LF 805; L9641 47NH-0.20-OHM 0805; L9642 0 5% 1/8W MF-LF 805; L9643 47NH-0.20-OHM 0805; L9644 0 5% 1/8W MF-LF 805; L9645 47NH-0.20-OHM 0805

OMIT FL9600 LCFILTER SM-220MHZ-LF
OMIT FL9601 LCFILTER SM-220MHZ-LF
OMIT FL9602 LCFILTER SM-220MHZ-LF

ANALOG_RED → ANALOG_RED_LC → ANALOG_RED_LCL
ANALOG_GRN → ANALOG_GRN_LC → ANALOG_GRN_LCL
ANALOG_BLU → ANALOG_BLU_LC → ANALOG_BLU_LCL

C9640 75 1% 1/16W MF-LF 402; C9643 75 1% 1/16W MF-LF 402; C9644 75 1% 1/16W MF-LF 402

R9643 8.2PF +/-0.25PF 50V CERM 402; R9644 8.2PF +/-0.25PF 50V CERM 402; R9645 8.2PF +/-0.25PF 50V CERM 402

R9640 0 NOSTUFF; R9641 0 NOSTUFF; R9642 0 NOSTUFF

PLACE R9321-3 & FL9600-2 CLOSE TO J9603

M33: 514S0097

CRITICAL
J9603
DV01793-M33-4F
F-ST-SM

GND_CHASSIS_RIGHT

VGA_HSYNC_R, FILT_ANALOG_RED, FILT_ANALOG_GRN, FILT_ANALOG_BLU, I2C_MON_SCL_R, MON_DETECT

VGA_VSYNC_R, (RED_RTN), (GRN_RTN), PP5V_VGA, I2C_MON_SDA_R, (BLU_RTN)

C9605 0.01UF 10% 16V CERM 402; C9604 0.01UF 10% 16V CERM 402; C9603 0.01UF 10% 16V CERM 402

GND_CHASSIS_VGA

TMDS / ExtVGA

SYNC_MASTER=M33-DD SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6863 | REV. F

SCALE NONE | SHT 96 OF 154

KODIAK PCI-E PHYSICAL CONSTRAINT TABLE

SIG_NAME	ELECTRICAL_CONSTRAINT_SET	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE	NET_SPACING_TYPE
100M_N<0>		CLK_100M	PCIE_CLK	PCIE_CLK
100M_P<0>		CLK_100M	PCIE_CLK	PCIE_CLK
CLK_KOD_100M_N<0>		CLK_KODPCIE_100M	PCIE_CLK	PCIE_CLK
CLK_KOD_100M_P<0>		CLK_KODPCIE_100M	PCIE_CLK	PCIE_CLK
CLK_KOD_100M_NF<0>		CLK_KODPCIE_100MF	PCIE_CLK	PCIE_CLK
CLK_KOD_100M_PF<0>		CLK_KODPCIE_100MF	PCIE_CLK	PCIE_CLK
PCIE_NB_TO_SLOTA_NF<0>	PCIE_NB2SA0	PCIE_NB_TO_SLOTA_0_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<0>	PCIE_NB2SA0	PCIE_NB_TO_SLOTA_0_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<1>	PCIE_NB2SA1	PCIE_NB_TO_SLOTA_1_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<1>	PCIE_NB2SA1	PCIE_NB_TO_SLOTA_1_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<2>	PCIE_NB2SA2	PCIE_NB_TO_SLOTA_2_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<2>	PCIE_NB2SA2	PCIE_NB_TO_SLOTA_2_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<3>	PCIE_NB2SA3	PCIE_NB_TO_SLOTA_3_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<3>	PCIE_NB2SA3	PCIE_NB_TO_SLOTA_3_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<4>	PCIE_NB2SA4	PCIE_NB_TO_SLOTA_4_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<4>	PCIE_NB2SA4	PCIE_NB_TO_SLOTA_4_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<5>	PCIE_NB2SA5	PCIE_NB_TO_SLOTA_5_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<5>	PCIE_NB2SA5	PCIE_NB_TO_SLOTA_5_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<6>	PCIE_NB2SA6	PCIE_NB_TO_SLOTA_6_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<6>	PCIE_NB2SA6	PCIE_NB_TO_SLOTA_6_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<7>	PCIE_NB2SA7	PCIE_NB_TO_SLOTA_7_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<7>	PCIE_NB2SA7	PCIE_NB_TO_SLOTA_7_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<8>	PCIE_NB2SA8	PCIE_NB_TO_SLOTA_8_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<8>	PCIE_NB2SA8	PCIE_NB_TO_SLOTA_8_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<9>	PCIE_NB2SA9	PCIE_NB_TO_SLOTA_9_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<9>	PCIE_NB2SA9	PCIE_NB_TO_SLOTA_9_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<10>	PCIE_NB2SA10	PCIE_NB_TO_SLOTA_10_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<10>	PCIE_NB2SA10	PCIE_NB_TO_SLOTA_10_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<11>	PCIE_NB2SA11	PCIE_NB_TO_SLOTA_11_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<11>	PCIE_NB2SA11	PCIE_NB_TO_SLOTA_11_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<12>	PCIE_NB2SA12	PCIE_NB_TO_SLOTA_12_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<12>	PCIE_NB2SA12	PCIE_NB_TO_SLOTA_12_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<13>	PCIE_NB2SA13	PCIE_NB_TO_SLOTA_13_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<13>	PCIE_NB2SA13	PCIE_NB_TO_SLOTA_13_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<14>	PCIE_NB2SA14	PCIE_NB_TO_SLOTA_14_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<14>	PCIE_NB2SA14	PCIE_NB_TO_SLOTA_14_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<15>	PCIE_NB2SA15	PCIE_NB_TO_SLOTA_15_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<15>	PCIE_NB2SA15	PCIE_NB_TO_SLOTA_15_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<0>		PCIE_NB_TO_SLOTA_0	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<0>		PCIE_NB_TO_SLOTA_0	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<1>		PCIE_NB_TO_SLOTA_1	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<1>		PCIE_NB_TO_SLOTA_1	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<2>		PCIE_NB_TO_SLOTA_2	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<2>		PCIE_NB_TO_SLOTA_2	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<3>		PCIE_NB_TO_SLOTA_3	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<3>		PCIE_NB_TO_SLOTA_3	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<4>		PCIE_NB_TO_SLOTA_4	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<4>		PCIE_NB_TO_SLOTA_4	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<5>		PCIE_NB_TO_SLOTA_5	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<5>		PCIE_NB_TO_SLOTA_5	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<6>		PCIE_NB_TO_SLOTA_6	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<6>		PCIE_NB_TO_SLOTA_6	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<7>		PCIE_NB_TO_SLOTA_7	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<7>		PCIE_NB_TO_SLOTA_7	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<8>		PCIE_NB_TO_SLOTA_8	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<8>		PCIE_NB_TO_SLOTA_8	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<9>		PCIE_NB_TO_SLOTA_9	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<9>		PCIE_NB_TO_SLOTA_9	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<10>		PCIE_NB_TO_SLOTA_10	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<10>		PCIE_NB_TO_SLOTA_10	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<11>		PCIE_NB_TO_SLOTA_11	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<11>		PCIE_NB_TO_SLOTA_11	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<12>		PCIE_NB_TO_SLOTA_12	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<12>		PCIE_NB_TO_SLOTA_12	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<13>		PCIE_NB_TO_SLOTA_13	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<13>		PCIE_NB_TO_SLOTA_13	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<14>		PCIE_NB_TO_SLOTA_14	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<14>		PCIE_NB_TO_SLOTA_14	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<15>		PCIE_NB_TO_SLOTA_15	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<15>		PCIE_NB_TO_SLOTA_15	PCIE_DATA	PCIE_DATA

SIG_NAME	ELECTRICAL_CONSTRAINT_SET	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE	NET_SPACING_TYPE
CLK_PCIE_SLOTA_N<0>		KODPCIE_CLK	PCIE_CLK	PCIE_CLK
CLK_PCIE_SLOTA_P<0>		KODPCIE_CLK	PCIE_CLK	PCIE_CLK
CLK_PCIE_SLOTA_NF<0>		KODPCIE_CLKF	PCIE_CLK	PCIE_CLK
CLK_PCIE_SLOTA_PF<0>		KODPCIE_CLKF	PCIE_CLK	PCIE_CLK
CKA_P<0>		CLK_SLOTA_CKA	PCIE_CLK	PCIE_CLK
CKA_N<0>		CLK_SLOTA_CKA	PCIE_CLK	PCIE_CLK
PCIE_SLOTA_TO_NB_NF<0>	PCIE_SA2NB0	PCIE_SLOTA_TO_NB_0_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<0>	PCIE_SA2NB0	PCIE_SLOTA_TO_NB_0_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<1>	PCIE_SA2NB1	PCIE_SLOTA_TO_NB_1_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<1>	PCIE_SA2NB1	PCIE_SLOTA_TO_NB_1_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<2>	PCIE_SA2NB2	PCIE_SLOTA_TO_NB_2_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<2>	PCIE_SA2NB2	PCIE_SLOTA_TO_NB_2_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<3>	PCIE_SA2NB3	PCIE_SLOTA_TO_NB_3_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<3>	PCIE_SA2NB3	PCIE_SLOTA_TO_NB_3_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<4>	PCIE_SA2NB4	PCIE_SLOTA_TO_NB_4_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<4>	PCIE_SA2NB4	PCIE_SLOTA_TO_NB_4_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<5>	PCIE_SA2NB5	PCIE_SLOTA_TO_NB_5_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<5>	PCIE_SA2NB5	PCIE_SLOTA_TO_NB_5_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<6>	PCIE_SA2NB6	PCIE_SLOTA_TO_NB_6_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<6>	PCIE_SA2NB6	PCIE_SLOTA_TO_NB_6_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<7>	PCIE_SA2NB7	PCIE_SLOTA_TO_NB_7_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<7>	PCIE_SA2NB7	PCIE_SLOTA_TO_NB_7_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<8>	PCIE_SA2NB8	PCIE_SLOTA_TO_NB_8_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<8>	PCIE_SA2NB8	PCIE_SLOTA_TO_NB_8_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<9>	PCIE_SA2NB9	PCIE_SLOTA_TO_NB_9_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<9>	PCIE_SA2NB9	PCIE_SLOTA_TO_NB_9_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<10>	PCIE_SA2NB10	PCIE_SLOTA_TO_NB_10_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<10>	PCIE_SA2NB10	PCIE_SLOTA_TO_NB_10_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<11>	PCIE_SA2NB11	PCIE_SLOTA_TO_NB_11_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<11>	PCIE_SA2NB11	PCIE_SLOTA_TO_NB_11_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<12>	PCIE_SA2NB12	PCIE_SLOTA_TO_NB_12_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<12>	PCIE_SA2NB12	PCIE_SLOTA_TO_NB_12_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<13>	PCIE_SA2NB13	PCIE_SLOTA_TO_NB_13_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<13>	PCIE_SA2NB13	PCIE_SLOTA_TO_NB_13_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<14>	PCIE_SA2NB14	PCIE_SLOTA_TO_NB_14_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<14>	PCIE_SA2NB14	PCIE_SLOTA_TO_NB_14_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<15>	PCIE_SA2NB15	PCIE_SLOTA_TO_NB_15_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<15>	PCIE_SA2NB15	PCIE_SLOTA_TO_NB_15_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<0>		PCIE_SLOTA_TO_NB_0	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<0>		PCIE_SLOTA_TO_NB_0	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<1>		PCIE_SLOTA_TO_NB_1	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<1>		PCIE_SLOTA_TO_NB_1	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<2>		PCIE_SLOTA_TO_NB_2	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<2>		PCIE_SLOTA_TO_NB_2	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<3>		PCIE_SLOTA_TO_NB_3	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<3>		PCIE_SLOTA_TO_NB_3	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<4>		PCIE_SLOTA_TO_NB_4	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<4>		PCIE_SLOTA_TO_NB_4	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<5>		PCIE_SLOTA_TO_NB_5	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<5>		PCIE_SLOTA_TO_NB_5	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<6>		PCIE_SLOTA_TO_NB_6	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<6>		PCIE_SLOTA_TO_NB_6	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<7>		PCIE_SLOTA_TO_NB_7	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<7>		PCIE_SLOTA_TO_NB_7	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<8>		PCIE_SLOTA_TO_NB_8	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<8>		PCIE_SLOTA_TO_NB_8	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<9>		PCIE_SLOTA_TO_NB_9	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<9>		PCIE_SLOTA_TO_NB_9	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<10>		PCIE_SLOTA_TO_NB_10	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<10>		PCIE_SLOTA_TO_NB_10	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<11>		PCIE_SLOTA_TO_NB_11	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<11>		PCIE_SLOTA_TO_NB_11	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<12>		PCIE_SLOTA_TO_NB_12	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<12>		PCIE_SLOTA_TO_NB_12	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<13>		PCIE_SLOTA_TO_NB_13	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<13>		PCIE_SLOTA_TO_NB_13	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<14>		PCIE_SLOTA_TO_NB_14	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<14>		PCIE_SLOTA_TO_NB_14	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<15>		PCIE_SLOTA_TO_NB_15	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<15>		PCIE_SLOTA_TO_NB_15	PCIE_DATA	PCIE_DATA

KODIAK PCI-E POWER PHYSICAL CONSTRAINT TABLE

SIG_NAME	MIN_LINE_WIDTH	MIN_NECK_WIDTH	VOLTAGE
KOD_G10_GND	0.3MM	0.25MM	0
KOD_H05_GND	0.3MM	0.25MM	0
KOD_H08_GND	0.3MM	0.25MM	0
KOD_J13_GND	0.3MM	0.25MM	0
KOD_K07_GND	0.3MM	0.25MM	0
KOD_L13_GND	0.3MM	0.25MM	0
PWR_PCIE_A_AVDD	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_2	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_1	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_0	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_A	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_B	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_C	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_2	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_0	0.3MM	0.25MM	1.2

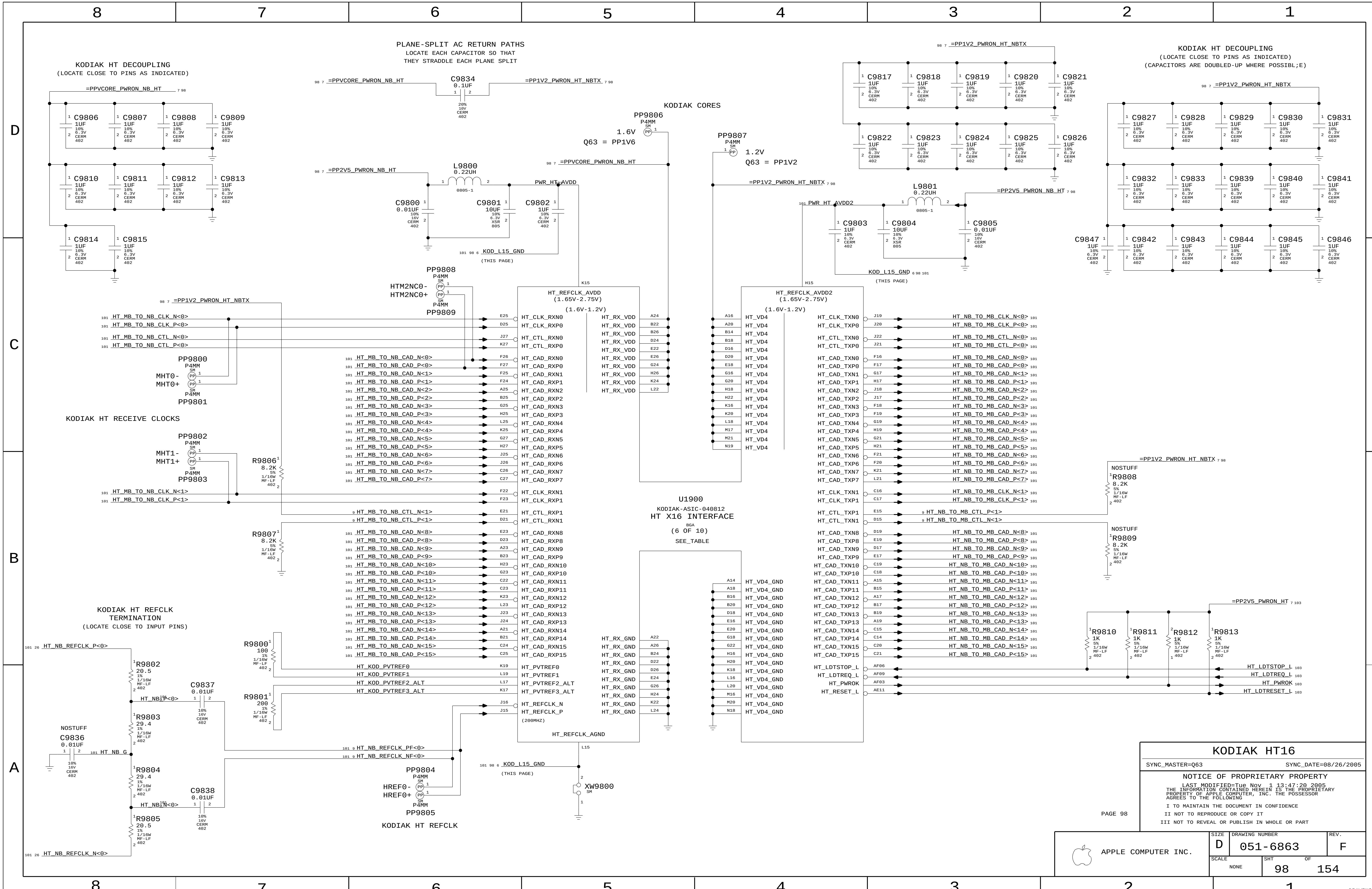
KODIAK PCI-E CONST

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F

SCALE	SHT	OF
NONE	97	154


PLANE-SPLIT AC RETURN PATHS
LOCATE EACH CAPACITOR SO THAT
THEY STRADDLE EACH PLANE SPLIT
KODIAK HT DECOUPLING
(LOCATE CLOSE TO PINS AS INDICATED)
KODIAK HT DECOUPLING
(LOCATE CLOSE TO PINS AS INDICATED)
(CAPACITORS ARE DOUBLED-UP WHERE POSSIBL;E)
KODIAK CORES
1.6V
Q63 = PP1V6
1.2V
Q63 = PP1V2
KODIAK HT RECEIVE CLOCKS
KODIAK HT REFCLK
TERMINATION
(LOCATE CLOSE TO INPUT PINS)
KODIAK HT REFCLK
U1900
KODIAK-ASIC-040812
HT X16 INTERFACE
BGA
(6 OF 10)
SEE_TABLE
HT_REFCLK_AVDD
(1.65V-2.75V)
(1.6V-1.2V)
HT_REFCLK_AVDD2
(1.65V-2.75V)
(1.6V-1.2V)
HT_REFCLK_AGND
KODIAK HT16
SYNC_MASTER=Q63
SYNC_DATE=08/26/2005
NOTICE OF PROPRIETARY PROPERTY
LAST_MODIFIED=Tue Nov 1 13:47:20 2005
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
PAGE 98
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-6863
REV. F
SCALE NONE
SHT 98 OF 154
DRAWING

SIG_NAME	MAKE_BASE	DIFFERENTIAL_PAIR	EC_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE
HT_NB_TO_MB_CLK_N<0>	TRUE	HT_NB_TO_SB_CLK	HT_NB_TO_SB_PP	HT_CAD	HT_NB_TO_SB_CLK
HT_NB_TO_MB_CLK_P<0>	TRUE	HT_NB_TO_SB_CLK	HT_NB_TO_SB_PP	HT_CAD	HT_NB_TO_SB_CLK
HT_NB_TO_MB_CAD_N<0>	TRUE	HT_NB_TO_SB_CAD0	HT_NB_TO_SB_PP	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_P<0>	TRUE	HT_NB_TO_SB_CAD0	HT_NB_TO_SB_PP	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_N<1>	TRUE	HT_NB_TO_SB_CAD1	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_P<1>	TRUE	HT_NB_TO_SB_CAD1	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_N<2>	TRUE	HT_NB_TO_SB_CAD2	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_P<2>	TRUE	HT_NB_TO_SB_CAD2	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_N<3>	TRUE	HT_NB_TO_SB_CAD3	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_P<3>	TRUE	HT_NB_TO_SB_CAD3	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_N<4>	TRUE	HT_NB_TO_SB_CAD4	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_P<4>	TRUE	HT_NB_TO_SB_CAD4	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_N<5>	TRUE	HT_NB_TO_SB_CAD5	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_P<5>	TRUE	HT_NB_TO_SB_CAD5	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_N<6>	TRUE	HT_NB_TO_SB_CAD6	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_P<6>	TRUE	HT_NB_TO_SB_CAD6	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_N<7>	TRUE	HT_NB_TO_SB_CAD7	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_P<7>	TRUE	HT_NB_TO_SB_CAD7	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CTL_N<0>	TRUE	HT_NB_TO_SB_CTL0	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CTL_P<0>	TRUE	HT_NB_TO_SB_CTL0	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_MB_TO_NB_CLK_N<0>	TRUE	HT_SB_TO_NB_CLK	HT_SB_TO_NB_PP	HT_CAD	HT_SB_TO_NB_CLK
HT_MB_TO_NB_CLK_P<0>	TRUE	HT_SB_TO_NB_CLK	HT_SB_TO_NB_PP	HT_CAD	HT_SB_TO_NB_CLK
HT_MB_TO_NB_CAD_N<0>	TRUE	HT_SB_TO_NB_CAD0	HT_SB_TO_NB_PP	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_P<0>	TRUE	HT_SB_TO_NB_CAD0	HT_SB_TO_NB_PP	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_N<1>	TRUE	HT_SB_TO_NB_CAD1	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_P<1>	TRUE	HT_SB_TO_NB_CAD1	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_N<2>	TRUE	HT_SB_TO_NB_CAD2	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_P<2>	TRUE	HT_SB_TO_NB_CAD2	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_N<3>	TRUE	HT_SB_TO_NB_CAD3	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_P<3>	TRUE	HT_SB_TO_NB_CAD3	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_N<4>	TRUE	HT_SB_TO_NB_CAD4	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_P<4>	TRUE	HT_SB_TO_NB_CAD4	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_N<5>	TRUE	HT_SB_TO_NB_CAD5	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_P<5>	TRUE	HT_SB_TO_NB_CAD5	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_N<6>	TRUE	HT_SB_TO_NB_CAD6	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_P<6>	TRUE	HT_SB_TO_NB_CAD6	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_N<7>	TRUE	HT_SB_TO_NB_CAD7	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_P<7>	TRUE	HT_SB_TO_NB_CAD7	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CTL_N<0>	TRUE	HT_SB_TO_NB_CTL0	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CTL_P<0>	TRUE	HT_SB_TO_NB_CTL0	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
NC_HT_MB_TO_NB_CAD_P<8..15>	TRUE				
NC_HT_MB_TO_NB_CAD_N<8..15>	TRUE				
TP_HT_MB_TO_NB_CLK_N<1>	TRUE				
TP_HT_MB_TO_NB_CLK_P<1>	TRUE				
NC_HT_NB_TO_MB_CAD_P<8..15>	TRUE				
NC_HT_NB_TO_MB_CAD_N<8..15>	TRUE				
NC_HT_NB_TO_MB_CLK_N<1>	TRUE				
NC_HT_NB_TO_MB_CLK_P<1>	TRUE				
HT_NB_REFCLK_P<0>		HT_NB_REFCLK0	HT_NB_REFCLK	HT_CLK	HT_CLK
HT_NB_REFCLK_N<0>		HT_NB_REFCLK0		HT_CLK	HT_CLK
HT_NB_P<0>		HT_NB0		HT_CLK	HT_CLK
HT_NB_N<0>		HT_NB0		HT_CLK	HT_CLK
HT_NB_REFCLK_PF<0>		HT_NB_REFCLK_F0		HT_CLK	HT_CLK
HT_NB_REFCLK_NF<0>		HT_NB_REFCLK_F0		HT_CLK	HT_CLK

SIG_NAME	MIN_LINE_WIDTH	MIN_NECK_WIDTH	VOLTAGE
PWR_HT_AVDD	0.4MM	0.2MM	2.5
PWR_HT_AVDD2	0.4MM	0.2MM	2.5
KOD_L15_GND	0.4MM	0.2MM	0
HT_NB_G KEEP DIFF CLOCK FROM BEING A SINGLE XNET			0

HT ALIASES

FINO-M23 08/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F

SCALE: NONE

SHT 101 OF 154

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	0.38mm SPACING	HT_CLK66M_SB_C
HT_CLK66M_SB	0.38mm SPACING	HT_CLK66M_SB
	P3MM SPACING	HT_LDTRESET_L

Page Notes

Power aliases required by this page:
=PP2V5_PWRON_HT
=PP1V2_PWRON_HT

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- SB_HT_200M
  Stuffs resistor to select 200MHz HT I/F.

RA300 3.3 5% 1/8W MF-LF 805 — PP1V2_PWRON_HT_PLLDVDD (VOLTAGE=1.2V) MIN_LINE_WIDTH=0.50mm MIN_NECK_WIDTH=0.38mm
CA300 10UF 10% 6.3V X5R 805
CA301 1uF 10% 6.3V CERM 402

RA310 3.3 5% 1/8W MF-LF 805 — PP1V2_PWRON_HT_PLLAVDD (VOLTAGE=1.2V) MIN_LINE_WIDTH=0.50mm MIN_NECK_WIDTH=0.38mm
CA310 10UF 10% 6.3V X5R 805
CA311 1uF 10% 6.3V CERM 402

=PP2V5_PWRON_HT
CA320 0.1uF 20% 10V CERM 402

=PP1V2_PWRON_SB_HT
CA302 10UF 10% 6.3V X5R 805
CA330 0.1uF 20% 10V CERM 402
CA331 0.1uF 20% 10V CERM 402
CA332 0.1uF 20% 10V CERM 402

=PP1V2_PWRON_SB_HT
CA309 10UF 10% 6.3V X5R 805
CA340 0.1uF 20% 10V CERM 402
CA341 0.1uF 20% 10V CERM 402
CA342 0.1uF 20% 10V CERM 402

HTS2MC0+ PPA300 P4MM SM
HTS2MC0- PPA301 P4MM SM
HTS2MC0+ PPA303 P4MM SM
HTS2MC0- PPA304 P4MM SM

U2300 SHASTA V1.1 BGA-LF (3 OF 8) SEE_TABLE — HYPERTRANSPORT

Pin	HT_PLL / HT_RXVDD / HT_TXVDD
C7	AVDD HT_PLL
B6	DVDD HT_PLL
B19	VDDP HT
B15	HT_RXVDD
B17	HT_RXVDD
G13	HT_RXVDD
B12	HT_TXVDD
B9	HT_TXVDD
G11	HT_TXVDD

Pin	HT_CLKIN / HT_CLKOUT
D15	HT_CLKIN_P
C15	HT_CLKIN_N
B10	HT_CLKOUT_P
A10	HT_CLKOUT_N

Pin	HT_CADIN	HT_CADOUT
D17	HT_CADIN_0_P	HT_CADOUT_0_P
C17	HT_CADIN_0_N	HT_CADOUT_0_N
B18	HT_CADIN_1_P	HT_CADOUT_1_P
A18	HT_CADIN_1_N	HT_CADOUT_1_N
F15	HT_CADIN_2_P	HT_CADOUT_2_P
E15	HT_CADIN_2_N	HT_CADOUT_2_N
D16	HT_CADIN_3_P	HT_CADOUT_3_P
C16	HT_CADIN_3_N	HT_CADOUT_3_N
B16	HT_CADIN_4_P	HT_CADOUT_4_P
A16	HT_CADIN_4_N	HT_CADOUT_4_N
D14	HT_CADIN_5_P	HT_CADOUT_5_P
C14	HT_CADIN_5_N	HT_CADOUT_5_N
E14	HT_CADIN_6_P	HT_CADOUT_6_P
F14	HT_CADIN_6_N	HT_CADOUT_6_N
B14	HT_CADIN_7_P	HT_CADOUT_7_P
A14	HT_CADIN_7_N	HT_CADOUT_7_N

Pin	HT_CTLIN / HT_CTLOUT
F13	HT_CTLIN_P
E13	HT_CTLIN_N
C13	HT_CTLOUT_P
D13	HT_CTLOUT_N

Pin		
E16	HT_PWROK	HT_PWROK_H
C18	HT_LDTRESET_L	HT_RESET_L
E17	HT_LDTSTOP_L	HT_LDTSTOP_L
C8	HT_CLK66M_SB_C	HT_REFCLK
D8	SB_HT_S100M66M	HT_S100M66M
V8	SB_SELHT100	SEL_HT00_H
A19		HT_LDTREQ_L
E10		HT_R100P
F10		HT_R100N

HT_PLL AGND C9 — HT_RXGND A11 A13 G14 — HT_TXGND A14 A9 G12

HT_MB_TO_SB_CLK_P<0>, HT_MB_TO_SB_CLK_N<0>
HT_MB_TO_SB_CAD_P<0>, HT_MB_TO_SB_CAD_N<0>
HT_MB_TO_SB_CAD_P<1>, HT_MB_TO_SB_CAD_N<1>
HT_MB_TO_SB_CAD_P<2>, HT_MB_TO_SB_CAD_N<2>
HT_MB_TO_SB_CAD_P<3>, HT_MB_TO_SB_CAD_N<3>
HT_MB_TO_SB_CAD_P<4>, HT_MB_TO_SB_CAD_N<4>
HT_MB_TO_SB_CAD_P<5>, HT_MB_TO_SB_CAD_N<5>
HT_MB_TO_SB_CAD_P<6>, HT_MB_TO_SB_CAD_N<6>
HT_MB_TO_SB_CAD_P<7>, HT_MB_TO_SB_CAD_N<7>
HT_MB_TO_SB_CTL_P<0>, HT_MB_TO_SB_CTL_N<0>
HT_PWROK, HT_LDTRESET_L, HT_LDTSTOP_L
HT_CLK66M_SB_C, SB_HT_S100M66M, SB_SELHT100
HT_LDTREQ_L — SB_HT_R100_P — SB_HT_R100_N

RA301 0 5% 1/10W MF-LF 402 — HT_LDTREQ_L
RA350 82.5 1% 1/10W MF-LF 402
CA350 47PF 5% 50V CERM 402
CA351 47PF 5% 50V CERM 402

P4MM SM PPA302
RA355 0 5% 1/10W MF-LF 402 — HT_CLK66M_SB — 1.0V pk-pk

=PP1V2_PWRON_SB_HT
RA352 4.7K 1% 1/16W MF-LF 402 — NOSTUFF — 1 = 100MHz
RA354 10K 5% 1/10W MF-LF 402 — NOSTUFF — 1 = 100MHz
RA353 4.7K 1% 1/16W MF-LF 402 — 0 = 66MHz
RA351 1K 1% 1/16W MF-LF 402 — 0 = 200MHz

HT Refclk	HT I/F Speed
1 = 100MHz	1 = 100MHz
0 = 66MHz	0 = 200MHz

← DETERMINES THE OPERATING FREQUENCY OF HT CORE
1: THE HT SLAVE, HTGS AND THE HT SIDE OF THE PCI BRIDGES OPERATE AT 100 MHZ
0: THE HT SLAVE, HTGS AND THE HT SIDE OF THE PCI BRIDGES OPERATE AT 200 MHZ

Shasta HyperTransport

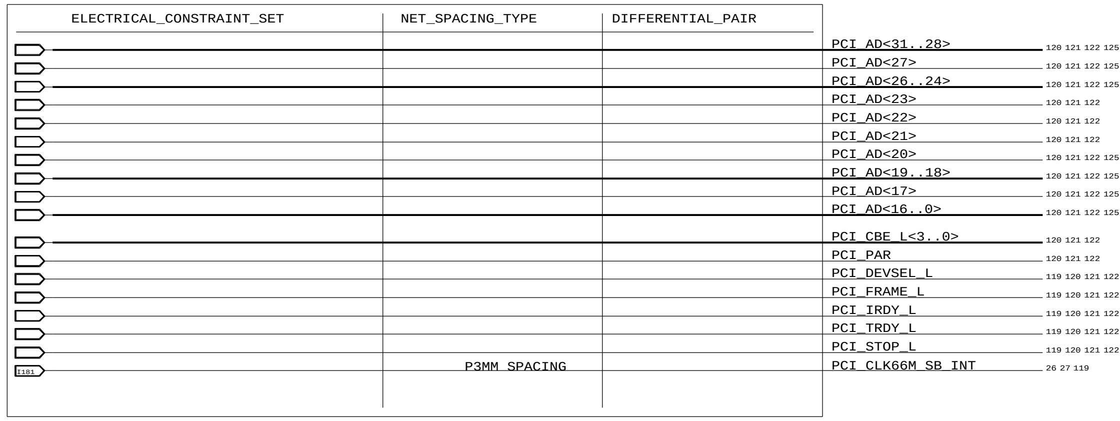
SYNC_MASTER=Q63 SYNC_DATE=08/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT: 103	OF: 154

LAST_MODIFIED=Tue Nov 1 13:45:49 2005

DRAWING
TITLE=K1LOWARA
ASSEMBLY=SRAWING



Q63 APPLICATION OF POWER NET "=PP3V3_SB_PCI" IS RUN

Page Notes

Power aliases required by this page:

- =PP3V3_PCI
- =PP3V3_SB_PCI (CAN BE _PP3V3_PCI)
- =PP3V3_PWRON_SB
- =PP2V5_PWRON_SB

Signal aliases required by this page:

(NONE)

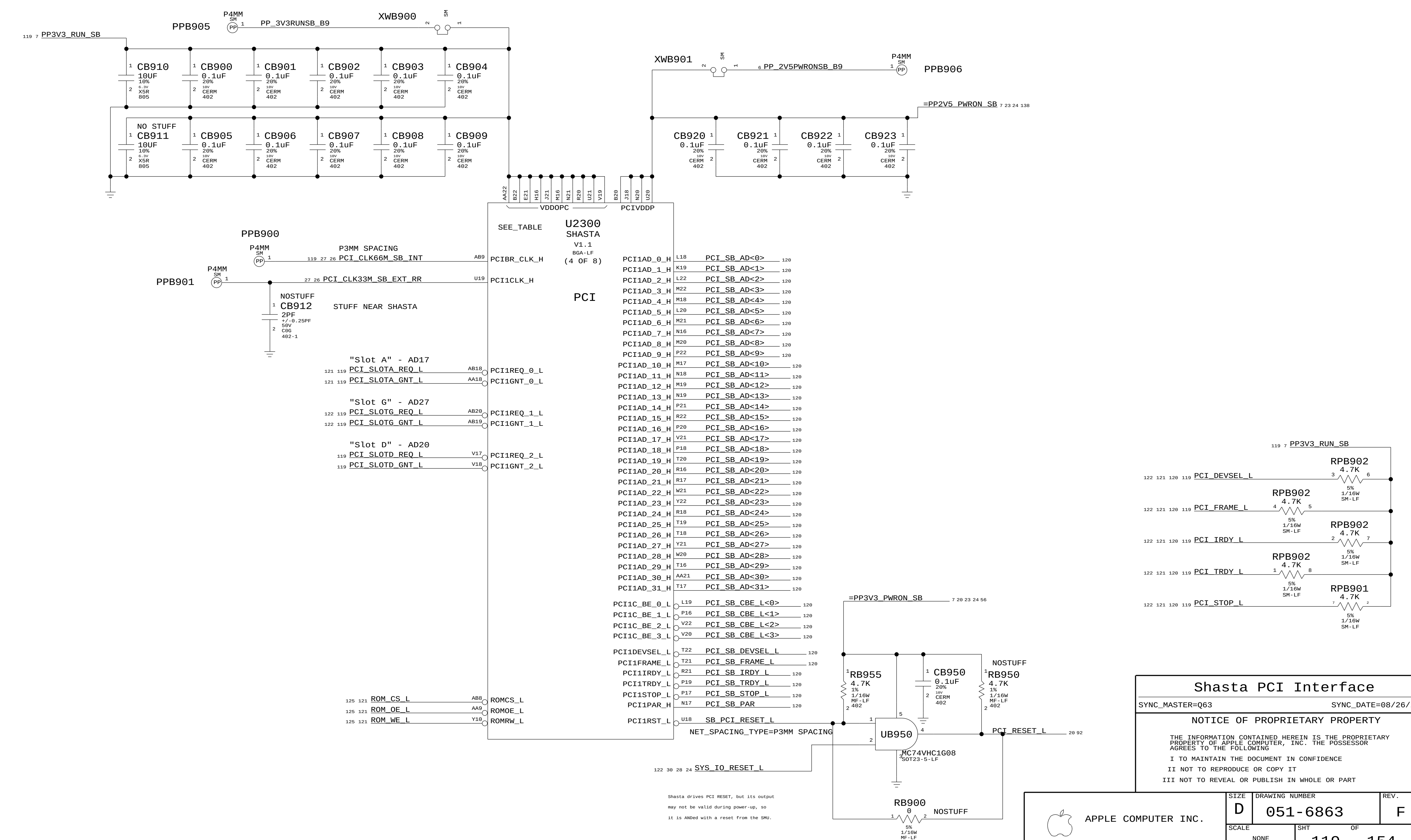
BOM options provided by this page:

(NONE)

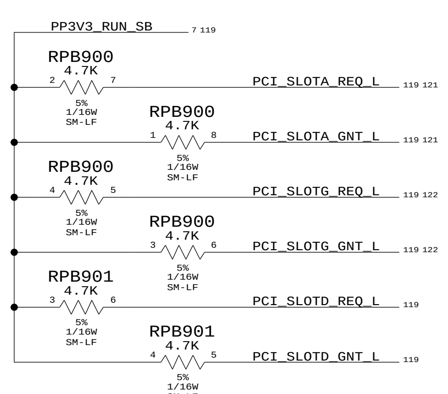
PCI Devices implemented on this page:

AD11 - PCI0 (0x106B/0x0053)
AD11 - PCI1 (0x106B/0x0054)
AD11 - PCI2 (0x106B/0x0055)

AD23 - KeyLargo (0x106B/0x004F, PCI1)
AD28 - SATA 150 (0x1166/0x0240, PCI0 or 2)
AD29 - UATA 133 (0x106B/0x0050, PCI0 or 2)
AD30 - FireWire (0x106B/0x0052, PCI0 or 2)
AD31 - Ethernet (0x106B/0x0051, PCI0)



Shasta drives PCI RESET, but its output may not be valid during power-up, so it is ANDed with a reset from the SMU.



Shasta PCI Interface

SYNC_MASTER=Q63 SYNC_DATE=08/26/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F

SCALE	SHT	OF
NONE	119	154

LAST_MODIFIED=Tue Nov 1 13:45:54 2005

ALL RESISTOR PACKS ARE 47 OHM 1/16W 5%

R PAKS ARE PIN SWAPPABLE ACROSS ALL SIGNALS (EXCEPT IDSELS)

119	PCI_SB_AD<0>	RPC003	4	5	47	PCI_AD<0>	119 121 122 125
119	PCI_SB_AD<1>	RPC003	1	8	47	PCI_AD<1>	119 121 122 125
119	PCI_SB_AD<2>	RPC009	1	8	47	PCI_AD<2>	119 121 122 125
119	PCI_SB_AD<3>	RPC001	3	6	47	PCI_AD<3>	119 121 122 125
119	PCI_SB_AD<4>	RPC000	3	6	47	PCI_AD<4>	119 121 122 125
119	PCI_SB_AD<5>	RPC003	2	7	47	PCI_AD<5>	119 121 122 125
119	PCI_SB_AD<6>	RPC001	4	5	47	PCI_AD<6>	119 121 122 125
119	PCI_SB_AD<7>	RPC000	2	7	47	PCI_AD<7>	119 121 122 125
119	PCI_SB_AD<8>	RPC007	4	5	47	PCI_AD<8>	119 121 122 125
119	PCI_SB_AD<9>	RPC002	1	8	47	PCI_AD<9>	119 121 122 125
119	PCI_SB_AD<10>	RPC000	1	8	47	PCI_AD<10>	119 121 122 125
119	PCI_SB_AD<11>	RPC009	3	6	47	PCI_AD<11>	119 121 122 125
119	PCI_SB_AD<12>	RPC000	4	5	47	PCI_AD<12>	119 121 122 125
119	PCI_SB_AD<13>	RPC009	4	5	47	PCI_AD<13>	119 121 122 125
119	PCI_SB_AD<14>	RPC002	2	7	47	PCI_AD<14>	119 121 122 125
119	PCI_SB_AD<15>	RPC002	4	5	47	PCI_AD<15>	119 121 122 125
119	PCI_SB_AD<16>	RPC002	3	6	47	PCI_AD<16>	119 121 122 125

RC000

119	PCI_SB_AD<17>		1	2	47 5% 1/16W MF-LF 402	PCI_AD<17>	119 121 122 125

119	PCI_SB_AD<18>	RPC007	1	8	47	PCI_AD<18>	119 121 122 125
119	PCI_SB_AD<19>	RPC006	2	7	47	PCI_AD<19>	119 121 122 125
119	PCI_SB_AD<20>	RPC007	2	7	47	PCI_AD<20>	119 121 122 125
119	PCI_SB_AD<21>	RPC008	1	8	47	PCI_AD<21>	119 121 122
119	PCI_SB_AD<22>	RPC004	1	8	47	PCI_AD<22>	119 121 122
119	PCI_SB_AD<23>	RPC006	4	5	47	PCI_AD<23>	119 121 122
119	PCI_SB_AD<24>	RPC008	4	5	47	PCI_AD<24>	119 121 122 125
119	PCI_SB_AD<25>	RPC006	3	6	47	PCI_AD<25>	119 121 122 125
119	PCI_SB_AD<26>	RPC008	3	6	47	PCI_AD<26>	119 121 122 125

RC001

119	PCI_SB_AD<27>		1	2	47 5% 1/16W MF-LF 402	PCI_AD<27>	119 121 122 125

119	PCI_SB_AD<28>	RPC004	4	5	47	PCI_AD<28>	119 121 122 125
119	PCI_SB_AD<29>	RPC008	2	7	47	PCI_AD<29>	119 121 122 125
119	PCI_SB_AD<30>	RPC004	2	7	47	PCI_AD<30>	119 121 122 125
119	PCI_SB_AD<31>	RPC007	3	6	47	PCI_AD<31>	119 121 122 125
119	PCI_SB_CBE_L<0>	RPC003	3	6	47	PCI_CBE_L<0>	119 121 122
119	PCI_SB_CBE_L<1>	RPC001	1	8	47	PCI_CBE_L<1>	119 121 122
119	PCI_SB_CBE_L<2>	RPC006	1	8	47	PCI_CBE_L<2>	119 121 122
119	PCI_SB_CBE_L<3>	RPC004	3	6	47	PCI_CBE_L<3>	119 121 122
119	PCI_SB_DEVSEL_L	RPC005	3	6	47	PCI_DEVSEL_L	119 121 122
119	PCI_SB_FRAME_L	RPC005	4	5	47	PCI_FRAME_L	119 121 122
119	PCI_SB_IRDY_L	RPC005	2	7	47	PCI_IRDY_L	119 121 122
119	PCI_SB_TRDY_L	RPC005	1	8	47	PCI_TRDY_L	119 121 122
119	PCI_SB_STOP_L	RPC001	2	7	47	PCI_STOP_L	119 121 122
119	PCI_SB_PAR	RPC009	2	7	47	PCI_PAR	119 121 122

PLACE CLOSE TO SHASTA

AD<17> IS IDSEL FOR AIRPORT
AD<27> IS IDSEL FOR USB

PCI SERIES TERMINATION

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 120 OF 154	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_CLK_AIRPORT	CLOCKS	

PCI_CLK33M_AIRPORT 26 121

Page Notes

Power aliases required by this page:
- _PP3V3_PCI

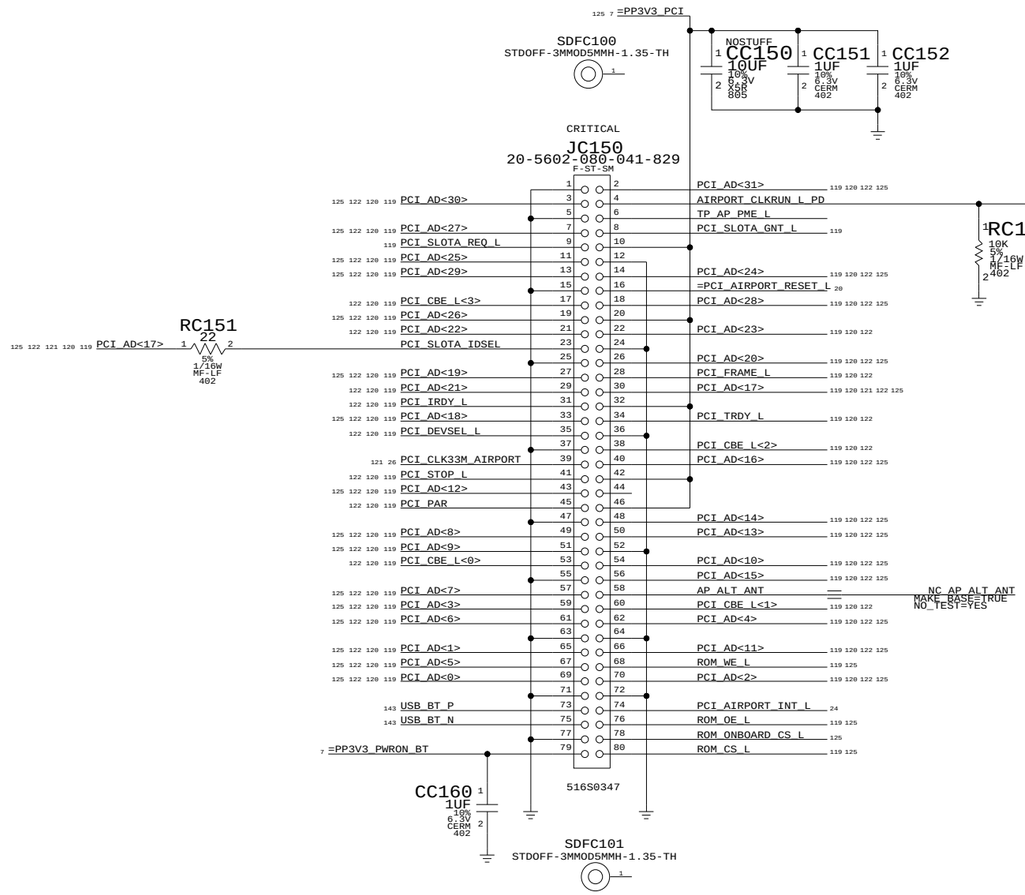
Signal aliases required by this page:
- _PCI_CLK33M_AIRPORT (33MHz PCI clock)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD17 (Slot "A") - AirPort (0x????/0x????)

NOTE: This AirPort implementation does not support PME#.

Q85 WIRELESS CONNECTOR



AIRPORT & BLUETOOTH

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F

SCALE	SHT	OF
NONE	121	154

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	CLOCKS	

=PCI_CLK33M_USB2 27 122

Page Notes

Power aliases required by this page:
- _PPVIO_PCI (to 3.3V or 5V)

Signal aliases required by this page:
- _PCI_CLK33M_USB2 (33MHz PCI clock)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD27 (Slot "G") - USB2 (0x1033/0x0035)

NOTE: This USB2 implementation supports
D3cold.

Q63 APPLICATION OF POWER NET "=PPVIO_PCI_USB2" IS PP3V3_RUN

122 7 =PPVIO_PCI_USB2

CC201 0.1uF 20% 10V CERM 402
CC202 0.1uF 20% 10V CERM 402
CC203 0.1uF 20% 10V CERM 402

XWC200 SM 6 PP_VIOPCIUSB2_C2 P4MM SM PPC203

M3 M4 C8 VDD_PCI

CRITICAL
UC200
NEC_UPD720101_USB2
FBGA-LF

125 121 120 119 PCI_AD<0>	M5	AD0	
125 121 120 119 PCI_AD<1>	P5	AD1	
125 121 120 119 PCI_AD<2>	N5	AD2	
125 121 120 119 PCI_AD<3>	P4	AD3	
125 121 120 119 PCI_AD<4>	N4	AD4	
125 121 120 119 PCI_AD<5>	M3	AD5	
125 121 120 119 PCI_AD<6>	N3	AD6	
125 121 120 119 PCI_AD<7>	M1	AD7	
125 121 120 119 PCI_AD<8>	L2	AD8	
125 121 120 119 PCI_AD<9>	L1	AD9	
125 121 120 119 PCI_AD<10>	K2	AD10	
125 121 120 119 PCI_AD<11>	L3	AD11	
125 121 120 119 PCI_AD<12>	K1	AD12	
125 121 120 119 PCI_AD<13>	K3	AD13	
125 121 120 119 PCI_AD<14>	J2	AD14	
125 121 120 119 PCI_AD<15>	J1	AD15	
125 121 120 119 PCI_AD<16>	F2	AD16	
125 121 120 119 PCI_AD<17>	E1	AD17	
125 121 120 119 PCI_AD<18>	E2	AD18	
125 121 120 119 PCI_AD<19>	D1	AD19	
125 121 120 119 PCI_AD<20>	D2	AD20	
121 120 119 PCI_AD<21>	D3	AD21	
121 120 119 PCI_AD<22>	C2	AD22	
121 120 119 PCI_AD<23>	C1	AD23	
125 121 120 119 PCI_AD<24>	B2	AD24	
125 121 120 119 PCI_AD<25>	A2	AD25	
125 121 120 119 PCI_AD<26>	B3	AD26	
125 121 120 119 PCI_AD<27> (PCI_AD<27>)	C4	AD27	
125 121 120 119 PCI_AD<28>	A3	AD28	
125 121 120 119 PCI_AD<29>	C5	AD29	
125 121 120 119 PCI_AD<30>	B4	AD30	
125 121 120 119 PCI_AD<31>	A4	AD31	
121 120 119 PCI_CBE_L<0>	M2	CBE0	
121 120 119 PCI_CBE_L<1>	J3	CBE1	
121 120 119 PCI_CBE_L<2>	F3	CBE2	
121 120 119 PCI_CBE_L<3>	C3	CBE3	
121 120 119 PCI_PAR	J4	PAR	
121 120 119 PCI_FRAME_L	F3	FRAME	
121 120 119 PCI_IRDY_L	F4	IRDY	
121 120 119 PCI_TRDY_L	G1	TRDY	
121 120 119 PCI_STOP_L	G3	STOP	
PCI_SLOTG_IDSEL	B5	IDSEL	
121 120 119 PCI_DEVSEL_L	G2	DEVSEL	
119 PCI_SLOTG_REQ_L	C6	REQ	
119 PCI_SLOTG_GNT_L	D6	GNT	
NEC_PERR_L_PU	H2	PERR	
NEC_SERR_L_PU	H1	SERR (OD)	
NEC_INTA_L	C7	INTA (OD)	
NEC_INTB_L	B7	INTB (OD)	
NEC_INTC_L	A7	INTC (OD)	
122 27 =PCI_CLK33M_USB2	A8	PCLK	
NEC_VBBRST_L	B8	VBBRST (CHIP RESET)	
NEC_CRUN_L_PD	N6	CRUN	
NEC_PME_L	D5	PME (OD)	
	C5	VCCRST (PCI RESET)	
6 TP_NEC_SMI_L	L6	SMI (OD)	
NEC_LEGC_PD	L7	LEGC	

IPD	NTEST1	M8	TP_NEC_NTEST1 6
IPD	SMC	M7	TP_NEC_SMC 6
IPD	TEB	N7	TP_NEC_TEB
IPD	AMC	P7	TP_NEC_AMC
IPD	TEST	L8	TP_NEC_TEST 6
	NANDTEST	M10	TP_NEC_NANDTEST
	SRCLK	M9	TP_NEC_SRCLK 6
	SRDTA	N9	TP_NEC_SRDATA
IPD	SRMOD	P9	TP_NEC_SRMOD 6

ALL NETS TO FUNCTIONAL TEST PAGE

RC214 22 5% 1/16W MF-LF 402

122 7 =PPVIO_PCI_USB2

RC216 10K 5% 1/16W MF-LF 402
RC213 10K 5% 1/16W MF-LF 402

24 PCI_USB2_INT_L
RPC203 47 5% 1/16W SM-LF (4 5)
RPC203 47 5% 1/16W SM-LF (2 7)
RPC203 47 5% 1/16W SM-LF (3 6)

119 30 28 24 SYS_IO_RESET_L
RC250 47 5% 1/16W MF-LF 402

28 24 SYS_PME_L
RC251 47 5% 1/16W MF-LF 402

20 =PCI_USB2_RESET_L

RC250, RC251 & RPC203 REQUIRED TO facilitate NAND-tree testing

RC215 4.7K 1% 1/16W MF-LF 402
RPC203 47 5% 1/16W SM-LF (8 1)

PPC200 P4MM SM PP 1
PPC201 P4MM SM PP 1

USB 2.0 PCI Interface

SYNC_MASTER=Q63 SYNC_DATE=08/26/2005

NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 122 OF 154	

LAST_MODIFIED=Tue Nov 1 13:45:57 2005

DRAWING

TITLE=PCIUSB4A

ASSEMBLY=SMAUSB4

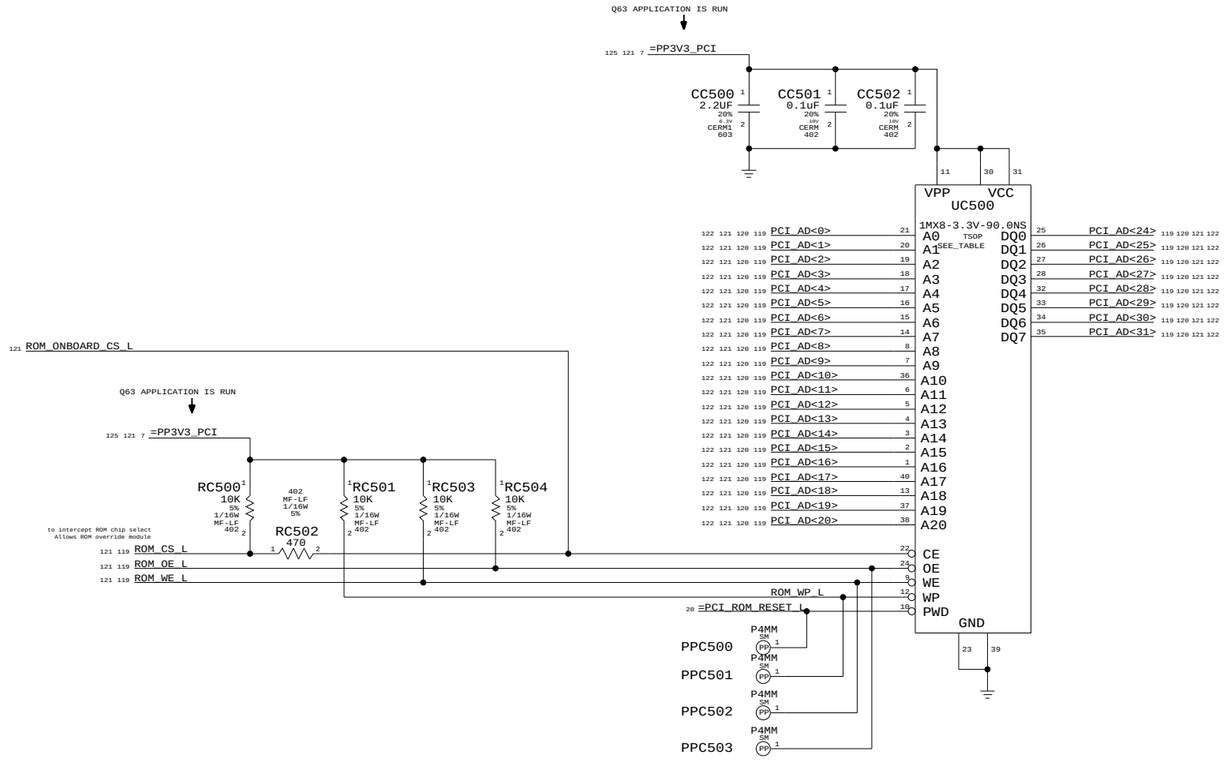
Page Notes

Power aliases required by this page:
- =PP3V3_PCI

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NOTE: This page does not specify a BootROM part number. Must use a TABLE_x_ITEM symbol to declare U7500 part number.



BootROM		
SYNC_MASTER=Q63	SYNC_DATE=08/26/2005	

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	F
	SCALE: NONE	SHT: 125	OF: 154

LAST_MODIFIED=Tue Nov 1 13:45:58 2005

DRAWING
TITLE=MISLOOKUP
ASSEMBLY=DRAWING

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR	
	SATA	SATA	SATA_RXD1_C	SATA_RXD_P1_C
	SATA	SATA	SATA_RXD1_C	SATA_RXD_N1_C
	SATA	SATA	SATA_TXD1	SATA_TXD_P1
	SATA	SATA	SATA_TXD1	SATA_TXD_N1
	SATA	SATA	SATA_RXD2_C	SATA_RXD_P2_C
	SATA	SATA	SATA_RXD2_C	SATA_RXD_N2_C
	SATA	SATA	SATA_TXD2	SATA_TXD_P2
	SATA	SATA	SATA_TXD2	SATA_TXD_N2
				UATA_DD<15..8>
				UATA_DD<7>
				UATA_DD<6..0>
				UATA_DA<2..0>
				UATA_CS0_L
				UATA_CS1_L
				UATA_HSTROBE
				UATA_STOP
				UATA_DMACK_L
	UATA_NETSPA			UATA_RESET_L
				UATA_DSTROBE
				UATA_DMARQ
				UATA_INTRQ
174				UATA_DD_R<15..8>
173				UATA_DD_R<7>
172				UATA_DD_R<6..0>
171				UATA_DA_R<2..0>
170				UATA_CS0_L_R
169				UATA_CS1_L_R
177				UATA_DMACK_L_R
176				UATA_HSTROBE_R
175				UATA_STOP_R
168				UATA_RESET_L_R

PLACE UATA TERMINATION RESISTORS NEAR JC901 CONNECTOR

DIOR- :HDMARDY- :HSTROBE >

DIOW- :STOP >

SPARE
RPC704 33 5% 1/16W SM-LF

RC706 33 5% 1/16W MF-LF 402: UATA_RESET_L_R → UATA_RESET_L
RC704 22 5% 1/16W MF-LF 402: UATA_DMACK_L_R → UATA_DMACK_L
RC702 22 5% 1/16W MF-LF 402: UATA_HSTROBE_R → UATA_HSTROBE
RC703 22 5% 1/16W MF-LF 402: UATA_STOP_R → UATA_STOP
RC700 33 5% 1/16W MF-LF 402: UATA_CS0_L_R → UATA_CS0_L
RC701 33 5% 1/16W MF-LF 402: UATA_CS1_L_R → UATA_CS1_L

RPC704 33 5% 1/16W SM-LF: UATA_DA_R<0> → UATA_DA<0>; UATA_DA_R<1> → UATA_DA<1>; UATA_DA_R<2> → UATA_DA<2>

RPC700 33 5% 1/16W SM-LF: UATA_DD_R<0> → UATA_DD<0>; UATA_DD_R<1> → UATA_DD<1>; UATA_DD_R<2> → UATA_DD<2>; UATA_DD_R<3> → UATA_DD<3>; UATA_DD_R<4> → UATA_DD<4>; UATA_DD_R<5> → UATA_DD<5>; UATA_DD_R<6> → UATA_DD<6>; UATA_DD_R<7> → UATA_DD<7>

RPC701 33 5% 1/16W SM-LF: UATA_DD_R<8> → UATA_DD<8>; UATA_DD_R<9> → UATA_DD<9>; UATA_DD_R<10> → UATA_DD<10>; UATA_DD_R<11> → UATA_DD<11>

RPC702 33 5% 1/16W SM-LF: UATA_DD_R<12> → UATA_DD<12>; UATA_DD_R<13> → UATA_DD<13>

RPC703 33 5% 1/16W SM-LF: UATA_DD_R<14> → UATA_DD<14>; UATA_DD_R<15> → UATA_DD<15>

RC705 10K 5% 1/16W MF-LF 402

=PP1V2_PWRON_DISK_SB → LC700 600-OHM-1.0A 0805

MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.6MM
PP1V2_SATA_VDD

CC705 2.2UF 20% 6.3V CERM1 603
CC700 0.1UF 20% 10V CERM 402
CC701 0.1UF 20% 10V CERM 402
CC702 0.1UF 20% 10V CERM 402
CC703 0.1UF 20% 10V CERM 402
CC704 0.1UF 20% 10V CERM 402

XWCC00 SM → PP_1V2PWRONDISKSB_CC, NO_TEST=YES → P4MM SM PP → PPCC00

SATA_VDD x 5

SATA_VDD (AB14, AB17, T14, W15, Y18)

U2300 SHASTA V1.1 BGA-LF (5 OF 8) SEE_TABLE

UATA:
UD_IDEDD_0_H J6 UATA_DD_R<0>
UD_IDEDD_1_H H7 UATA_DD_R<1>
UD_IDEDD_2_H H6 UATA_DD_R<2>
UD_IDEDD_3_H E2 UATA_DD_R<3>
UD_IDEDD_4_H C1 UATA_DD_R<4>
UD_IDEDD_5_H C2 UATA_DD_R<5>
UD_IDEDD_6_H E3 UATA_DD_R<6>
UD_IDEDD_7_H G6 UATA_DD_R<7>
UD_IDEDD_8_H G5 UATA_DD_R<8>
UD_IDEDD_9_H D4 UATA_DD_R<9>
UD_IDEDD_10_H G7 UATA_DD_R<10>
UD_IDEDD_11_H F6 UATA_DD_R<11>
UD_IDEDD_12_H C3 UATA_DD_R<12>
UD_IDEDD_13_H F5 UATA_DD_R<13>
UD_IDEDD_14_H E5 UATA_DD_R<14>
UD_IDEDD_15_H D5 UATA_DD_R<15>

DSTROBE aka: IORDY/HDMARDY* / HSTROBE aka: DIOR* / STOP aka: DIOW*

UD_IDEDA0_H E6 UATA_DA_R<0>
UD_IDEDA1_H C4 UATA_DA_R<1>
UD_IDEDA2_H D6 UATA_DA_R<2>

UD_IDECS1FX_L B3 UATA_CS0_L_R
UD_IDECS3FX_L B4 UATA_CS1_L_R

UATA_DSTROBE F9 → UD_IDECHRDY_H
UATA_DMARQ D7 ← UD_IDEDMARQ_H
UATA_INTRQ C5 ← UD_IDEINTRQ_H

UD_IDEDMACK_L E8 UATA_DMACK_L_R
UD_IDERD_L E4 UATA_HSTROBE_R
UD_IDEWR_L D3 UATA_STOP_R
UD_IDERST_L E7 UATA_RESET_L_R

SATA 0:
SATA_RXD_P1_C Y17 → RXDP1
SATA_RXD_N1_C Y16 → RXDN1
RXDP1 AA16 SATA_TXD_P1
RXDN1 AB16 SATA_TXD_N1

SATA 1:
SATA_RXD_P2_C AB15 → RXDP2
SATA_RXD_N2_C AA15 → RXDN2
RXDP2 Y15 SATA_TXD_P2
RXDN2 Y14 SATA_TXD_N2

SATA_GND (AA14, AA17, T13, W13)

P4MM SM PP → PPCC01

Page Notes

Power aliases required by this page:
- _P1V2_PWRON_DISK

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: SATA

Line To Line:	0.38mm
Length Tolerance:	1.27mm
Primary Max Sep:	0.25mm outer
Primary Max Sep:	0.23mm inner
Secondary Max Sep:	2.54mm
Secondary Length:	12.70mm

NOTE: Target differential impedance for SATA data pairs is 100 ohms.

4-29-05

AS OF TODAY THIS PAGE FOR M33 IS NOT SYNC WITH Q63.
RPAK PINS WERE REMAPPED FOR BETTER ROUTING AROUND UATA CONNECTOR.

Shasta Disk

SYNC_MASTER=M33-DC SYNC_DATE=06/20/2005

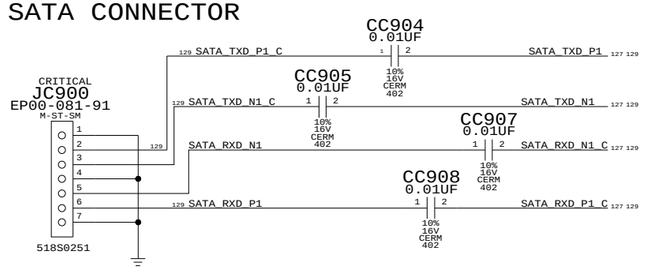
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 127 OF 154	

DRAWING

LAST_MODIFIED=Tue Nov 1 13:45:59 2005

SATA CONNECTOR



SATA PORT1 IS NOT USED IN M23/M33:NO TEST

SATA_TXD_P2 — NC_SATA_TXD_P2 (MAKE_BASE=TRUE)
SATA_TXD_N2 — NC_SATA_TXD_N2 (MAKE_BASE=TRUE)
SATA_RXD_N2_C — NC_SATA_RXD_N2_C (MAKE_BASE=TRUE)
SATA_RXD_P2_C — NC_SATA_RXD_P2_C (MAKE_BASE=TRUE)

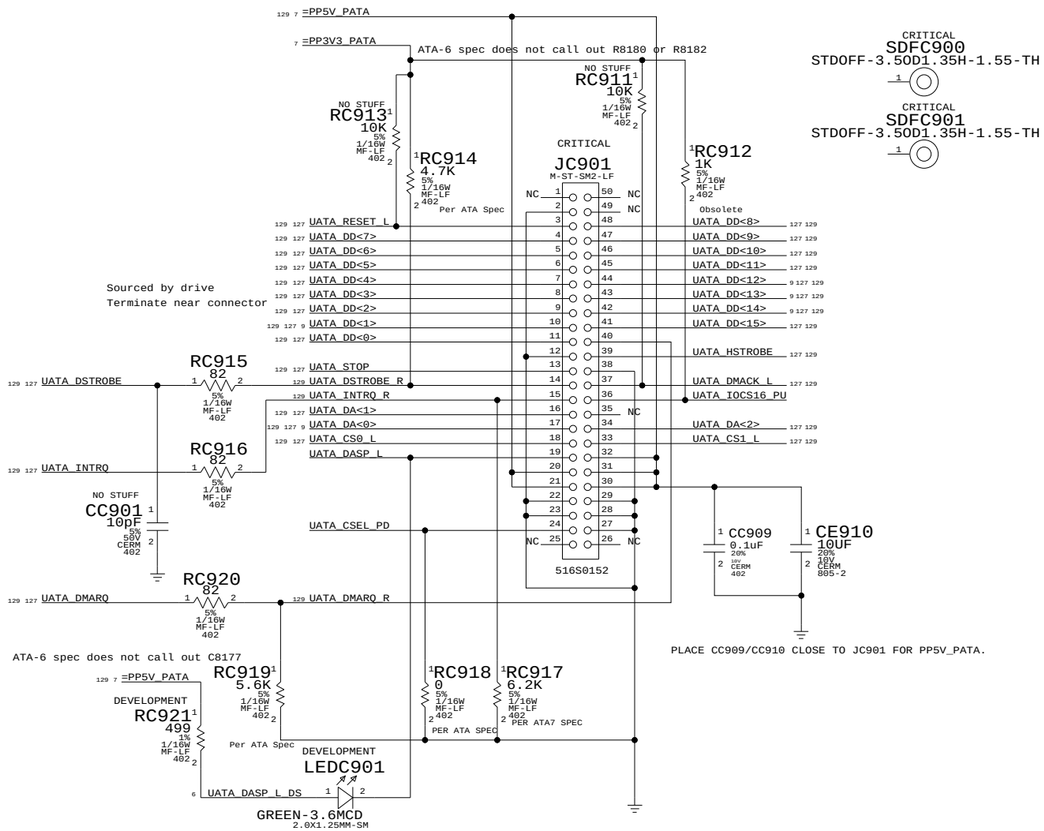
SATA & USB DIFF PAIR GND VIAS

ADD THESE GROUND VIAS NEAR EACH LAYER JUMP FOR THE SATA DIFF PAIRS. ONE GND VIA PER SIGNAL VIA, AND PLACE GND VIA APPROXIMATELY 0.152MM AWAY FROM SIGNAL VIA.

GV901 HOLE-VIA-P5RP25
GV902 HOLE-VIA-P5RP25
GV903 HOLE-VIA-P5RP25
GV904 HOLE-VIA-P5RP25
GV905 HOLE-VIA-P5RP25
GV906 HOLE-VIA-P5RP25
GV907 HOLE-VIA-P5RP25
GV908 HOLE-VIA-P5RP25
GV909 HOLE-VIA-P5RP25
GV910 HOLE-VIA-P5RP25
GV911 HOLE-VIA-P5RP25
GV912 HOLE-VIA-P5RP25
GV913 HOLE-VIA-P5RP25
GV914 HOLE-VIA-P5RP25
GV915 HOLE-VIA-P5RP25
GV916 HOLE-VIA-P5RP25

M33 PATA CONNECTOR

4-12-05



CRITICAL
SDFC900
STDOFF-3.5OD1.35H-1.55-TH

CRITICAL
SDFC901
STDOFF-3.5OD1.35H-1.55-TH

UATA FROM RPAKS TO JC901

	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	NO_TEST
UATA_DD<15..8>	UATA_DD	UATA_NETPH	UATA_NETSPA		
UATA_DD<7>	UATA_DD7	UATA_NETPH	UATA_NETSPA		
UATA_DD<6..0>	UATA_DD	UATA_NETPH	UATA_NETSPA		
UATA_DA<2..0>	UATA_HOST	UATA_NETPH	UATA_NETSPA		
UATA_CS0_L	UATA_HOST	UATA_NETPH	UATA_NETSPA		
UATA_CS1_L	UATA_HOST	UATA_NETPH	UATA_NETSPA		
UATA_HSTROBE	UATA_HOST	UATA_NETPH	UATA_NETSPA		
UATA_STOP	UATA_HOST	UATA_NETPH	UATA_NETSPA		
UATA_DMACK_L	UATA_HOST_R	UATA_NETPH	UATA_NETSPA		
UATA_RESET_L	UATA_RESET_L	UATA_NETPH	UATA_NETSPA		
UATA_DSTROBE_R	UATA_DEV_R_C	UATA_NETPH	UATA_NETSPA		
UATA_DMARQ_R	UATA_DEV_R	UATA_NETPH	UATA_NETSPA		
UATA_INTRQ_R	UATA_DEV_R	UATA_NETPH	UATA_NETSPA		

UATA FROM SHASTA U2300 TO RPAKS

SATA_TXD_P1	SATA_TXD1	SATA	SATA		TRUE
SATA_TXD_N1	SATA_TXD1	SATA	SATA		TRUE
SATA_TXD_P1_C	SATA_TXD1	SATA	SATA	TX1C	TRUE
SATA_TXD_N1_C	SATA_TXD1	SATA	SATA	TX1C	TRUE
SATA_RXD_N1_C	SATA_RXD1	SATA	SATA		TRUE
SATA_RXD_P1_C	SATA_RXD1	SATA	SATA		TRUE
SATA_RXD_N1	SATA_RXD1	SATA	SATA	RX1C	TRUE
SATA_RXD_P1	SATA_RXD1	SATA	SATA	RX1C	TRUE

4-11-05: BOARD FILE HAS PHYSICAL/SPACING NAME ASSIGMENT ALREADY FOR SATA DIFF PAIRS (CAP TO SHASTA). BUT NOT FOR THE SATA CAP TO CONNECTOR ROUTES, WHICH THE ABOVE ARE ADDED FOR THIS PURPOSE.

UATA TRACE IMPEDANCE ROUTE TO 50 OHMS

4-8-05
NOTES FOR SHARED PAGE 127
FOR M23/M33 CREATE A WIDE SHAPE
FOR PP1V2_SATA_VDD AND THEN NECK DOWN
TO THE DEFAULT VALUE WHEN NECESSARY.
THE WIDTH/NECK PROPERTIES ON PAGE 127
ARE SET BY Q63 FOR SCHEMATIC SHARING.

LC700 CHANGED TO 155S0240 (600 OHM,0.2 OHM DCR,1A)
PREVIOUS ONE WAS 155S0031 (600 OHM,0.6 OHM DCR,0.2A)
PER TOKIN AMERICA PN: N2012Z601.

4-11-05.
PP1V2_ALL REG. IS SET TO BE 1.22V TO 1.23V
AS NOTED ON THE 1.2 REG PAGE 13. THIS WILL
HELP MITIGATE THE LOSS ACROSS THE Q1306 FET
SI3326DV.

4-12-05.
UPDATED AC COUPLING CAPS FOR SATA JC900.
ADDED DECOUPLING CAPS FOR JC901 PP5V_PATA NET.

Disk Connectors

SYNC_MASTER=M33-DC SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 129 OF 154	

PLACE THESE SERIES TERM CLOSE TO DRIVER: SB/SHASTA

SHASTA -> VESTA

131 9	ENET_TXD_R<0>	I59	MAKE_BASE=TRUE	ENET_TXD<0>	9 131 132
131 9	ENET_TXD_R<1>	I60	MAKE_BASE=TRUE	ENET_TXD<1>	9 131 132
131 9	ENET_TXD_R<2>	I61	MAKE_BASE=TRUE	ENET_TXD<2>	9 131 132
131 9	ENET_TXD_R<3>	I62	MAKE_BASE=TRUE	ENET_TXD<3>	9 131 132
131 9	ENET_TXD_R<4>	I63	MAKE_BASE=TRUE	ENET_TXD<4>	9 131 132
131 9	ENET_TXD_R<5>	I64	MAKE_BASE=TRUE	ENET_TXD<5>	9 131 132
131 9	ENET_TXD_R<6>	I65	MAKE_BASE=TRUE	ENET_TXD<6>	9 131 132
131 9	ENET_TXD_R<7>	I66	MAKE_BASE=TRUE	ENET_TXD<7>	9 131 132
131 9	ENET_TX_EN_R	I67	MAKE_BASE=TRUE	ENET_TX_EN	9 131 132
131 9	ENET_TX_ER_R	I68	MAKE_BASE=TRUE	ENET_TX_ER	9 131 132
131	ENET_CLK125M_GTX_R	I69	MAKE_BASE=TRUE	ENET_CLK125M_GTX	131 132
131	ENET_MDIO_R		MAKE_BASE=TRUE	ENET_MDIO	131 132

PLACE THESE SERIES TERM CLOSE TO DRIVER: VESTA

VESTA -> SHASTA

132	ENET_CLK125M_GBE_REF_R	I84	MAKE_BASE=TRUE	ENET_CLK125M_GBE_REF	131
132	ENET_CLK25M_TX_R	I70	MAKE_BASE=TRUE	ENET_CLK25M_TX	131
132	ENET_CLK125M_RX_R	I71	MAKE_BASE=TRUE	ENET_CLK125M_RX	131
132 131 9	ENET_RXD_R<0>	I72	MAKE_BASE=TRUE	ENET_RXD<0>	9 131
132 131 9	ENET_RXD_R<1>	I73	MAKE_BASE=TRUE	ENET_RXD<1>	9 131
132 131 9	ENET_RXD_R<2>	I74	MAKE_BASE=TRUE	ENET_RXD<2>	9 131
132 131 9	ENET_RXD_R<3>	I75	MAKE_BASE=TRUE	ENET_RXD<3>	9 131
132 131 9	ENET_RXD_R<4>	I76	MAKE_BASE=TRUE	ENET_RXD<4>	9 131
132 131 9	ENET_RXD_R<5>	I77	MAKE_BASE=TRUE	ENET_RXD<5>	9 131
132 131 9	ENET_RXD_R<6>	I78	MAKE_BASE=TRUE	ENET_RXD<6>	9 131
132 131 9	ENET_RXD_R<7>	I79	MAKE_BASE=TRUE	ENET_RXD<7>	9 131
132 131	ENET_RX_DV_R	I80	MAKE_BASE=TRUE	ENET_RX_DV	131
132 131	ENET_RX_ER_R	I81	MAKE_BASE=TRUE	ENET_RX_ER	131
132 131	ENET_COL_R	I82	MAKE_BASE=TRUE	ENET_COL	131
132 131	ENET_CRS_R	I83	MAKE_BASE=TRUE	ENET_CRS	131

ENET SERIES TERM

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F

SCALE	SHT	OF
NONE	130	154

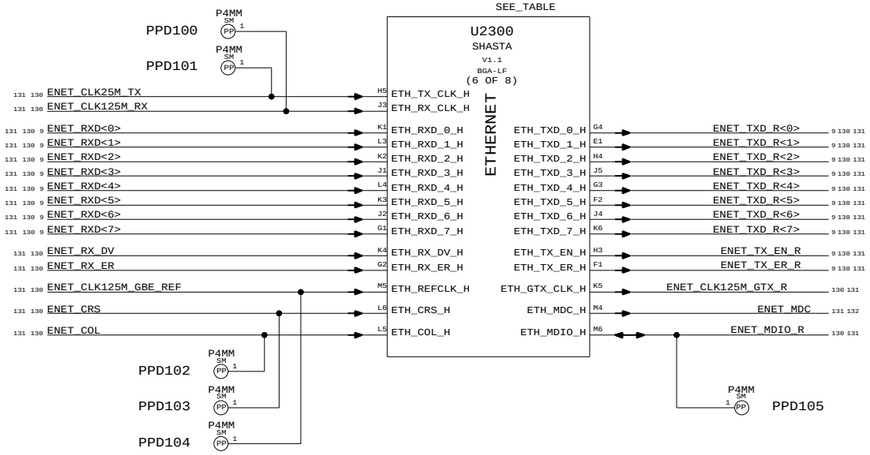
ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
I47	0.38mm SPACING		ENET_CLK25M_TX 130 131
I46	0.38mm SPACING		ENET_CLK125M_RX 130 131
I48	0.38mm SPACING		ENET_CLK125M_GBE_REF 130 131
I22	0.38mm SPACING		ENET_CLK125M_GTX 130 132
I50	0.38mm SPACING		ENET_CLK125M_GTX_R 130 131
I53	ENET_FW_2X		ENET_RXD_R<7..0> 9 130 132
I52	ENET_FW_3X		ENET_RX_DV_R 130 132
I53	ENET_FW_3X		ENET_RX_ER_R 130 132
I54	ENET_FW_2X		ENET_RXD<7..0> 9 130 131
I55	ENET_FW_3X		ENET_RX_DV 130 131
I56	ENET_FW_3X		ENET_RX_ER 130 131
I58	ENET_FW_2X		ENET_TXD_R<7..0> 9 130 131
I57	ENET_FW_3X		ENET_TX_EN_R 9 130 131
I59	ENET_FW_3X		ENET_TX_ER_R 9 130 131
I60	ENET_FW_2X		ENET_TXD<7..0> 9 130 132
I61	ENET_FW_3X		ENET_TX_EN 9 130 132
I62	ENET_FW_3X		ENET_TX_ER 9 130 132
I63	ENET_FW_3X		ENET_CRS_R 130 132
I64	ENET_FW_3X		ENET_COL_R 130 132
I65	ENET_FW_3X		ENET_CRS 130 131
I66	ENET_FW_3X		ENET_COL 130 131
I68	ENET_FW_3X		ENET_MDC 131 132
I41	ENET_FW_3X		ENET_MDIO 130 131 132
I42	ENET_FW_3X		ENET_MDIO_R 130 131
I43	ENET_FW_3X		R8405_1 131
I45	ENET_FW_3X		R8405_2 131
I44	ENET_FW_3X		R8407_2 131

Page Notes

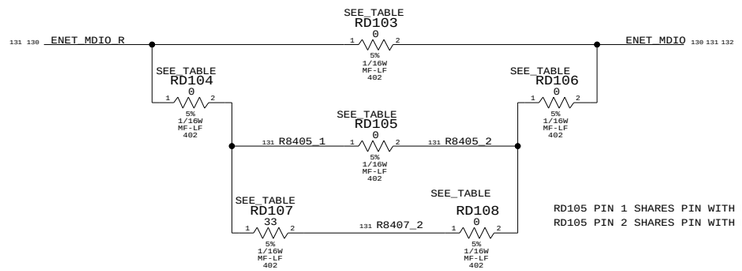
Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



RD103 PIN 1 SHARES PIN WITH RD104 PIN 1
RD103 PIN 2 SHARES PIN WITH RD106 PIN 2



RD105 PIN 1 SHARES PIN WITH RD107 PIN 1
RD105 PIN 2 SHARES PIN WITH RD108 PIN 2

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,0-OHM,402,5%	RD103		ENET_MDIO_DELAY_0
116S0004	3	RES,0-OHM,402,5%	RD104,RD105,RD106		ENET_MDIO_DELAY_2NS
116S0004	3	RES,0-OHM,402,5%	RD104,RD108,RD106		ENET_MDIO_DELAY_4NS
116S0030	1	RES,33-OHM,402,5%	RD107		ENET_MDIO_DELAY_4NS

*

Shasta Ethernet

SYNC_MASTER=Q63 SYNC_DATE=08/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 131 OF 154	

LAST_MODIFIED=Tue Nov 1 12:01:57 2005

DRAWING

TITLE=KILOWHRA

ABBREV=SMDRAWING

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
	0.38mm SPACING		ENET_CLK125M_GBE_REF_R 130 132
	0.38mm SPACING		ENET_CLK125M_RX_R 130 132
	0.38mm SPACING		ENET_CLK25M_TX_R 130 132
	ENET	ENET_MDI0	ENET_MDI_P<0> 132 136
	ENET	ENET_MDI0	ENET_MDI_N<0> 132 136
	ENET	ENET_MDI1	ENET_MDI_P<1> 132 136
	ENET	ENET_MDI1	ENET_MDI_N<1> 132 136
	ENET	ENET_MDI2	ENET_MDI_P<2> 132 136
	ENET	ENET_MDI2	ENET_MDI_N<2> 132 136
	ENET	ENET_MDI3	ENET_MDI_P<3> 132 136
	ENET	ENET_MDI3	ENET_MDI_N<3> 132 136
	0.38mm SPACING		VESTA_CLK25M_XTALI 132
	0.38mm SPACING		VESTA_CLK25M_XTALO 132
	0.38mm SPACING		VESTA_CLK25M_XTALO_R 132

Page Notes

Power aliases required by this page:
- =PP3V3_ENET
- =PP2V5_ENETFW
- =PP1V2_ENETFW

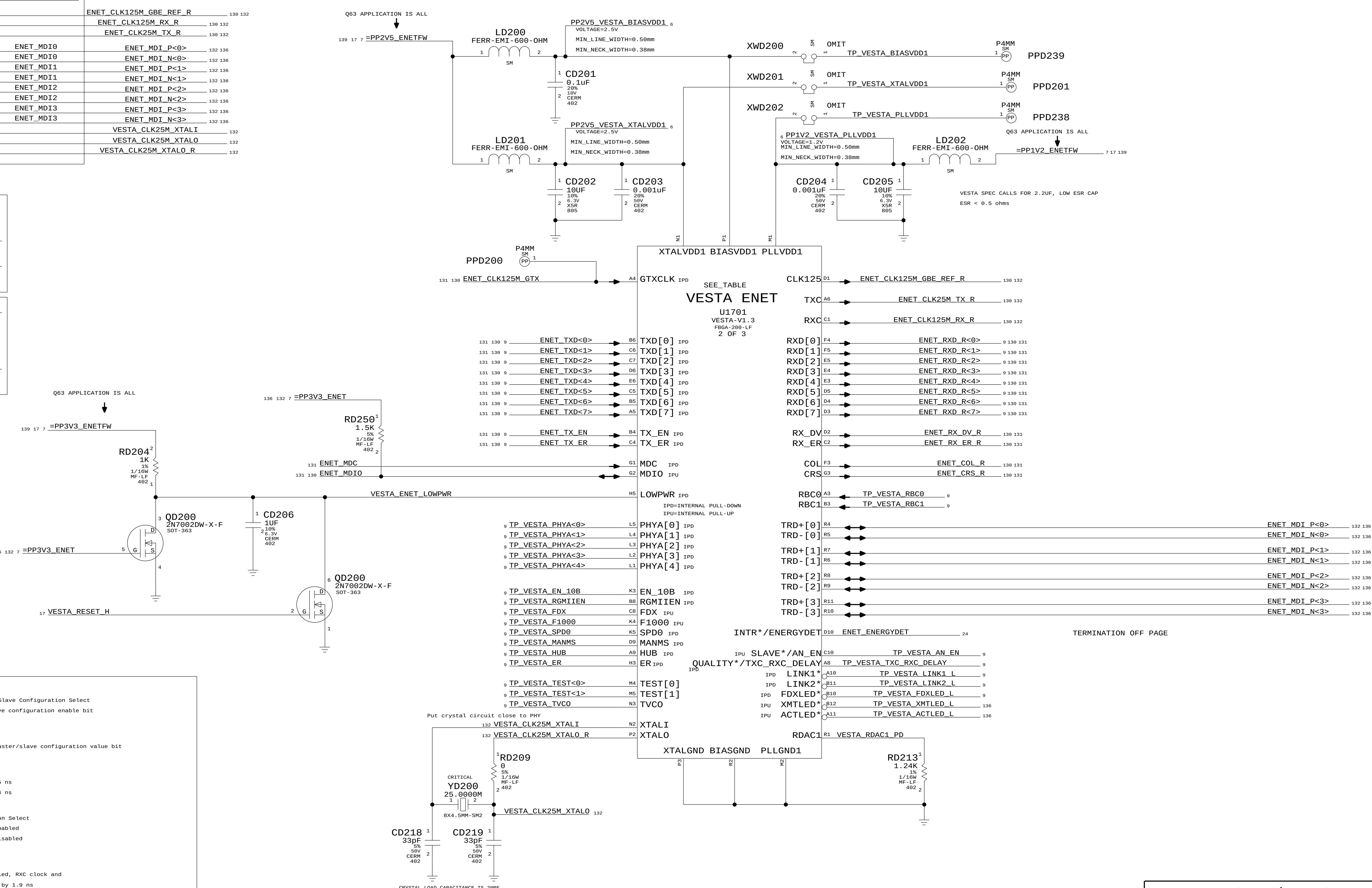
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: ENET

Line To Line: 0.38mm
Length Tolerance: 1.27mm
Primary Max Sep: 0.13mm
Secondary Max Sep: 2.54mm
Secondary Length: 12.70mm

NOTE: Target differential impedance for ENET data pairs is 100 ohms.



Q63 APPLICATION IS ALL
=PP2V5_ENETFW
LD200
FERR-EMI-600-OHM
PP2V5_VESTA_BIASVDD1
VOLTAGE=2.5V
MIN_LINE_WIDTH=0.50mm
MIN_NECK_WIDTH=0.38mm
CD201
0.1uF
XWD200
XWD201
XWD202
OMIT
TP_VESTA_BIASVDD1
TP_VESTA_XTALVDD1
TP_VESTA_PLLVDD1
PPD239
PPD201
PPD238
LD201
PP2V5_VESTA_XTALVDD1
CD202
10UF
CD203
0.001uF
PP1V2_VESTA_PLLVDD1
VOLTAGE=1.2V
LD202
=PP1V2_ENETFW
CD204
0.001uF
CD205
10UF
VESTA SPEC CALLS FOR 2.2UF, LOW ESR CAP
ESR < 0.5 ohms
PPD200
XTALVDD1 BIASVDD1 PLLVDD1
GTXCLK
SEE_TABLE
VESTA ENET
U1701
VESTA-V1.3
FBGA-200-LF
2 OF 3
ENET_CLK125M_GTX
CLK125
TXC
RXC
ENET_CLK125M_GBE_REF_R
ENET_CLK25M_TX_R
ENET_CLK125M_RX_R
ENET_TXD<0>
ENET_TXD<1>
ENET_TXD<2>
ENET_TXD<3>
ENET_TXD<4>
ENET_TXD<5>
ENET_TXD<6>
ENET_TXD<7>
ENET_RXD_R<0>
ENET_RXD_R<1>
ENET_RXD_R<2>
ENET_RXD_R<3>
ENET_RXD_R<4>
ENET_RXD_R<5>
ENET_RXD_R<6>
ENET_RXD_R<7>
ENET_TX_EN
ENET_TX_ER
ENET_RX_DV_R
ENET_RX_ER_R
=PP3V3_ENET
RD250
1.5K
=PP3V3_ENETFW
RD204
1K
ENET_MDC
ENET_MDIO
ENET_COL_R
ENET_CRS_R
VESTA_ENET_LOWPWR
LOWPWR
IPD=INTERNAL PULL-DOWN
IPU=INTERNAL PULL-UP
RBC0
RBC1
TP_VESTA_RBC0
TP_VESTA_RBC1
QD200
2N7002DW-X-F
SOT-363
CD206
1UF
TP_VESTA_PHYA<0>
TP_VESTA_PHYA<1>
TP_VESTA_PHYA<2>
TP_VESTA_PHYA<3>
TP_VESTA_PHYA<4>
ENET_MDI_P<0>
ENET_MDI_N<0>
ENET_MDI_P<1>
ENET_MDI_N<1>
ENET_MDI_P<2>
ENET_MDI_N<2>
ENET_MDI_P<3>
ENET_MDI_N<3>
VESTA_RESET_H
TP_VESTA_EN_10B
TP_VESTA_RGMIIEN
TP_VESTA_FDX
TP_VESTA_F1000
TP_VESTA_SPD0
TP_VESTA_MANMS
TP_VESTA_HUB
TP_VESTA_ER
INTR*/ENERGYDET
ENET_ENERGYDET
TERMINATION OFF PAGE
SLAVE*/AN_EN
TP_VESTA_AN_EN
QUALITY*/TXC_RXC_DELAY
TP_VESTA_TXC_RXC_DELAY
TP_VESTA_LINK1_L
TP_VESTA_LINK2_L
TP_VESTA_FDXLED_L
TP_VESTA_XMTLED_L
TP_VESTA_ACTLED_L
TP_VESTA_TEST<0>
TP_VESTA_TEST<1>
TP_VESTA_TVCO
Put crystal circuit close to PHY
VESTA_CLK25M_XTALI
VESTA_CLK25M_XTALO_R
RDAC1
VESTA_RDAC1_PD
XTALGND BIASGND PLLGND1
RD209
0
RD213
1.24K
CRITICAL
YD200
25.0000M
8X4.5MM-SM2
VESTA_CLK25M_XTALO
CD218
33pF
CD219
33pF
CRYSTAL LOAD CAPACITANCE IS 20PF

Vesta Config Straps:

PHYA<4..0> - PHY Address Select
(Internal Pull-downs)

EN_10B - TBI Interface Select
1 - TBI/RTBI Mode
0 - GMII/RGMII Mode
(Internal Pull-down)

RGMIIEN - RGMII Enable
1 - RGMII/RTBI Mode
0 - GMII/TBI Mode
(Internal Pull-down)

FDX - Full-Duplex Select
Sets manual duplex mode bit
(Internal Pull-up)

F1000 - Speed Select
See table below
(Internal Pull-up)

SPD0 - Speed Select
See table below
(Internal Pull-down)

MANMS - Manual Master/Slave Configuration Select
Sets manual master/slave configuration enable bit
(Internal Pull-down)

HUB - Repeater Select
Sets Hub/DTE bit and master/slave configuration value bit
(Internal Pull-down)

ER - Edge Rate Select
1 - Rise time approx. 5 ns
0 - Rise time approx. 4 ns
(Internal Pull-down)

AN_EN - Auto-Negotiation Select
1 - Auto-negotiation enabled
0 - Auto-negotiation disabled
(Internal Pull-up)

TXC_RXC_DELAY
1 - If RGMII Mode enabled, RXC clock and GTXCLK are delayed by 1.9 ns
0 - No clock delay
(Internal Pull-down)

AN_EN	F1000	SPD0	Description
0	0	0	Force 10BASE-T
0	0	1	Force 100BASE-TX
0	1	X	Force 1000BASE-T (test use only)
1	0	0	Auto-negotiate advertise 10BASE-T
1	0	1	Auto-negotiate advertise 10/100BASE-TX
1	1	0	Auto-negotiate advertise 10/100/1000BASE-T
1	1	1	Auto-negotiate advertise 1000BASE-T

LAST_MODIFIED=Tue Nov 1 13:46:02 2005

Vesta Ethernet PHY

SYNC_MASTER=Q63 SYNC_DATE=08/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE NONE	SHT 132	OF 154

EXTRA CONSTRAINTS TO SUPPLEMENT THE THE MISSING NET PHYSICAL FROM EARLIER PAGE

NET_PHYSICAL_TYPE

U292	ENET	ENET_MDI_P<0>	132 136
U296	ENET	ENET_MDI_N<0>	132 136
U297	ENET	ENET_MDI_P<1>	132 136
U298	ENET	ENET_MDI_N<1>	132 136
U299	ENET	ENET_MDI_P<2>	132 136
U300	ENET	ENET_MDI_N<2>	132 136
U301	ENET	ENET_MDI_P<3>	132 136
U302	ENET	ENET_MDI_N<3>	132 136

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0253	1	CON,RJ-45 7 DEGRESS	JD600	CRITICAL	17_INCH_LCD
514-0254	1	CON,RJ-45 7 DEGRESS	JD600	CRITICAL	20_INCH_LCD

PUT DEVELOPMENT LEDS ON TOP SIDE OF BOARD

136 132 7 =PP3V3_ENET
DEVELOPMENT
RD601 330 5% 1/10W MF-LF 603
LED8700_P 9
DEVELOPMENT
LEDD600
GREEN-3.6MCD 2.0X1.25MM-SM

132 TP_VESTA_XMTLED_L = VESTA_XMTLED_L
MAKE_BASE=TRUE

LD600
FERR-EMI-600-OHM
7 =PP2V5_ENET
PP2V5_ENET_CTAP
MIN_LINE_WIDTH=0.150mm
MIN_NECK_WIDTH=0.138mm
VOLTAGE=2.5V
CD600 0.1UF 20% 10V CERM 402
CD601 0.1UF 20% 10V CERM 402
7 GND_CHASSIS_RJ45
CD604 0.001UF 10% 50V CERM 402

ENET TERMINATION

PLACE THESE PARTS NEAR VESTA

136 132 ENET_MDI_P<0>
136 132 ENET_MDI_N<0>
RD604 49.9 1% 1/16W MF-LF 402
RD605 49.9 1% 1/16W MF-LF 402
ENET_MDI0
136 132 ENET_MDI_P<1>
136 132 ENET_MDI_N<1>
CD606 0.01UF 20% 16V CERM 402
RD606 49.9 1% 1/16W MF-LF 402
RD607 49.9 1% 1/16W MF-LF 402
ENET_MDI1
136 132 ENET_MDI_P<2>
136 132 ENET_MDI_N<2>
RD608 49.9 1% 1/16W MF-LF 402
RD609 49.9 1% 1/16W MF-LF 402
CD607 0.01UF 20% 16V CERM 402
ENET_MDI2
136 132 ENET_MDI_P<3>
136 132 ENET_MDI_N<3>
CD608 0.01UF 20% 16V CERM 402
RD610 49.9 1% 1/16W MF-LF 402
RD611 49.9 1% 1/16W MF-LF 402
ENET_MDI3
CD609 0.01UF 20% 16V CERM 402

(514-0253)
OMIT
JD600
JFM38V10-0112-4F
F-ANG-TH

PRIMARY
13
11
5 ENET_CTAP
6 ENET_CTAP
1 MDI_0+
2 MDI_0-
3 MDI_1+
4 MDI_1-
7 MDI_2+
8 MDI_2-
9 MDI_3+
10 MDI_3-
12
RJ45 CHIP SIDE

1CT:1CT
75 OHM
SECONDARY
J1
J2
J3
J4
J5
J6
J7
J8
RJ45 CABLE SIDE

SHIELD 1000PF, 2000V

CD605 0.001UF 10% 50V CERM 402

136 132 7 =PP3V3_ENET
DEVELOPMENT
RD603 330 5% 1/10W MF-LF 603
LED8701_P 9
DEVELOPMENT
LEDD601
GREEN-3.6MCD 2.0X1.25MM-SM

132 TP_VESTA_ACTLED_L = VESTA_ACTLED_L
MAKE_BASE=TRUE

SPARE GND VIAS FOR LAYER TRAVERSALS DURING ROUTING

ZHD690 HOLE-VIA
ZHD691 HOLE-VIA
ZHD692 HOLE-VIA
ZHD693 HOLE-VIA

ETHERNET CONNECTOR

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 136 OF 154	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	ENET_FW_2X	
fdi	ENET_FW_3X	
	ENET_FW_3X	
fdr	ENET_FW_2X	
fdm	ENET_FW_3X	
	ENET_FW_3X	
	ENET_FW_3X	
	ENET_FW_3X	
	0.38mm_SPACING	
	0.38mm_SPACING	
	0.38mm_SPACING	

FW_DATA<7..0> 138 139
FW_CTL_S<1..0> 138 139
FW_CTL<1..0> 138 139
FW_DATA_R<7..0> 139
FW_CTL_R<1..0> 139
FW_LPS 138 139
FW_LREQ 138 139
FW_PINT 138 139
FW_CLK98M_LCLK 138 139
FW_CLK98M_PCLK 138 139
FW_CLK98M_LCLK_R 138

Page Notes

Power aliases required by this page:
- _PP2V5_PWRON_SB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

119 24 23 7 =PP2V5_PWRON_SB

CD800 0.1uF 20% 10V CERM 402
CD801 0.1uF 20% 10V CERM 402
CD802 0.1uF 20% 10V CERM 402

FWVDDP

U2300
SHASTA
V1.1
BGA-LF
SEE TABLE (7 OF 8)

FIREWIRE

PHY_DATA_0_H	N4	FW_DATA<0>	138 139
PHY_DATA_1_H	P5	FW_DATA<1>	138 139
PHY_DATA_2_H	N1	FW_DATA<2>	138 139
PHY_DATA_3_H	M7	FW_DATA<3>	138 139
PHY_DATA_4_H	N6	FW_DATA<4>	138 139
PHY_DATA_5_H	L1	FW_DATA<5>	138 139
PHY_DATA_6_H	M3	FW_DATA<6>	138 139
PHY_DATA_7_H	L2	FW_DATA<7>	138 139
PHY_CTL_0_H	N2	139 138 FW_CTL_S<0>	RD801 0 5% 1/16W MF-LF 402 FW_CTL<0> 138 139
PHY_CTL_1_H	N3	139 138 FW_CTL_S<1>	RD802 0 5% 1/16W MF-LF 402 FW_CTL<1> 138 139
PHY_LPS_H	P6	FW_LPS	138 139
PHY_LREQ_H	P1	FW_LREQ	138 139
PHY_SCLK_H	P2	139 138 FW_CLK98M_PCLK	
PHY_PINT_L	P3	139 138 FW_PINT	
PHY_LCLK_H	R1	138 FW_CLK98M_LCLK_R	RD800 22 5% 1/16W MF-LF 402 FW_CLK98M_LCLK 138 139
PHY_LINKON_L	N7	FW_LINKON	139

Shasta FireWire

SYNC_MASTER=Q63 SYNC_DATE=08/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 138 OF 154	

LAST_MODIFIED=Tue Nov 1 13:46:04 2005

DRAWING

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
(PROVIDED BY LINK PAGE)		0.38mm SPACING		FW_CLK98M_PCLK_R 139
	FW	FW	FW_TPA0	FW_TPA_P<0> 139 140
	FW	FW	FW_TPA0	FW_TPA_N<0> 139 140
	FW	FW	FW_TPB0	FW_TPB_P<0> 139 140
	FW	FW	FW_TPB0	FW_TPB_N<0> 139 140
	FW	FW	FW_TPA1	FW_TPA_P<1> 139 140
	FW	FW	FW_TPA1	FW_TPA_N<1> 139 140
	FW	FW	FW_TPB1	FW_TPB_P<1> 139 140
	FW	FW	FW_TPB1	FW_TPB_N<1> 139 140
ETHERNET SPACING TO ROUTE ON LAYER 6	FW	FW	FW_TPA2	FW_TPA_P<2> 139 140
	FW	FW	FW_TPA2	FW_TPA_N<2> 139 140
	FW	FW	FW_TPB2	FW_TPB_P<2> 139 140
	FW	FW	FW_TPB2	FW_TPB_N<2> 139 140
		0.38mm SPACING		VESTA_CLK24M_XTALI 139
		0.38mm SPACING		VESTA_CLK24M_XTALO 139
		0.38mm SPACING		VESTA_CLK24M_XTALO_R 139
	FW_CTL			FW_CTL_S<1..0> 138
	FW_CTL			FW_CTL<1..0> 138 139
	FW_CTL			FW_CTL_R<1..0> 138 139

Page Notes

Power aliases required by this page:
- =PPFW_PHY
- =PP3V3_FW
- =PP3V3_ENETFW
- =PP2V5_ENETFW
- =PP1V2_ENETFW

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- VESTA_DS_ONLY_EN0
  If stuffed, adds external pull-up to counter internal pull-down in Vesta.
  See straps table for more information.
- VESTA_PWR_CLASS_0
  If stuffed, adds external pull-down to counter internal pull-up in Vesta.
  See straps table for more information.

Net Spacing Type: FW

NOTE: Target differential impedance for FW data pairs is 110 ohms.

VESTA CONFIG STRAPS:

FW_PWR_CLASS_MSB - FIREWIRE POWER CLASS
1 - Sets Power Class to 0x4
0 - Sets Power Class to 0x0
(Internal Pull-up)

FW_DS_ONLY_P0 - PORT 0 DATA/STROBE mode only
1 - Port 0 Data/Strobe mode only
0 - Port 0 Bilingual mode
(Internal Pull-down)

ESDET[0]
1=PORTS 1 AND 2 DS ONLY
0=PARTS 1 AND 2 BI-LINGUAL
ESDET[1]
1=PORT 1 PRESENT
0=PORT 1 NOT PRESENT
ESDET[2]
1=PORT 2 PRESENT
0=PORT 2 NOT PRESENT

CRYSTAL LOAD CAPACITANCE IS 12PF

LAST_MODIFIED=Tue Nov 1 13:46:05 2005

Vesta FireWire PHY

SYNC_MASTER=Q63 SYNC_DATE=08/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 139 OF 154	

NET_TYPE SPACING	PHYSICAL	DIFFERENTIAL_PAIR		
T401 FW	FW	FW_TPA0_FL	FW_PORT0_TPA_P_FL	140
T400 FW	FW	FW_TPA0_FL	FW_PORT0_TPA_N_FL	140
T402 FW	FW	FW_TPB0_FL	FW_PORT0_TPB_P_FL	140
T403 FW	FW	FW_TPB0_FL	FW_PORT0_TPB_N_FL	140
T493 FW	FW	FW_TPA1_FL	FW_PORT1_TPA_P_FL	140
T495 FW	FW	FW_TPA1_FL	FW_PORT1_TPA_N_FL	140
T497 FW	FW	FW_TPB1_FL	FW_PORT1_TPB_P_FL	140
T496 FW	FW	FW_TPB1_FL	FW_PORT1_TPB_N_FL	140

7 =PP12V_ALL_FW

8 WATTS MAX
12 VOLTS

RE056 1.3 20% 1W FF 2512
PP12V_FW MIN_LINE_WIDTH=0.8MM MIN_NECK_WIDTH=0.25MM VOLTAGE=12V MAKE_BASE=TRUE
I443 =PPFW_PHY 139
TO FW CDS PIN (CABLE POWER DETECT)

DE000 MURS320XXG SMC
FW_VP_R MIN_LINE_WIDTH=0.8MM MIN_NECK_WIDTH=0.25MM MAKE_BASE=TRUE VOLTAGE=24V
CE009 0.1UF 10% 50V X7R 603-1
FW_VP MAX IS 24V

CRITICAL
RE002 1.3 20% 1W FF 2512
FW_VP MIN_LINE_WIDTH=0.8MM MIN_NECK_WIDTH=0.25MM VOLTAGE=24V

FE002 0.75AMP-13.2V MINISMD-LF
PPFW_PORT0_VP MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=24V

DESIGNED WITH INTENTION TO RESIZE FUSE LIMITS EQUAL FW SPEC 1.5A LIMIT
FE000 1.5AMP-33V SM-LF
PPFW_PORT1_VP MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=24V
POSSIBLE CURRENT SHARING SCENARIO
KCL = CABLE POWER + SYSTEM POWER = > 1.5 AMPS

Termination

Place close to FireWire PHY

VOLTAGE=1.86V
139 FW_TPBIAS<1> VOLTAGE=1.86V
139 FW_TPBIAS<0> VOLTAGE=1.86V
CE050 1UF 10% 6.3V CERM 402
CE060 1UF 10% 6.3V CERM 402

RE050 56.2 1% 1/10W MF-LF 402
RE051 56.2 1% 1/16W MF-LF 402
RE060 56.2 1% 1/16W MF-LF 402
RE061 56.2 1% 1/16W MF-LF 402

139 FW_TPA_P<0> — FW_PORT0_TPA_P 140
139 FW_TPA_N<0> — FW_PORT0_TPA_N 140
139 FW_TPB_P<0> — FW_PORT0_TPB_P 140
139 FW_TPB_N<0> — FW_PORT0_TPB_N 140
MAKE_BASE=TRUE
139 FW_TPA_P<1> — FW_PORT1_TPA_P 140
139 FW_TPA_N<1> — FW_PORT1_TPA_N 140
139 FW_TPB_P<1> — FW_PORT1_TPB_P 140
139 FW_TPB_N<1> — FW_PORT1_TPB_N 140
MAKE_BASE=TRUE

RE052 56.2 1% 1/10W MF-LF 402
RE053 56.2 1% 1/16W MF-LF 402
RE062 56.2 1% 1/16W MF-LF 402
RE063 56.2 1% 1/16W MF-LF 402

FW_TPA_C<0> VOLTAGE=0V
CE054 270pF 5% 25V CERM 402
RE054 4.99K 1% 1/16W MF-LF 402
FW_TPA_C<1> VOLTAGE=0V
CE064 270pF 5% 25V CERM 402
RE064 4.99K 1% 1/16W MF-LF 402

3rd TPA/TPB pair unused

139 FW_TPBIAS<2> — NC_FW_TPBIAS2 MAKE_BASE=TRUE NO_TEST=YES
139 FW_TPA_P<2> — NC_FW_TPA_P2 MAKE_BASE=TRUE NO_TEST=YES
139 FW_TPA_N<2> — NC_FW_TPA_N2 MAKE_BASE=TRUE NO_TEST=YES
139 FW_TPB_P<2> — FW_TPB2_PD MAKE_BASE=TRUE NO_TEST=YES
139 FW_TPB_N<2> — FW_TPB2_PD MAKE_BASE=TRUE NO_TEST=YES
RE070 1K 5% 1/10W MF-LF 402

ESD Rail

CALCULATION = 220 OHMS, THERE'S ALREADY A 215 IN THE DESIGN, SO I'M USING 215 INSTEAD

7 =PP3V3_FW — RE090 215 1% 1/10W MF-LF 402 — PP3V3_FW_ESD_F VOLTAGE=3.3V MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm — LE090 400-OHM-EMI SM-1 — PP3V3_FW_ESD 140 VOLTAGE=3.3V MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm

DE090 SOT23 BZX84C2V7-X-F

[LATE VG NOTES]
CURRENT THROUGH THE BIAS RESISTOR SHOULD BE 5MA FOR A VOLTAGE DROP TO 2.2V
IT IS 2.2V INSTEAD OF 2.7V BECAUSE THE SNAPBACK ESD DIODES HAVE A .5V DROP

ZHE090 HOLE-VIA
ZHE091 HOLE-VIA
ZHE092 HOLE-VIA
ZHE093 HOLE-VIA

SPARE GND VIAS FOR LAYER TRAVERSALS DURING ROUTING

"Snapback" & "Late VG" Protection

140 PP3V3_FW_ESD
DPE010 BAV99DW-X-F SOT-363
CE010 0.001UF 10% 50V CERM 402
CE011 0.001UF 10% 50V CERM 402

140 FW_PORT0_TPA_P
140 FW_PORT0_TPA_N
140 FW_PORT0_TPB_P
140 FW_PORT0_TPB_N
FLE010 120-OHM 2012 SYM_VER-1
FLE011 120-OHM 2012 SYM_VER-1

140 PP3V3_FW_ESD
DPE011 BAV99DW-X-F SOT-363
CE012 0.001UF 10% 50V CERM 402
CE013 0.001UF 10% 50V CERM 402

LE010 FERR-160-OHM 1206-LF
PORT 0 1394A OMIT
JE000 UF01613-M33-4F F-ST-TH

140 FW_PORT0_TPA_P_FL — TPO (TPA+)
140 FW_PORT0_TPA_N_FL — TPO# (TPA-)
140 FW_PORT0_TPB_P_FL — TPI (TPB+)
140 FW_PORT0_TPB_N_FL — TPI# (TPB-)
PPFW_PORT0_VP_FL — VP
VGND
7 8 9 10

FW_VP MAX IS 24V
CE015 0.1UF 10% 50V X7R 603-1
CE016 0.01UF 20% 16V CERM 402

514-0251 20_INCH_VERSION SHOWN
GND_CHASSIS_FIREWIRE 7 140

"Snapback" & "Late VG" Protection

140 PP3V3_FW_ESD
DPE020 BAV99DW-X-F SOT-363
CE020 0.001UF 10% 50V CERM 402
CE021 0.001UF 10% 50V CERM 402

140 FW_PORT1_TPA_P
140 FW_PORT1_TPA_N
140 FW_PORT1_TPB_P
140 FW_PORT1_TPB_N
FLE020 120-OHM 2012 SYM_VER-1
FLE021 120-OHM 2012 SYM_VER-1

140 PP3V3_FW_ESD
DPE021 BAV99DW-X-F SOT-363
CE022 0.001UF 10% 50V CERM 402
CE023 0.001UF 10% 50V CERM 402

PPFW_PORT1_VP 140
LE020 FERR-160-OHM 1206-LF
PORT 1 1394A OMIT
JE001 UF01613-M33-4F F-ST-TH

140 FW_PORT1_TPA_P_FL — TPO (TPA+)
140 FW_PORT1_TPA_N_FL — TPO# (TPA-)
140 FW_PORT1_TPB_P_FL — TPI (TPB+)
140 FW_PORT1_TPB_N_FL — TPI# (TPB-)
PPFW_PORT1_VP_FL — VP
VGND
7 8 9 10

CE025 0.1UF 10% 50V X7R 603-1
CE026 0.01UF 20% 16V CERM 402

514-0251 20_INCH_VERSION SHOWN
GND_CHASSIS_FIREWIRE 7 140

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0248	1	CON,1394A 7 DEGREES	JE000	CRITICAL	17_INCH_LCD
514-0248	1	CON,1394A 7 DEGREES	JE001	CRITICAL	17_INCH_LCD
514-0251	1	CON,1394A 7 DEGREES	JE000	CRITICAL	20_INCH_LCD
514-0251	1	CON,1394A 7 DEGREES	JE001	CRITICAL	20_INCH_LCD

FIREWIRE CONNECTORS

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6863 | REV. F

SCALE NONE | SHT 140 OF 154

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR	
	USB2	USB2_S	USB2_0	USB2_P<0>
	USB2	USB2_S	USB2_0	USB2_N<0>
	USB2	USB2_S	USB2_1	USB2_P<1>
	USB2	USB2_S	USB2_1	USB2_N<1>
	USB2	USB2_S	USB2_2	USB2_P<2>
	USB2	USB2_S	USB2_2	USB2_N<2>
	USB2	USB2_S	USB2_3	USB2_P<3>
	USB2	USB2_S	USB2_3	USB2_N<3>
	USB2	USB2_S	USB2_4	USB2_P<4>
	USB2	USB2_S	USB2_4	USB2_N<4>
	0.38mm SPACING			NEC_CLK30M_XT1
	0.38mm SPACING			NEC_CLK30M_XT2
	0.38mm SPACING			NEC_CLK30M_XT2_R

Page Notes

Power aliases required by this page:
- =PP3V3_PWRON_USB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: USB2

Line To Line: 0.50mm
Length Tolerance: 1.27mm
Primary Max Sep: 0.19mm
Secondary Max Sep: 2.54mm
Secondary Length: 12.70mm

NOTE: Target differential impedance for USB2 data pairs is 90 ohms.

Q63 USB PORT ALLOCATION
REAR USB (PORT #0)
FRONT PANEL USB (PORT #1)
REAR USB (PORT #2)
REAR USB (PORT #3)

U2300 SHASTA V1.1 BGA-LF (8 OF 8)

NC0 P7 TP_SB<0> 6
NC1 P8 TP_SB<1> 6
NC2 R3 TP_SB<2> 6
NC3 R4 TP_SB<3> 6
NC4 R5 TP_SB<4> 6
NC5 R6 TP_SB<5> 6
NC6 R7 TP_SB<6> 6
NC7 R8 TP_SB<7> 6
NC8 T1 TP_SB<8> 6
NC9 T2 TP_SB<9> 6
NC10 T3 TP_SB<10> 6
NC11 T4 TP_SB<11> 6
NC12 T5 TP_SB<12> 6
NC13 T6 TP_SB<13> 6
NC14 T7 TP_SB<14> 6
NC15 T8 TP_SB<15> 6
NC16 U1 TP_SB<16> 6
NC17 U2 TP_SB<17> 6
NC18 U3 TP_SB<18> 6
NC19 U4 TP_SB<19> 6
NC20 U5 TP_SB<20> 6
NC21 U6 TP_SB<21> 6
NC22 V1 TP_SB<22> 6
NC23 V2 TP_SB<23> 6
NC24 V3 TP_SB<24> 6
NC25 V4 TP_SB<25> 6
NC26 W1 TP_SB<26> 6
NC27 W3 TP_SB<27> 6
NC28 Y1 TP_SB<28> 6
NC29 Y3 TP_SB<29> 6

USB2_P<0> 142 143
USB2_N<0> 142 143
USB2_P<1> 142 143
USB2_N<1> 142 143
USB2_P<2> 142 143
USB2_N<2> 142 143
USB2_P<3> 142 143
USB2_N<3> 142 143
USB2_P<4> 142 143
USB2_N<4> 142 143
NEC_CLK30M_XT1 142
NEC_CLK30M_XT2 142
NEC_CLK30M_XT2_R 142

LE235 FERR-EMI-100-OHM SM
PP3V3_PWRON_NEC_AVDD 6 VOLTAGE=3.3V
MIN_LINE_WIDTH=0.50mm
MIN_NECK_WIDTH=0.2MM
XWE200 OMIT SM
TP_NEC_AVDD
P4MM SM PPE2000
RE235 4.7 5% 1/10W MF-LF 603
CE235 10UF 10% X-3V X5R 805
CE236 0.1uF 20% 10V CERM 402
CE237 0.1uF 20% 10V CERM 402
MINIMIZE TRACE LENGTH OF CAPS FROM AVDD TO AVSS PINS
GND_NEC_AVSS_R 6 142
145 144 142 7 =PP3V3_PWRON_USB
CE220 10UF 10% X-3V X5R 805
CE221 CE222 CE223 CE224 CE225 0.1uF 20% 10V CERM 402
CE226 CE227 CE228 CE229 CE230 0.1uF 20% 10V CERM 402
P2 P3 P12 A13 A12 A3 E2 N8 L13 J13 H13 F13 D13 G12 H4 D7
VDD
N10 N12
AVDD
CRITICAL
UC200 NEC_UPD720101_USB2 FBGA-LF

RSDM1 M14 143 USB_NEC_N<0>
DM1 M13 (USB2_Nc0s)
DP1 L14 (USB2_Pc0s)
RSDP1 K13 143 USB_NEC_P<0>
RE200 36 1% 1/10W MF-LF 402
RE201 36 1% 1/10W MF-LF 402
USB2_N<0> 142 143
USB2_P<0> 142 143

P4MM SM PPE2002
RSDM2 K14 143 USB_NEC_N<1>
DM2 K12 (USB2_Nc1s)
DP2 J14 (USB2_Pc1s)
RSDP2 J12 143 USB_NEC_P<1>
RE202 36 1% 1/10W MF-LF 402
RE203 36 1% 1/10W MF-LF 402
USB2_N<1> 142 143
USB2_P<1> 142 143

P4MM SM PPE2001
RSDM3 H11 143 USB_NEC_N<2>
DM3 G11 (USB2_Nc2s)
DP3 G13 (USB2_Pc2s)
RSDP3 G14 143 USB_NEC_P<2>
RE204 36 1% 1/10W MF-LF 402
RE205 36 1% 1/10W MF-LF 402
USB2_N<2> 142 143
USB2_P<2> 142 143
40.2 OHM RESISTORS ON PORT 2 FOR EVALUATION

RSDM4 F12 143 USB_NEC_N<3>
DM4 F14 (USB2_Nc3s)
DP4 E12 (USB2_Pc3s)
RSDP4 E14 143 USB_NEC_P<3>
RE206 36 1% 1/10W MF-LF 402
RE207 36 1% 1/10W MF-LF 402
USB2_N<3> 142 143
USB2_P<3> 142 143

RSDM5 E13 143 USB_NEC_N<4>
DM5 D14 (USB2_Nc4s)
DP5 C13 (USB2_Pc4s)
RSDP5 C14 143 USB_NEC_P<4>
RE208 36 1% 1/10W MF-LF 402
RE209 36 1% 1/10W MF-LF 402
USB2_N<4> 142 143
USB2_P<4> 142 143
BLUTOOTH CONNECTOR,(PORT #4)

145 144 142 7 =PP3V3_PWRON_USB
RE210 33K 5% 1/16W MF-LF 402
RPE210 10K 5% 1/16W SM-LF
143 USB2_OC<0> (USB2_OC<0>) B12 OCI1
143 USB2_OC<1> (USB2_OC<1>) B11 OCI2
143 USB2_OC<2> (USB2_OC<2>) B10 OCI3
USB2_OC<3> (USB2_OC<3>) A10 OCI4
USB2_OC<4> (USB2_OC<4>) B9 OCI5
143 USB2_PWREN<0> C12 PPON1
143 USB2_PWREN<1> A11 PPON2
143 USB2_PWREN<2> C11 PPON3
143 USB2_PWREN<3> C10 PPON4
143 USB2_PWREN<4> A9 PPON5

145 144 142 7 =PP3V3_PWRON_USB
RE240 1.5K 5% 1/16W MF-LF 402
RE241 1.5K 5% 1/16W MF-LF 402
NEC_NC1_PU P6 NC1
NEC_NC2_PU M6 NC2

142 NEC_CLK30M_XT1 L9 XT1/SCLK
142 NEC_CLK30M_XT2_R P8 XT2
RE245 100 1% 1/16W MF-LF 402
CRITICAL
YE245 30.0000M 8X4.5MM-SM1
NEC_CLK30M_XT2 142
CE245 22pF 5% 50V CERM 402
CE246 22pF 5% 50V CERM 402
SPEC SHOWS LOAD CAPACITANCE OF 16PF

B1 N1 P10 N14 H14 B14 A2 B2 N2 N13 B13 M11 L12 H12 D12 G4 J11 F11 D8
VSS
XWE201 SM OMIT
P13 M12 N11
AVSS
AVSS(R)
Tie to GND at ball N11
RREF P11 NEC_RREF_PD
RE238 9.09K 1% 1/10W MF-LF 402
MINIMIZE TRACE LENGTH TO PINS
GND_NEC_AVSS_R 6 142 VOLTAGE=0V
MIN_LINE_WIDTH=0.50mm
MIN_NECK_WIDTH=0.2MM

USB Host Interfaces

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 142 OF 154	

LAST_MODIFIED=Tue Nov 1 13:46:07 2005
DRAWING
TITLE=KILOHANA
ABBREV=DRAWING

Page Notes

Power aliases required by this page:
- _PP5V_PWRON_USB
- _PP5V_PWRON_UDASH
- _PP3V3_PWRON_UDASH
- _PP3V3_PWRON_BT

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the USB pairs to their appropriate destinations and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

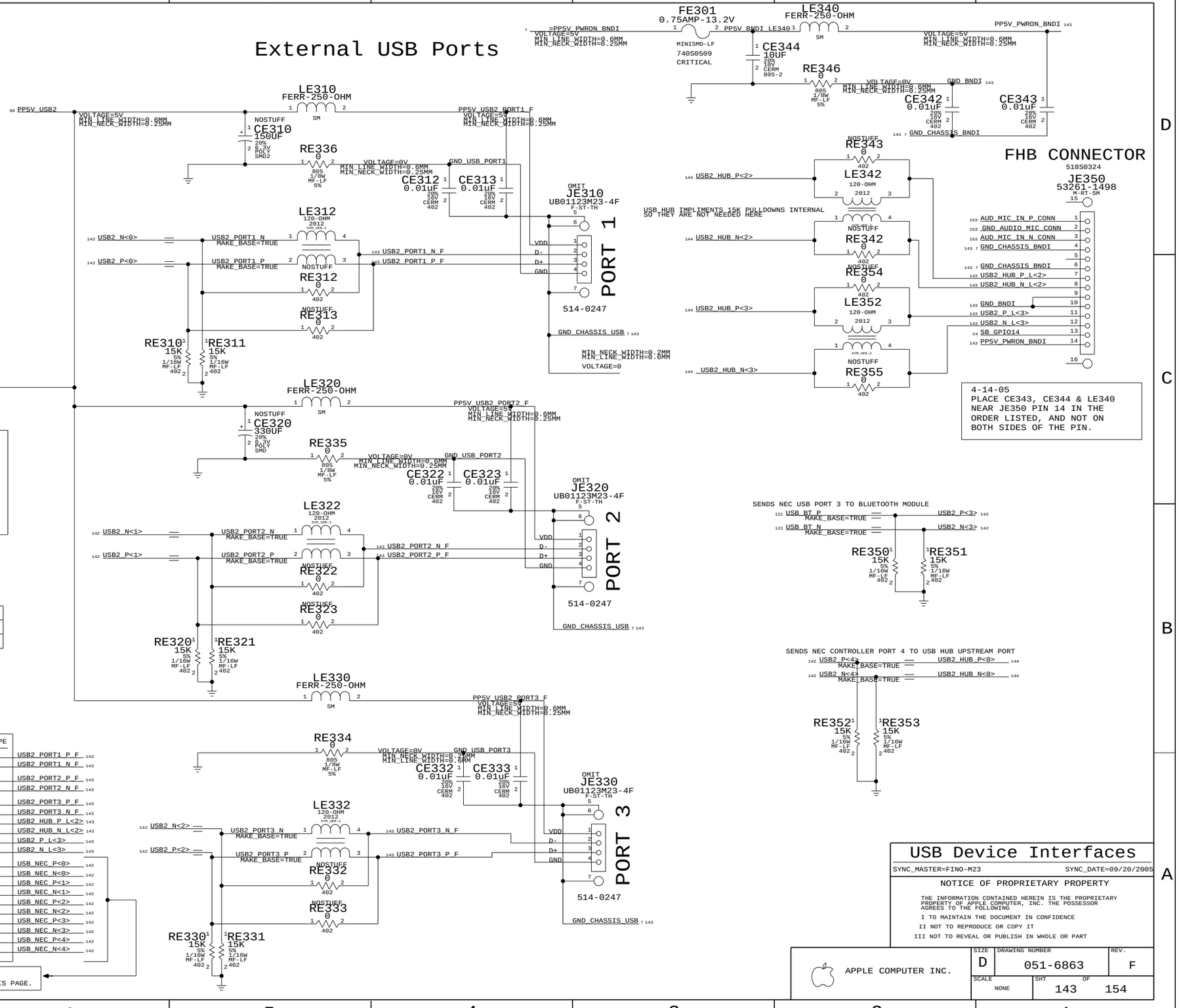
NOTE: USB pairs are NOT constrained on this page. It is assumed that the USB Host Controller page will provide the appropriate constraints to apply to entire USB D+/D- XNets.

neoBorg Implementation

NOTE: This design does not provide power control on USB ports 2-4. Rename USB controller outputs to indicate single-pin connections.

- USB2_PWREN<0> — TP_USB2_PWREN<0> MAKE_BASE=TRUE
- USB2_PWREN<1> — TP_USB2_PWREN<1> MAKE_BASE=TRUE
- USB2_PWREN<2> — TP_USB2_PWREN<2> MAKE_BASE=TRUE
- USB2_PWREN<3> — TP_USB2_PWREN<3> MAKE_BASE=TRUE
- USB2_PWREN<4> — TP_USB2_PWREN<4> MAKE_BASE=TRUE

External USB Ports



USB HUB IMPLIMENTS 15K PULLDOWNS INTERNAL SO THEY ARE NOT NEEDED HERE

SENDS NEC USB PORT 3 TO BLUETOOTH MODULE

SENDS NEC CONTROLLER PORT 4 TO USB HUB UPSTREAM PORT

4-14-05
PLACE CE343, CE344 & LE340 NEAR JE350 PIN 14 IN THE ORDER LISTED, AND NOT ON BOTH SIDES OF THE PIN.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0294	3	USB RECEPTACLE,4P,UB1123-M23B-4F	JE310,JE320,JE330	CRITICAL	17_INCH_LCD
514-0295	3	USB RECEPTACLE,4P,UB1123-M33B-4F	JE310,JE320,JE330	CRITICAL	20_INCH_LCD

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE	
PROVIDED BY USB CONTROLLER	USB2	USB2_PORT1_F	USB2	USB2_PORT1_P_F
	USB2	USB2_PORT1_F	USB2	USB2_PORT1_N_F
	USB2	USB2_PORT2_F	USB2	USB2_PORT2_P_F
	USB2	USB2_PORT2_F	USB2	USB2_PORT2_N_F
	USB2	USB2_PORT3_F	USB2	USB2_PORT3_P_F
	USB2	USB2_PORT3_F	USB2	USB2_PORT3_N_F
	USB2	USB2_HUB_F	USB2	USB2_HUB_P_L<2>
	USB2	USB2_HUB_F	USB2	USB2_HUB_N_L<2>
	USB2	USB2_BNDI_F	USB2	USB2_P_L<3>
	USB2	USB2_BNDI_F	USB2	USB2_N_L<3>
	USB2	USB2_0_IC	USB2	USB_NEC_P<0>
	USB2	USB2_0_IC	USB2	USB_NEC_N<0>
	USB2	USB2_1_IC	USB2	USB_NEC_P<1>
	USB2	USB2_1_IC	USB2	USB_NEC_N<1>
	USB2	USB2_2_IC	USB2	USB_NEC_P<2>
	USB2	USB2_2_IC	USB2	USB_NEC_N<2>
	USB2	USB2_3_IC	USB2	USB_NEC_P<3>
	USB2	USB2_3_IC	USB2	USB_NEC_N<3>
	USB2	USB2_4_IC	USB2	USB_NEC_P<4>
	USB2	USB2_4_IC	USB2	USB_NEC_N<4>

DUE TO THESE NETS ARE ON A Q63 SHARED PAGE 124, THESE PROPERTIES FOR M23/M33 WERE PLACED ON THIS PAGE.

USB Device Interfaces

SYNC_MASTER=FINO-M23 SYNC_DATE=09/20/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 143 OF 154	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0257	1	USX2006-NU-01 CUSTOM MASK	UE400	CRITICAL	CARD_READER

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR	
IN	USB2	USB2	USB2_HUB_1	USB2_HUB_P<1>
IN	USB2	USB2	USB2_HUB_1	USB2_HUB_N<1>
IN	USB2	USB2	USB2_HUB_2	USB2_HUB_P<2>
IN	USB2	USB2	USB2_HUB_2	USB2_HUB_N<2>
IN	USB2	USB2	USB2_HUB_3	USB2_HUB_P<3>
IN	USB2	USB2	USB2_HUB_3	USB2_HUB_N<3>
IN	0.38MM SPACING			XTAL_IN_CARD_READER
IN	0.38MM SPACING			XTAL_OUT_CARD_READER
IN	0.38MM SPACING			XTAL_OUT_CARD_READER_R
IN	0.38MM SPACING			XTAL_IN_USB_HUB
IN	0.38MM SPACING			XTAL_OUT_USB_HUB
IN	0.38MM SPACING			XTAL_OUT_USB_HUB_R

Flash Media Ctrl

SYNC_MASTER=FINO-M23 SYNC_DATE=09/27/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

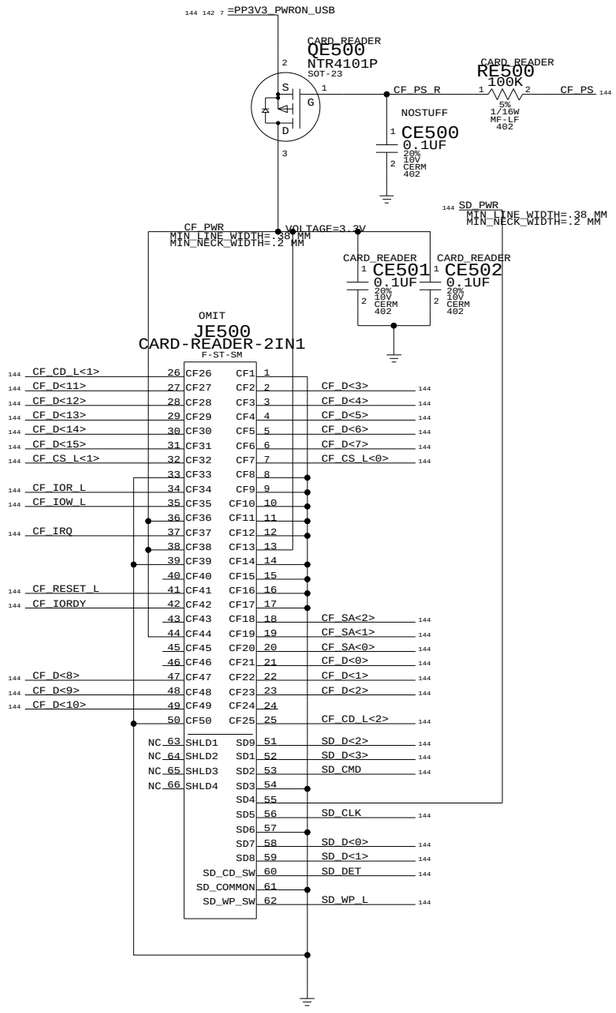
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 144 OF 154	

IF USING THE CARD READER, MUST CHANGE THESE BOM OPTIONS TO:

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION	
512S0010	1	CONN, MEDIA CARD M23	JE500	CRITICAL	CARD_READER	17_INCH_LCD
512S0012	1	CONN, MEDIA CARD M33	JE500	CRITICAL	CARD_READER	20_INCH_LCD



WRITE PROTECT AND CARD DETECT SWITCHES

CARD STATUS	WRITE PROTECT	WRITE ENABLE	CARD DETECT
NOT INSERTED	OPEN	OPEN	OPEN
FULLY INSERTED	OPEN	CLOSE	CLOSE

Flash Connector

SYNC_MASTER=FINO-M23 SYNC_DATE=09/27/2005

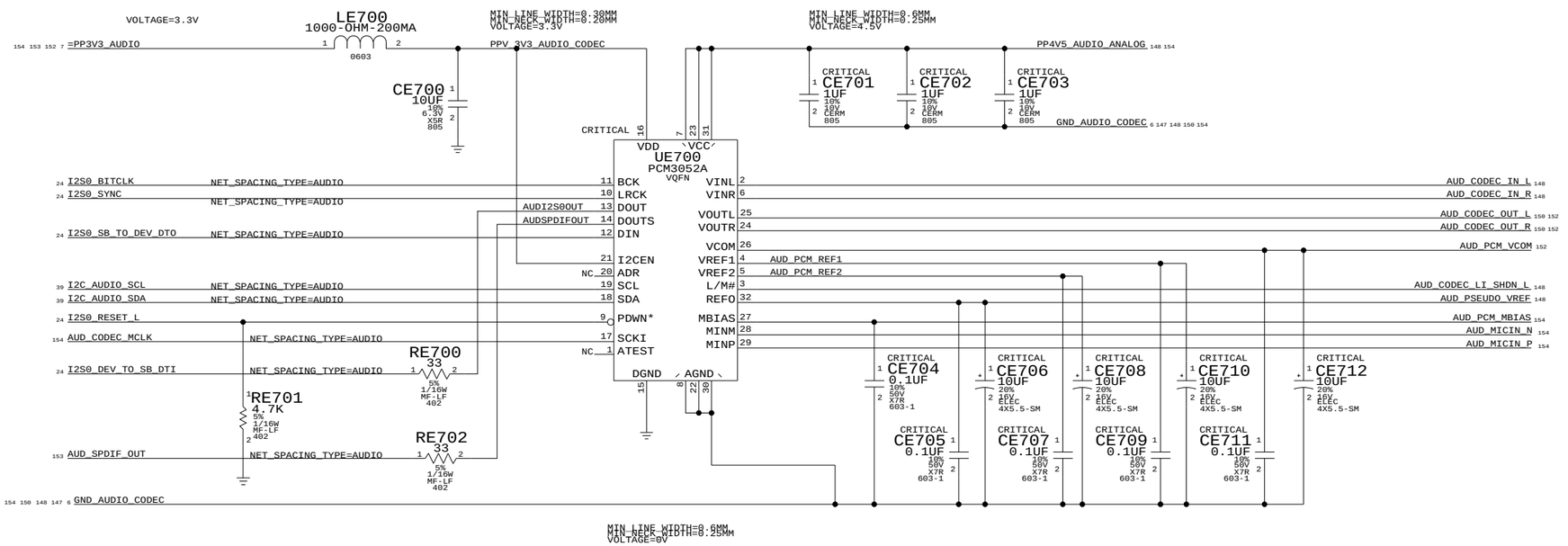
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F

SCALE: NONE

SHT 145 OF 154

AUDIO CODEC
APPLE P/N 353S0933



AUDIO: CODEC

SYNC_MASTER=FINO-SO SYNC_DATE=10/07/2005

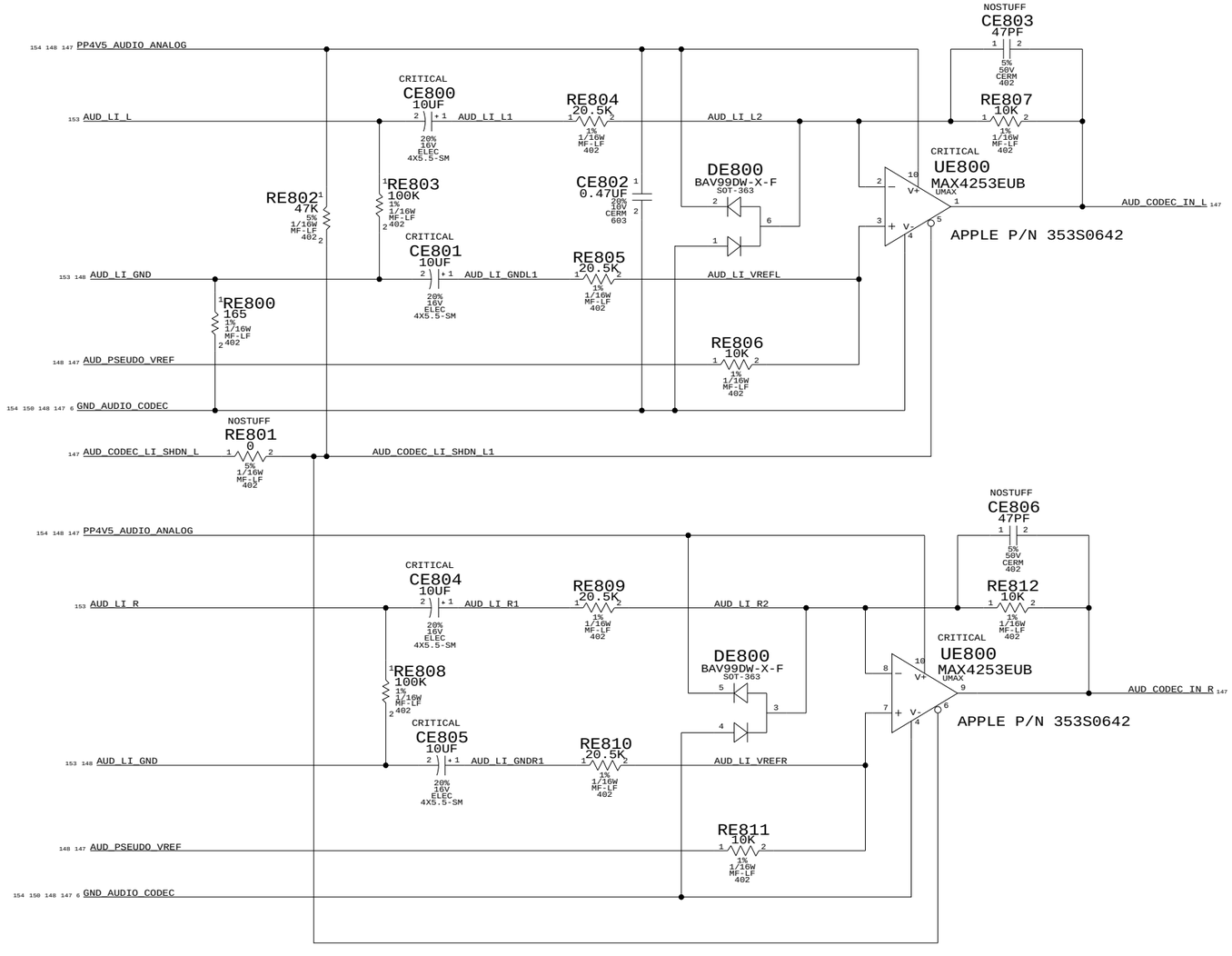
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F

SCALE	SHT	OF
NONE	147	154

LINE IN PSEUDO-DIFFERENTIAL AMP

AV= 0.49



AUDIO: LINE INPUT AMP

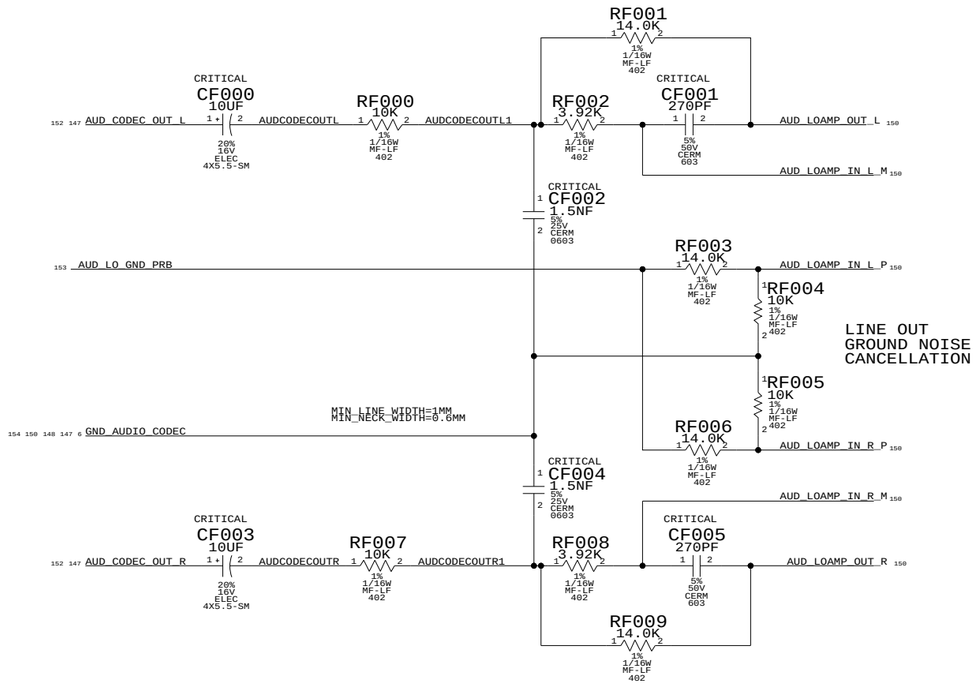
SYNC_MASTER=FINO-SO SYNC_DATE=10/07/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 148 OF 154	

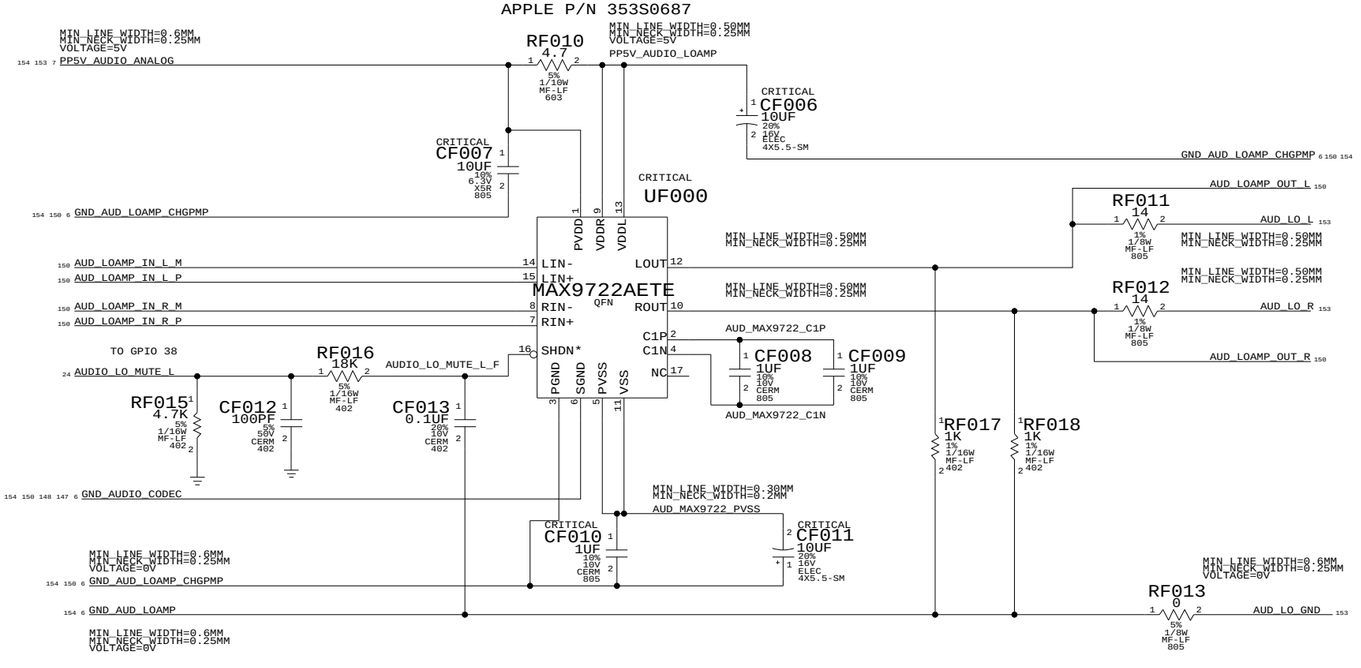
LINE OUT LOW-PASS FILTER

FC = 37 KHZ, HO = -1.4



LINE OUT AMP

APPLE P/N 353S0687



AUDIO: LINE OUT AMP

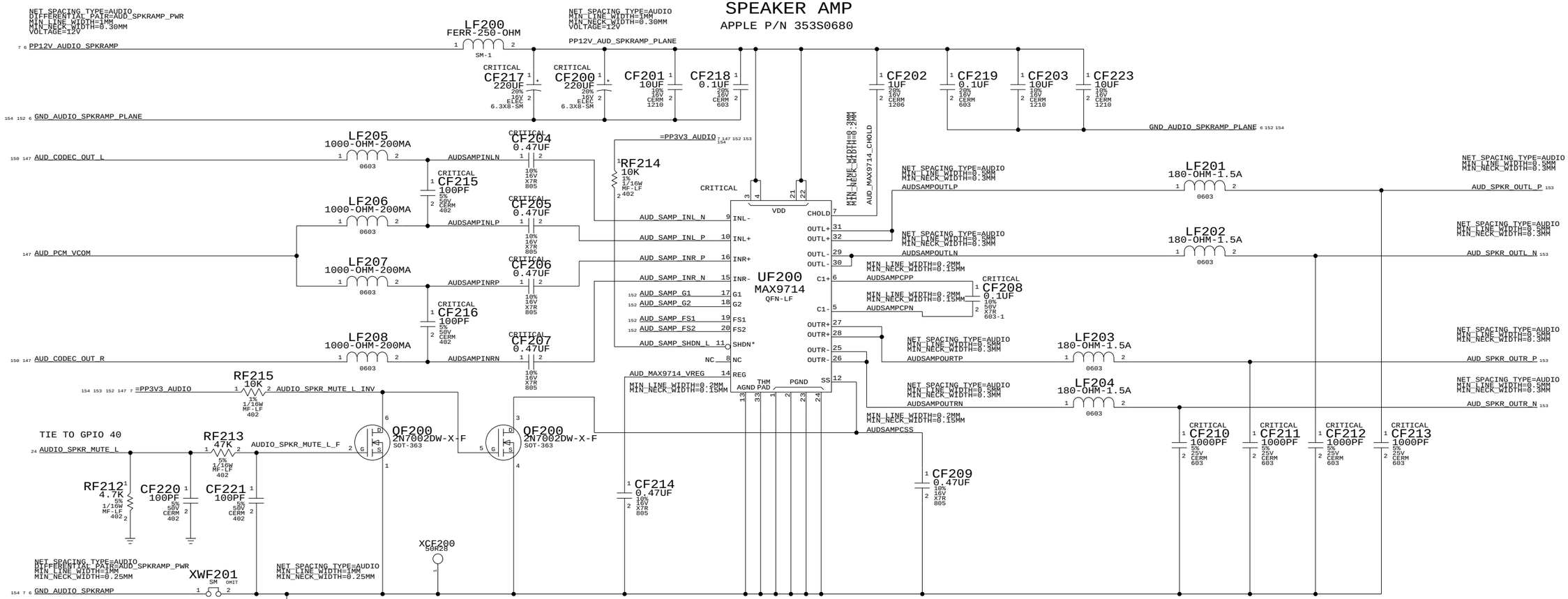
SYNC_MASTER=FINO-SO SYNC_DATE=10/07/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 150 OF 154	

SPEAKER AMP

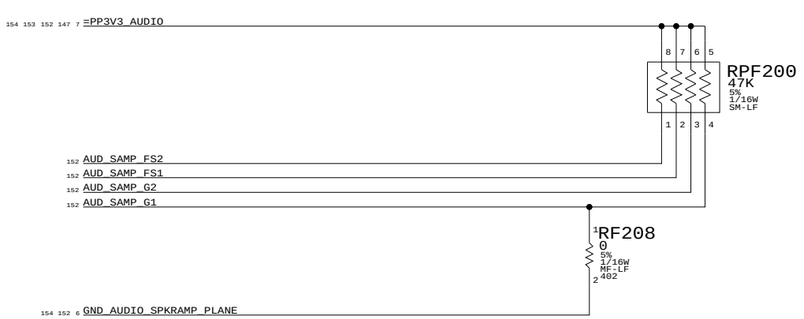
APPLE P/N 353S0680



GAIN SETTINGS: +19DB

MODULATION SETTING: LOW EMI

GAIN AND SWITCHING FREQUENCY STUFF OPTIONS



AUDIO: SPEAKER AMP

SYNC_MASTER=FINO-SO SYNC_DATE=10/07/2005

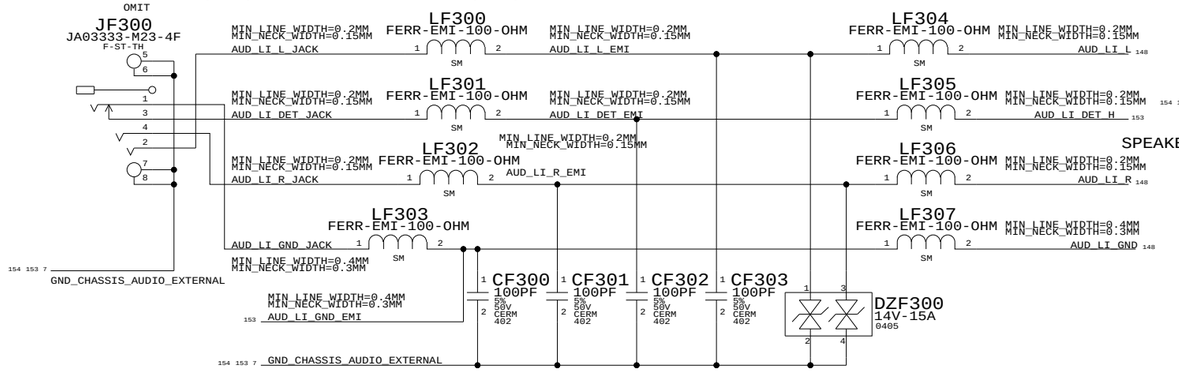
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F

SCALE	SHT	OF
NONE	152	154

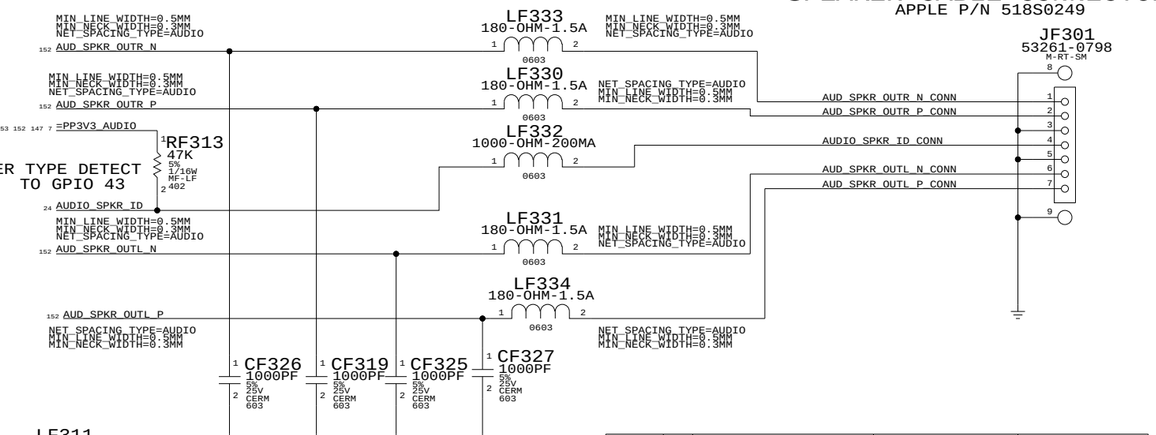
LINE IN JACK

APPLE P/N 514-0246 (M23) APPLE P/N 514-0249 (M33)



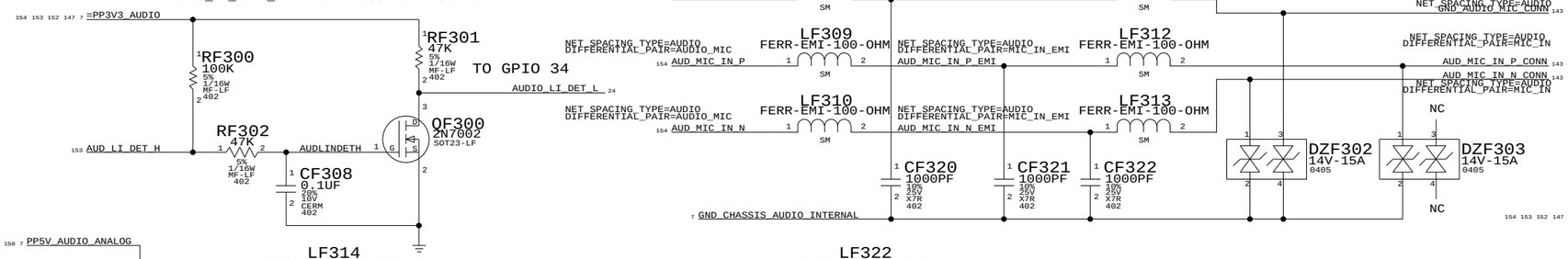
SPEAKER CABLE CONNECTOR

APPLE P/N 518S0249



LINE IN PLUG DETECT

AUDIO_IN_DET0_L = LOW: PLUG INSERTED
AUDIO_IN_DET0_L = HIGH: PLUG NOT INSERTED



CRITICAL	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
CRITICAL	514-0246	1	LINE IN CONNECTOR, 5.5 DEG	JF300	17_INCH_LCD
CRITICAL	514-0260	1	COMBO OUT CONN, 4.5 DEG	JF303	17_INCH_LCD
CRITICAL	514-0249	1	LINE IN CONNECTOR, 5.5 DEG	JF300	20_INCH_LCD
CRITICAL	514-0261	1	COMBO OUT CONN, 4.5 DEG	JF303	20_INCH_LCD

LINE OUT PLUG DETECTS

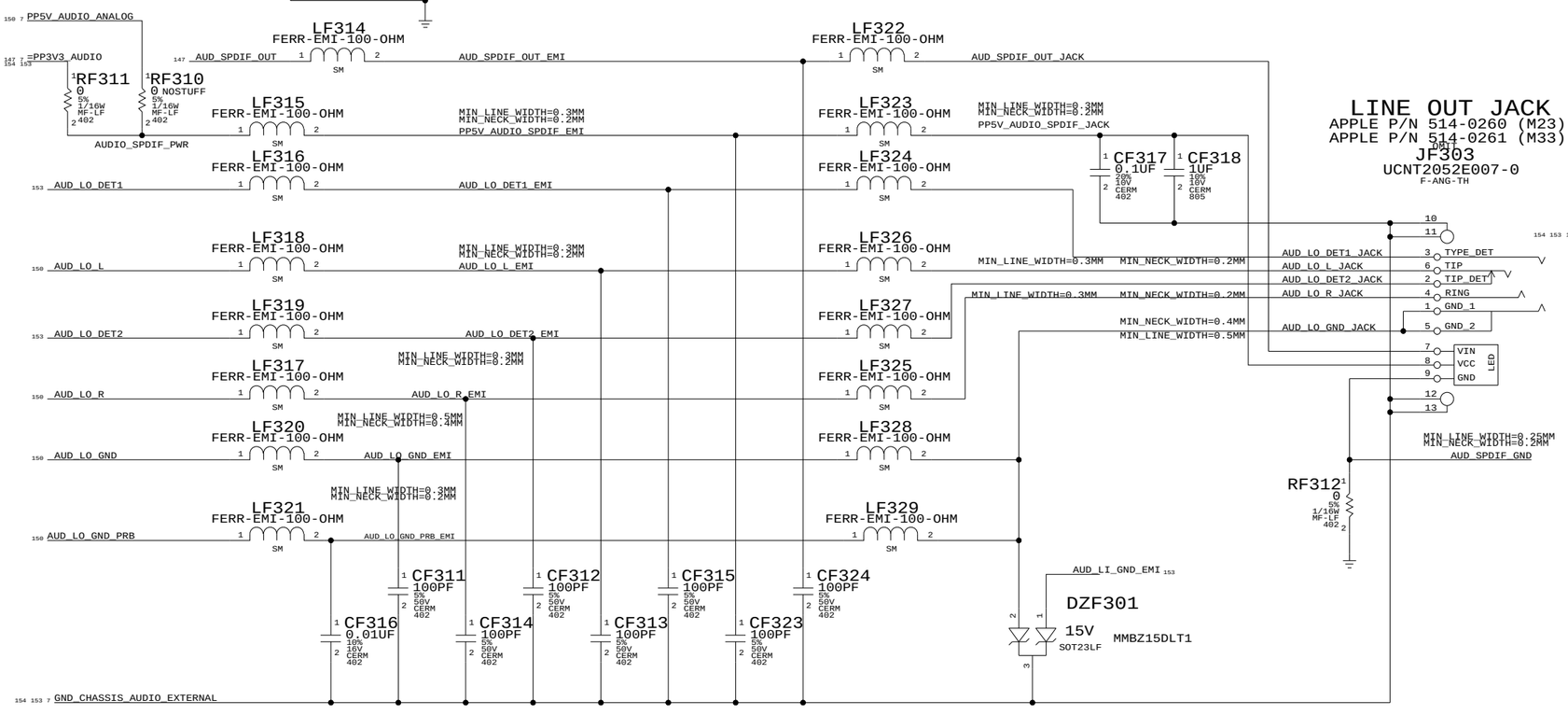
AUDIO_LO_DET_L = LOW: PLUG INSERTED
AUDIO_LO_DET_L = HIGH: PLUG NOT INSERTED

AUDIO_LO_OPTICAL_PLUG_L = LOW: OPTICAL DIGITAL AUDIO PLUG INSERTED
AUDIO_LO_OPTICAL_PLUG_L = HIGH: ANALOG AUDIO PLUG INSERTED

LINE OUT JACK

APPLE P/N 514-0260 (M23)
APPLE P/N 514-0261 (M33)

JF303
UCNT2052E007-0
F-ANG-TH



AUDIO: CONNECTORS

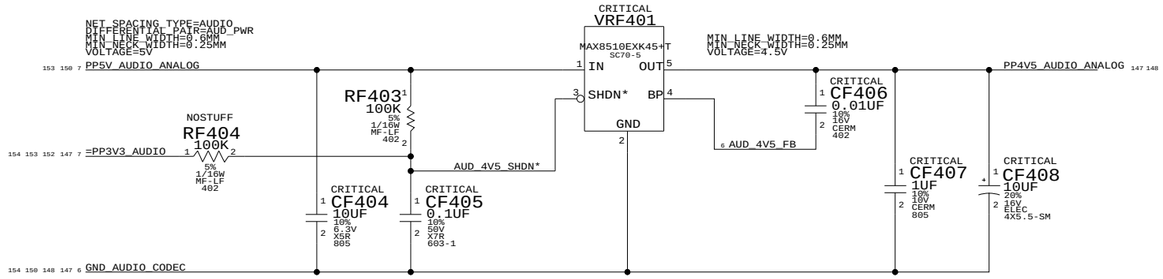
SYNC_MASTER=FINO-SO SYNC_DATE=10/07/2005

APPLE COMPUTER INC.

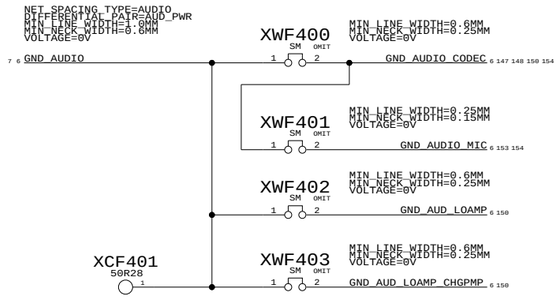
SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 153 OF 154	

4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP

APPLE P/N 353S0733



AUDIO GROUND RETURNS



PLACE ACROSS GROUND SPLIT

NOSTUFF

RF416

0

5%

1/8W

MF-LF

805

152 6 GND_AUDIO_SPKRAMP_PLANE — GND_AUDIO_CODEC 6 147 148 150 154

PLACE NEAR ENTRY TO SPEAKER AMP GROUND PLANE

NOSTUFF

RF417

0

5%

1/8W

MF-LF

805

152 7 6 GND_AUDIO_SPKRAMP

PLACE ACROSS GROUND SPLIT AT CODEC UE700

RF405

0

5%

1/8W

MF-LF

805

154 150 148 147 6 GND_AUDIO_CODEC

PLACE AT JF303

RF429

0

5%

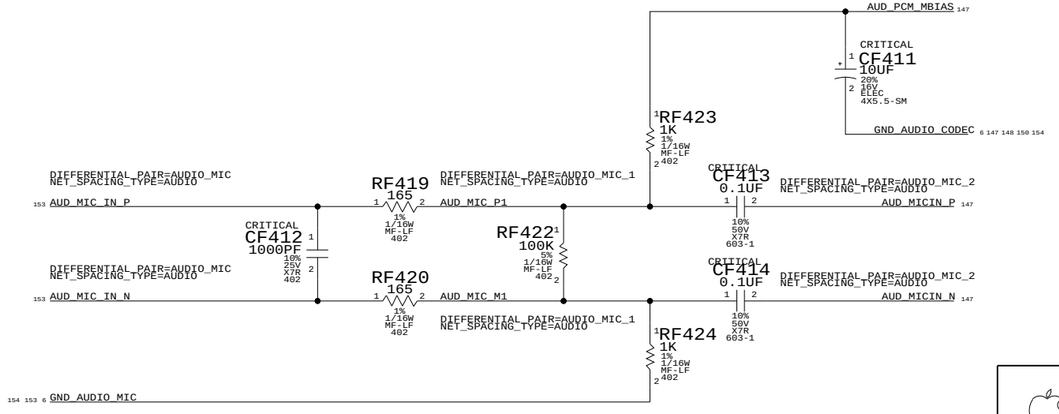
1/8W

MF-LF

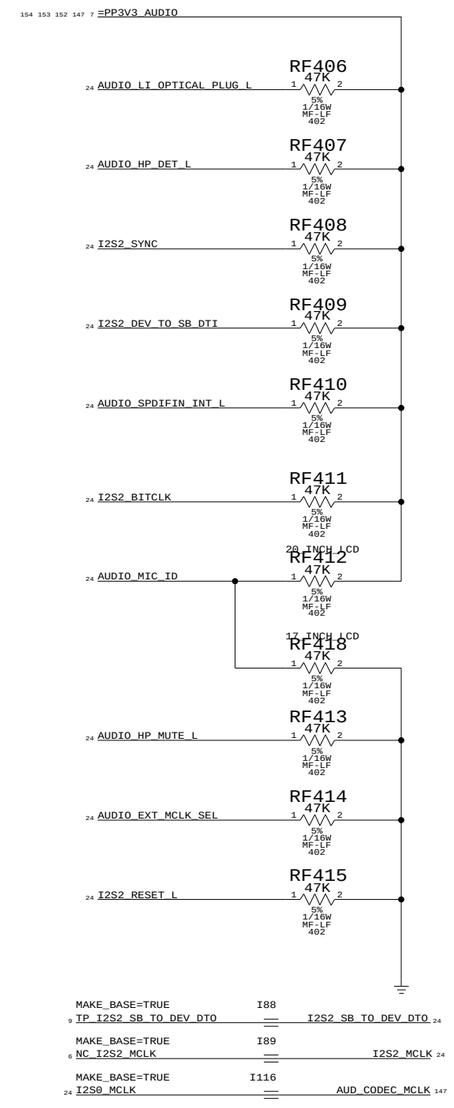
805

153 7 GND_CHASSIS_AUDIO_EXTERNAL

MICROPHONE IMPEDANCE MATCHING CIRCUIT



UNUSED GPIO TERMINATIONS



AUDIO: POWER SUPPLIES

SYNC_MASTER=FINO-SO SYNC_DATE=10/07/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE: NONE	SHT 154 OF 154	