1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD	DATE
				2009-05-19

SCHEM,BLACK_PEARL,MLB,K92

pre-evt 11/22/10 rev3.11.3

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8618	1	SCHEM,BLACK_PEARL,MLB,K92	SCH	CRITICAL	
820-2914	1	PCBF,BLACK_PEARL,MLB,K92	PCB	CRITICAL	

DRAWING

TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Tue Nov 23 20:44:38 2010

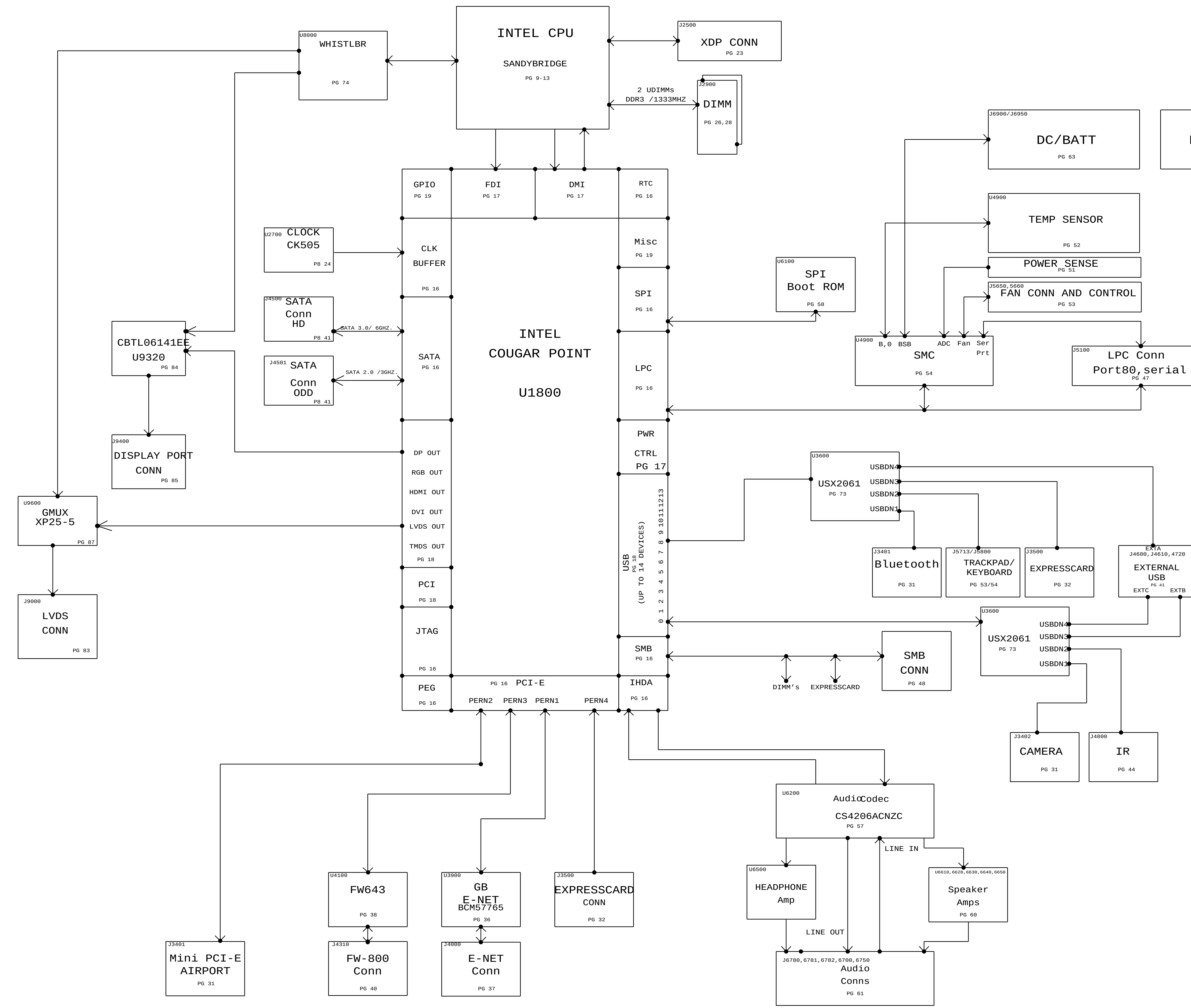
DRAWING TITLE: SCHEM,MLB,K92

Apple Inc.

DRAWING NUMBER | SIZE: D

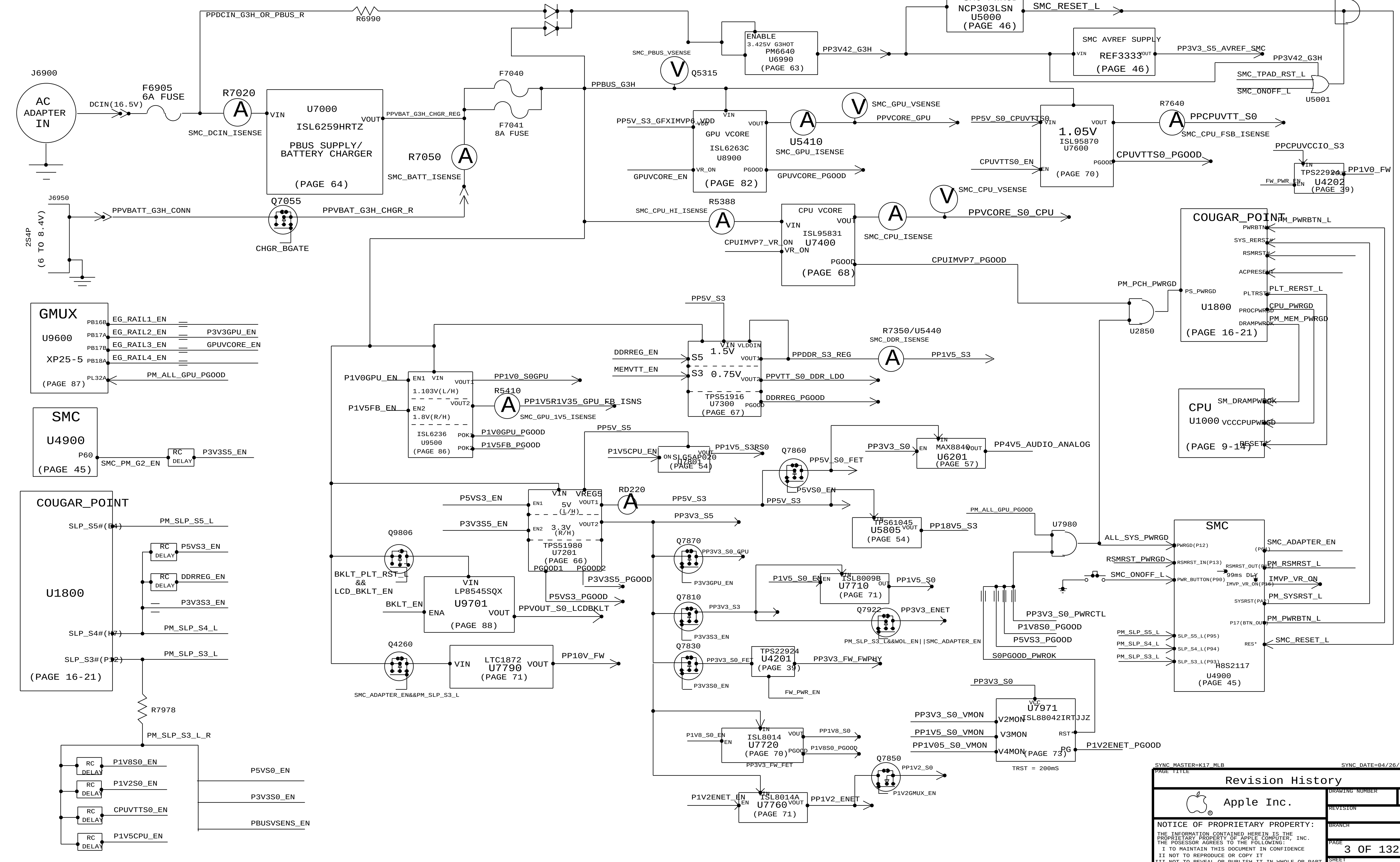
REVISION

BRANCH



SYNC_MASTER=K60_MLB	SYNC_DATE=04/26/2010
PAGE TITLE	
System Block Diagram	
Apple Inc.	DRAWING NUMBER / SIZE D
	REVISION
	BRANCH
NOTICE OF PROPRIETARY PROPERTY:	PAGE 2 OF 132
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:	SHEET 2 OF 105

K92 POWER SYSTEM ARCHITECTURE



SYNC_MASTER=K17_MLB SYNC_DATE=04/26/2010

PAGE TITLE

Revision History

Apple Inc.

DRAWING NUMBER

SIZE D

REVISION

BRANCH

PROTO2/EVT 11/11/10 rev3.0 for board 820-2914-05.brd release
PROTO2/EVT 11/15/10 rev3.6 for board 820-2914-06.brd release
PROTO2/EVT 11/19/10 rev3.7 for board 820-2914-07.brd release
EVT 11/22/10 rev3.9 for board 820-2914-07.brd release

SYNC_MASTER=K17_MLB	SYNC_DATE=04/26/2010
PAGE TITLE	Revision History
Apple Inc.	DRAWING NUMBER / SIZE D
	REVISION
NOTICE OF PROPRIETARY PROPERTY:	BRANCH
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	PAGE 4 OF 132
	SHEET 4 OF 105

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-1303	PCBA,MLB,K92	K92_COMMON,CPU:2_2GHZ,FB_1G_SAMSUNG,EEEE_DG5Y
639-1464	PCBA,MLB,CFG2,K92	K92_COMMON,CPU:2_2GHZ,FB_1G_HYNIX,VRAM_HYNIX,EEEE_DG60
639-1466	PCBA,MLB,CFG3,K92	K92_COMMON,CPU:2_3GHZ,FB_1G_SAMSUNG,EEEE_DG62
639-1465	PCBA,MLB,CFG4,K92	K92_COMMON,CPU:2_3GHZ,FB_1G_HYNIX,VRAM_HYNIX,EEEE_DG61
085-1898	K92 MLB DEVELOPMENT BOM	K92_DEVEL:ENG

K92 BOM GROUPS

BOM GROUP	BOM OPTIONS
K92_COMMON	ALTERNATE,COMMON,K92_COMMON1,K92_COMMON2,K92_PROGPARTS
K92_COMMON1	CPUMEM_S0,EXT_HP_AMP,SMC_DEBUG_YES,USBHUB_2514B
K92_COMMON2	GPUVID_1P11V,HUB1_2NONREM,HUB2_2NONREM,KB_BL,ENET:B0,T29BST:Y,T29:YES,T29_DP_HPD:ALL_OR
K92_DEVEL:ENG	SNB_CPT_XDP,DEBUG_ADC,LPCPLUS:YES,VREFMRGN,GMUX_JTAG_CONN,S0PGOOD_ISL,BMON:ENG,CPURIPPLE_ENG,IMVPISNS_ENG,SDRVI2C:MCU
K92_DEVEL:PVT	SNB_CPT_XDP,LPCPLUS:YES,VREFMRGN_NOT
K92_PROGPARTS	SMC_PROG:EVT,BOOTROM_PROG:EVT,ENETROM_PROG:B0_NOSD,TPAD_PROG:EVT,T29ROM:PROG,GMUX_PROG,T29MCU:PROG
K92_PVT	VREFMRGN_NOT,XDP,XDP_CPU_BPM,BMON:PROD
SNB_CPT_XDP	XDP,XDP_CONN,XDP_CPU_BPM,XDP_PCH

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG5Y]	CRITICAL	EEEE_DG5Y
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG60]	CRITICAL	EEEE_DG60
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG61]	CRITICAL	EEEE_DG61
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG62]	CRITICAL	EEEE_DG62

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4032	1	IC,CPU,SNB,SR00W,PRQ,D2,2.2,45W,4+2,1.30,6M,BGA	U1000	CRITICAL	CPU:2_2GHZ
337S4033	1	IC,CPU,SNB,SR00U,PRQ.D2,2.3,45W,4+2,1.30,8M,BGA	U1000	CRITICAL	CPU:2_3GHZ
337S4029	1	IC,PCH,COUGARPOINT SLH9D,PRQ,BD82HM63	U1800	CRITICAL	
343S0534	1	IC,ASIC,GBIT ETHNET&SD CTRLR,686 QFN 8X8	U3900	CRITICAL	ENET:B0
343S0494	1	IC,ASIC,GBIT ETHNET&SD CTRLR,686 QFN 8X8	U3900	CRITICAL	ENET:A0
338S0753	1	IC,FW643-E,1394B PHY/OHCI LINK/PCI-E,12	U4100	CRITICAL	
333S0543	4	IC,SGRAM,GDDR5,32MX32.1.25GHz,E-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB_512_SAMSUNG
333S0564	4	IC,SDRAM,GDDR5,32MX32,1.25GHz,A-DIE1.35V	U8400,U8450,U8500,U8550	CRITICAL	FB_512_HYNIX
333S0571	4	IC,SGRAM,GDDR5,64MX32,3.6GBPS,C-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB_1G_SAMSUNG
333S0572	4	IC,SGRAM,GDDR5,64MX32,3.6GBPS,M-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB_1G_HYNIX
337S3936	1	IC,GPU,AMD,WHISTLER,962FCBGA,40NM,ES	U8000	CRITICAL	
338S0945	1	Light Ridge,S LHAJ,FCBGA,15x15mmm	U3600	CRITICAL	T29:YES
353S3055	1	IC, P13VEDP212,x2 DISPLAYPORT 2:1 MUX, QFN	U9390	CRITICAL	

Programmed Parts-All Builds

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0777	1	IC,EEPROM,SERIAL,8KB,SOIC	U3690	CRITICAL	T29ROM:BLANK
341S2899	1	IC,T29 EEPROM,K92	U3690	CRITICAL	T29ROM:PROG
341S2384	1	IR,ENCORE II, CY7C63833-LFXC	U4800	CRITICAL	
335S0724	1	IC,GPU ROM,K91/F,K92	U8701	CRITICAL	GPUROM:BLANK
341S2957	1	IC,GPU ROM,K91/F,K92	U8701	CRITICAL	GPUROM:PROG
336S0042	1	IC,PLD,LATTICE,LFXP2-5E-5,132 BALL CSBGA	U9600	CRITICAL	GMUX_BLANK
341S2996	1	IC,GMUX,K92	U9600	CRITICAL	GMUX_PROG
337S3997	1	IC,MCU,32B,LPC1112A,16KB/2KB,HVQFN25	U9330	CRITICAL	T29MCU:BLANK
341S2939	1	IC,PROGRAMMED MCU,32B,LPC1112A,16KB/2KB,HVQFN25	U9330	CRITICAL	T29MCU:PROG

GPUROM will NOSUFFED @EVT

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
157S0058	157S0055		ALL	Delta alt to TDK Magnetics	
152S0896	152S0518		ALL	MAG LAYERS ALT TO CYNTEC	
152S0915	152S0796		ALL	MAG LAYERS ALT TO CYNTEC	
155S0457	155S0329		ALL	MAG LAYERS ALT TO MURATA	
516S0805	516S0806		ALL	FOXCONN ALT TO MOLEX	
353S2805	353S2603		ALL	Fairchild 8' alt to 6'wafer	
127S0111	127S0060		ALL	Rohm alt to Kemet	
353S3085	353S1658		ALL	ST Micro alt to LT	(U5850)
152S0905	152S1307		ALL	Cyntec (used on K90i) as alt	(L7630)
353S3055	353S3151		ALL	Pericom alt to NXP DP Mux	(U9390)
376S0855	376S0613		ALL	radar8515240 Toshiba FET	(Q3200, etc)
870-1939	870-1698		ALL	Silver alt to Gold tall pogo pins	
870-2015	870-1699		ALL	Silver alt to Gold short pogo pins	
376S0972	376S0612		ALL	add ROHM part as 2nd source	
138S0676	138S0691		ALL	add Murata part as 2nd source	
128S0327	128S0264		ALL	add NEC part as 2nd source	
376S0977	376S0859		ALL	add new part as 2nd source	
138S0681	138S0638		ALL	add new part as 2nd source	(Q3888,Q9430)

SMC

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0895	1	IC,SMC,HS8/2117,9MMX9MM,TLP	U4900	CRITICAL	SMC_BLANK
341S2855	1	IC,SMC,DEVELOPMENT-PROTO,K92	U4900	CRITICAL	SMC_PROG:PROTO0
341S2855	1	IC,SMC,DEVELOPMENT-PROTO1,K92	U4900	CRITICAL	SMC_PROG:PROTO1
341S2995	1	IC,SMC,DEVELOPMENT-PROTO2,K92	U4900	CRITICAL	SMC_PROG:PROTO2
341S2862	1	IC,SMC,DEVELOPMENT-EVT,K92	U4900	CRITICAL	SMC_PROG:EVT
341S2865	1	IC,SMC,DEVELOPMENT-DVT,K92	U4900	CRITICAL	SMC_PROG:DVT
341S2868	1	IC,SMC,DEVELOPMENT-PVT,K92	U4900	CRITICAL	SMC_PROG:PVT

EFI

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0740	1	64 MBIT SPI SERIAL DUAL I/O FLASH	U6100	CRITICAL	BOOTROM_BLANK
341S2893	1	IC,EFI,ROM,PROTO, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:PROTO0
341S2934	1	IC,EFI,ROM,PROTO1, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:PROTO1
341S2991	1	IC,EFI,ROM,PROTO1, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:PROTO2
341S2894	1	IC,EFI,ROM,EVT, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:EVT
341S2895	1	IC,EFI,ROM,DVT, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:DVT
341S2896	1	IC,EFI,ROM,PVT, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:PVT

Ethernet

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0539	1	IC,FLASH,SERIAL,SPI,1MBIT,2V7,8P,SOIC	U3990	CRITICAL	ENETROM_BLANK
341S2685	1	IC,ENET ROM,PROTO1,K92	U3990	CRITICAL	ENETROM_PROG:A0_SD
341S3027	1	IC,ENET ROM, PROTO2, EVT,DVT,PVT,K92	U3990	CRITICAL	ENETROM_PROG:B0_NOSD

PSOC

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S2902	1	IC,TP PSOC,PROTO,K90,K90i,K91,K91F,K92	U5701	CRITICAL	TPAD_PROG:PROTO1
341S3024	1	IC,TP PSOC,proto2,K90,K90i,K91,K91F,K92T	U5701	CRITICAL	TPAD_PROG:PROTO2
341S3024	1	IC,TP PSOC,proto1,EVT,K90,K90i,K91,K91F,K92T	U5701	CRITICAL	TPAD_PROG:EVT
341S3024	1	IC,TP PSOC,proto1,DVT,pVT,K90,K90i,K91,K91F,K92T	U5701	CRITICAL	TPAD_PROG:DVTPVT

SYNC_MASTER=K17_MLB SYNC_DATE=04/26/2010

PAGE TITLE

BOM Configuration

Apple Inc.

DRAWING NUMBER

SIZE D

REVISION

BRANCH

Functional Test Points

FUNC_TEST

J5650 (LEFT FAN CONN)
FAN_LT_PWM
FAN_LT_TACH
PP5V_S0 — 2 TPs
GND — 2 TPs

J5660 (RIGHT FAN CONN)
FAN_RT_PWM
FAN_RT_TACH
PP5V_S0 — 2 TPs
GND — 2 TPs

J6780 (MIC FR CONN)
AUD_DMIC_CLK_FR
AUD_DMIC_SDA_FR
AUD_DMIC_PWR_FR
GND — 2 TPs

J6783 (MIC BK CONN)
AUD_DMIC_CLK_BK
AUD_DMIC_SDA_BK
AUD_DMIC_PWR_BK
GND — 2 TPs

J6781 (LEFT SPEAKER)
SPKRAMP_FL_OUT_P
SPKRAMP_FL_OUT_N
SPKRAMP_BL_OUT_P
SPKRAMP_BL_OUT_N

J6782 (RIGHT & SUB SPEAKER)
SPKRAMP_LFE_OUT_P
SPKRAMP_LFE_OUT_N
SPKRAMP_FR_OUT_P
SPKRAMP_FR_OUT_N
SPKRAMP_BR_OUT_P
SPKRAMP_BR_OUT_N

J9000 (LVDS CONN)
PP3V3_SW_LCD — 2 TPs
PP3V3_S0 — 2 TPs
PPVOUT_S0_LCDBKLT — 2 TPs
LVDS_DDC_CLK
LVDS_DDC_DATA
LVDS_CONN_A_DATA_P<0>
LVDS_CONN_A_DATA_N<0>
LVDS_CONN_A_DATA_P<1>
LVDS_CONN_A_DATA_N<1>
LVDS_CONN_A_DATA_P<2>
LVDS_CONN_A_DATA_N<2>
LVDS_CONN_A_CLK_F_P
LVDS_CONN_A_CLK_F_N
LVDS_CONN_B_DATA_P<0>
LVDS_CONN_B_DATA_N<0>
LVDS_CONN_B_DATA_P<1>
LVDS_CONN_B_DATA_N<1>
LVDS_CONN_B_DATA_P<2>
LVDS_CONN_B_DATA_N<2>
LVDS_CONN_B_CLK_F_P
LVDS_CONN_B_CLK_F_N
LED_RETURN_1
LED_RETURN_2
LED_RETURN_3
LED_RETURN_4
LED_RETURN_5
LED_RETURN_6
GND — 5 TPs

J4500 (SATA ODD CONN)
PP5V_SW_ODD — 3 TPs
SMC_ODD_DETECT
SATA_ODD_D2R_UF_P
SATA_ODD_D2R_UF_N
SATA_ODD_R2D_P
SATA_ODD_R2D_N
GND — 4 TPs

J4501 (SATA HDD CONN)
PP5V_S0_HDD_FLT — 3 TPs
SATA_HDD_R2D_P
SATA_HDD_R2D_N
SATA_HDD_D2R_C_P
SATA_HDD_D2R_C_N
PP5V_S3_IR_R
IR_RX_OUT
SYS_LED_ANODE_R
GND — 4 TPs

J5815 (KBD BACKLIGHT CONN)
KBDLED_ANODE
SMC_KDBLED_PRESENT_L
GND

J6995 (BAT LED CONN)
PP3V42_G3H
SMBUS_SMC_BSA_SDA
SMBUS_SMC_BSA_SCL
SMC_BIL_BUTTON_L
SMC_LID_R
GND

J6900 (DC POWER CONN)
ADAPTER_SENSE
PP18V5_DCIN_FUSE — 3 TPs
GND — 4 TPs

J3401 (AIRPORT/BT CONN)
WIFI_EVENT_L
PCIE_AP_R2D_P
PCIE_AP_R2D_N
PCIE_AP_D2R_P
PCIE_AP_D2R_N
PCIE_CLK100M_AP_CONN_P
PCIE_CLK100M_AP_CONN_N
AP_CLKREQ_Q_L
PCIE_WAKE_L
AP_RESET_CONN_L
PP3V3_WLAN — 3 TP needed
PP3V3_S3_BT_F
SMBUS_SMC_0_S0_SDA
SMBUS_SMC_0_S0_SCL
USB_BT_P
USB_BT_N
GND — 6 TP needed

J3402 (CAMERA/ALS CONN)
USB_CAMERA_CONN_P
USB_CAMERA_CONN_N
PP5V_S3_ALSCAMERA_F
SMBUS_SMC_A_S3_SDA
SMBUS_SMC_A_S3_SCL
GND — 2 TP needed

J3500 (EXPRESS CARD CONN)
PP1V5_S0_EXCARD_SWITCH
PCIE_WAKE_L
SMBUS_PCH_CLK
SMBUS_PCH_DATA
PP3V3_S0_EXCARD_SWITCH
PP3V3_S3_EXCARD_SWITCH
USB2_EXCARD_CONN_N
USB2_EXCARD_CONN_P
EXCARD_CPUSB_L
EXCARD_CLKREQ_CONN_L
EXCARD_CPPE_L
PLT_RESET_SWITCH_L
PCIE_EXCARD_D2R_P
PCIE_EXCARD_D2R_N
PCIE_EXCARD_R2D_P
PCIE_EXCARD_R2D_N
PCIE_CLK100M_EXCARD_CONN_P
PCIE_CLK100M_EXCARD_CONN_N

J5800 (IPD FLEX CONN)
PP3V3_S3
PP18V5_S4
PP3V3_S4
Z2_CS_L
Z2_DEBUG3
Z2_MISO
Z2_BOOST_EN
Z2_MOSI
Z2_CLKIN
Z2_KEY_ACT_L
Z2_RESET
Z2_HOST_INTN
Z2_SCLK
PSOC_F_CS_L
PICKB_L
PSOC_MISO
PSOC_MOSI
PSOC_SCLK
SMBUS_SMC_A_S3_SCL
SMBUS_SMC_A_S3_SDA
GND — 2 TPS

J6950 (MAIN BATT CONN)
PPVBAT_G3H_CONN — 5 TPs
SMBUS_SMC_BSA_SCL
SMBUS_SMC_BSA_SDA
SYS_DETECT_L
GND — 5 TPs

J4800 (FRONT CABLE CONN)
PP3V42_G3H_LIDSWITCH_R
PP5V_S3_IR_R
SMC_LID_R
IR_RX_OUT
SYS_LED_ANODE
GND

J5713 (KEY BOARD CONN)
PP3V3_S4
PP3V42_G3H
WS_KBD1
WS_KBD2
WS_KBD3
WS_KBD4
WS_KBD5
WS_KBD6
WS_KBD7
WS_KBD8
WS_KBD9
WS_KBD10
WS_KBD11
WS_KBD12
WS_KBD13
WS_KBD14
WS_KBD15_CAP
WS_KBD16_NUM
WS_KBD17
WS_KBD18
WS_KBD19
WS_KBD20
WS_KBD21
WS_KBD22
WS_KBD23
WS_KBD_ONOFF_L
WS_LEFT_SHIFT_KBD
WS_LEFT_OPTION_KBD
WS_CONTROL_KBD
GND — 2 TP needed

POWER RAILS
FUNC_TEST
PM_SLP_S3_L
PPBUS_G3H
PP3V42_G3H
PP5V_S3
PP5V_S0
PPVCORE_S0_CPU
PP3V3_S5 — 2 TPs
PP3V3_S3
PP3V3_S0
PP1V2_S0
PP1V8_S0
PPVTTDDR_S3
PPVP_FW
PP3V3_S0GPU
PP1V8_S0GPU
PPVCORE_GPU
PP1V8_S0GPU_ISNS_R
PP3V3_S5_AVREF_SMC
PP18V5_S4
PPDCIN_G3H

FUNC_TEST
SYS_LED_ANODE_R
LPC_CLK33M_LPCPLUS
LPC_AD<0..3>
SPI_ALT_MOSI
SPI_ALT_MISO
LPC_FRAME_L
PM_CLKRUN_L
SMC_TMS
LPCPLUS_RESET_L
SMC_TDO
SMC_TRST_L
SMC_MD1
SMC_TX_L
SPIROM_USE_MLB
SPI_ALT_CLK
SPI_ALT_CS_L
LPC_SERIRQ
LPC_PWRDWN_L
SMC_TDI
SMC_TCK
SMC_RESET_L
SMC_NMI
SMC_RX_L
LPCPLUS_GPIO
ISSP_SCLK_P1_1
ISSP_SDATA_P1_0
SMC_ONOFF_L
PM_SYSRST_L
LCD_BKLT_PWM

NO_TEST=TRUE

T29_D2R_P<1..0>
T29_D2R_N<1..0>
T29_D2R_C_P<1..0>
T29_D2R_C_N<1..0>
T29_R2D_C_P<1..0>
T29_R2D_C_N<1..0>
T29_R2D_P<1..0>
T29_R2D_N<1..0>
T29DPA_ML_P<3..0>
T29DPA_ML_N<3..0>
DP_T29SNK0_AUXCH_C_P
DP_T29SNK0_AUXCH_C_N
DP_T29SNK0_AUXCH_P
DP_T29SNK0_AUXCH_N
DP_T29SNK0_ML_C_P<3..0>
DP_T29SNK0_ML_C_N<3..0>
DP_T29SNK0_ML_P<3..0>
DP_T29SNK0_ML_N<3..0>
DP_T29SNK1_AUXCH_C_P
DP_T29SNK1_AUXCH_C_N
DP_T29SNK1_AUXCH_P
DP_T29SNK1_AUXCH_N
DP_T29SNK1_ML_C_P<3..0>
DP_T29SNK1_ML_C_N<3..0>
DP_T29SNK1_ML_P<3..0>
DP_T29SNK1_ML_N<3..0>
TP_DP_T29SRC_AUXCH_CN
TP_DP_T29SRC_AUXCH_CP
TP_DP_T29SRC_ML_CP<3..0>
TP_DP_T29SRC_ML_CN<3..0>
DP_SDRVA_ML_C_P<0>
DP_SDRVA_ML_C_N<0>
DP_SDRVA_ML_C_P<2>
DP_SDRVA_ML_C_N<2>
DP_SDRVA_ML_P<0>
DP_SDRVA_ML_N<0>
DP_SDRVA_ML_P<2>
DP_SDRVA_ML_N<2>
TP_T29_PCIE_RESET0_L
TP_T29_PCIE_RESET1_L
TP_T29_PCIE_RESET2_L
TP_T29_PCIE_RESET3_L
T29DPA_D2R1_AUXCH_N
T29DPA_D2R1_AUXCH_P
T29_D2R1_BIAS
DP_EXTA_ML_P<3..0>
DP_A_BIAS_N_0
DP_A_BIAS_P_0
DP_A_BIAS_N_2
DP_A_BIAS_P_2
DP_A_BIAS
DP_SDRVA_ML_R_N<0>
DP_SDRVA_ML_R_P<0>
DP_SDRVA_ML_R_N<2>
DP_SDRVA_ML_R_P<2>
T29_A_BIAS_R2D_N0
T29_A_BIAS_R2D_P0
T29_A_BIAS_R2D_N1
T29_A_BIAS_R2D_P1
SATA_HDD_R2D_UF_N
SATA_HDD_R2D_UF_P
SATA_HDD_R2D_RC_UF_N
SATA_HDD_R2D_RC_UF_P
SATA_HDD_R2D_RDRVR_OUT_N
SATA_HDD_R2D_RDRVR_OUT_P
SATA_HDD_R2D_RDRVR_IN_N
SATA_HDD_R2D_RDRVR_IN_P
SATA_HDD_R2D_C_N
SATA_HDD_R2D_C_P
SATA_HDD_D2R_UF_N
SATA_HDD_D2R_UF_P
SATA_HDD_D2R_N
SATA_HDD_D2R_P
SATA_HDD_D2R_RDRVR_OUT_N
SATA_HDD_D2R_RDRVR_OUT_P
SATA_HDD_D2R_RDRVR_IN_N
SATA_HDD_D2R_RDRVR_IN_P
SATA_HDD_D2R_C_N
SATA_HDD_D2R_C_P

NO_TEST=TRUE

TP_DVPCLK
TP_DVPCNTL<2..0>
TP_DVPCNTL_M<1..0>
TP_DVPDATA<23..0>
TP_GPU_JTAG_TRST_L
TP_DC_TEST_A4
TP_DC_TEST_D1
TP_EDP_TX_P<3..0>
TP_T29_SENSOR_ALERT
DMI_S2N_P<1..0>
DMI_S2N_N<1..0>
DMI_N2S_P<1>
DMI_N2S_N<1>
DMI_N2S_P<3>
DMI_N2S_N<3>

NC NO_TESTs

NO_TEST
NC_CRT_IG_BLUE
NC_CRT_IG_GREEN
NC_CRT_IG_RED
NC_CRT_IG_DDC_CLK
NC_CRT_IG_DDC_DATA
NC_CRT_IG_HSYNC
NC_CRT_IG_VSYNC
NC_LVDS_IG_CTRL_CLK
NC_LVDS_IG_CTRL_DATA
NC_PCH_LVDS_VBG
NC_HDA_SDIN1
NC_HDA_SDIN2
NC_HDA_SDIN3

NC NO_TESTs

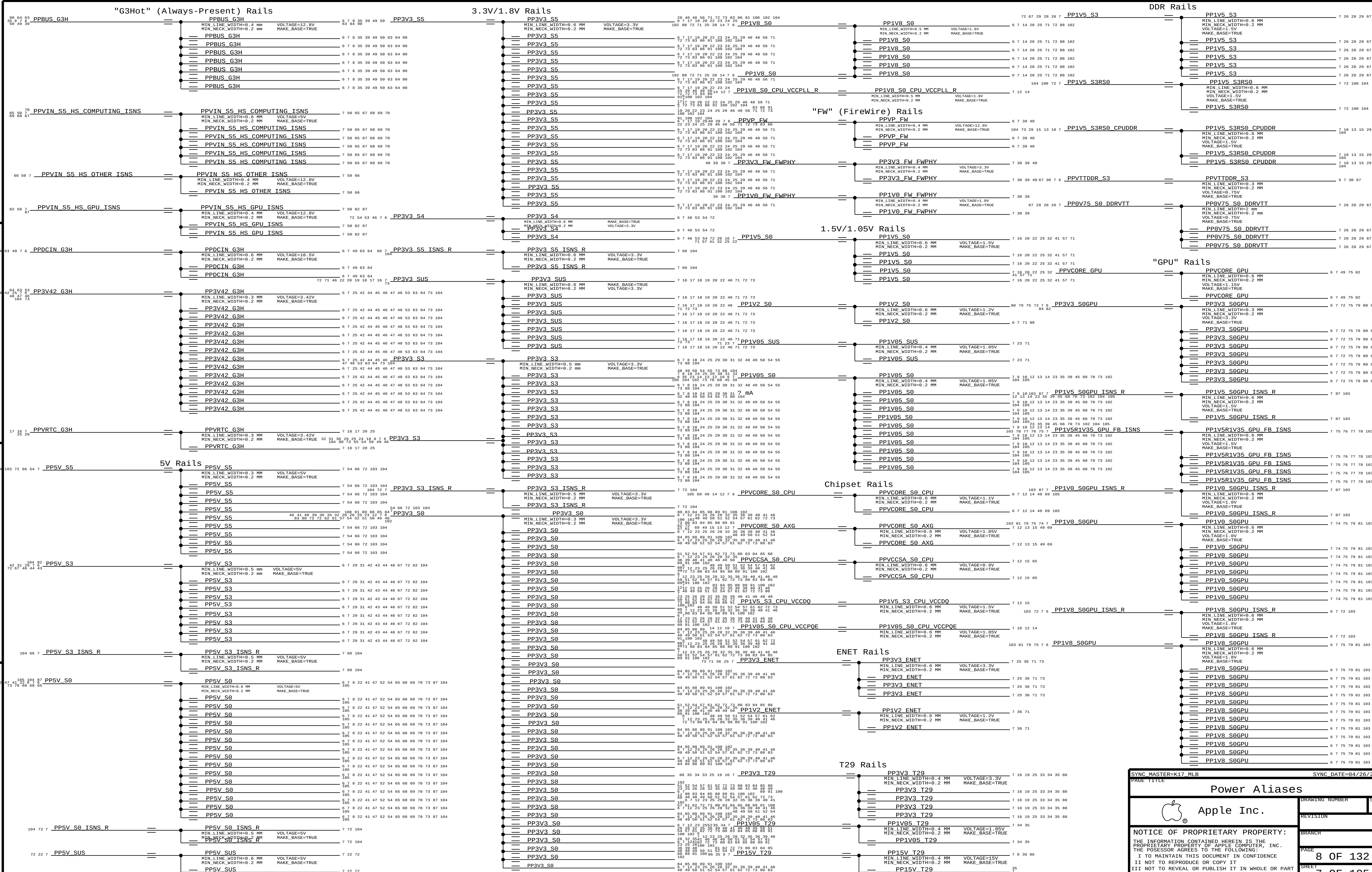
NO_TEST
TP_PCI_AD<31..0>
TP_PCI_C_BE_L<3..0>
NC_PCI_GNT3_L
NC_PCI_GNT2_L
NC_PCI_GNT1_L
NC_PCI_GNT0_L
NC_PCI_PAR
NC_PCI_RESET_L
NC_PCI_PME_L
NC_PCI_CLK33M_OUT3
TP_NV_DQ<15..0>
TP_NV_DQS<1..0>
TP_NV_CE_L<3..0>
NC_NV_ALE
NC_NV_CLE
NC_NV_RB_L
TP_NV_WR_RE_L<1..0>
TP_NV_WE_CK_L<1..0>
NC_PCIE_CLK100M_PE4N
NC_PCIE_CLK100M_PE4P
NC_PCIE_CLK100M_PE5N
NC_PCIE_CLK100M_PE5P
NC_PCIE_CLK100M_PE6N
NC_PCIE_CLK100M_PE6P
NC_PCIE_CLK100M_PE7N
NC_PCIE_CLK100M_PE7P
NC_PSOC_P1_3
NC_SATA_C_D2RN
NC_SATA_C_D2RP
NC_SATA_C_R2D_CN
NC_SATA_C_R2D_CP
NC_SATA_D_D2RN
NC_SATA_D_D2RP
NC_SATA_D_R2D_CN
NC_SATA_D_R2D_CP
NC_SATA_SSD2_D2RN
NC_SATA_SSD2_D2RP
NC_SATA_SSD2_R2D_CN
NC_SATA_SSD2_R2D_CP
NC_BCM57765_SPD100LED_L
NC_BCM57765_TRAFFICLED_L
NC_CE_L_MS_INS_L

NC NO_TESTs

NO_TEST
NC_SMC_FAN_3_TACH
NC_SMC_FAN_3_CTL
NC_SMC_FAN_2_TACH
NC_SMC_FAN_2_CTL
NC_FW2_TPBP
NC_FW2_TPBN
NC_FW2_TPBIAS
NC_FW2_TPAP
NC_FW2_TPAN
NC_FW0_TPBP
NC_FW0_TPBN
NC_FW0_TPAP
has TP

TP_FW643_AVREG — NC_FW643_AVREG — has TP
NC_FW643_TDI
NC_DP_IG_C_HPD
NC_DP_IG_C_CTRL_CLK
NC_DP_IG_C_CTRL_DATA
TP_DP_IG_C_MLP<3..0>
TP_DP_IG_C_MLN<3..0>
NC_DP_IG_C_AUXP
NC_DP_IG_C_AUXN
NC_DP_IG_D_HPD
NC_DP_IG_D_CTRL_CLK
NC_DP_IG_D_CTRL_DATA
TP_DP_IG_D_MLP<3..0>
TP_DP_IG_D_MLN<3..0>
NC_DP_IG_D_AUXP
NC_DP_IG_D_AUXN
NC_SDVO_TVCLKINN
NC_SDVO_TVCLKINP
NC_SDVO_STALLN
NC_SDVO_STALLP
NC_SDVO_INTN
NC_SDVO_INTP
NC_GPU_BUFRST_L
NC_GPU_GSTATE<0>
TP_GPU_GSTATE<1>
TP_GPU_MIOA_D<9..0>
NC_GPU_MIOA_DE
NC_LVDS_EG_B_CLKN
NC_LVDS_EG_B_CLKP
NC_LVDS_EG_BKL_PWM
TP_LVDS_IG_B_CLKN
TP_LVDS_IG_B_CLKP
TP_LVDS_IG_BKL_PWM
NC_PCH_SST
NC_PCH_NC1
NC_PCH_NC2
NC_PCH_NC3
NC_PCH_NC4
NC_PCH_NC5
NC_PCH_TP19
NC_PCH_TP18
NC_PCH_TP17
NC_PCH_TP16
NC_PCH_TP15
NC_PCH_TP14
NC_PCH_TP13
NC_PCH_TP12
NC_PCH_TP11
NC_PCH_TP10
NC_PCH_TP9
NC_PCH_TP8
NC_PCH_TP7
NC_PCH_TP6
NC_PCH_TP5
NC_PCH_TP4
NC_PCH_TP3
NC_PCH_TP2
NC_PCH_TP1
PCH_VSS_NCTF<1>
PCH_VSS_NCTF<2>
PCH_VSS_NCTF<5>
PCH_VSS_NCTF<7>
PCH_VSS_NCTF<9>
PCH_VSS_NCTF<11>
PCH_VSS_NCTF<12>
PCH_VSS_NCTF<15>
PCH_VSS_NCTF<17>
PCH_VSS_NCTF<19>
PCH_VSS_NCTF<21>
PCH_VSS_NCTF<25>
PCH_VSS_NCTF<27>
PCH_VSS_NCTF<29>

SYNC_MASTER=K17_MLB SYNC_DATE=04/26/2010
PAGE TITLE
Functional / ICT Test
Apple Inc.
DRAWING NUMBER
SIZE D
REVISION
BRANCH



SYNC_MASTER=K17_MLB SYNC_DATE=04/26/2010

PAGE TITLE

Power Aliases

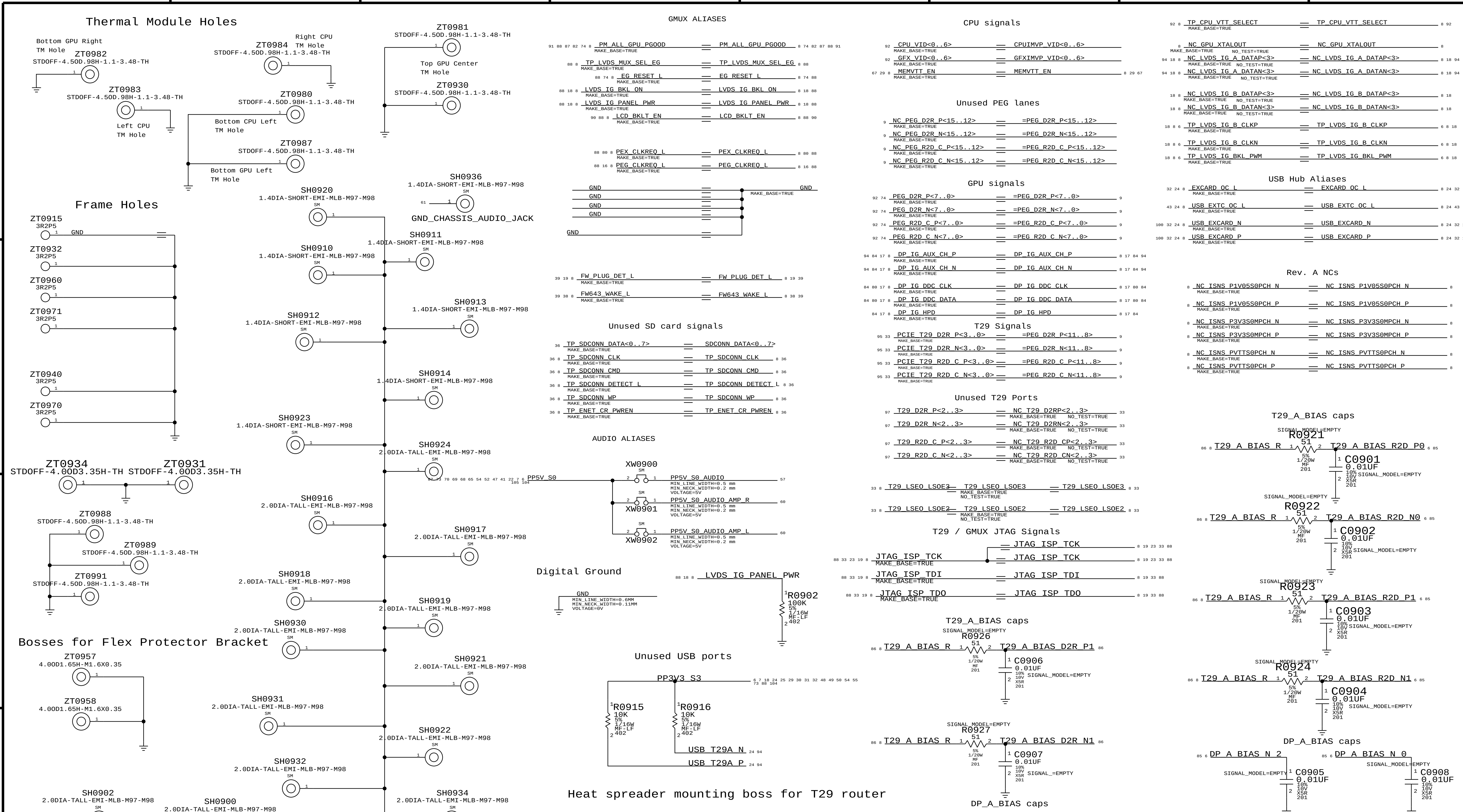
Apple Inc.

DRAWING NUMBER SIZE D

REVISION

BRANCH

NOTICE OF PROPRIETARY PROPERTY:



SYNC_MASTER=K17_MLB SYNC_DATE=04/26/2010

PAGE TITLE: Signal Aliases

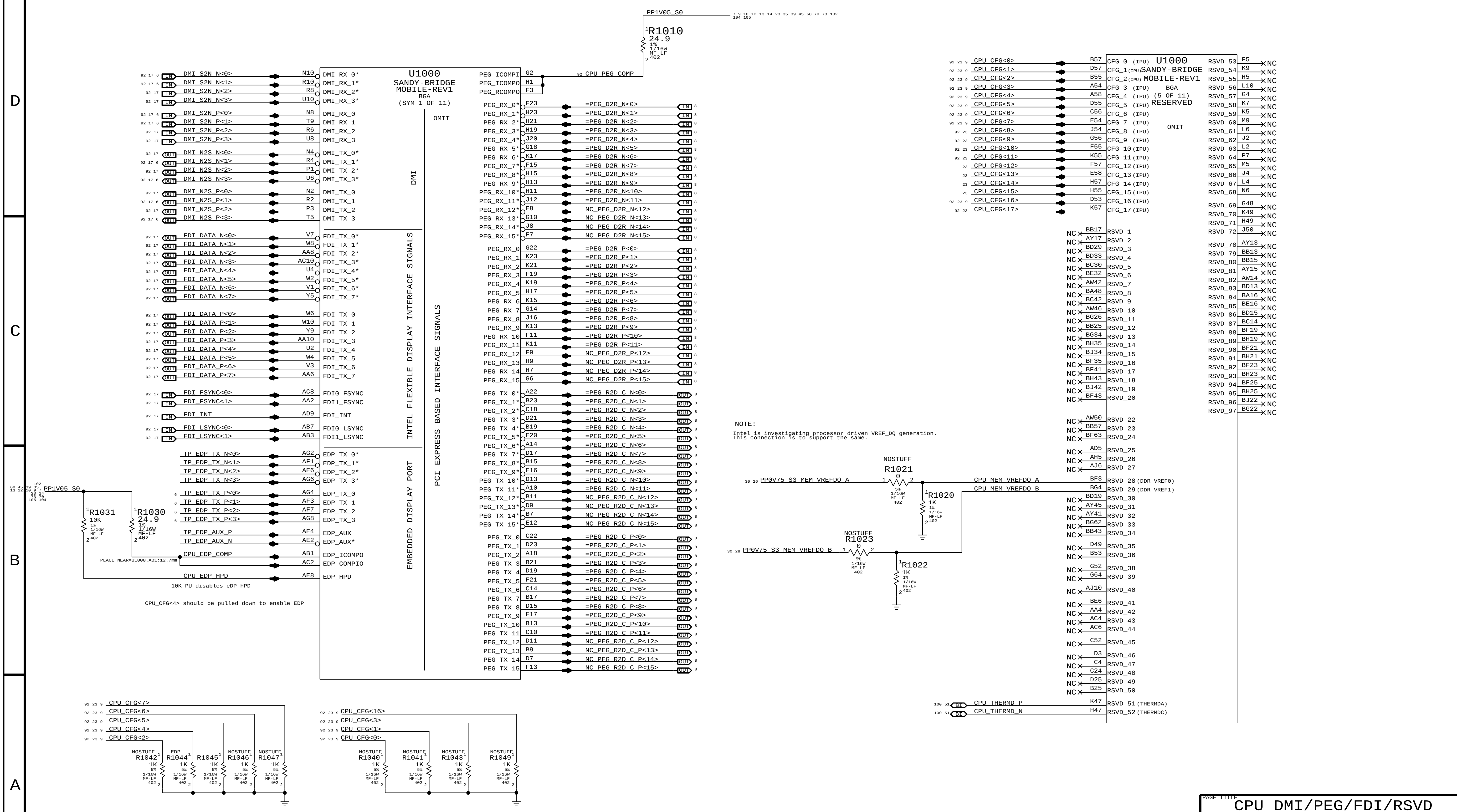
Apple Inc.

DRAWING NUMBER | SIZE D

REVISION

BRANCH

NOTICE OF PROPRIETARY PROPERTY:



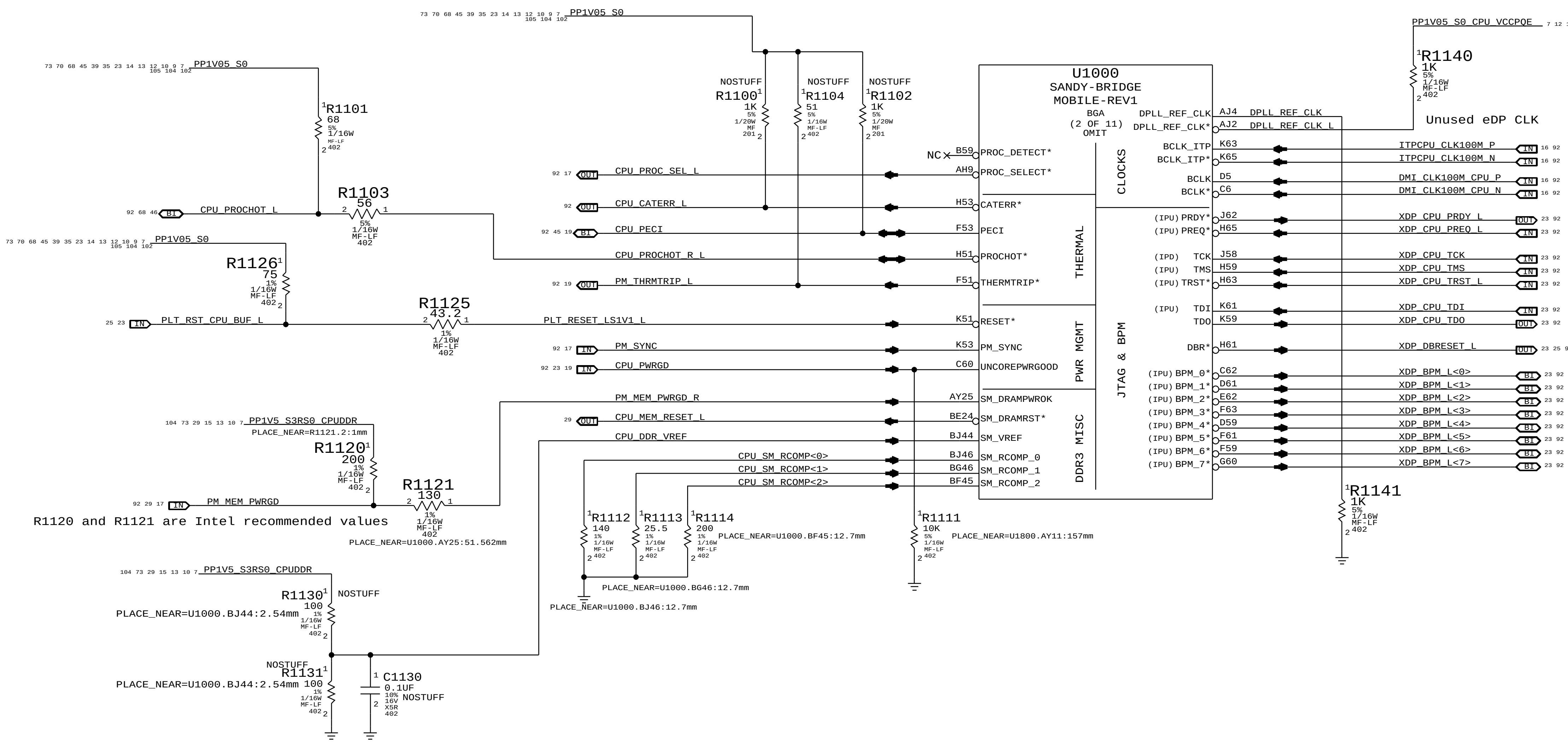
FOR SANDYBRIDGE PROCESSOR

CFG [7]	:PEG DEFER TRAINING	1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB 0 = WAIT FOR BIOS
CFG [6:5]	:PCIE BIFURCATION	11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD 00 = X8, X4, X4
CFG [4]	:eDP ENABLE/DISABLE	1 = DISABLED 0 = ENABLED
CFG [3]	:PCIE x4 LANE REVERSAL	1 = NORMAL OPERATION 0 = LANES REVERSED
CFG [2]	:PCIE x16 LANE REVERSAL	1 = NORMAL OPERATION 0 = LANES REVERSED

PAGE TITLE
CPU DMI/PEG/FDI/RSVD

Apple Inc.

DRAWING NUMBER
SIZE D
REVISION
BRANCH



CPU CLOCK/MISC/JTAG

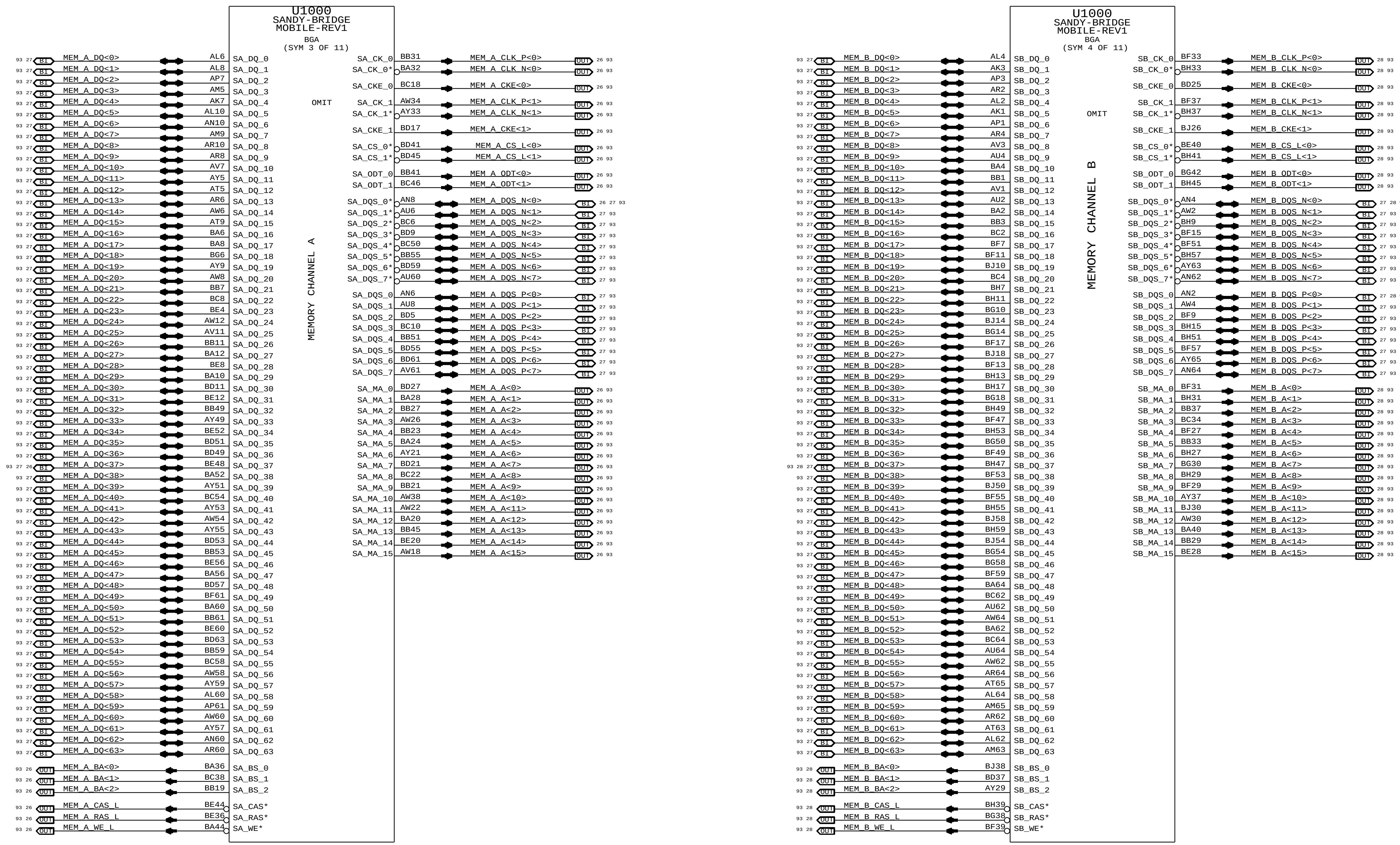
Apple Inc.

DRAWING NUMBER

SIZE D

REVISION

BRANCH



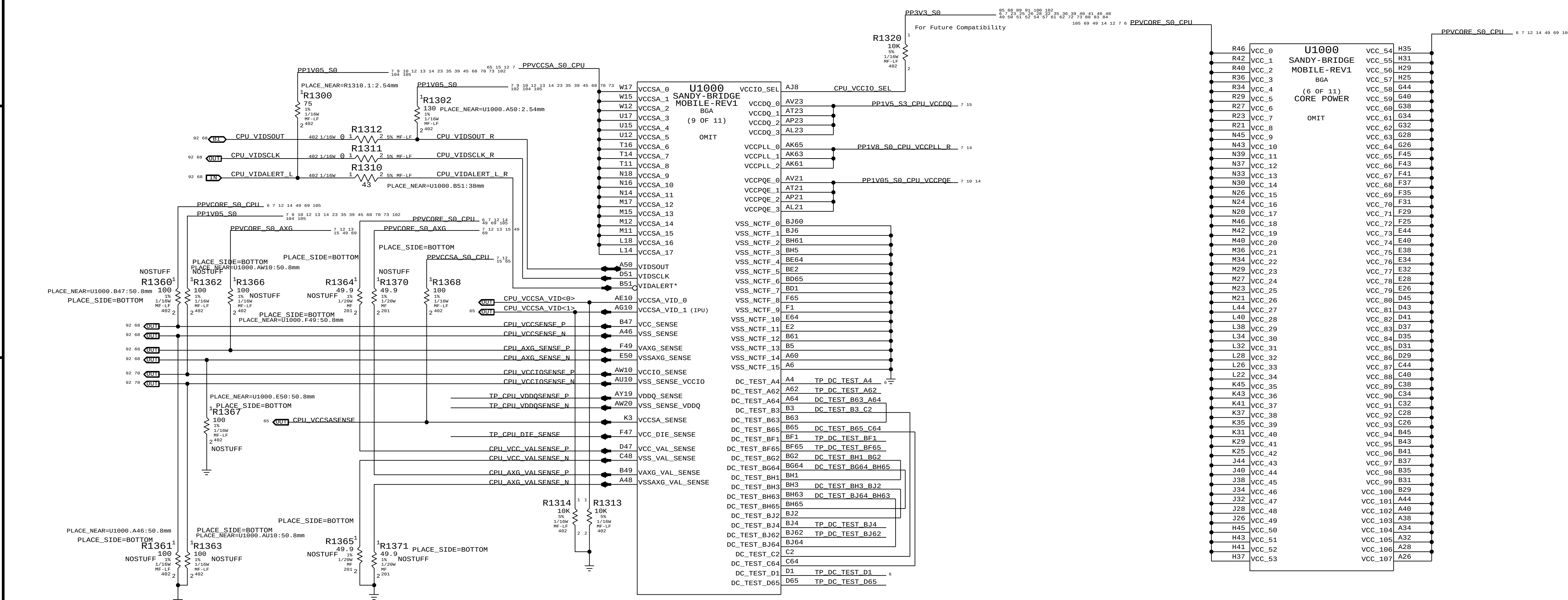
SYNC_DATE=04/26/2010

PAGE TITLE

CPU DDR3 INTERFACES

Apple Inc.

DRAWING NUMBER	SIZE
	D
REVISION	
BRANCH	
PAGE 12 OF 132	
SHEET 11 OF 105	



PLACEMENT NOTE: Please place all sense line resistors on BOTTOM side.
NOTE: Intel validation sense lines per doc 439028 rev1.0
HR_PPDG sections 6.2.1 and 6.3.1.

SYNC_MASTER=K91_MLB SYNC_DATE=07/16/2010

PAGE TITLE

CPU POWER

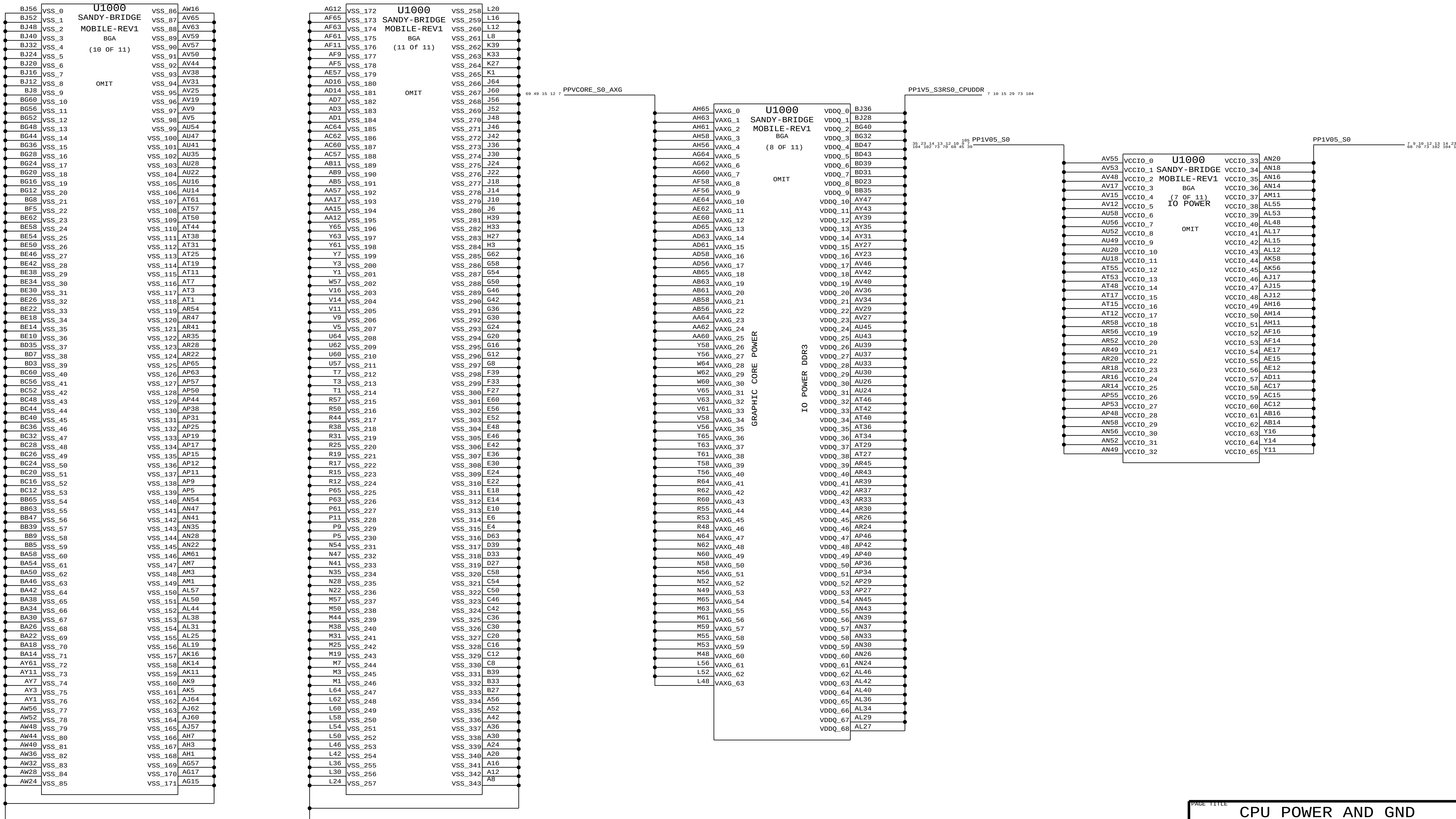
Apple Inc.

DRAWING NUMBER

SIZE D

REVISION

BRANCH



PAGE TITLE

CPU POWER AND GND

Apple Inc.

DRAWING NUMBER

SIZE D

REVISION

BRANCH

CPU VCORE DECOUPLING

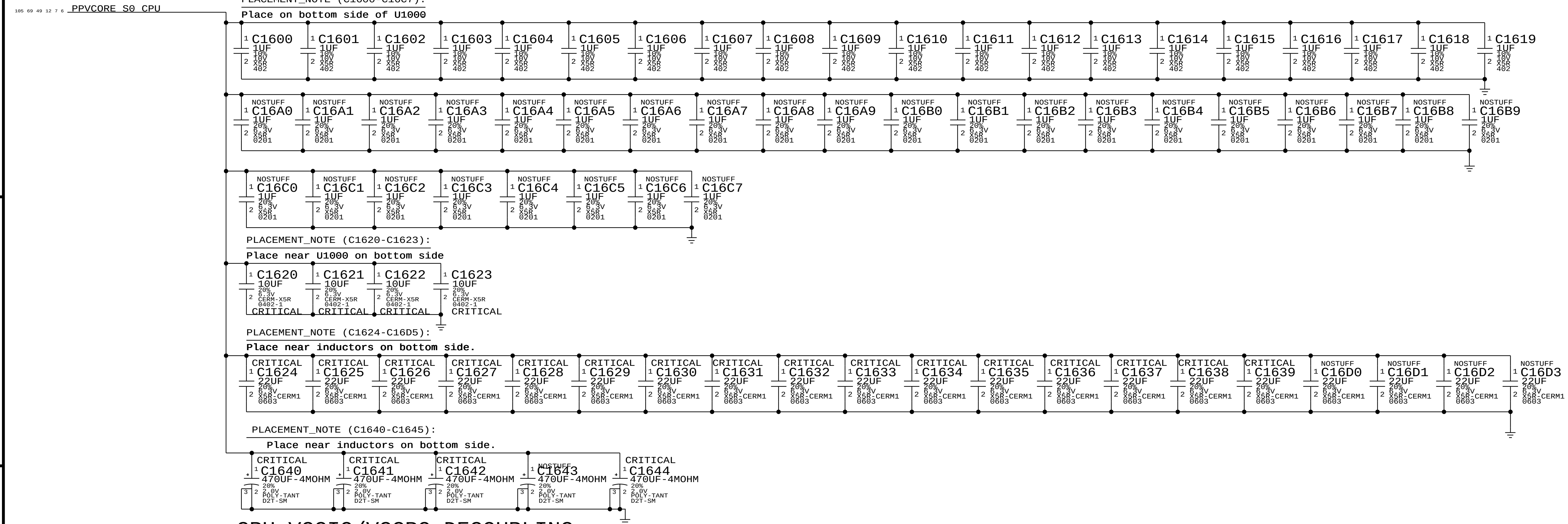
Intel recommendation: 4x 470uF 4mOhm, 2x 470uF 4mOhm (NOSTUFF), 16x 22uF 0805, 4x 10uF 0603, 20x 1uF 0402, 28x 1uF 0402 (NOSTUFF)
Apple Implementation: 4x 470uF 4mOhm, 1x 470uF 4mOhm (NOSTUFF), 16x 22uF 0603, 4x 10uF 0402, 20x 1uF 0402, 28x 1uF 0201 (NOSTUFF), 4x 22uF 0603 (NOSTUFF)

PLACEMENT_NOTE (C1600-C16C7):
Place on bottom side of U1000

PLACEMENT_NOTE (C1620-C1623):
Place near U1000 on bottom side

PLACEMENT_NOTE (C1624-C16D5):
Place near inductors on bottom side.

PLACEMENT_NOTE (C1640-C1645):
Place near inductors on bottom side.



CPU VCCIO/VCCPQ DECOUPLING

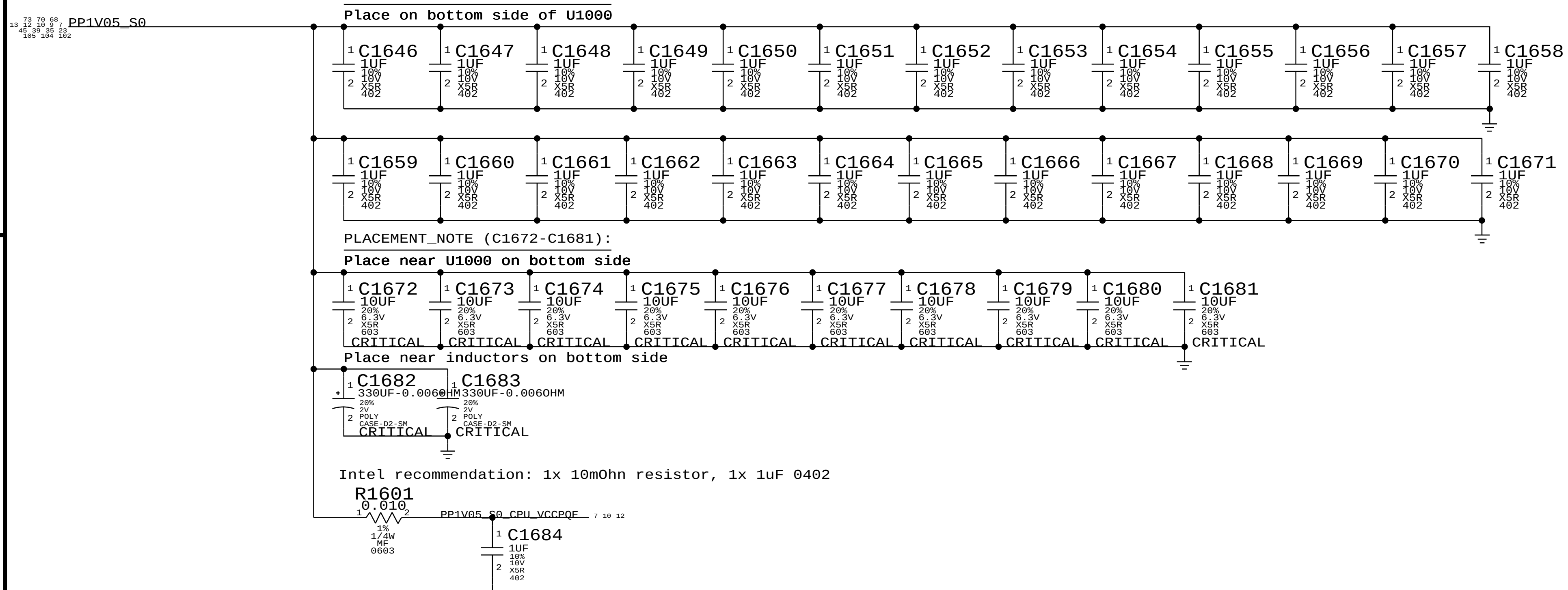
Intel recommendation: 2x 330uF, 10x 10uF 0603, 26x 1uF 0402
Apple Implementation: 2x 330uF, 10x 10uF 0603, 26x 1uF 0402

PLACEMENT_NOTE (C1646-C1671):
Place on bottom side of U1000

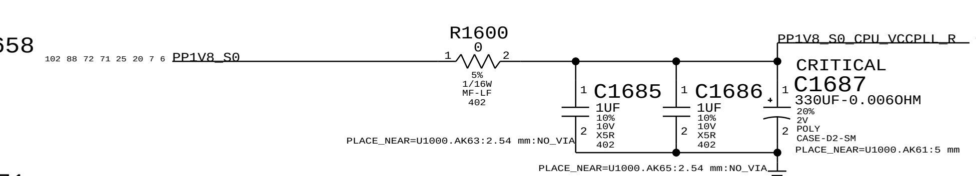
PLACEMENT_NOTE (C1672-C1681):
Place near U1000 on bottom side

Place near inductors on bottom side

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402



CPU VCCPLL DECOUPLING



CPU VCCPLL Low pass filter

SYNC_MASTER=K91_MLB SYNC_DATE=07/21/2010

PAGE TITLE: CPU DECOUPLING-I

Apple Inc.

DRAWING NUMBER | SIZE D | REVISION | BRANCH

VAXG DECOUPLING

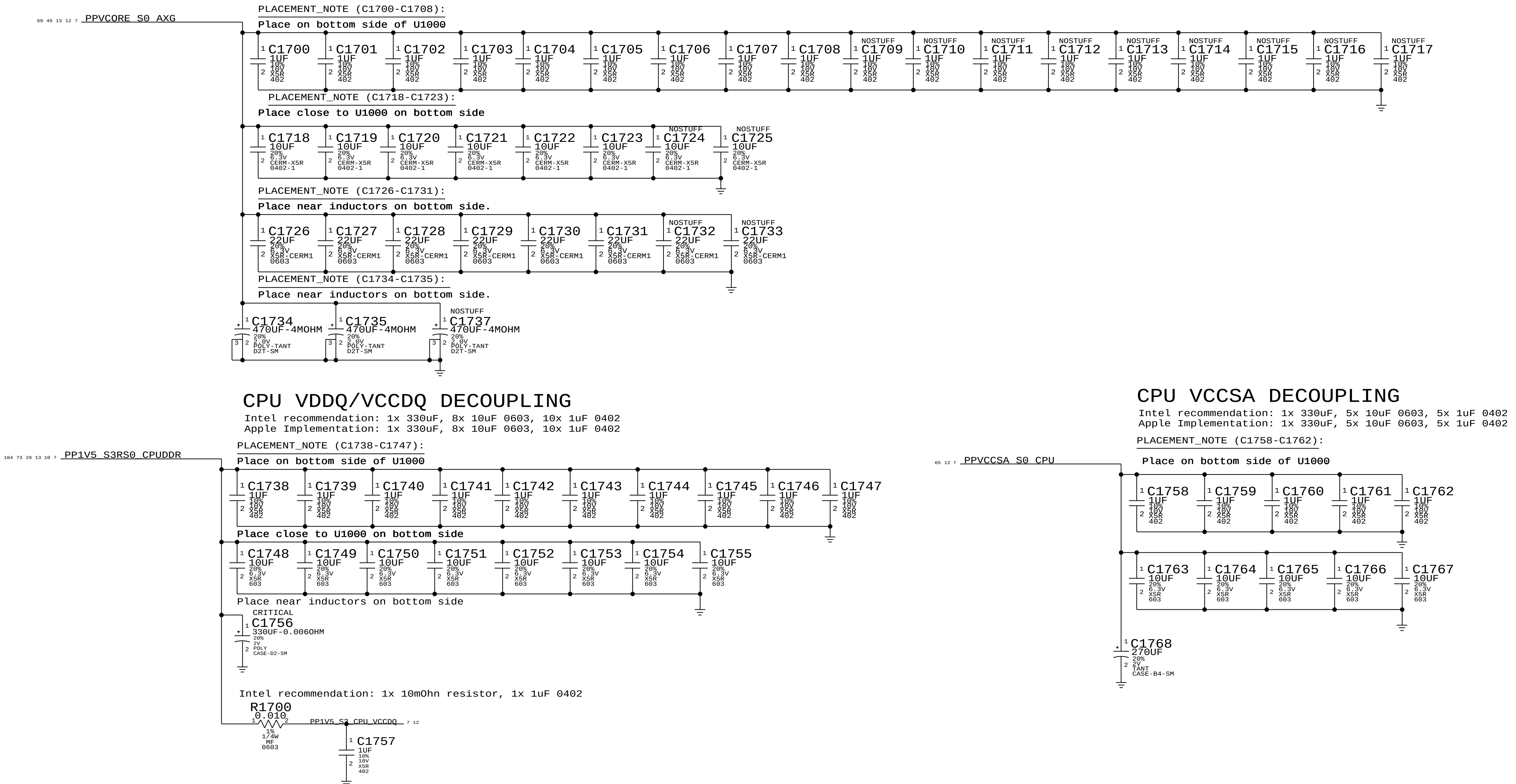
Intel recommendation: 2x 470uF 4mOhm, 2x 470uF 4mOhm (NOSTUFF), 6x 22uF 0805, 2x 22uF 0805 (NOSTUFF), 6x 10uF 0603, 2x 10uF 0603 (NOSTUFF), 9x 1uF 0402, 9x 1uF 0402 (NOSTUFF)
Apple Implementation: 2x 470uF 4mOhm, 1x 470uF 4mOhm (NOSTUFF), 6x 22uF 0603, 2x 22uF 0603 (NOSTUFF), 6x 10uF 0402, 2x 10uF 0402 (NOSTUFF), 9x 1uF 0402, 9x 1uF 0402 (NOSTUFF)

CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402
Apple Implementation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402

CPU VCCSA DECOUPLING

Intel recommendation: 1x 330uF, 5x 10uF 0603, 5x 1uF 0402
Apple Implementation: 1x 330uF, 5x 10uF 0603, 5x 1uF 0402



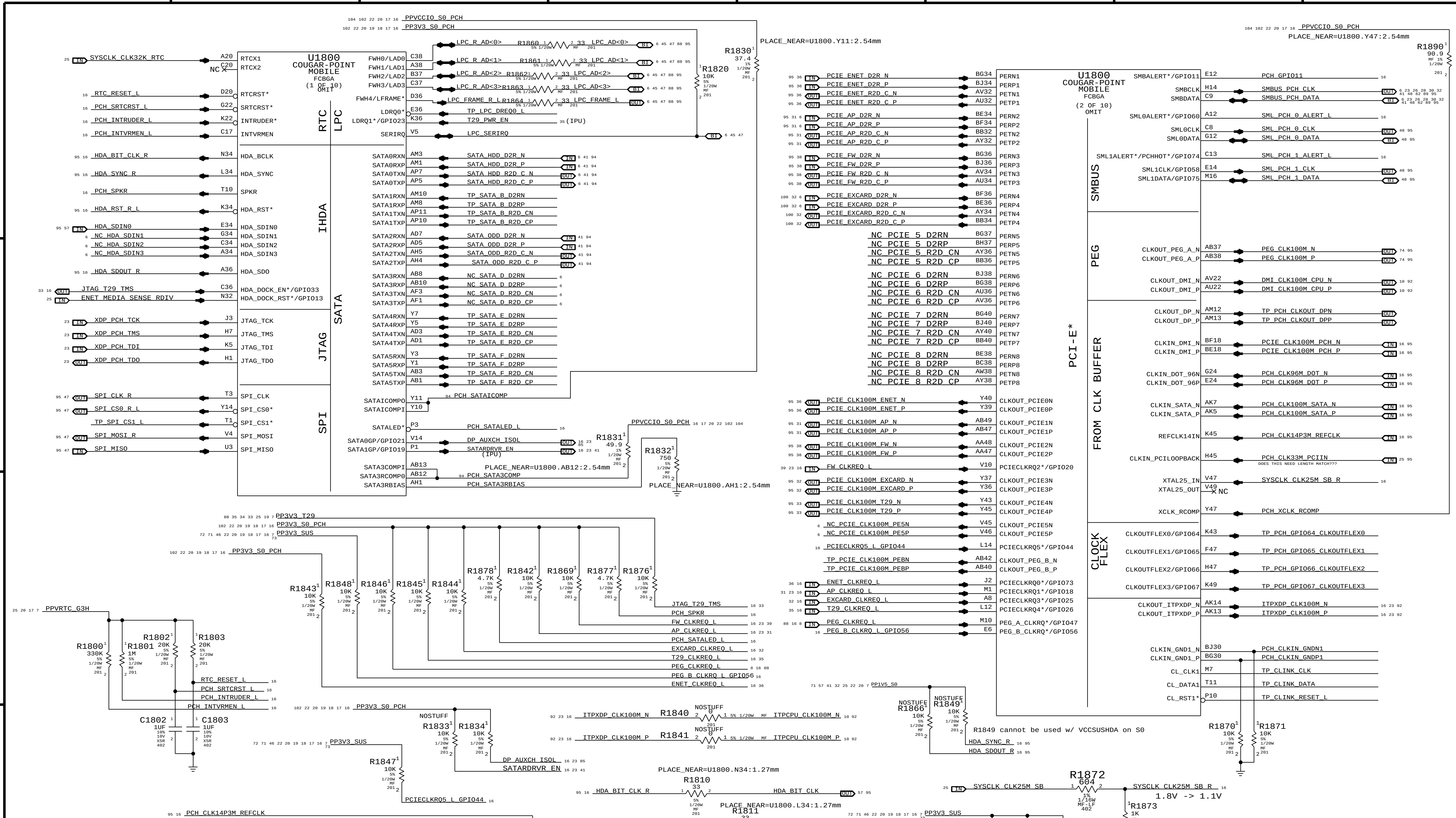
SYNC_MASTER=K91_MLB SYNC_DATE=07/21/2010

PAGE TITLE: CPU DECOUPLING-II

Apple Inc.

DRAWING NUMBER | SIZE D | REVISION | BRANCH

NOTICE OF PROPRIETARY PROPERTY:



SYNC_MASTER=K91_MLB SYNC_DATE=10/19/2010

PAGE TITLE

PCH SATA/PCIE/CLK/LPC/SPI

Apple Inc.

DRAWING NUMBER SIZE D

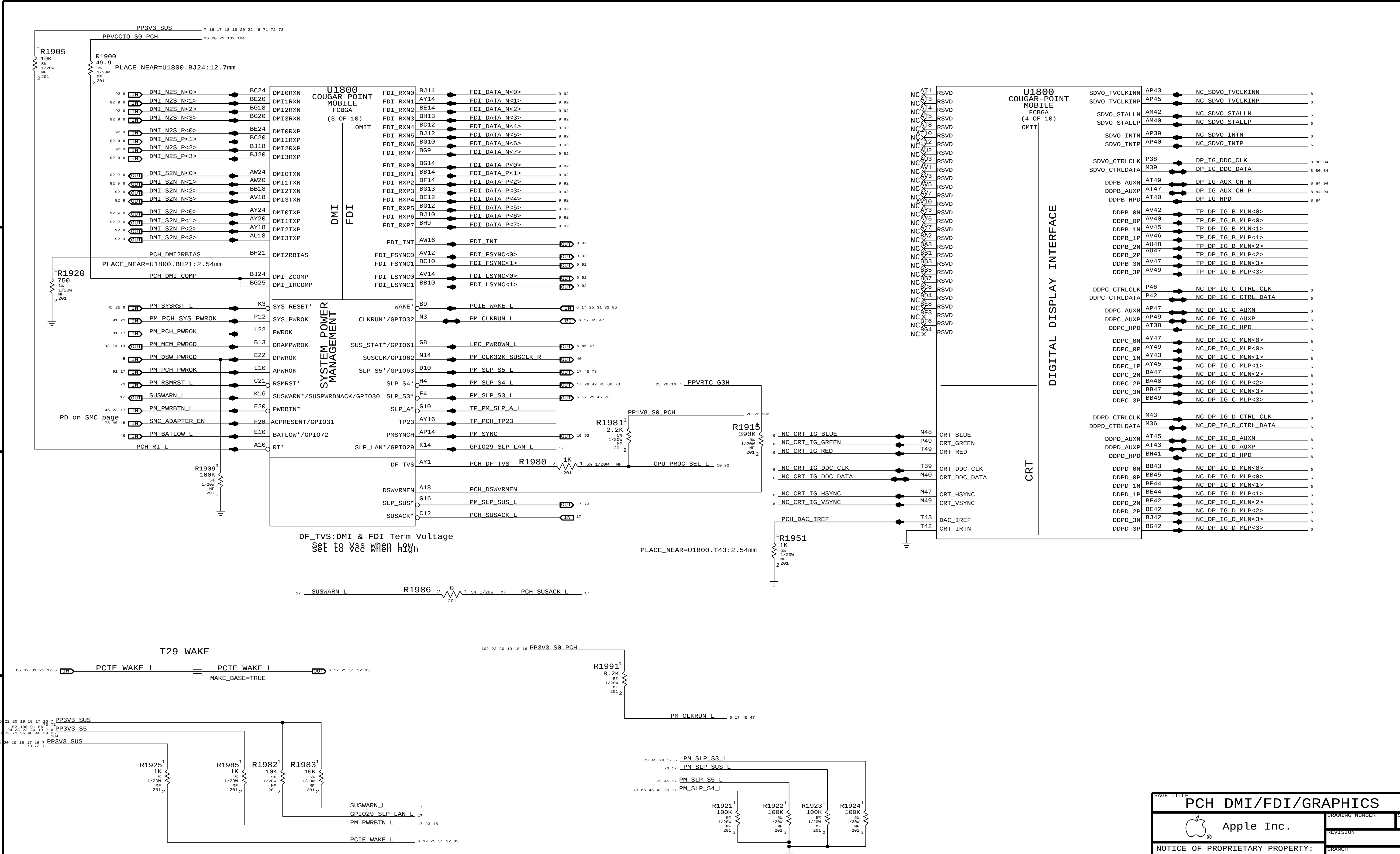
REVISION

BRANCH

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART

PAGE 18 OF 132



PAGE TITLE

PCH DMI/FDI/GRAPHICS

Apple Inc.

DRAWING NUMBER

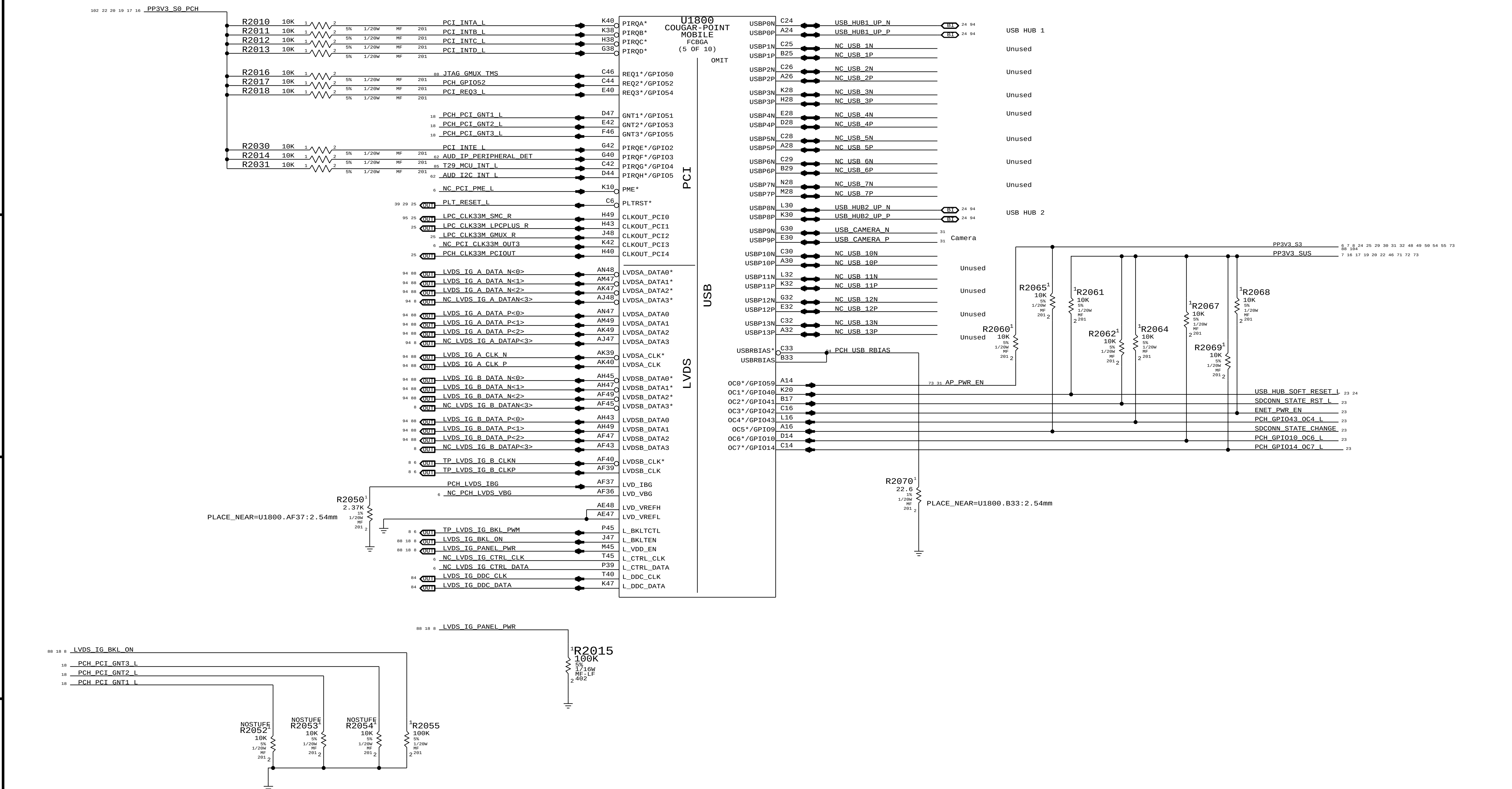
SIZE D

REVISION

BRANCH

PAGE 19 OF 132

SHEET 17 OF 105



SYNC_MASTER=K91_MLB SYNC_DATE=10/20/2010

PAGE TITLE

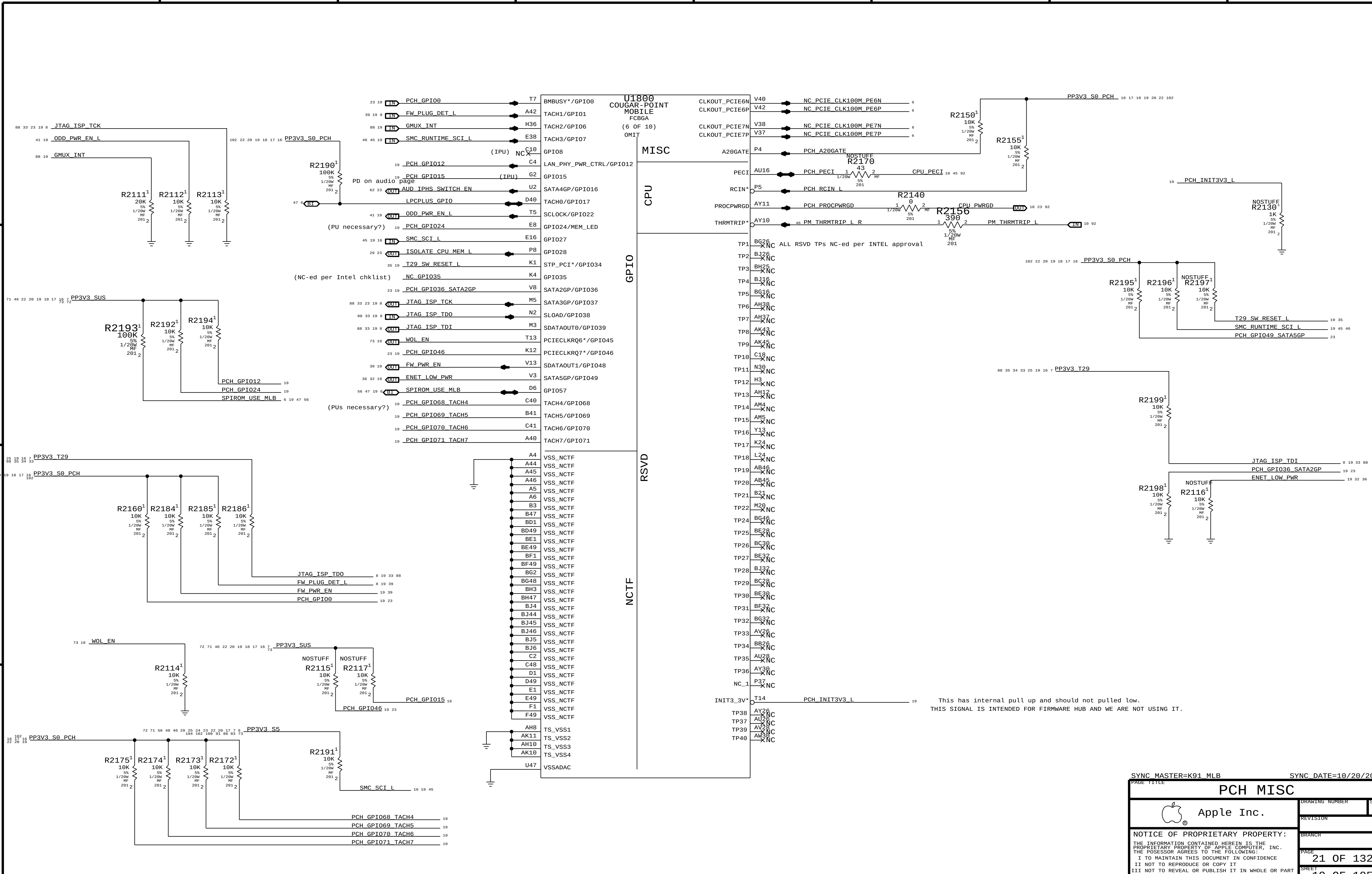
PCH PCI/FLASHCACHE/USB

Apple Inc.

DRAWING NUMBER | SIZE D

REVISION

BRANCH



SYNC_MASTER=K91_MLB SYNC_DATE=10/20/2010

PAGE TITLE

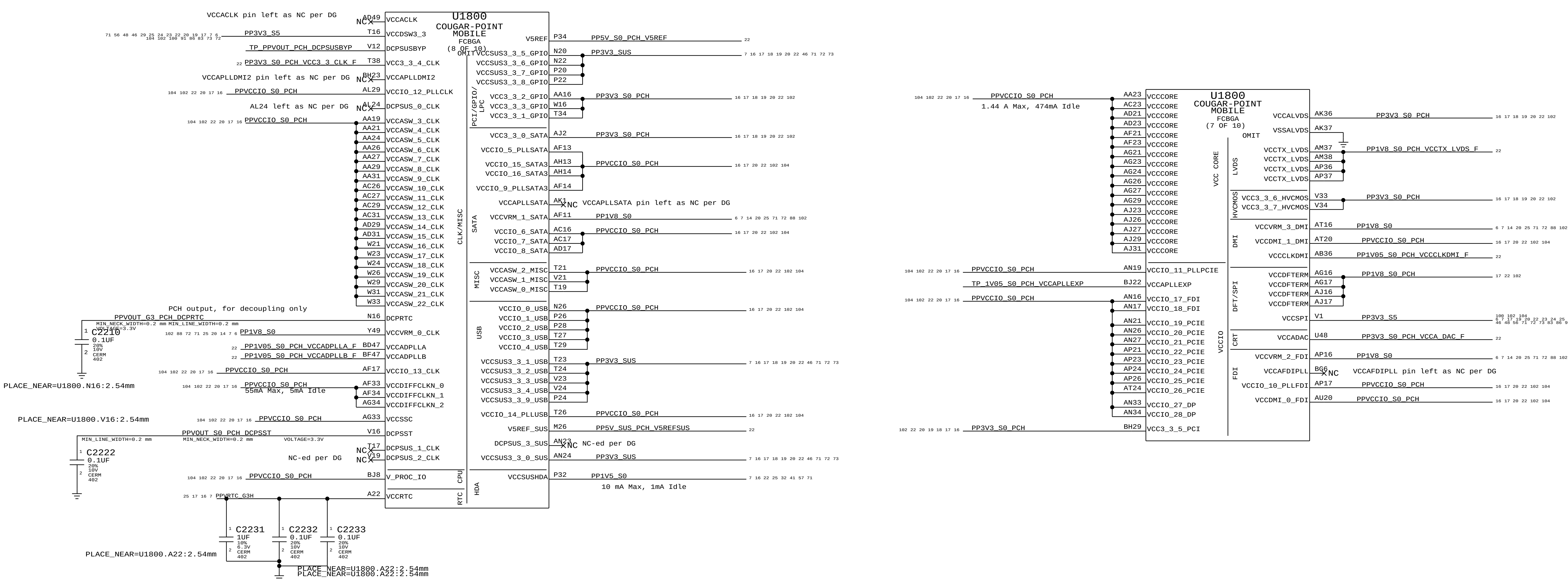
PCH MISC

Apple Inc.

DRAWING NUMBER | SIZE D

REVISION

BRANCH



PAGE TITLE
PCH POWER

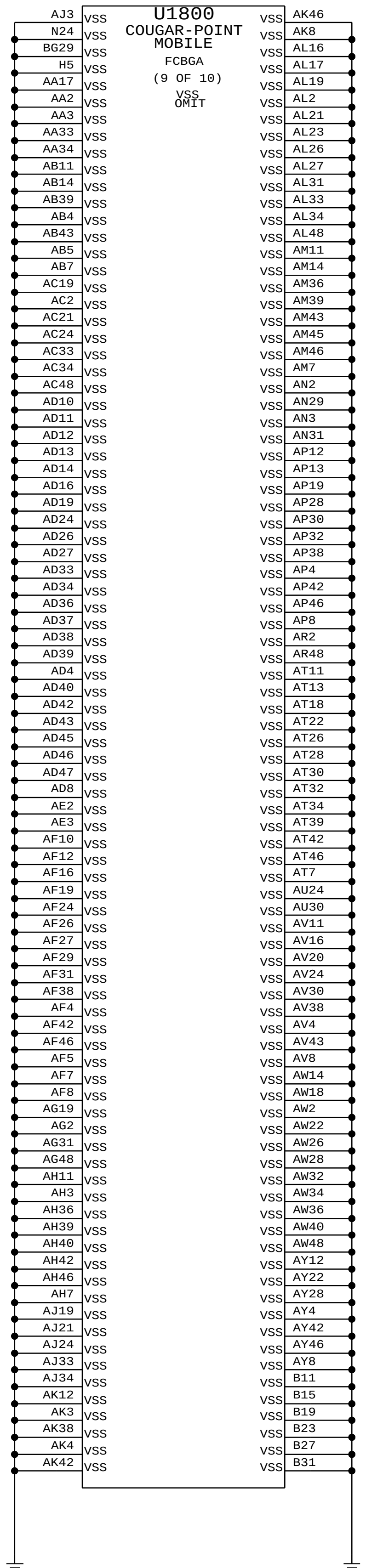
Apple Inc.

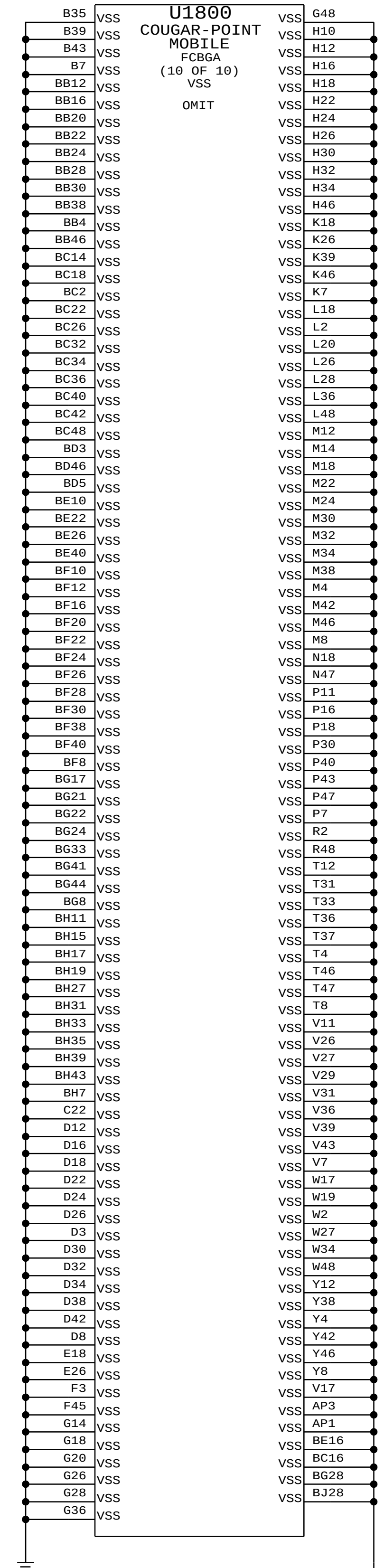
DRAWING NUMBER | SIZE D | REVISION | BRANCH

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:

I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART





SYNC_MASTER=K92_YUN SYNC_DATE=05/20/2010

PAGE TITLE

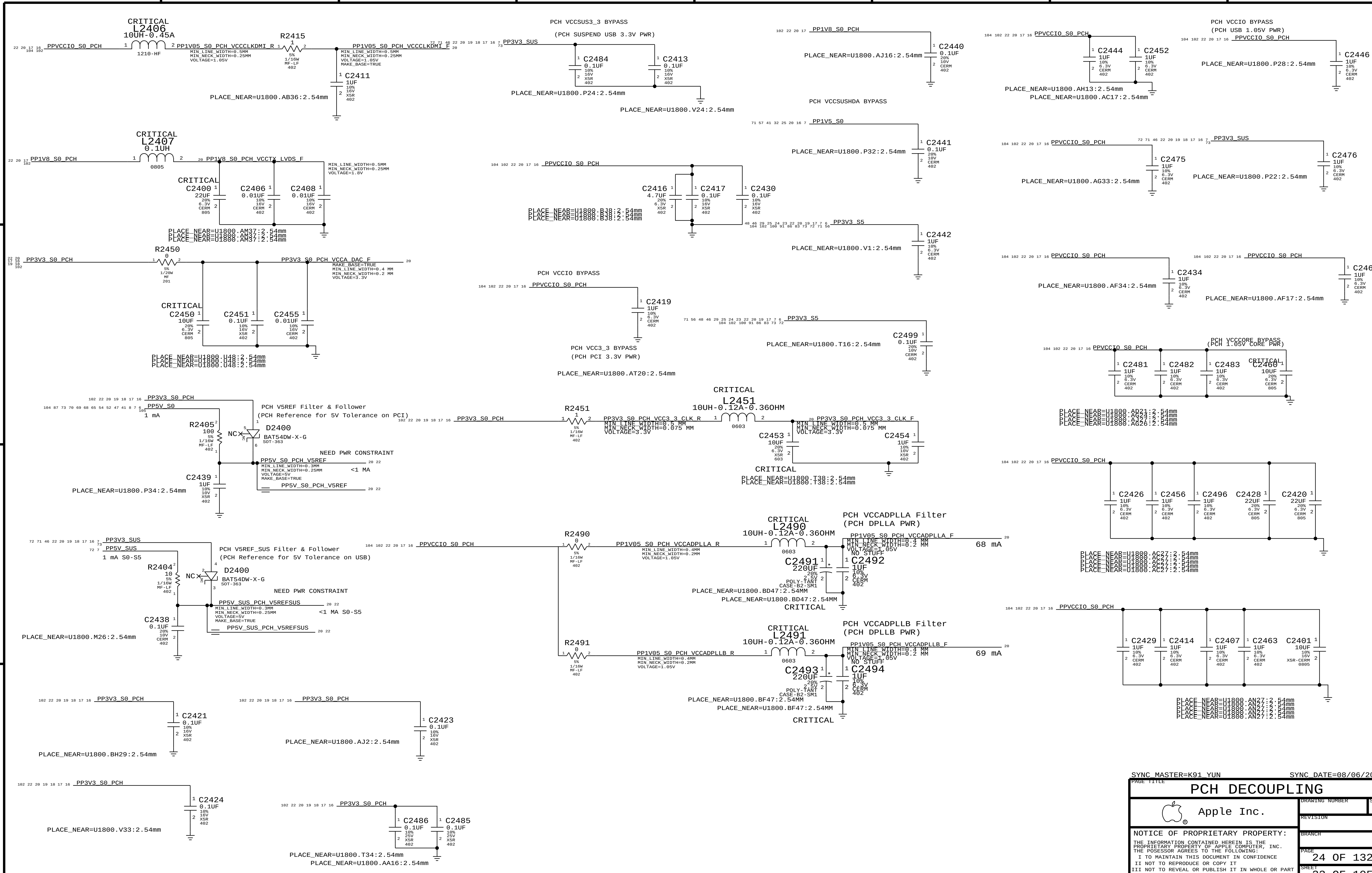
PCH GROUNDS

Apple Inc.

DRAWING NUMBER | SIZE D

REVISION

BRANCH



SYNC_MASTER=K91_YUN SYNC_DATE=08/06/2010

PAGE TITLE

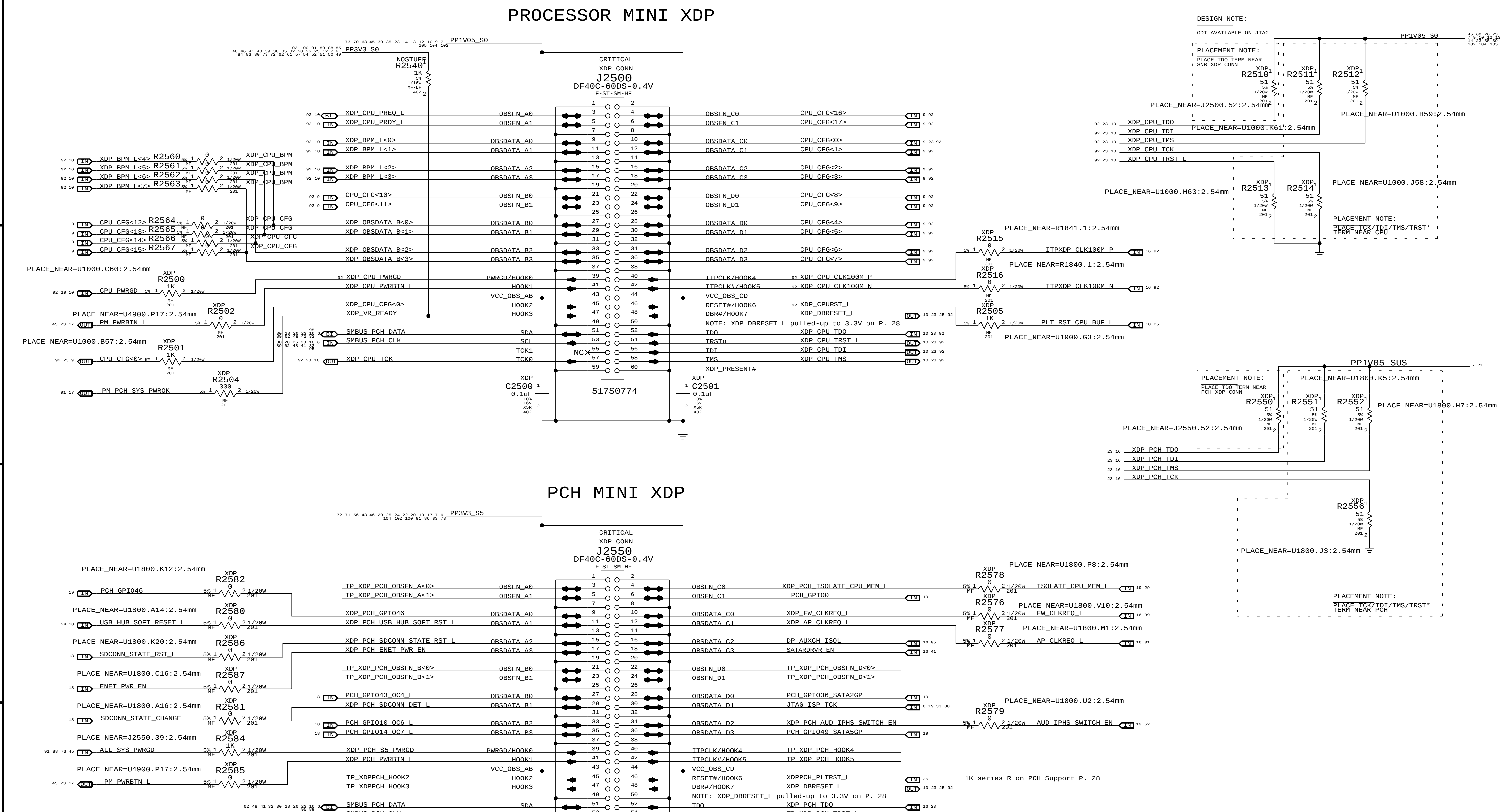
PCH DECOUPLING

Apple Inc.

DRAWING NUMBER SIZE D

REVISION

BRANCH



SYNC_MASTER=K91_MLB SYNC_DATE=10/17/2010

PAGE TITLE

CPU & PCH XDP

Apple Inc.

DRAWING NUMBER SIZE D

REVISION

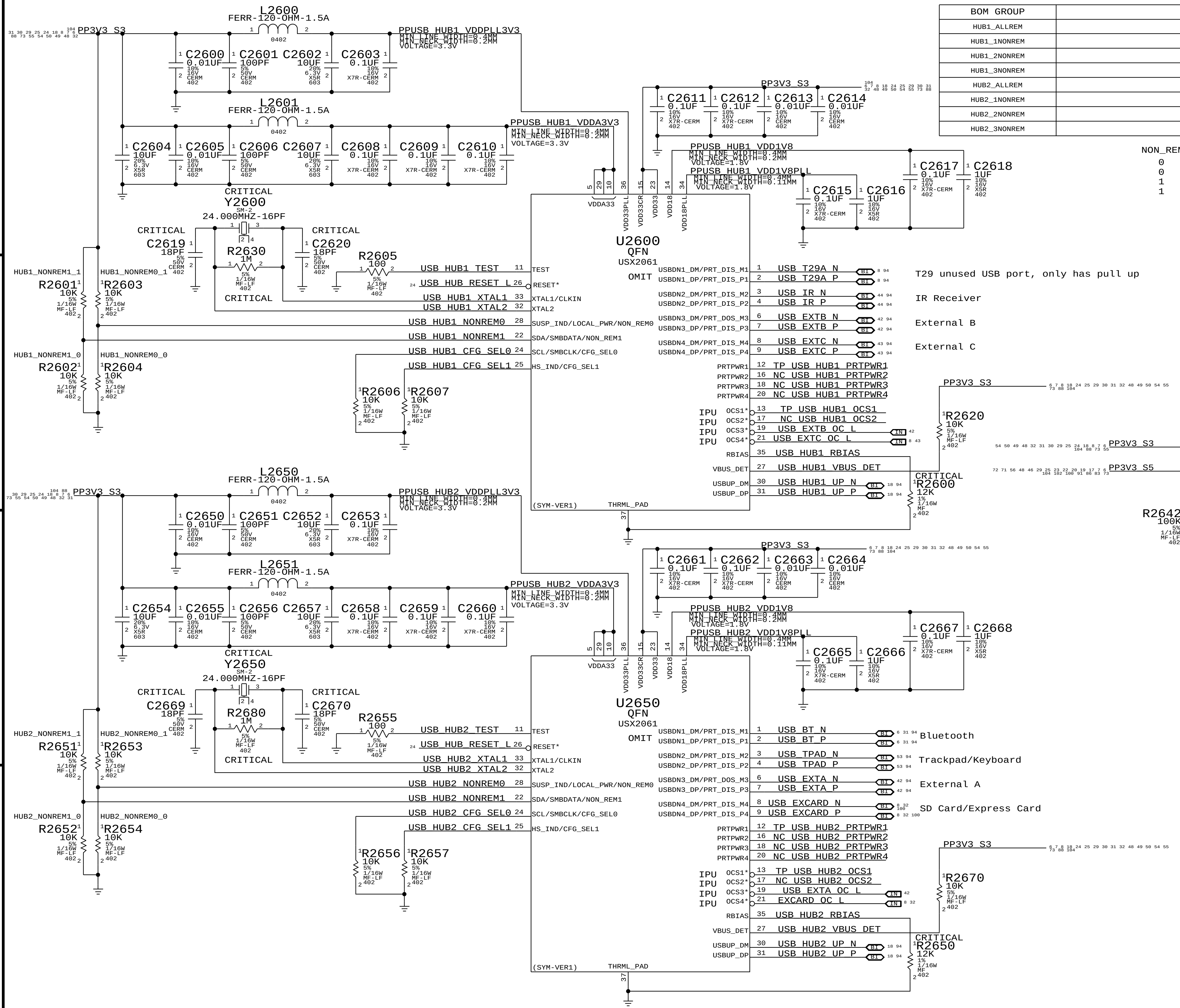
BRANCH

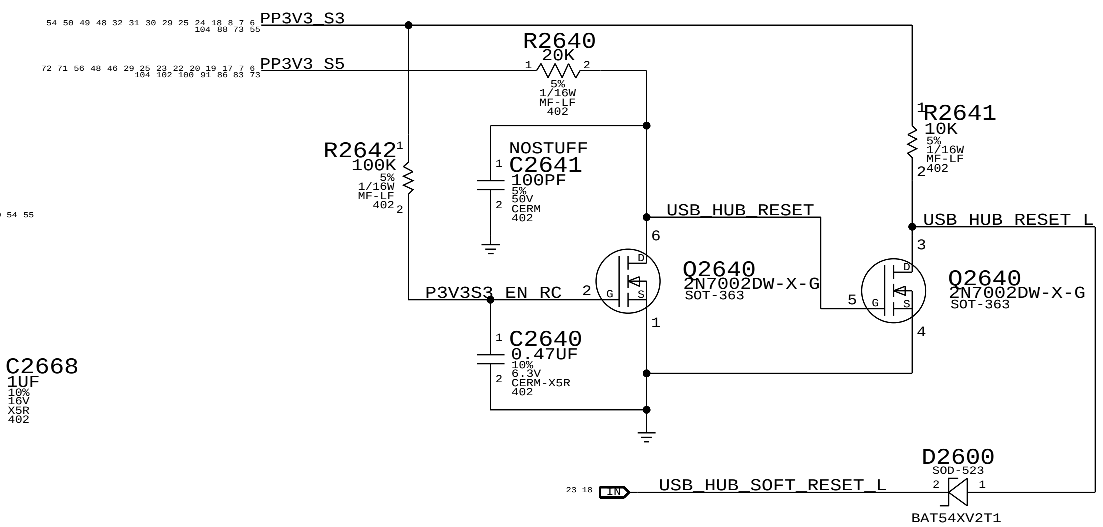
BOM GROUP	BOM OPTIONS
HUB1_ALLREM	HUB1_NONREM1_0,HUB1_NONREM0_0
HUB1_1NONREM	HUB1_NONREM1_0,HUB1_NONREM0_1
HUB1_2NONREM	HUB1_NONREM1_1,HUB1_NONREM0_0
HUB1_3NONREM	HUB1_NONREM1_1,HUB1_NONREM0_1
HUB2_ALLREM	HUB2_NONREM1_0,HUB2_NONREM0_0
HUB2_1NONREM	HUB2_NONREM1_0,HUB2_NONREM0_1
HUB2_2NONREM	HUB2_NONREM1_1,HUB2_NONREM0_0
HUB2_3NONREM	HUB2_NONREM1_1,HUB2_NONREM0_1

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0720	2	SMSC USB2514	U2600,U2650	CRITICAL	USBHUB_2514
338S0824	2	SMSC USB2514B	U2600,U2650	CRITICAL	USBHUB_2514B
338S0721	2	SMSC USX2061	U2600,U2650	CRITICAL	USBHUB_2061





SYNC_MASTER=K92_BEN SYNC_DATE=06/29/2010

PAGE TITLE

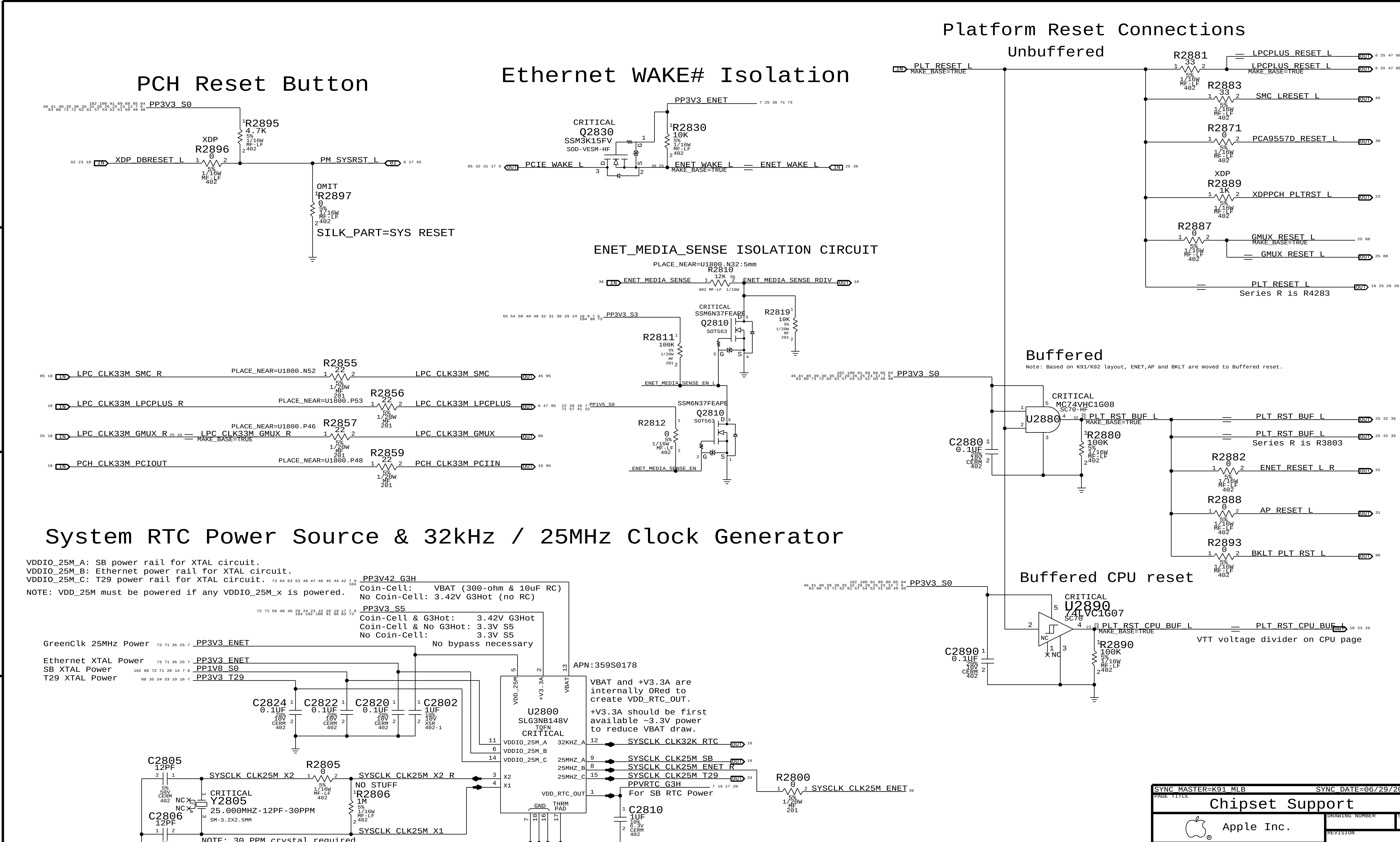
USB HUBS

Apple Inc.

DRAWING NUMBER | SIZE D

REVISION

BRANCH



SYNC_MASTER=K91_MLB SYNC_DATE=06/29/2010

PAGE TITLE

Chipset Support

Apple Inc.

DRAWING NUMBER SIZE D

REVISION

BRANCH

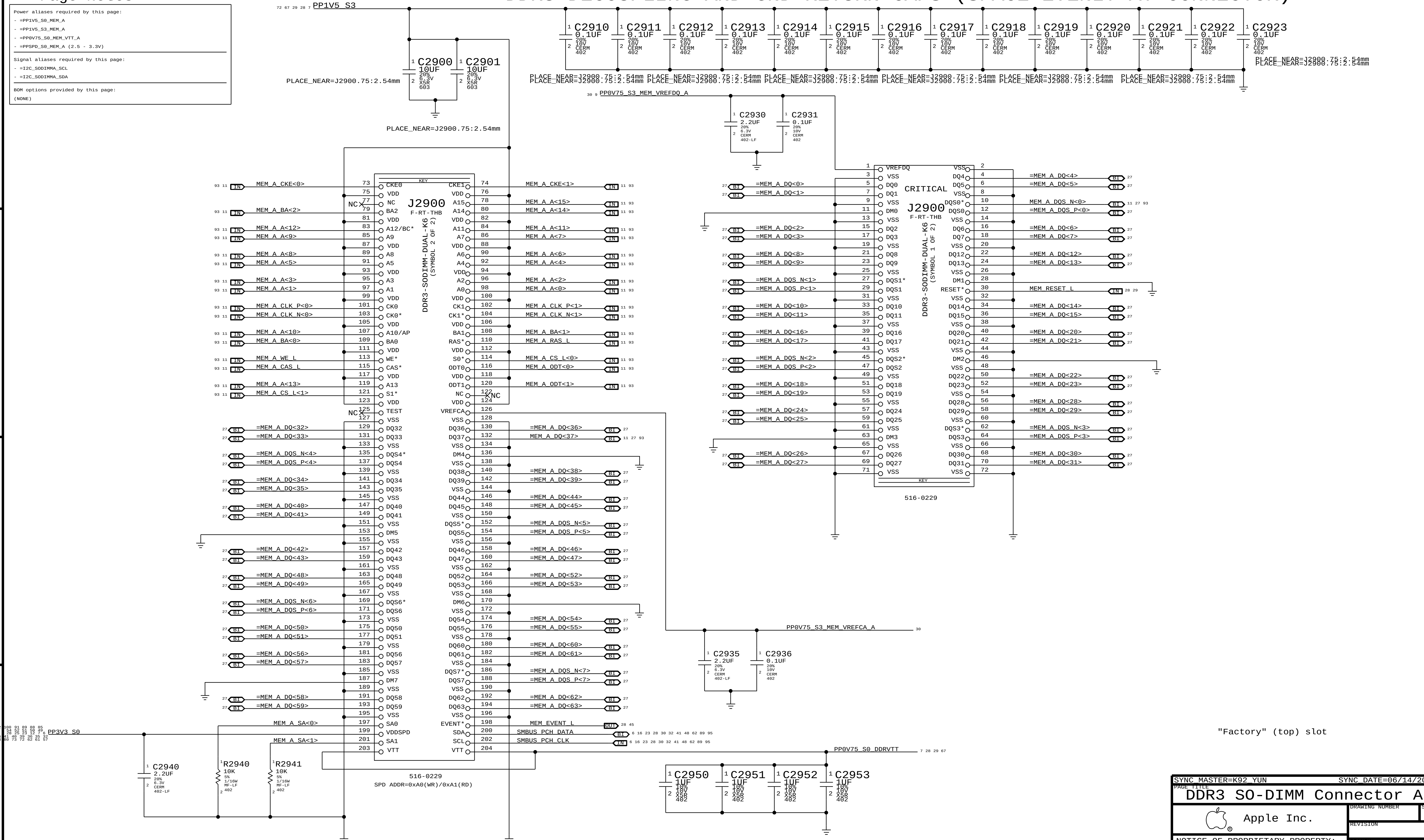
DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)



SYNC_MASTER=K92_YUN SYNC_DATE=06/14/2010

PAGE TITLE

DDR3 SO-DIMM Connector A

Apple Inc.

DRAWING NUMBER

SIZE D

REVISION

BRANCH

CPU CHANNEL A DQS 0 -> DIMM A DQS 0

93 27 26 11	MEM_A_DQS_N<0>	MAKE_BASE=TRUE	MEM_A_DQS_N<0>	11 26 27 93
93 11	MEM_A_DQS_P<0>	MAKE_BASE=TRUE	=MEM_A_DQS_P<0>	26
93 11	MEM_A_DQ<7>	MAKE_BASE=TRUE	=MEM_A_DQ<7>	26
93 11	MEM_A_DQ<6>	MAKE_BASE=TRUE	=MEM_A_DQ<6>	26
93 11	MEM_A_DQ<5>	MAKE_BASE=TRUE	=MEM_A_DQ<5>	26
93 11	MEM_A_DQ<4>	MAKE_BASE=TRUE	=MEM_A_DQ<4>	26
93 11	MEM_A_DQ<3>	MAKE_BASE=TRUE	=MEM_A_DQ<3>	26
93 11	MEM_A_DQ<2>	MAKE_BASE=TRUE	=MEM_A_DQ<2>	26
93 11	MEM_A_DQ<1>	MAKE_BASE=TRUE	=MEM_A_DQ<1>	26
93 11	MEM_A_DQ<0>	MAKE_BASE=TRUE	=MEM_A_DQ<0>	26

CPU CHANNEL A DQS 1 -> DIMM A DQS 1

93 11	MEM_A_DQS_N<1>	MAKE_BASE=TRUE	=MEM_A_DQS_N<1>	26
93 11	MEM_A_DQS_P<1>	MAKE_BASE=TRUE	=MEM_A_DQS_P<1>	26
93 11	MEM_A_DQ<15>	MAKE_BASE=TRUE	=MEM_A_DQ<15>	26
93 11	MEM_A_DQ<14>	MAKE_BASE=TRUE	=MEM_A_DQ<14>	26
93 11	MEM_A_DQ<13>	MAKE_BASE=TRUE	=MEM_A_DQ<13>	26
93 11	MEM_A_DQ<12>	MAKE_BASE=TRUE	=MEM_A_DQ<12>	26
93 11	MEM_A_DQ<11>	MAKE_BASE=TRUE	=MEM_A_DQ<11>	26
93 11	MEM_A_DQ<10>	MAKE_BASE=TRUE	=MEM_A_DQ<10>	26
93 11	MEM_A_DQ<9>	MAKE_BASE=TRUE	=MEM_A_DQ<9>	26
93 11	MEM_A_DQ<8>	MAKE_BASE=TRUE	=MEM_A_DQ<8>	26

CPU CHANNEL A DQS 2 -> DIMM A DQS 2

93 11	MEM_A_DQS_N<2>	MAKE_BASE=TRUE	=MEM_A_DQS_N<2>	26
93 11	MEM_A_DQS_P<2>	MAKE_BASE=TRUE	=MEM_A_DQS_P<2>	26
93 11	MEM_A_DQ<23>	MAKE_BASE=TRUE	=MEM_A_DQ<23>	26
93 11	MEM_A_DQ<22>	MAKE_BASE=TRUE	=MEM_A_DQ<22>	26
93 11	MEM_A_DQ<21>	MAKE_BASE=TRUE	=MEM_A_DQ<21>	26
93 11	MEM_A_DQ<20>	MAKE_BASE=TRUE	=MEM_A_DQ<20>	26
93 11	MEM_A_DQ<19>	MAKE_BASE=TRUE	=MEM_A_DQ<19>	26
93 11	MEM_A_DQ<18>	MAKE_BASE=TRUE	=MEM_A_DQ<18>	26
93 11	MEM_A_DQ<17>	MAKE_BASE=TRUE	=MEM_A_DQ<17>	26
93 11	MEM_A_DQ<16>	MAKE_BASE=TRUE	=MEM_A_DQ<16>	26

CPU CHANNEL A DQS 3 -> DIMM A DQS 3

93 11	MEM_A_DQS_N<3>	MAKE_BASE=TRUE	=MEM_A_DQS_N<3>	26
93 11	MEM_A_DQS_P<3>	MAKE_BASE=TRUE	=MEM_A_DQS_P<3>	26
93 11	MEM_A_DQ<31>	MAKE_BASE=TRUE	=MEM_A_DQ<31>	26
93 11	MEM_A_DQ<30>	MAKE_BASE=TRUE	=MEM_A_DQ<30>	26
93 11	MEM_A_DQ<29>	MAKE_BASE=TRUE	=MEM_A_DQ<29>	26
93 11	MEM_A_DQ<28>	MAKE_BASE=TRUE	=MEM_A_DQ<28>	26
93 11	MEM_A_DQ<27>	MAKE_BASE=TRUE	=MEM_A_DQ<27>	26
93 11	MEM_A_DQ<26>	MAKE_BASE=TRUE	=MEM_A_DQ<26>	26
93 11	MEM_A_DQ<25>	MAKE_BASE=TRUE	=MEM_A_DQ<25>	26
93 11	MEM_A_DQ<24>	MAKE_BASE=TRUE	=MEM_A_DQ<24>	26

CPU CHANNEL A DQS 4 -> DIMM A DQS 4

93 11	MEM_A_DQS_N<4>	MAKE_BASE=TRUE	=MEM_A_DQS_N<4>	26
93 11	MEM_A_DQS_P<4>	MAKE_BASE=TRUE	=MEM_A_DQS_P<4>	26
93 11	MEM_A_DQ<39>	MAKE_BASE=TRUE	=MEM_A_DQ<39>	26
93 11	MEM_A_DQ<38>	MAKE_BASE=TRUE	=MEM_A_DQ<38>	26
93 27 26 11	MEM_A_DQ<37>	MAKE_BASE=TRUE	MEM_A_DQ<37>	11 26 27 93
93 11	MEM_A_DQ<36>	MAKE_BASE=TRUE	=MEM_A_DQ<36>	26
93 11	MEM_A_DQ<35>	MAKE_BASE=TRUE	=MEM_A_DQ<35>	26
93 11	MEM_A_DQ<34>	MAKE_BASE=TRUE	=MEM_A_DQ<34>	26
93 11	MEM_A_DQ<33>	MAKE_BASE=TRUE	=MEM_A_DQ<33>	26
93 11	MEM_A_DQ<32>	MAKE_BASE=TRUE	=MEM_A_DQ<32>	26

CPU CHANNEL A DQS 5 -> DIMM A DQS 5

93 11	MEM_A_DQS_N<5>	MAKE_BASE=TRUE	=MEM_A_DQS_N<5>	26
93 11	MEM_A_DQS_P<5>	MAKE_BASE=TRUE	=MEM_A_DQS_P<5>	26
93 11	MEM_A_DQ<47>	MAKE_BASE=TRUE	=MEM_A_DQ<47>	26
93 11	MEM_A_DQ<46>	MAKE_BASE=TRUE	=MEM_A_DQ<46>	26
93 11	MEM_A_DQ<45>	MAKE_BASE=TRUE	=MEM_A_DQ<45>	26
93 11	MEM_A_DQ<44>	MAKE_BASE=TRUE	=MEM_A_DQ<44>	26
93 11	MEM_A_DQ<43>	MAKE_BASE=TRUE	=MEM_A_DQ<43>	26
93 11	MEM_A_DQ<42>	MAKE_BASE=TRUE	=MEM_A_DQ<42>	26
93 11	MEM_A_DQ<41>	MAKE_BASE=TRUE	=MEM_A_DQ<41>	26
93 11	MEM_A_DQ<40>	MAKE_BASE=TRUE	=MEM_A_DQ<40>	26

CPU CHANNEL A DQS 6 -> DIMM A DQS 6

93 11	MEM_A_DQS_N<6>	MAKE_BASE=TRUE	=MEM_A_DQS_N<6>	26
93 11	MEM_A_DQS_P<6>	MAKE_BASE=TRUE	=MEM_A_DQS_P<6>	26
93 11	MEM_A_DQ<55>	MAKE_BASE=TRUE	=MEM_A_DQ<55>	26
93 11	MEM_A_DQ<54>	MAKE_BASE=TRUE	=MEM_A_DQ<54>	26
93 11	MEM_A_DQ<53>	MAKE_BASE=TRUE	=MEM_A_DQ<53>	26
93 11	MEM_A_DQ<52>	MAKE_BASE=TRUE	=MEM_A_DQ<52>	26
93 11	MEM_A_DQ<51>	MAKE_BASE=TRUE	=MEM_A_DQ<51>	26
93 11	MEM_A_DQ<50>	MAKE_BASE=TRUE	=MEM_A_DQ<50>	26
93 11	MEM_A_DQ<49>	MAKE_BASE=TRUE	=MEM_A_DQ<49>	26
93 11	MEM_A_DQ<48>	MAKE_BASE=TRUE	=MEM_A_DQ<48>	26

CPU CHANNEL A DQS 7 -> DIMM A DQS 7

93 11	MEM_A_DQS_N<7>	MAKE_BASE=TRUE	=MEM_A_DQS_N<7>	26
93 11	MEM_A_DQS_P<7>	MAKE_BASE=TRUE	=MEM_A_DQS_P<7>	26
93 11	MEM_A_DQ<63>	MAKE_BASE=TRUE	=MEM_A_DQ<63>	26
93 11	MEM_A_DQ<62>	MAKE_BASE=TRUE	=MEM_A_DQ<62>	26
93 11	MEM_A_DQ<61>	MAKE_BASE=TRUE	=MEM_A_DQ<61>	26
93 11	MEM_A_DQ<60>	MAKE_BASE=TRUE	=MEM_A_DQ<60>	26
93 11	MEM_A_DQ<59>	MAKE_BASE=TRUE	=MEM_A_DQ<59>	26
93 11	MEM_A_DQ<58>	MAKE_BASE=TRUE	=MEM_A_DQ<58>	26
93 11	MEM_A_DQ<57>	MAKE_BASE=TRUE	=MEM_A_DQ<57>	26
93 11	MEM_A_DQ<56>	MAKE_BASE=TRUE	=MEM_A_DQ<56>	26

CPU CHANNEL B DQS 0 -> DIMM B DQS 0

93 28 27 11	MEM_B_DQS_N<0>	MAKE_BASE=TRUE	MEM_B_DQS_N<0>	11 27 28 93
93 28 27 11	MEM_B_DQS_P<0>	MAKE_BASE=TRUE	MEM_B_DQS_P<0>	11 27 28 93
93 11	MEM_B_DQ<7>	MAKE_BASE=TRUE	=MEM_B_DQ<7>	28
93 11	MEM_B_DQ<6>	MAKE_BASE=TRUE	=MEM_B_DQ<6>	28
93 11	MEM_B_DQ<5>	MAKE_BASE=TRUE	=MEM_B_DQ<5>	28
93 11	MEM_B_DQ<4>	MAKE_BASE=TRUE	=MEM_B_DQ<4>	28
93 11	MEM_B_DQ<3>	MAKE_BASE=TRUE	=MEM_B_DQ<3>	28
93 11	MEM_B_DQ<2>	MAKE_BASE=TRUE	=MEM_B_DQ<2>	28
93 11	MEM_B_DQ<1>	MAKE_BASE=TRUE	=MEM_B_DQ<1>	28
93 11	MEM_B_DQ<0>	MAKE_BASE=TRUE	=MEM_B_DQ<0>	28

CPU CHANNEL B DQS 1 -> DIMM B DQS 1

93 11	MEM_B_DQS_N<1>	MAKE_BASE=TRUE	=MEM_B_DQS_N<1>	28
93 11	MEM_B_DQS_P<1>	MAKE_BASE=TRUE	=MEM_B_DQS_P<1>	28
93 11	MEM_B_DQ<15>	MAKE_BASE=TRUE	=MEM_B_DQ<15>	28
93 11	MEM_B_DQ<14>	MAKE_BASE=TRUE	=MEM_B_DQ<14>	28
93 11	MEM_B_DQ<13>	MAKE_BASE=TRUE	=MEM_B_DQ<13>	28
93 11	MEM_B_DQ<12>	MAKE_BASE=TRUE	=MEM_B_DQ<12>	28
93 11	MEM_B_DQ<11>	MAKE_BASE=TRUE	=MEM_B_DQ<11>	28
93 11	MEM_B_DQ<10>	MAKE_BASE=TRUE	=MEM_B_DQ<10>	28
93 11	MEM_B_DQ<9>	MAKE_BASE=TRUE	=MEM_B_DQ<9>	28
93 11	MEM_B_DQ<8>	MAKE_BASE=TRUE	=MEM_B_DQ<8>	28

CPU CHANNEL B DQS 2 -> DIMM B DQS 2

93 11	MEM_B_DQS_N<2>	MAKE_BASE=TRUE	=MEM_B_DQS_N<2>	28
93 11	MEM_B_DQS_P<2>	MAKE_BASE=TRUE	=MEM_B_DQS_P<2>	28
93 11	MEM_B_DQ<23>	MAKE_BASE=TRUE	=MEM_B_DQ<23>	28
93 11	MEM_B_DQ<22>	MAKE_BASE=TRUE	=MEM_B_DQ<22>	28
93 11	MEM_B_DQ<21>	MAKE_BASE=TRUE	=MEM_B_DQ<21>	28
93 11	MEM_B_DQ<20>	MAKE_BASE=TRUE	=MEM_B_DQ<20>	28
93 11	MEM_B_DQ<19>	MAKE_BASE=TRUE	=MEM_B_DQ<19>	28
93 11	MEM_B_DQ<18>	MAKE_BASE=TRUE	=MEM_B_DQ<18>	28
93 11	MEM_B_DQ<17>	MAKE_BASE=TRUE	=MEM_B_DQ<17>	28
93 11	MEM_B_DQ<16>	MAKE_BASE=TRUE	=MEM_B_DQ<16>	28

CPU CHANNEL B DQS 3 -> DIMM B DQS 3

93 11	MEM_B_DQS_N<3>	MAKE_BASE=TRUE	=MEM_B_DQS_N<3>	28
93 11	MEM_B_DQS_P<3>	MAKE_BASE=TRUE	=MEM_B_DQS_P<3>	28
93 11	MEM_B_DQ<31>	MAKE_BASE=TRUE	=MEM_B_DQ<31>	28
93 11	MEM_B_DQ<30>	MAKE_BASE=TRUE	=MEM_B_DQ<30>	28
93 11	MEM_B_DQ<29>	MAKE_BASE=TRUE	=MEM_B_DQ<29>	28
93 11	MEM_B_DQ<28>	MAKE_BASE=TRUE	=MEM_B_DQ<28>	28
93 11	MEM_B_DQ<27>	MAKE_BASE=TRUE	=MEM_B_DQ<27>	28
93 11	MEM_B_DQ<26>	MAKE_BASE=TRUE	=MEM_B_DQ<26>	28
93 11	MEM_B_DQ<25>	MAKE_BASE=TRUE	=MEM_B_DQ<25>	28
93 11	MEM_B_DQ<24>	MAKE_BASE=TRUE	=MEM_B_DQ<24>	28

CPU CHANNEL B DQS 4 -> DIMM B DQS 4

93 11	MEM_B_DQS_N<4>	MAKE_BASE=TRUE	=MEM_B_DQS_N<4>	28
93 11	MEM_B_DQS_P<4>	MAKE_BASE=TRUE	=MEM_B_DQS_P<4>	28
93 11	MEM_B_DQ<39>	MAKE_BASE=TRUE	=MEM_B_DQ<39>	28
93 11	MEM_B_DQ<38>	MAKE_BASE=TRUE	=MEM_B_DQ<38>	28
93 28 27 11	MEM_B_DQ<37>	MAKE_BASE=TRUE	MEM_B_DQ<37>	11 27 28 93
93 11	MEM_B_DQ<36>	MAKE_BASE=TRUE	=MEM_B_DQ<36>	28
93 11	MEM_B_DQ<35>	MAKE_BASE=TRUE	=MEM_B_DQ<35>	28
93 11	MEM_B_DQ<34>	MAKE_BASE=TRUE	=MEM_B_DQ<34>	28
93 11	MEM_B_DQ<33>	MAKE_BASE=TRUE	=MEM_B_DQ<33>	28
93 11	MEM_B_DQ<32>	MAKE_BASE=TRUE	=MEM_B_DQ<32>	28

CPU CHANNEL B DQS 5 -> DIMM B DQS 5

93 11	MEM_B_DQS_N<5>	MAKE_BASE=TRUE	=MEM_B_DQS_N<5>	28
93 11	MEM_B_DQS_P<5>	MAKE_BASE=TRUE	=MEM_B_DQS_P<5>	28
93 11	MEM_B_DQ<47>	MAKE_BASE=TRUE	=MEM_B_DQ<47>	28
93 11	MEM_B_DQ<46>	MAKE_BASE=TRUE	=MEM_B_DQ<46>	28
93 11	MEM_B_DQ<45>	MAKE_BASE=TRUE	=MEM_B_DQ<45>	28
93 11	MEM_B_DQ<44>	MAKE_BASE=TRUE	=MEM_B_DQ<44>	28
93 11	MEM_B_DQ<43>	MAKE_BASE=TRUE	=MEM_B_DQ<43>	28
93 11	MEM_B_DQ<42>	MAKE_BASE=TRUE	=MEM_B_DQ<42>	28
93 11	MEM_B_DQ<41>	MAKE_BASE=TRUE	=MEM_B_DQ<41>	28
93 11	MEM_B_DQ<40>	MAKE_BASE=TRUE	=MEM_B_DQ<40>	28

CPU CHANNEL B DQS 6 -> DIMM B DQS 6

93 11	MEM_B_DQS_N<6>	MAKE_BASE=TRUE	=MEM_B_DQS_N<6>	28
93 11	MEM_B_DQS_P<6>	MAKE_BASE=TRUE	=MEM_B_DQS_P<6>	28
93 11	MEM_B_DQ<55>	MAKE_BASE=TRUE	=MEM_B_DQ<55>	28
93 11	MEM_B_DQ<54>	MAKE_BASE=TRUE	=MEM_B_DQ<54>	28
93 11	MEM_B_DQ<53>	MAKE_BASE=TRUE	=MEM_B_DQ<53>	28
93 11	MEM_B_DQ<52>	MAKE_BASE=TRUE	=MEM_B_DQ<52>	28
93 11	MEM_B_DQ<51>	MAKE_BASE=TRUE	=MEM_B_DQ<51>	28
93 11	MEM_B_DQ<50>	MAKE_BASE=TRUE	=MEM_B_DQ<50>	28
93 11	MEM_B_DQ<49>	MAKE_BASE=TRUE	=MEM_B_DQ<49>	28
93 11	MEM_B_DQ<48>	MAKE_BASE=TRUE	=MEM_B_DQ<48>	28

CPU CHANNEL B DQS 7 -> DIMM B DQS 7

93 11	MEM_B_DQS_N<7>	MAKE_BASE=TRUE	=MEM_B_DQS_N<7>	28
93 11	MEM_B_DQS_P<7>	MAKE_BASE=TRUE	=MEM_B_DQS_P<7>	28
93 11	MEM_B_DQ<63>	MAKE_BASE=TRUE	=MEM_B_DQ<63>	28
93 11	MEM_B_DQ<62>	MAKE_BASE=TRUE	=MEM_B_DQ<62>	28
93 11	MEM_B_DQ<61>	MAKE_BASE=TRUE	=MEM_B_DQ<61>	28
93 11	MEM_B_DQ<60>	MAKE_BASE=TRUE	=MEM_B_DQ<60>	28
93 11	MEM_B_DQ<59>	MAKE_BASE=TRUE	=MEM_B_DQ<59>	28
93 11	MEM_B_DQ<58>	MAKE_BASE=TRUE	=MEM_B_DQ<58>	28
93 11	MEM_B_DQ<57>	MAKE_BASE=TRUE	=MEM_B_DQ<57>	28
93 11	MEM_B_DQ<56>	MAKE_BASE=TRUE	=MEM_B_DQ<56>	28

Page Notes

Power aliases required by this page:

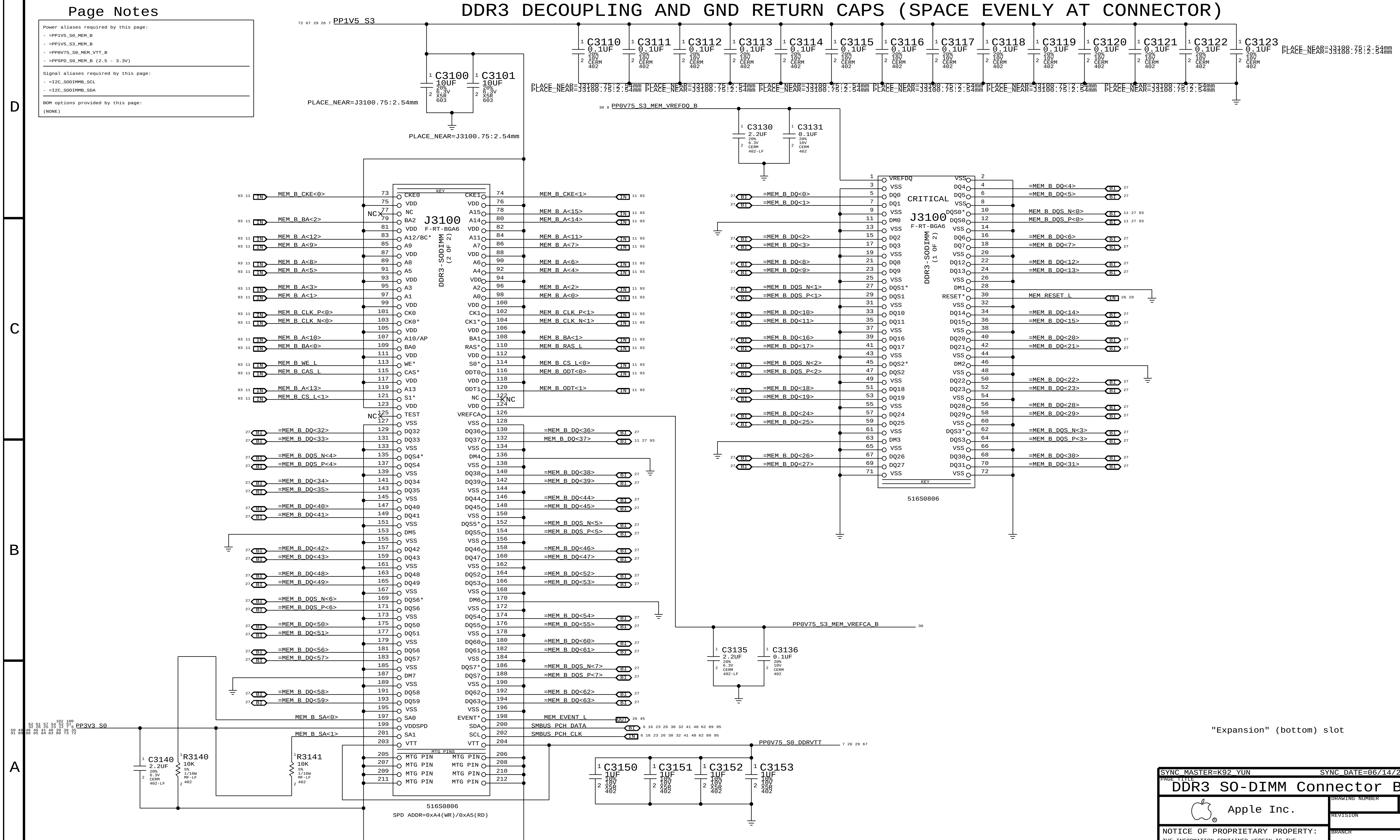
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:

- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:

(NONE)



SYNC_MASTER=K92_YUN SYNC_DATE=06/14/2010

PAGE TITLE
DDR3 SO-DIMM Connector B

Apple Inc.

DRAWING NUMBER | SIZE D

REVISION

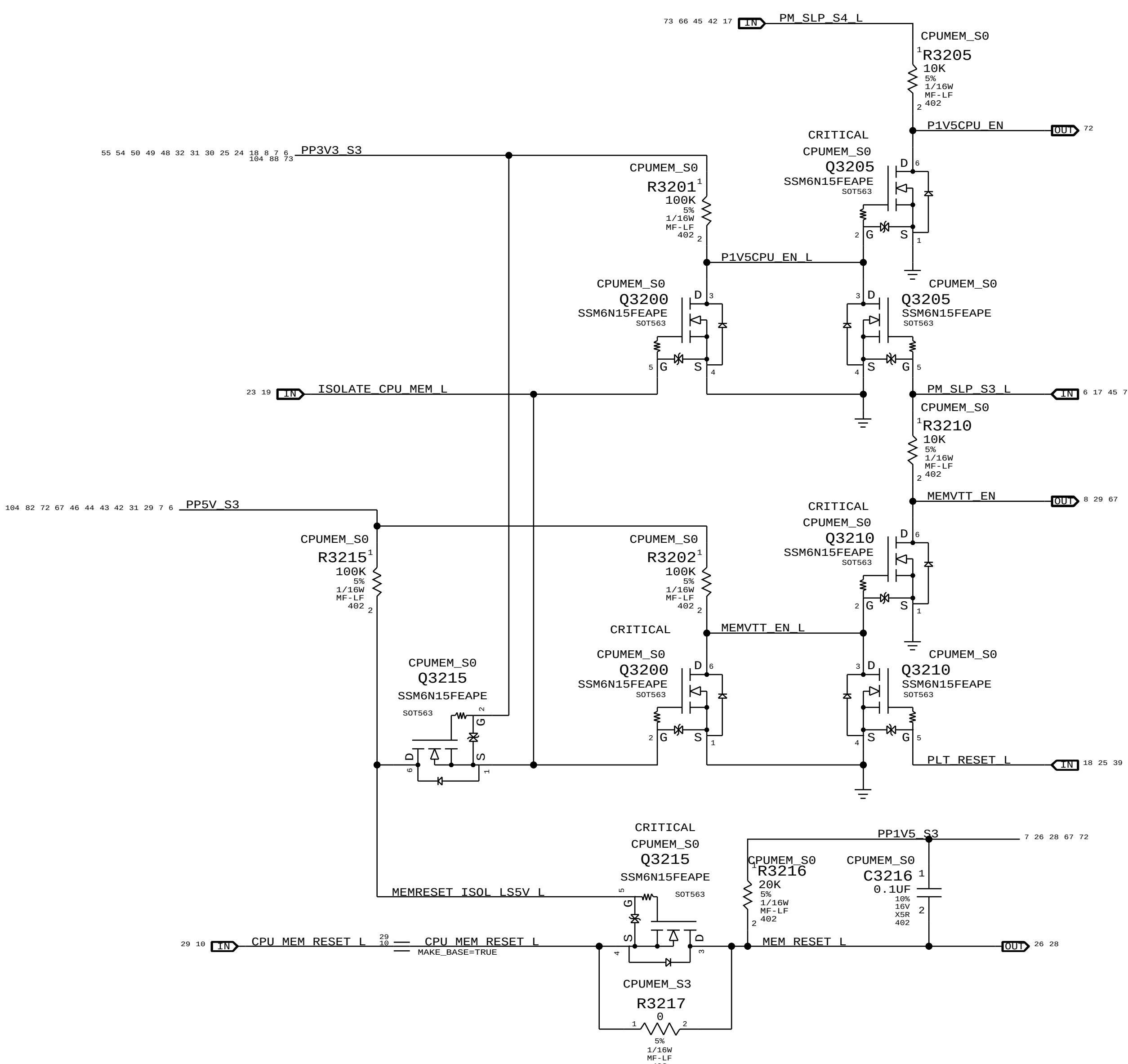
BRANCH

NOTICE OF PROPRIETARY PROPERTY:

The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

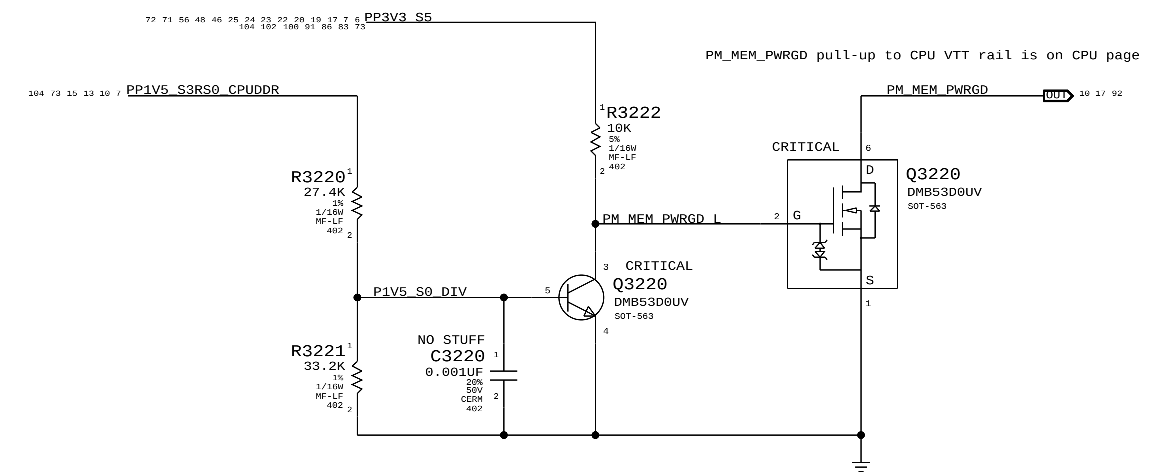


Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0 0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
to 1	0	1	1	1	1	1	1	1
2	0	0	1	1	1	1	0	1
S3 3	0	0	0	1	X	1	0	0
4	0	0	1	1	X	1	0	1
to 5	0	1	1	1	0 (*)	1	1	1
6	0	1	1	1	1	1	1	1
S0 7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

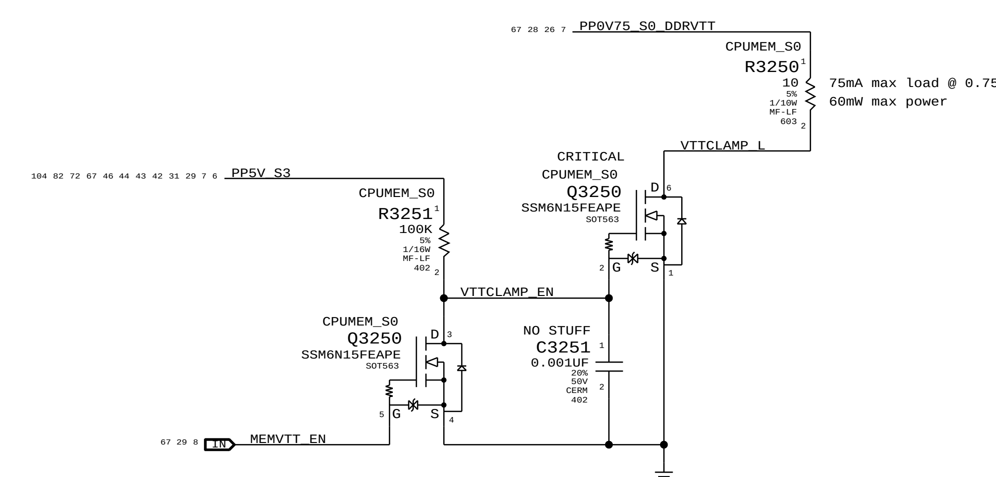
NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



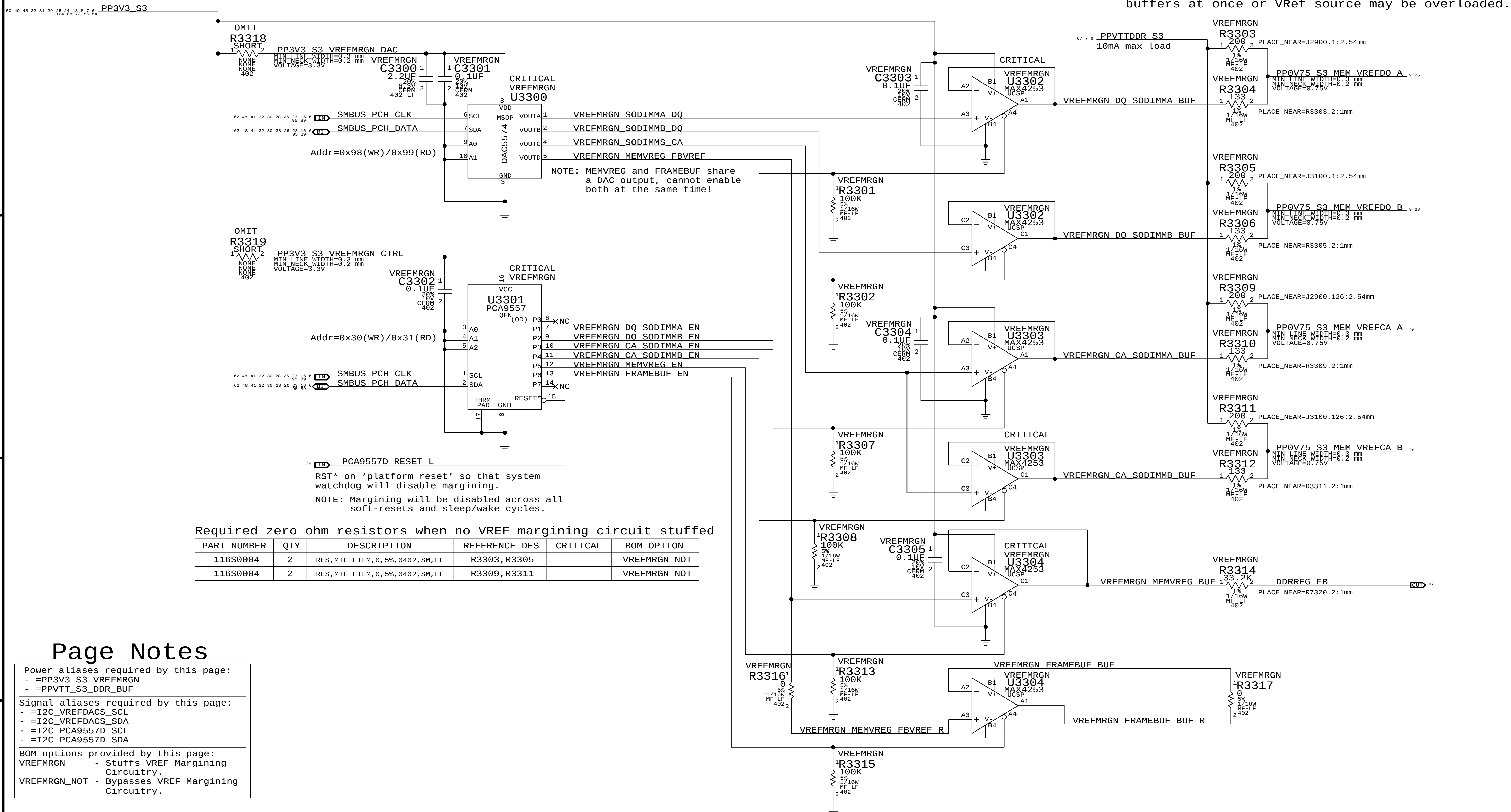
SYNC_MASTER=K17_MLB SYNC_DATE=04/26/2010

PAGE TITLE: CPU Memory S3 Support

Apple Inc.

DRAWING NUMBER | SIZE D | REVISION | BRANCH

NOTE: Must not enable more than two SO-DIMM margining buffers at once or VRef source may be overloaded.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3303,R3305		VREFMRGN_NOT
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3309,R3311		VREFMRGN_NOT

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN - Stuffs VREF Margining Circuitry.
VREFMRGN_NOT - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC_MASTER=K91_YUN SYNC_DATE=08/26/2010

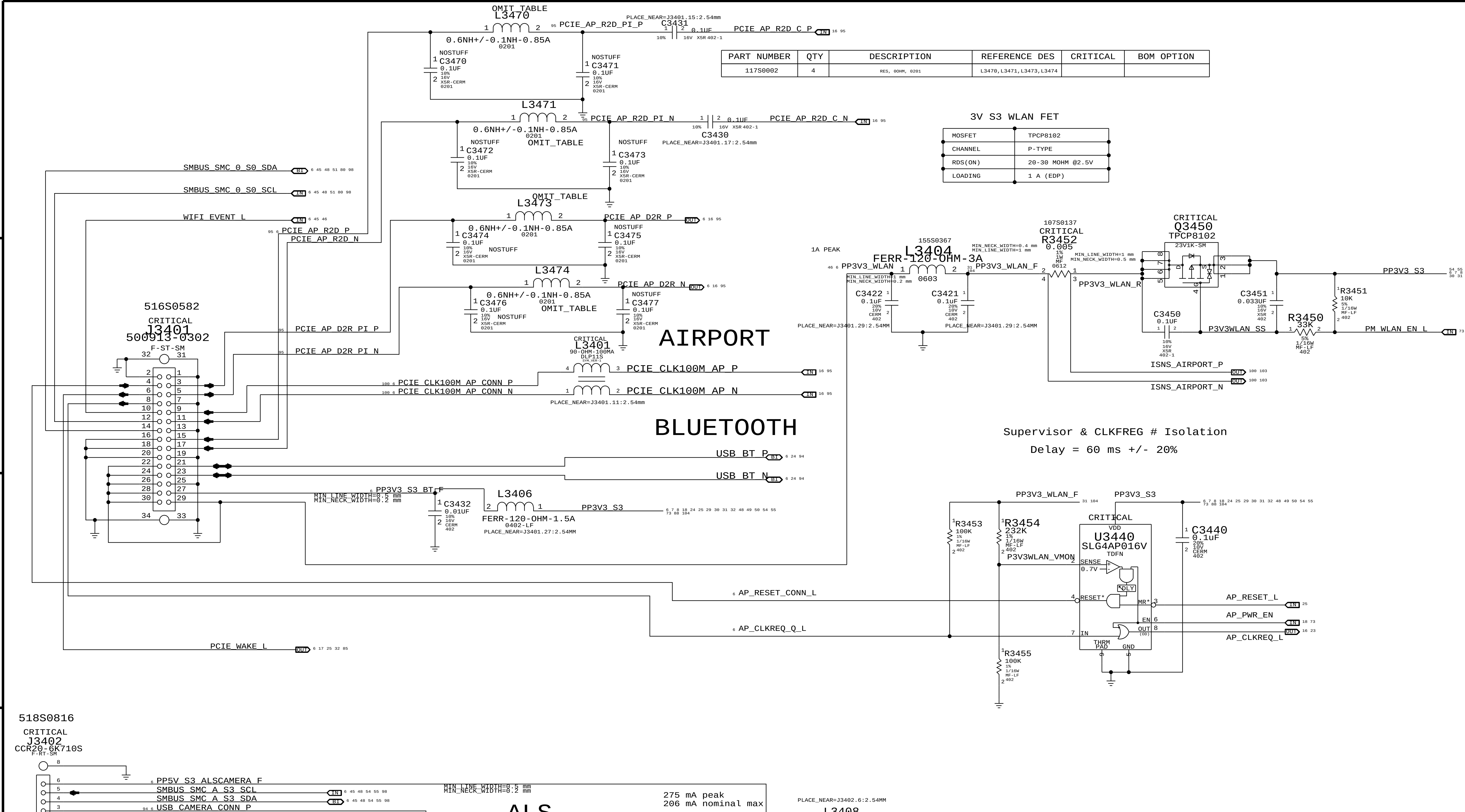
PAGE TITLE
FSB/DDR3/FRAMEBUF Vref Margining

Apple Inc.

DRAWING NUMBER SIZE D

REVISION

BRANCH



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	4	RES, 0OHM, 0201	L3470,L3471,L3473,L3474		

3V S3 WLAN FET

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	20-30 MOHM @2.5V
LOADING	1 A (EDP)

SYNC_MASTER=K91_MLB SYNC_DATE=10/21/2010

PAGE TITLE

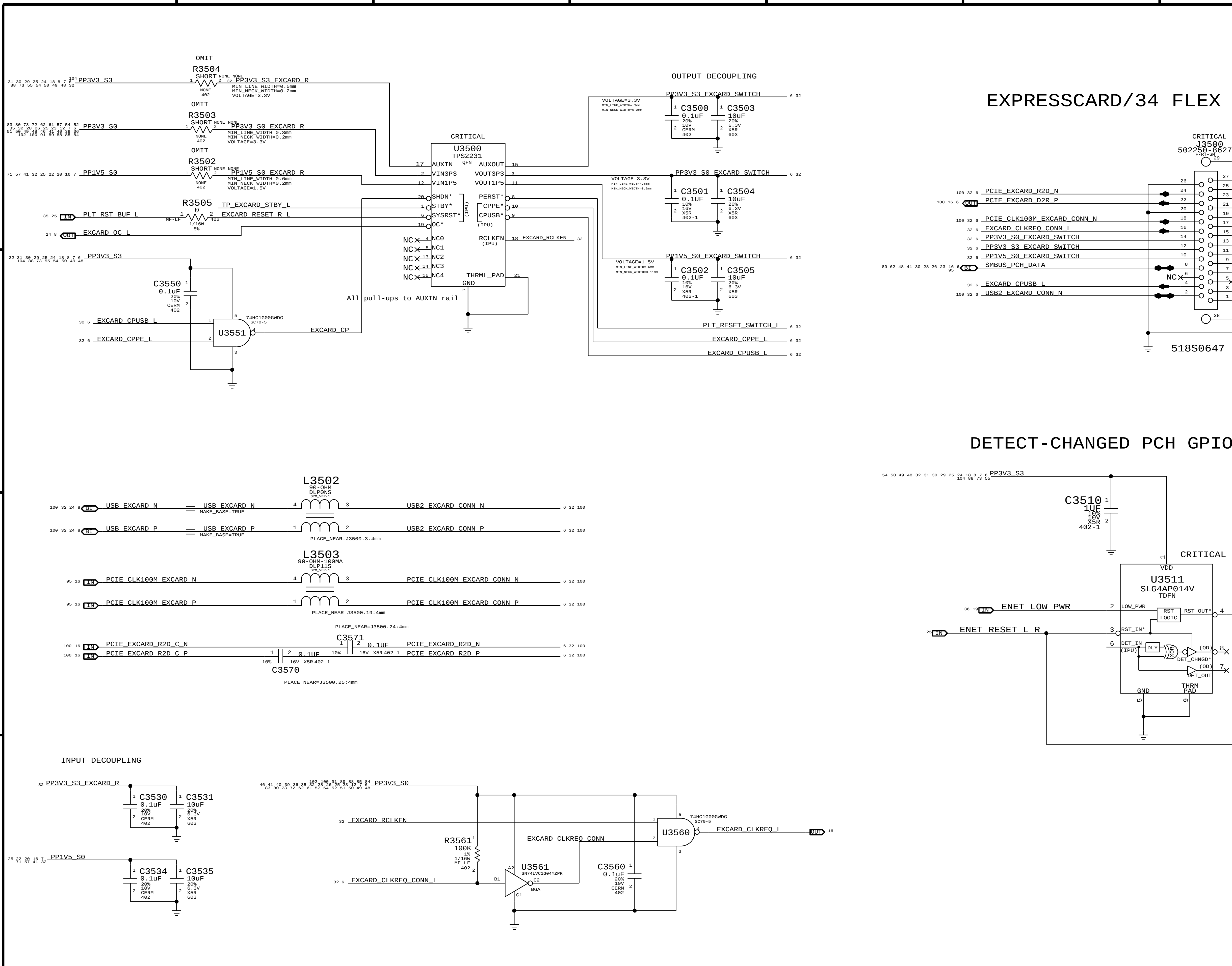
X19/ALS/CAMERA CONNECTOR

Apple Inc.

DRAWING NUMBER SIZE D

REVISION

BRANCH



SYNC_MASTER=K92_ERIC SYNC_DATE=07/27/2010

PAGE TITLE

ExpressCard Connector

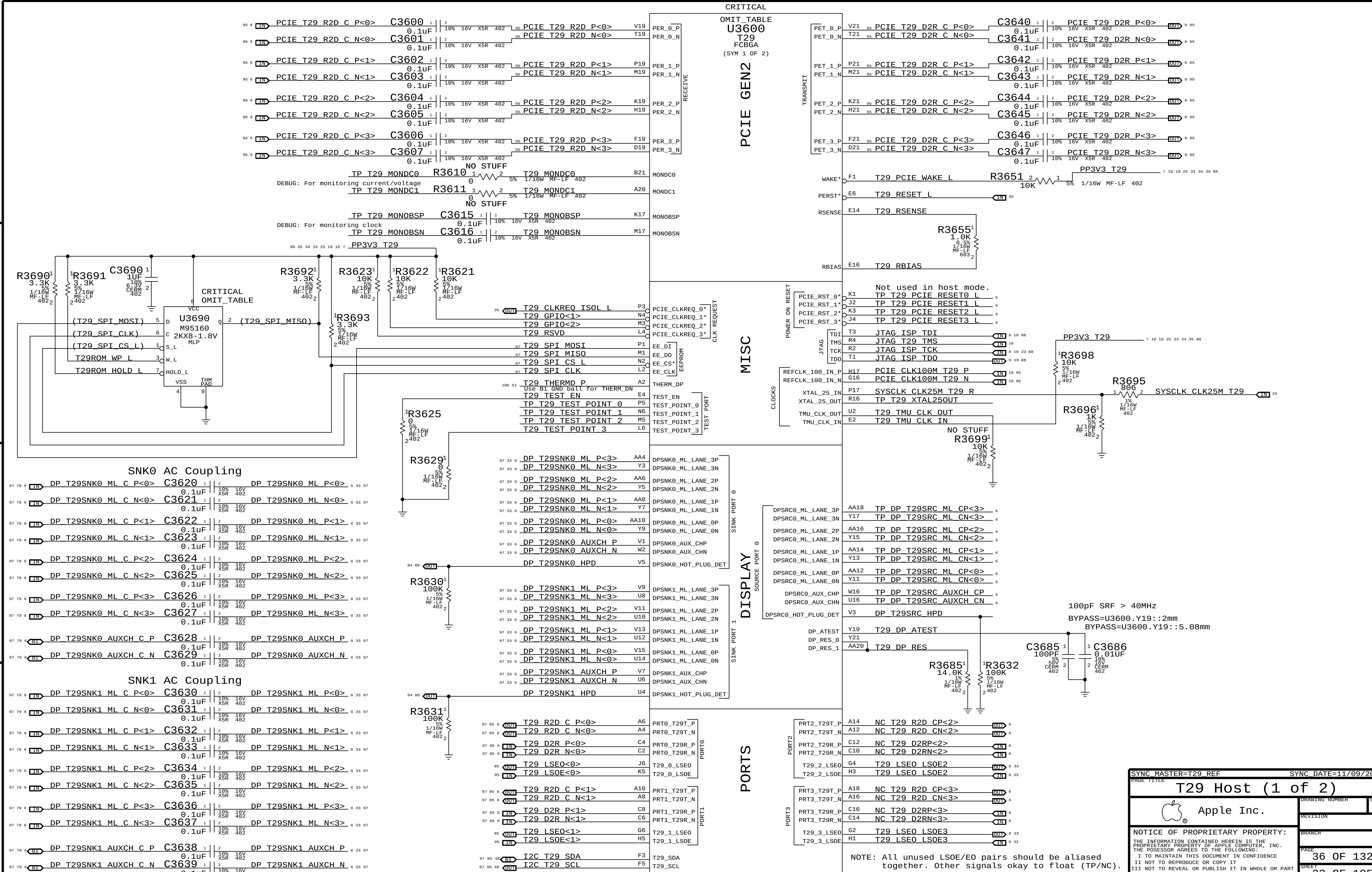
Apple Inc.

DRAWING NUMBER

SIZE D

REVISION

BRANCH



SYNC_MASTER=T29_REF SYNC_DATE=11/09/2010

PAGE TITLE

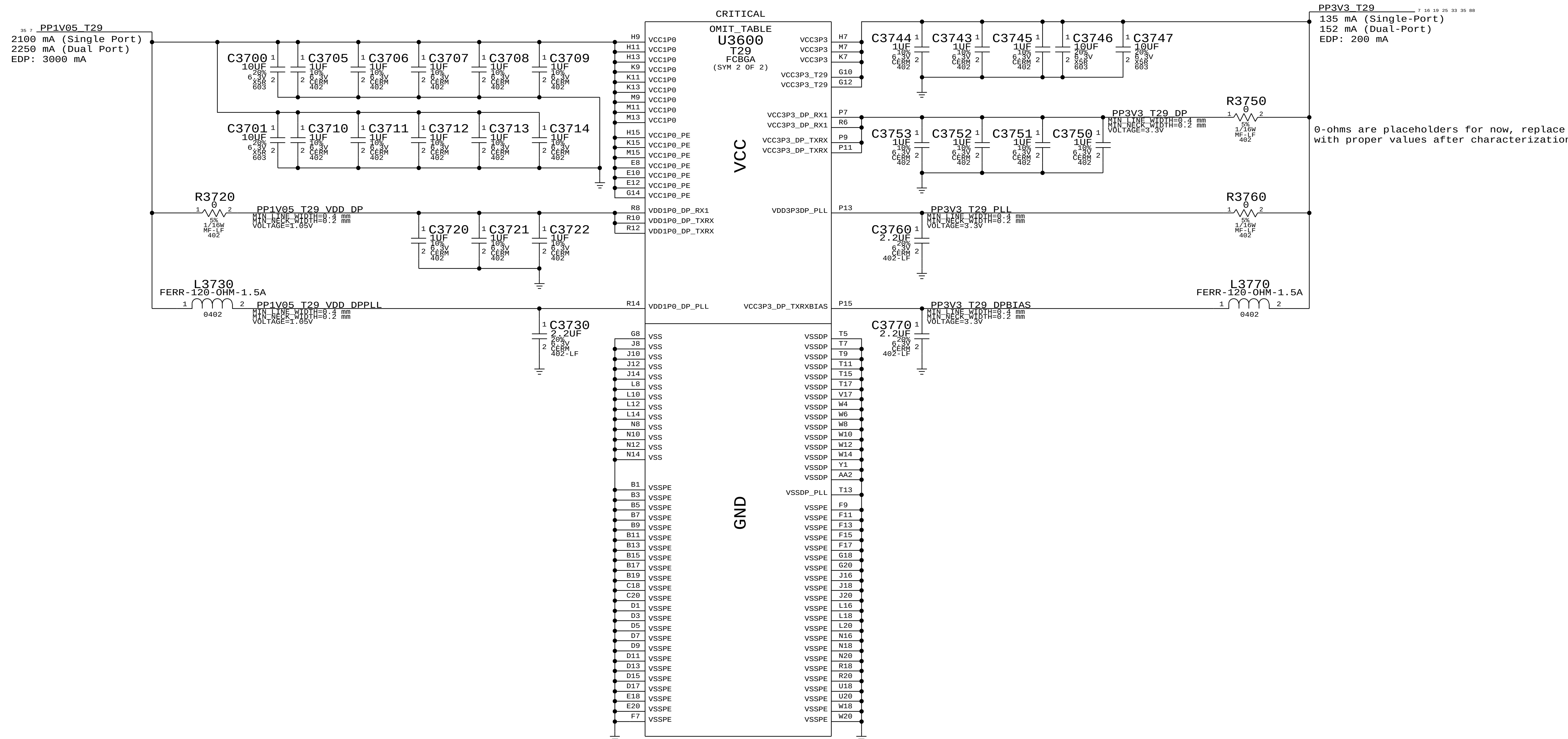
T29 Host (1 of 2)

Apple Inc.

DRAWING NUMBER SIZE D

REVISION

BRANCH



Current numbers from Vendor slide (<REDACTED> power measure 1.ppt), emailed 6/21/2010, TDP @ 90C.

SYNC_MASTER=T29_REF SYNC_DATE=11/09/2010

PAGE TITLE

T29 Host (2 of 2)

Apple Inc.

DRAWING NUMBER | SIZE D | REVISION | BRANCH

NOTICE OF PROPRIETARY PROPERTY:

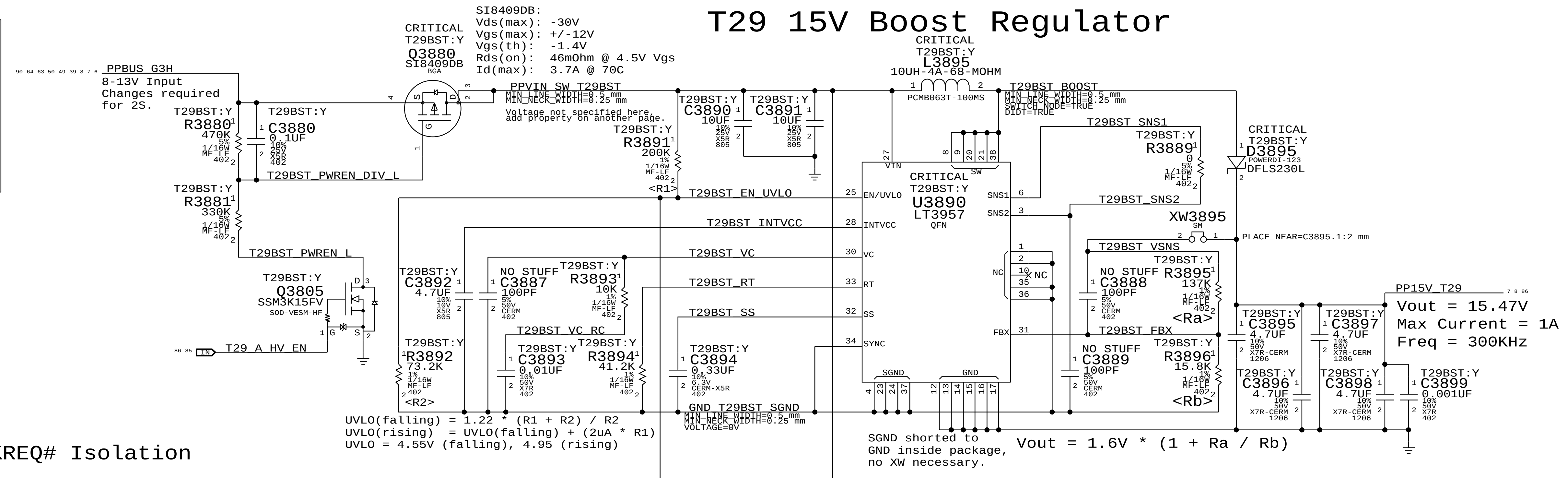
Page Notes

Power aliases required by this page:
- =PPVIN_SW_T29BST (8-13V Boost Input)
- =PP18V_T29_REG (18V Boost Output)
- =PP3V3_T29_P3V3T29FET (3.3V FET Input)
- =PP3V3_T29_FET (3.3V FET Output)
- =PP3V3_S0_T29PWRCTL
- =PP1V05_T29_P1V05T29FET (1.05V FET Input)
- =PP1V05_T29_FET (1.05V FET Output)

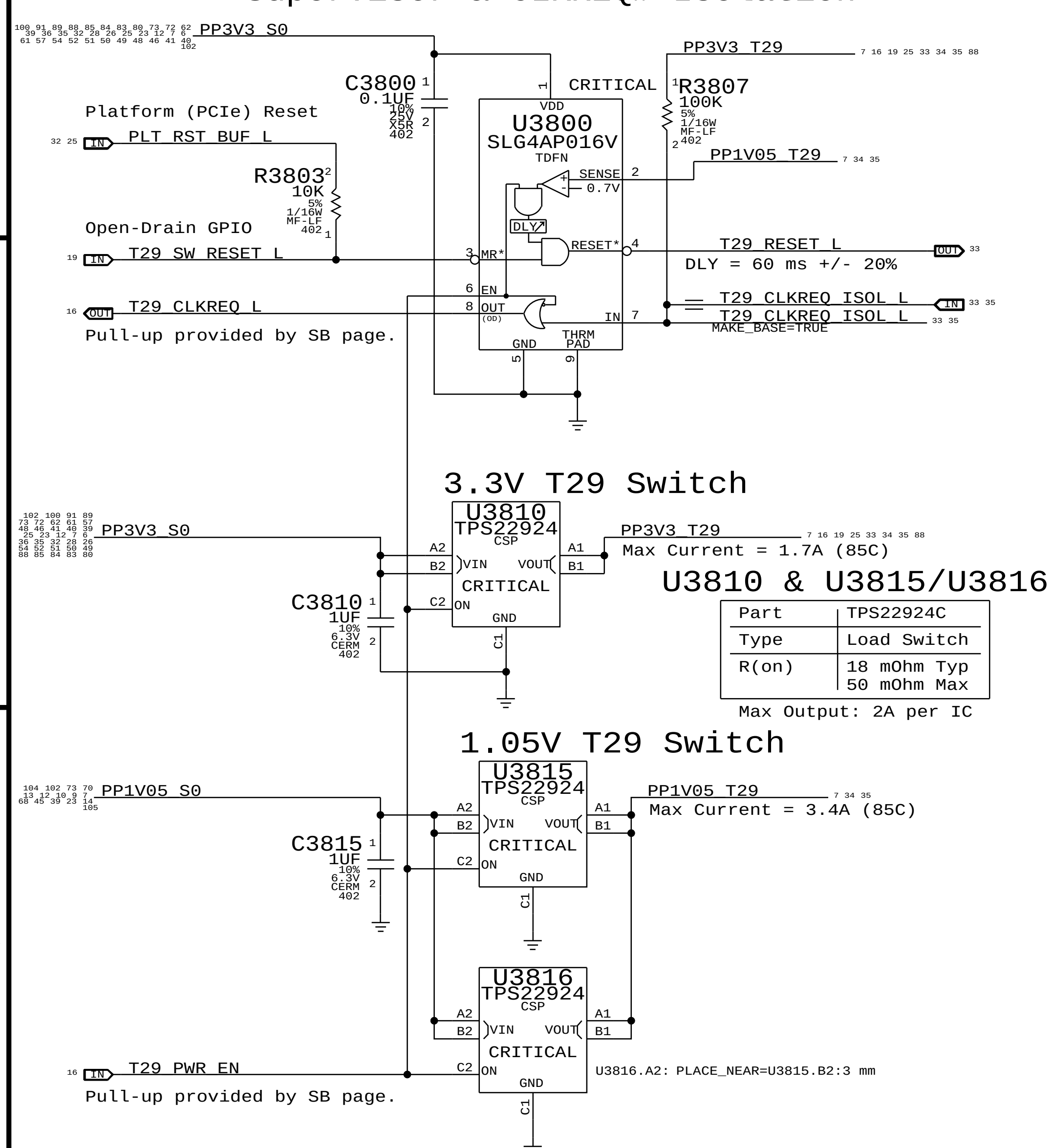
Signal aliases required by this page:
- =T29_CLKREQ_L
- =T29_RESET_L

BOM options provided by this page:
T29BST:Y - Stuffs 18V boost circuitry.

T29 15V Boost Regulator



Supervisor & CLKREQ# Isolation



U3810 & U3815/U3816

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

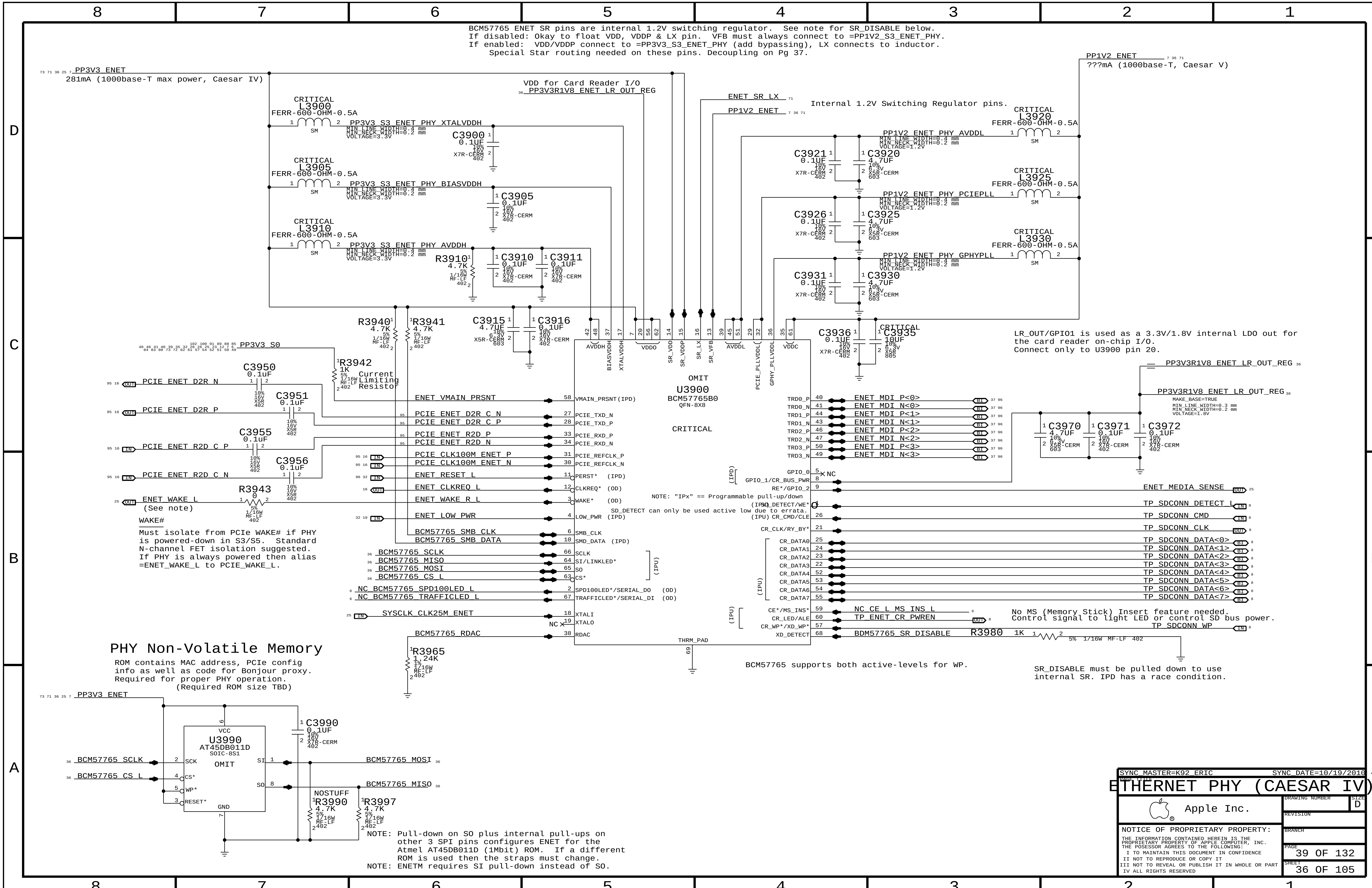
Max Output: 2A per IC

SYNC_MASTER=T29_REF SYNC_DATE=11/09/2010

PAGE TITLE: T29 Power Support

Apple Inc.

DRAWING NUMBER SIZE D

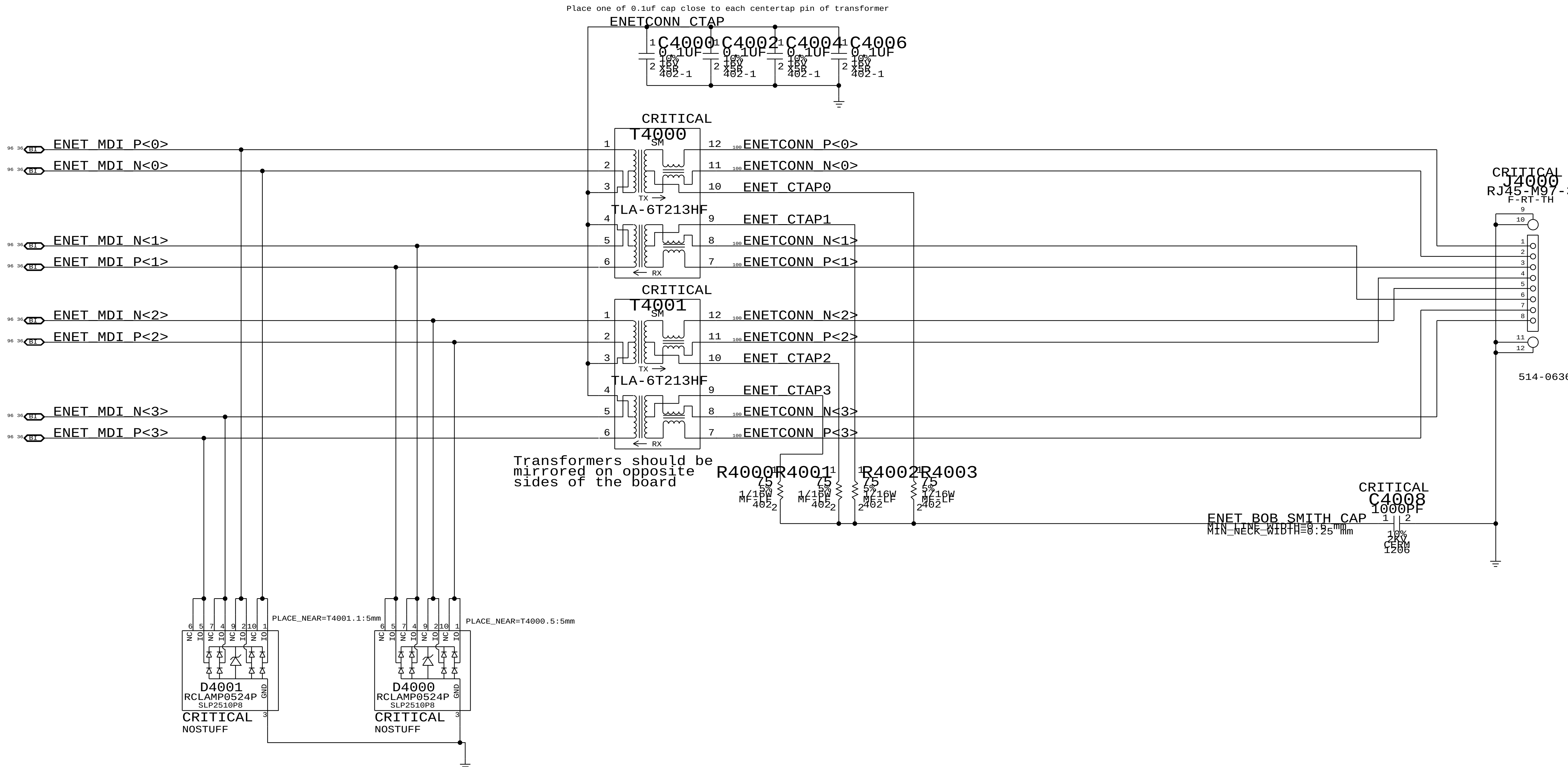

BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.
PP3V3_ENET
281mA (1000base-T max power, Caesar IV)
PP1V2_ENET
???mA (1000base-T, Caesar V)
VDD for Card Reader I/O
PP3V3R1V8_ENET_LR_OUT_REG
ENET_SR_LX
PP1V2_ENET
Internal 1.2V Switching Regulator pins.
PP3V3_S3_ENET_PHY_XTALVDDH
PP3V3_S3_ENET_PHY_BIASVDDH
PP3V3_S3_ENET_PHY_AVDDH
PP1V2_ENET_PHY_AVDDL
PP1V2_ENET_PHY_PCIEPLL
PP1V2_ENET_PHY_GPHYPLL
OMIT
U3900
BCM57765B0
QFN-8X8
CRITICAL
LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for
the card reader on-chip I/O.
Connect only to U3900 pin 20.
NOTE: "IPx" == Programmable pull-up/down
SD_DETECT can only be used active low due to errata.
PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_P
PCIE_ENET_R2D_C_N
ENET_WAKE_L
(See note)
WAKE#
Must isolate from PCIe WAKE# if PHY
is powered-down in S3/S5. Standard
N-channel FET isolation suggested.
If PHY is always powered then alias
=ENET_WAKE_L to PCIE_WAKE_L.
Current
Limiting
Resistor
ENET_MDI_P<0>
ENET_MDI_N<0>
ENET_MDI_P<1>
ENET_MDI_N<1>
ENET_MDI_P<2>
ENET_MDI_N<2>
ENET_MDI_P<3>
ENET_MDI_N<3>
ENET_MEDIA_SENSE
TP_SDCONN_DETECT_L
TP_SDCONN_CMD
TP_SDCONN_CLK
TP_SDCONN_DATA<0>
TP_SDCONN_DATA<1>
TP_SDCONN_DATA<2>
TP_SDCONN_DATA<3>
TP_SDCONN_DATA<4>
TP_SDCONN_DATA<5>
TP_SDCONN_DATA<6>
TP_SDCONN_DATA<7>
NC_CE_L_MS_INS_L
TP_ENET_CR_PWREN
TP_SDCONN_WP
No MS (Memory Stick) Insert feature needed.
Control signal to light LED or control SD bus power.
BDM57765_SR_DISABLE
BCM57765 supports both active-levels for WP.
SR_DISABLE must be pulled down to use
internal SR. IPD has a race condition.
ENET_VMAIN_PRSNT
PCIE_ENET_D2R_C_N
PCIE_ENET_D2R_C_P
PCIE_ENET_R2D_P
PCIE_ENET_R2D_N
PCIE_CLK100M_ENET_P
PCIE_CLK100M_ENET_N
ENET_RESET_L
ENET_CLKREQ_L
ENET_WAKE_R_L
ENET_LOW_PWR
BCM57765_SMB_CLK
BCM57765_SMB_DATA
BCM57765_SCLK
BCM57765_MISO
BCM57765_MOSI
BCM57765_CS_L
NC_BCM57765_SPD100LED_L
NC_BCM57765_TRAFFICLED_L
SYSCLK_CLK25M_ENET
BCM57765_RDAC
PHY Non-Volatile Memory
ROM contains MAC address, PCIe config
info as well as code for Bonjour proxy.
Required for proper PHY operation.
(Required ROM size TBD)
U3990
AT45DB011D
SOIC-8S1
OMIT
NOTE: Pull-down on SO plus internal pull-ups on
other 3 SPI pins configures ENET for the
Atmel AT45DB011D (1Mbit) ROM. If a different
ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.
SYNC_MASTER=K92_ERIC
SYNC_DATE=10/19/2010
ETHERNET PHY (CAESAR IV)
Apple Inc.
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE
PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED
PAGE 39 OF 132
SHEET 36 OF 105

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

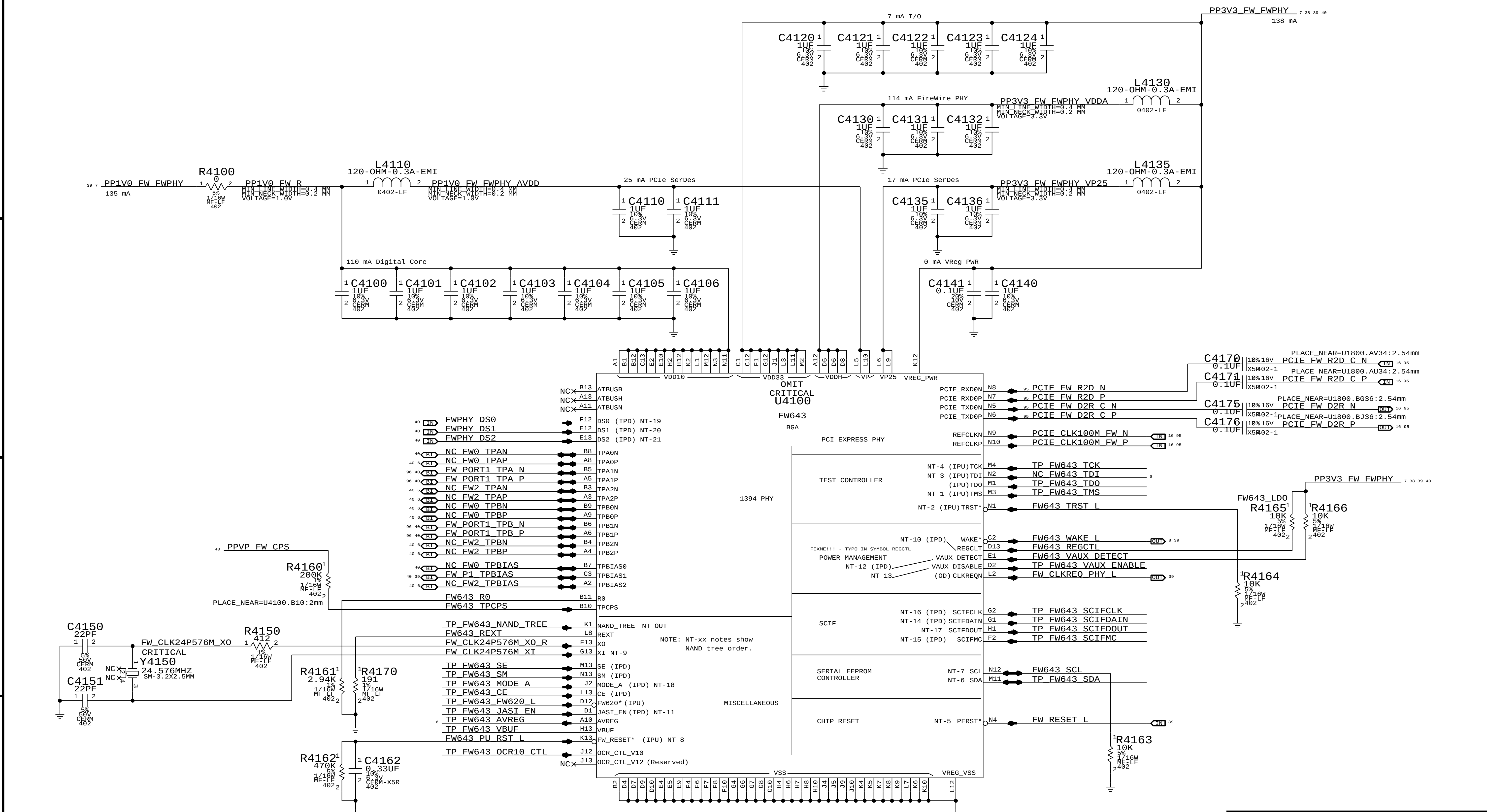


SYNC_MASTER=K92_ERIC SYNC_DATE=08/24/2010

PAGE TITLE
Ethernet Connector

Apple Inc.

DRAWING NUMBER | SIZE D | REVISION | BRANCH



SYNC_MASTER=K91_MLB SYNC_DATE=10/20/2010

PAGE TITLE

FireWire LLC/PHY (FW643)

Apple Inc.

DRAWING NUMBER

SIZE D

REVISION

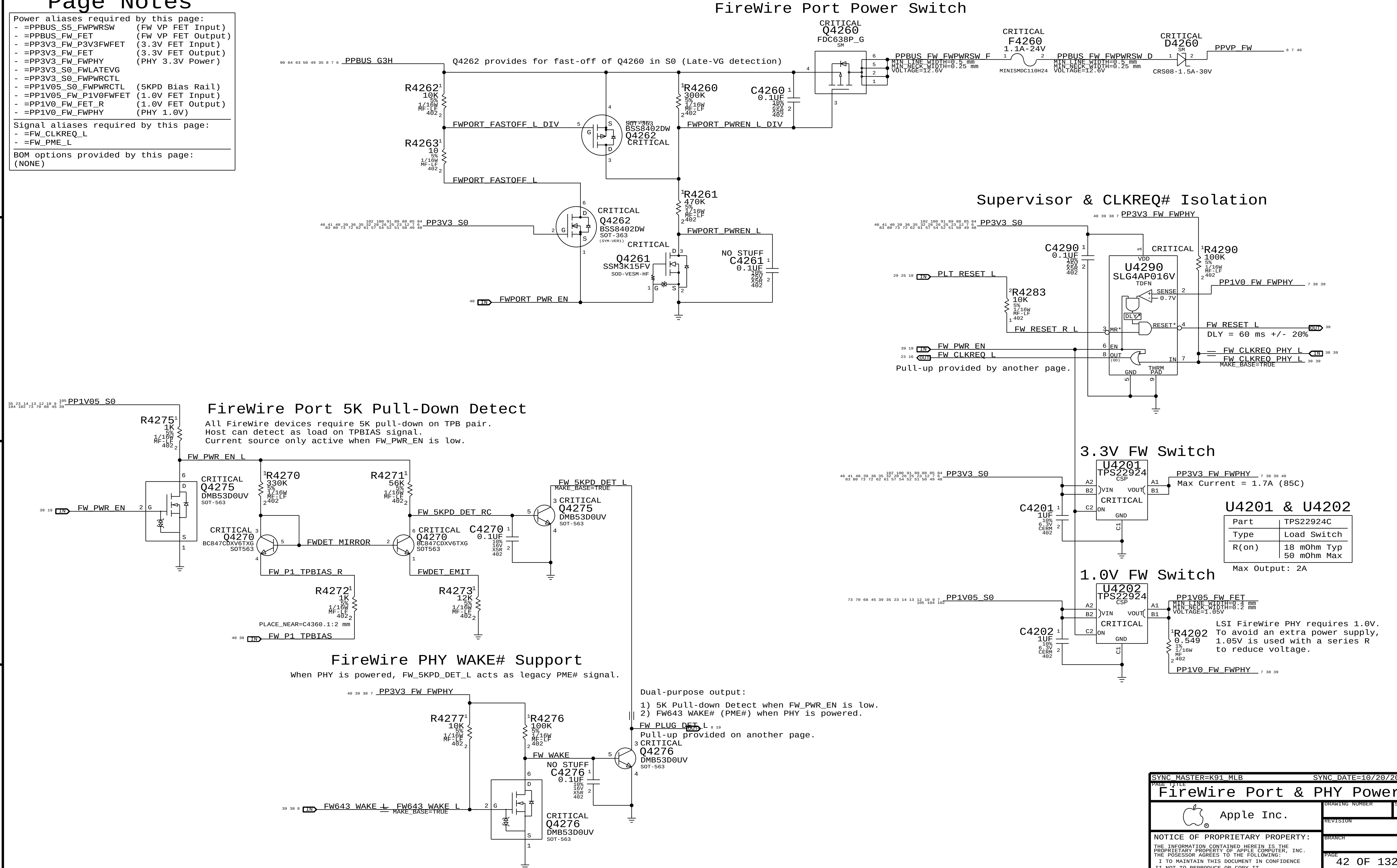
BRANCH

Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (FW VP FET Input)
- =PPBUS_FW_FET (FW VP FET Output)
- =PP3V3_FW_P3V3FWFET (3.3V FET Input)
- =PP3V3_FW_FET (3.3V FET Output)
- =PP3V3_FW_FWPHY (PHY 3.3V Power)
- =PP3V3_S0_FWLATEVG
- =PP3V3_S0_FWPWRCTL
- =PP1V05_S0_FWPWRCTL (5KPD Bias Rail)
- =PP1V05_FW_P1V0FWFET (1.0V FET Input)
- =PP1V0_FW_FET_R (1.0V FET Output)
- =PP1V0_FW_FWPHY (PHY 1.0V)

Signal aliases required by this page:
- =FW_CLKREQ_L
- =FW_PME_L

BOM options provided by this page:
(NONE)



U4201 & U4202

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A

SYNC_MASTER=K91_MLB SYNC_DATE=10/20/2010

PAGE TITLE
FireWire Port & PHY Power

Apple Inc.

DRAWING NUMBER SIZE D
REVISION
BRANCH

Page Notes

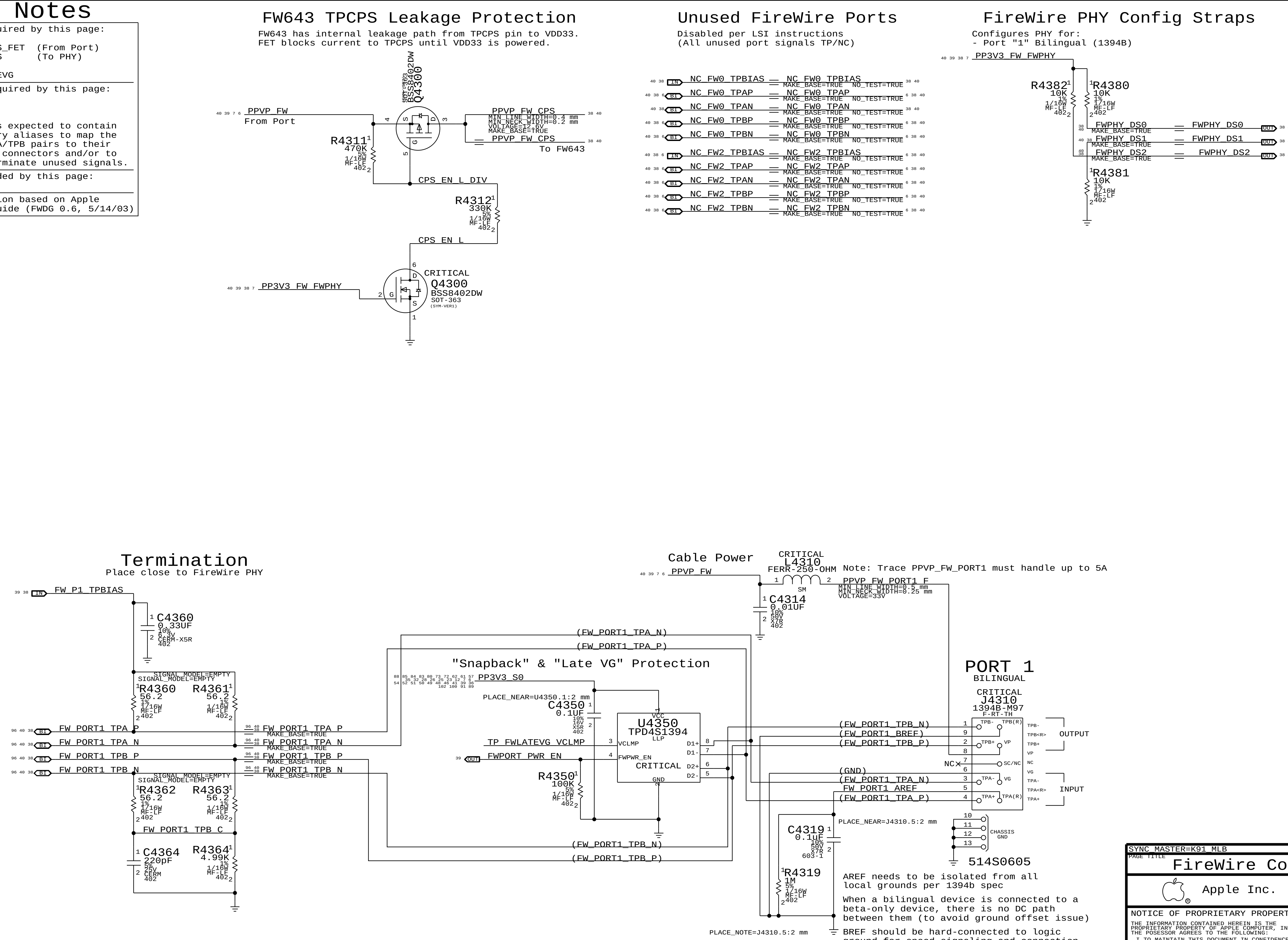
Power aliases required by this page:
- =PPVP_FW_PORT1
- =PPVP_FW_PHY_CPS_FET (From Port)
- =PPVP_FW_PHY_CPS (To PHY)
- =PP3V3_FW_FWPHY
- =PP3V3_S0_FWLATEVG

Signal aliases required by this page:
- =FW_PHY_DS0
- =FW_PHY_DS1
- =FW_PHY_DS2

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)



SYNC_MASTER=K91_MLB SYNC_DATE=07/22/2010

PAGE TITLE: FireWire Connector

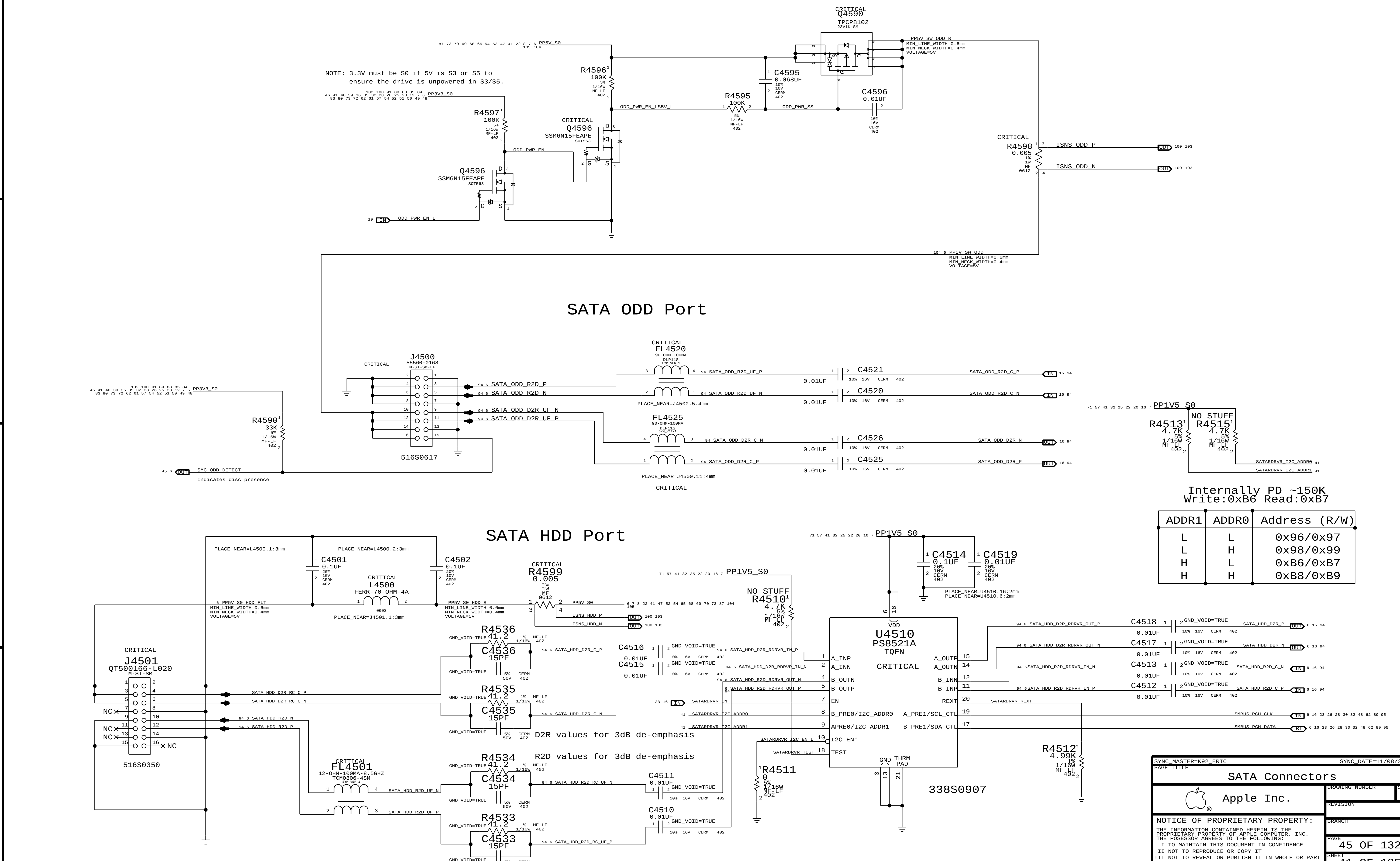
Apple Inc.

DRAWING NUMBER | SIZE D | REVISION | BRANCH

ODD Power Control

SATA ODD Port

SATA HDD Port



Internally PD ~150K
Write:0xB6 Read:0xB7

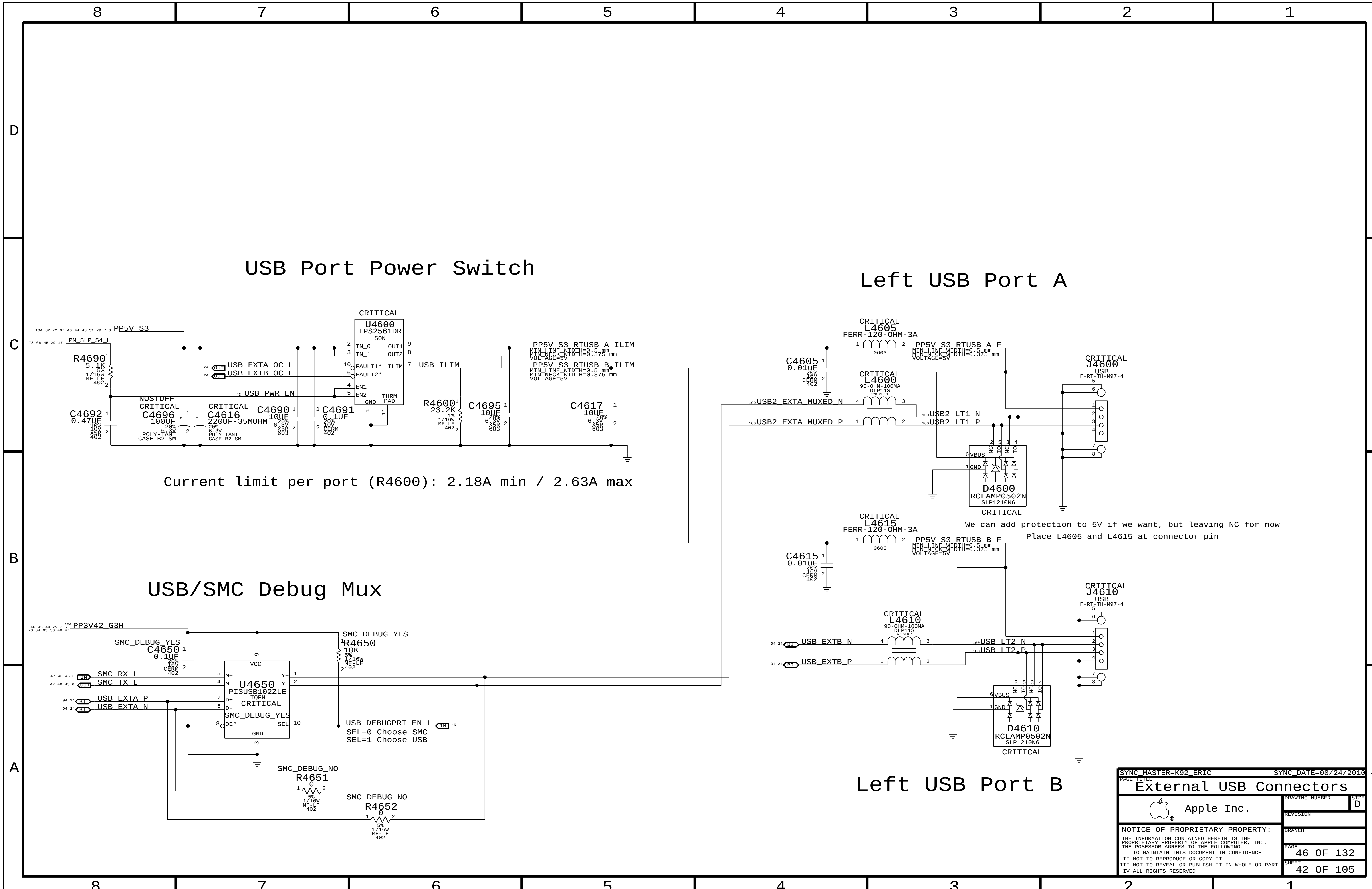
ADDR1	ADDR0	Address (R/W)
L	L	0x96/0x97
L	H	0x98/0x99
H	L	0xB6/0xB7
H	H	0xB8/0xB9

SYNC_MASTER=K92_ERIC SYNC_DATE=11/08/2010

PAGE TITLE: SATA Connectors

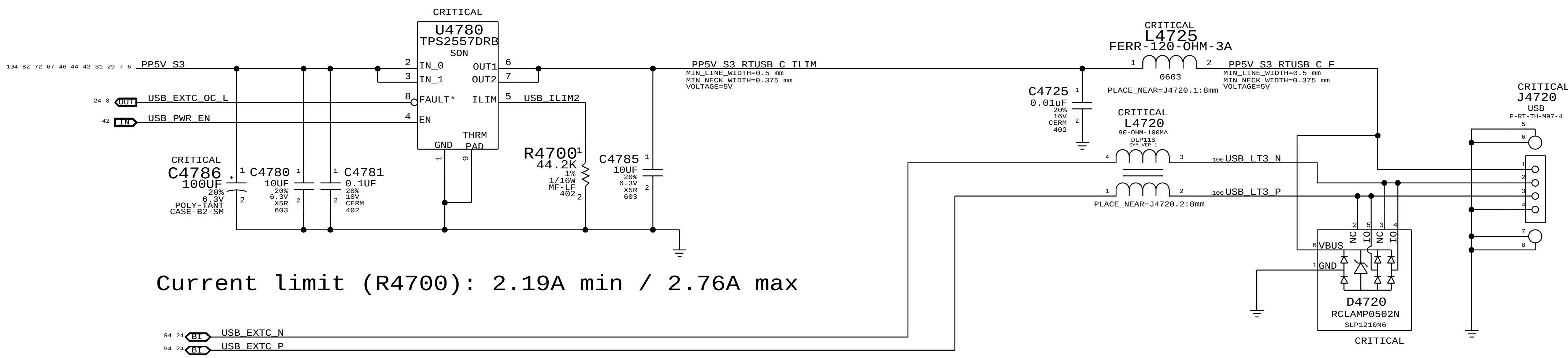
Apple Inc.

DRAWING NUMBER · SIZE D · REVISION · BRANCH


USB Port Power Switch
Left USB Port A
USB/SMC Debug Mux
Left USB Port B
Current limit per port (R4600): 2.18A min / 2.63A max
We can add protection to 5V if we want, but leaving NC for now
Place L4605 and L4615 at connector pin
CRITICAL
U4600
TPS2561DR
SON
PP5V_S3
PM_SLP_S4_L
R4690
5.1K
USB_EXTA_OC_L
USB_EXTB_OC_L
USB_PWR_EN
C4692
0.47UF
NOSTUFF
C4696
100UF
C4616
220UF-35MOHM
C4690
10UF
C4691
0.1UF
USB_ILIM
R4600
23.2K
C4695
10UF
C4617
10UF
PP5V_S3_RTUSB_A_ILIM
PP5V_S3_RTUSB_B_ILIM
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.375 mm
VOLTAGE=5V
L4605
FERR-120-OHM-3A
PP5V_S3_RTUSB_A_F
C4605
0.01UF
L4600
90-OHM-100MA
DLP11S
USB2_EXTA_MUXED_N
USB2_EXTA_MUXED_P
USB2_LT1_N
USB2_LT1_P
J4600
USB
F-RT-TH-M97-4
D4600
RCLAMP0502N
SLP1210N6
L4615
FERR-120-OHM-3A
PP5V_S3_RTUSB_B_F
C4615
0.01UF
J4610
USB
F-RT-TH-M97-4
L4610
90-OHM-100MA
DLP11S
USB_EXTB_N
USB_EXTB_P
USB_LT2_N
USB_LT2_P
D4610
RCLAMP0502N
SLP1210N6
PP3V42_G3H
SMC_DEBUG_YES
C4650
0.1UF
SMC_RX_L
SMC_TX_L
USB_EXTA_P
USB_EXTA_N
U4650
PI3USB102ZLE
TQFN
R4650
10K
USB_DEBUGPRT_EN_L
SEL=0 Choose SMC
SEL=1 Choose USB
SMC_DEBUG_NO
R4651
0
R4652
0
SYNC_MASTER=K92_ERIC
SYNC_DATE=08/24/2010
PAGE TITLE
External USB Connectors
Apple Inc.
DRAWING NUMBER
SIZE
D
REVISION
BRANCH
PAGE
46 OF 132
SHEET
42 OF 105
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

USB Port Power Switch

LEFT USB PORT C



Current limit (R4700): 2.19A min / 2.76A max

SYNC_MASTER=K92_ERIC SYNC_DATE=07/22/2010

PAGE TITLE

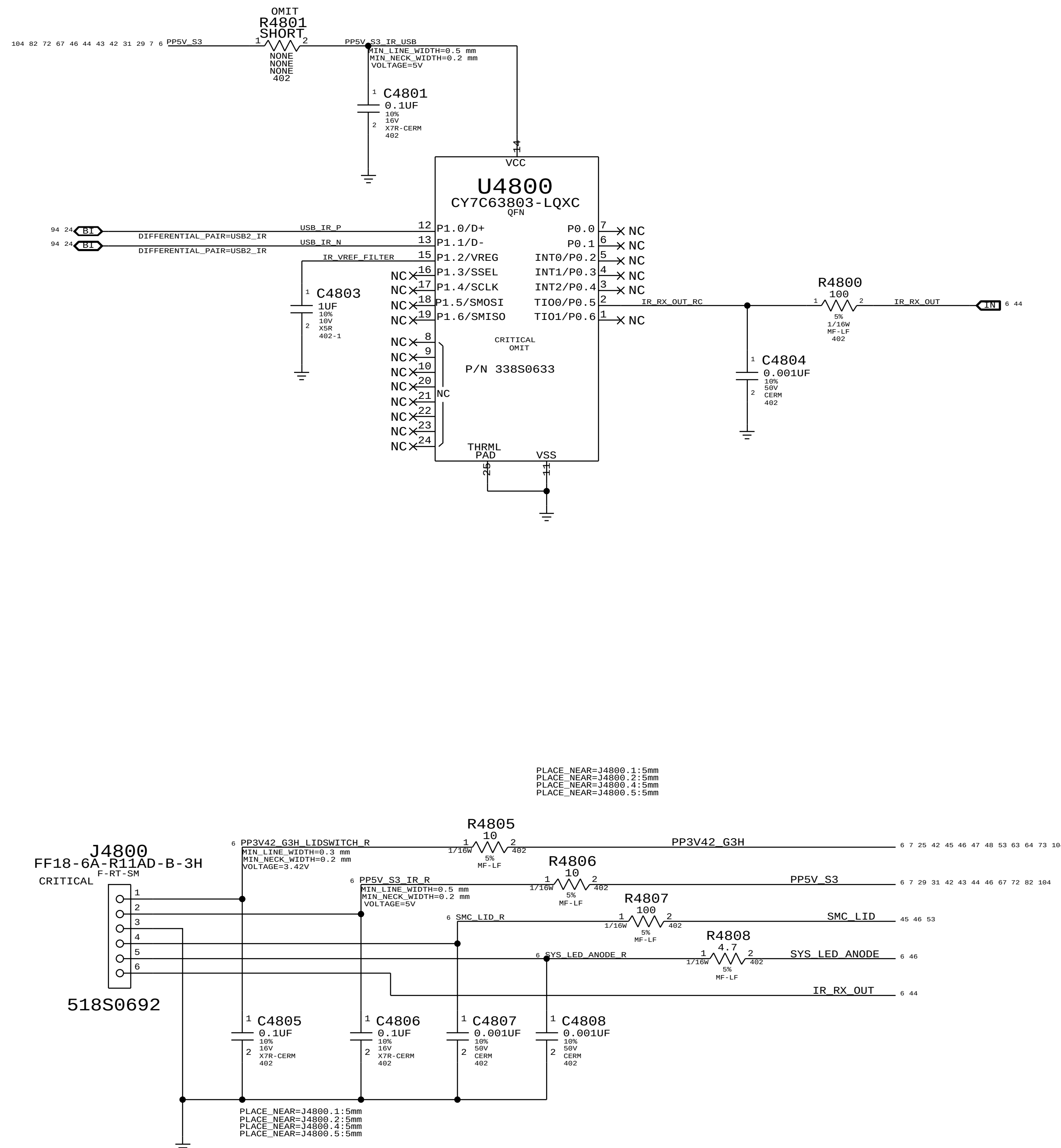
PROJECT SPECIFIC CONNS

Apple Inc.

DRAWING NUMBER SIZE D

REVISION

BRANCH



SYNC_MASTER=K17_MLB SYNC_DATE=04/26/2010

PAGE TITLE

Front Flex Support

Apple Inc.

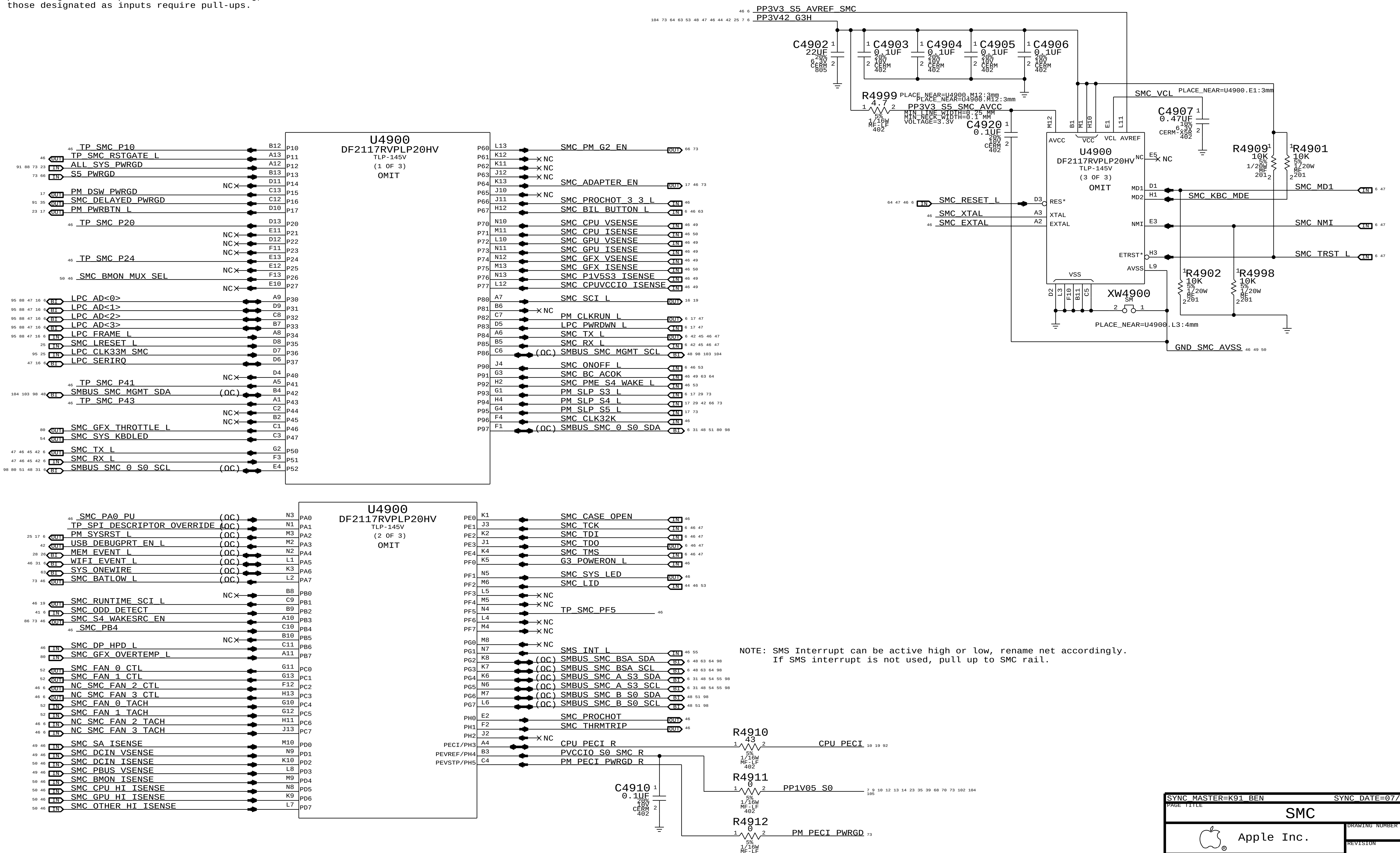
DRAWING NUMBER

SIZE D

REVISION

BRANCH

NOTE: Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.



NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SYNC_MASTER=K91_BEN SYNC_DATE=07/12/2010

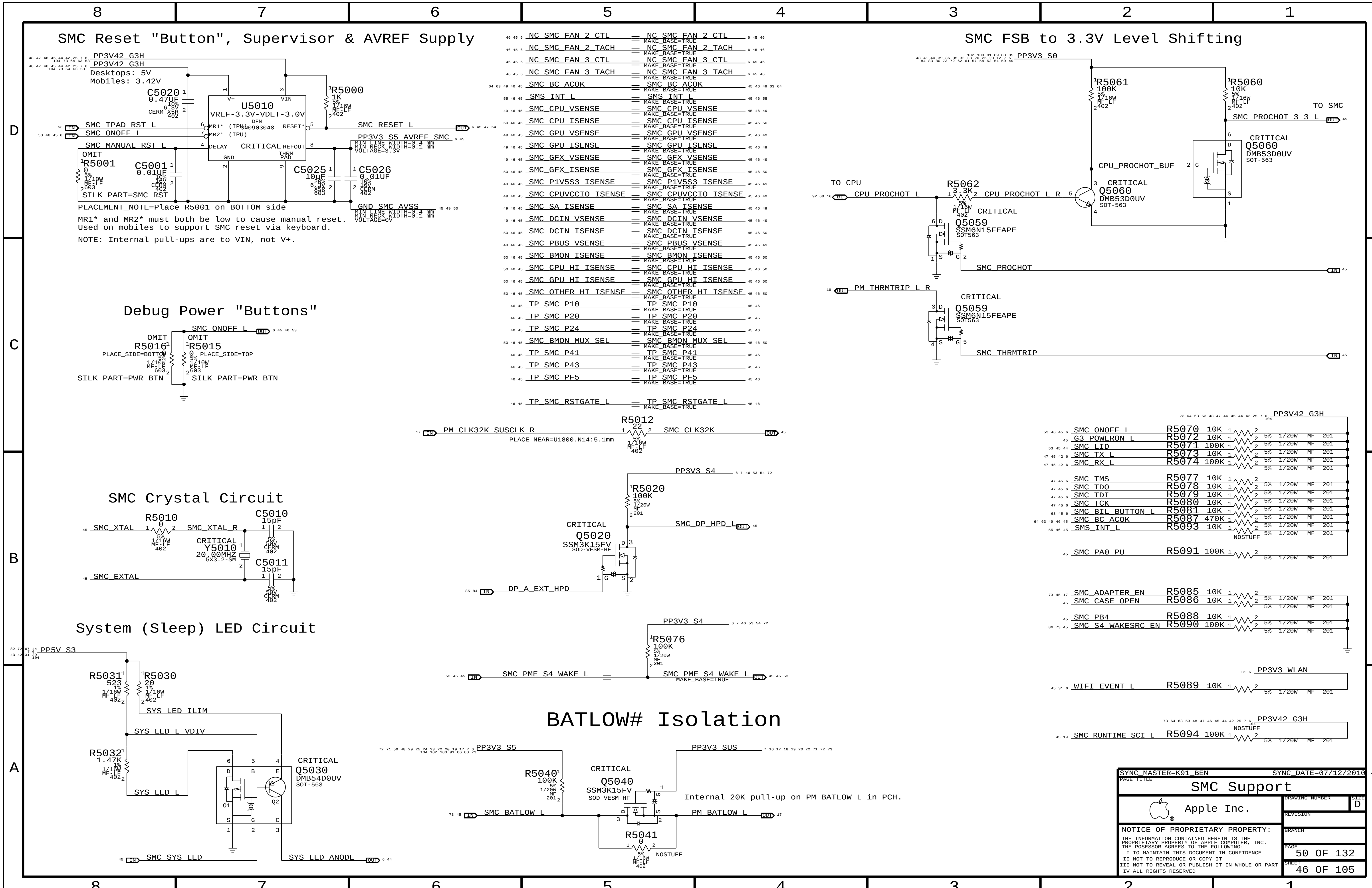
PAGE TITLE

SMC

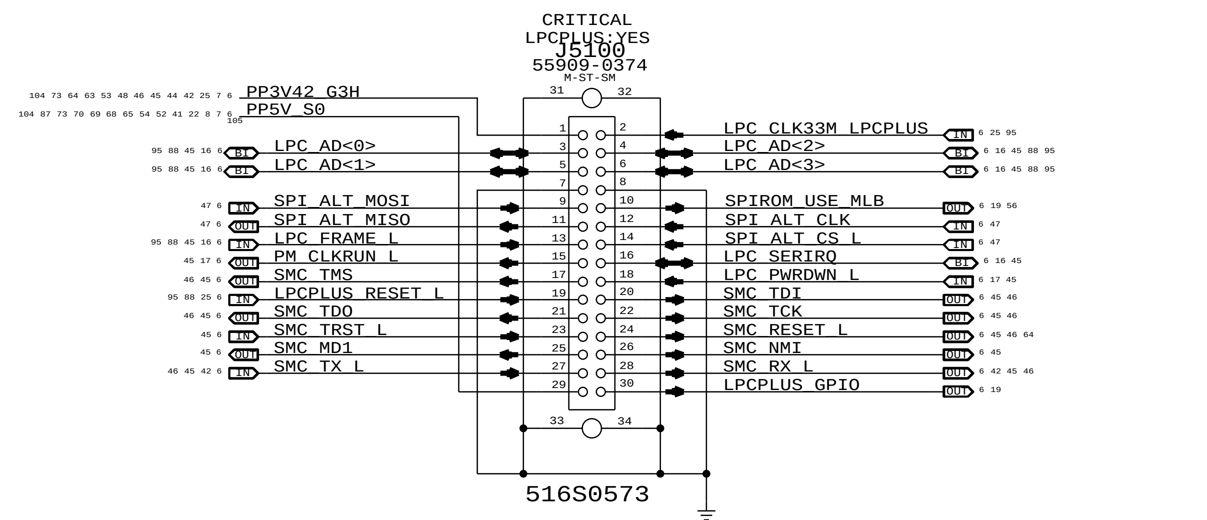
Apple Inc.

DRAWING NUMBER | SIZE D | REVISION | BRANCH

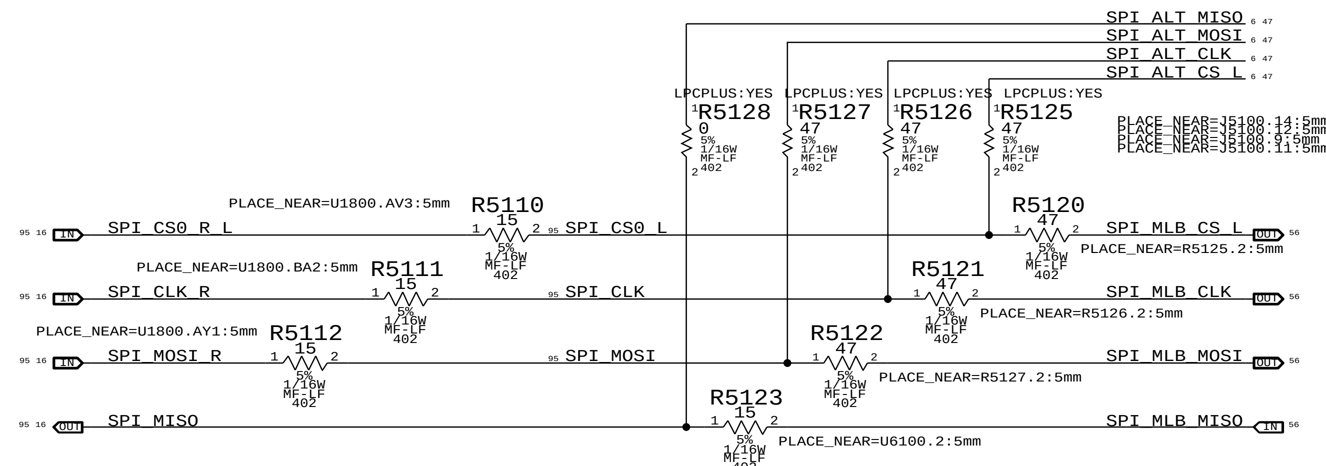
NOTICE OF PROPRIETARY PROPERTY:


SMC Reset "Button", Supervisor & AVREF Supply
PP3V42_G3H
Desktops: 5V
Mobiles: 3.42V
C5020 0.47UF
U5010 VREF-3.3V-VDET-3.0V
SMC_TPAD_RST_L
SMC_ONOFF_L
SMC_MANUAL_RST_L
SMC_RESET_L
R5000 1K
R5001 0
C5001 0.01UF
C5025 10uF
C5026 0.01UF
PP3V3_S5_AVREF_SMC
GND_SMC_AVSS
SILK_PART=SMC_RST
PLACEMENT_NOTE=Place R5001 on BOTTOM side
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.
NOTE: Internal pull-ups are to VIN, not V+.
Debug Power "Buttons"
SMC_ONOFF_L
R5016 0
R5015 0
SILK_PART=PWR_BTN
SMC Crystal Circuit
SMC_XTAL
SMC_EXTAL
R5010 0
Y5010 20.00MHZ
C5010 15pF
C5011 15pF
System (Sleep) LED Circuit
PP5V_S3
R5031 523
R5030 20
R5032 1.47K
Q5030 DMB54D0UV
SYS_LED_ILIM
SYS_LED_L_VDIV
SYS_LED_L
SMC_SYS_LED
SYS_LED_ANODE
NC_SMC_FAN_2_CTL
NC_SMC_FAN_2_TACH
NC_SMC_FAN_3_CTL
NC_SMC_FAN_3_TACH
SMC_BC_ACOK
SMS_INT_L
SMC_CPU_VSENSE
SMC_CPU_ISENSE
SMC_GPU_VSENSE
SMC_GPU_ISENSE
SMC_GFX_VSENSE
SMC_GFX_ISENSE
SMC_P1V5S3_ISENSE
SMC_CPUVCCIO_ISENSE
SMC_SA_ISENSE
SMC_DCIN_VSENSE
SMC_DCIN_ISENSE
SMC_PBUS_VSENSE
SMC_BMON_ISENSE
SMC_CPU_HI_ISENSE
SMC_GPU_HI_ISENSE
SMC_OTHER_HI_ISENSE
TP_SMC_P10
TP_SMC_P20
TP_SMC_P24
SMC_BMON_MUX_SEL
TP_SMC_P41
TP_SMC_P43
TP_SMC_PF5
TP_SMC_RSTGATE_L
MAKE_BASE=TRUE
PM_CLK32K_SUSCLK_R
R5012 22
SMC_CLK32K
PLACE_NEAR=U1800.N14:5.1mm
PP3V3_S4
R5020 100K
SMC_DP_HPD_L
Q5020 SSM3K15FV
DP_A_EXT_HPD
R5076 100K
SMC_PME_S4_WAKE_L
BATLOW# Isolation
PP3V3_S5
PP3V3_SUS
R5040 100K
Q5040 SSM3K15FV
SMC_BATLOW_L
PM_BATLOW_L
R5041 0
NOSTUFF
Internal 20K pull-up on PM_BATLOW_L in PCH.
SMC FSB to 3.3V Level Shifting
PP3V3_S0
R5061 100K
R5060 10K
TO SMC
SMC_PROCHOT_3_3_L
Q5060 DMB53D0UV
CPU_PROCHOT_BUF
TO CPU
CPU_PROCHOT_L
R5062 3.3K
CPU_PROCHOT_L_R
Q5059 SSM6N15FEAPE
SMC_PROCHOT
PM_THRMTRIP_L_R
SMC_THRMTRIP
PP3V42_G3H
SMC_ONOFF_L R5070 10K
G3_POWERON_L R5072 10K
SMC_LID R5071 100K
SMC_TX_L R5073 10K
SMC_RX_L R5074 100K
SMC_TMS R5077 10K
SMC_TDO R5078 10K
SMC_TDI R5079 10K
SMC_TCK R5080 10K
SMC_BIL_BUTTON_L R5081 10K
SMC_BC_ACOK R5087 470K
SMS_INT_L R5093 10K
SMC_PA0_PU R5091 100K
SMC_ADAPTER_EN R5085 10K
SMC_CASE_OPEN R5086 10K
SMC_PB4 R5088 10K
SMC_S4_WAKESRC_EN R5090 100K
PP3V3_WLAN
WIFI_EVENT_L R5089 10K
SMC_RUNTIME_SCI_L R5094 100K
SYNC_MASTER=K91_BEN
SYNC_DATE=07/12/2010
SMC Support
Apple Inc.
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED
D
50 OF 132
46 OF 105

LPC+SPI Connector



SPI Bus Series Termination



SYNC_MASTER=K91_YUN SYNC_DATE=09/23/2010

PAGE TITLE

LPC+SPI Debug Connector

Apple Inc.

DRAWING NUMBER

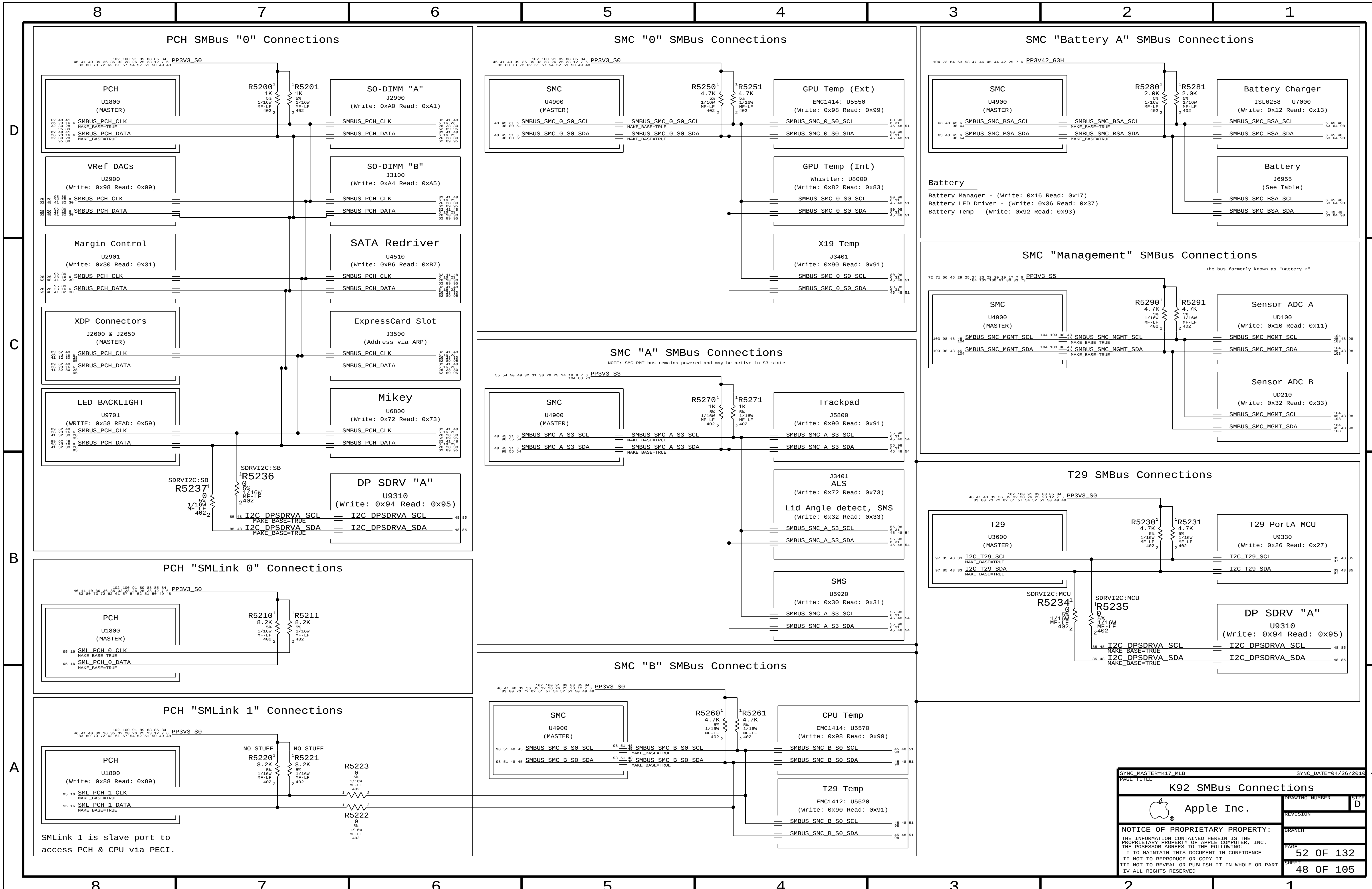
SIZE D

REVISION

BRANCH

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART



SYNC_MASTER=K17_MLB SYNC_DATE=04/26/2010

PAGE TITLE

K92 SMBus Connections

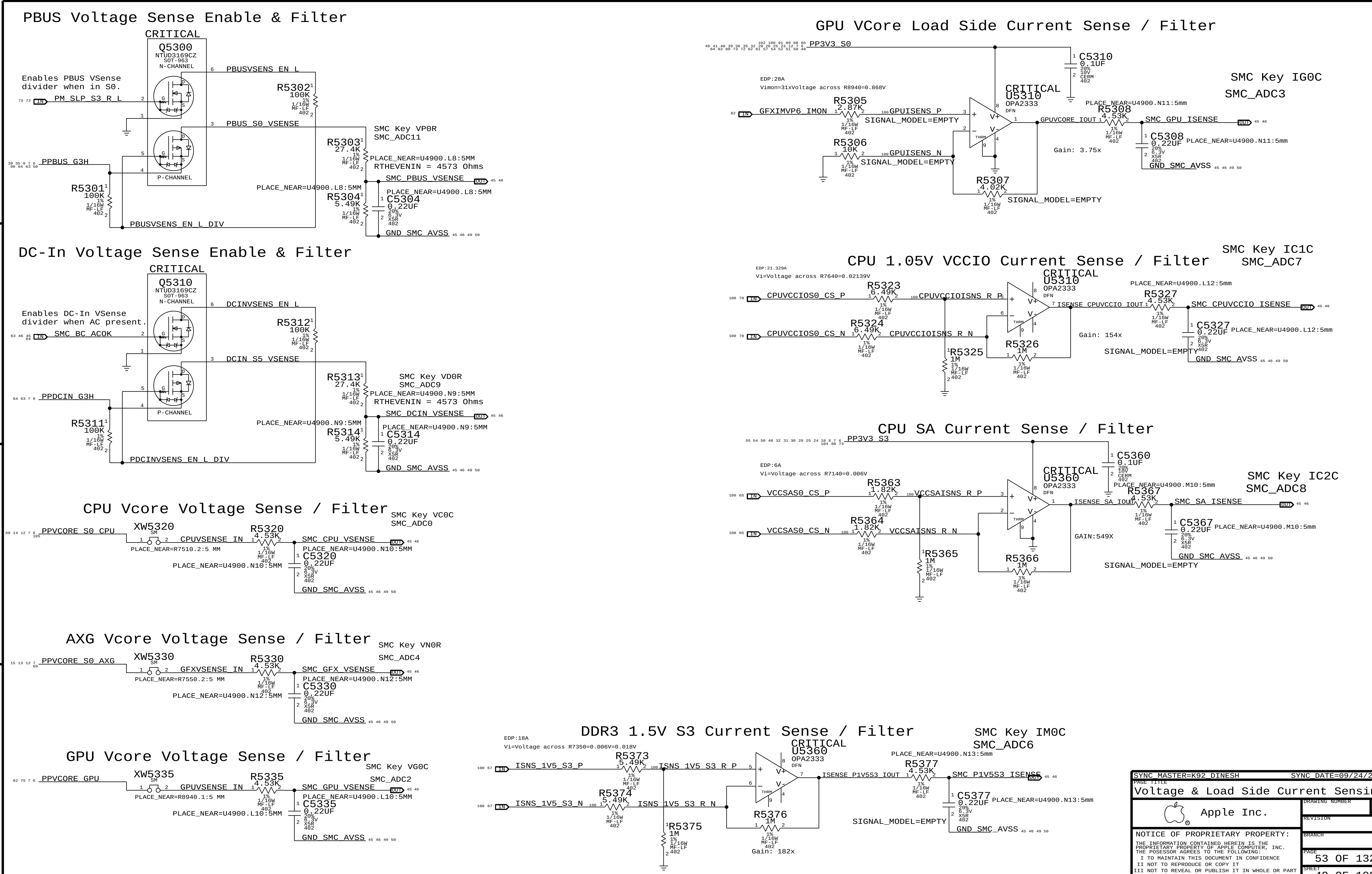
Apple Inc.

DRAWING NUMBER

SIZE D

REVISION

BRANCH



SYNC_MASTER=K92_DINESH
SYNC_DATE=09/24/2010

PAGE TITLE

Voltage & Load Side Current Sensing

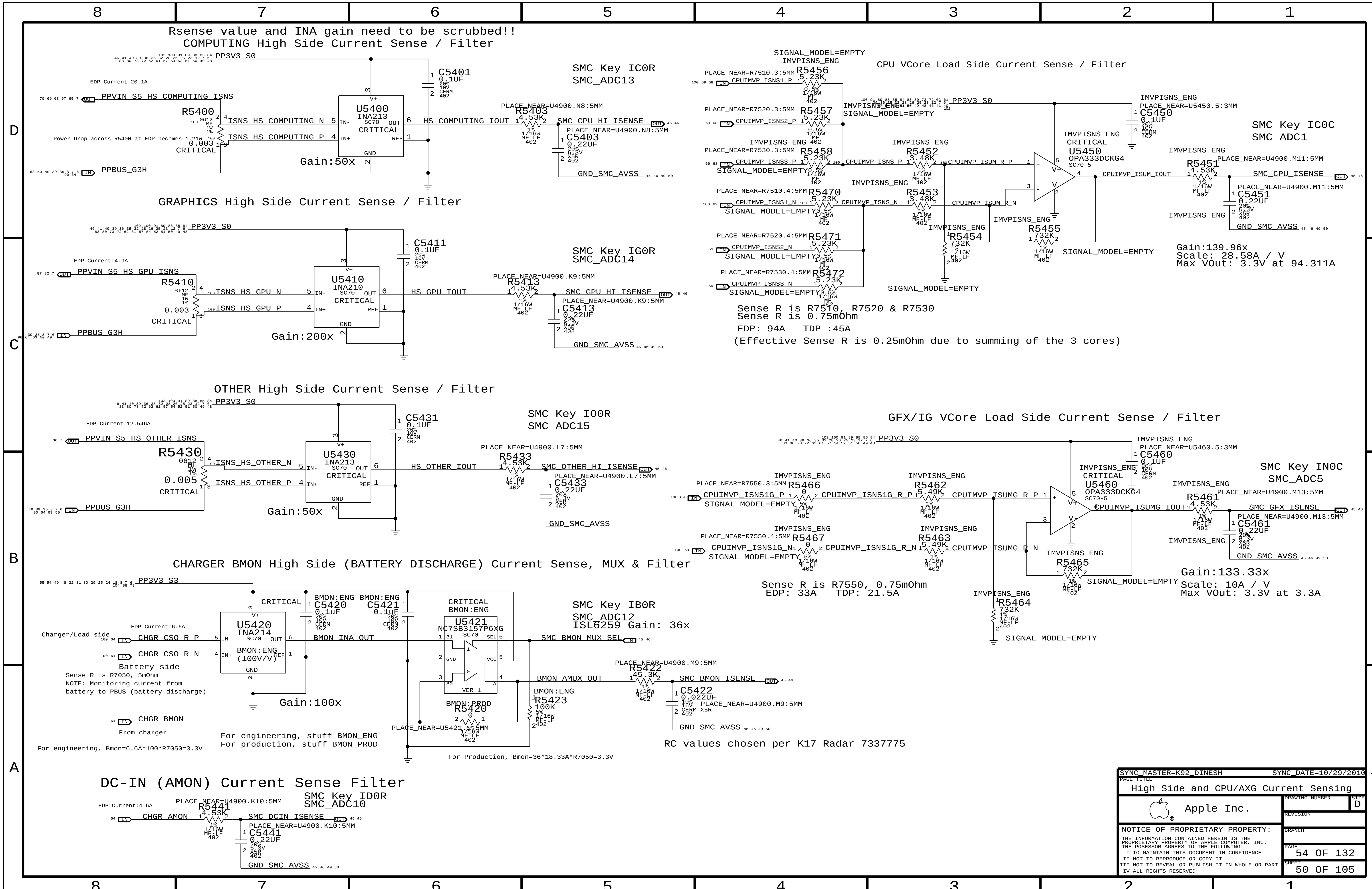
Apple Inc.

DRAWING NUMBER

SIZE D

REVISION

BRANCH



SYNC_MASTER=K92_DINESH SYNC_DATE=10/29/2010

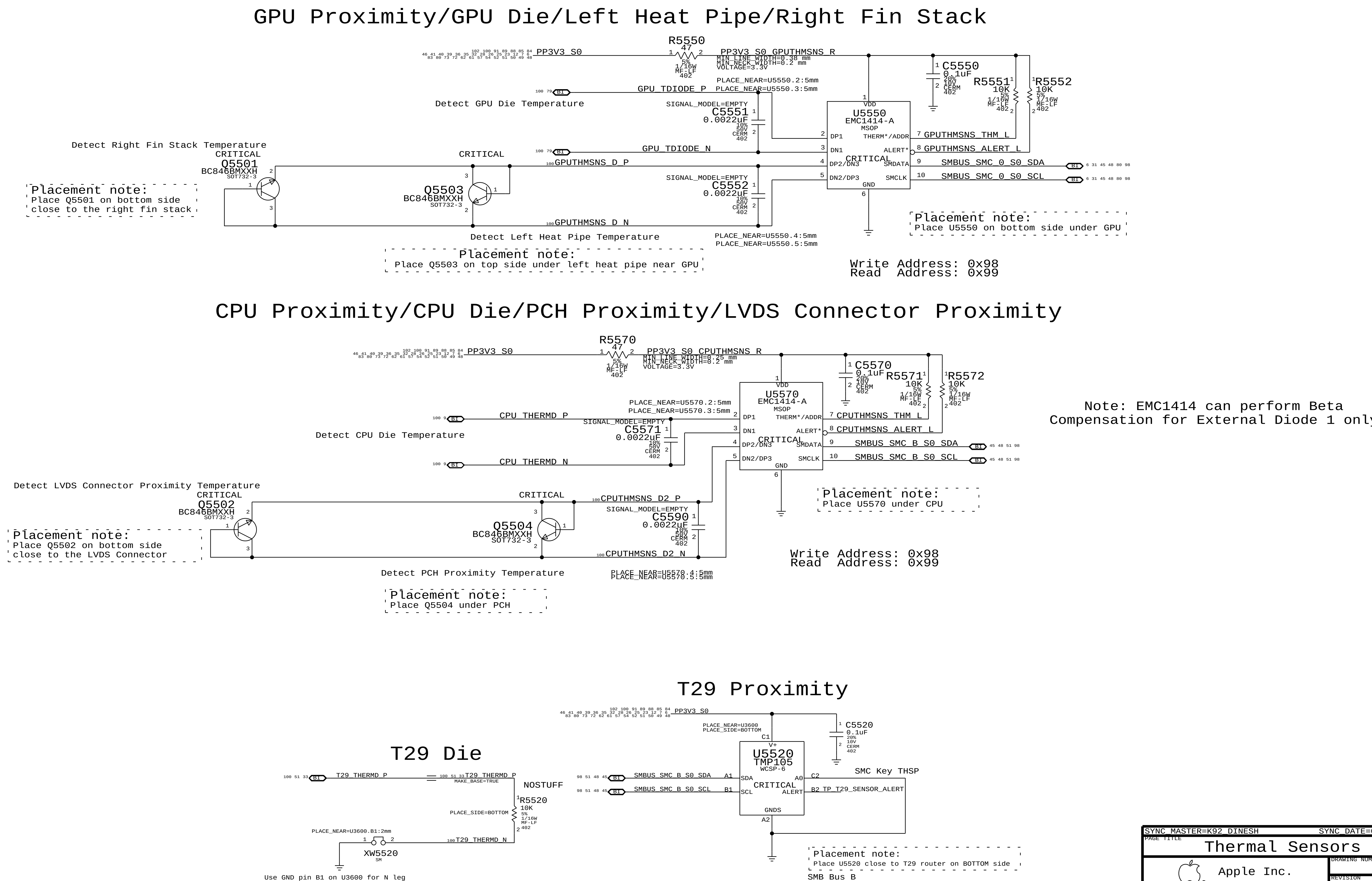
PAGE TITLE: High Side and CPU/AXG Current Sensing

Apple Inc.

DRAWING NUMBER — SIZE D

REVISION

BRANCH



SYNC_MASTER=K92_DINESH SYNC_DATE=09/24/2010

PAGE TITLE

Thermal Sensors

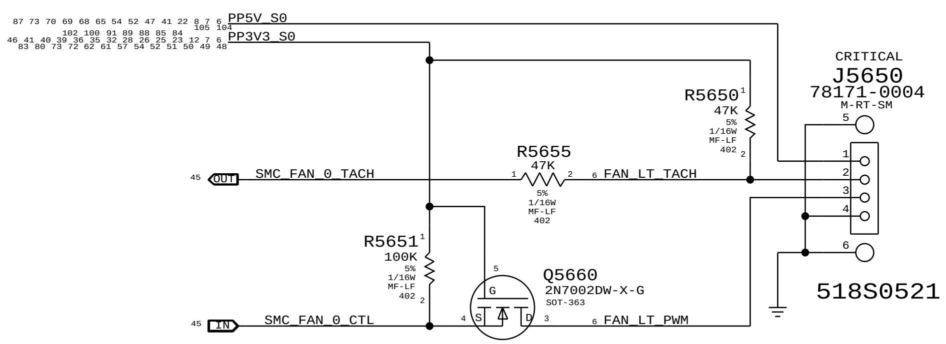
Apple Inc.

DRAWING NUMBER SIZE D

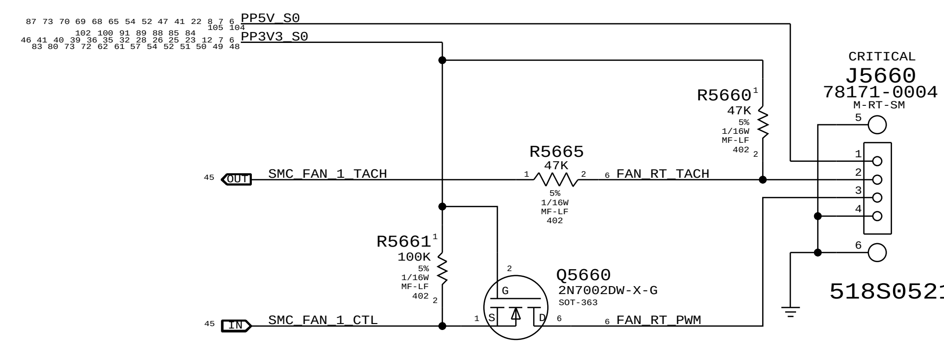
REVISION

BRANCH

Left Fan



Right Fan



SYNC_MASTER=K17_MLB SYNC_DATE=04/26/2010

PAGE TITLE

Fan Connectors

Apple Inc.

DRAWING NUMBER

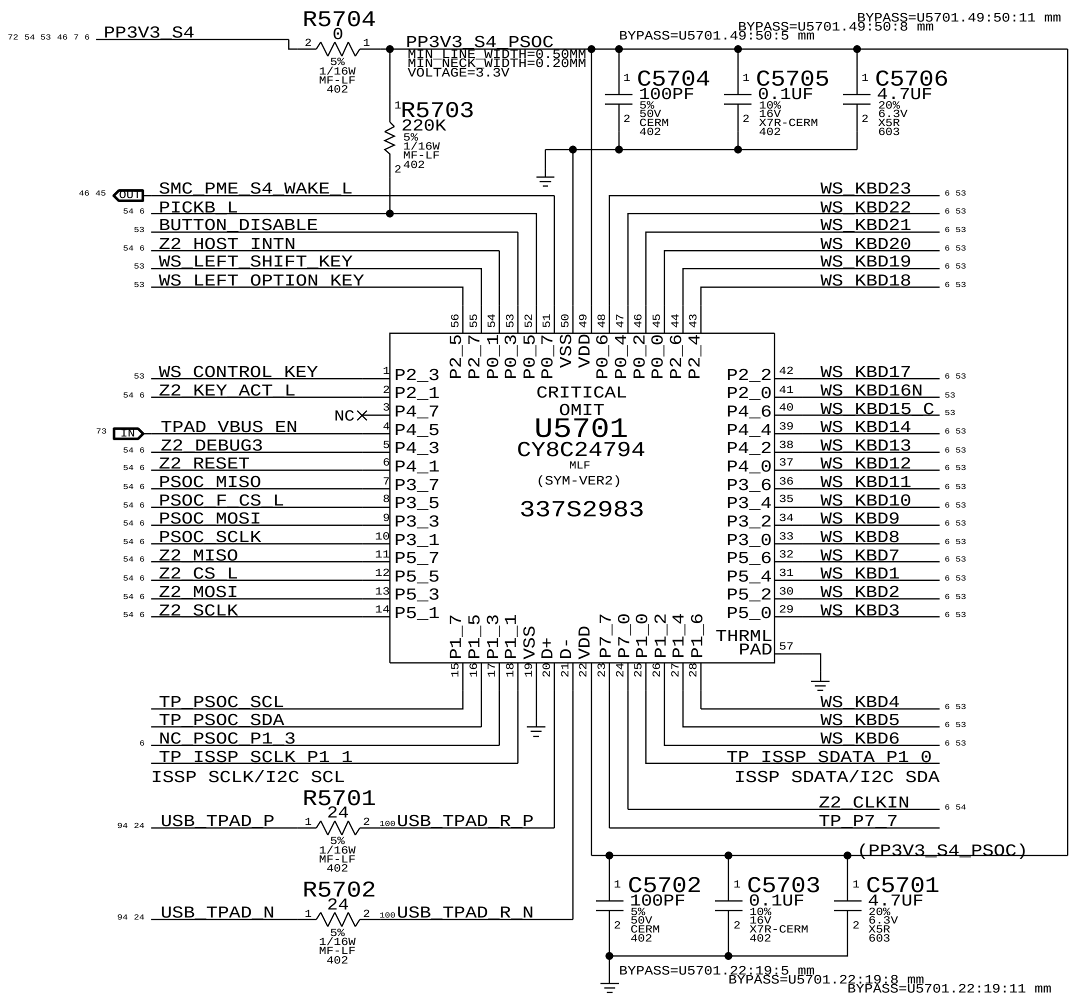
SIZE D

REVISION

BRANCH

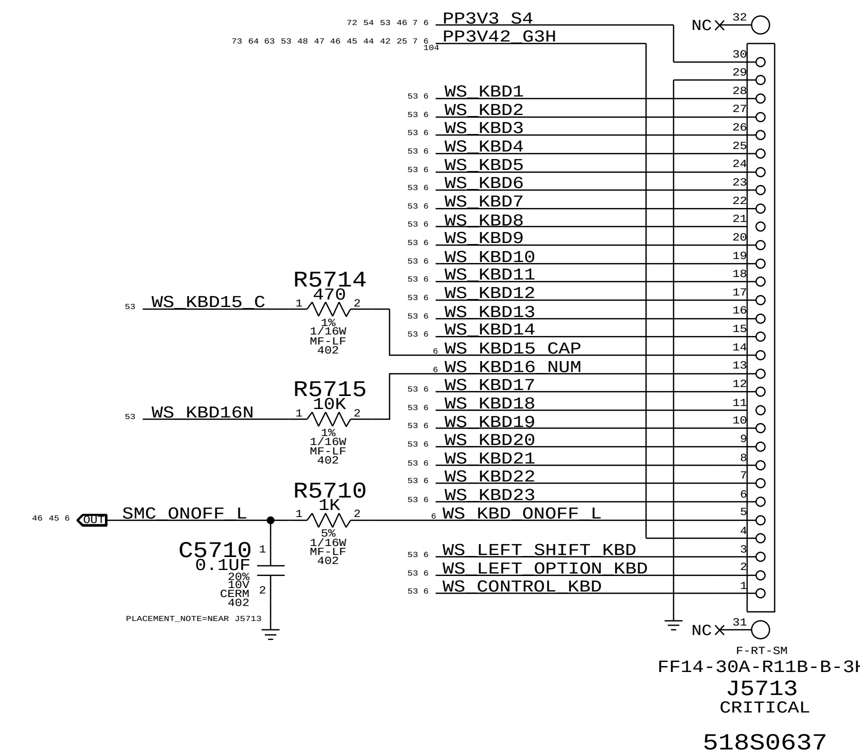
PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA 80UA	2.55 KOHM	0.0255 V 0.204 V	0.255E-6 W 16.32E-6 W
3V3 LDO	VDD VOUT	60MA (MAX) 60MA (MAX)	10 OHM 0.2 OHM	0.6 V 0.012 V	36E-3 W 0.72E-3 W
PSOC	VDD	8MA (TYP) 14MA (MAX)	1.5 OHM	0.012 V 0.021 V	96E-6 W 294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

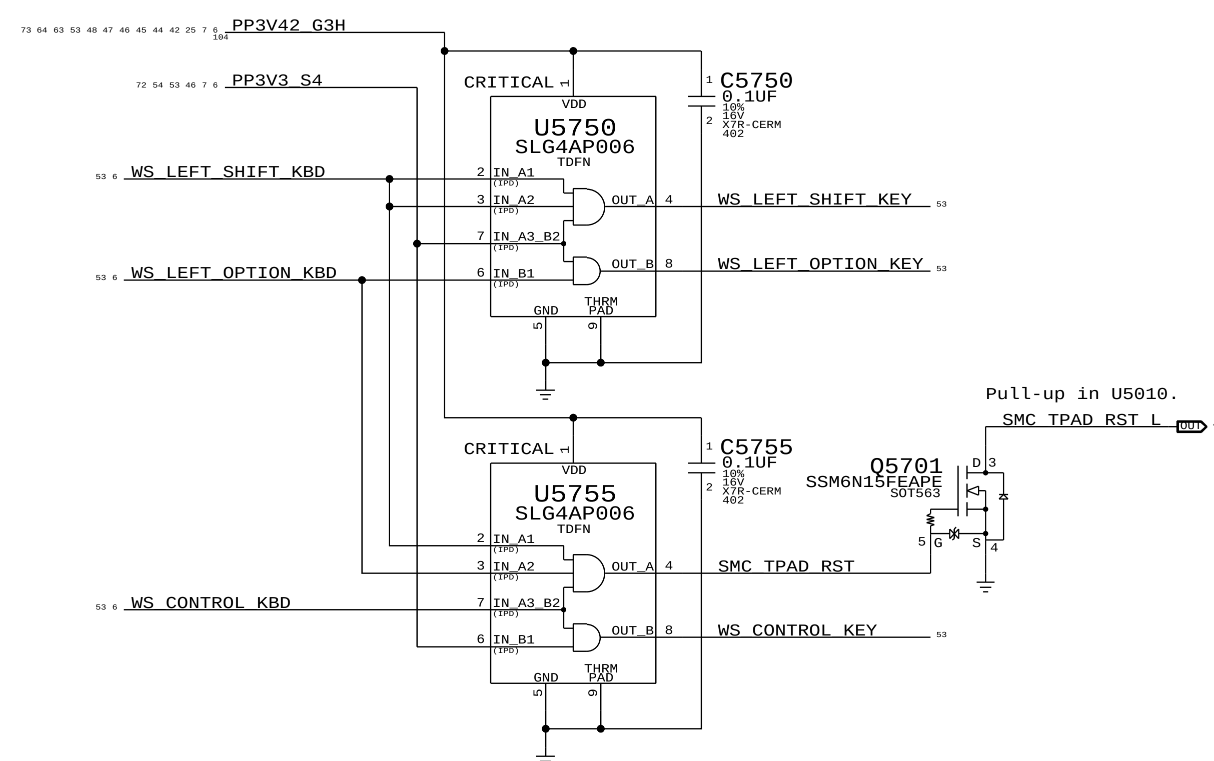
Keyboard Connector



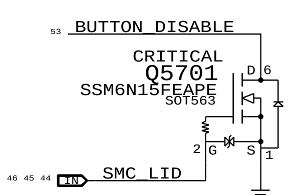
SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.

Keys ANDed with PSOC power to isolate when PSOC is not powered.



TPAD Buttons Disable



PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

SYNC_MASTER=K92_ERIC SYNC_DATE=10/11/2010

PAGE TITLE: WELLSPRING 1

Apple Inc.

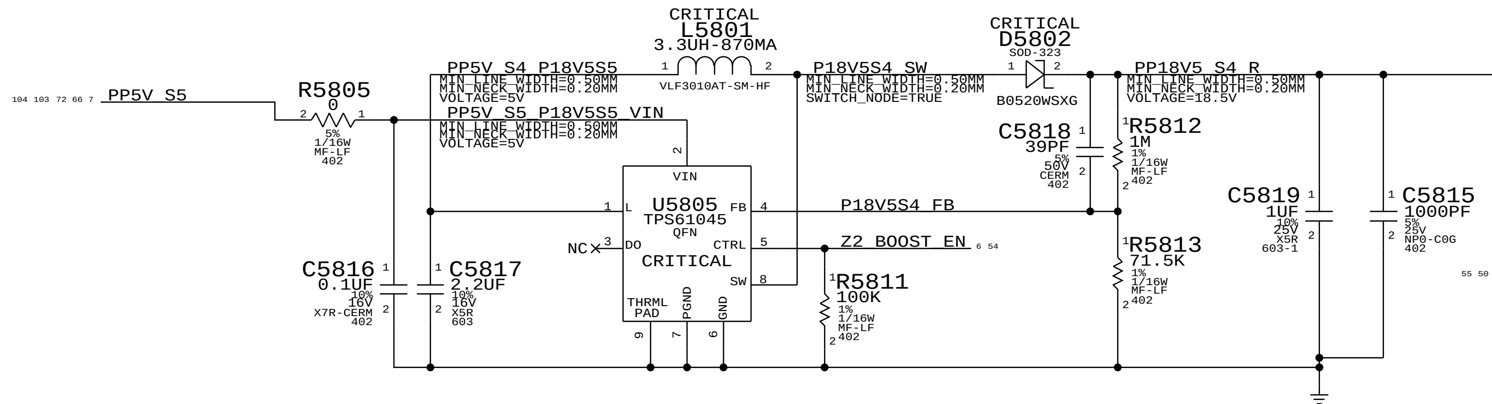
DRAWING NUMBER SIZE D

REVISION

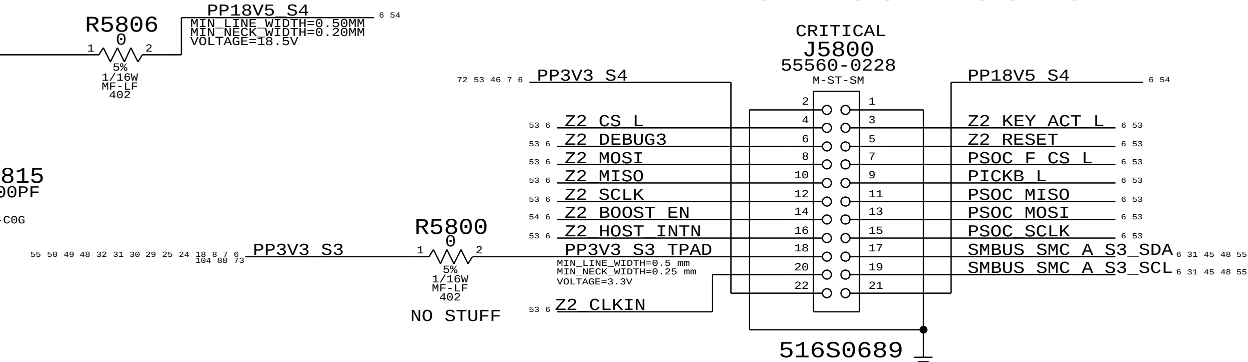
BRANCH

BOOSTER +18.5VDC FOR SENSORS

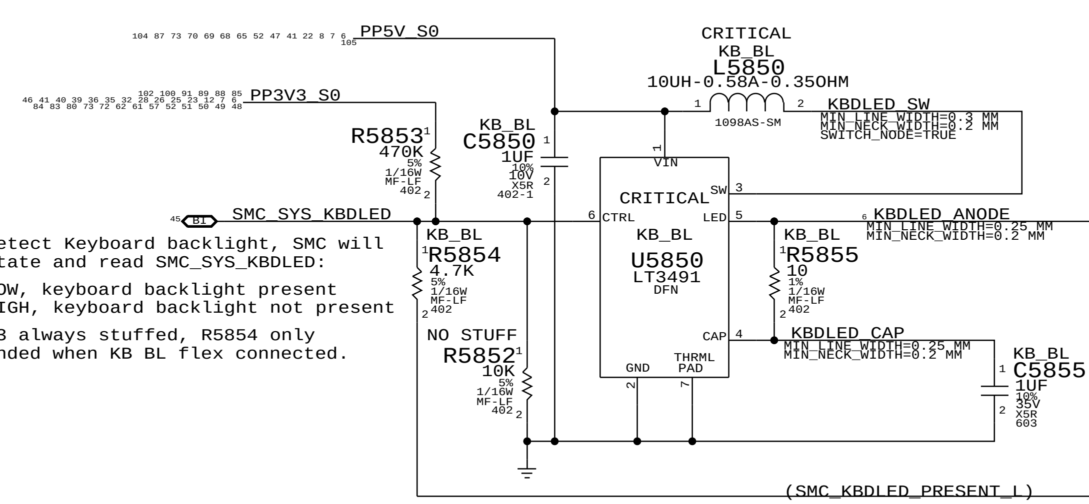
BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



IPD Flex Connector



Keyboard Backlight Driver & Detection

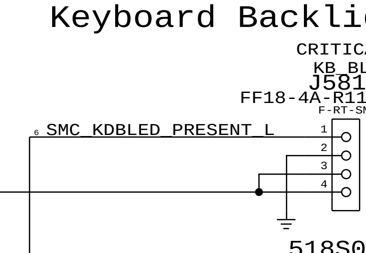


To detect Keyboard backlight, SMC will tristate and read SMC_SYS_KBDLED:

If LOW, keyboard backlight present
If HIGH, keyboard backlight not present

R5853 always stuffed, R5854 only grounded when KB BL flex connected.

Keyboard Backlight Connector



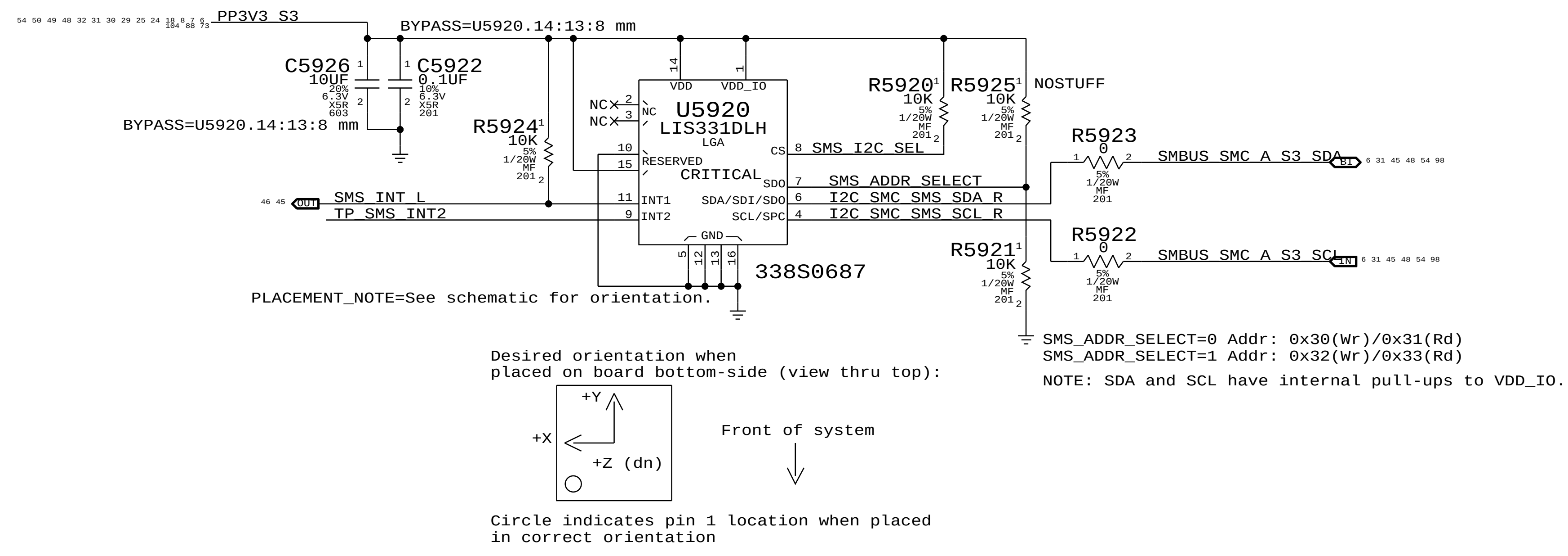
J5815 pin 1 is grounded on keyboard backlight flex

SYNC_MASTER=K92_ERIC SYNC_DATE=07/27/2010

PAGE TITLE
WELLSPRING 2

Apple Inc.

DRAWING NUMBER
SIZE D
REVISION
BRANCH



SYNC_MASTER=K92_DINESH SYNC_DATE=06/02/2010

PAGE TITLE

Digital Accelerometer

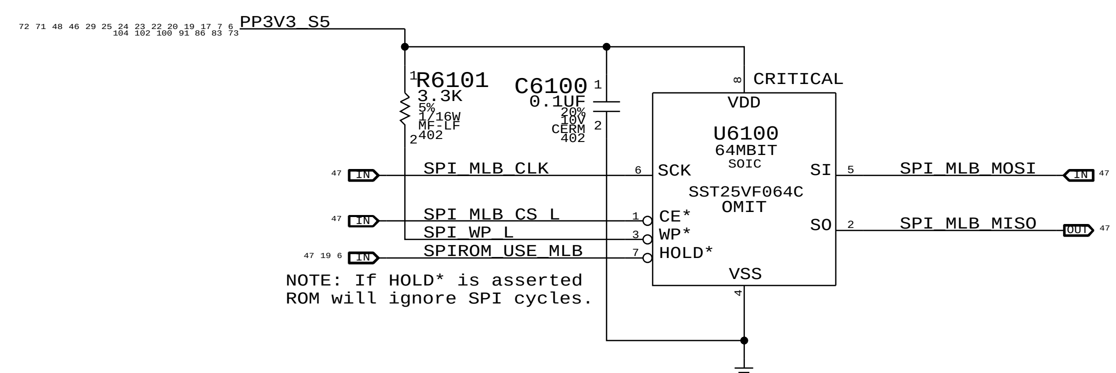
Apple Inc.

DRAWING NUMBER

SIZE D

REVISION

BRANCH



SYNC_MASTER=K92_BEN SYNC_DATE=05/27/2010

PAGE TITLE

SPI ROM

Apple Inc.

DRAWING NUMBER

SIZE D

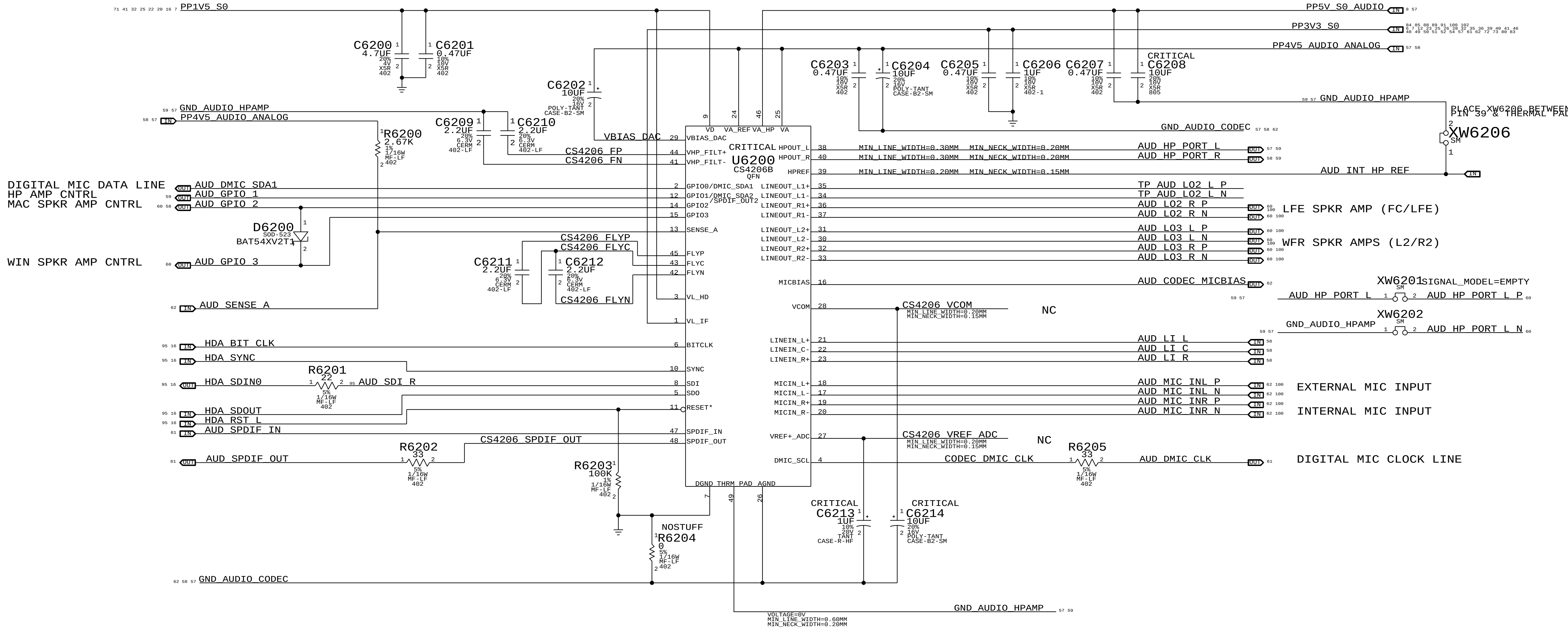
REVISION

BRANCH

NOTICE OF PROPRIETARY PROPERTY:

AUDIO CODEC

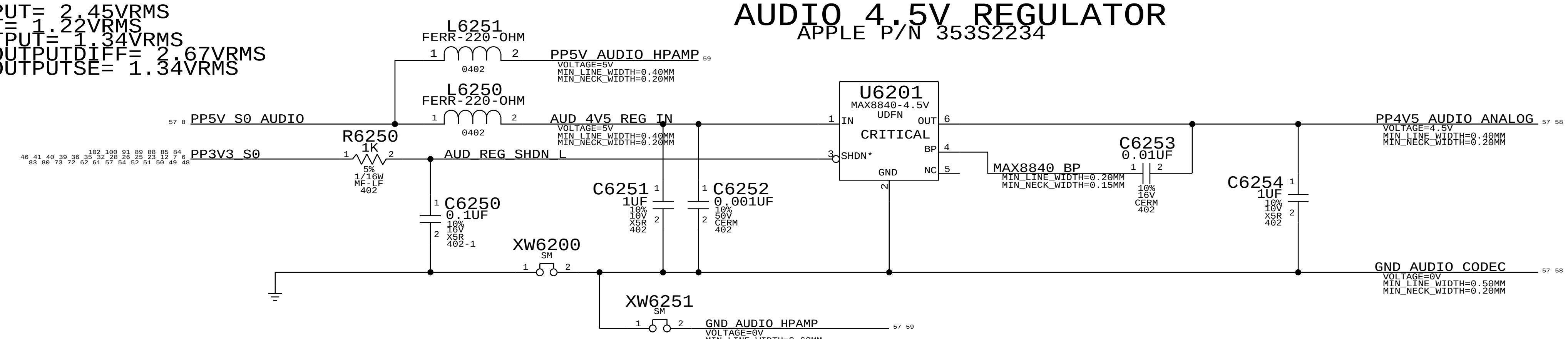
APPLE P/N 353S3199



DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

AUDIO 4.5V REGULATOR

APPLE P/N 353S2234

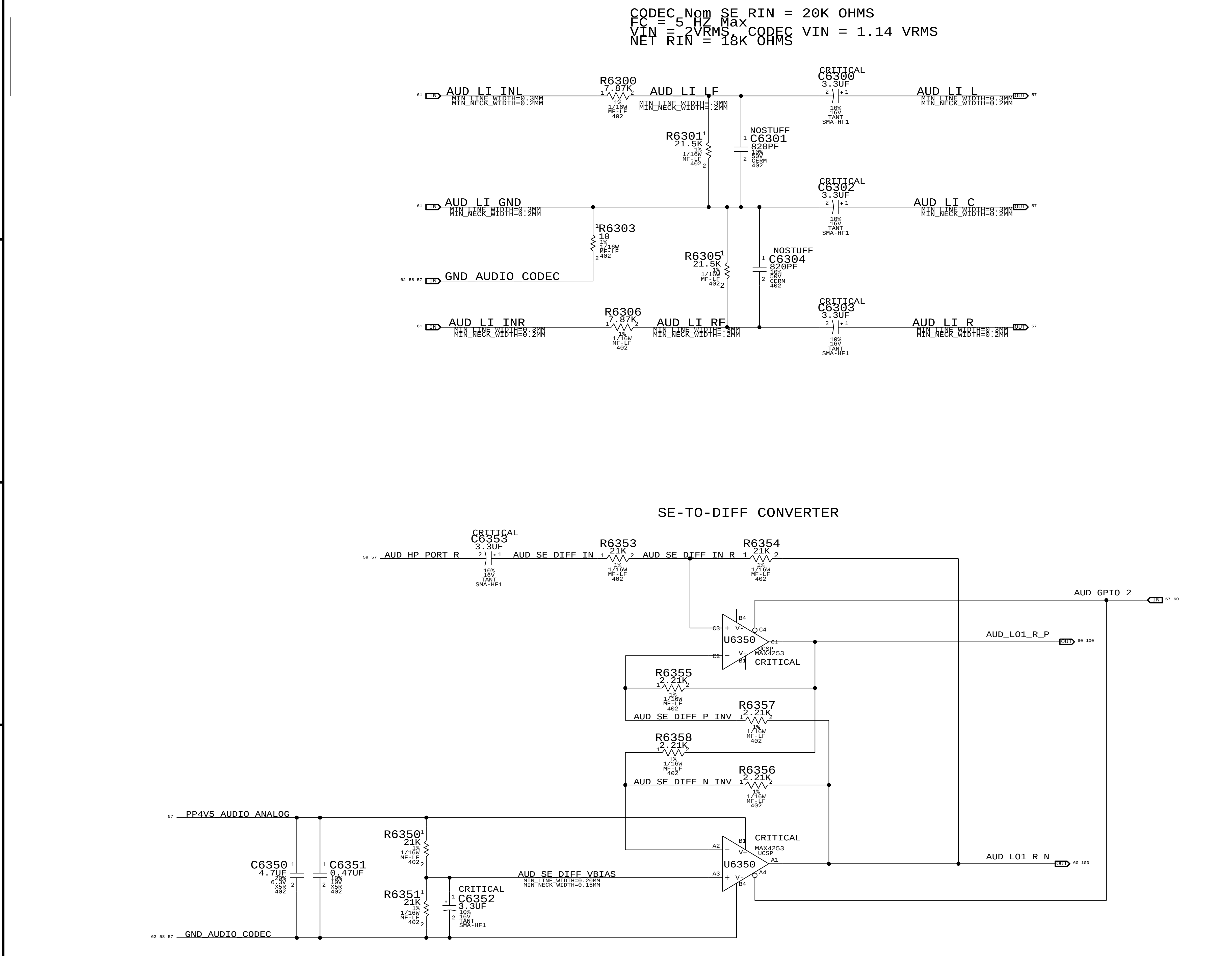


SYNC_MASTER=K92_KAVITHA SYNC_DATE=07/30/2010

PAGE TITLE: AUDIO:CODEC

Apple Inc.

DRAWING NUMBER | SIZE D | REVISION | BRANCH



SYNC_MASTER=K92_AUDIO SYNC_DATE=06/16/2010

PAGE TITLE

AUDIO: LINE IN

Apple Inc.

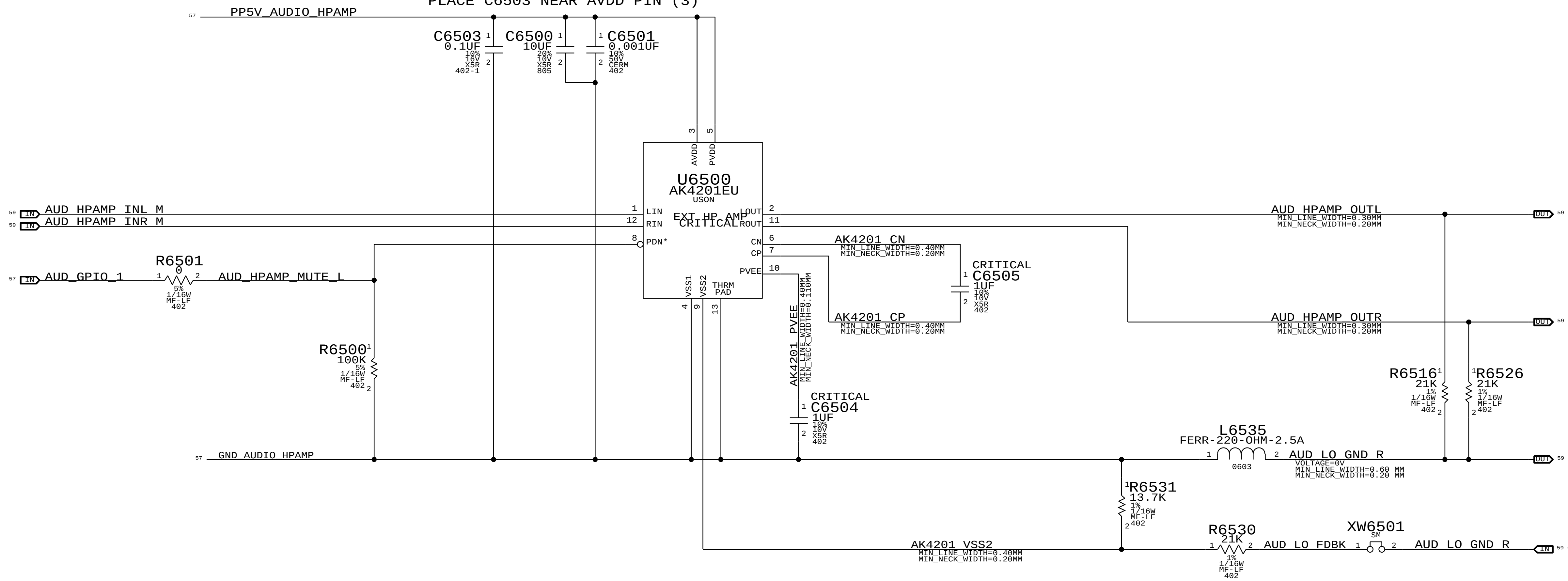
DRAWING NUMBER

SIZE D

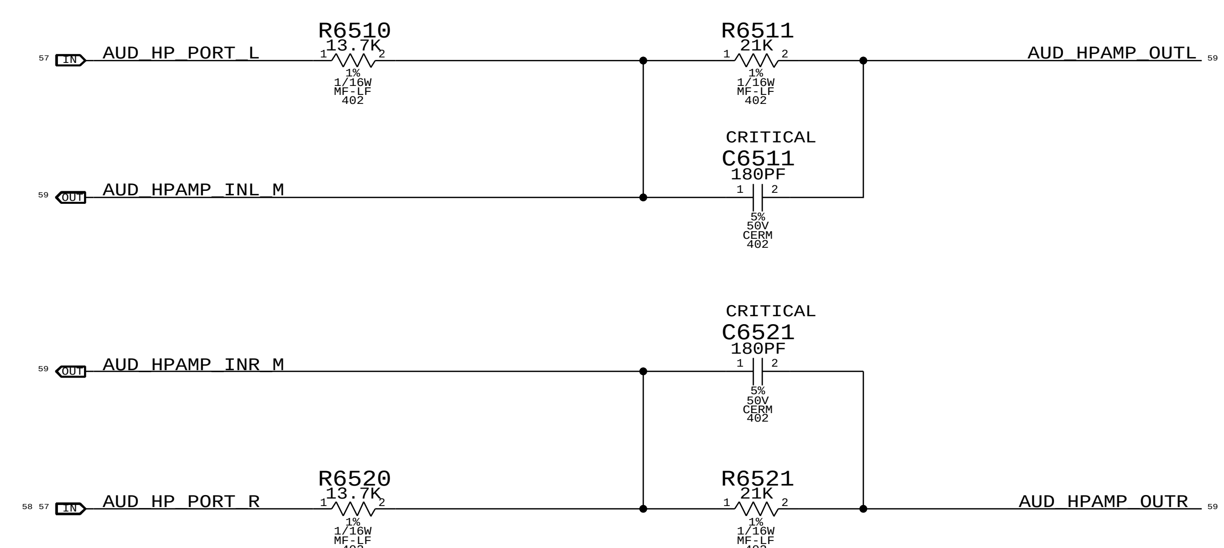
REVISION

BRANCH

HEADPHONE AMPLIFIER (AK4201)
APN:353S2347
VOLTAGE GAIN:1.53



1ST ORDER DAC FILTER
LP:42.10 KHZ



SYNC_MASTER=K92_KAVITHA SYNC_DATE=10/22/2010

PAGE TITLE: AUDIO: HEADPHONE OUT

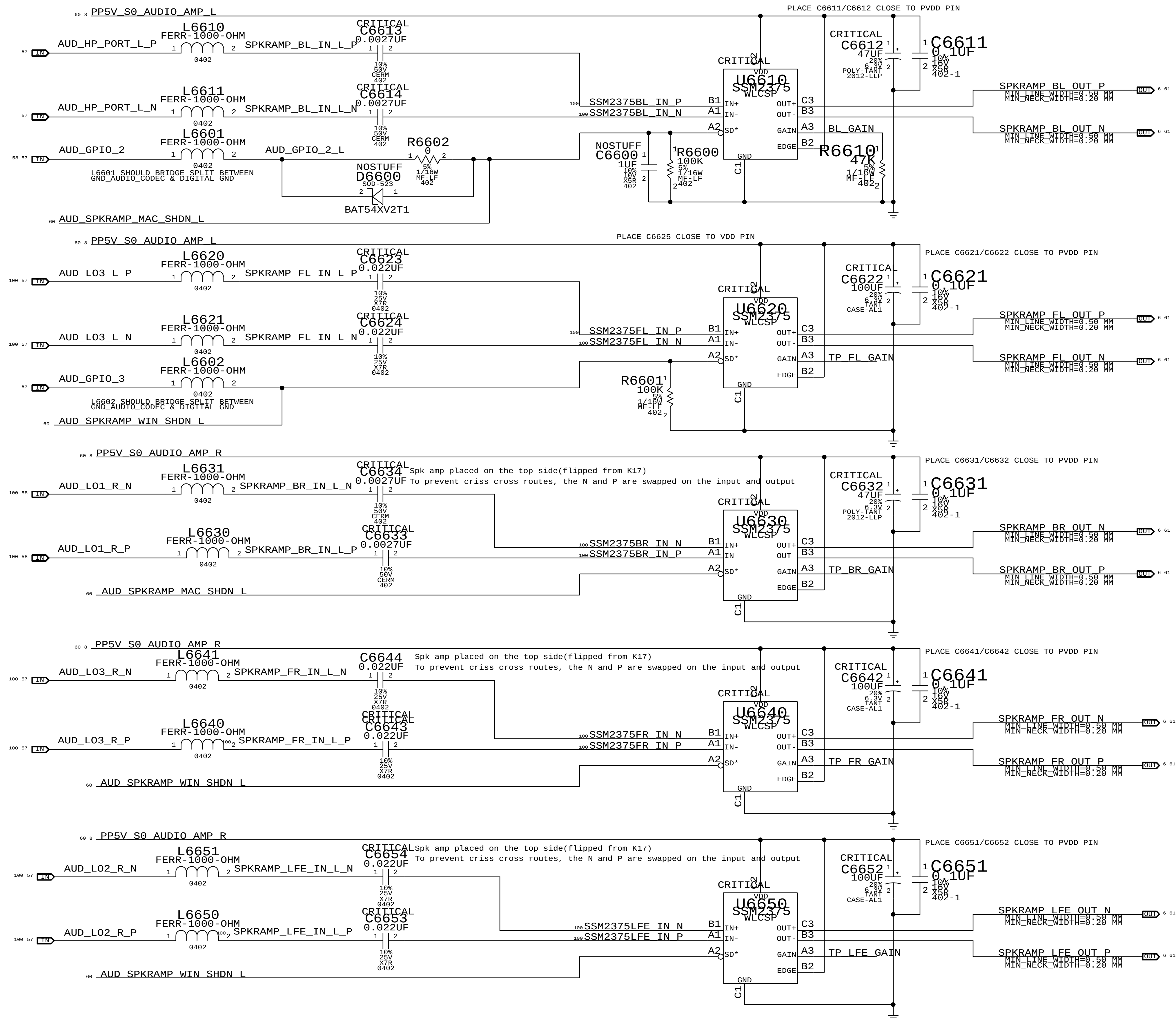
Apple Inc.

DRAWING NUMBER | SIZE D | REVISION | BRANCH

5X MONO SPEAKER AMPLIFIERS (SSM2375)

APN: 353S2958
GAIN = +3 DB (BR, FL, FR, LFE), +9 DB (BL)

FC (SPEAKERS BL/BR) = ~737 HZ
FC (SPEAKERS FL/FR/LFE) = ~90 HZ



SYNC_MASTER=K92_KAVITHA SYNC_DATE=10/22/2010

PAGE TITLE

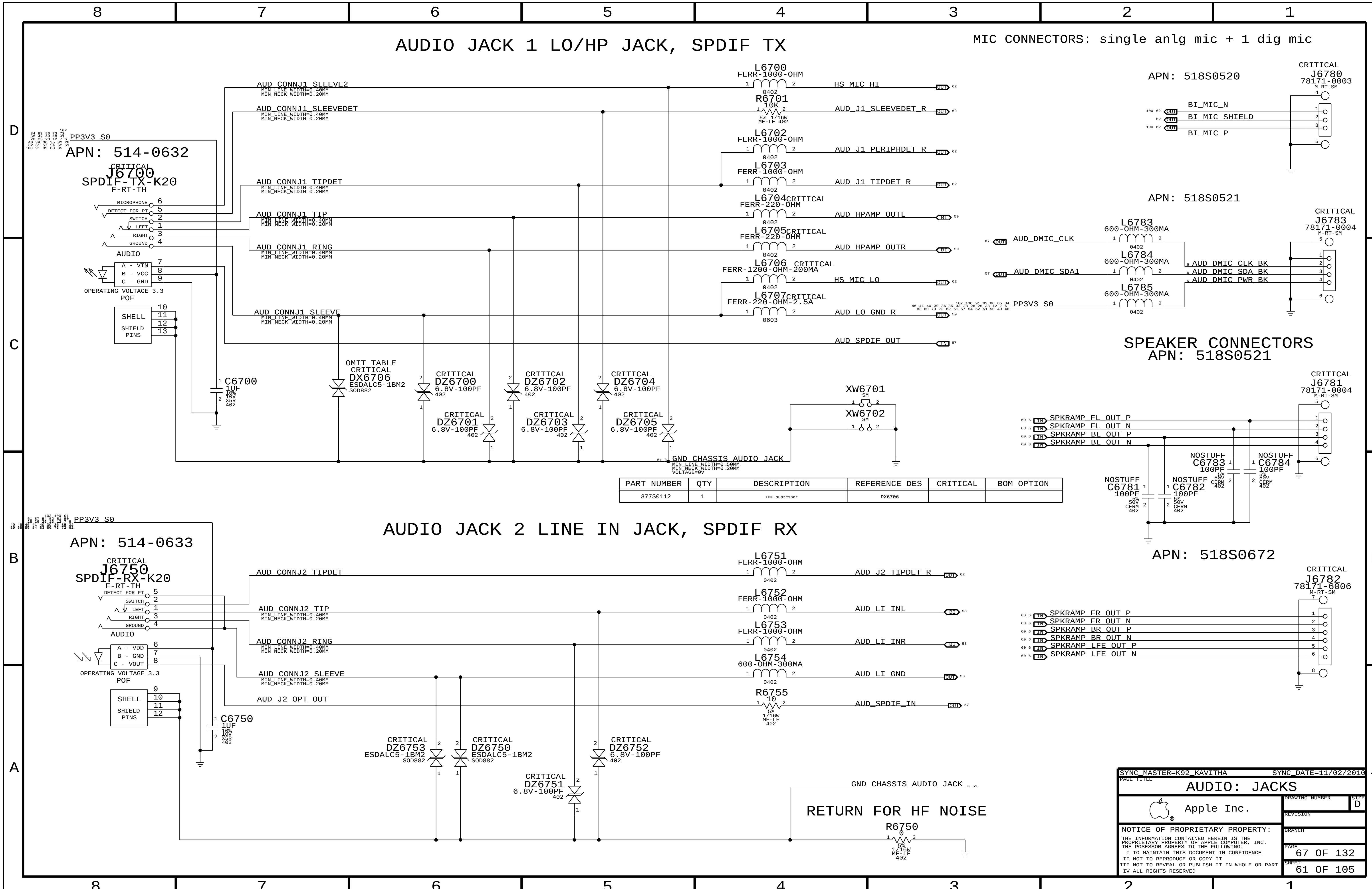
AUDIO:SPEAKER AMP

Apple Inc.

DRAWING NUMBER SIZE D

REVISION

BRANCH



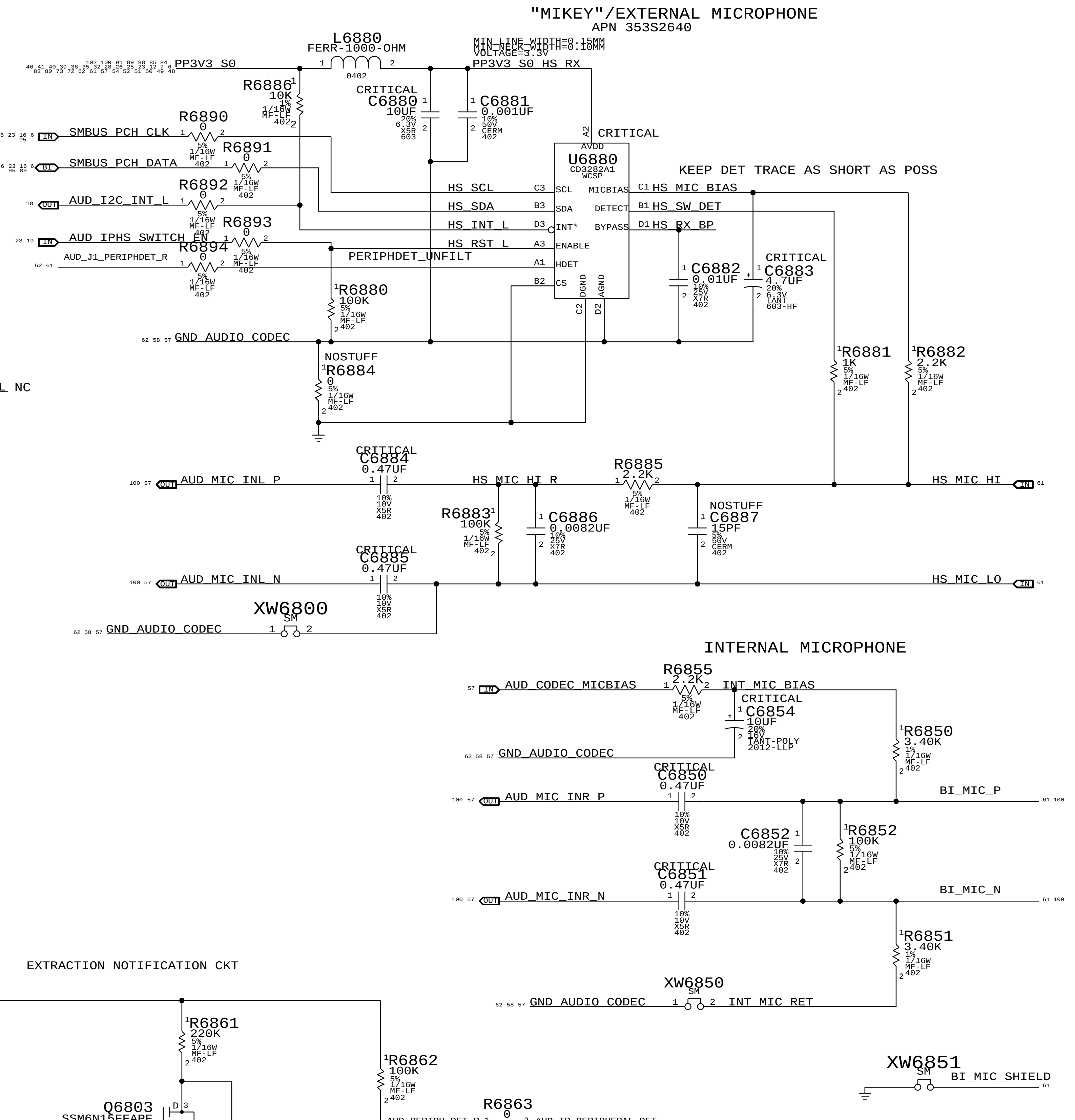
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
377S0112	1	EMC supressor	DX6706		

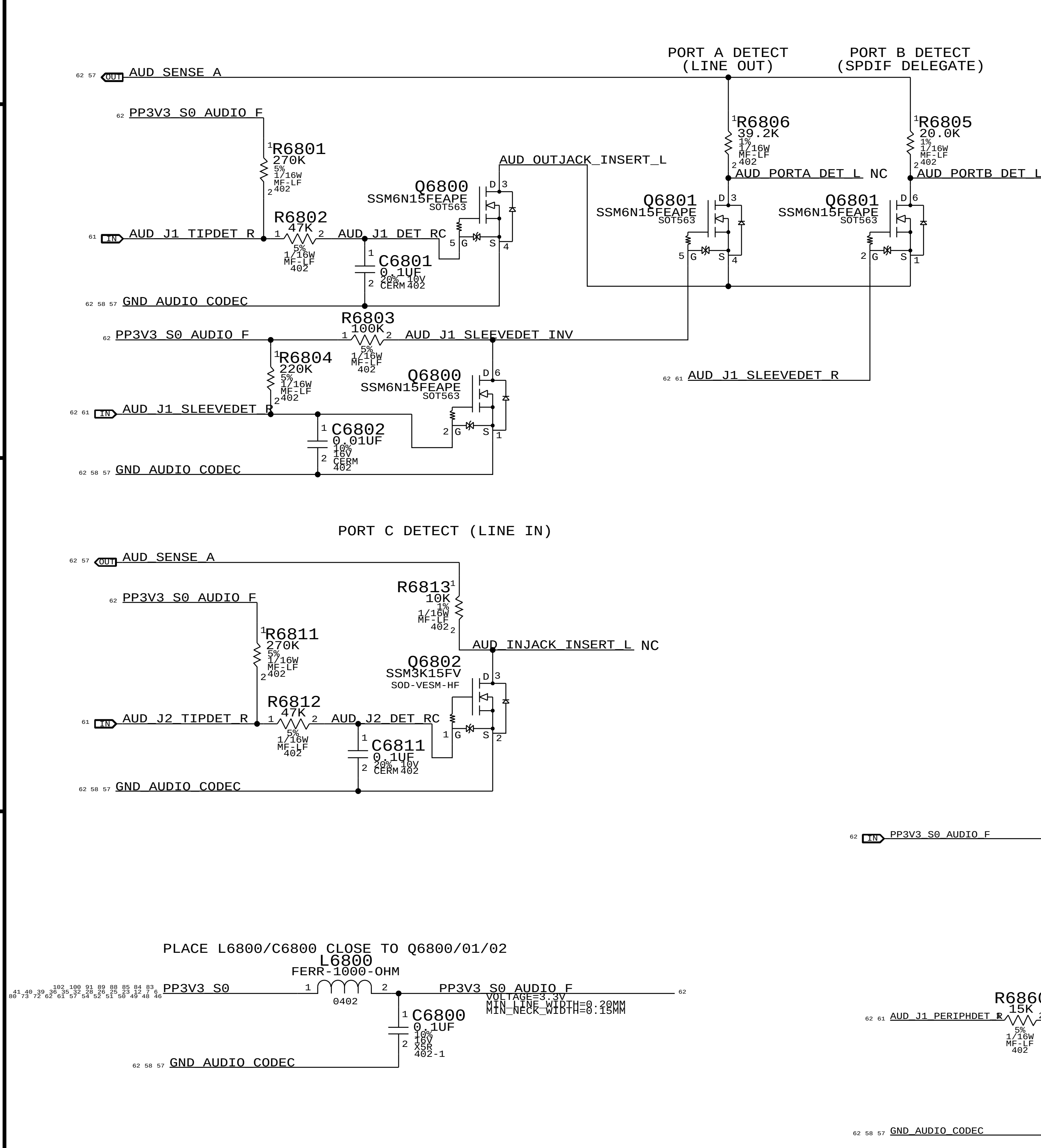
CODEC OUTPUT SIGNAL PATHS

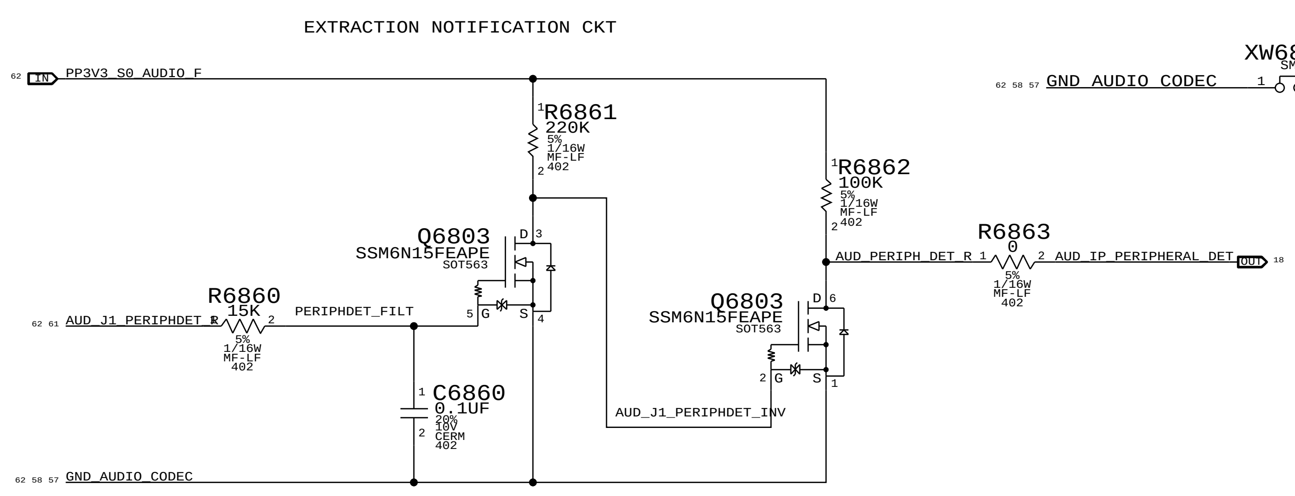
FUNCTION	VOLUME/MUTE	CONVERTER	PIN COMPLEX	MAC OS SHDN	WIN SHDN	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	N/A	N/A	0X09 (A)
SPEAKERS BL/BR	0X02 (2)	0X02 (2)	0X09 (9,V23)	GPIO_2	N/A	N/A
SPEAKERS FL/FR	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_2	GPIO_3	N/A
SPEAKER LFE	0X03 (3)	0X03 (3)	0X0A (10,D)	GPIO_2	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0x10 (16)	N/A	N/A	0X0D (B)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X05 (5)	0X12 (12,C)	N/A	0X12 (C)
SPDIF IN	0X07 (7)	0X0F (15)	N/A	N/A
INTERNAL MIC	0X06 (6)	0X0D (13,B,RIGHT)	MICBIAS (80%)	N/A
EXTERNAL MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY







SYNC_MASTER=K92_KAVITHA SYNC_DATE=11/22/2010

PAGE TITLE

AUDIO: JACK TRANSLATORS

Apple Inc.

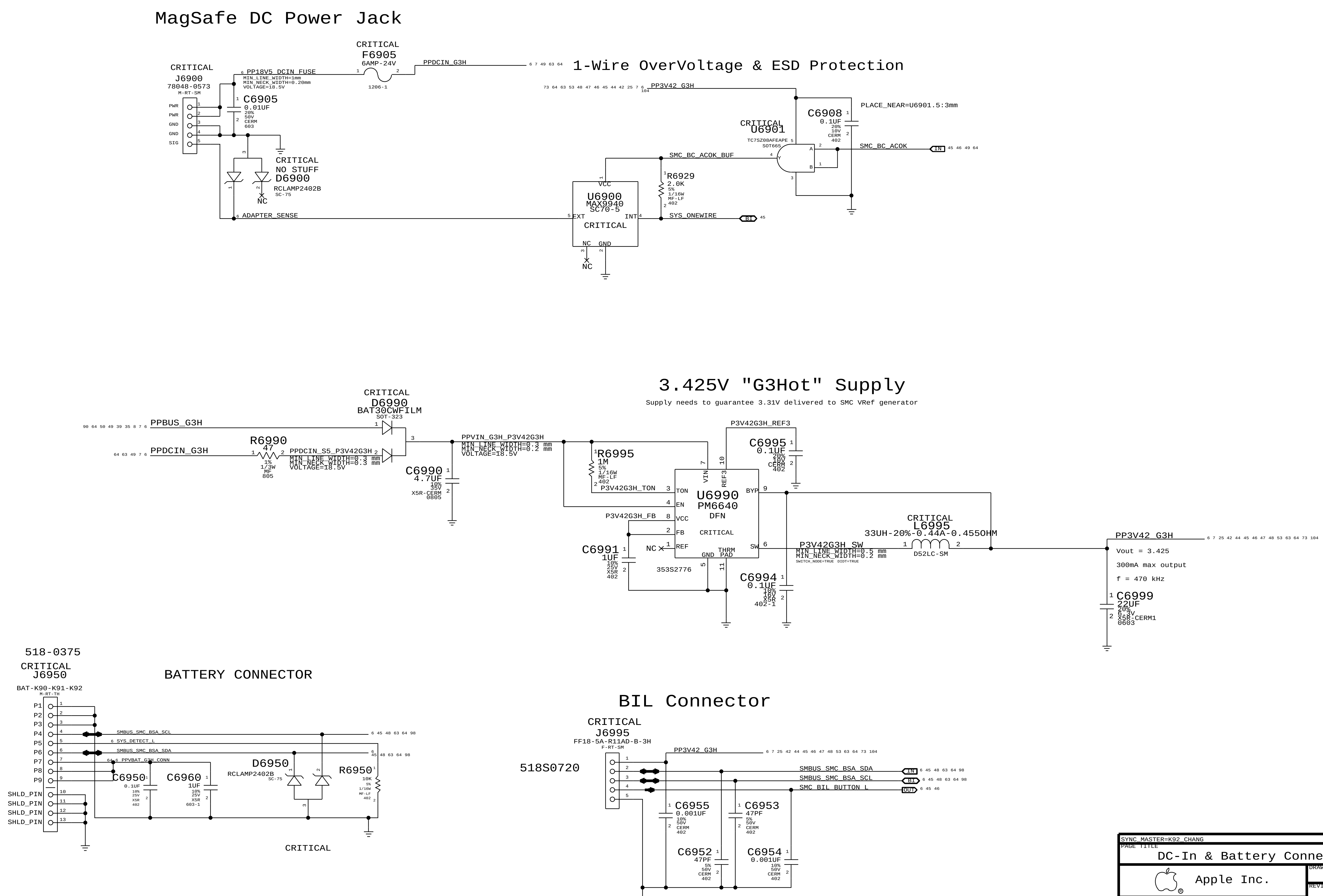
DRAWING NUMBER SIZE D

REVISION

BRANCH

PAGE 68 OF 132

SHEET 62 OF 105



SYNC_MASTER=K92_CHANG SYNC_DATE=06/28/2010

PAGE TITLE

DC-In & Battery Connectors

Apple Inc.

DRAWING NUMBER

SIZE D

REVISION

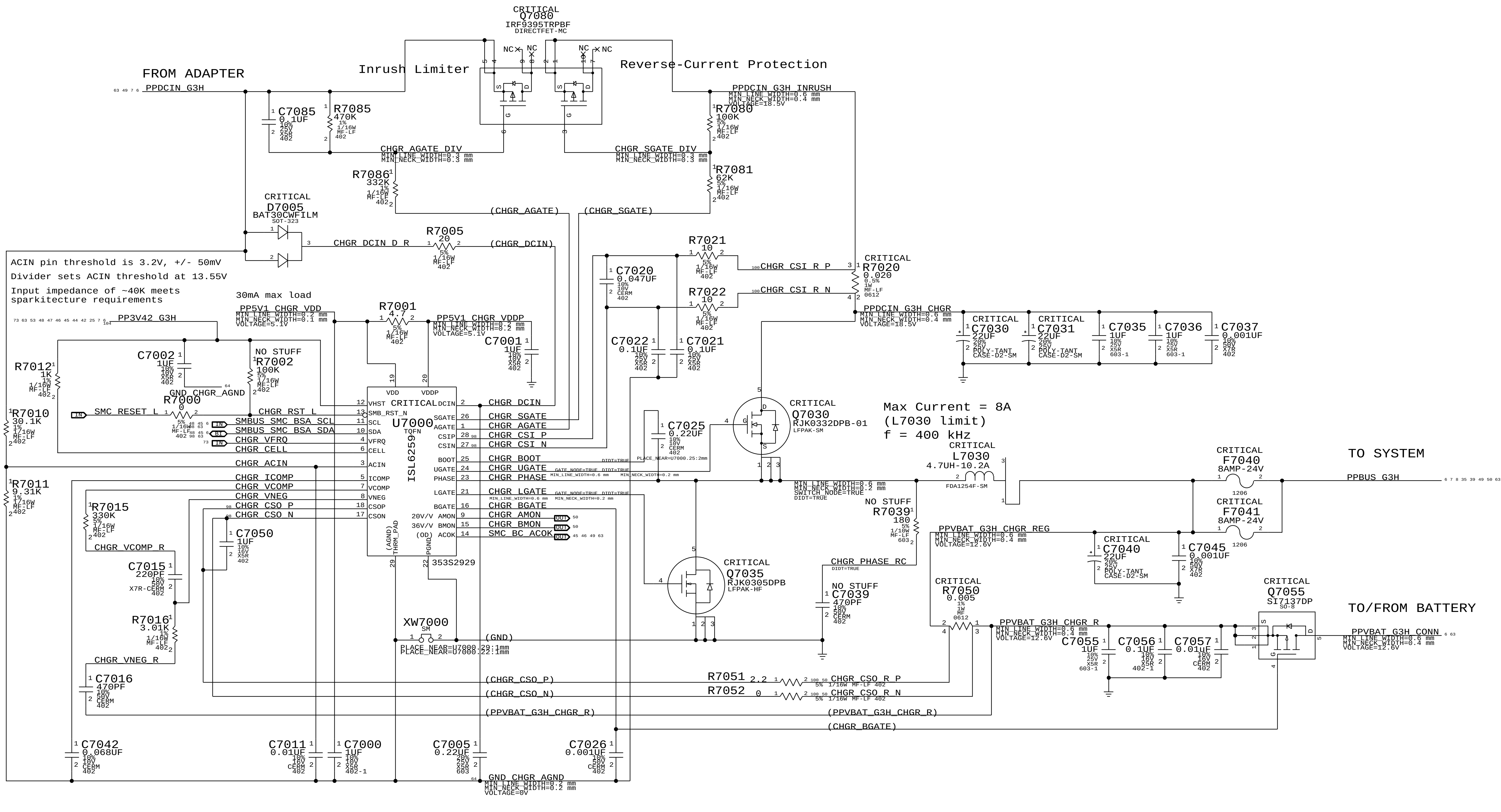
BRANCH

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PAGE 69 OF 132

SHEET 63 OF 105



SYNC_MASTER=K91_CHANG SYNC_DATE=07/21/2010

PAGE TITLE

PBus Supply & Battery Charger

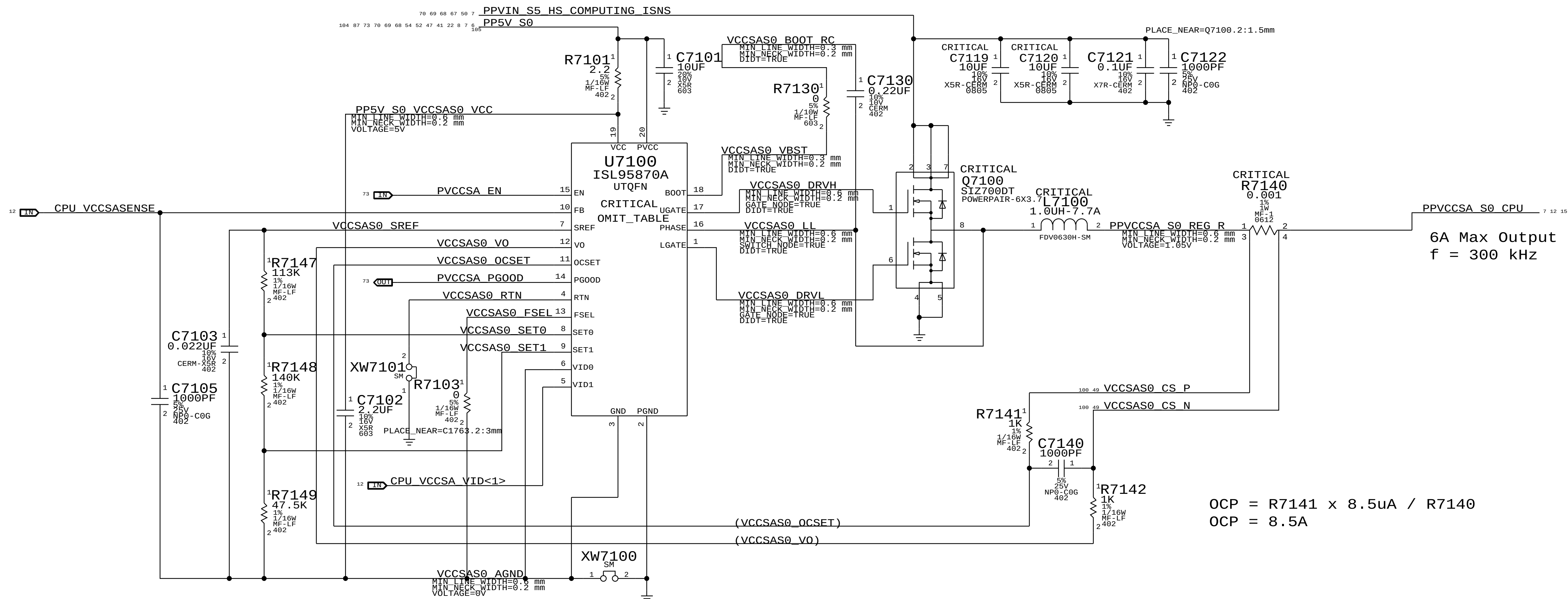
Apple Inc.

DRAWING NUMBER

SIZE D

REVISION

BRANCH



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3074	1	IC,ISL95870A,PWM,2BIT-VID,RMOT-SNSE,20P	U7100	CRITICAL	

VID1	VID0	Voltage
0	0	0.9V
1	0	0.8V

SYNC_MASTER=K91_CHANG SYNC_DATE=07/21/2010

PAGE TITLE

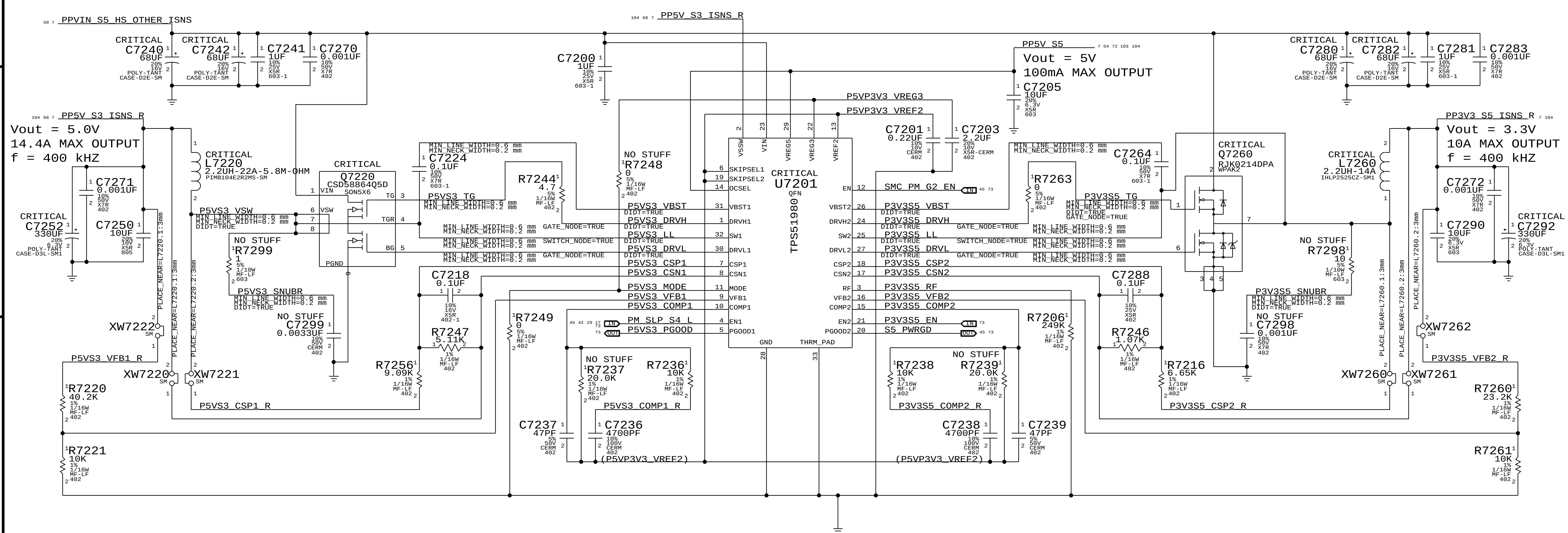
System Agent Supply

Apple Inc.

DRAWING NUMBER SIZE D

REVISION

BRANCH



SYNC_MASTER=K92_ERIC	SYNC_DATE=08/30/2010

PAGE TITLE

5V / 3.3V Power Supply

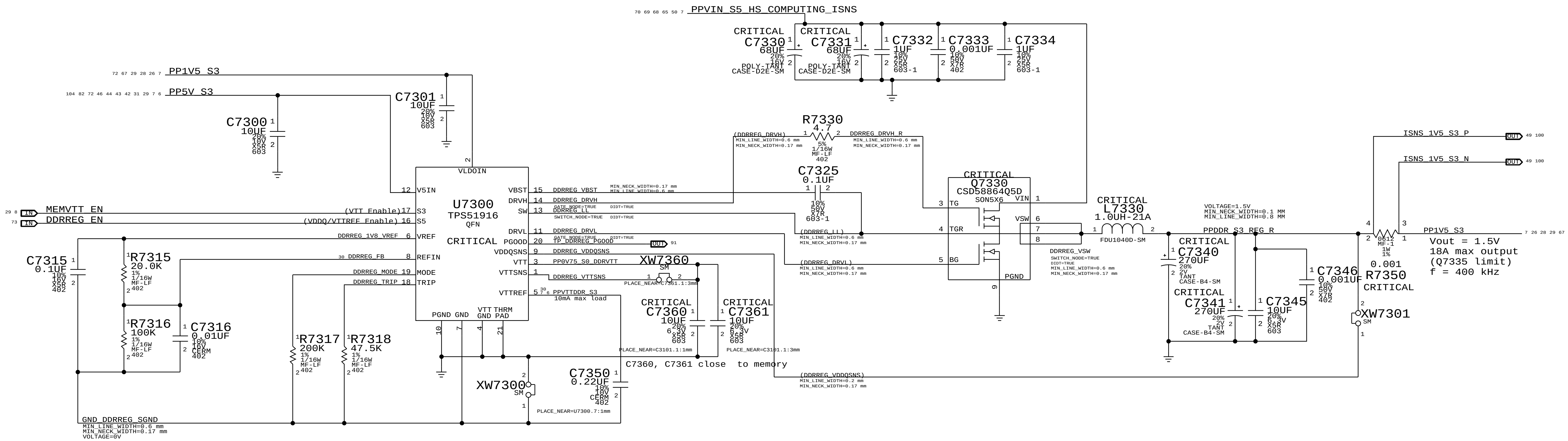
Apple Inc.

DRAWING NUMBER

SIZE D

REVISION

BRANCH



SYNC_MASTER=K91_CHANG SYNC_DATE=07/21/2010

PAGE TITLE

1.5V DDR3 Supply

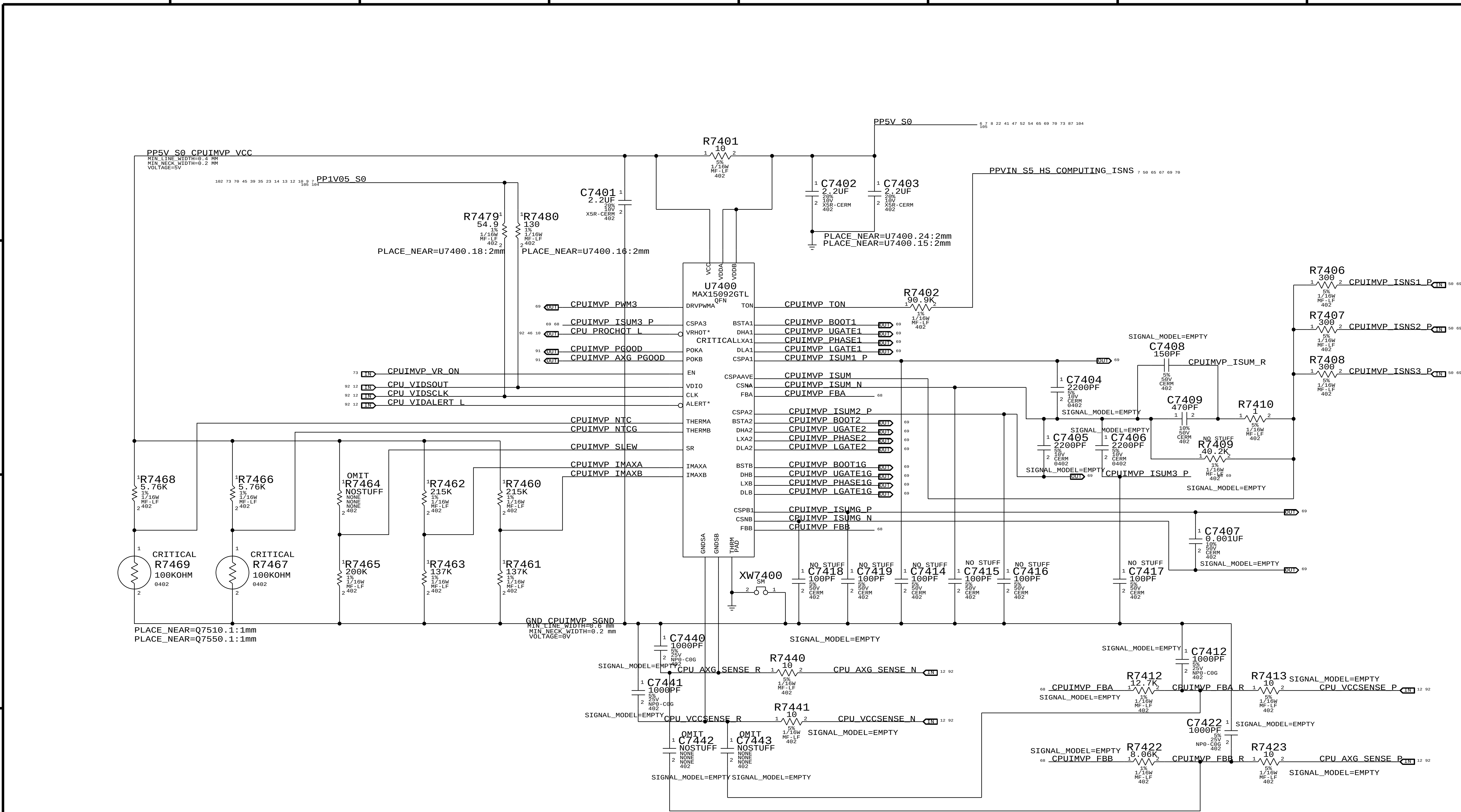
Apple Inc.

DRAWING NUMBER

SIZE D

REVISION

BRANCH



SYNC_MASTER=K92_ERIC SYNC_DATE=11/09/2010

PAGE TITLE

CPU IMVP7 & AXG VCore Regulator

Apple Inc.

DRAWING NUMBER

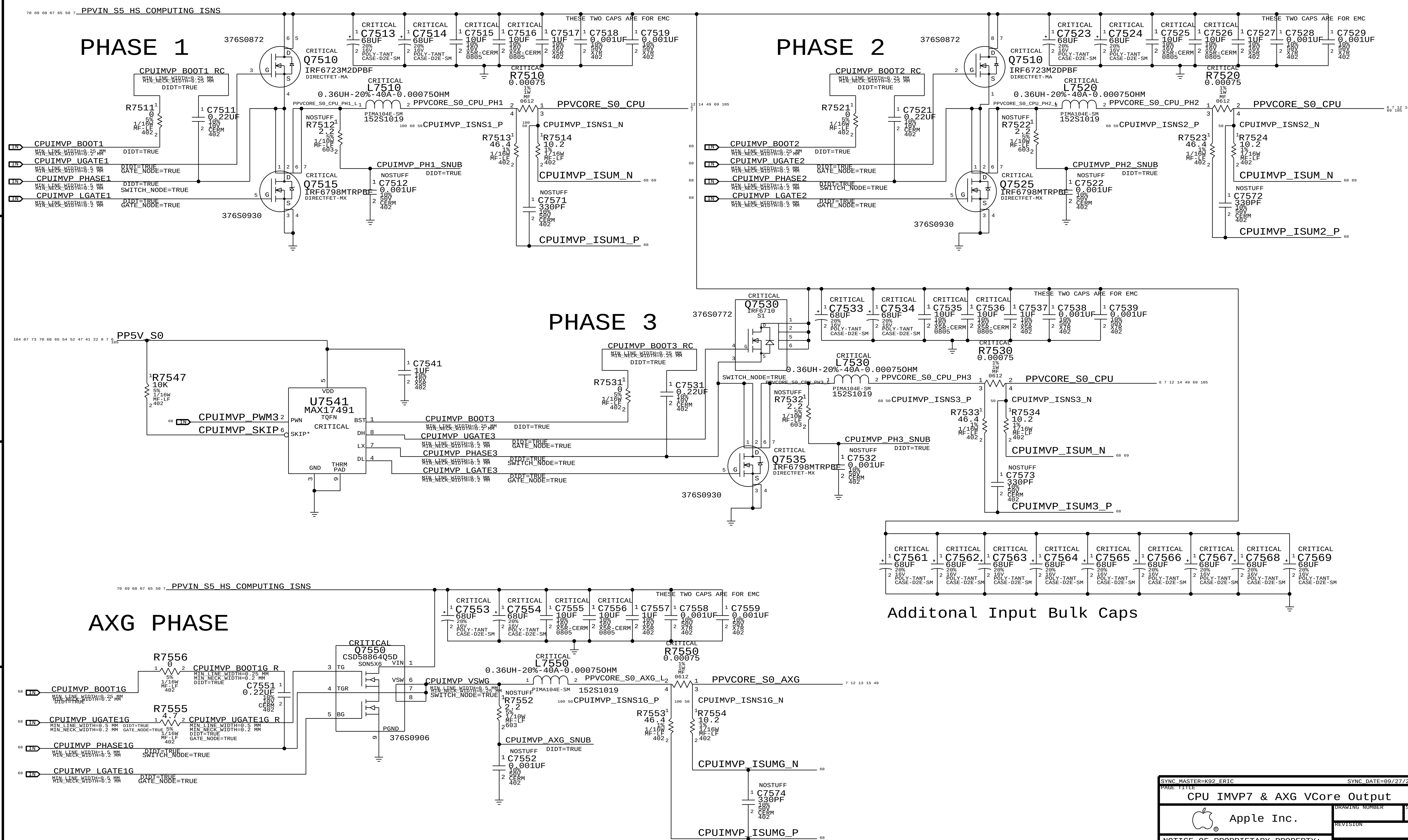
SIZE D

REVISION

BRANCH

PAGE 74 OF 132

SHEET 68 OF 105



SYNC_MASTER=K92_ERIC SYNC_DATE=09/27/2010

PAGE TITLE

CPU IMVP7 & AXG VCore Output

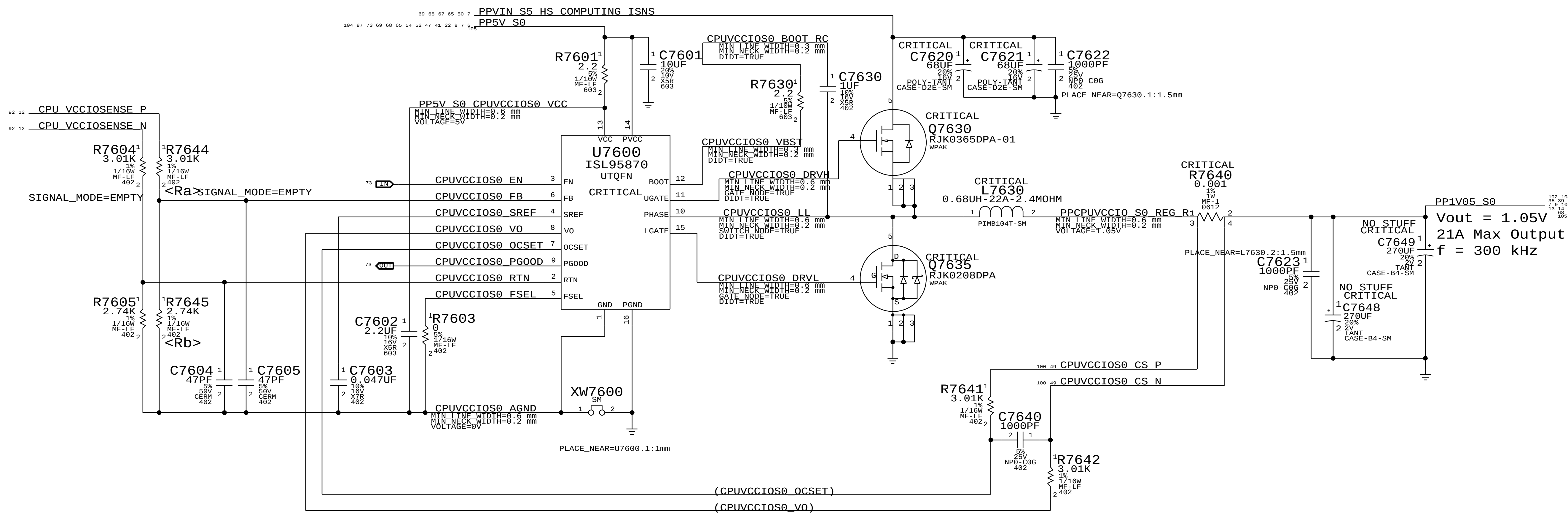
Apple Inc.

DRAWING NUMBER SIZE D

REVISION

BRANCH

CPU VCCIO (1.05V S0) Regulator



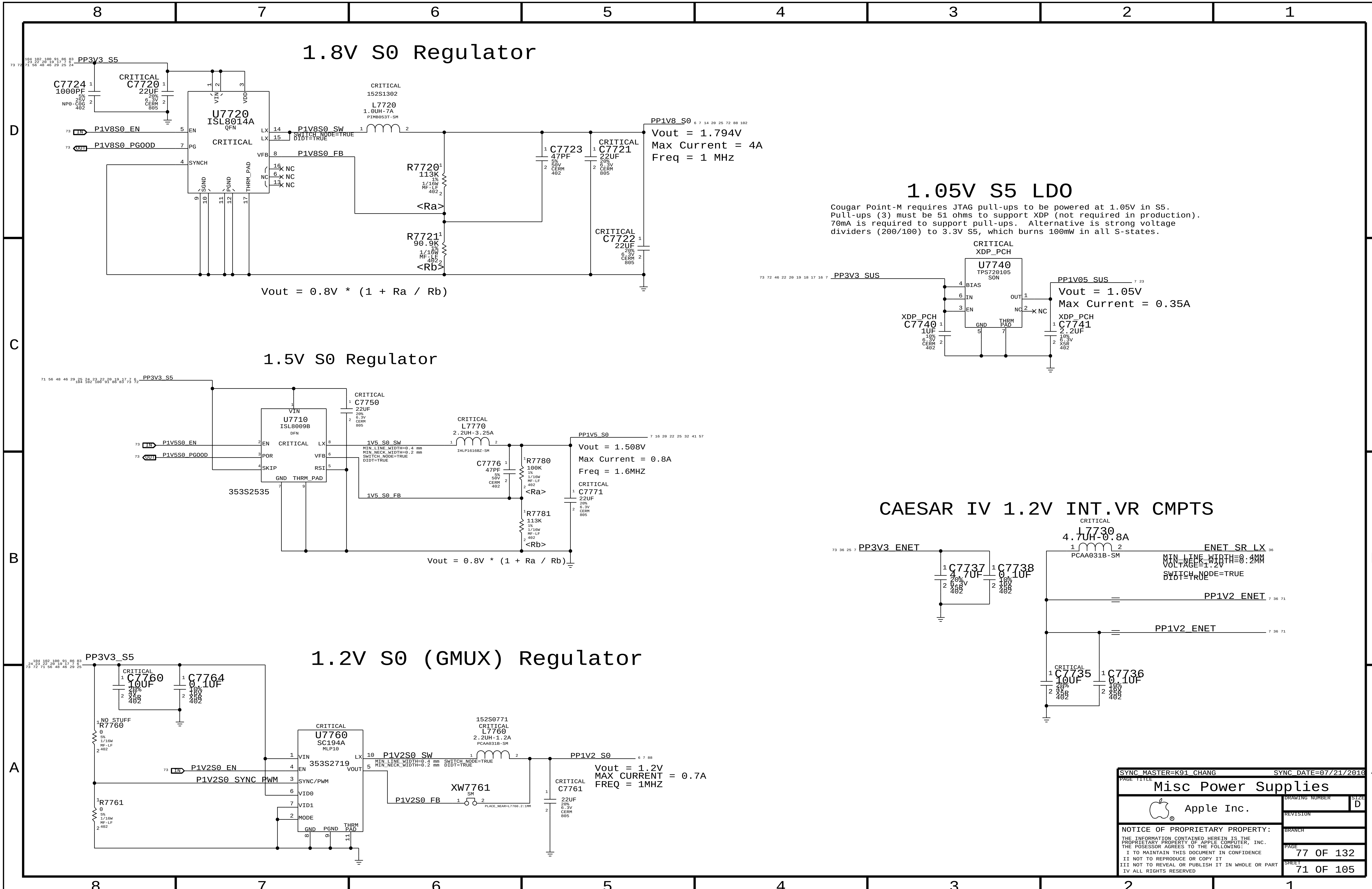
OCP = R7641 x 8.5uA / R7640
OCP = 25.6A
Vout = 0.5V * (1 + Ra / Rb)

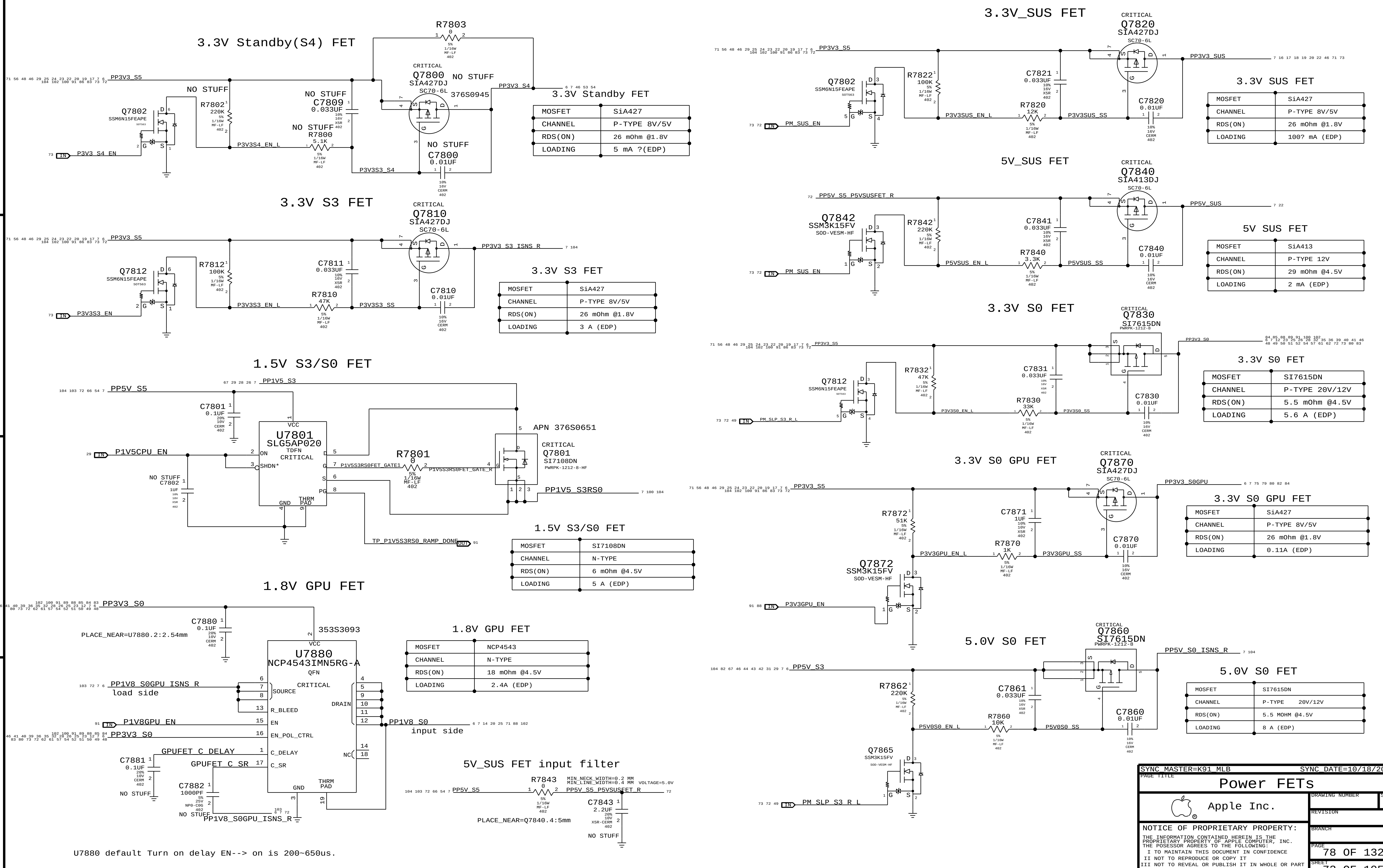
SYNC_MASTER=K92_ERIC SYNC_DATE=09/23/2010

PAGE TITLE: CPU VCCIO (1.05V) Power Supply

Apple Inc.

DRAWING NUMBER SIZE D


1.8V S0 Regulator
PP3V3_S5
C7724
1000PF
CRITICAL
C7720
22UF
U7720
ISL8014A
QFN
CRITICAL
P1V8S0_EN
P1V8S0_PGOOD
SYNCH
P1V8S0_SW
SWITCH_NODE=TRUE
DIDT=TRUE
P1V8S0_FB
CRITICAL
152S1302
L7720
1.0UH-7A
PIMB053T-SM
R7720
113K
R7721
90.9K
<Ra>
<Rb>
C7723
47PF
CRITICAL
C7721
22UF
CRITICAL
C7722
22UF
PP1V8_S0
Vout = 1.794V
Max Current = 4A
Freq = 1 MHz
Vout = 0.8V * (1 + Ra / Rb)
1.05V S5 LDO
Cougar Point-M requires JTAG pull-ups to be powered at 1.05V in S5.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.
CRITICAL
XDP_PCH
U7740
TPS720105
SON
PP3V3_SUS
PP1V05_SUS
Vout = 1.05V
Max Current = 0.35A
XDP_PCH
C7740
1UF
XDP_PCH
C7741
2.2UF
1.5V S0 Regulator
PP3V3_S5
U7710
ISL8009B
DFN
CRITICAL
P1V5S0_EN
P1V5S0_PGOOD
353S2535
CRITICAL
C7750
22UF
1V5_S0_SW
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
SWITCH_NODE=TRUE
DIDT=TRUE
1V5_S0_FB
CRITICAL
L7770
2.2UH-3.25A
IHLP1616BZ-SM
C7776
47PF
R7780
100K
<Ra>
R7781
113K
<Rb>
PP1V5_S0
Vout = 1.508V
Max Current = 0.8A
Freq = 1.6MHZ
CRITICAL
C7771
22UF
Vout = 0.8V * (1 + Ra / Rb)
CAESAR IV 1.2V INT.VR CMPTS
CRITICAL
L7730
4.7UH-0.8A
PCAA031B-SM
PP3V3_ENET
C7737
4.7UF
C7738
0.1UF
ENET_SR_LX
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.2V
SWITCH_NODE=TRUE
DIDT=TRUE
PP1V2_ENET
PP1V2_ENET
CRITICAL
C7735
10UF
C7736
0.1UF
1.2V S0 (GMUX) Regulator
PP3V3_S5
CRITICAL
C7760
10UF
C7764
0.1UF
NO STUFF
R7760
0
R7761
0
CRITICAL
U7760
SC194A
MLP10
353S2719
P1V2S0_EN
P1V2S0_SYNC_PWM
P1V2S0_SW
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
SWITCH_NODE=TRUE
DIDT=TRUE
152S0771
CRITICAL
L7760
2.2UH-1.2A
PCAA031B-SM
P1V2S0_FB
XW7761
SM
PLACE_NEAR=L7760.2:1MM
PP1V2_S0
CRITICAL
C7761
22UF
Vout = 1.2V
MAX CURRENT = 0.7A
FREQ = 1MHZ
SYNC_MASTER=K91_CHANG
SYNC_DATE=07/21/2010
PAGE TITLE
Misc Power Supplies
Apple Inc.
DRAWING NUMBER
SIZE
D
REVISION
BRANCH
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED
PAGE
77 OF 132
SHEET
71 OF 105



3.3V Standby FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	5 mA ?(EDP)

3.3V S3 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3 A (EDP)

1.5V S3/S0 FET

MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	6 mOhm @4.5V
LOADING	5 A (EDP)

1.8V GPU FET

MOSFET	NCP4543
CHANNEL	N-TYPE
RDS(ON)	18 mOhm @4.5V
LOADING	2.4A (EDP)

3.3V SUS FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	100? mA (EDP)

5V SUS FET

MOSFET	SiA413
CHANNEL	P-TYPE 12V
RDS(ON)	29 mOhm @4.5V
LOADING	2 mA (EDP)

3.3V S0 FET

MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 mOhm @4.5V
LOADING	5.6 A (EDP)

3.3V S0 GPU FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.11A (EDP)

5.0V S0 FET

MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 MOHM @4.5V
LOADING	8 A (EDP)

SYNC_MASTER=K91_MLB SYNC_DATE=10/18/2010

PAGE TITLE

Power FETs

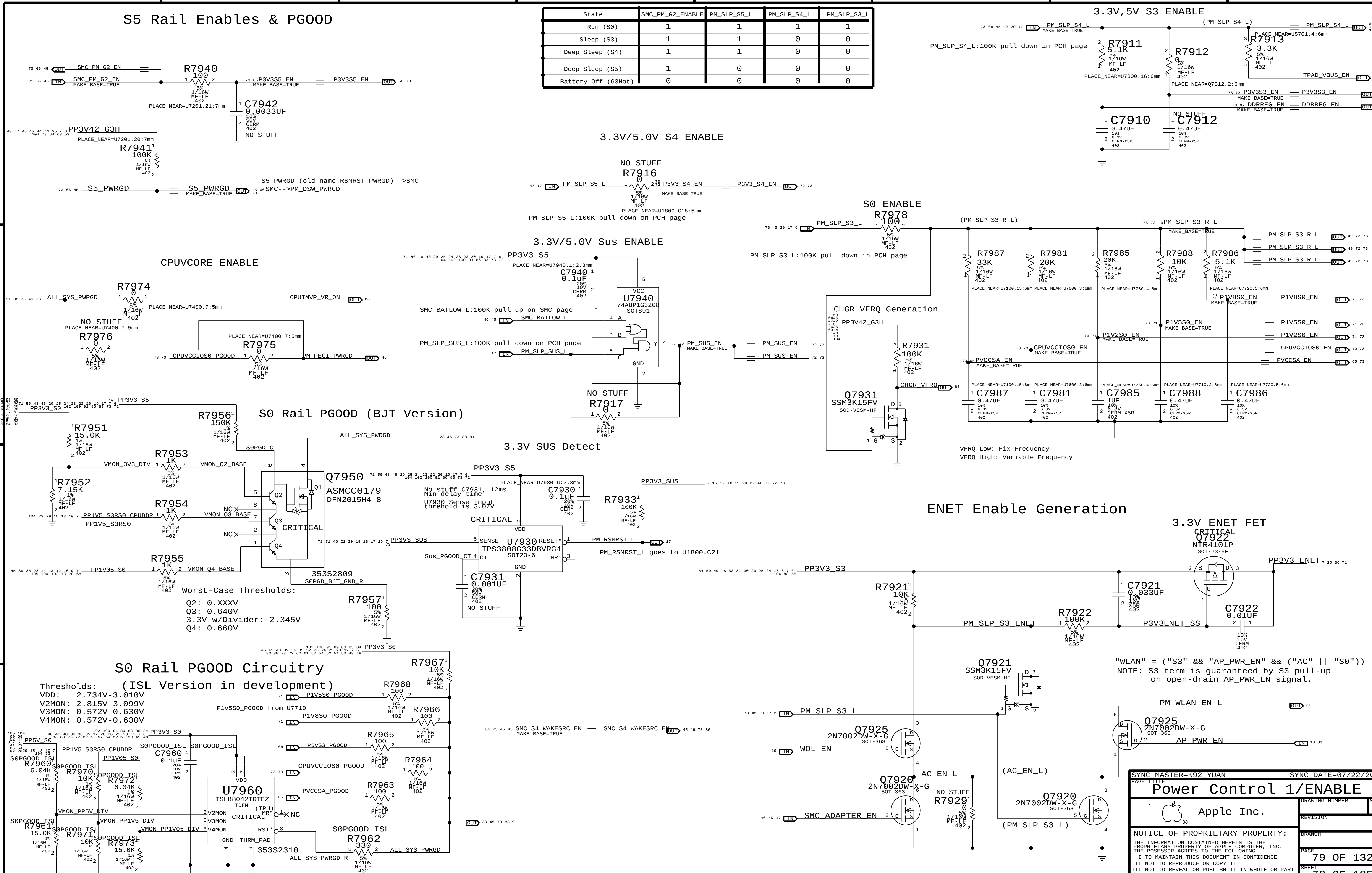
Apple Inc.

DRAWING NUMBER SIZE D

REVISION

BRANCH

State	SMC_PM_G2_ENABLE	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1	1
Sleep (S3)	1	1	0	0
Deep Sleep (S4)	1	1	0	0
Deep Sleep (S5)	1	0	0	0
Battery Off (G3Hot)	0	0	0	0



SYNC_MASTER=K92_YUAN SYNC_DATE=07/22/2010

PAGE TITLE

Power Control 1/ENABLE

Apple Inc.

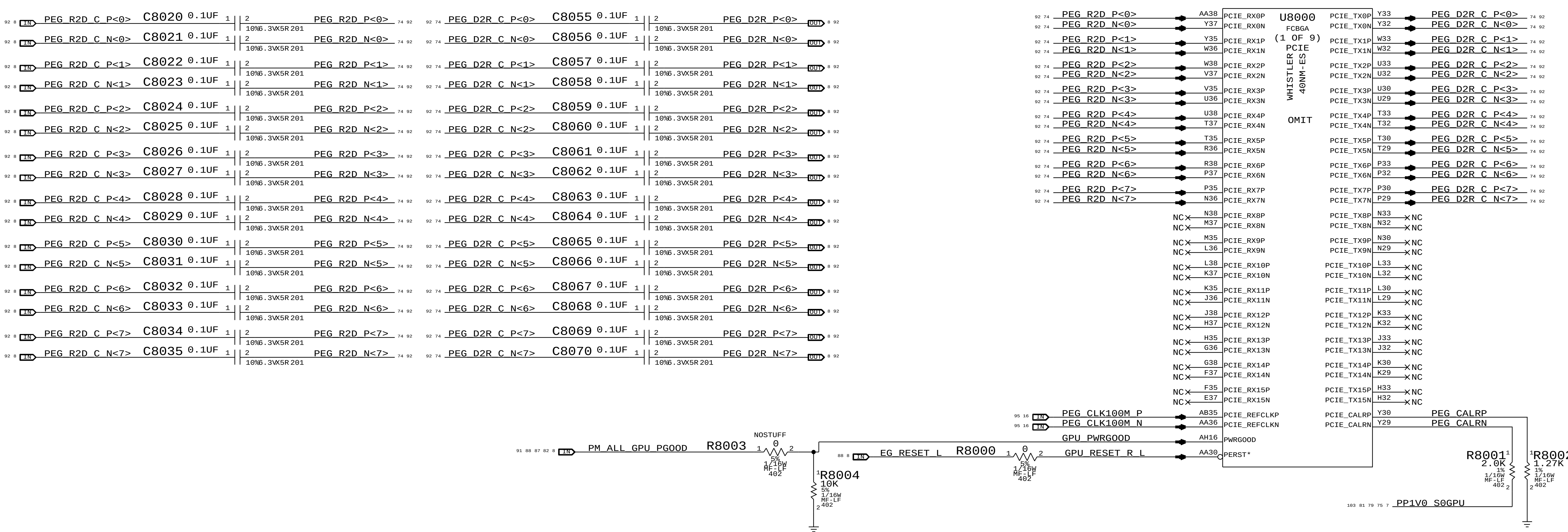
DRAWING NUMBER | SIZE D | REVISION | BRANCH

Page Notes

Power aliases required by this page:
- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



SYNC_MASTER=K91_MLB SYNC_DATE=10/19/2010

PAGE TITLE

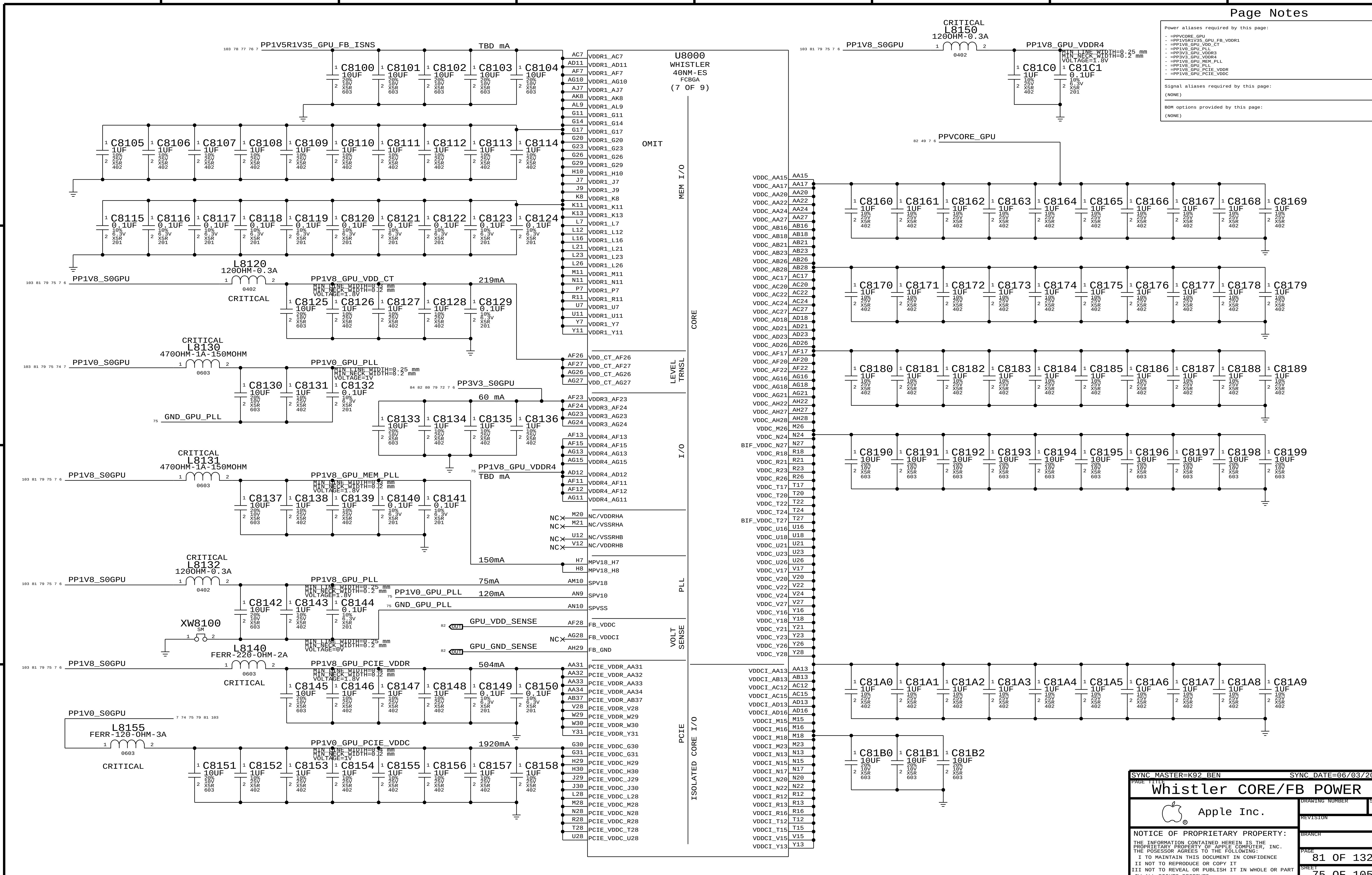
Whistler PCI-E

Apple Inc.

DRAWING NUMBER SIZE D

REVISION

BRANCH



Page Notes

Power aliases required by this page:

- =PPVCORE_GPU
- =PP1V5R1V35_GPU_FB_VDDR1
- =PP1V8_GPU_VDD_CT
- =PP1V0_GPU_PLL
- =PP3V3_GPU_VDDR3
- =PP1V8_GPU_VDDR4
- =PP1V8_GPU_MEM_PLL
- =PP1V8_GPU_PLL
- =PP1V8_GPU_PCIE_VDDR
- =PP1V0_GPU_PCIE_VDDC

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

SYNC_MASTER=K92_BEN SYNC_DATE=06/03/2010

PAGE TITLE

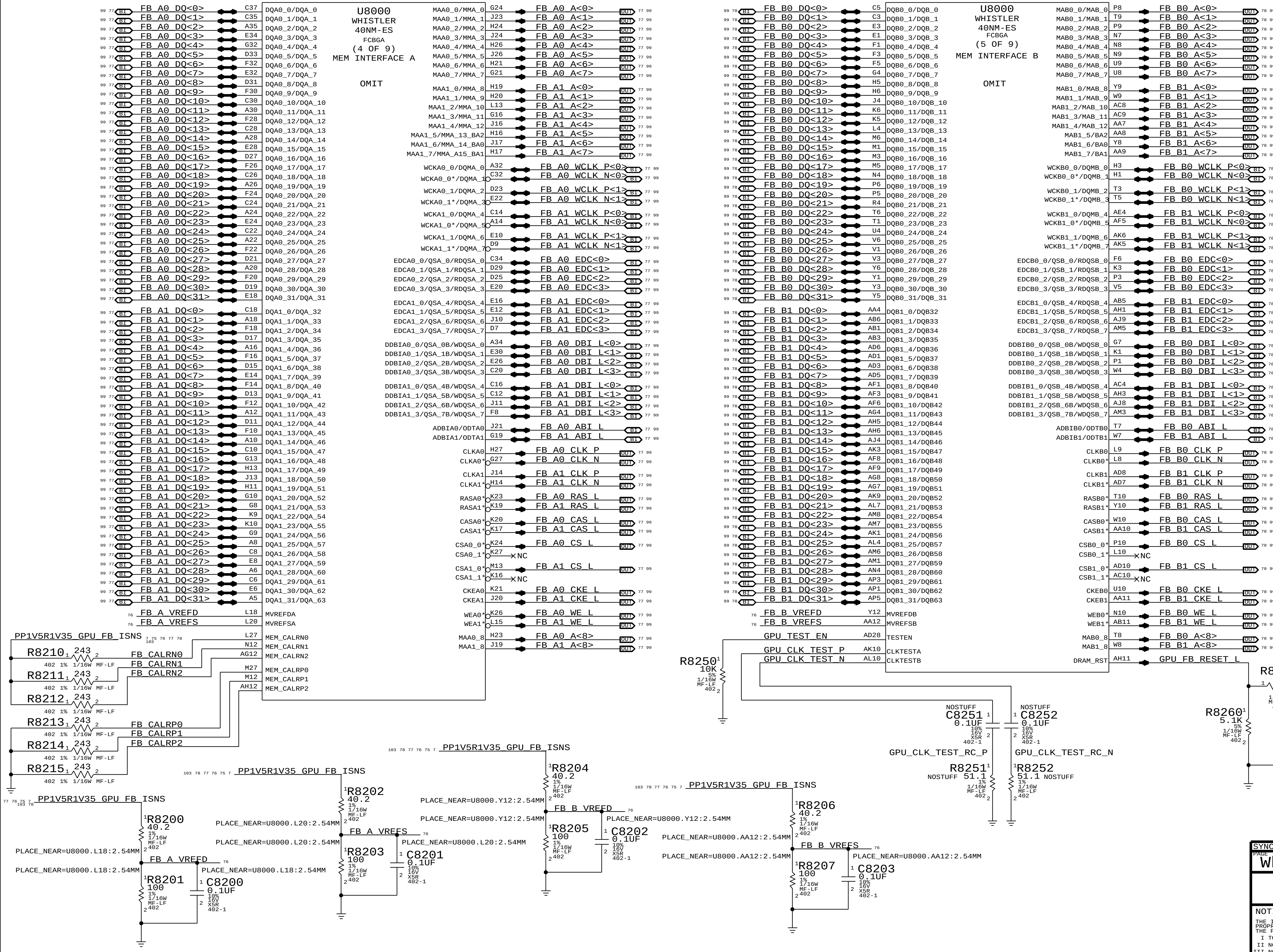
Whistler CORE/FB POWER

Apple Inc.

DRAWING NUMBER SIZE D

REVISION

BRANCH



Page Notes

Power aliases required by this page:
- =PP1V5R1V35_FB_CAL
- =PP1V5R1V35_FB_REF

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE

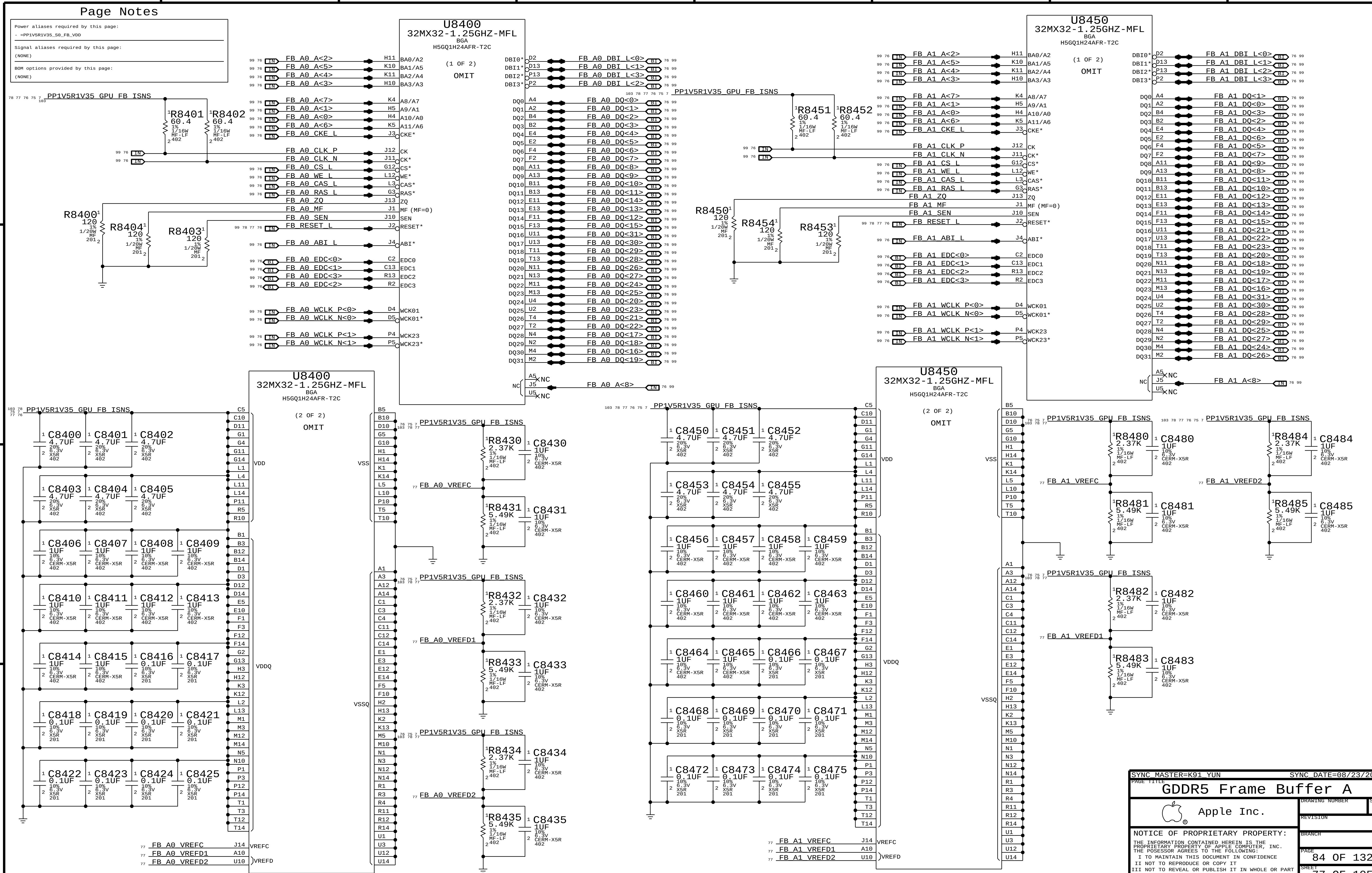
Whistler FRAME BUFFER I/F

Apple Inc.

DRAWING NUMBER | SIZE D

REVISION

BRANCH



SYNC_MASTER=K91_YUN SYNC_DATE=08/23/2010

PAGE TITLE

GDDR5 Frame Buffer A

Apple Inc.

DRAWING NUMBER

SIZE D

REVISION

BRANCH

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:

I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PAGE 84 OF 132

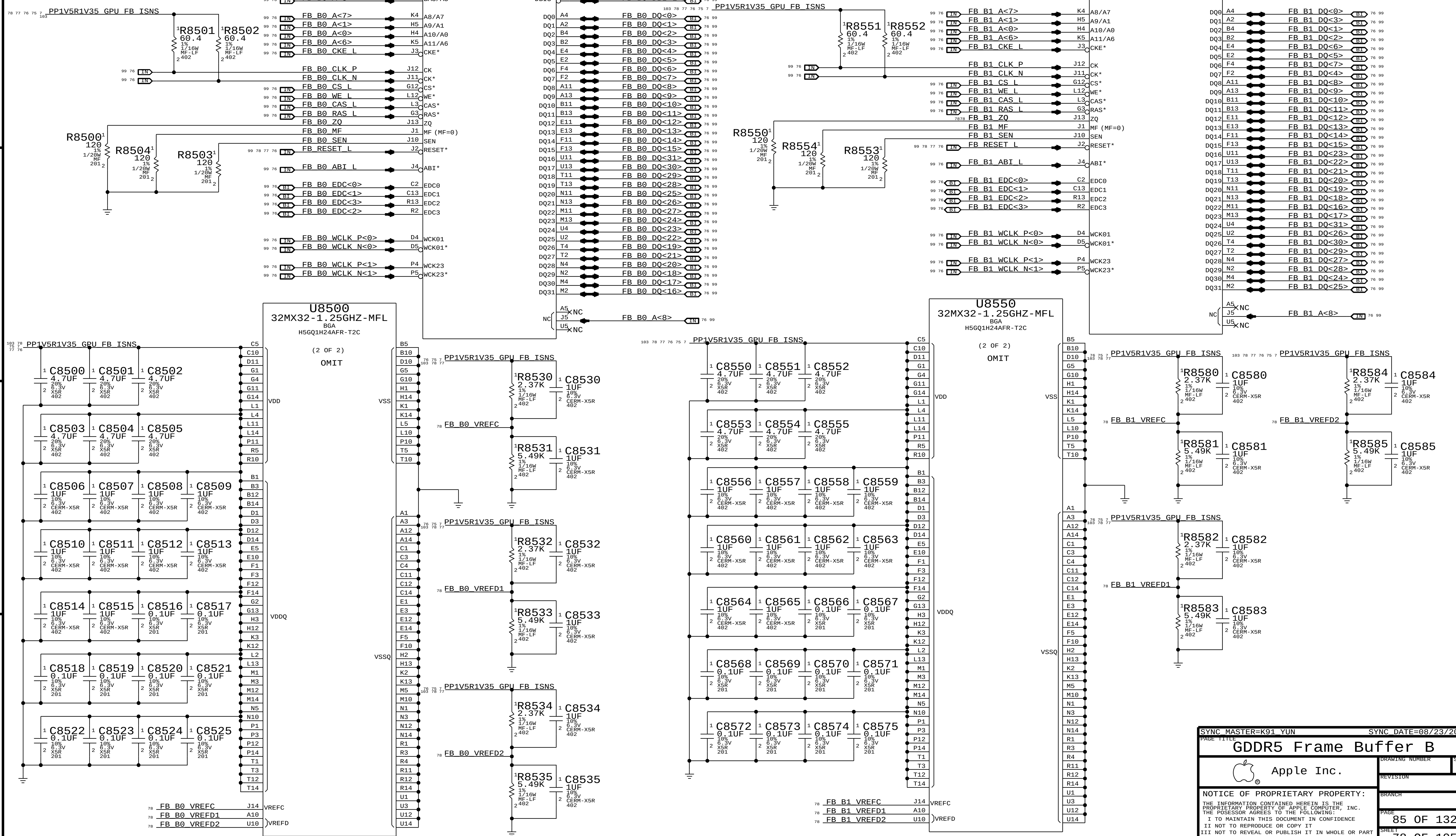
SHEET 77 OF 105

Page Notes

Power aliases required by this page:
- =PP1V5R1V35_S0_FB_VDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



SYNC_MASTER=K91_YUN SYNC_DATE=08/23/2010

PAGE TITLE

GDDR5 Frame Buffer B

Apple Inc.

DRAWING NUMBER

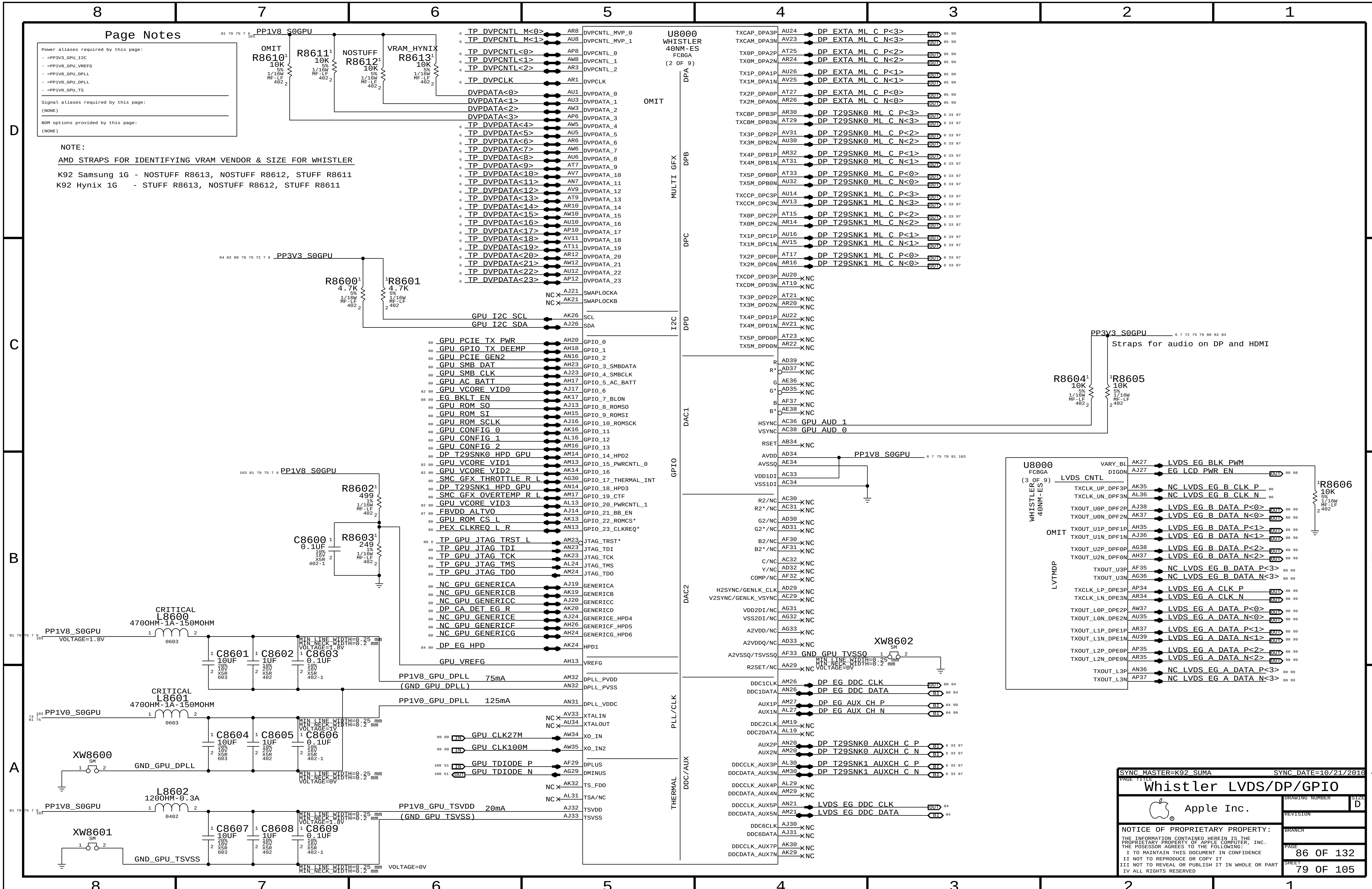
SIZE D

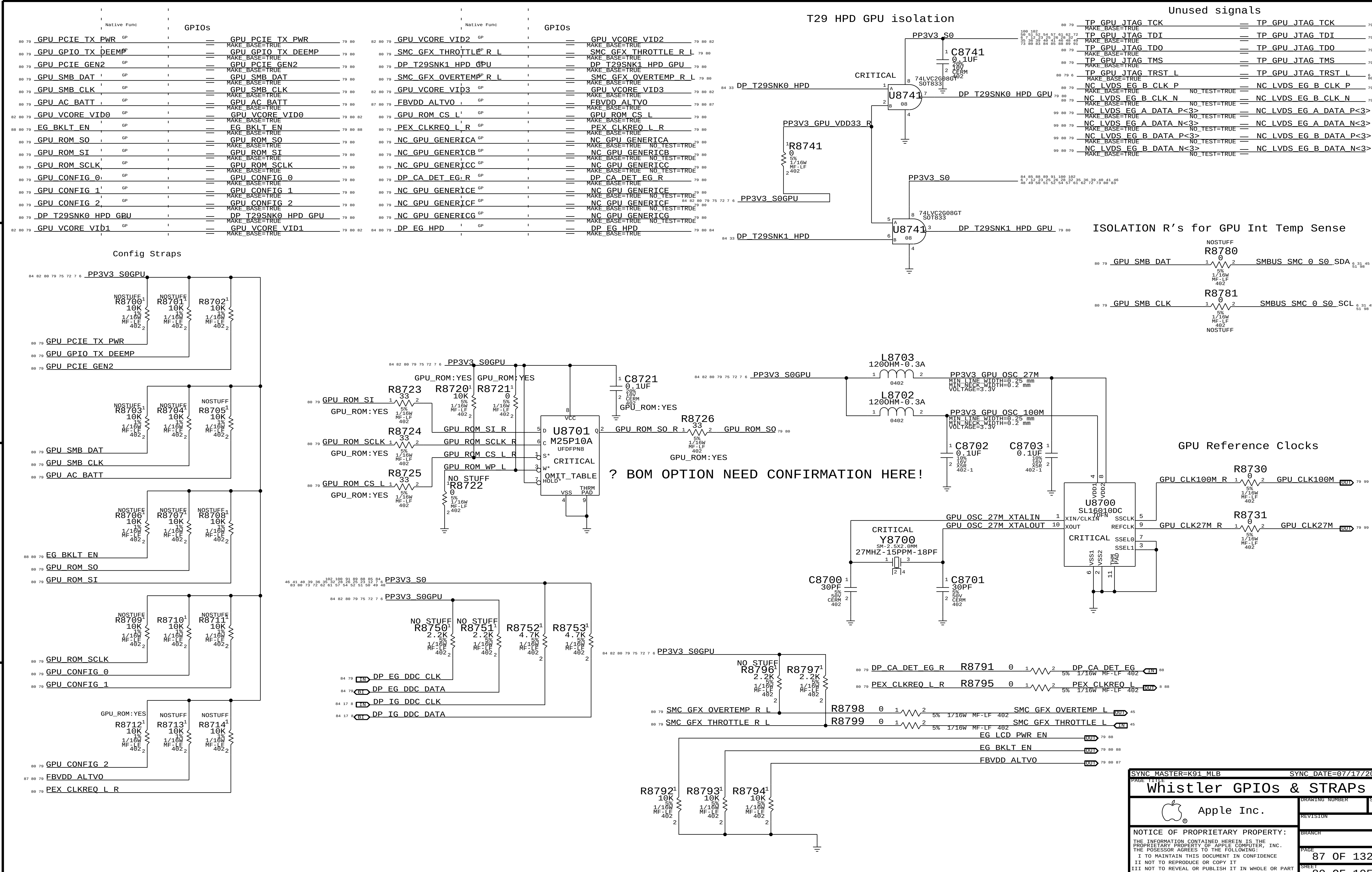
REVISION

BRANCH

PAGE 85 OF 132

SHEET 78 OF 105


Page Notes
Power aliases required by this page:
- =PP3V3_GPU_I2C
- =PP1V8_GPU_VREFG
- =PP1V8_GPU_DPLL
- =PP1V0_GPU_DPLL
- =PP1V8_GPU_TS
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)
NOTE:
AMD STRAPS FOR IDENTIFYING VRAM VENDOR & SIZE FOR WHISTLER
K92 Samsung 1G - NOSTUFF R8613, NOSTUFF R8612, STUFF R8611
K92 Hynix 1G - STUFF R8613, NOSTUFF R8612, STUFF R8611
PP1V8_S0GPU
OMIT
R8610
R8611
NOSTUFF
R8612
VRAM_HYNIX
R8613
10K
U8000
WHISTLER
40NM-ES
FCBGA
(2 OF 9)
OMIT
MULTI GFX
DPA
DPB
DPC
DPD
I2C
DAC1
GPIO
DAC2
PLL/CLK
THERMAL
DDC/AUX
PP3V3_S0GPU
R8600
4.7K
R8601
4.7K
GPU_I2C_SCL
GPU_I2C_SDA
GPU_PCIE_TX_PWR
GPU_GPIO_TX_DEEMP
GPU_PCIE_GEN2
GPU_SMB_DAT
GPU_SMB_CLK
GPU_AC_BATT
GPU_VCORE_VID0
EG_BKLT_EN
GPU_ROM_SO
GPU_ROM_SI
GPU_ROM_SCLK
GPU_CONFIG_0
GPU_CONFIG_1
GPU_CONFIG_2
DP_T29SNK0_HPD_GPU
GPU_VCORE_VID1
GPU_VCORE_VID2
SMC_GFX_THROTTLE_R_L
DP_T29SNK1_HPD_GPU
SMC_GFX_OVERTEMP_R_L
GPU_VCORE_VID3
FBVDD_ALTVO
GPU_ROM_CS_L
PEX_CLKREQ_L_R
TP_GPU_JTAG_TRST_L
TP_GPU_JTAG_TDI
TP_GPU_JTAG_TCK
TP_GPU_JTAG_TMS
TP_GPU_JTAG_TDO
DP_EG_HPD
GPU_VREFG
R8602
499
C8600
0.1UF
R8603
249
CRITICAL
L8600
470OHM-1A-150MOHM
C8601 10UF
C8602 1UF
C8603 0.1UF
PP1V8_GPU_DPLL 75mA
(GND_GPU_DPLL)
L8601
PP1V0_S0GPU
C8604 10UF
C8605 1UF
C8606 0.1UF
PP1V0_GPU_DPLL 125mA
XW8600
GND_GPU_DPLL
L8602
120OHM-0.3A
C8607 10UF
C8608 1UF
C8609 0.1UF
PP1V8_GPU_TSVDD 20mA
(GND_GPU_TSVSS)
XW8601
GND_GPU_TSVSS
GPU_CLK27M
GPU_CLK100M
GPU_TDIODE_P
GPU_TDIODE_N
DP_EXTA_ML_C_P<3>
DP_T29SNK0_ML_C_P<3>
DP_T29SNK1_ML_C_P<3>
PP3V3_S0GPU
Straps for audio on DP and HDMI
R8604 10K
R8605 10K
GPU_AUD_1
GPU_AUD_0
PP1V8_S0GPU
XW8602
GND_GPU_TVSSQ
DP_EG_DDC_CLK
DP_EG_DDC_DATA
DP_EG_AUX_CH_P
DP_EG_AUX_CH_N
DP_T29SNK0_AUXCH_C_P
DP_T29SNK0_AUXCH_C_N
DP_T29SNK1_AUXCH_C_P
DP_T29SNK1_AUXCH_C_N
LVDS_EG_DDC_CLK
LVDS_EG_DDC_DATA
U8000
FCBGA
(3 OF 9)
WHISTLER 40NM-ES
OMIT
LVTMDP
LVDS_CNTL
LVDS_EG_BLK_PWM
EG_LCD_PWR_EN
R8606 10K
LVDS_EG_B_DATA_P<0>
LVDS_EG_A_CLK_P
LVDS_EG_A_DATA_P<0>
SYNC_MASTER=K92_SUMA
SYNC_DATE=10/21/2010
PAGE TITLE
Whistler LVDS/DP/GPIO
Apple Inc.
DRAWING NUMBER
SIZE D
REVISION
BRANCH
PAGE 86 OF 132
SHEET 79 OF 105
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=K91_MLB SYNC_DATE=07/17/2010

PAGE TITLE

Whistler GPIOs & STRAPs

Apple Inc.

DRAWING NUMBER | SIZE D

REVISION

BRANCH

NOTICE OF PROPRIETARY PROPERTY:

Page Notes

Power aliases required by this page:
- =PP1V8_GPU_DP_AB
- =PP1V8_GPU_DP_CD
- =PP1V8_GPU_DP_EF
- =PP1V0_GPU_DP_AB
- =PP1V0_GPU_DP_CD
- =PP1V0_GPU_DP_EF

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

SYNC_MASTER=K92_BEN SYNC_DATE=06/01/2010

PAGE TITLE

Whistler DP PWR/GNDs

Apple Inc.

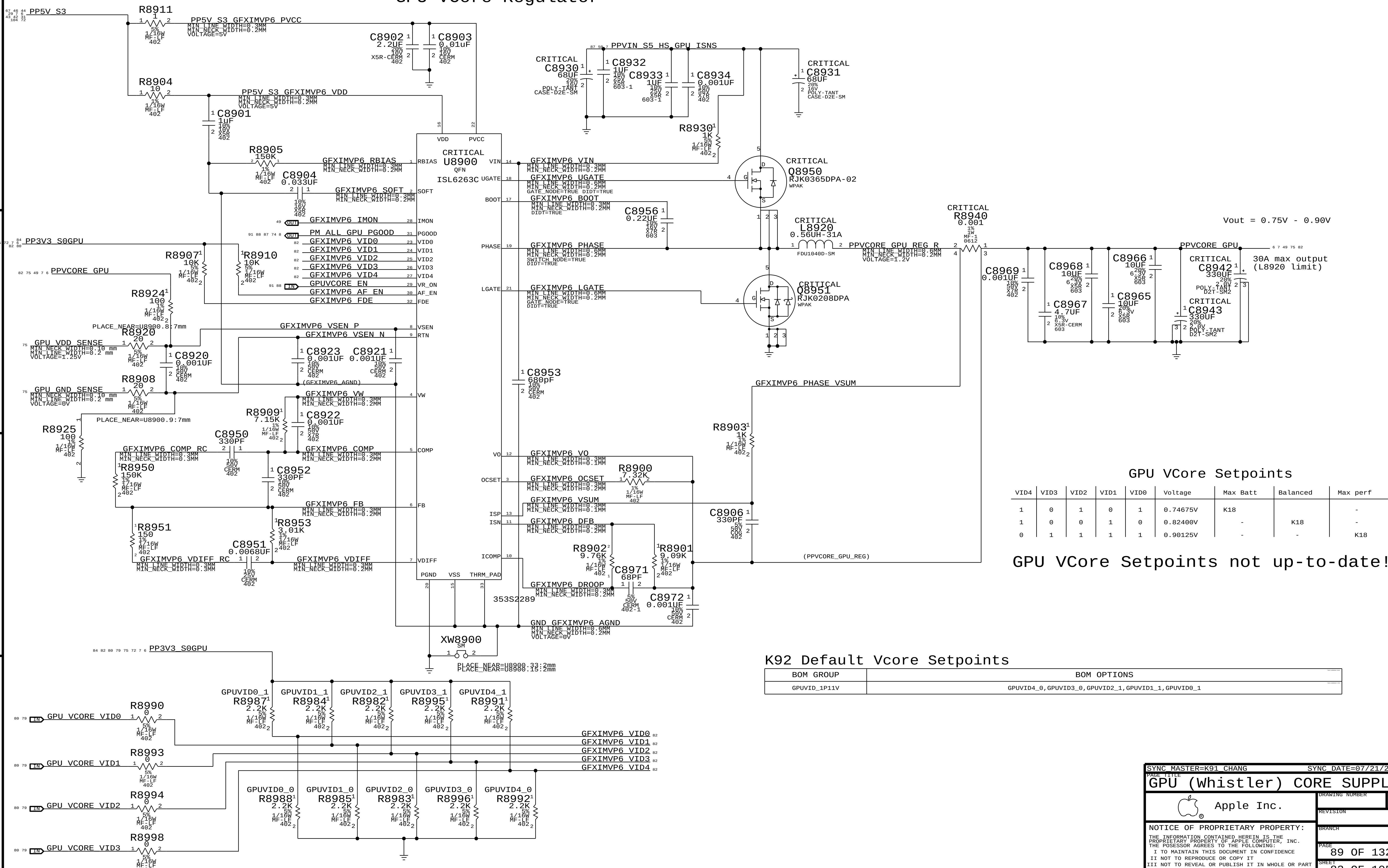
DRAWING NUMBER

SIZE D

REVISION

BRANCH

GPU VCore Regulator



GPU VCore Setpoints

VID4	VID3	VID2	VID1	VID0	Voltage	Max Batt	Balanced	Max perf
1	0	1	0	1	0.74675V	K18		-
1	0	0	1	0	0.82400V	-	K18	-
0	1	1	1	1	0.90125V	-	-	K18

GPU VCore Setpoints not up-to-date!

K92 Default Vcore Setpoints

BOM GROUP	BOM OPTIONS
GPUVID_1P11V	GPUVID4_0,GPUVID3_0,GPUVID2_1,GPUVID1_1,GPUVID0_1

SYNC_MASTER=K91_CHANG SYNC_DATE=07/21/2010

PAGE TITLE

GPU (Whistler) CORE SUPPLY

Apple Inc.

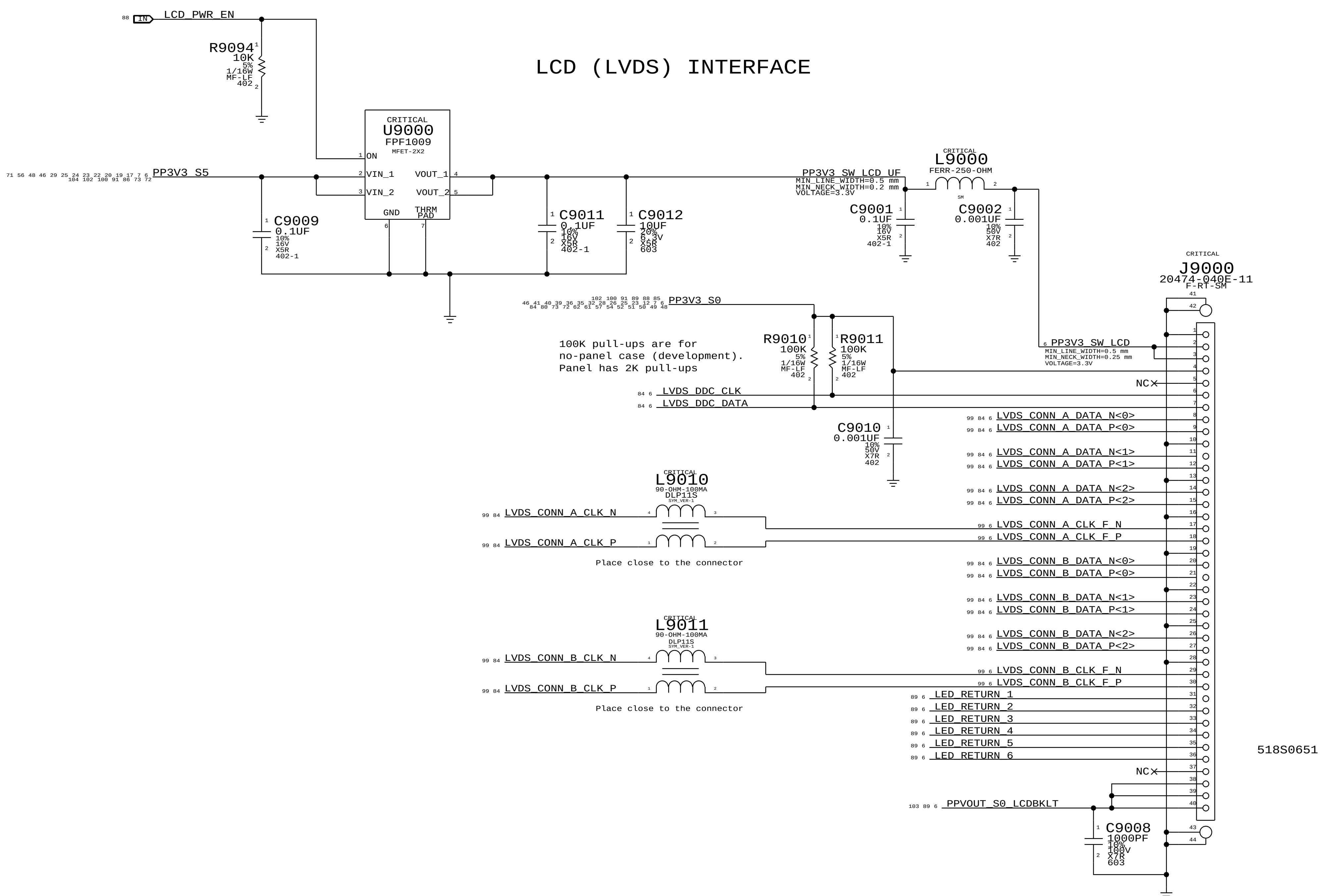
DRAWING NUMBER

SIZE D

REVISION

BRANCH

LCD (LVDS) INTERFACE



SYNC_MASTER=K17_MLB SYNC_DATE=04/26/2010

PAGE TITLE

LVDS Display Connector

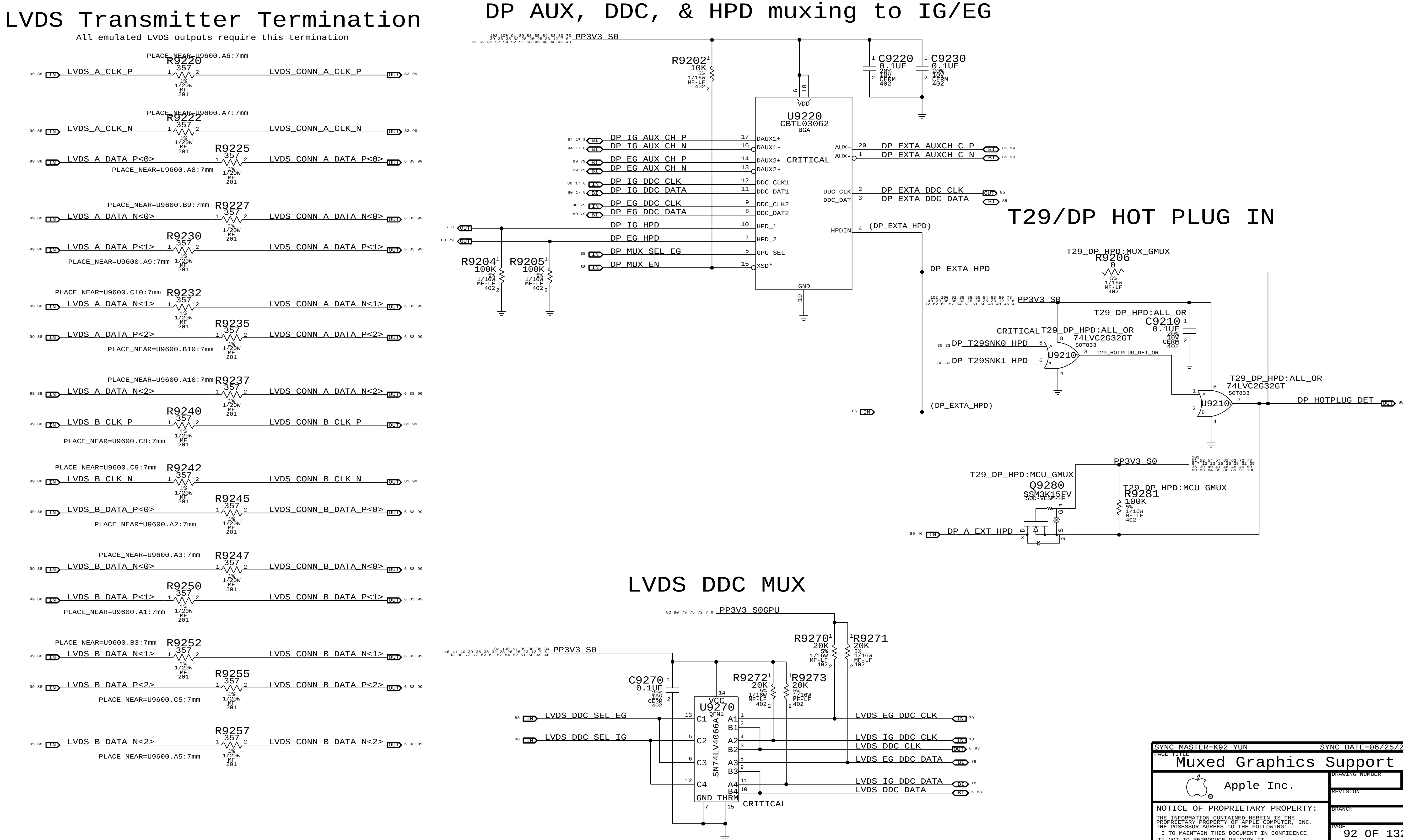
Apple Inc.

DRAWING NUMBER

SIZE D

REVISION

BRANCH



SYNC_MASTER=K92_YUN SYNC_DATE=06/25/2010

PAGE TITLE

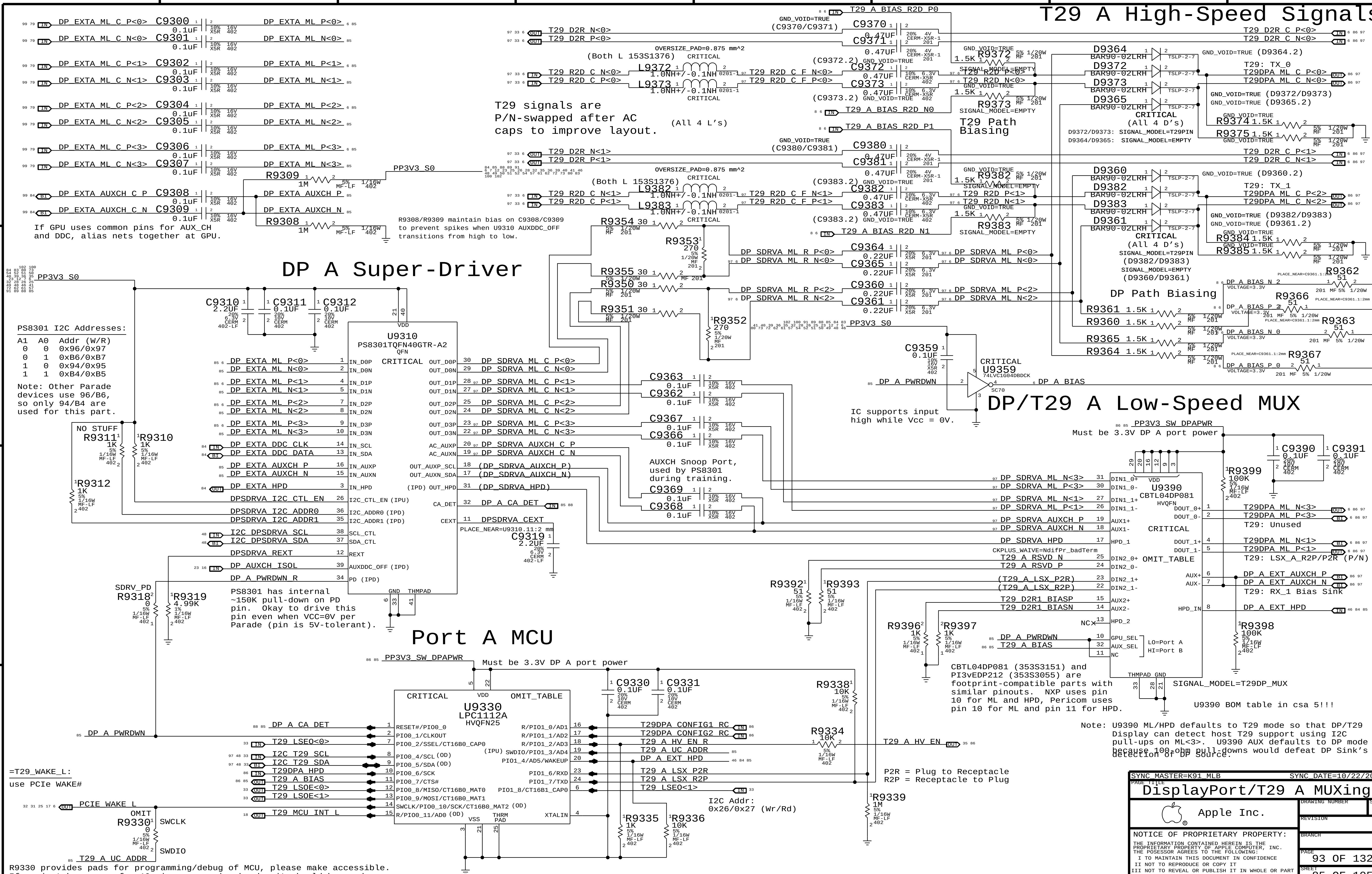
Muxed Graphics Support

Apple Inc.

DRAWING NUMBER SIZE D

REVISION

BRANCH

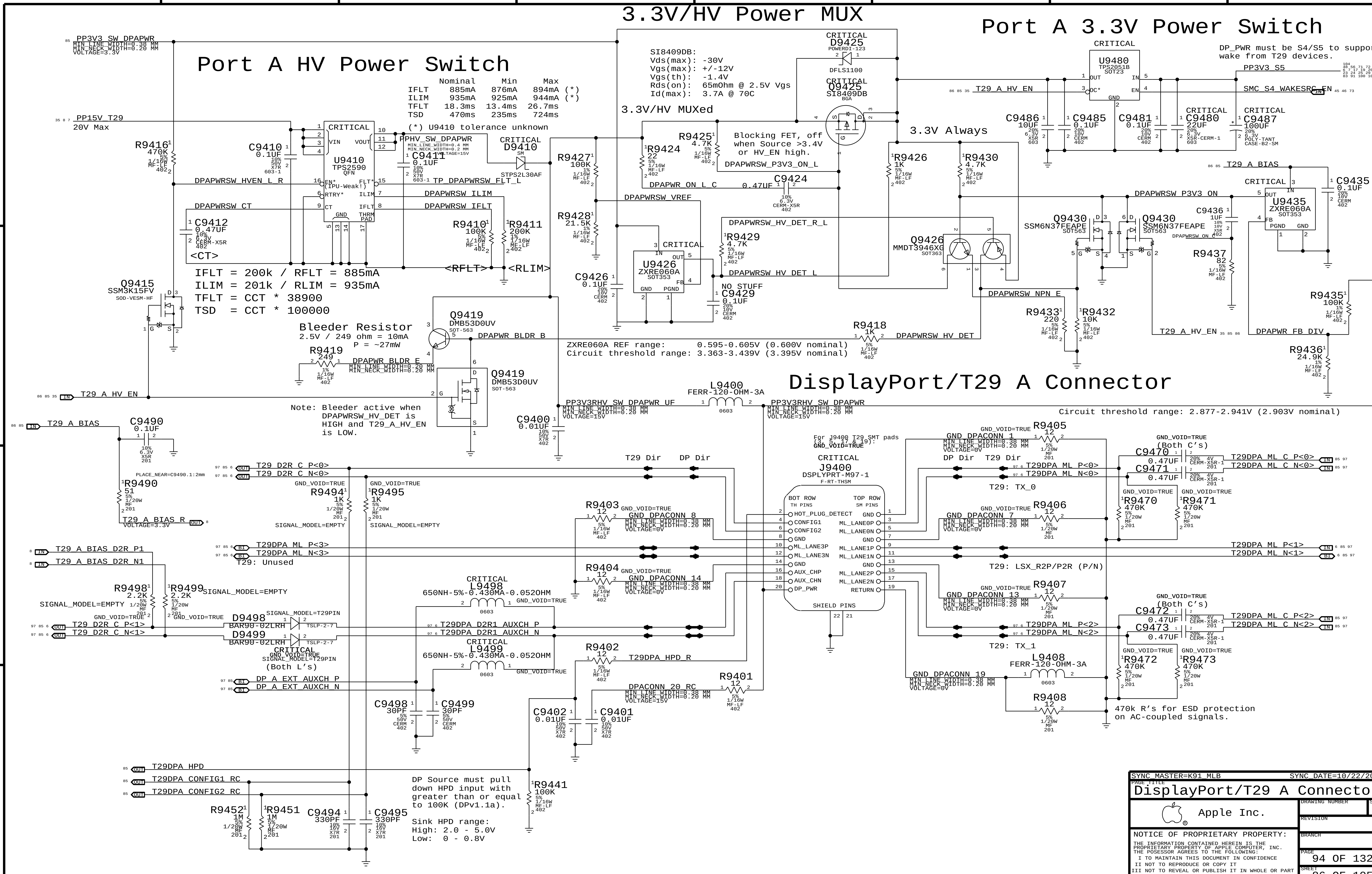


SYNC_MASTER=K91_MLB SYNC_DATE=10/22/2010

DisplayPort/T29 A MUXing

Apple Inc.

SIZE D



SYNC_MASTER=K91_MLB SYNC_DATE=10/22/2010

PAGE TITLE

DisplayPort/T29 A Connector

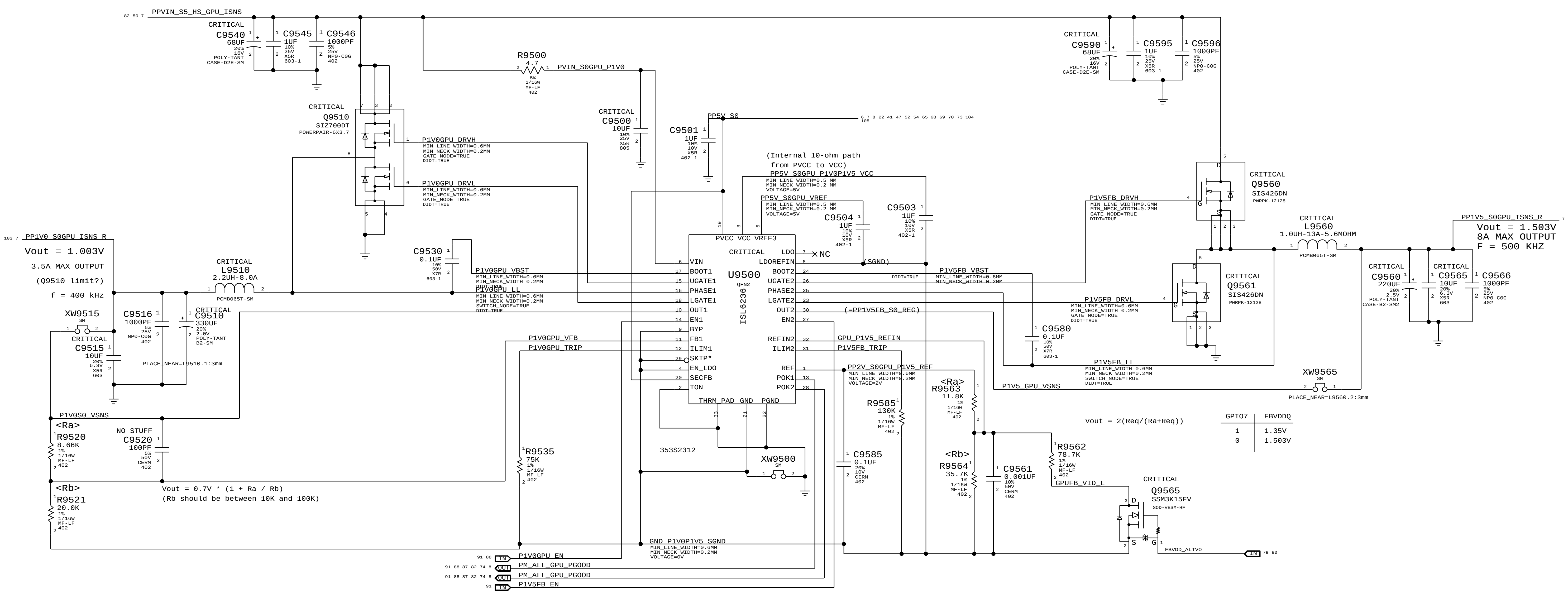
Apple Inc.

DRAWING NUMBER

SIZE D

REVISION

BRANCH



SYNC_MASTER=K91_CHANG SYNC_DATE=07/21/2010

PAGE TITLE

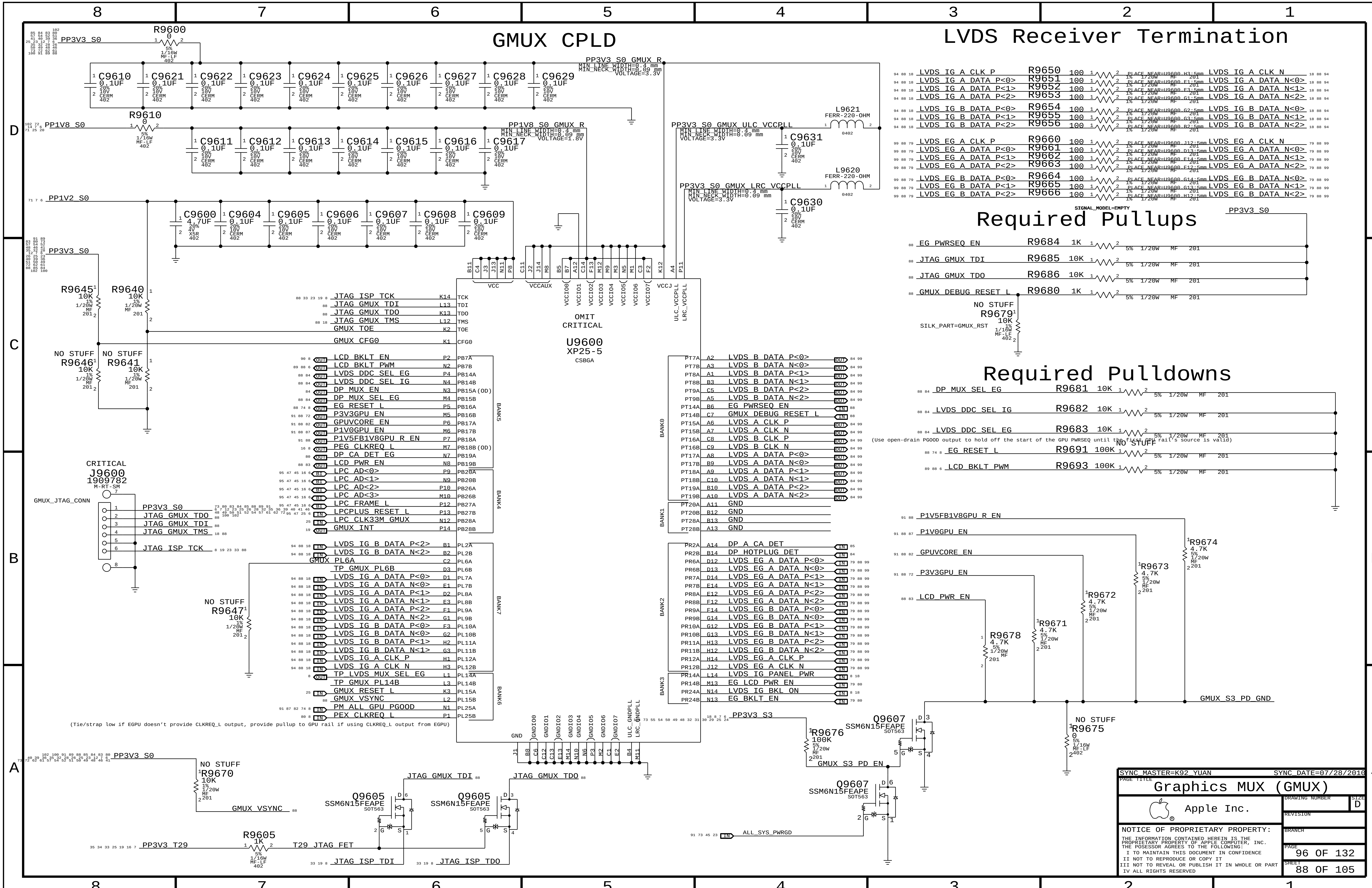
1V0 GPU / 1V5 FB Power Supply

Apple Inc.

DRAWING NUMBER SIZE D

REVISION

BRANCH



SYNC_MASTER=K92_YUAN SYNC_DATE=07/28/2010

PAGE TITLE

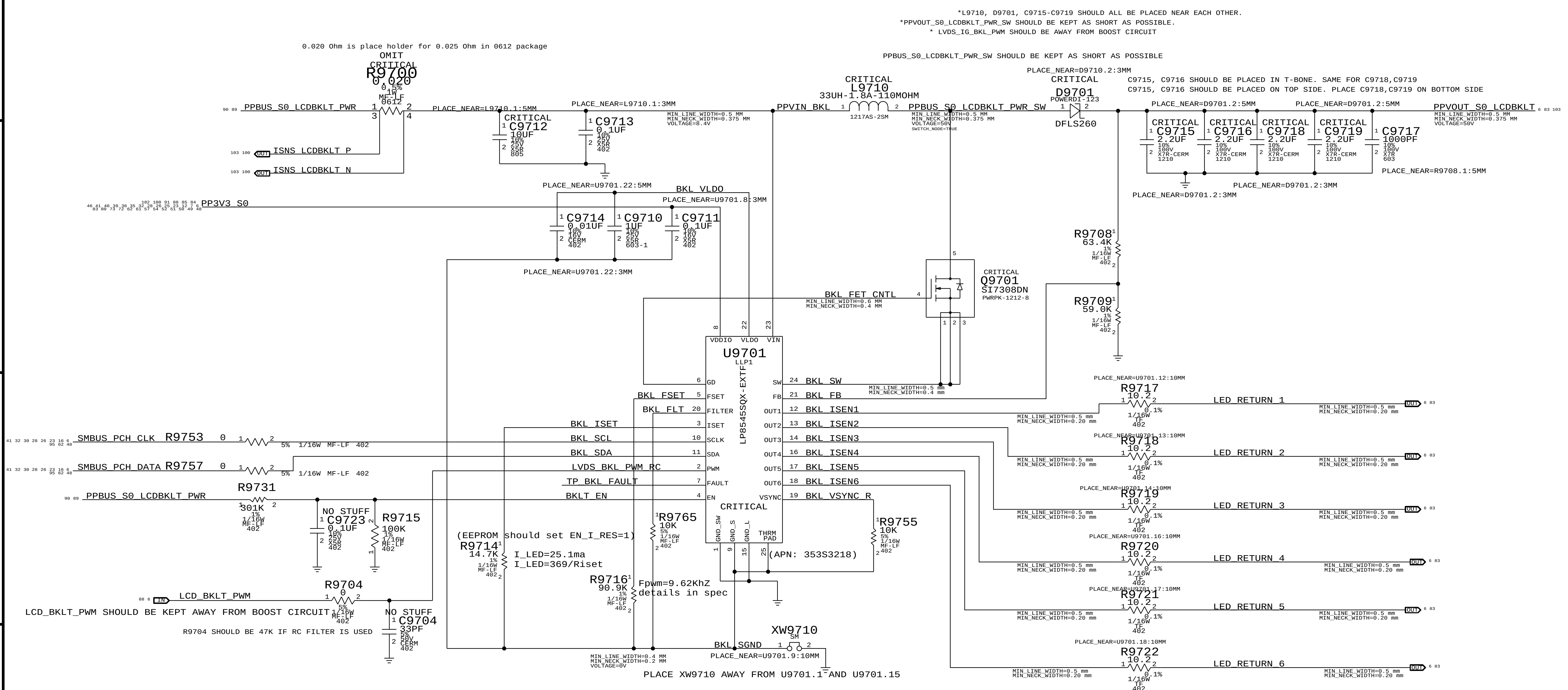
Graphics MUX (GMUX)

Apple Inc.

DRAWING NUMBER SIZE D

REVISION

BRANCH



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
107S0196	1	0.025OHM,1W,0612,MTL FILM RES	R9700	CRITICAL	

SYNC_MASTER=K92_DINESH SYNC_DATE=09/07/2010

PAGE TITLE

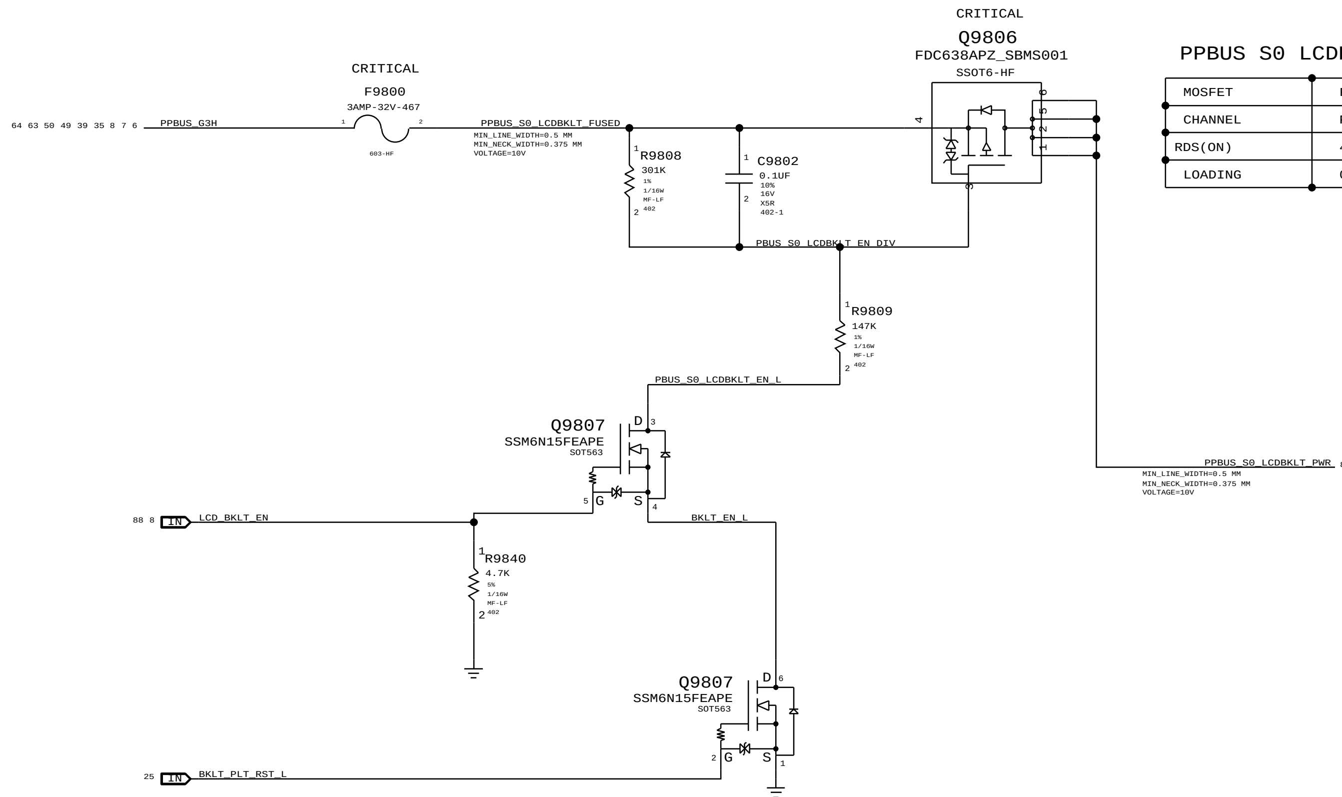
LCD Backlight Driver (LP8545)

Apple Inc.

DRAWING NUMBER SIZE D

REVISION

BRANCH



PPBUS S0 LCDBkLT FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.4 A (EDP)

SYNC_MASTER=K17_MLB SYNC_DATE=04/26/2010

PAGE TITLE

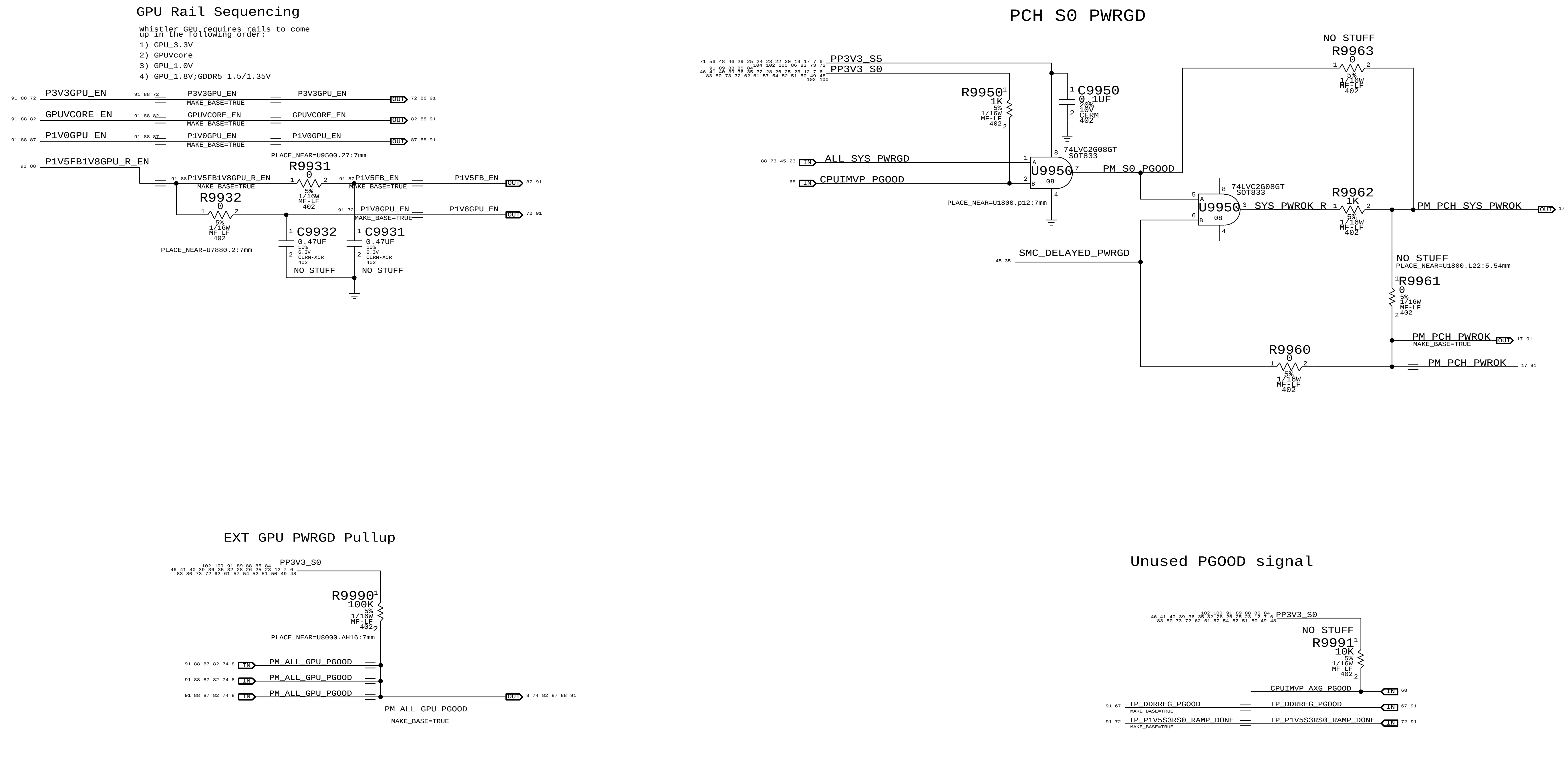
LCD Backlight Support

DRAWING NUMBER SIZE D

Apple Inc.

REVISION

BRANCH



SYNC_MASTER=K92_YUAN SYNC_DATE=07/30/2010

PAGE TITLE

Power Sequencing EG/PCH S0

Apple Inc.

DRAWING NUMBER

SIZE D

REVISION

BRANCH

8	7	6	5	4	3	2	1

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_VID	*	0.457 MM	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Calpella SFF DG (DG-407364_v1.5), Section 2.8

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

CPU Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	DMI_S2N	PCIE_85D	PCIE	DMI_S2N_P<3:0>	6 9 17
	DMI_S2N	PCIE_85D	PCIE	DMI_S2N_N<3:0>	6 9 17
	DMI_N2S	PCIE_85D	PCIE	DMI_N2S_P<3:0>	6 9 17
	DMI_N2S	PCIE_85D	PCIE	DMI_N2S_N<3:0>	6 9 17
	FDI_DATA	PCIE_85D	PCIE	FDI_DATA_P<7:0>	9 17
	FDI_DATA	PCIE_85D	PCIE	FDI_DATA_N<7:0>	9 17
		CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	9 17
		CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	9 17
I125	DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_P	10 16
I126		CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_N	10 16
		CPU_50S	CPU_AGTL	FDI_INT	9 17
	CPU_PECI	CPU_50S	PCIE	CPU_PECI	10 19 45
	PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC	10 17
	PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM_MEM_PWRGD	10 17 29
	XDP_CPU_PWRGOOD	CPU_50S	CPU_ITP	XDP_CPU_PWRGD	23
	XDP_BDRESET_L	CPU_50S	CPU_ITP	XDP_DBRESET_L	10 23 25
	XDP_PRDY_L	CPU_50S	CPU_ITP	XDP_CPU_PRDY_L	10 23
	XDP_PREQ_l	CPU_50S	CPU_ITP	XDP_CPU_PREQ_L	10 23
	CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP0	
	CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP1	
	CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP2	
	CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<11..0>	9 23
I124	CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<17..16>	9 23
	CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU_CATERR_L	10
I115		CPU_50S	CPU_AGTL	CPU_PROC_SEL_L	10 17
		CPU_50S	CPU_AGTL	TP_CPU_VTT_SELECT	8
	CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 46 68
	CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 19 23
	PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	10 19
	XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_P	10 16
	XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_N	10 16
	XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_P	16 23
	XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_N	16 23
	XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_P	23
	XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_N	23
		CPU_55S	CPU_8MIL	CPU_PSI_L	
	PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	
		CPU_27P4S	CPU_COMP	CPU_PEG_COMP	9
		CPU_27P4S	CPU_COMP	CPU_PEG_RBIAS	
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP3	
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP2	
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP1	
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP0	
	XDP_TDI	CPU_50S	CPU_ITP	XDP_CPU_TDI	10 23
	XDP_TDO	CPU_50S	CPU_ITP	XDP_CPU_TDO	10 23
	XDP_TMS	CPU_50S	CPU_ITP	XDP_CPU_TMS	10 23
	XDP_TCK	CPU_50S	CPU_ITP	XDP_CPU_TCK	10 23
	XDP_TRST_L	CPU_50S	CPU_ITP	XDP_CPU_TRST_L	10 23
	XDP_BPM	CPU_50S	CPU_ITP	XDP_BPM_L<3..0>	10 23
	XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<7..4>	10 23
	(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	23
		CPU_55S	CPU_8MIL	CPU_VID<6..0>	8
		CPU_50S	CPU_AGTL	CPUIMVP_IMON	
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	12 68
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	12 68
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_P	12 70
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_N	12 70
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_P	12 68
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_N	12 68
I120		CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	12
I121		CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	12
I122		CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	12
I123		CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	12
		CPU_55S	CPU_8MIL	GFX_VID<6..0>	8
	PM_DPRSLPVR	CPU_50S	CPU_AGTL	GFX_DPRSLPVR	
		CPU_50S	CPU_AGTL	GFX_VR_EN	
		CPU_50S	CPU_AGTL	GFXIMVP_IMON	
		PCIE_85D	PCIE	PEG_R2D_P<7..0>	74
		PCIE_85D	PCIE	PEG_R2D_N<7..0>	74
	PEG_R2D	PCIE_85D	PCIE	PEG_R2D_C_P<7..0>	8 74
		PCIE_85D	PCIE	PEG_R2D_C_N<7..0>	8 74
	PEG_D2R	PCIE_85D	PCIE	PEG_D2R_P<7..0>	8 74
		PCIE_85D	PCIE	PEG_D2R_N<7..0>	8 74
		PCIE_85D	PCIE	PEG_D2R_C_P<7..0>	74
		PCIE_85D	PCIE	PEG_D2R_C_N<7..0>	74
		CPU_50S	CPU_VID	CPU_VIDSOUT	12 68
		CPU_50S	CPU_VID	CPU_VIDSCLK	12 68
		CPU_50S	CPU_VID	CPU_VIDALERT_L	12 68

D C B A

SYNC_MASTER=K91_MLB SYNC_DATE=07/22/2010

PAGE TITLE

CPU Constraints

Apple Inc.

DRAWING NUMBER

SIZE D

REVISION

BRANCH

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=3:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MILS	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR3:
DQ/DM signals should be matched within 0.508mm of associated DQS pair.
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-12.7mm] and [CLK+25.4mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-12.7mm] to [CLK+0.0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to SODIMM pad is 139.7mm, from procesor ball to SODIMM pad is 114.3mm.

SOURCE: Calpella SFF Platform DG, Rev 1.5 (#407364), Section 2.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_P<5..0>	11 26
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_N<5..0>	11 26
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CKE<3..0>	11 26
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CS_L<3..0>	11 26
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_ODT<3..0>	11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0>	11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0>	11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L	11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L	11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L	11 26
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_A_DQ<7..0>	11 27
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_A_DQ<15..8>	11 27
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_A_DQ<23..16>	11 27
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_A_DQ<31..24>	11 27
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_A_DQ<39..32>	11 26 27
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_A_DQ<47..40>	11 27
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_A_DQ<55..48>	11 27
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_A_DQ<63..56>	11 27
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0>	11 27
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_N<0>	11 26 27
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1>	11 27
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_N<1>	11 27
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2>	11 27
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_N<2>	11 27
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3>	11 27
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_N<3>	11 27
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4>	11 27
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_N<4>	11 27
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5>	11 27
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_N<5>	11 27
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6>	11 27
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_N<6>	11 27
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7>	11 27
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_N<7>	11 27
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_P<5..0>	11 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_N<5..0>	11 28
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CKE<3..0>	11 28
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CS_L<3..0>	11 28
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_ODT<3..0>	11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0>	11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0>	11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L	11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L	11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L	11 28
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_B_DQ<7..0>	11 27
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_B_DQ<15..8>	11 27
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_B_DQ<23..16>	11 27
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_B_DQ<31..24>	11 27
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_B_DQ<39..32>	11 27 28
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_B_DQ<47..40>	11 27
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_B_DQ<55..48>	11 27
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_B_DQ<63..56>	11 27
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0>	11 27 28
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_N<0>	11 27 28
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1>	11 27
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_N<1>	11 27
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2>	11 27
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_N<2>	11 27
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3>	11 27
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_N<3>	11 27
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4>	11 27
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_N<4>	11 27
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5>	11 27
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_N<5>	11 27
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6>	11 27
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_N<6>	11 27
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7>	11 27
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_N<7>	11 27

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
LVDS_85D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	ISL3,ISL4,ISL9,ISL10	=4:1_SPACING	?
LVDS	ISL3,ISL4,ISL9,ISL10	=4:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4:1_SPACING	?
LVDS	TOP,BOTTOM	=4:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
SATA_37SE	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE
SATA_50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	ISL3,ISL4,ISL9,ISL10	=5:1_SPACING	?
SATA_ICOMP	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=5:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	ISL3,ISL4,ISL9,ISL10	=4:1_SPACING	?
USB_RBIAS	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_P	8 17 84
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_N	8 17 84
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_P	18 88
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_N	18 88
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_P<2..0>	18 88
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_N<2..0>	18 88
LVDS_IG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_A_DATAP<3>	8 18
LVDS_IG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_A_DATAN<3>	8 18
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_P<2..0>	18 88
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_N<2..0>	18 88
DP_SATA_G3_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_P	6 16 41
	SATA_90D	SATA	SATA_HDD_R2D_C_N	6 16 41
SATA_HDD_RDVR_R2D	SATA_90D	SATA	SATA_HDD_R2D_P	6 41
	SATA_90D	SATA	SATA_HDD_R2D_N	6 41
DP_SATA_G3_R2D	SATA_90D	SATA	SATA_HDD_R2D_UF_P	6 41
	SATA_90D	SATA	SATA_HDD_R2D_UF_N	6 41
DP_SATA_G3_R2D	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_OUT_P	6 41
	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_OUT_N	6 41
DP_SATA_G3_R2D	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_IN_P	6 41
	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_IN_N	6 41
DP_SATA_G3_R2D	SATA_90D	SATA	SATA_HDD_R2D_RC_UF_P	6 41
	SATA_90D	SATA	SATA_HDD_R2D_RC_UF_N	6 41
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_P	6 16 41
	SATA_90D	SATA	SATA_HDD_D2R_N	6 16 41
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_OUT_P	6 41
	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_OUT_N	6 41
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_IN_P	6 41
	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_IN_N	6 41
SATA_HDD_RDVR_D2R	SATA_90D	SATA	SATA_HDD_D2R_C_P	6 41
	SATA_90D	SATA	SATA_HDD_D2R_C_N	6 41
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_C_P	16 41
	SATA_90D	SATA	SATA_ODD_R2D_C_N	16 41
	SATA_90D	SATA	SATA_ODD_R2D_P	6 41
	SATA_90D	SATA	SATA_ODD_R2D_N	6 41
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_UF_P	41
	SATA_90D	SATA	SATA_ODD_R2D_UF_N	41
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_P	16 41
	SATA_90D	SATA	SATA_ODD_D2R_N	16 41
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_C_P	41
	SATA_90D	SATA	SATA_ODD_D2R_C_N	41
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_UF_P	6 41
	SATA_90D	SATA	SATA_ODD_D2R_UF_N	6 41
PCH_SATA3_ICOMP	SATA_50SE	SATA_ICOMP	PCH_SATA3COMP	16
PCH_SATA_ICOMP	SATA_37SE	SATA_ICOMP	PCH_SATAICOMP	16
USB_HUB1_UP	USB_85D	USB	USB_HUB1_UP_P	18 24
	USB_85D	USB	USB_HUB1_UP_N	18 24
USB_HUB2_UP	USB_85D	USB	USB_HUB2_UP_P	18 24
	USB_85D	USB	USB_HUB2_UP_N	18 24
USB_EXTA	USB_85D	USB	USB_EXTA_P	24 42
	USB_85D	USB	USB_EXTA_N	24 42
USB_EXTB	USB_85D	USB	USB_EXTB_P	24 42
	USB_85D	USB	USB_EXTB_N	24 42
USB_EXTC	USB_85D	USB	USB_EXTC_P	24 43
	USB_85D	USB	USB_EXTC_N	24 43
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_P	6 31
	USB_85D	USB	USB_CAMERA_CONN_N	6 31
USB_BT	USB_85D	USB	USB_BT_P	6 24 31
	USB_85D	USB	USB_BT_N	6 24 31
USB_TPAD	USB_85D	USB	USB_TPAD_P	24 53
	USB_85D	USB	USB_TPAD_N	24 53
USB_IR	USB_85D	USB	USB_IR_P	24 44
	USB_85D	USB	USB_IR_N	24 44
PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS	18
USB_T29A	USB_85D	USB	USB_T29A_P	8 24
	USB_85D	USB	USB_T29A_N	8 24

SYNC_MASTER=K92_YUN SYNC_DATE=06/25/2010

PAGE TITLE

PCH Constraints 1

Apple Inc.

DRAWING NUMBER

SIZE D

REVISION

BRANCH

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Net Properties

		ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	LPC_AD	LPC_50S	LPC	LPC_AD<3..0>	6 16 45 47 88
	LPC_FRAME_L	LPC_50S	LPC	LPC_FRAME_L	6 16 45 47 88
	LPC_RESET_L	LPC_50S	LPC	LPCPLUS_RESET_L	6 25 47 88
	PCH_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC_R	18 25
	PCH_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC	25 45
	PCH_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS	6 25 47
	SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS_PCH_CLK	6 16 23 26 28 30 32 41 48 62 89
	SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS_PCH_DATA	6 16 23 26 28 30 32 41 48 62 89
	SMBUS_PCH_0_CLK	SMB_50S	SMB	SML_PCH_0_CLK	16 48
	SMBUS_PCH_0_DATA	SMB_50S	SMB	SML_PCH_0_DATA	16 48
	SMBUS_PCH_1_CLK	SMB_50S	SMB	SML_PCH_1_CLK	16 48
	SMBUS_PCH_1_DATA	SMB_50S	SMB	SML_PCH_1_DATA	16 48
	HDA_BIT_CLK	HDA_50S	HDA	HDA_BIT_CLK	16 57
		HDA_50S	HDA	HDA_BIT_CLK_R	16
	HDA_SYNC	HDA_50S	HDA	HDA_SYNC	16 57
		HDA_50S	HDA	HDA_SYNC_R	16
	HDA_RST_L	HDA_50S	HDA	HDA_RST_R_L	16
		HDA_50S	HDA	HDA_RST_L	16 57
	HDA_SDIN0	HDA_50S	HDA	HDA_SDIN0	16 57
		HDA_50S	HDA	AUD_SDI_R	57
	HDA_SDOUT	HDA_50S	HDA	HDA_SDOUT	16 57
		HDA_50S	HDA	HDA_SDOUT_R	16
	SPI_CLK	SPI_55S	SPI	SPI_CLK_R	16 47
	SPI_CLK	SPI_55S	SPI	SPI_CLK	47
	SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	16 47
	SPI_MOSI	SPI_55S	SPI	SPI_MOSI	47
	SPI_MISO	SPI_55S	SPI	SPI_MISO	16 47
	SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	16 47
		SPI_55S	SPI	SPI_CS0_L	47
	PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_P	36
	PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_N	36
	PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_P	16 36
	PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_N	16 36
	PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_P	16 36
	PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_N	16 36
	PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_C_P	36
	PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_C_N	36
	PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_P	6 31
	PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_N	6 31
	PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_P	16 31
	PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_N	16 31
	PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_P	6 16 31
	PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_N	6 16 31
	PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_PI_P	31
	PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_PI_N	31
	PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_PI_P	31
	PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_PI_N	31
	PCIE_FW_R2D	PCIE_85D	PCIE	PCIE_FW_R2D_P	38
	PCIE_FW_R2D	PCIE_85D	PCIE	PCIE_FW_R2D_N	38
	PCIE_FW_R2D	PCIE_85D	PCIE	PCIE_FW_R2D_C_P	16 38
	PCIE_FW_R2D	PCIE_85D	PCIE	PCIE_FW_R2D_C_N	16 38
	PCIE_FW_D2R	PCIE_85D	PCIE	PCIE_FW_D2R_P	16 38
	PCIE_FW_D2R	PCIE_85D	PCIE	PCIE_FW_D2R_N	16 38
	PCIE_FW_D2R	PCIE_85D	PCIE	PCIE_FW_D2R_C_P	38
	PCIE_FW_D2R	PCIE_85D	PCIE	PCIE_FW_D2R_C_N	38
I253	PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_P	16
I254	PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_N	16
I262	PCIE_CLK100M_T29_	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_P	16 33
I261	PCIE_CLK100M_T29_	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_N	16 33
I255		CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P	16
I257		CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N	16
I256	PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P	16
I259	PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N	16
I258		CPU_50S	CLK_PCIE	PCH_CLK14P3M_REFCLK	16
I260		CPU_50S	CLK_PCIE	PCH_CLK33M_PCIIN	16 25
	PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_P	16 74
		CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_N	16 74
	PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P	16 36
		CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N	16 36
	PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_P	16 31
		CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_N	16 31
	PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P	16 38
		CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N	16 38
	PCIE_CLK100M_EXCARD	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	16 32
		CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	16 32
I263	PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_T29_R2D_C_P<3..0>	8 33
I264	PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_T29_R2D_C_N<3..0>	8 33
I265	PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_T29_R2D_P<3..0>	33
I267	PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_T29_R2D_N<3..0>	33
I266	PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_T29_D2R_P<3..0>	8 33
I268	PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_T29_D2R_N<3..0>	8 33
I270	PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_T29_D2R_C_P<3..0>	33
I269	PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_T29_D2R_C_N<3..0>	33

SYNC_MASTER=K91_MLB SYNC_DATE=07/22/2010

PAGE TITLE: PCH Constraints 2

Apple Inc.

DRAWING NUMBER | SIZE: D | REVISION | BRANCH

CAESAR II (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_3X	*	=3:1_SPACING	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

CAESAR II (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

Ethernet Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALI	
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALO	
	ENET_50S	ENET_3X	ENET_RESET_L	32 36
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<3..0>	36 37
	ENET_100D	ENET_MDI	ENET_MDI_N<3..0>	36 37

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	
I162 FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_P	38 40
I163 FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_N	38 40
I164 FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_P	38 40
I165 FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_N	38 40

Port 0 and 2 Not Used

DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

T29 I2C Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_I2C	*	=2x_DIELECTRIC	?

T29 SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	=2x_DIELECTRIC	?

T29/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
T29DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	TOP,BOTTOM	=7x_DIELECTRIC	?

SOURCE: Bill Cornelius's T29 Routing Notes

T29/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL (NET_TYPE)	SPACING (NET_TYPE)	NET	
T29_R2D0	T29DP_80D	T29DP	T29_R2D_P<0>	6 85
T29_R2D0	T29DP_80D	T29DP	T29_R2D_N<0>	6 85
T29_R2D1	T29DP_80D	T29DP	T29_R2D_P<1>	6 85
T29_R2D1	T29DP_80D	T29DP	T29_R2D_N<1>	6 85
	T29DP_80D	T29DP	T29_R2D_C_F_P<1..0>	85
	T29DP_80D	T29DP	T29_R2D_C_F_N<1..0>	85
T29_D2R0	T29DP_100D	T29DP	T29_D2R_C_P<0>	6 85 86
T29_D2R0	T29DP_100D	T29DP	T29_D2R_C_N<0>	6 85 86
T29_D2R1	T29DP_100D	T29DP	T29_D2R_C_P<1>	6 85 86
T29_D2R1	T29DP_100D	T29DP	T29_D2R_C_N<1>	6 85 86
	T29DP_100D	T29DP	T29DPA_D2R1_AUXCH_P	6 86
	T29DP_100D	T29DP	T29DPA_D2R1_AUXCH_N	6 86
	T29DP_80D	T29DP	DP_SDRVA_ML_C_P<3..0>	6 85
	T29DP_80D	T29DP	DP_SDRVA_ML_C_N<3..0>	6 85
	T29DP_80D	T29DP	DP_SDRVA_ML_R_P<3..0>	6 85
	T29DP_80D	T29DP	DP_SDRVA_ML_R_N<3..0>	6 85
DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_P<2..0:2>	6 85 97
DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_N<2..0:2>	6 85 97
DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_P<3..1:2>	85
DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_N<3..1:2>	85
DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP_SDRVA_AUXCH_P	85
DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP_SDRVA_AUXCH_N	85
	T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_P	85
	T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_N	85
	T29DP_80D	T29DP	T29DPA_ML_P<3..0>	6 85 86
	T29DP_80D	T29DP	T29DPA_ML_N<3..0>	6 85 86
	T29DP_80D	T29DP	T29DPA_ML_C_P<3..0>	85 86
	T29DP_80D	T29DP	T29DPA_ML_C_N<3..0>	85 86
	T29DP_80D	T29DP	DP_A_EXT_AUXCH_P	85 86
	T29DP_80D	T29DP	DP_A_EXT_AUXCH_N	85 86
T29_R2D2	T29DP_80D	T29DP	T29_R2D_P<2>	
T29_R2D2	T29DP_80D	T29DP	T29_R2D_N<2>	
T29_R2D3	T29DP_80D	T29DP	T29_R2D_P<3>	
T29_R2D3	T29DP_80D	T29DP	T29_R2D_N<3>	
	T29DP_80D	T29DP	T29_R2D_C_F_P<3..2>	
	T29DP_80D	T29DP	T29_R2D_C_F_N<3..2>	
T29_D2R2	T29DP_100D	T29DP	T29_D2R_C_P<2>	
T29_D2R2	T29DP_100D	T29DP	T29_D2R_C_N<2>	
T29_D2R3	T29DP_100D	T29DP	T29_D2R_C_P<3>	
T29_D2R3	T29DP_100D	T29DP	T29_D2R_C_N<3>	
	T29DP_100D	T29DP	T29DPB_D2R3_AUXCH_P	
	T29DP_100D	T29DP	T29DPB_D2R3_AUXCH_N	
	T29DP_80D	T29DP	DP_SDRVB_ML_C_P<3..0>	
	T29DP_80D	T29DP	DP_SDRVB_ML_C_N<3..0>	
	T29DP_80D	T29DP	DP_SDRVB_ML_R_P<3..0>	
	T29DP_80D	T29DP	DP_SDRVB_ML_R_N<3..0>	
DP_SDRVB_ML_EVEN	T29DP_80D	T29DP	DP_SDRVB_ML_P<2..0:2>	97
DP_SDRVB_ML_EVEN	T29DP_80D	T29DP	DP_SDRVB_ML_N<2..0:2>	97
DP_SDRVB_ML_ODD	T29DP_80D	T29DP	DP_SDRVB_ML_P<3..1:2>	
DP_SDRVB_ML_ODD	T29DP_80D	T29DP	DP_SDRVB_ML_N<3..1:2>	
DP_SDRVB_AUXCH	T29DP_80D	T29DP	DP_SDRVB_AUXCH_P	
DP_SDRVB_AUXCH	T29DP_80D	T29DP	DP_SDRVB_AUXCH_N	
	T29DP_80D	T29DP	DP_SDRVB_AUXCH_C_P	
	T29DP_80D	T29DP	DP_SDRVB_AUXCH_C_N	
	T29DP_80D	T29DP	T29DPB_ML_P<3..0>	
	T29DP_80D	T29DP	T29DPB_ML_N<3..0>	
	T29DP_80D	T29DP	T29DPB_ML_C_P<3..0>	
	T29DP_80D	T29DP	T29DPB_ML_C_N<3..0>	
	T29DP_80D	T29DP	DP_B_EXT_AUXCH_P	
	T29DP_80D	T29DP	DP_B_EXT_AUXCH_N	

Only used on dual-port hosts.

T29 IC Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL (NET_TYPE)	SPACING (NET_TYPE)	NET	
	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_P<3..0>	6 33 79
	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_N<3..0>	6 33 79
DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_P<3..0>	6 33
DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_N<3..0>	6 33
	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_P	6 33 79
	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_N	6 33 79
DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_P	6 33
DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_N	6 33
	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_P<3..0>	6 33 79
	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_N<3..0>	6 33 79
DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_P<3..0>	6 33
DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_N<3..0>	6 33
	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_P	6 33 79
	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_N	6 33 79
DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_P	6 33
DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_N	6 33
	DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_P<3..0>	
	DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_N<3..0>	
	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_P	
	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_N	
	T29_I2C_55S	T29_I2C	I2C_T29_SCL	33 48 85
	T29_I2C_55S	T29_I2C	I2C_T29_SDA	33 48 85
T29_SPI_CLK	T29_SPI_55S	T29_SPI	T29_SPI_CLK	33
T29_SPI_MOSI	T29_SPI_55S	T29_SPI	T29_SPI_MOSI	33
T29_SPI_MISO	T29_SPI_55S	T29_SPI	T29_SPI_MISO	33
T29_SPI_CS_L	T29_SPI_55S	T29_SPI	T29_SPI_CS_L	33
	T29DP_80D	T29DP	T29_R2D_C_P<3..0>	6 8 33 85
	T29DP_80D	T29DP	T29_R2D_C_N<3..0>	6 8 33 85
	T29DP_100D	T29DP	T29_D2R_P<3..0>	6 8 33 85
	T29DP_100D	T29DP	T29_D2R_N<3..0>	6 8 33 85

Only used on hosts supporting T29 video-in

SYNC_MASTER=T29_REF SYNC_DATE=10/20/2010

PAGE TITLE

T29 Constraints

Apple Inc.

DRAWING NUMBER

SIZE D

REVISION

BRANCH

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	Net	Pages
SMBUS_SMC_A_S3_SCL	SMB_50S	SMB	SMBUS_SMC_A_S3_SCL	6 31 45 48 54 55
SMBUS_SMC_A_S3_SDA	SMB_50S	SMB	SMBUS_SMC_A_S3_SDA	6 31 45 48 54 55
SMBUS_SMC_B_S0_SCL	SMB_50S	SMB	SMBUS_SMC_B_S0_SCL	45 48 51
SMBUS_SMC_B_S0_SDA	SMB_50S	SMB	SMBUS_SMC_B_S0_SDA	45 48 51
SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL	6 31 45 48 51 80
SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA	6 31 45 48 51 80
SMBUS_SMC_BSA_SCL	SMB_50S	SMB	SMBUS_SMC_BSA_SCL	6 45 48 63 64
SMBUS_SMC_BSA_SDA	SMB_50S	SMB	SMBUS_SMC_BSA_SDA	6 45 48 63 64
SMBUS_SMC_MGMT_SCL	SMB_50S	SMB	SMBUS_SMC_MGMT_SCL	45 48 103 104
SMBUS_SMC_MGMT_SDA	SMB_50S	SMB	SMBUS_SMC_MGMT_SDA	45 48 103 104

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	Net	Pages
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	64
	1TO1_DIFFPAIR		CHGR_CSI_N	64
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	64
	1TO1_DIFFPAIR		CHGR_CSO_N	64

SYNC_MASTER=K17_MLB SYNC_DATE=05/14/2010

PAGE TITLE

SMC Constraints

Apple Inc.

DRAWING NUMBER

SIZE D

REVISION

BRANCH

8 7 6 5 4 3 2 1

GDDR5 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR5_45R50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR5_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
GDDR5_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	*	=5x_DIELECTRIC	?
GDDR5_CMD	*	=2x_DIELECTRIC	?
GDDR5_DATA	*	=3x_DIELECTRIC	?
GDDR5_EDC	*	=7x_DIELECTRIC	?

D

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 0.127 mm. Pairs should be within 0.508mm of entire channel.
DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DIsplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
Max length of LVDS/DisplayPort/TMDS traces: 13 inches.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.

C

GDDR5 FB A Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB_A0_CLK_P	76 77
	FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB_A0_CLK_N	76 77
	FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB_A1_CLK_P	76 77
	FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB_A1_CLK_N	76 77
	FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_A<8..0>	76 77
	FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_A<8..0>	76 77
	FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_ABI_L	76 77
	FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_ABI_L	76 77
	FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_RAS_L	76 77
	FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_RAS_L	76 77
	FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_CAS_L	76 77
	FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_CAS_L	76 77
	FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_WE_L	76 77
	FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_WE_L	76 77
	FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_CKE_L	76 77
	FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_CKE_L	76 77
	FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_CS_L	76 77
	FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_CS_L	76 77
	FB_A0_EDC0	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<0>	76 77
I293	FB_A0_EDC1	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<1>	76 77
I294	FB_A0_EDC2	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<2>	76 77
I295	FB_A0_EDC3	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<3>	76 77
I296	FB_A1_EDC0	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<0>	76 77
I297	FB_A1_EDC1	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<1>	76 77
I298	FB_A1_EDC2	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<2>	76 77
	FB_A1_EDC3	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<3>	76 77
	FB_A0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<0>	76 77
I299	FB_A0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<1>	76 77
I300	FB_A0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<2>	76 77
I301	FB_A0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<3>	76 77
I302	FB_A1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<0>	76 77
I303	FB_A1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<1>	76 77
I304	FB_A1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<2>	76 77
	FB_A1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<3>	76 77
	FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_P<0>	76 77
	FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_N<0>	76 77
	FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_P<1>	76 77
	FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_N<1>	76 77
	FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_P<0>	76 77
	FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_N<0>	76 77
	FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_P<1>	76 77
	FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_N<1>	76 77
	FB_A0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<7..0>	76 77
	FB_A0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<15..8>	76 77
	FB_A0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<23..16>	76 77
	FB_A0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<31..24>	76 77
	FB_A1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<7..0>	76 77
	FB_A1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<15..8>	76 77
	FB_A1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<23..16>	76 77
	FB_A1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<31..24>	76 77
	FB_AB_RESET	GDDR5_45R50SE	GDDR5_CMD	FB_RESET_L	76 77 78

GDDR5 FB B Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_P	76 78
	FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_N	76 78
	FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_P	76 78
	FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_N	76 78
	FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_A<8..0>	76 78
	FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_A<8..0>	76 78
	FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_ABI_L	76 78
	FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_ABI_L	76 78
	FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_RAS_L	76 78
	FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_RAS_L	76 78
	FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_CAS_L	76 78
	FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_CAS_L	76 78
	FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_WE_L	76 78
	FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_WE_L	76 78
	FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_CKE_L	76 78
	FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_CKE_L	76 78
	FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_CS_L	76 78
	FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_CS_L	76 78
	FB_B0_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<0>	76 78
I305	FB_B0_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<1>	76 78
I306	FB_B0_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<2>	76 78
I307	FB_B0_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<3>	76 78
I310	FB_B1_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<0>	76 78
I309	FB_B1_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<1>	76 78
I308	FB_B1_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<2>	76 78
	FB_B1_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<3>	76 78
	FB_B0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<0>	76 78
I311	FB_B0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<1>	76 78
I312	FB_B0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<2>	76 78
I313	FB_B0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<3>	76 78
I316	FB_B1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<0>	76 78
I315	FB_B1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<1>	76 78
I314	FB_B1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<2>	76 78
	FB_B1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<3>	76 78
	FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_P<0>	76 78
	FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_N<0>	76 78
	FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_P<1>	76 78
	FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_N<1>	76 78
	FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_P<0>	76 78
	FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_N<0>	76 78
	FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_P<1>	76 78
	FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_N<1>	76 78
	FB_B0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<7..0>	76 78
	FB_B0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<15..8>	76 78
	FB_B0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<23..16>	76 78
	FB_B0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<31..24>	76 78
	FB_B1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<7..0>	76 78
	FB_B1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<15..8>	76 78
	FB_B1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<23..16>	76 78
	FB_B1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<31..24>	76 78

B

MUXGFX Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LVDS_A_CLK	LVDS_85D	LVDS	LVDS_A_CLK_P	84 88
LVDS_A_CLK	LVDS_85D	LVDS	LVDS_A_CLK_N	84 88
LVDS_A_DATA	LVDS_85D	LVDS	LVDS_A_DATA_P<2..0>	84 88
LVDS_A_DATA	LVDS_85D	LVDS	LVDS_A_DATA_N<2..0>	84 88
LVDS_B_CLK	LVDS_85D	LVDS	LVDS_B_CLK_P	84 88
LVDS_B_CLK	LVDS_85D	LVDS	LVDS_B_CLK_N	84 88
LVDS_B_DATA	LVDS_85D	LVDS	LVDS_B_DATA_P<2..0>	84 88
LVDS_B_DATA	LVDS_85D	LVDS	LVDS_B_DATA_N<2..0>	84 88
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_F_P	6 83
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_F_N	6 83
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_F_P	6 83
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_F_N	6 83
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_P	83 84
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_N	83 84
	LVDS_85D	LVDS	LVDS_CONN_A_DATA_P<2..0>	6 83 84
	LVDS_85D	LVDS	LVDS_CONN_A_DATA_N<2..0>	6 83 84
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_P	83 84
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_N	83 84
	LVDS_85D	LVDS	LVDS_CONN_B_DATA_P<2..0>	6 83 84
	LVDS_85D	LVDS	LVDS_CONN_B_DATA_N<2..0>	6 83 84

Whistler Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
GPU_CLK27M	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M	79 80
GPU_CLK100M	CLK_SLOW_55S	CLK_SLOW	GPU_CLK100M	79 80
LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS_EG_A_CLK_P	79 88
LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS_EG_A_CLK_N	79 88
LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS_EG_A_DATA_P<2..0>	79 88
LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS_EG_A_DATA_N<2..0>	79 88
LVDS_EG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_A_DATA_P<3>	79 80
LVDS_EG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_A_DATA_N<3>	79 80
LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS_EG_B_DATA_P<2..0>	79 88
LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS_EG_B_DATA_N<2..0>	79 88
LVDS_EG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_B_DATA_P<3>	79 80
LVDS_EG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_B_DATA_N<3>	79 80
DP_ML	DP_85D	DISPLAYPORT	DP_EXTA_ML_C_P<3..0>	79 85
	DP_85D	DISPLAYPORT	DP_EXTA_ML_C_N<3..0>	79 85
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_P	84 85
	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_N	84 85
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_EG_AUX_CH_P	79 84
	DP_85D	DISPLAYPORT	DP_EG_AUX_CH_N	79 84

A

SYNC_MASTER=K91_MLB SYNC_DATE=07/21/2010

PAGE TITLE
GPU (Whistler) CONSTRAINTS

Apple Inc.

DRAWING NUMBER
SIZE D
REVISION
BRANCH

8 7 6 5 4 3 2 1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
AUDIODIFF	*	=1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	10 mm OVERRIDE	OVERRIDE	OVERRIDE
USB_85D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	BOTTOM OVERRIDE	OVERRIDE	OVERRIDE	0.23 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_85D	BGA	LVDS_85D
DP_85D	BGA	100_DIFF_BGA
SATA_90D	BGA	100_DIFF_BGA
CLK_PCIE_90D	BGA	100_DIFF_BGA

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

K92 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET	PAGES
	ENET_100D	ENETCONN	ENETCONN_P<3..0>	37
	ENET_100D	ENETCONN	ENETCONN_N<3..0>	37
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_P	49 65
	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_N	49 65
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAISNS_R_P	49
	SENSE_1TO1_55S	SENSE	VCCSAISNS_R_N	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_R_P	49
	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_R_N	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_P	49 70
	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_N	49 70
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOISNS_R_P	49
	SENSE_1TO1_55S	SENSE	CPUVCCIOISNS_R_N	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GPUISENS_N	49
	SENSE_1TO1_55S	SENSE	GPUISENS_P	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_N	49 67
	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_P	49 67
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P	31 103
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N	31 103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_P	103
	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_N	103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V8_S0GPU_P	103
	SENSE_1TO1_55S	SENSE	ISNS_PP1V8_S0GPU_N	103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_N	41 103
	SENSE_1TO1_55S	SENSE	ISNS_HDD_P	41 103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V5_S0GPU_P	103
	SENSE_1TO1_55S	SENSE	ISNS_PP1V5_S0GPU_N	103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N	89 103
	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P	89 103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_N	41 103
	SENSE_1TO1_55S	SENSE	ISNS_ODD_P	41 103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_P	50
	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_GPU_P	50
	SENSE_1TO1_55S	SENSE	ISNS_HS_GPU_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_P	50
	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1_P	50 68 69
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1_N	50 69
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUM_R_P	50
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUM_R_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_P	50
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_P	50 69
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_N	50 69
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_R_P	50
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_R_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_R_P	50
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_R_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_R_P	103
	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_R_N	103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V8_S0GPU_R_P	103
	SENSE_1TO1_55S	SENSE	ISNS_PP1V8_S0GPU_R_N	103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V5_S0GPU_R_P	103
	SENSE_1TO1_55S	SENSE	ISNS_PP1V5_S0GPU_R_N	103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_P	103
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_N	103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_P	103
	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_N	103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_P	103
	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_N	103
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	BI_MIC_P	61 62
	AUDIODIFF	AUDIO	BI_MIC_N	61 62
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_P	58 60
	AUDIODIFF	AUDIO	AUD_LO1_R_N	58 60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	57 60
	AUDIODIFF	AUDIO	AUD_LO2_R_N	57 60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_R_P	57 60
	AUDIODIFF	AUDIO	AUD_LO3_R_N	57 60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_L_P	57 60
	AUDIODIFF	AUDIO	AUD_LO3_L_N	57 60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INR_P	57 62
	AUDIODIFF	AUDIO	AUD_MIC_INR_N	57 62
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_P	57 62
	AUDIODIFF	AUDIO	AUD_MIC_INL_N	57 62
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_BL_IN_L_P	60
	AUDIODIFF	AUDIO	SPKRAMP_BL_IN_L_N	60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_FL_IN_L_P	60
	AUDIODIFF	AUDIO	SPKRAMP_FL_IN_L_N	60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_BR_IN_L_P	60
	AUDIODIFF	AUDIO	SPKRAMP_BR_IN_L_N	60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_FR_IN_L_P	60
	AUDIODIFF	AUDIO	SPKRAMP_FR_IN_L_N	60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_LFE_IN_L_P	60
	AUDIODIFF	AUDIO	SPKRAMP_LFE_IN_L_N	60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375BL_IN_P	60
	AUDIODIFF	AUDIO	SSM2375BL_IN_N	60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375FL_IN_P	60
	AUDIODIFF	AUDIO	SSM2375FL_IN_N	60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375BR_IN_P	60
	AUDIODIFF	AUDIO	SSM2375BR_IN_N	60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375FR_IN_P	60
	AUDIODIFF	AUDIO	SSM2375FR_IN_N	60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375LFE_IN_P	60
	AUDIODIFF	AUDIO	SSM2375LFE_IN_N	60

K92 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET	PAGES
PCIE_EXCARD_R2D	PCIE_85D	PCIE	PCIE_EXCARD_R2D_P	6 32
	PCIE_85D	PCIE	PCIE_EXCARD_R2D_N	6 32
PCIE_EXCARD_D2R	PCIE_85D	PCIE	PCIE_EXCARD_D2R_P	6 16 32
	PCIE_85D	PCIE	PCIE_EXCARD_D2R_N	6 16 32
PCIE_EXCARD_R2D	PCIE_85D	PCIE	PCIE_EXCARD_R2D_C_P	16 32
	PCIE_85D	PCIE	PCIE_EXCARD_R2D_C_N	16 32
PCIE_CLK100M_EXCARD	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_CONN_P	6 32
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_CONN_N	6 32
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	6 31
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	6 31
	1TO1_DIFFPAIR		CHGR_CSI_R_P	64
	1TO1_DIFFPAIR		CHGR_CSI_R_N	64
	1TO1_DIFFPAIR		CHGR_CSO_R_P	50 64
	1TO1_DIFFPAIR		CHGR_CSO_R_N	50 64
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_P	42
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_N	42
(USB_EXTA)	USB_85D	USB	USB2_LT1_P	42
(USB_EXTA)	USB_85D	USB	USB2_LT1_N	42
	USB_85D	USB	CONN_USB2_BT_P	
	USB_85D	USB	CONN_USB2_BT_N	
(USB_EXTB)	USB_85D	USB	USB_LT2_P	42
	USB_85D	USB	USB_LT2_N	42
USB_EXCARD	USB_85D	USB	USB_EXCARD_P	8 24 32
	USB_85D	USB	USB_EXCARD_N	8 24 32
USB_EXCARD	USB_85D	USB	USB2_EXCARD_CONN_P	6 32
	USB_85D	USB	USB2_EXCARD_CONN_N	6 32
(USB_EXTC)	USB_85D	USB	USB_LT3_P	43
	USB_85D	USB	USB_LT3_N	43
	USB_85D	USB	USB_TPAD_R_P	53
	USB_85D	USB	USB_TPAD_R_N	53
		SB_POWER	PP3V3_S5	48 56 71 72 73 83 86 91 102 104 6 7 17 19 20 22 23 24 25 29 46
		SB_POWER	PP3V3_S0	61 62 72 73 80 83 84 85 88 89 6 7 12 23 25 26 28 32 35 36 39 40 41 45 46 48 49 50 51 52 54 57
		SB_POWER	PP1V5_S3RS0	7 72 104 91 102
		GND	GND	

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET	PAGES
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	51
	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N	51
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPU_THERMD_P	9 51
	THERM_1TO1_55S	THERM	CPU_THERMD_N	9 51
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P	51
	THERM_1TO1_55S	THERM	GPUTHMSNS_D_N	51
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_P	51 79
	THERM_1TO1_55S	THERM	GPU_TDIODE_N	51 79
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	T29_THERMD_P	33 51
	THERM_1TO1_55S	THERM	T29_THERMD_N	51

K92 Specific Net Properties
K91 does not have

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET	PAGES
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP3V3_S3_P	104
	SENSE_1TO1_55S	SENSE	ISNS_PP3V3_S3_N	104
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP3V3_S5_N	104
	SENSE_1TO1_55S	SENSE	ISNS_PP3V3_S5_P	104
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP5V_S3_N	104
	SENSE_1TO1_55S	SENSE	ISNS_PP5V_S3_P	104
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V05_S0PCH_N	104
	SENSE_1TO1_55S	SENSE	ISNS_PP1V05_S0PCH_P	104
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP5V_S0_N	104
	SENSE_1TO1_55S	SENSE	ISNS_PP5V_S0_P	104
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_CPU_DDR_N	104
	SENSE_1TO1_55S	SENSE	ISNS_CPU_DDR_P	104

SYNC_MASTER=K91_MLB SYNC_DATE=07/22/2010

PAGE TITLE
Project Specific Constraints

Apple Inc.

DRAWING NUMBER
SIZE D
REVISION
BRANCH

K92 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD
37_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.095 MM			
37_OHM_SE	*	Y	0.155 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
40_OHM_SE	*	Y	0.135 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD
45_OHM_SE	TOP,BOTTOM	Y	0.13 MM	0.13 MM			
45_OHM_SE	*	Y	0.099 MM	0.099 MM	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.095 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	ISL9,ISL10	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.175 MM	0.175 MM		0.200 MM	0.200 MM
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.135 MM	0.135 MM		0.160 MM	0.160 MM
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL9,ISL10	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.090 MM		0.190 MM	0.190 MM
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL9,ISL10	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.090 MM		0.230 MM	0.230 MM
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL9,ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2,ISL11	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4	Y	0.065 MM	0.065 MM		0.200 MM	0.200 MM
110_OHM_DIFF	ISL9,ISL10	Y	0.065 MM	0.065 MM		0.200 MM	0.200 MM
110_OHM_DIFF	ISL2,ISL11	Y	0.065 MM	0.065 MM		0.200 MM	0.200 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
P072_SPACE	*	0.071 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?
5:1_SPACING	*	0.5 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?
7X_DIELECTRIC	*	0.490 MM	?

NOTE: Based on K92 mlb stackup.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

SYNC_MASTER=K17_MLB SYNC_DATE=05/14/2010

PAGE TITLE

PCB Rule Definitions

Apple Inc.

DRAWING NUMBER

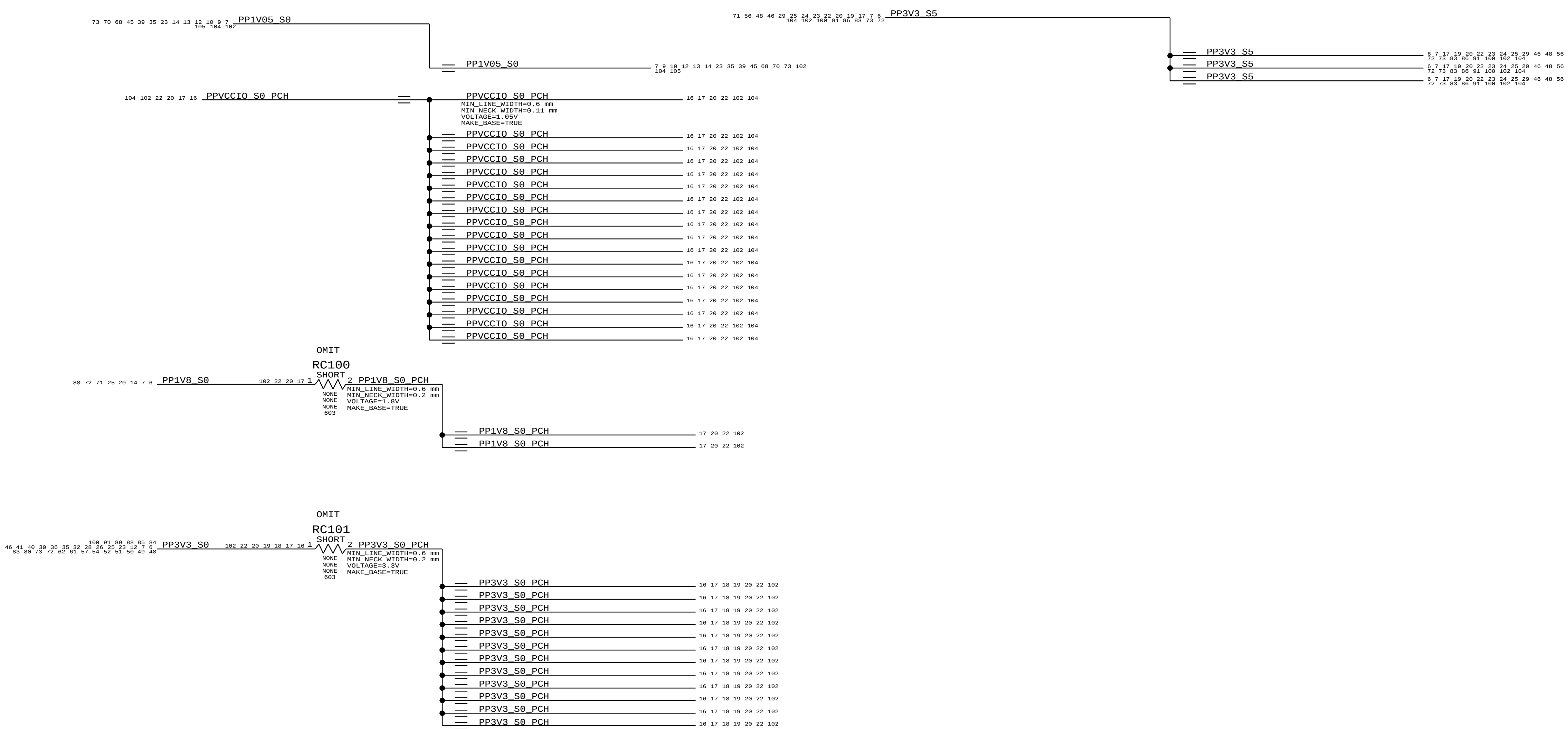
SIZE D

REVISION

BRANCH

PCH "S0" Rails

PCH "S5" Rail



SYNC_MASTER=K17_MLB SYNC_DATE=04/27/2010

PAGE TITLE

PCH Power Aliases

Apple Inc.

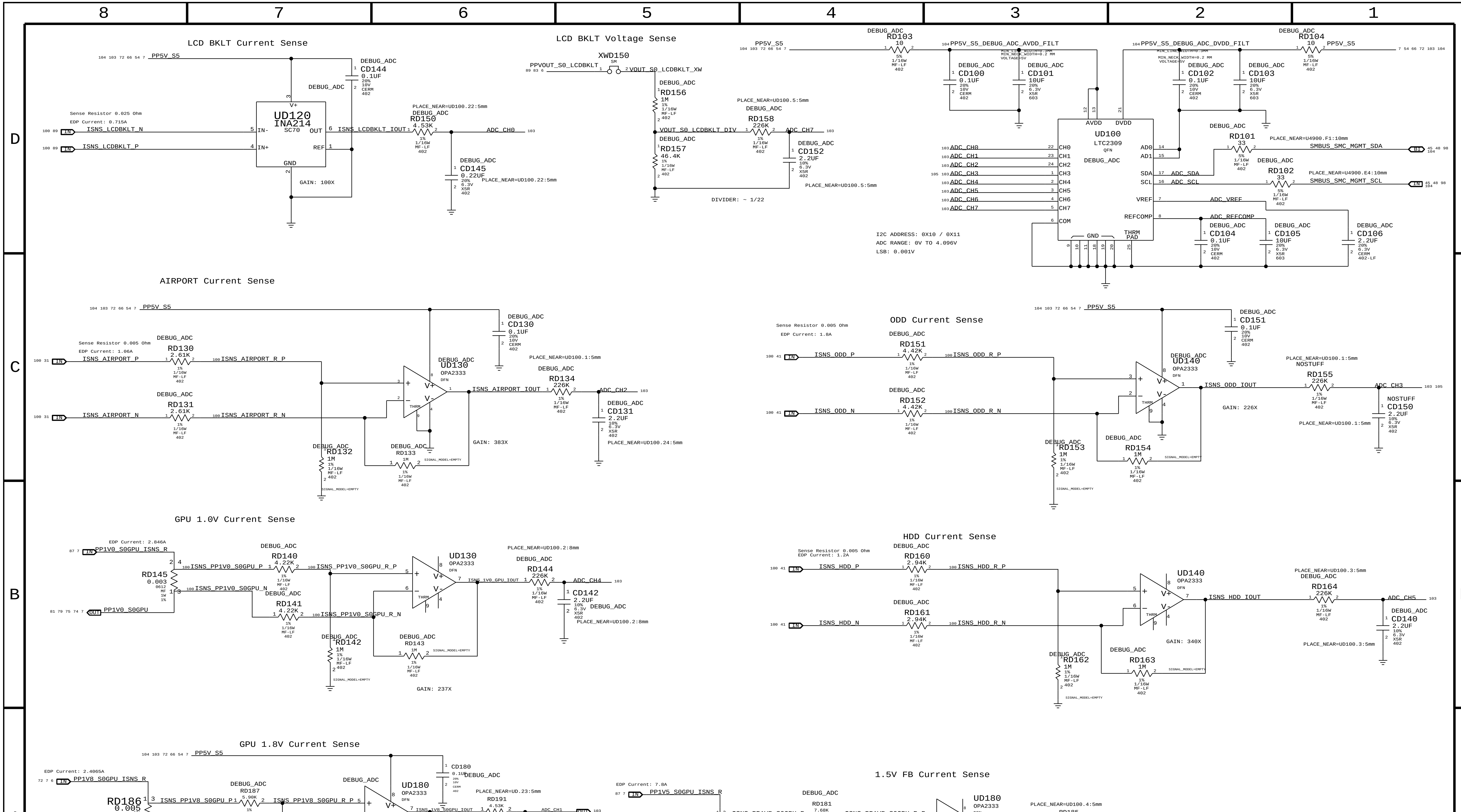
DRAWING NUMBER

SIZE D

REVISION

BRANCH

NOTICE OF PROPRIETARY PROPERTY:



SYNC_MASTER=K92_DINESH SYNC_DATE=09/07/2010

PAGE TITLE

DEBUG SENSORS AND ADC

Apple Inc.

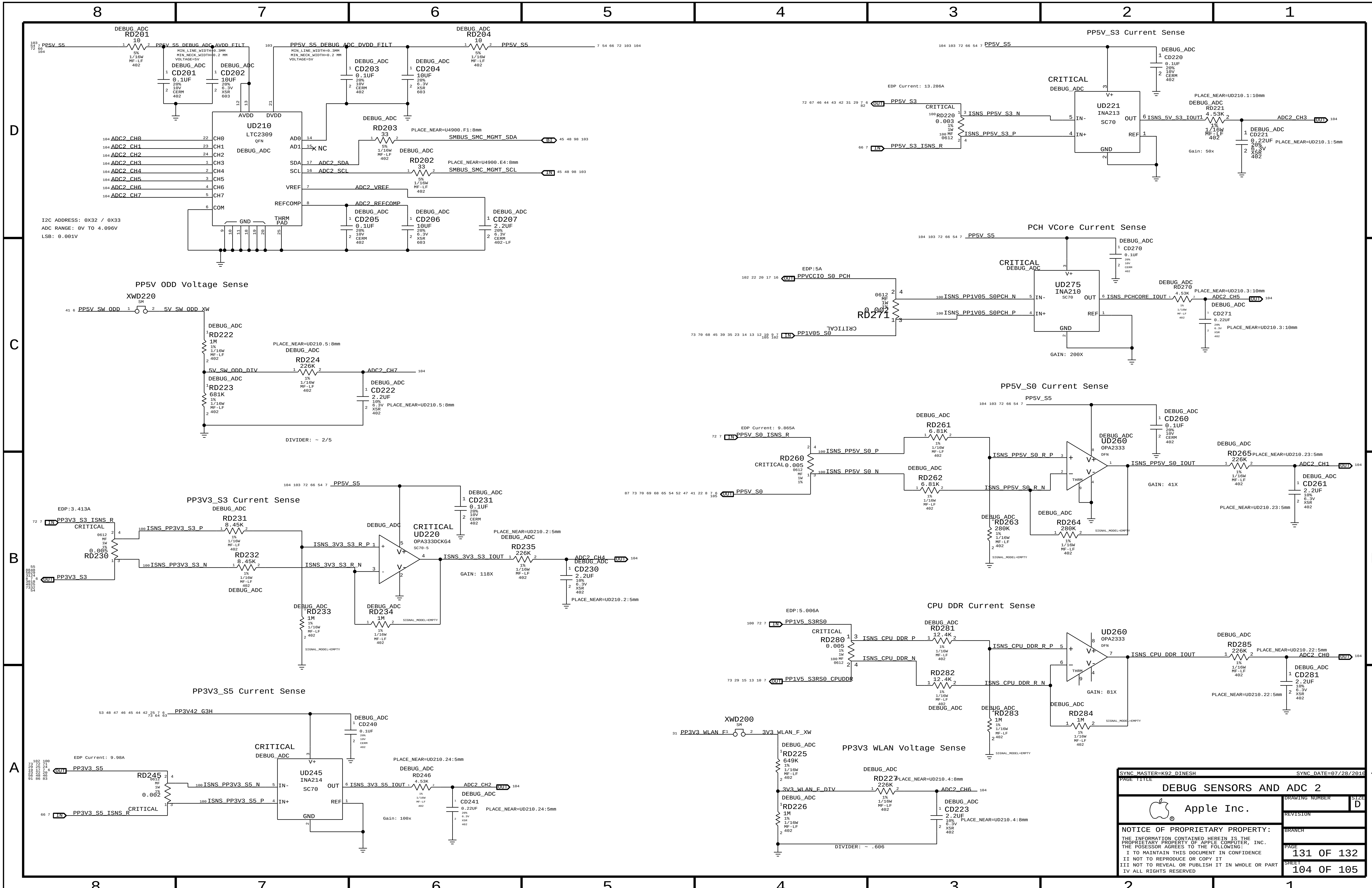
DRAWING NUMBER SIZE D

REVISION

BRANCH

PAGE 130 OF 132

SHEET 103 OF 105



SYNC_MASTER=K92_DINESH SYNC_DATE=07/28/2010

PAGE TITLE

DEBUG SENSORS AND ADC 2

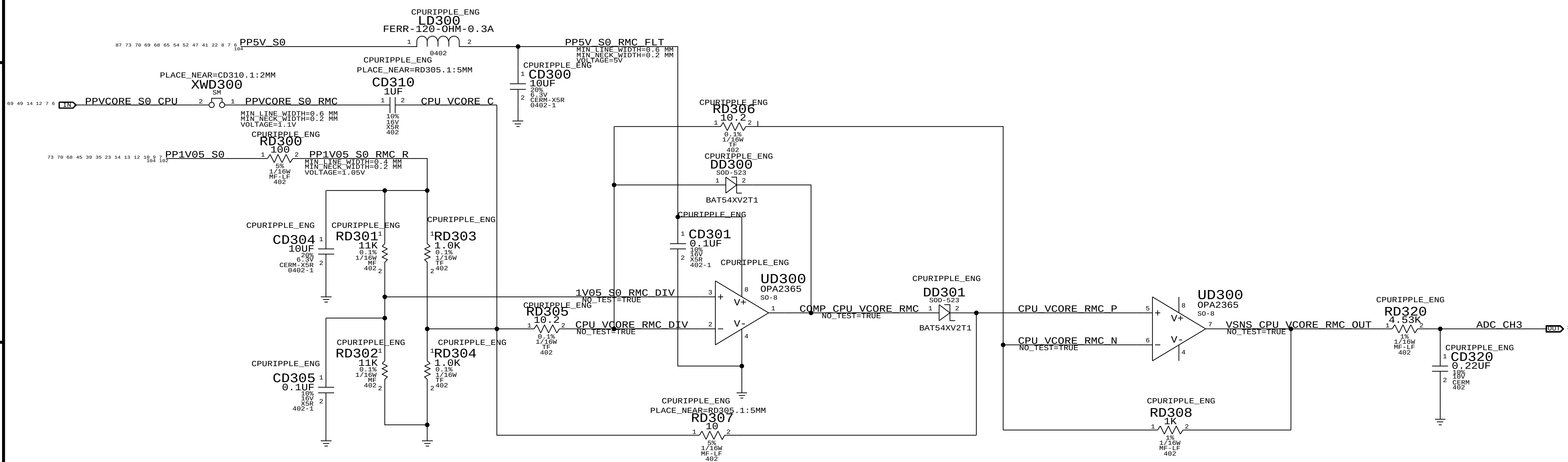
Apple Inc.

DRAWING NUMBER

SIZE D

REVISION

BRANCH



SYNC_MASTER=K92_DINESH SYNC_DATE=08/23/2010

PAGE TITLE

Power Supplies BIST

Apple Inc.

DRAWING NUMBER

SIZE D

REVISION

BRANCH