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HSF Property:ROHS or Halogen-Free(5L3?)

DAKAR10F/FG

2011.09.02

DATE	CHANGE NO.	REV
21-OCT-2002		

	EE	DATE	POWER	DATE
DRAWER				
DESIGN				
CHECK				
RESPONSIBLE				

SIZE= VER:

FILE NAME:

P/N XXX 1310xxxxx-0-0

INVENTEC

TITLE MODEL,PROJECT,FUNCTION
Everest Main Board

SIZE	CODE	DOC.NUMBER	REV
C	CS		X01

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AMD
W/ POWER EXPRESS
THAMES
29X 29 MM

PEG

IVY BRIDGE
DC 35W
SOCKET-RPGA989
37.5 X 37.5 X 5 mm

DDR3 INTERFACE
DDR3@1.5/0.75V
(1333/1600 MHZ)
204-PIN SODIMM0

DDR3 INTERFACE
DDR3@1.5/0.75V
(1333/1600 MHZ)
204-PIN SODIMM1

FDI
DMI 2.0

HDMI
CRT
LCM
LVDS

PCH
PANTHER POINT
25 X 25 X 2.3 mm

HDA
AUDIO CODEC
REA_ALC269Q_VB6
INTERNAL MIC IN
EXT MIC IN
HEADPHONE

USB2.0
USB_0: USB CONN
USB_2: USB CONN
USB_8: CARD READER
USB_9: MINICARD WLAN
USB_10:WEBCAM

SLEEP & CHARGE
USB3.0
USB_1: USB3.0 CONN

USB2.0
USB_8:CARD READER
REA_RTS5129

SATA
SATA0:ESATA
SATA1: HDD
SATA6: ODD

SPI

RJ45
PCIE_1:LAN
ATHEROS_AR8161/8162
PCIE

PCIE_2:WLAN
PCIE

PCIE_3:USB3.0
PCIE

EC WINDBOND
NPCE885LA0DX
SPI
SPI FLASH 8MB
MXIC_MX25L3206EM2I

KEYBOARD
TOUCH PAD

ENE-P2809A
THERMAL SENSOR

BATTERY CHARGER &
DC/DC & IMVP 7

LI-ION BATTERY
6-Cell

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ADAPTOR

FUSE

65W-75W 8A 6036A0003401
90W 10A 6036A0002901
120W 12A 6036A0006001

BQ24725RGRR
CHARGER

EC_SMB2
CHG_EN
BATT_IN
ACPRES

BATTERY PACK

+VBAT

TPS51123

POWER BUDGET 12.139 A
F 300K
OCP 10.4A R=120K
PEAK 7.283A AVG 2.363A
220UF_25M£[// 53.92UF_1.529M£[

+V5A_+-5%

AO6402L

POWER BUDGET 4.711A INRUSH 0.9A
PEAK2.592A 100.82UF_0.842M£[

+V5S

TSP51461

POWER BUDGET 6A
F 340K
OCP 6A
PEAK 6A AVG 1.262A

+V0.85S_+-0.5%

+VCORE_+-0.5%

+VCORE1_+-0.5%

TI_TPS61640

POWER BUDGET 53A
F 280K
OCP 53A
PEAK 53A AVG 28.822A
1880UF_1.1M£[// 2276UF_0.203M£[

TPS51123

POWER BUDGET 9.429 A
F 375K
OCP 10.7A R=130K
PEAK 5.695A AVG1.048 A
220UF_25M£[//10.6UF_5.924M£[

+V3LA_+-5%

AO6402L

POWER BUDGET 4.711A INRUSH 0.9A
PEAK2.592A 100.82UF_0.842M£[

+V3A

AM2321P

POWER BUDGET 4.711A INRUSH 0.9A
PEAK2.592A 100.82UF_0.842M£[

+V3_LAN

AO6402L

POWER BUDGET 4.711A INRUSH 0.9A
PEAK2.592A 100.82UF_0.842M£[

+V3S

GMT_AT1530F11U

POWER BUDGET 4.711A INRUSH 0.9A
PEAK2.592A 100.82UF_0.842M£[

+V1.8S

VDD_CORE

TPS51217

POWER BUDGET 20.070A
F 340K
OCP 29.1A R=75K
PEAK 20.070A AVG 11.531A
560UF_25M£[// 80UF_0.93M£[

TPS51216

POWER BUDGET 13.7 A
F 340K
OCP 10.1A R=115K
PEAK 17.107A AVG4.835 A
560UF_25M£[// 1274.8UF_0.214M£[

V1.5_+-5%

TPS51216

+V0.75S

AON7410

+V1.5S

AON7410

+V1.5_CPU

TPS51216

+VTT_+-5%

POWER BUDGET 13.7 A
F 340K
OCP 10.1A R=115K
PEAK 17.107A AVG4.835 A
560UF_25M£[// 1274.8UF_0.214M£[

CHANGING POINTS~~
TPS51218 SAME AS 2009 PROJECT
TPS51217 SAME AS 2010 PROJECT
+V1.8S IS NEW IC GMT_AT1530F11U
CHARGE IS NEW IC BQ24725
VCC CORE IS NEW IC TPS51640
VTT IS NEW IC TPS51219
V0.85 IS NEW IC TPS 51641
V3_V5 IS NEW IC TPS51123
POWER BUDGET ~~IC SPEC (MAX CURRENT)
PEAK CURRENT ~~RATIO OF INTERNAL PREDICTION
AVG CURRENT ~~TEST RESULT(MAX CURRENT)
INRUSH ~~L/S TURN NO

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FUSE6000
65W-75W 8A(6036A0003401)
90W 10A(6036A0002901)
120W 12A(6036A0006001)

CN6000
ACES_50315_0047N_002_4P
FUSE6000
8A_125V
C7601
1000PF_50V_2
C7602
10PF_50V_2
L7600
NFE31PT222Z1E9L
PVADPTR
TP6003
TP6004
TP6005
TP30
TP30
TP30
PVBAT
R6800
RSC_0603_DY
OUT
HW_V_ADC
R6802
33K_5%_2_DY
C6800
0.1UF_16V_2_DY
NEAR EC
R6801
RSC_0603_DY
21E8
21E6
21D2
21D3
BATT_IN
EC_SMB1_DATA
EC_SMB1_CLK
BI
BI
P3V3AL
R6054
1M_5%_2
R6053
220K_1%_2
PVPACK
FUSE6050
LITTLEFUSE_R451015_15A_65V
C6050
1000PF_50V_2
R6052
1K_5%_2
R6050
33_5%_2
R6051
33_5%_2
D6701
EZJZ0V500AA_DY
D6702
EZJZ0V500AA_DY
D6703
CN6050
SYN_200045GR009G18TZR_9P
BATT+
BATT+
ID
B-I
TS
SMD
SMC
GND
GND
G1
G2
G3
G4
PVADPTR
R6015
4.7K_5%_3
R6014
RSC_0603_DY
Q6010
AM4410NC
Q6011
AM4410NC
C6030
2200PF_50V_2
C6031
0.1UF_25V_3
R6006
RSC_0603_DY
R6004
4.3K_5%_2
R6005
4.3K_5%_2
D6002
DIODES_BAV99
C6014
CSC0805_DY
R6018
RSC_1206_DY
R6019
RSC_1206_DY
R6002
20.5K_1%_2
R6013
10K_5%_3
ACPRES
R6000
0.01_1%_6
C6020
0.1UF_16V_2
C6021
0.1UF_25V_3
C6022
0.1UF_25V_3
PVADPTR
D6000
BAT54C_30V_0.2A
R6012
10_5%_5
C6026
1UF_25V_3
U6000
TI_BQ24725RGRR_QFN_20P
ACOK
ACDRV
CMSRC
ACP
ACN
TML
VCC
PHASE
HIDRV
BTST
REGN
LODRV
GND
SRN
SRP
BATDRV
ACDET
IOUT
SDA
SCL
ILIM
VRCHARGER_HG
VRCHARGER_PH
VRCHARGER_LG
C6027
0.047UF_16V_2
C6028
1UF_10V_2
D6001
BAT54C_30V_0.2A
PVBAT
PAD6000
POWERPAD_2_0610
Q6000
AON7410
C6001
470PF_50V_2
C6002
4.7UF_25V_5
C6003
4.7UF_25V_5
C6004
CSC0805_DY
Q6001
AON7410
D6700
SBR3U40P1_DY
R7600
RSC_0603_DY
C7600
CSC0402_DY
L6000
ETQP3W4R7WFN
R6001
0.01_1%_6
C6023
0.1UF_16V_2
C6024
0.1UF_25V_3
C6025
0.1UF_25V_3
C6010
4.7UF_25V_5
C6011
4.7UF_25V_5
C6012
4.7UF_25V_5
C6013
4.7UF_25V_5
CSC0805_DY
PVPACK
Q6012
TPCA8065_H
C6033
0.1UF_25V_3
C6036
100PF_50V_2
NEAR IC
C6037
100PF_50V_2
NEAR EC
C6035
CSC0402_DY
C6034
CSC0402_DY
R6003
3.32K_1%_3
C6029
CSC0603_DY
R6016
SHORT_0402
EC_SMB2_DATA
R6017
SHORT_0402
EC_SMB2_CLK
P3V3AL
R6007
10K_5%_2
R6008
30K_5%_2
C6032
0.1UF_16V_2
R6011
SHORT_0402
R6010
6.98_1%_2
R6009
4.3K_5%_2

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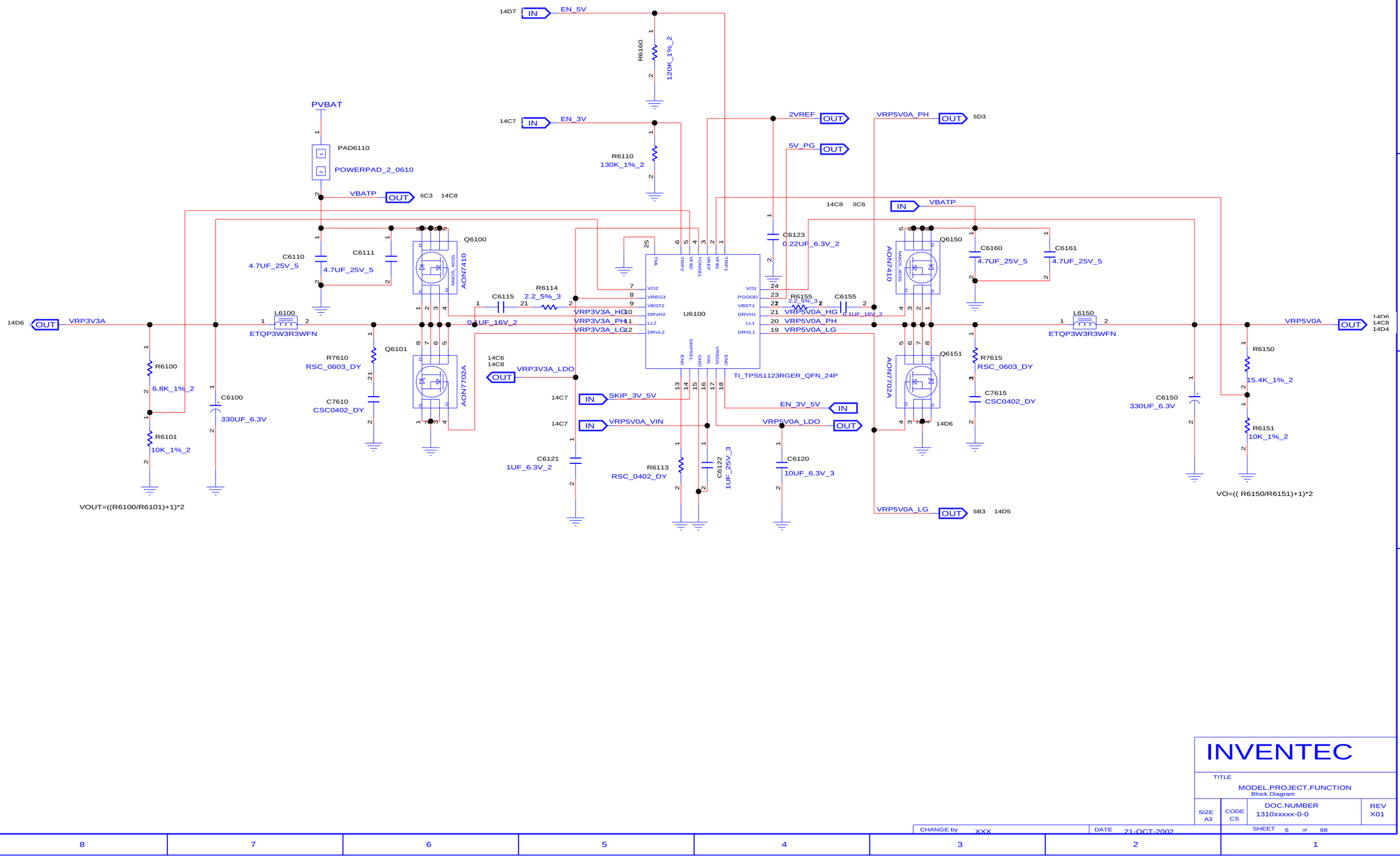

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SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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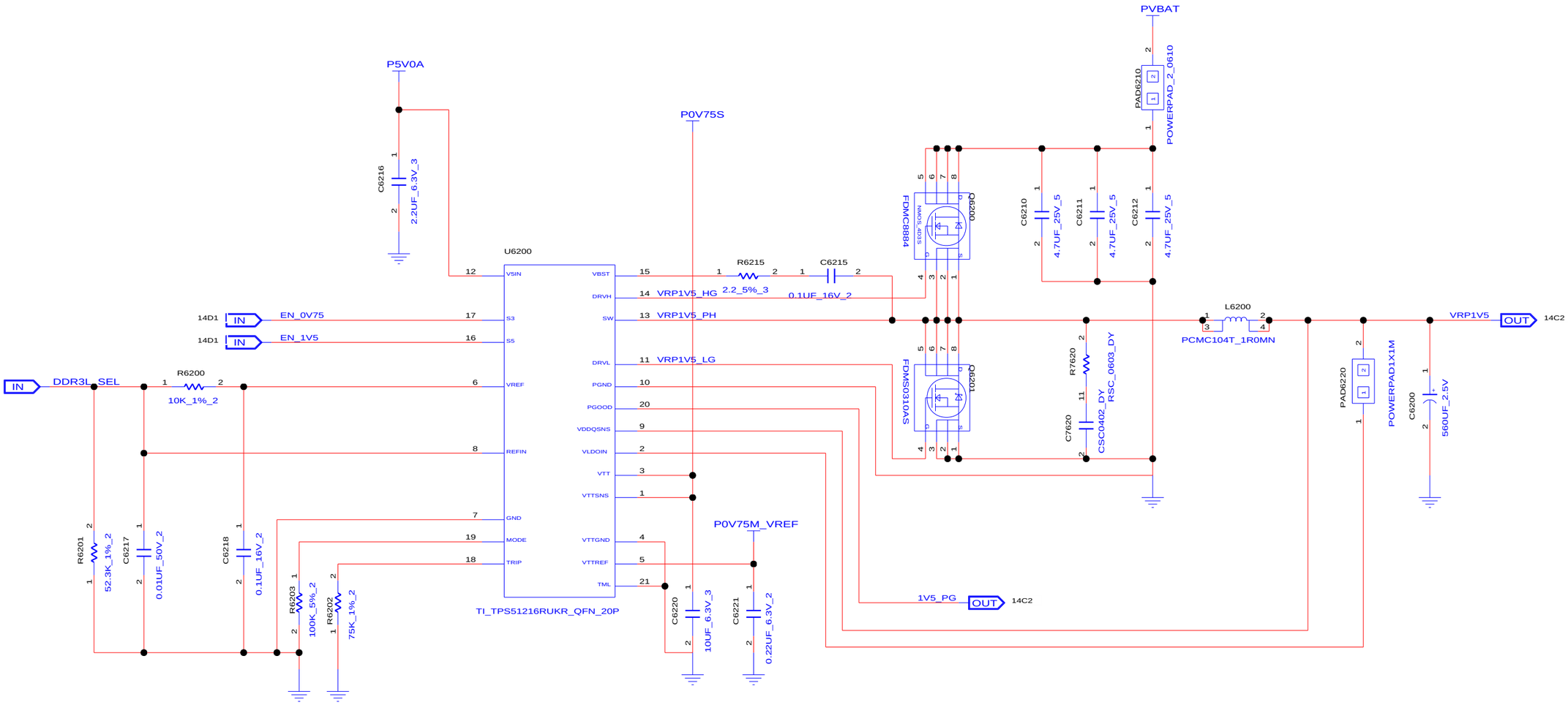

VOUT=REFIN=1.8*(R6201/(R6200+R6201))

MODE=100KOHM:TRACKING DISCHARGE

STATE	S3	S5	VREF	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF(High-Z)
S4/S5	LO	LO	OFF	OFF(Discharge)	OFF(Discharge)	OFF(Discharge)

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SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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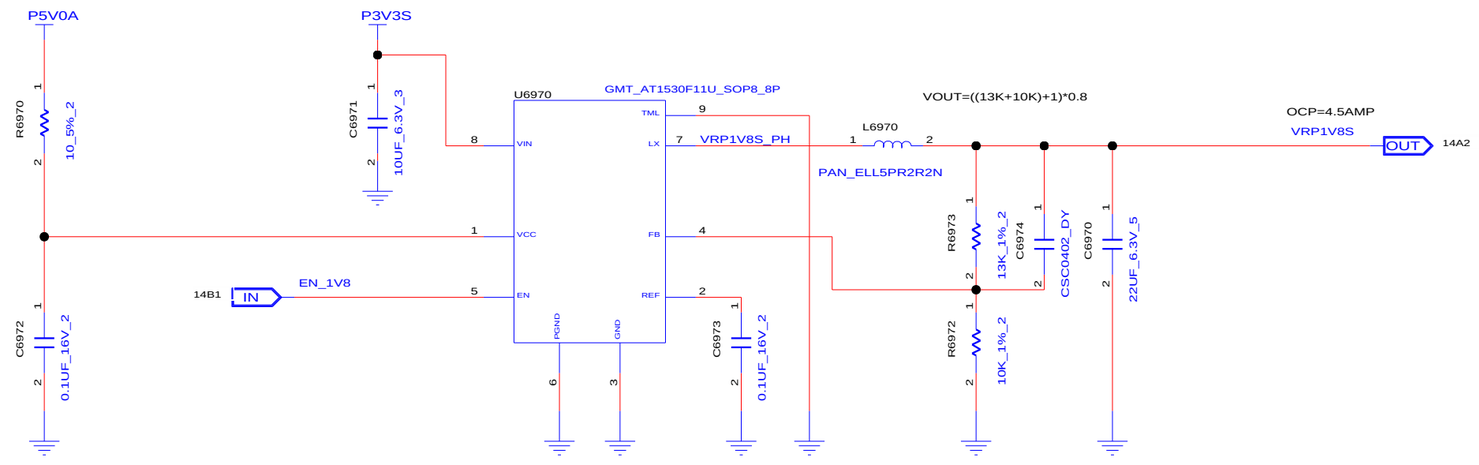

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TITLE

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SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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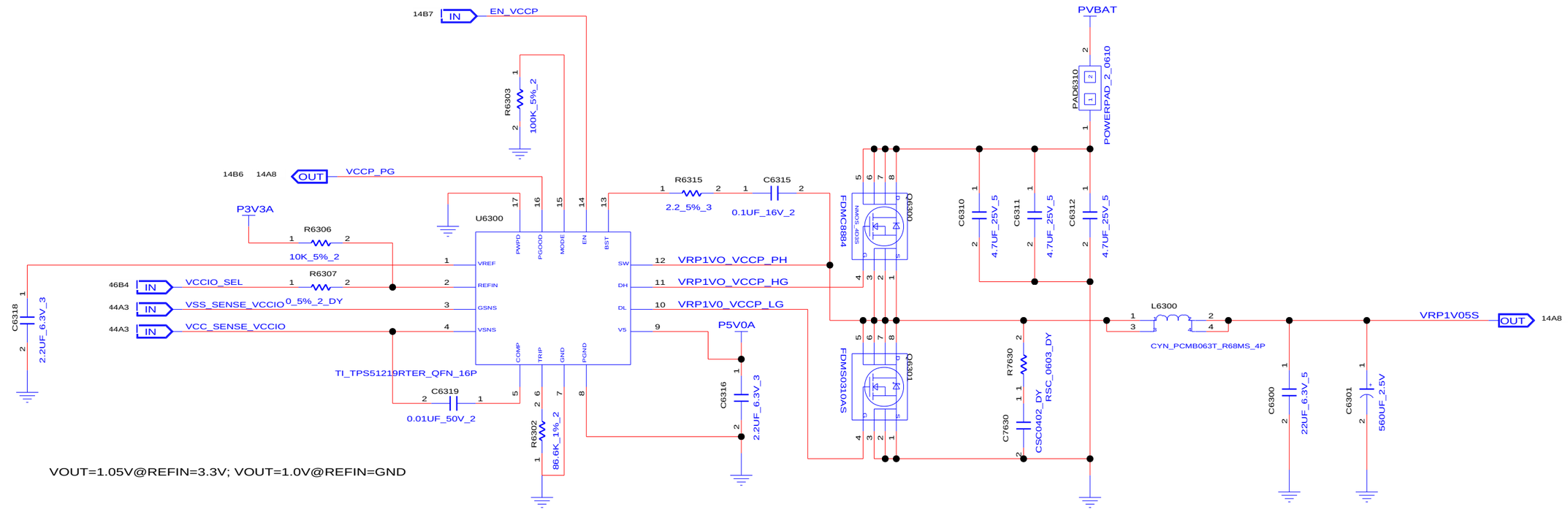

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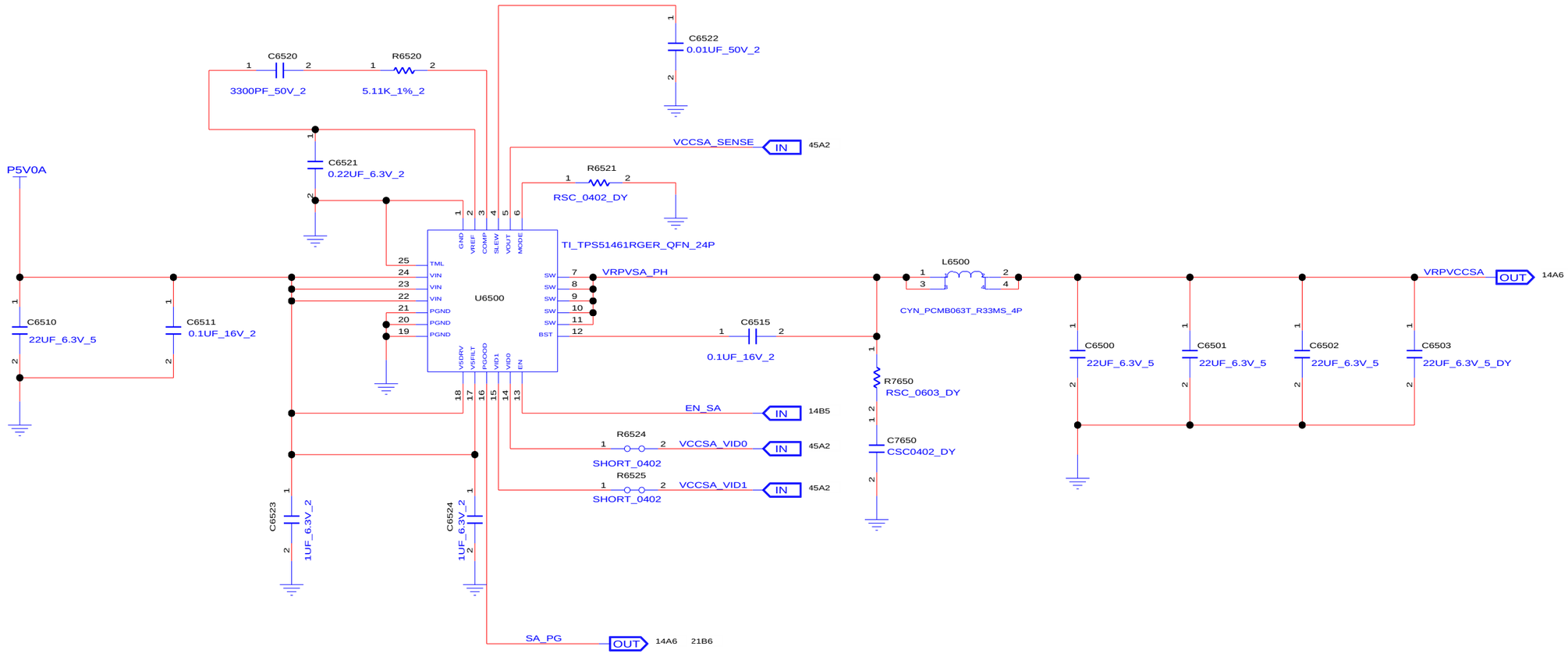

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	2+1	2+0
R6626	3.3K	DNP
R6627	56K	DNP
R6711	200K	DNP
R6712	30K	DNP
R6714	DNP	0
R6716	DNP	0
R6719	DNP	0
R6723	DNP	0

U6600

TI_TPS51650RSLR_QFN_48P

R6638

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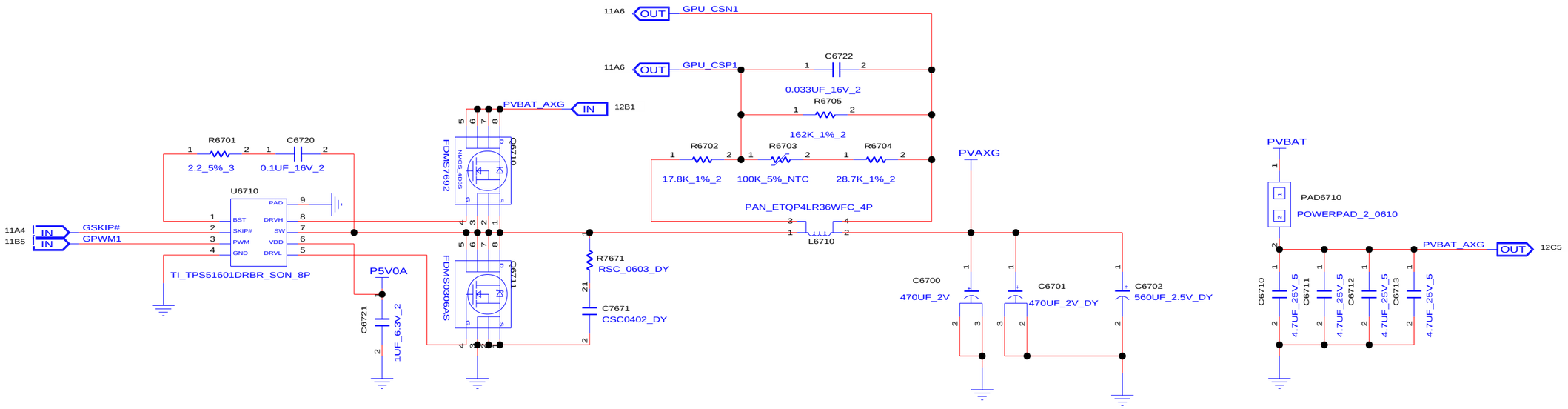

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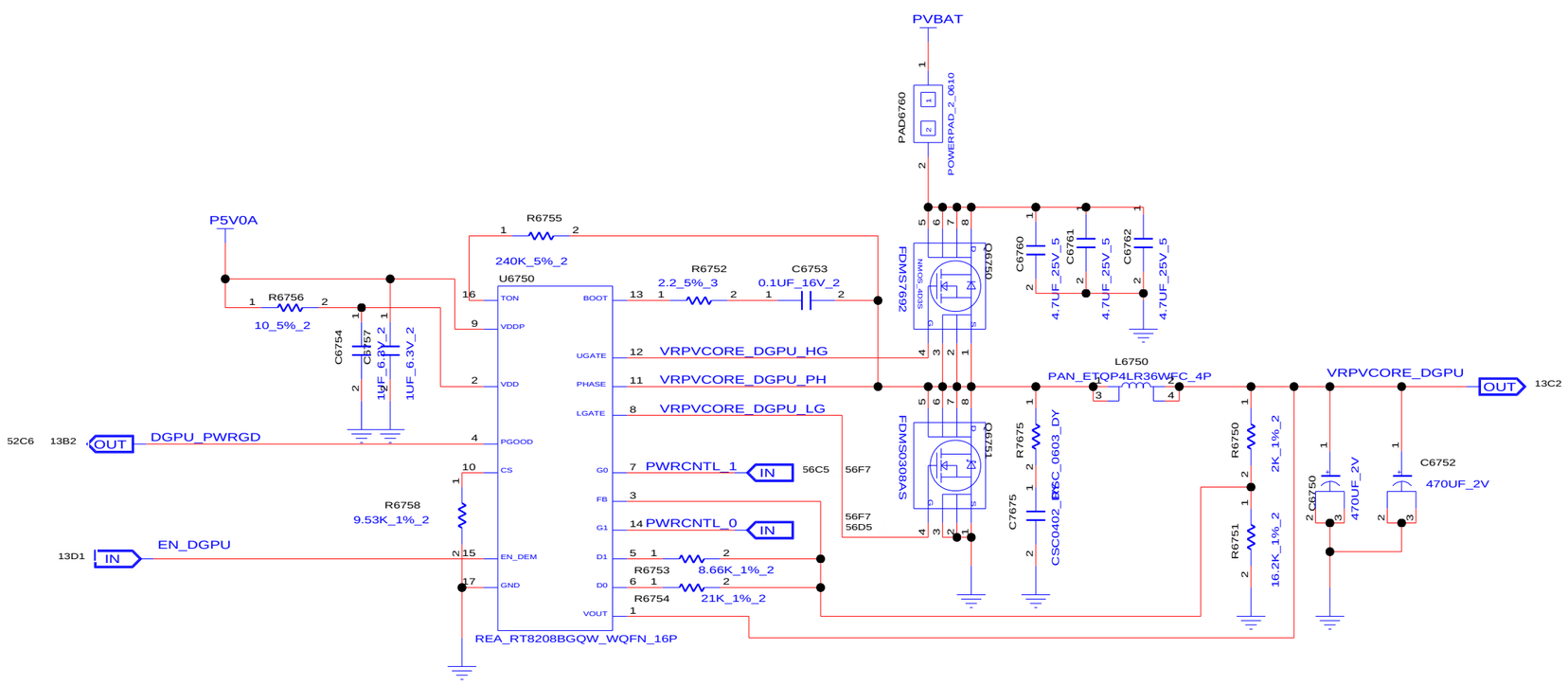
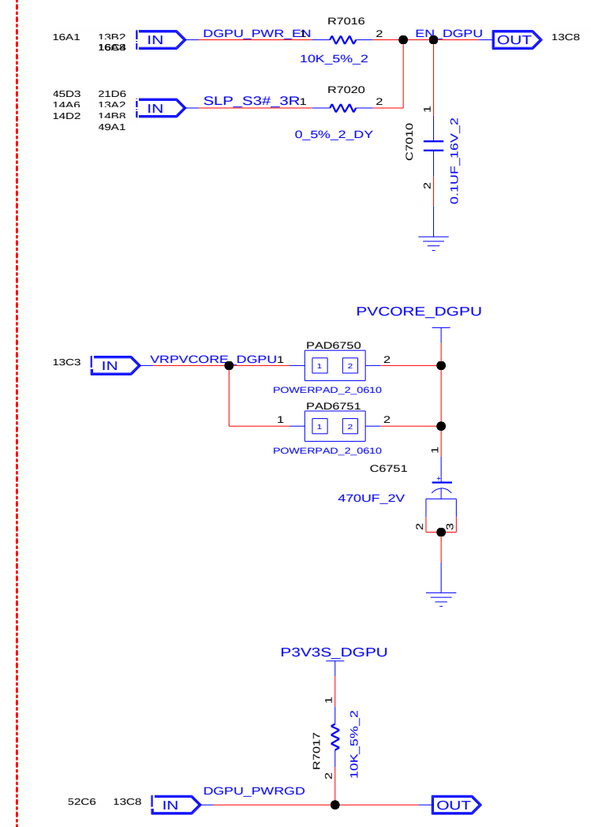
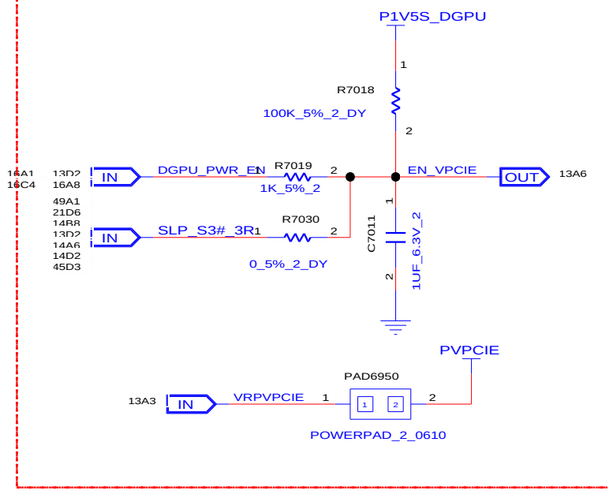
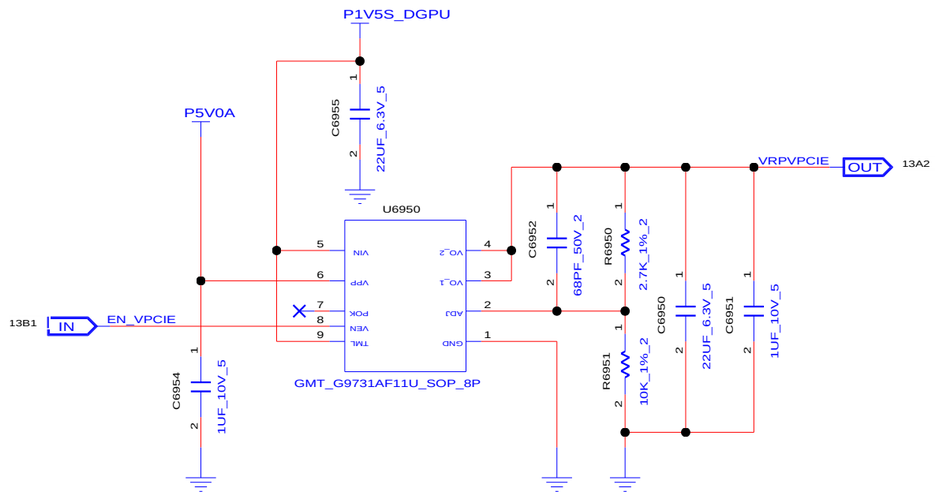




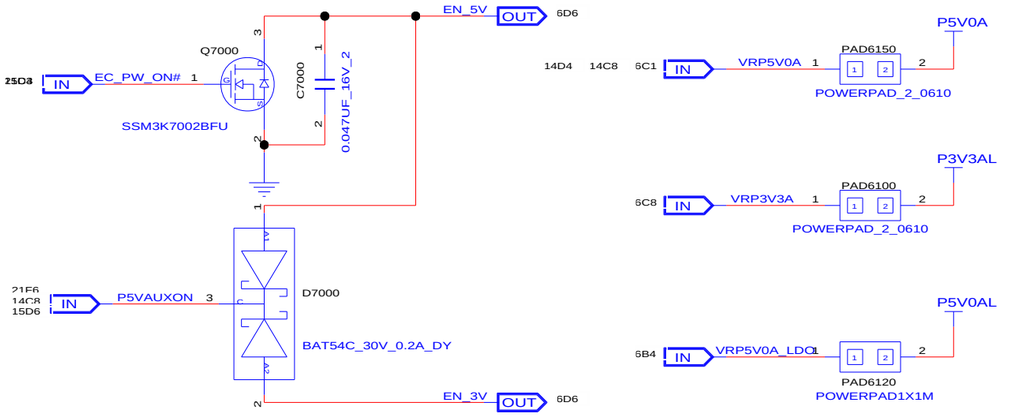


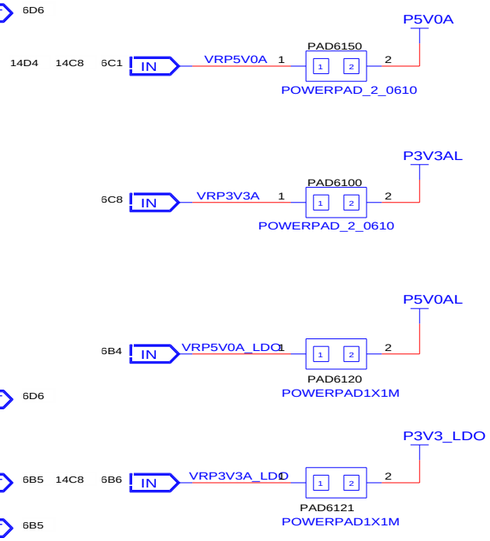
RT8208A		RT8208B		Output Voltage Equation
G0	G1	G0	G1	
0	0	1	1	$V_{OUT} = \frac{R1+R2}{R2} \times 0.75$
1	0	0	1	$V_{OUT} = \frac{R1+(R2//R3)}{(R2//R3)} \times 0.75$
0	1	1	0	$V_{OUT} = \frac{R1+(R2//R4)}{(R2//R4)} \times 0.75$
1	1	0	0	$V_{OUT} = \frac{R1+(R2//R3//R4)}{(R2//R3//R4)} \times 0.75$

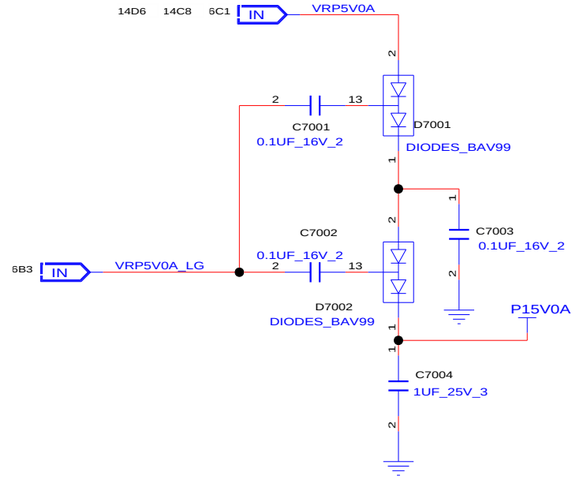
P.S. R6750(R1) R6751(R2) R6753(R3) R6754(R4)



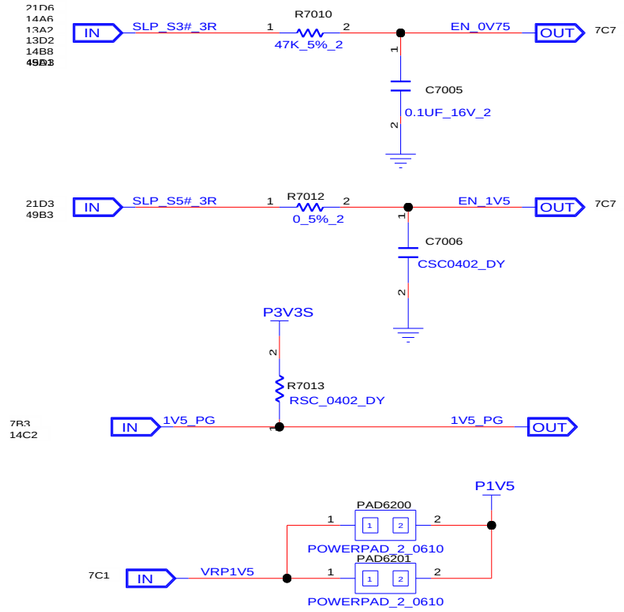
3V & 5V



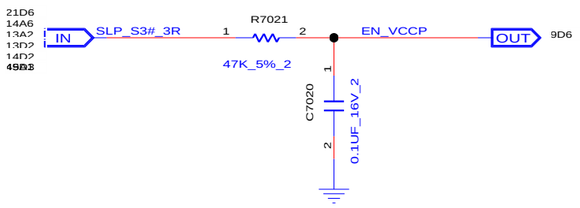


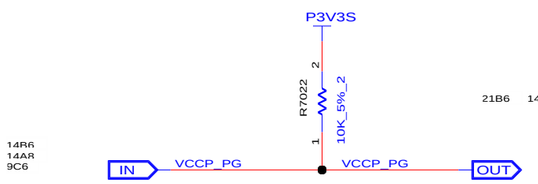


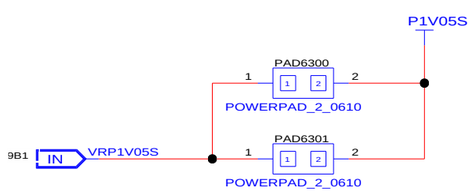
DDR_P1V5



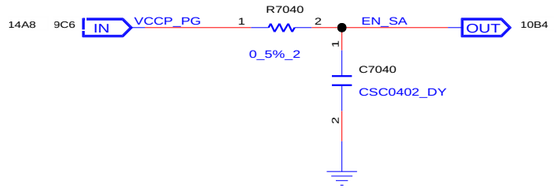
VCCIO

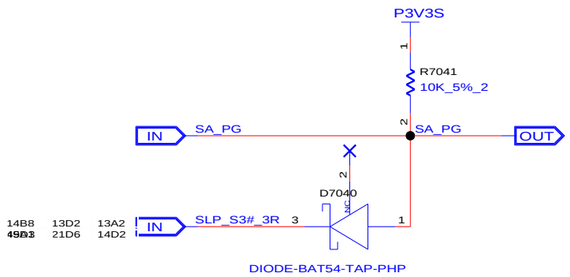


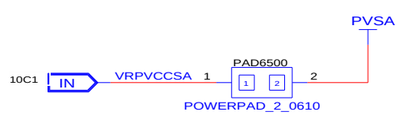




VCCSA

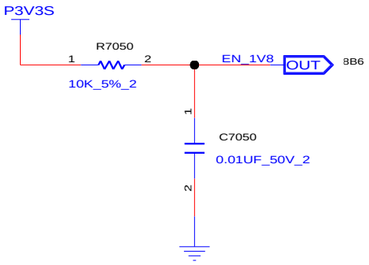


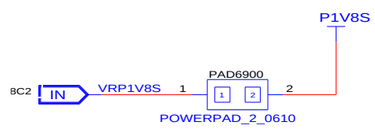




DGPU

P1V8S





INVENTEC			
TITLE: MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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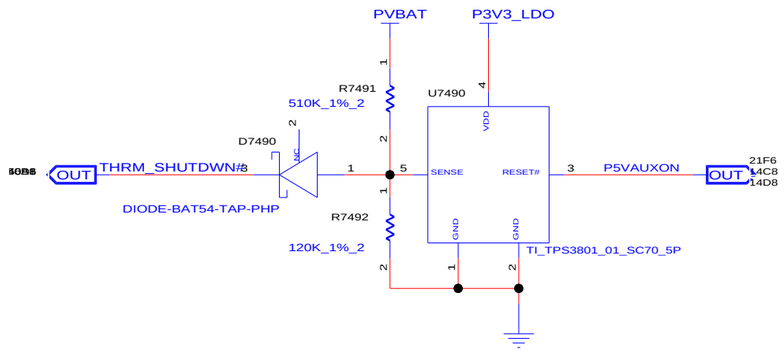

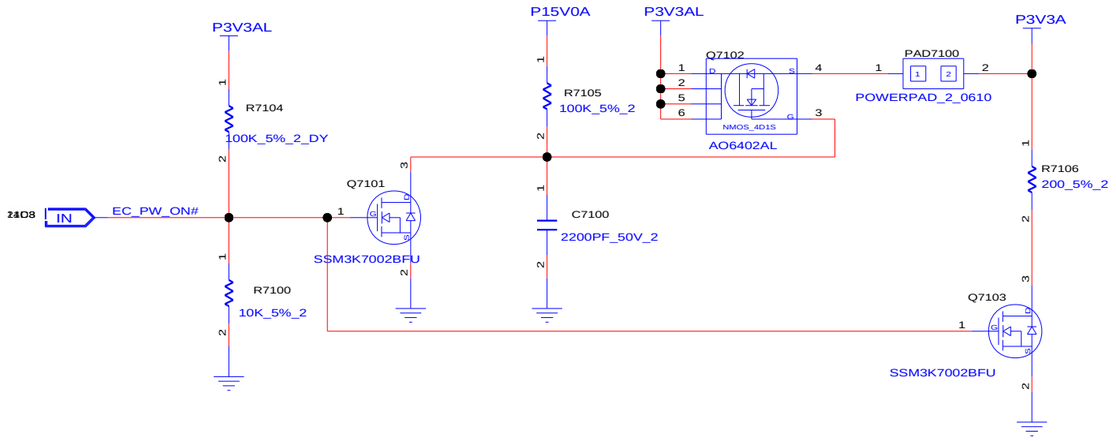

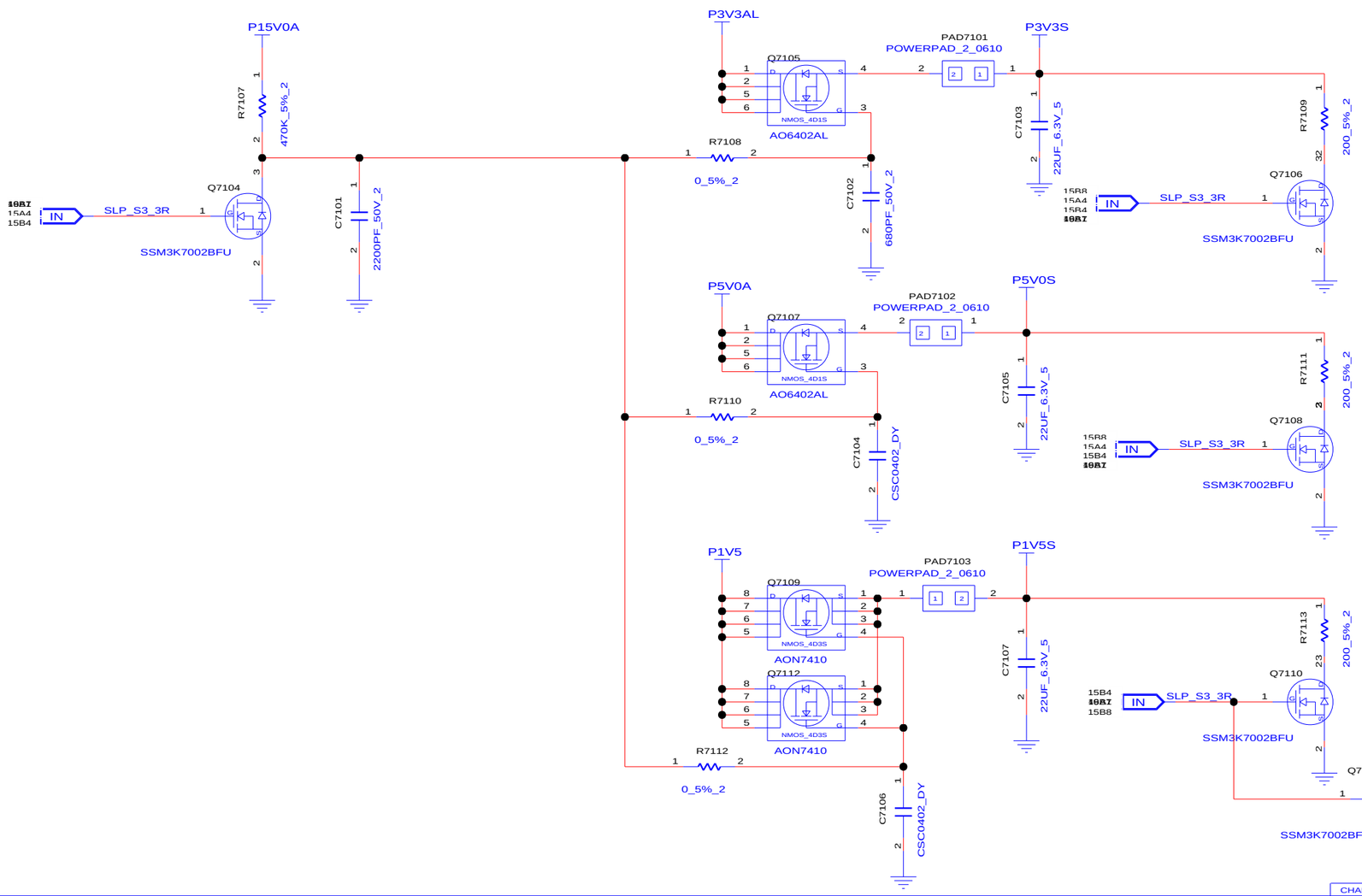

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
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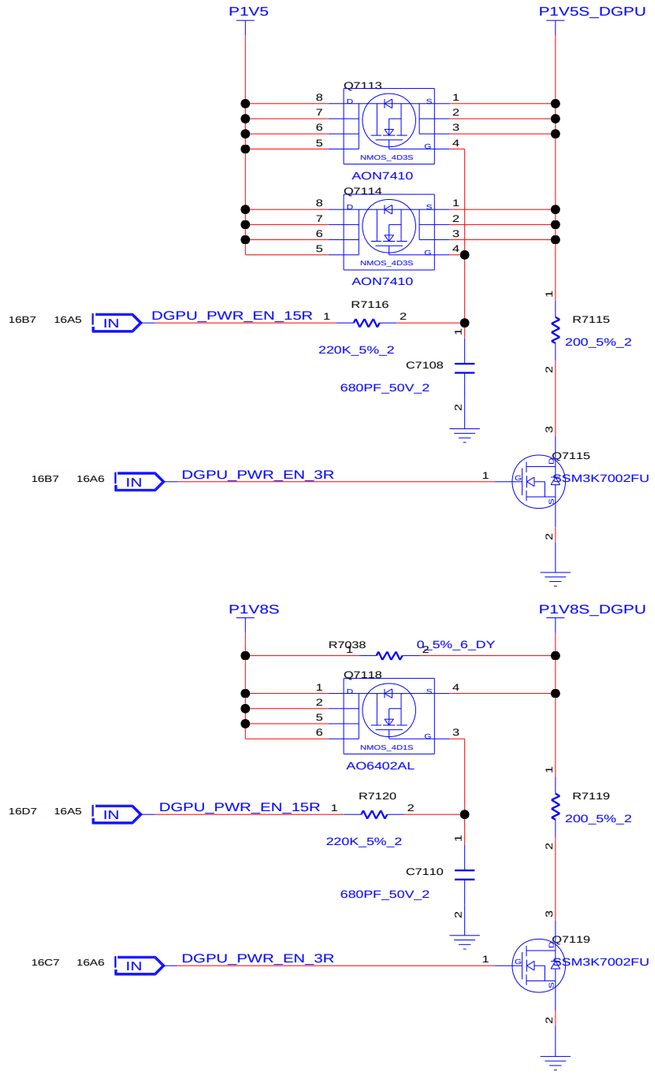
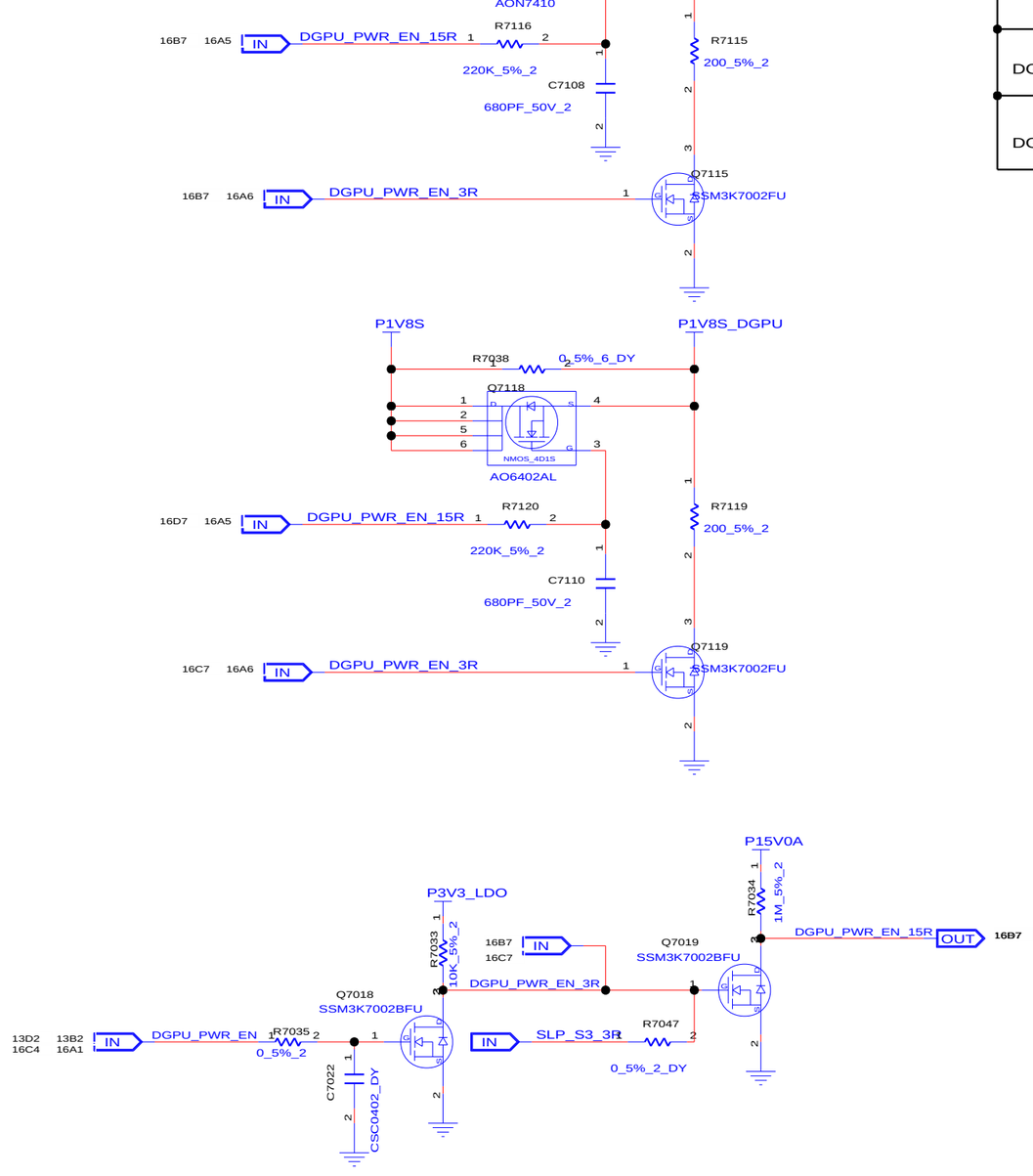
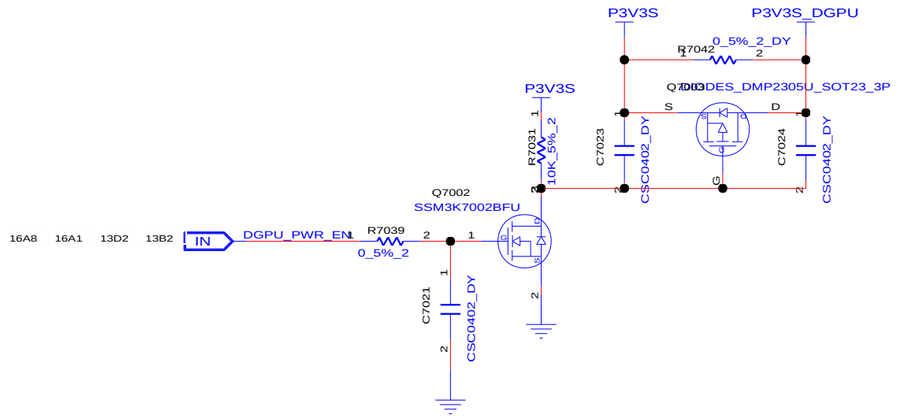
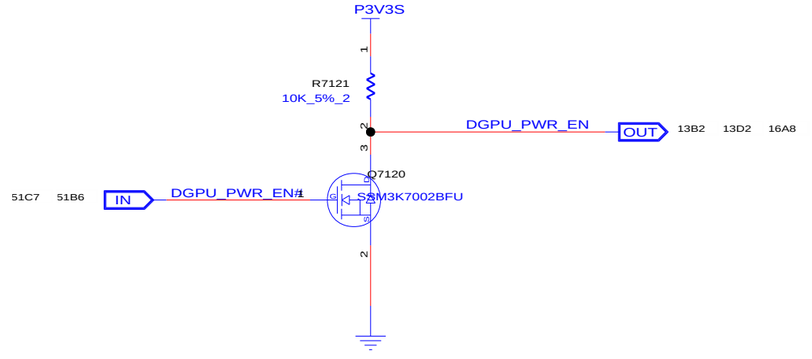




POWER EXPRESS

	DURING RESET	AFTER RESET	
DGPU_PWR_EN#	HIGH	HIGH	0 : DGPU POWER SWITCH TURNED ON 1 : POWER SWITCH TURNED OFF
DGPU_PWRGD			0 : DGPU POWER IS NOT STABLE 1 : DGPU POWER IS STABLE
DGPU_HOLD_RST#	LOW	LOW	0 : KEEP DGPU IN RESET 1 : RESET IS RELEASED





INVENTEC

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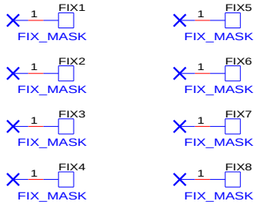
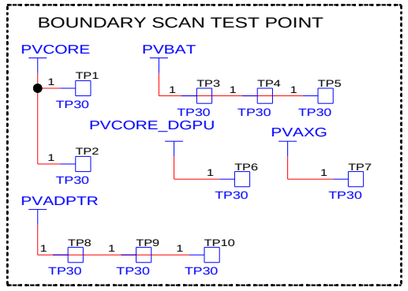
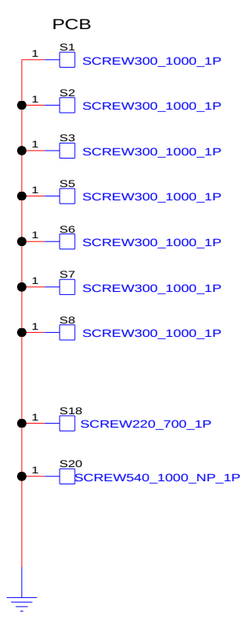
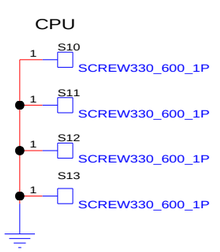
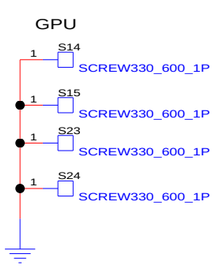
REFERENCE 0~49(PCB SCREW)

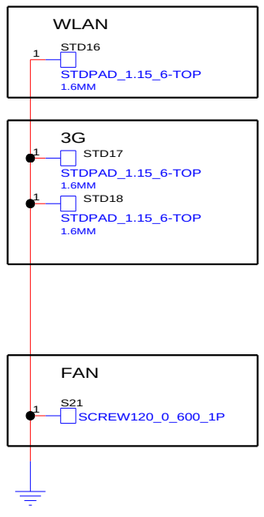












INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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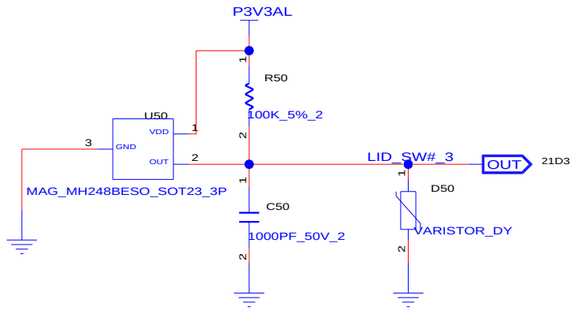
REFERENCE 50-99(HALL SENSOR)



INVENTEC

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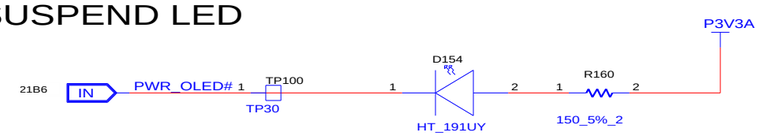
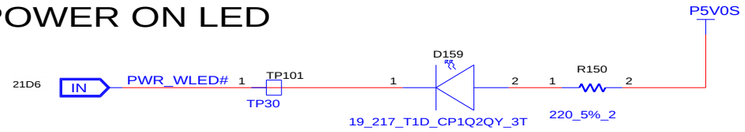
REFERENCE 100~199(LED)

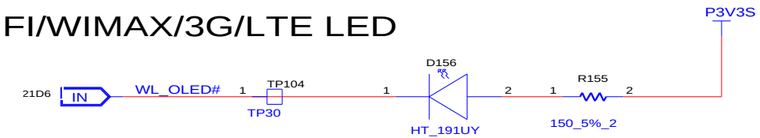
SUSPEND LED



POWER ON LED



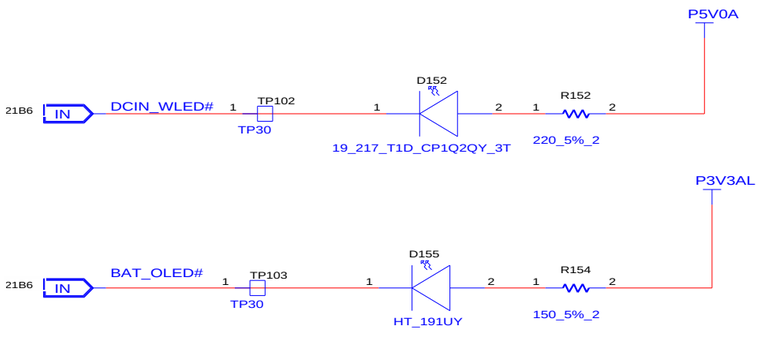
WIFI/WIMAX/3G/LTE LED



DC IN / BATTERY CHARGE LED

D152 BRIGHT:BOTH AC-ADAPTER IS PLUGGED IN AND BATTERY IS FULL CHARGED

D155 BRIGHT:WHILE CHARGING BATTERY FROM AC-ADAPTER
BLINK:LOW BATTERY



INVENTEC

TITLE
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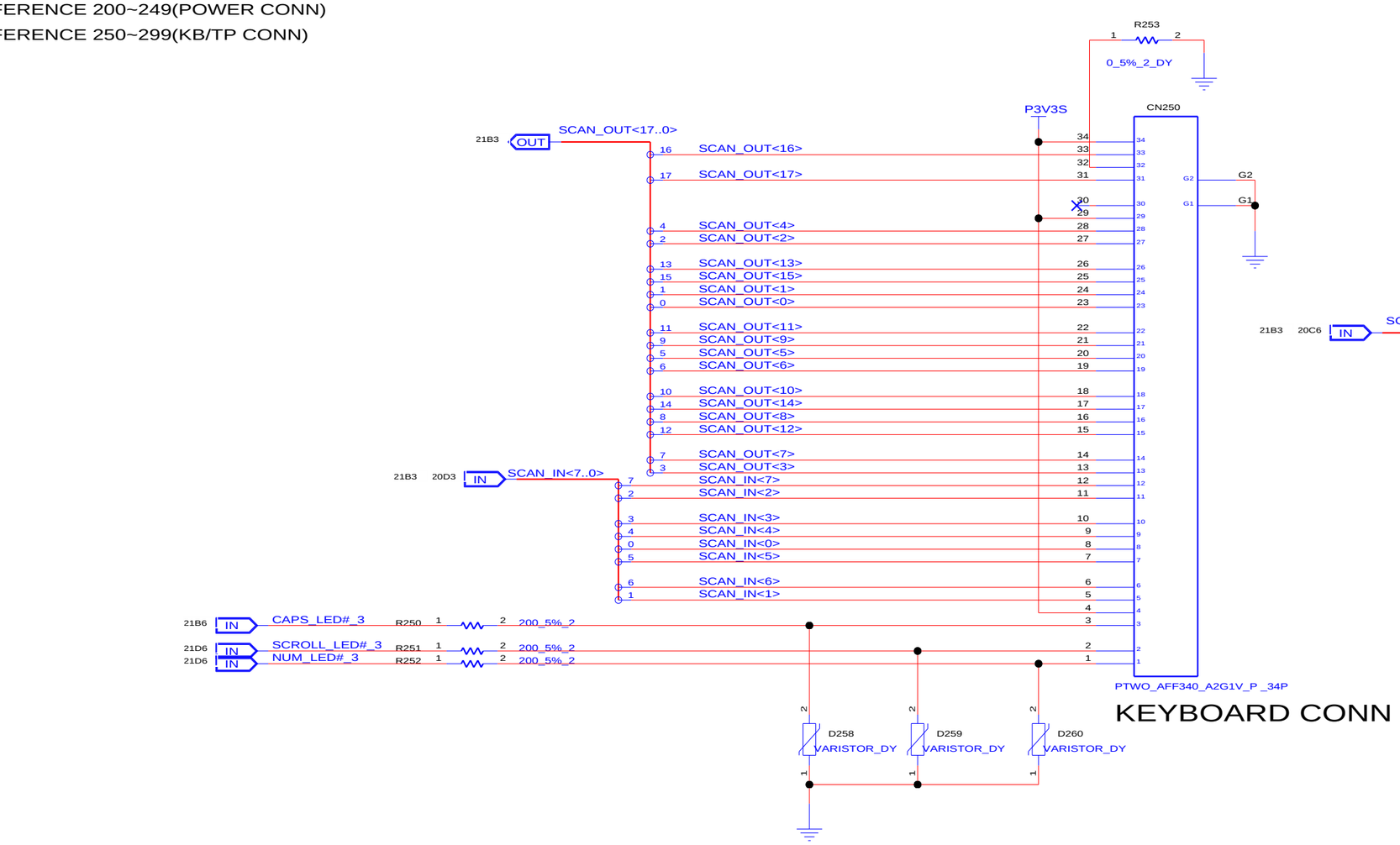
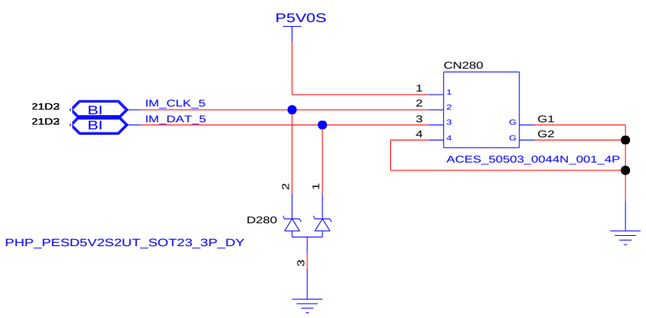
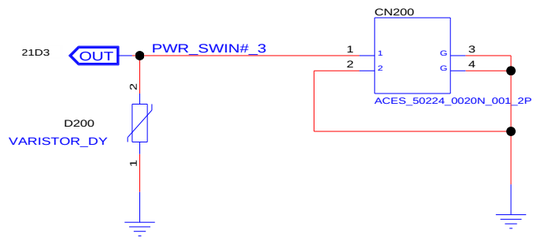
REFERENCE 200~249(POWER CONN)
REFERENCE 250~299(KB/TP CONN)



KEYBOARD CONN



TOUCHPAD CONN



POWER CONN

INVENTEC

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A3	CS	1310xxxxx-0-0	X01

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REFERENCE 300~389(KBC)

EC_SMB1	EC_SMB2	EC_SMB3
1.BATTERY	1.CHARGE	
	2.GPU THERMAL	
	3.CEC	

MXIC_MX25L3206EM2I_12G_SOP_8P

MXIC_MX25L3206EM2I_12G_SOP_8P_DY

WINB_NPCE885LA0DX_LQFP_128P

POWERPAD1X1M

SSM3K7002BFU

DIODE-BAT54-TAP-PHP

FBM_11_160808_121T

AGND_KBC

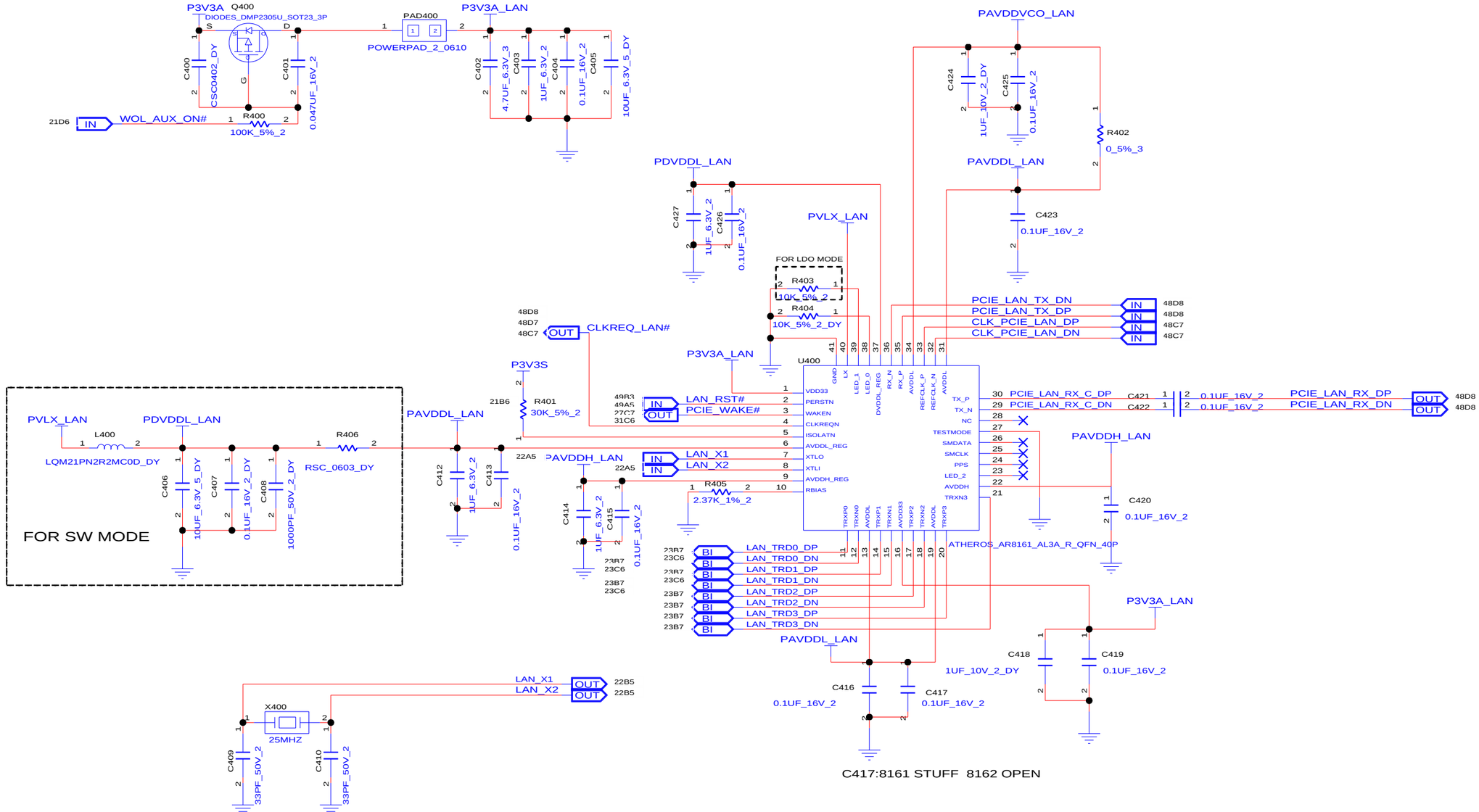
P1V05S

SIZE	CODE	DOC.NUMBER	REV
C	CS	1310xxxxx-0-0	X01

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

REFERENCE 400~499(LAN)



C417:8161 STUFF 8162 OPEN

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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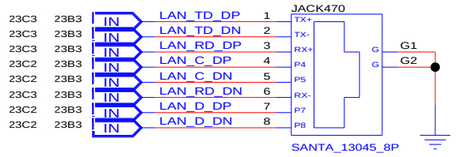
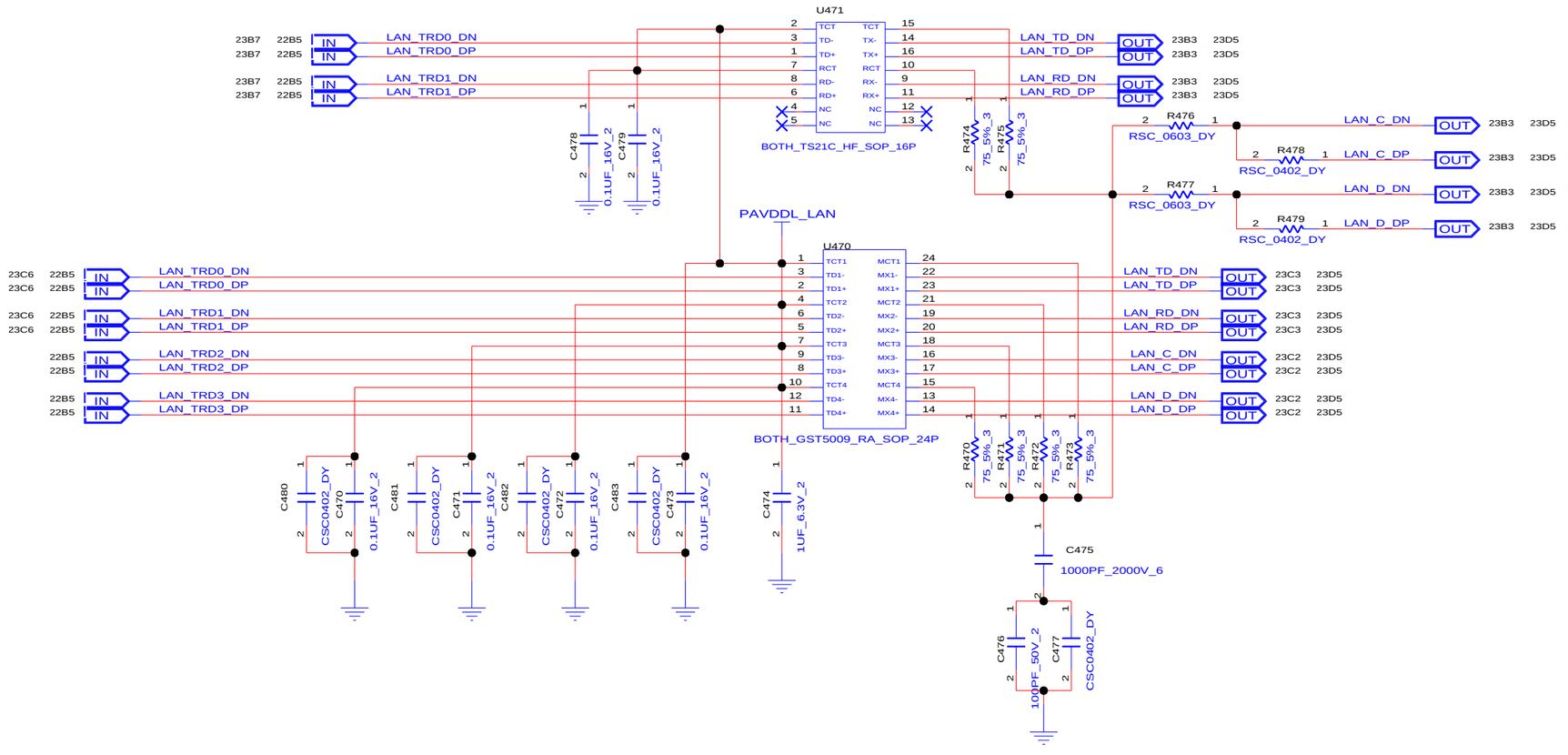
REFERENCE 400~499(LAN)





REFERENCE 500~549(AUDIO CODEC)

U500

REA_ALC269Q_VB6_CGT_QFN_48P

ANALOG

DIGITAL

(THERMAL PAD 4X4 VIAS)

RESERVE FOR EMI

CLOSE TO PIN27

CLOSE TO PIN13

TIED UNDER OR NEAR CODEC

BLM18PG121SN1(6014B0041601_0603)

P5V0S

P5V0S_PVDD

P5V0S_AUDIO_AVDD

P3V3S

P3V3A

AGND_AUDIO

HP_R

HP_L

MIC_REF_L

MIC_REF_R

MIC_R

MIC_L

MICS

HPS

SPK_OUT_L_P

SPK_OUT_L_N

SPK_OUT_R_N

SPK_OUT_R_P

MIC_IN_DATA

MIC_IN_CLK

MIC_IN_CLK_R

PCSPKR_PCH_3

HDA_3S_RST#

HDA_3S_SYNC

HDA_R_SDIN0

HDA_3S_SDIN0

HDA_R_BITCLK

HDA_3S_BITCLK

HDA_3S_SDOUT

EC_MUTE#

PAD500 POWERPAD1X1M

C503	2.2UF_6.3V_3	C512	10UF_6.3V_3
C519	2.2UF_6.3V_3	C513	0.1UF_16V_2
C502	2.2UF_6.3V_3	C532	10UF_6.3V_3_DY
C506	0.1UF_16V_2_DY	C505	4.7UF_6.3V_3
C507	0.1UF_16V_2	C536	4.7UF_6.3V_3
C500	0.1UF_16V_2	C501	0.1UF_16V_2
C504	4.7UF_6.3V_3	C529	4.7UF_6.3V_3
C531	0.1UF_16V_2	C514	1000PF_50V_2
C515	1000PF_50V_2	C516	1000PF_50V_2
C517	1000PF_50V_2	C508	1UF_6.3V_2
C509	0.1UF_16V_2	C520	0.1UF_16V_2
C521	100PF_50V_2	C518	22PF_50V_2_DY
C510	0.1UF_16V_2	C522	1UF_6.3V_2

R515	0_5%_3	R516	0_5%_3
R512	0_5%_3	R511	0_5%_3
R510	0_5%_3	R509	0_5%_3
R514	20K_1%_2	R500	20K_1%_2
R501	39.2K_1%_2	R505	100_5%_2
R507	47K_1%_2	R506	4.7K_1%_2
R502	22_5%_2	R503	0_5%_2

INVENTEC	
TITLE	MODEL,PROJECT,FUNCTION Block Diagram
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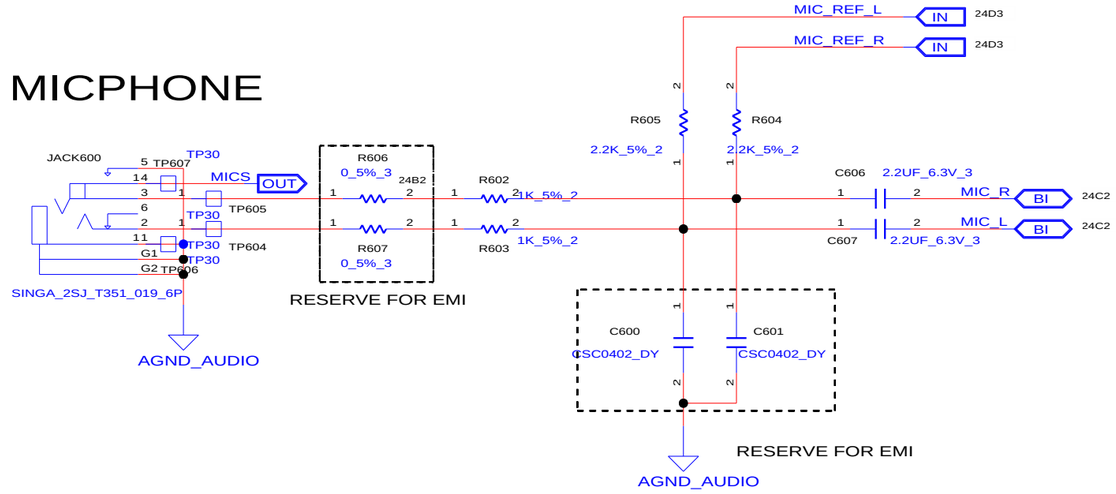
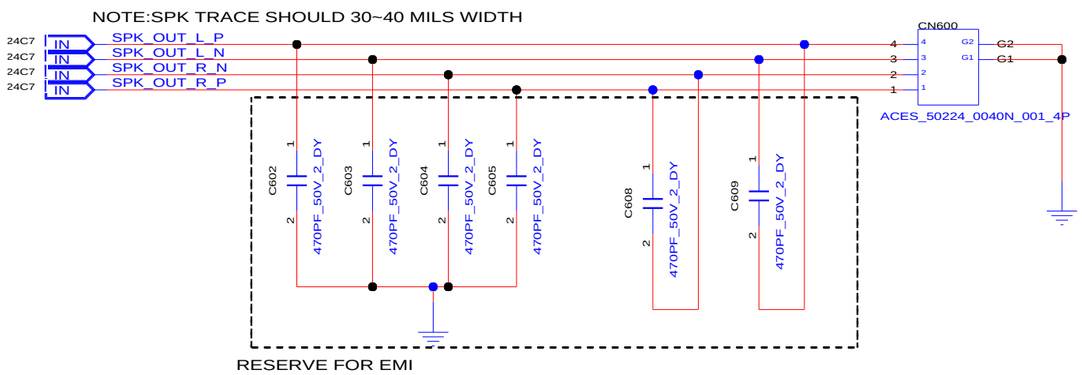
REFERCE 600~649(JACK/MIC/SPEAKER)

AUDIO JACKS

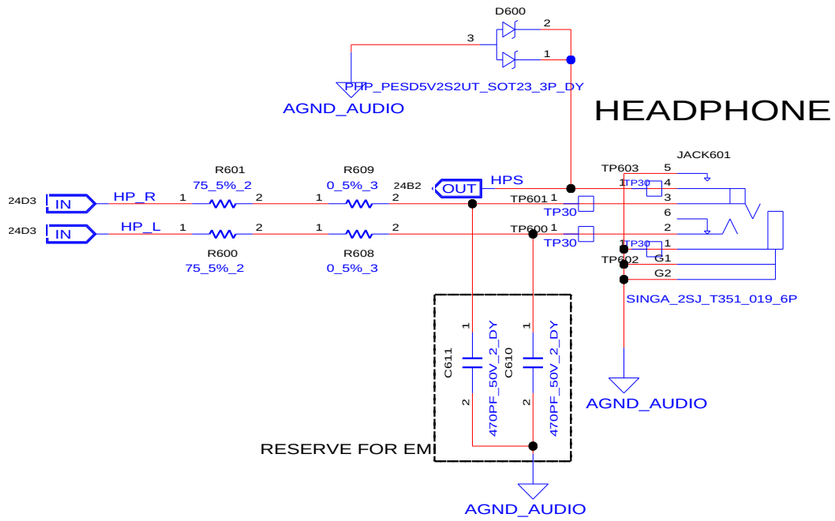
MICPHONE



INTERNAL SPEAKERS



HEADPHONE



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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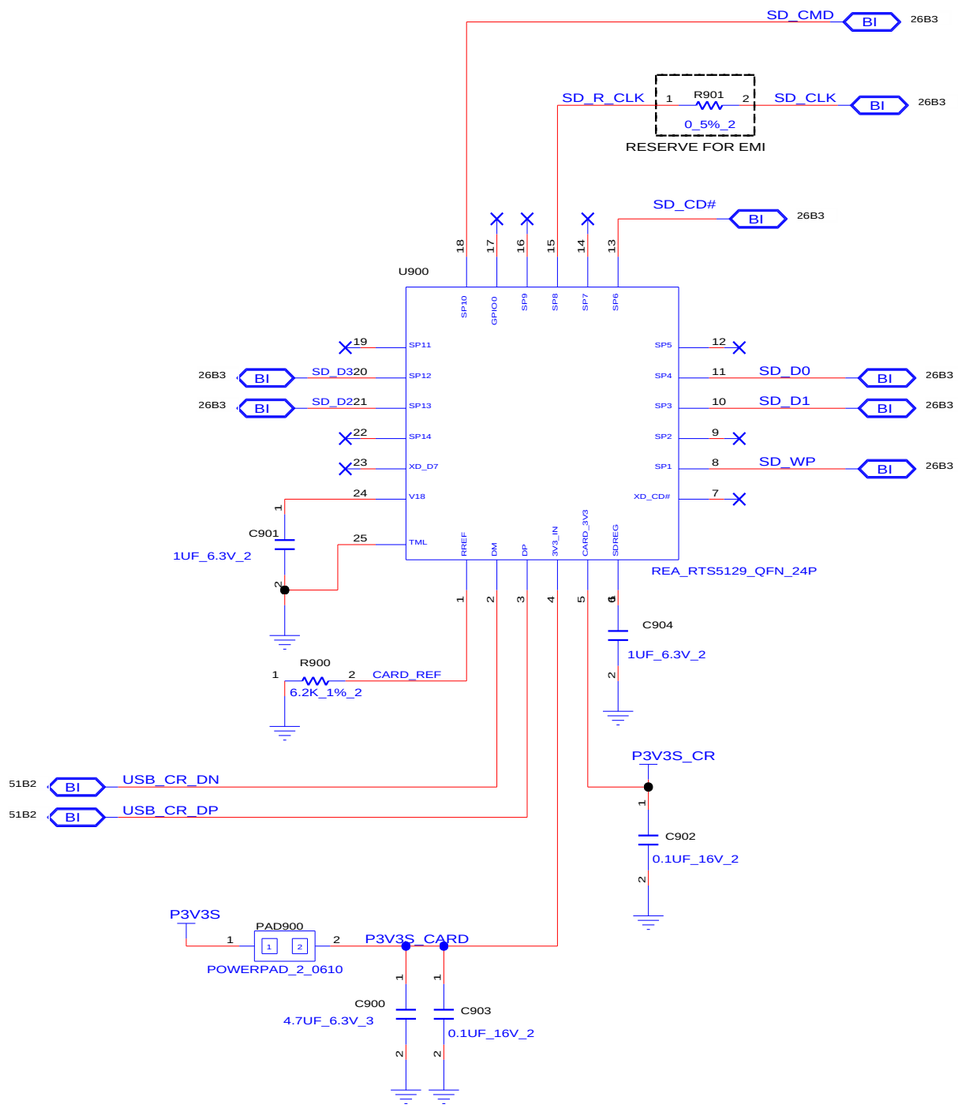
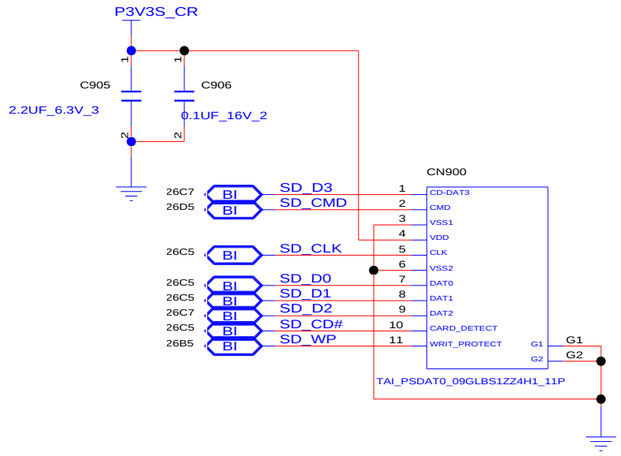
REFERNCE 900~999(CARDREADER)





INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
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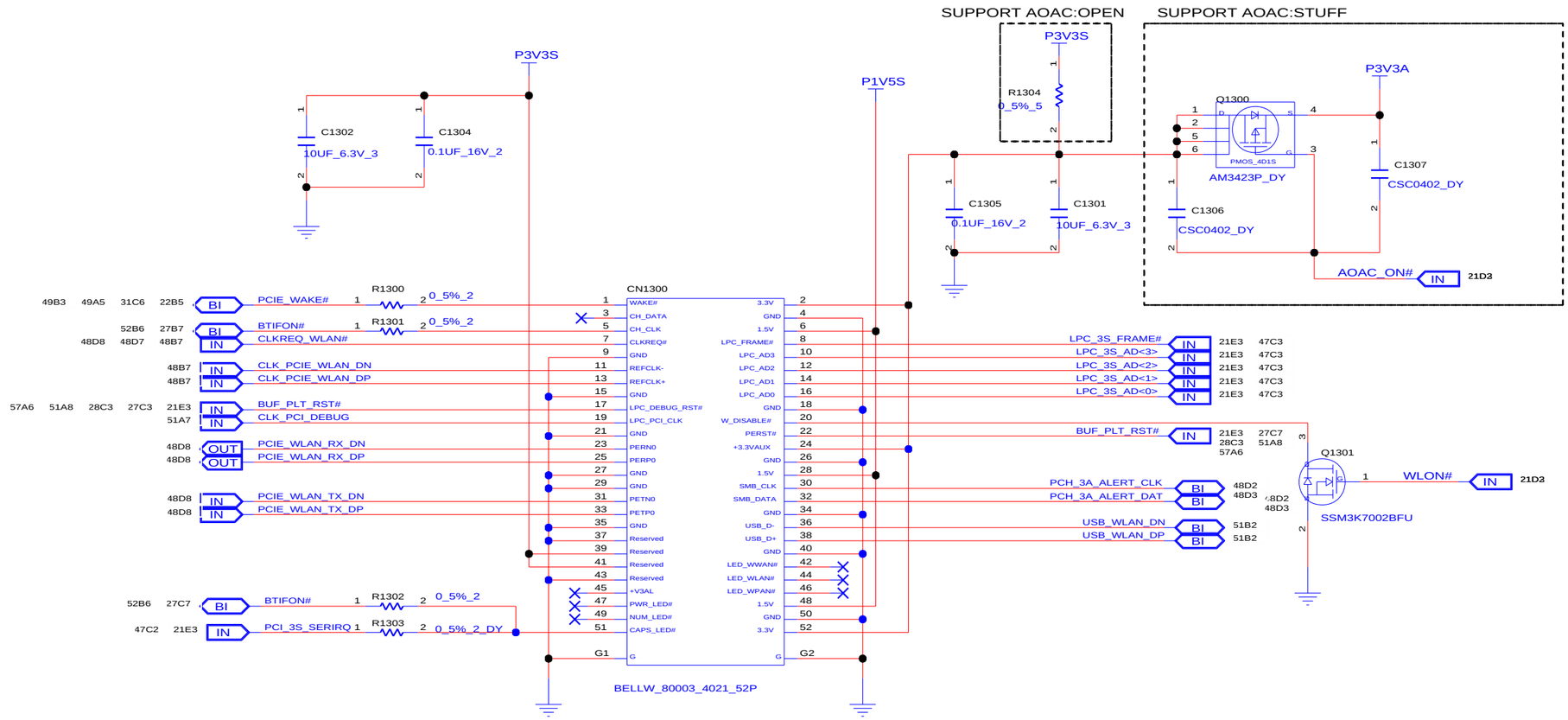
REFERENCE 1300~1349(WLAN)



MINI CARD 1(WLAN)

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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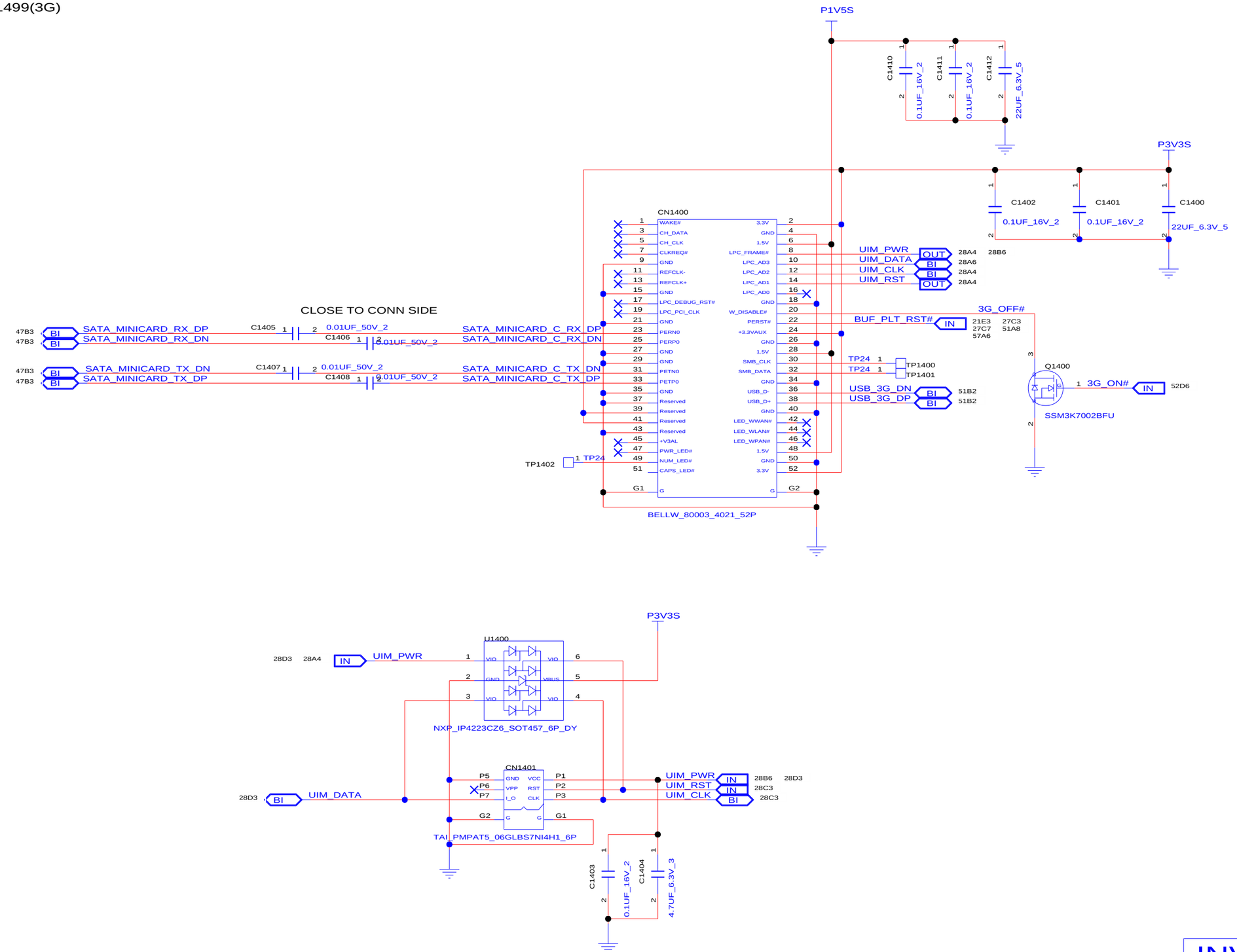
REFERENCE 1400~1499(3G)



INVENTEC							
TITLE: MODEL,PROJECT,FUNCTION Block Diagram							
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01				
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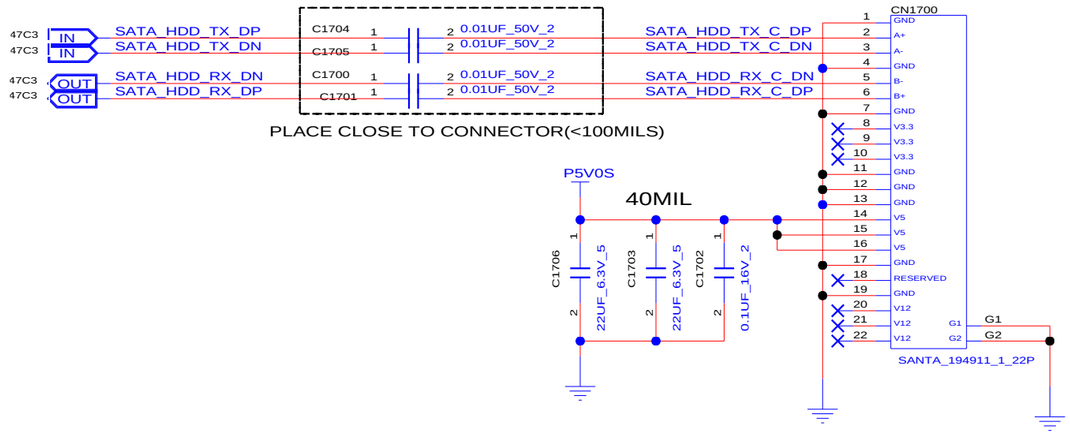
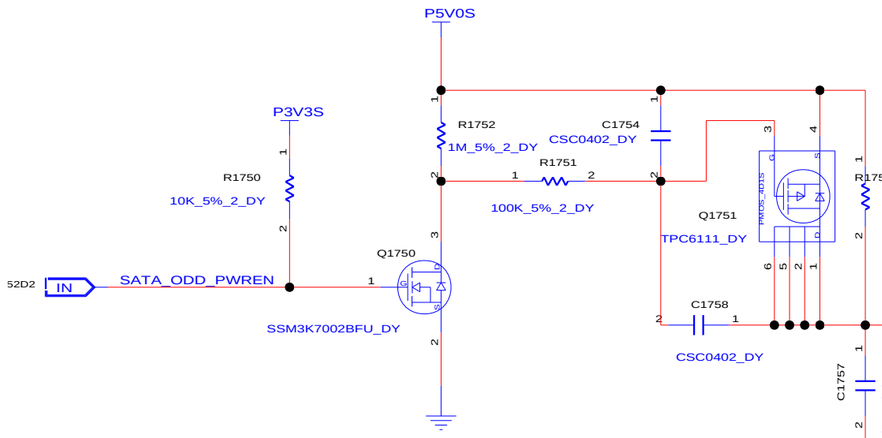
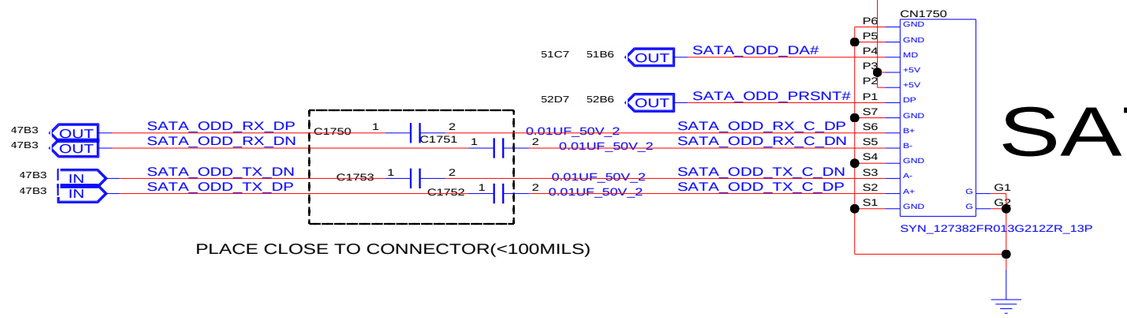
REFERENCE 1700~1749(HDD)
REFERENCE 1750~1799(ODD)

SATA HDD





SATA ODD



INVENTEC

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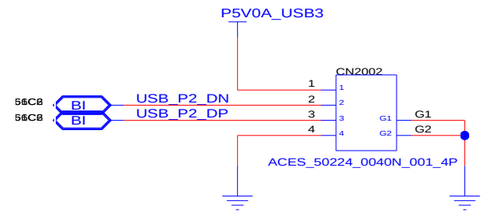
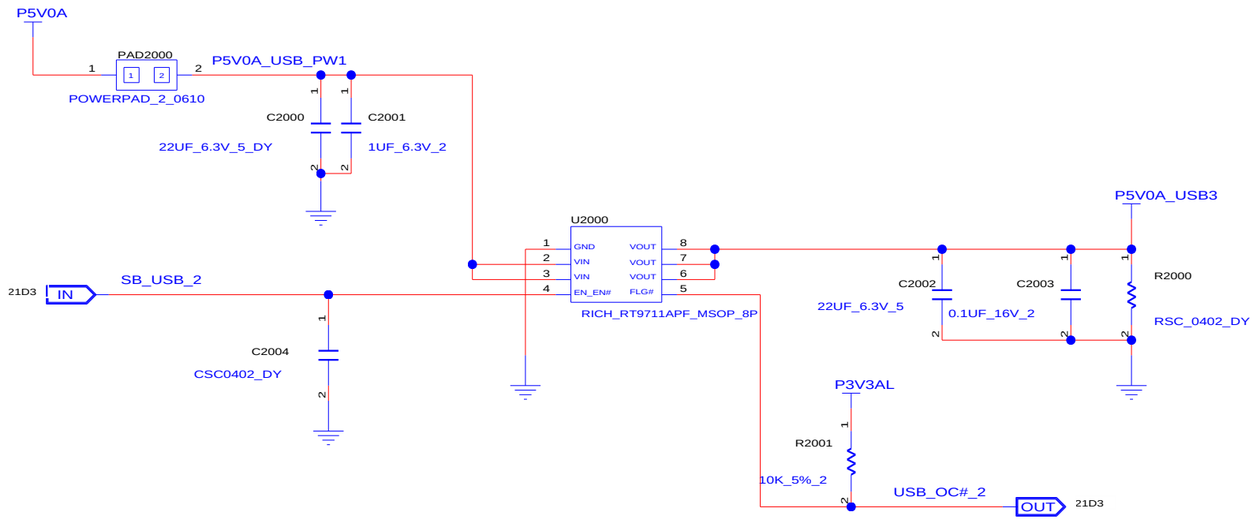
REFERENCE 2000~2099(USB)





INVENTEC			
TITLE: MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX	DATE 21-OCT-2002	SHEET 30 of 68	

REFERENCE 2400~2499(USB3.0)

P1V05_USB3
C2417 0.01UF_50V_2
C2418 0.01UF_50V_2
C2419 0.01UF_50V_2
C2420 0.01UF_50V_2
C2421 0.01UF_50V_2
C2422 0.01UF_50V_2
C2423 0.1UF_16V_2
C2424 0.1UF_16V_2
C2425 0.1UF_16V_2

P3V3A
R2424 10K_5%_2
R2427 220K_5%_2
Q2403 DIODES_DMP2305U_SOT23_3P
C2472 CSC0402_DY
C2473 CSC0402_DY
P3V3_USB3
C2400 CSC0402_DY
C2401 0.1UF_16V_2
C2402 0.1UF_16V_2
C2403 0.01UF_50V_2
C2404 0.01UF_50V_2
C2405 0.01UF_50V_2
C2470 0.01UF_50V_2
C2471 10UF_6.3V_3
31A5 21D6 IN USB30_PWR_EN
Q2402 SSM3K7002BFU

P3V3_USB3 P1V05_USB3 P3V3_USB30_AVDD
U2400
VDD33 12 22 34 43
VDD10 6 9 21 30 33 39 42
AVDD33 3 25

48B7 IN CLK_PCIE_USB3_DP → PECLKP 1
48B7 IN CLK_PCIE_USB3_DN → PECLKN 2
C2409 0.1UF_16V_2
48D8 OUT PCIE_USB3_RX_DP → PETXP 4
PCIE_USB3_RX_C_DP
48D8 OUT PCIE_USB3_RX_DN → PETXN 5
PCIE_USB3_RX_C_DN
C2410 0.1UF_16V_2
48D8 IN PCIE_USB3_TX_DP → PERXP 7
48D8 IN PCIE_USB3_TX_DN → PERXN 8

P3V3_USB3
R4754 10K_5%_2 CLKREQ_USB3# IN 31B8 48B7
R4955 10K_5%_2 USB3_SMI# IN 31C6 51B6
51A7 36B2 41C7 IN PLT_RST# → PERSTB 47
49B3 49A5 27C7 22B5 OUT PCIE_WAKE# → PEWAKEB 48
31B6 IN CLKREQ_IC_USB3# → PECREQB 10
31C7 51B6 OUT USB3_SMI# → SMIB 46
PONRSTB 11
31A6 OUT USB3_SCLK → SPISCK 15
31A8 OUT USB3_CS# → SPICSB 14
31A6 OUT USB3_SI → SPISI 16
31A8 IN USB3_SO → SPISO 13

P3V3_USB3
R2406 10K_5%_2
D2400 DIODE-BAT54-TAP-PHP
C2411 1UF_6.3V_2
USB3_XT1 → XT1 24
X2400 24MHZ
USB3_XT2 → XT2 23
C2413 12PF_50V_2
C2412 12PF_50V_2
IC(L) 27

31C7 48B7 OUT CLKREQ_USB3# R2405 0_5%_2 CLKREQ_IC_USB3# IN 31C6

U3TXDP2 37 USB3_IC_TX2_DP BI 33B5
U3TXDN2 38 USB3_IC_TX2_DN BI 33B5
U2DM2 45 USB2_IC_TX2_DN BI 33C5
U2DP2 44 USB2_IC_TX2_DP BI 33C5
U3RXDP2 40 USB3_IC_RX2_DP BI 33B5
U3RXDN2 41 USB3_IC_RX2_DN BI 33B5
OCI2B 17 R2415 10K_5%_2 P3V3_USB3
OCI1B 19 R2416 10K_5%_2
PPON2 18
PPON1 20
U3TXDP1 28 USB3_IC_TX1_DP BI 32D7
U3TXDN1 29 USB3_IC_TX1_DN BI 32D7
U2DM1 36 USB2_IC_TX1_DN BI 32B8
U2DP1 35 USB2_IC_TX1_DP BI 32B8
U3RXDP1 31 USB3_IC_RX1_DP BI 32D7
U3RXDN1 32 USB3_IC_RX1_DN BI 32D7
R2400 1.6K_1%_2
RREF 26
GND 49
RENESAS_UPD720202K8_BAA_A_QFN_48P

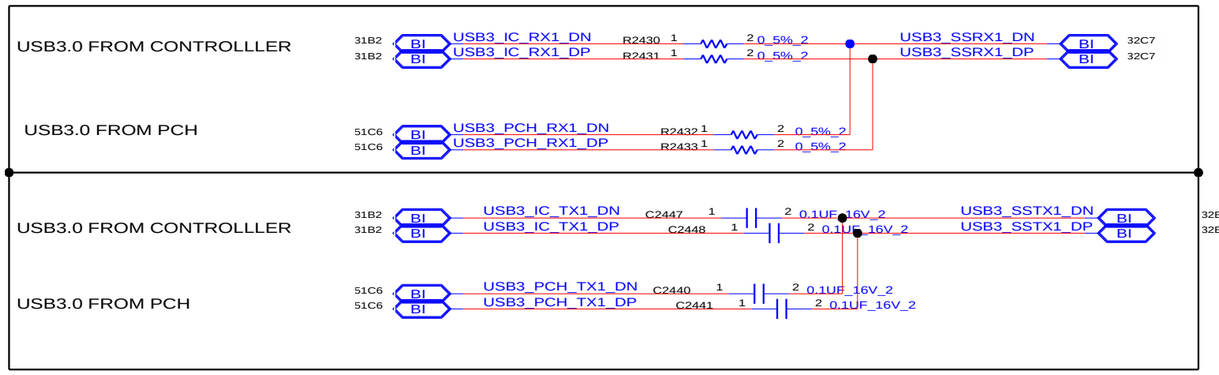
P3V3_USB3 P3V3_USB30_AVDD
L2400 BLM21PG600SN1D_3A
C2406 10UF_6.3V_3
C2408 0.1UF_16V_2
C2414 0.1UF_16V_2
C2415 0.01UF_50V_2
C2416 0.01UF_50V_2

P3V3_USB3
R2480 10K_5%_2
R2481 47K_5%_2
U2480
31B6 IN USB3_CS# → CS# 1
31B6 OUT USB3_SO → SO 2
WP# 3
GND 4
VCC 8
NC 7
SCLK 6 USB3_SCLK IN 31B6
SI 5 USB3_SI IN 31B6
MAC_MX25L5121EMC_20G_SOP_8P
P3V3_USB3
C2480 0.1UF_16V_2

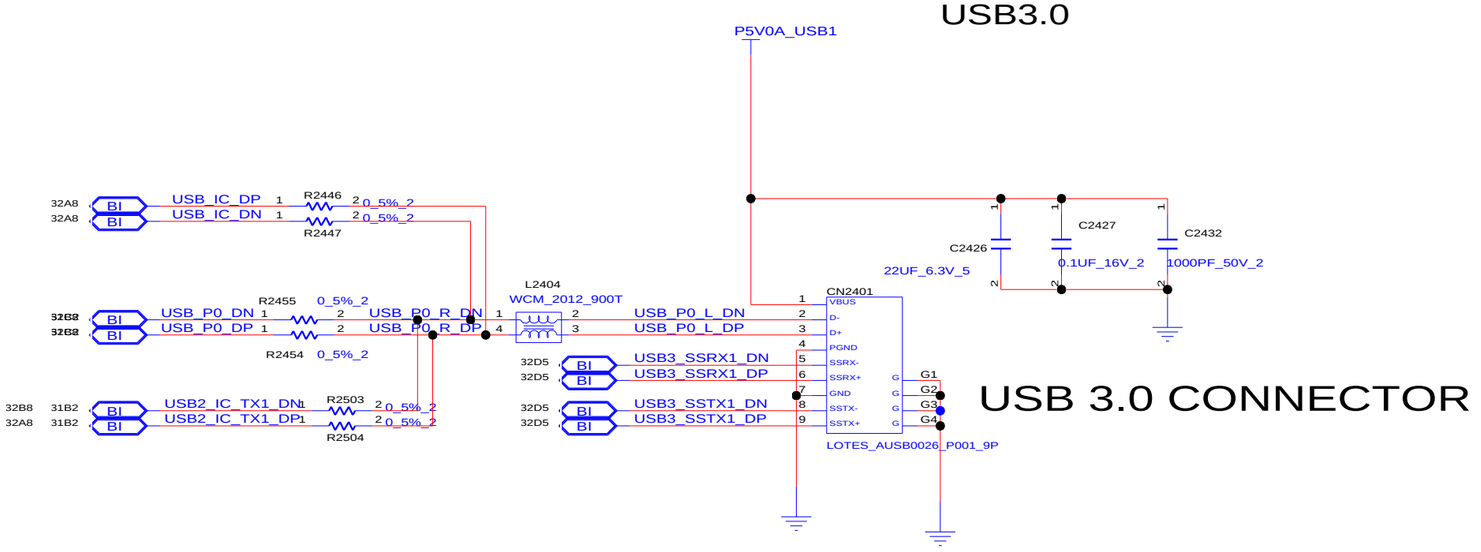
31D4 21D6 IN USB30_PWR_EN
P1V5 P5V0A
U2403
VIN 9 8 5
EN
POK 7
VCNTL 6
GND 1
FB 2
VOUT 3 4
ANPEC_APL5930KAI_TRG_SOP_8P
C2438 22UF_6.3V_5
C2435 1UF_6.3V_2
R2423 31.6K_1%_2
R2422 10K_1%_2
C2433 150PF_50V_2
TRACE WIDTH>20MILS
PAD2400 POWERPAD1X1M
P1V05_USB3
C2434 22UF_6.3V_5

INVENTEC			
TITLE: MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX	DATE 21-OCT-2002	SHEET 31 of 68	

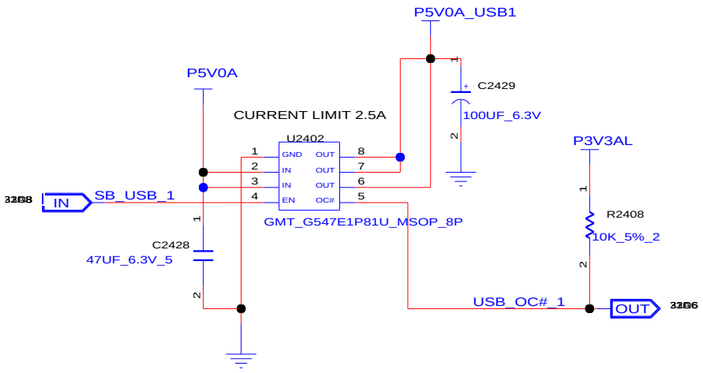
REFERENCE 2400~2499(USB3.0)

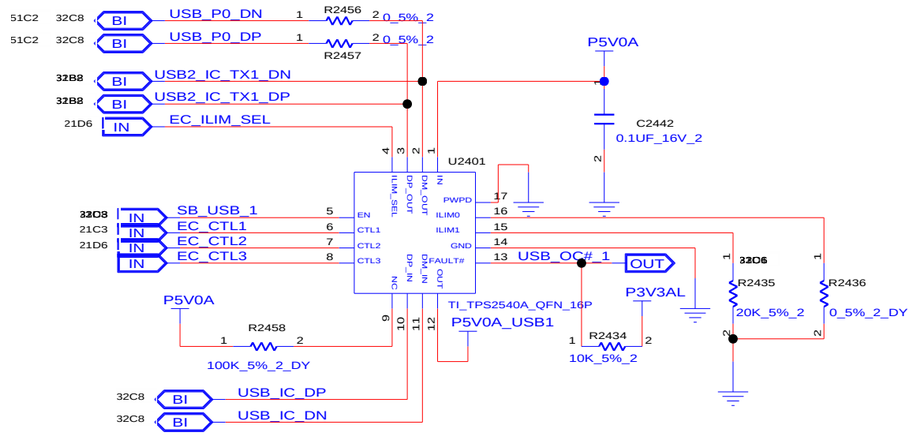


USB3.0



USB 3.0 CONNECTOR





CTL1	CTL2	CTL3	Mode
0	0	X	Dedicated Charging Port, Auto-detect
0	1	X	Dedicated Charging Port, BC Specification 1.1 Only
1	0	X	Dedicated Charging Port, Apple Only
1	1	0	Standard Downstream Port, USB 2.0 Mode
1	1	1	Charging Downstream Port, BC Specification 1.1

Table 3 – TPS2541 Control Truth Table

INVENTEC

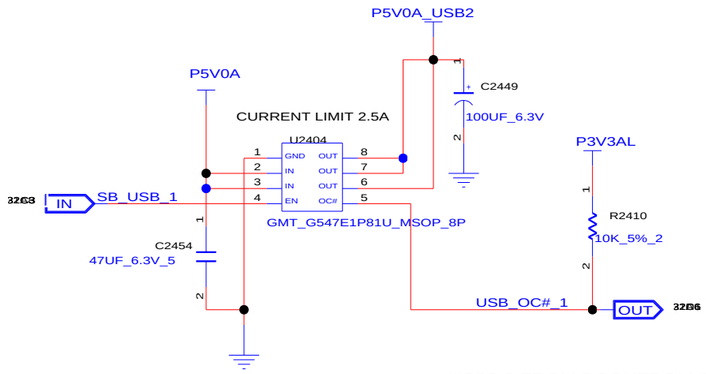
TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

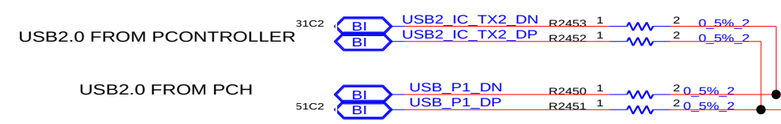
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

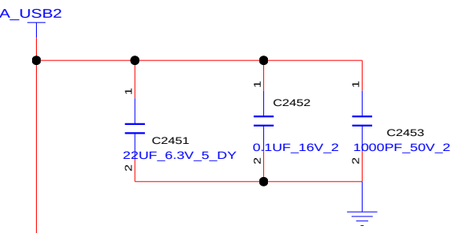
CHANGE by XXX | DATE 21-OCT-2002 | SHEET 32 of 68

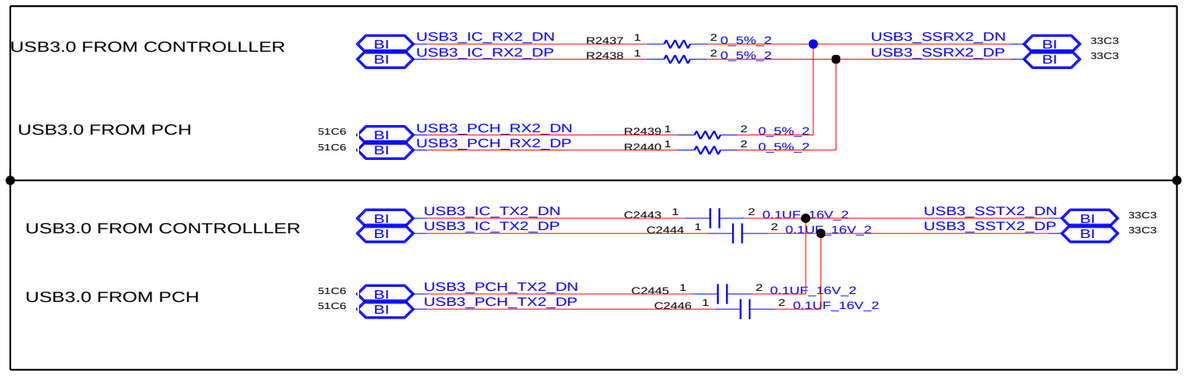
REFERENCE 2400~2499(USB3.0)

USB 3.0 CONNECTOR







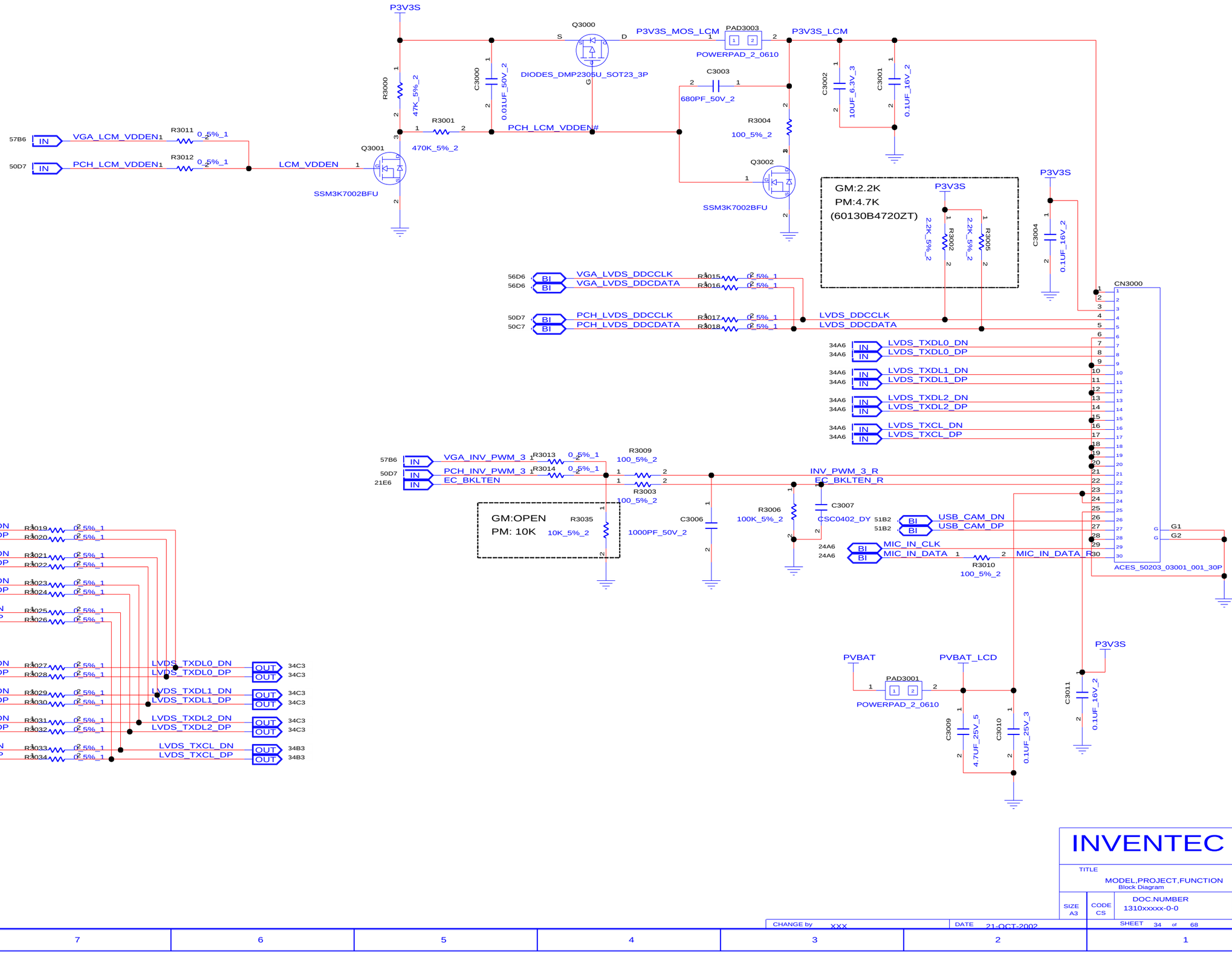


USB3.0

INVENTEC

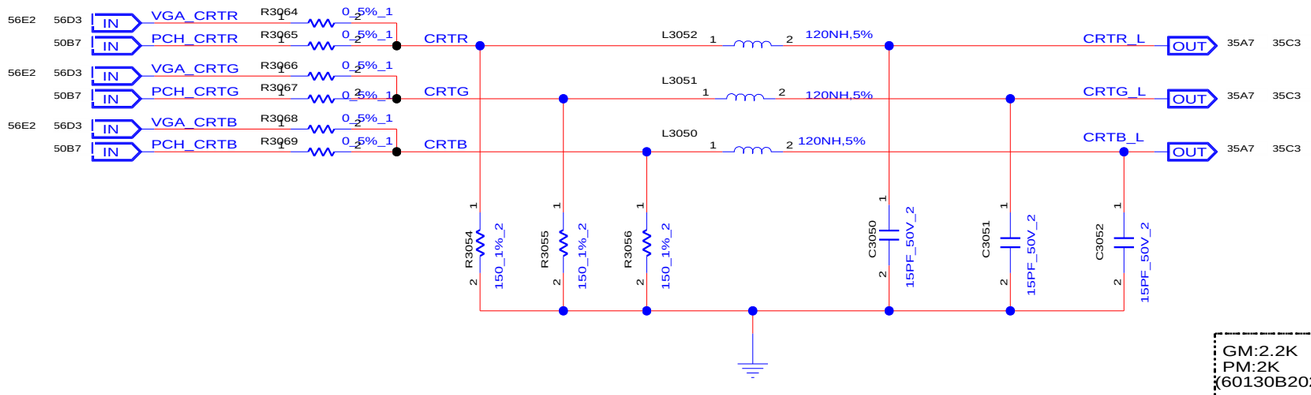
TITLE: MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX	DATE 21-OCT-2002	SHEET 33 of 68	

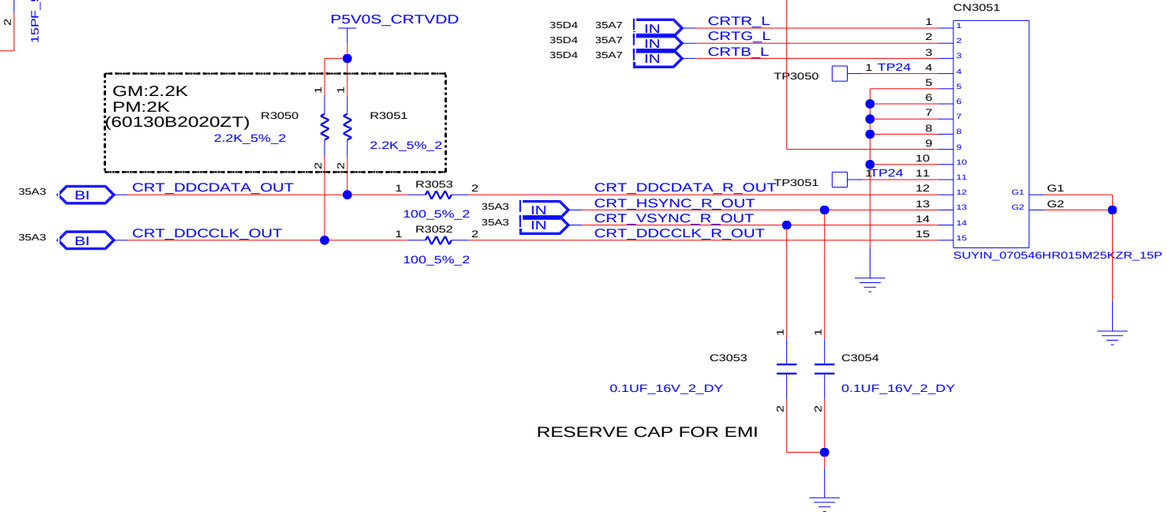
REFFERENCE 3000~3049(LCM)

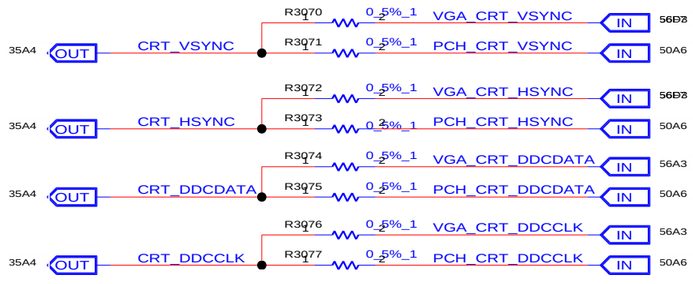


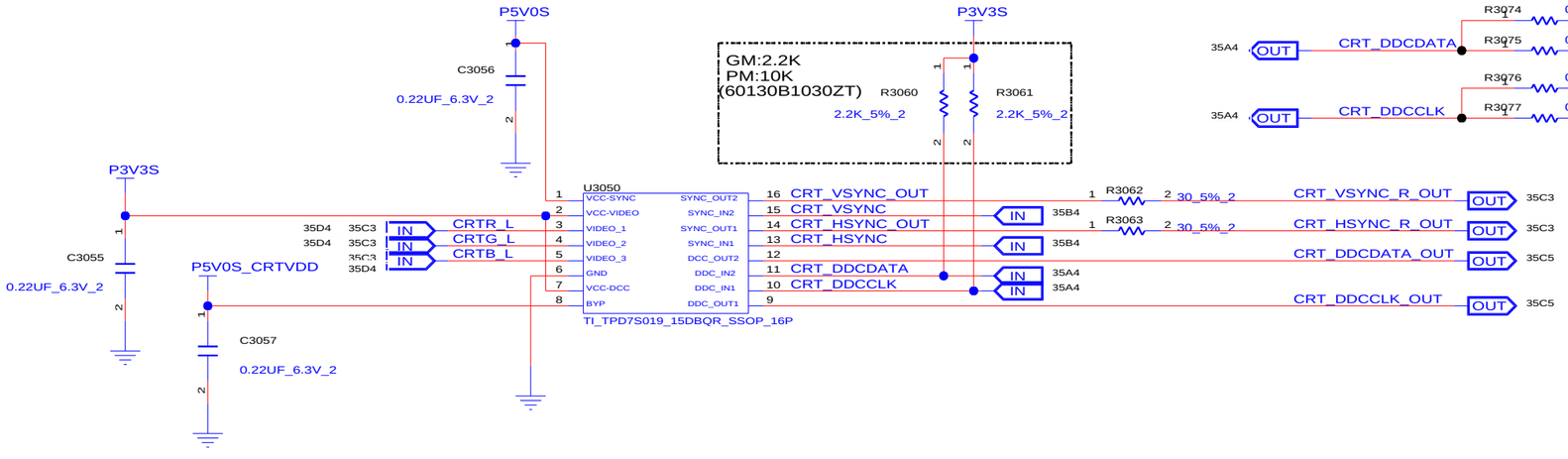
INVENTEC			
TITLE: MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX	DATE 21-OCT-2002	SHEET 34 of 68	

REFERENCE 3050~3099(CRT)









INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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REFERENCE 3150~3199(HDMI)

PLACE CLOSE TO CONNECTOR

50B3 BI PCH_HDMI_DDCDATA R3174 2 0_5%_1
50B3 BI PCH_HDMI_DDCCLK R3175 2 0_5%_1
56B3 BI VGA_HDMI_DDCDATA R3176 2 0_5%_1 HDMI_DDCDATA BI 36C8
56B3 BI VGA_HDMI_DDCCLK R3177 2 0_5%_1 HDMI_DDCCLK BI 36C8

36A7 36A2 IN HDMI_TX2_C_DP R3166 2 0_5%_2 HDMI_TX2_R_DP
36A7 36A2 IN HDMI_TX2_C_DN R3167 2 0_5%_2 HDMI_TX2_R_DN
36A7 36A2 IN HDMI_TX1_C_DP R3168 2 0_5%_2 HDMI_TX1_R_DP
36A7 36A2 IN HDMI_TX1_C_DN R3169 2 0_5%_2 HDMI_TX1_R_DN
36A7 36A2 IN HDMI_TX0_C_DP R3170 2 0_5%_2 HDMI_TX0_R_DP
36B7 36A2 IN HDMI_TX0_C_DN R3171 2 0_5%_2 HDMI_TX0_R_DN
36B7 36A2 IN HDMI_TXC_C_DP R3172 2 0_5%_2 HDMI_TXC_R_DP
36B7 36A2 IN HDMI_TXC_C_DN R3173 2 0_5%_2 HDMI_TXC_R_DN

P5V0AL
D3150
DIODE-BAT54-TAP-PHP
R3152 2.2K_5%_2
R3153 2.2K_5%_2
GM: 2.2K
PM:10K
(60130B1030ZT)

P3V3S
GM: 2.2K
PM:10K
(60130B1030ZT)
R3178 2.2K_5%_2
R3179 2.2K_5%_2
Q3151 SSM3K17FU
36D6 BI HDMI_DDCDATA S D HDMI_CN_DDCDATA BI 36C3 37C3
Q3150 SSM3K17FU
36D6 BI HDMI_DDCCLK S D HDMI_CN_DDCCLK BI 36C3 37D3

CN3150
1 TMDS Data2+
2 TMDS Data2 Shield
3 TMDS Data2-
4 TMDS Data1+
5 TMDS Data1 Shield
6 TMDS Data1-
7 TMDS Data0+
8 TMDS Data0 Shield
9 TMDS Data0-
10 TMDS Clock+
11 TMDS Clock Shield
12 TMDS Clock-
13 CEC G1 G1
14 Reserved G2 G2
15 DDC Clock G3 G3
16 DDC Data G4 G4
17 DDC/CEC GND
18 +5V Power
19 Hot Plug Detect
SYN_100042GR019M26DZL_19P

37D6 BI HDMI_CEC
37D3 36C6 BI HDMI_CN_DDCCLK
37C3 36C6 BI HDMI_CN_DDCDATA
TP3151 TP24 1

P5V0AL
40MIL
D3155 SBR3U40P1
P5V0AL_HDMI_VDD1 FUSE3150 SMD1812P110TF P5V0AL_HDMI_VDD2
C3150 100PF_50V_2
CLOSE TO CONNECTOR

37C1 OUT HPDET_IC
R3154 1K_5%_2
R3150 470K_5%_2
C3151 22PF_50V_2_DY

P3V3S
GM:680_5%
PM:499_5%
(6013A0076801)
Q3152 SSM3K7002BFU
R3165 100K_5%_2

36C5 36A2 IN HDMI_TXC_C_DP R3164 680_5%_2
36C5 36A2 IN HDMI_TXC_C_DN R3163 680_5%_2
36D5 36A2 IN HDMI_TX0_C_DN R3162 680_5%_2
36D5 36A2 IN HDMI_TX0_C_DP R3161 680_5%_2
36D5 36A2 IN HDMI_TX1_C_DN R3160 680_5%_2
36D5 36A2 IN HDMI_TX1_C_DP R3159 680_5%_2
36D5 36A2 IN HDMI_TX2_C_DN R3158 680_5%_2
36D5 36A2 IN HDMI_TX2_C_DP R3157 680_5%_2

50B3 OUT PCH_HPDET R3180 2 0_5%_1
56C5 OUT VGA_HPDET R3181 2 0_5%_1
HPDET
P3V3S
U3150 TC7SZ08FU
HDMI_HPD_EC IN 21D6 37B1
PLT_RST# IN 31C6 41C7 51A7

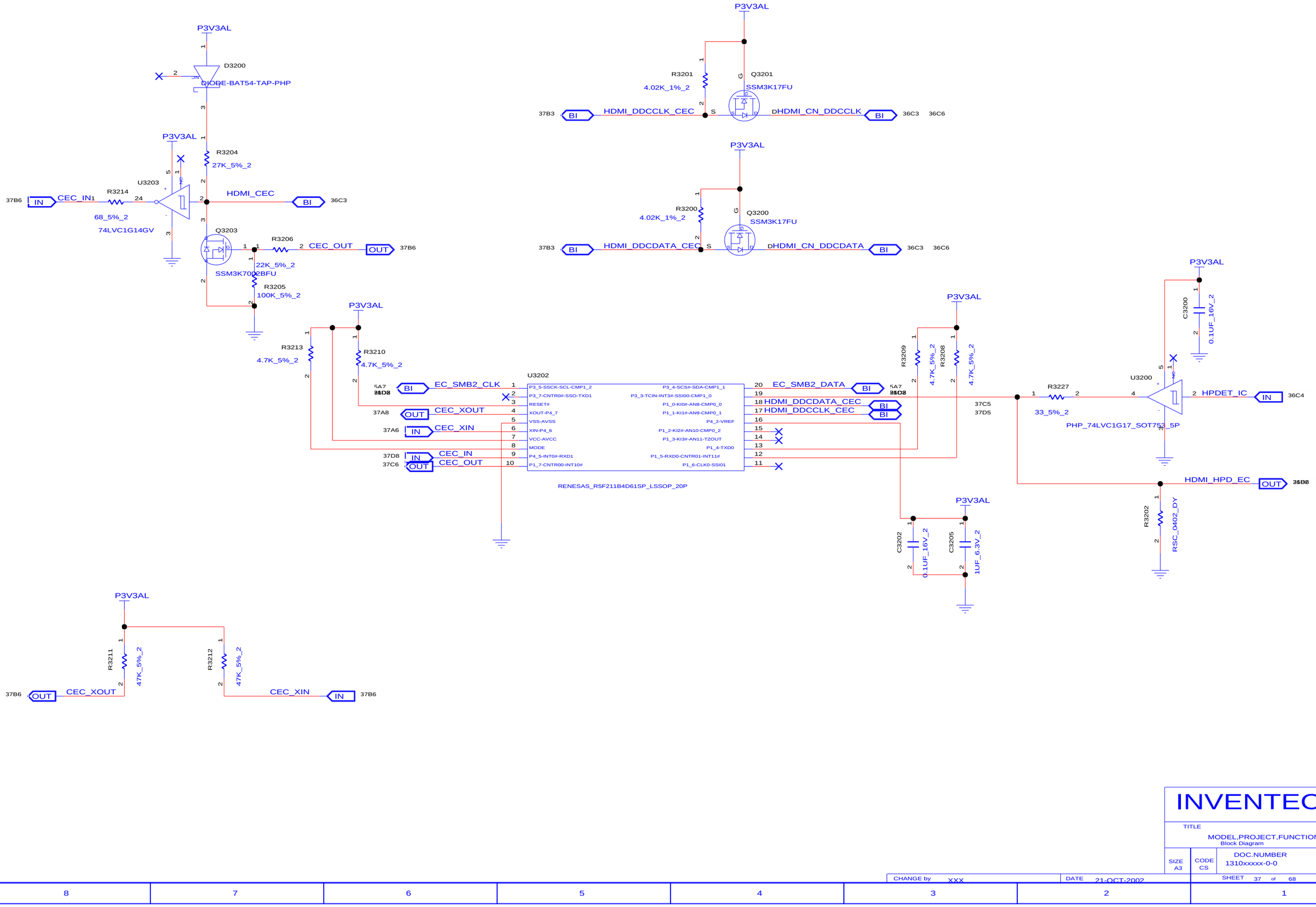
56F3 IN VGA_HDMI_TX2_DN C3152 0.1UF_6.3V_1
56F3 IN VGA_HDMI_TX2_DP C3154 0.1UF_6.3V_1
56F3 IN VGA_HDMI_TX1_DN C3153 0.1UF_6.3V_1
56F3 IN VGA_HDMI_TX1_DP C3155 0.1UF_6.3V_1
56F3 IN VGA_HDMI_TX0_DN C3156 0.1UF_6.3V_1
56F3 IN VGA_HDMI_TX0_DP C3157 0.1UF_6.3V_1
56F3 IN VGA_HDMI_TXC_DN C3158 0.1UF_6.3V_1
56F3 IN VGA_HDMI_TXC_DP C3159 0.1UF_6.3V_1

50B3 IN PCH_HDMI_TX2_DN C3160 0.1UF_6.3V_1
50B3 IN PCH_HDMI_TX2_DP C3162 0.1UF_6.3V_1
50B3 IN PCH_HDMI_TX1_DN C3161 0.1UF_6.3V_1
50B3 IN PCH_HDMI_TX1_DP C3163 0.1UF_6.3V_1
50B3 IN PCH_HDMI_TX0_DN C3164 0.1UF_6.3V_1
50B3 IN PCH_HDMI_TX0_DP C3165 0.1UF_6.3V_1
50B3 IN PCH_HDMI_TXC_DN C3166 0.1UF_6.3V_1
50B3 IN PCH_HDMI_TXC_DP C3167 0.1UF_6.3V_1

HDMI_TX2_C_DN OUT 36A7 36D5
HDMI_TX2_C_DP OUT 36A7 36D5
HDMI_TX1_C_DN OUT 36A7 36D5
HDMI_TX1_C_DP OUT 36A7 36D5
HDMI_TX0_C_DN OUT 36B7 36D5
HDMI_TX0_C_DP OUT 36A7 36D5
HDMI_TXC_C_DN OUT 36B7 36C5
HDMI_TXC_C_DP OUT 36B7 36C5

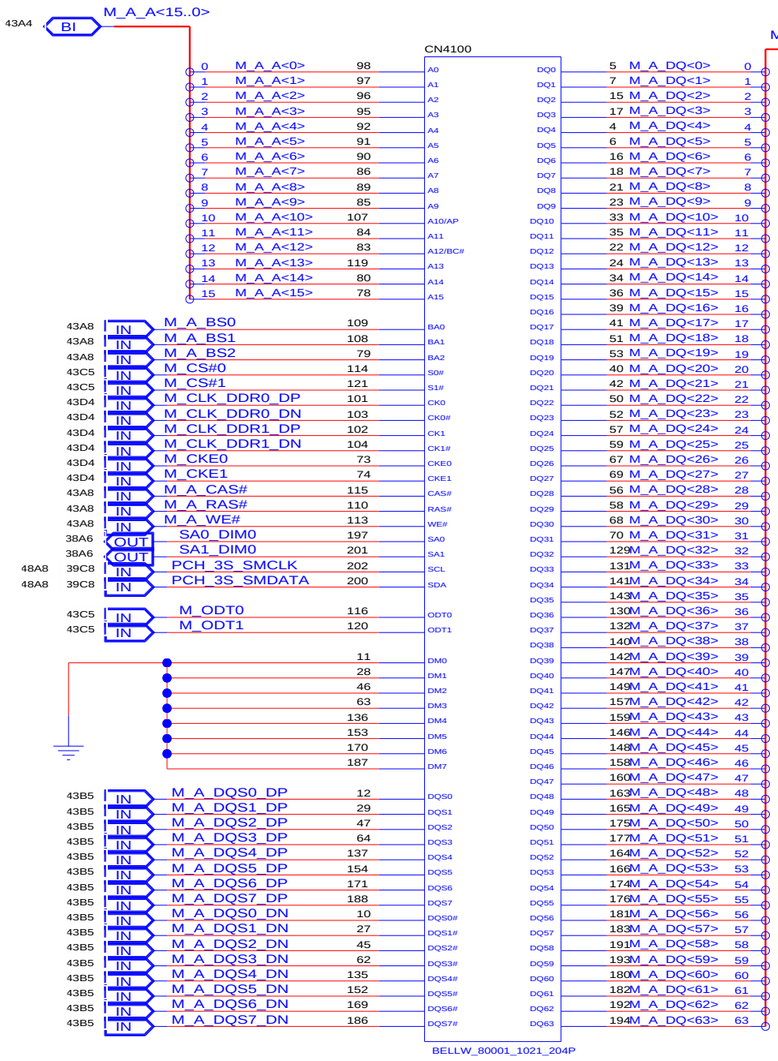
INVENTEC

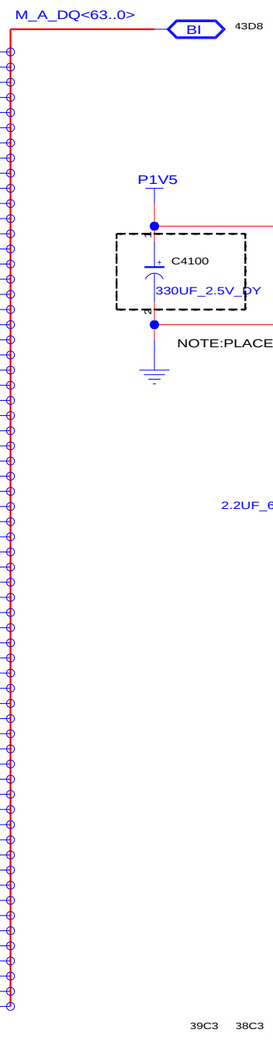
TITLE: MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX	DATE 21-OCT-2002	SHEET 36 of 68	

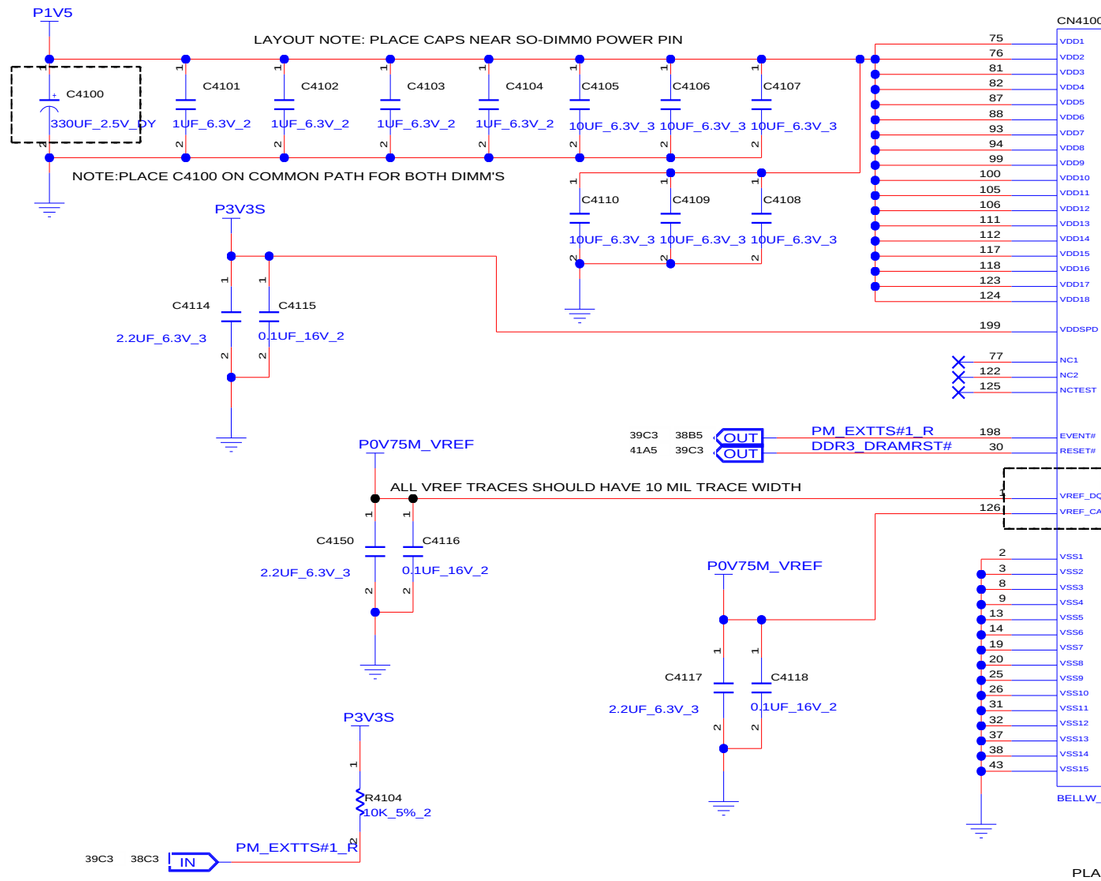

P3V3AL
D3200
DIODE-BAT54-TAP-PHP
R3204
27K_5%_2
U3203
R3214
68_5%_2
74LVC1G14GV
37B6
IN
CEC_IN1
HDMI_CEC
BI
36C3
Q3203
SSM3K7002BFU
R3206
22K_5%_2
CEC_OUT
OUT
37B6
R3205
100K_5%_2
R3201
4.02K_1%_2
Q3201
SSM3K17FU
37B3
HDMI_DDCCLK_CEC
HDMI_CN_DDCCLK
36C3
36C6
R3200
4.02K_1%_2
Q3200
SSM3K17FU
HDMI_DDCDATA_CEC
HDMI_CN_DDCDATA
R3213
4.7K_5%_2
R3210
4.7K_5%_2
U3202
EC_SMB2_CLK
CEC_XOUT
CEC_XIN
CEC_IN
CEC_OUT
37D8
37C6
P3_5-SSCK-SCL-CMP1_2
P3_7-CNTR0#-SSO-TXD1
RESET#
XOUT-P4_7
VSS-AVSS
XIN-P4_6
VCC-AVCC
MODE
P4_5-INT0#-RXD1
P1_7-CNTR00-INT10#
P3_4-SCS#-SDA-CMP1_1
P3_3-TCIN-INT3#-SSI00-CMP1_0
P1_0-KI0#-AN8-CMP0_0
P1_1-KI1#-AN9-CMP0_1
P4_2-VREF
P1_2-KI2#-AN10-CMP0_2
P1_3-KI3#-AN11-TZOUT
P1_4-TXD0
P1_5-RXD0-CNTR01-INT11#
P1_6-CLK0-SSI01
RENESAS_R5F211B4D61SP_LSSOP_20P
EC_SMB2_DATA
HDMI_DDCDATA_CEC
HDMI_DDCCLK_CEC
R3209
4.7K_5%_2
R3208
4.7K_5%_2
C3202
0.1UF_16V_2
C3205
1UF_6.3V_2
C3200
0.1UF_16V_2
U3200
R3227
33_5%_2
PHP_74LVC1G17_SOT753_5P
HPDET_IC
HDMI_HPD_EC
R3202
RSC_0402_DY
R3211
47K_5%_2
R3212
47K_5%_2
CEC_XOUT
CEC_XIN

REFERENCE 4100~4299(DDR)

CHA



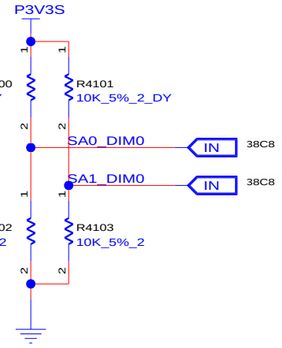




NOTE:

IF SA0_DIM0=1 , SA1_DIM0=0
SO-DIMMA SPD ADDRESS IS 0XA2
SO-DIMMA TS ADDRESS IS 0X32

IF SA0_DIM0=0 , SA1_DIM0=0
SO-DIMMA SPD ADDRESS IS 0XA0
SO-DIMMA TS ADDRESS IS 0X30



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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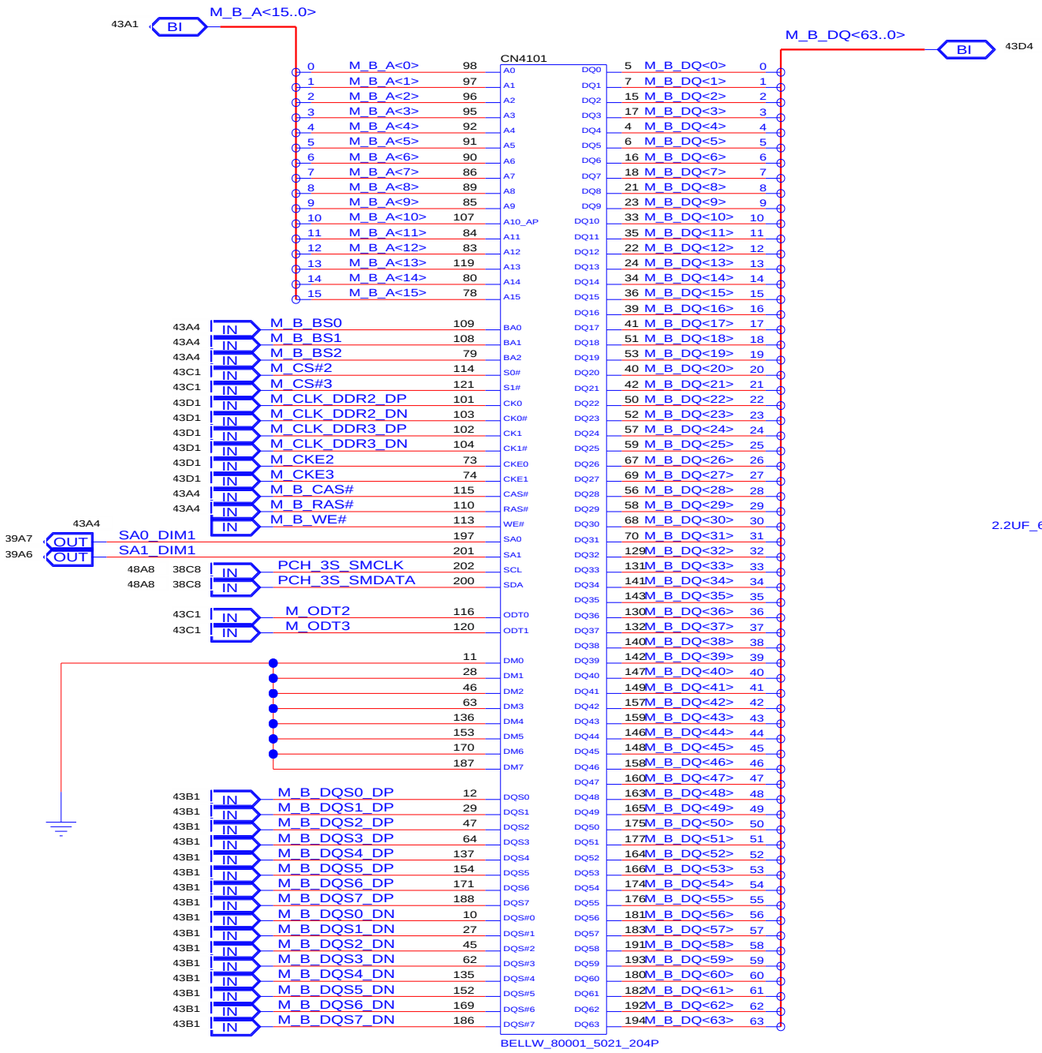
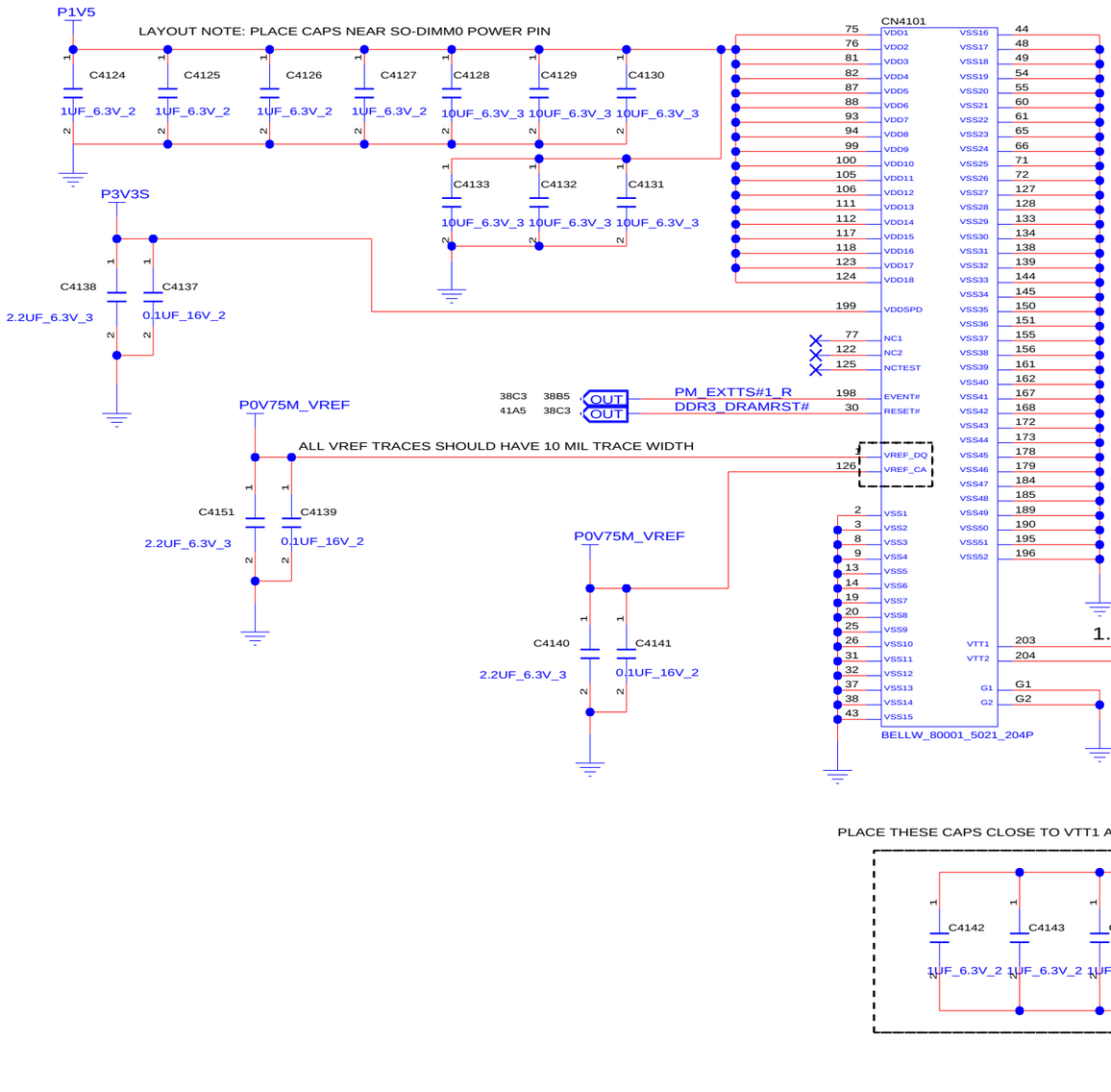
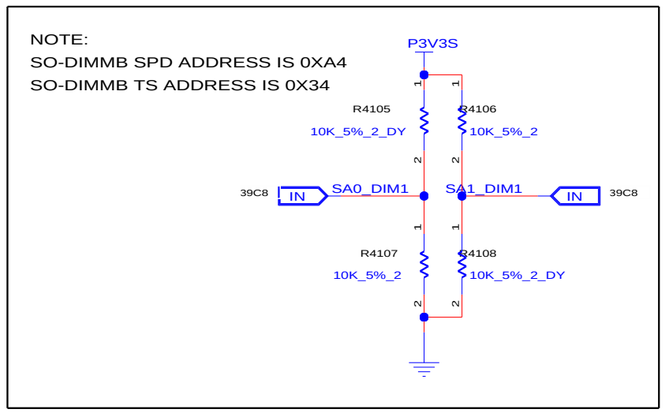
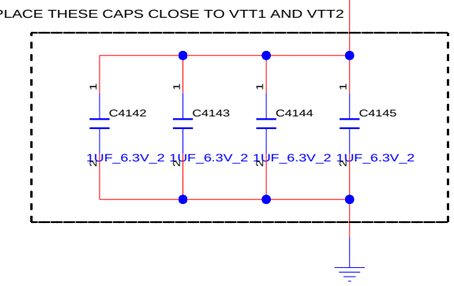
REFERENCE 4100~4299(DDR)

CHB









INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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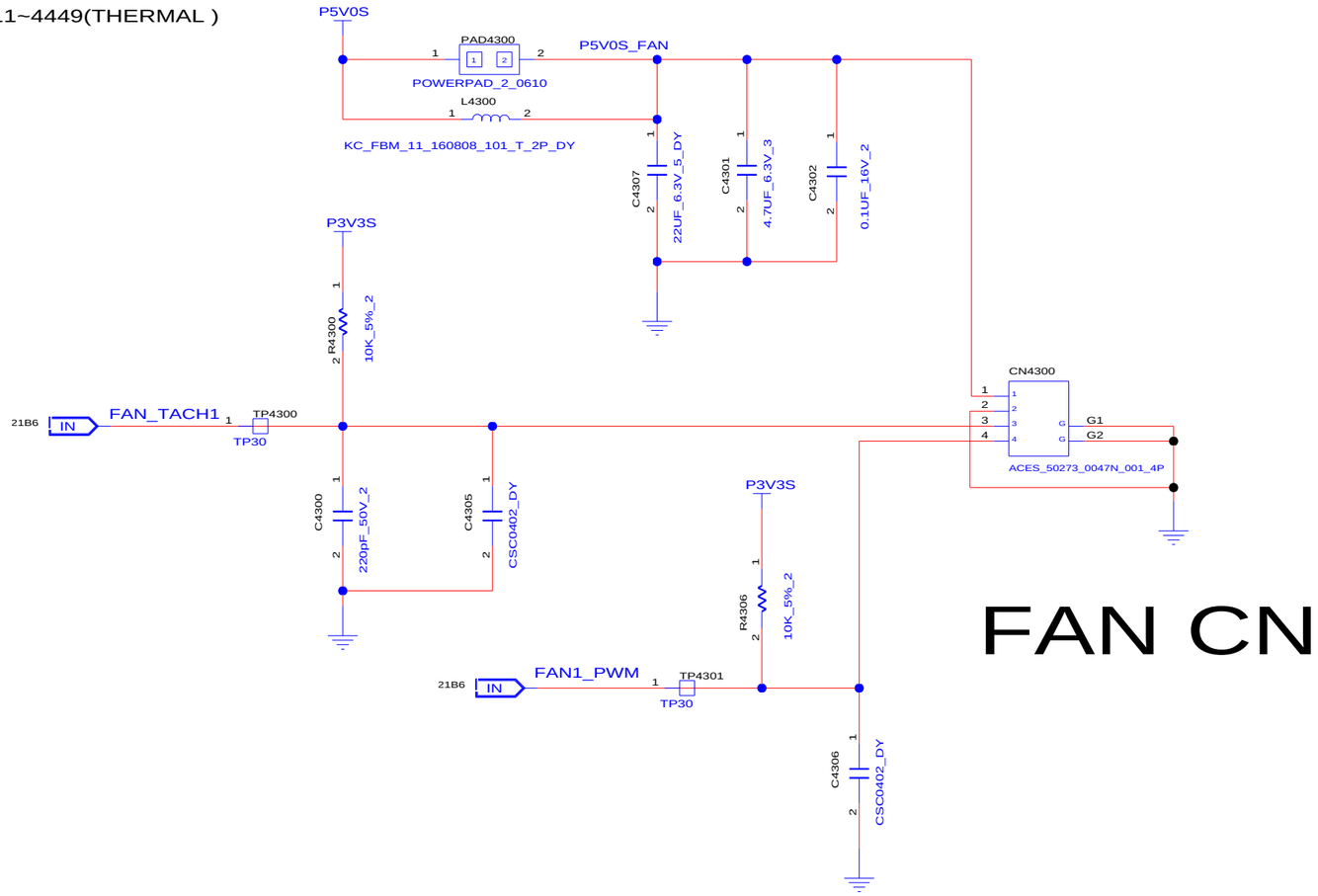
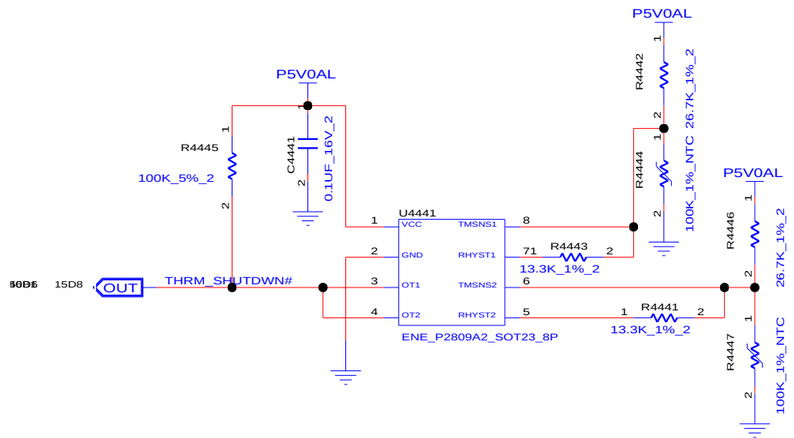
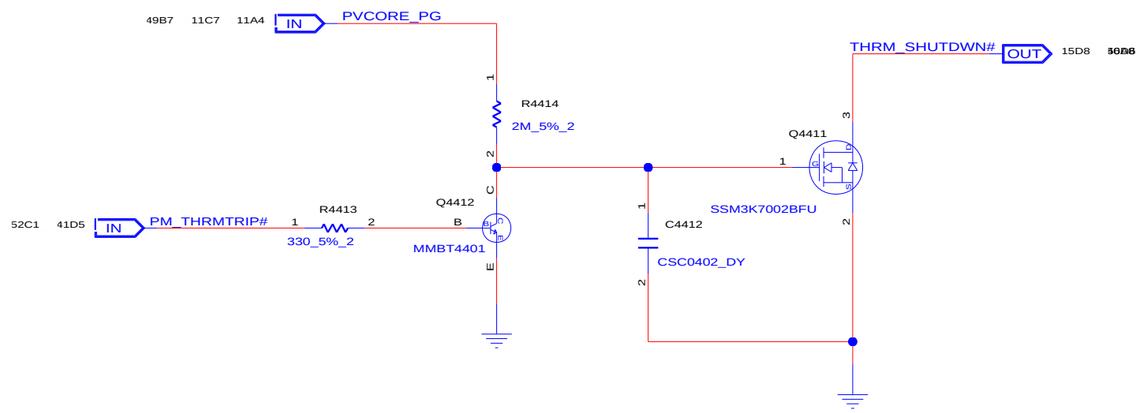
REFERENCE 4300~4349(FAN)

REFERENCE 4411~4449(THERMAL)



FAN CN





INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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REFERENCE 4500~4699(CPU)

P1V8S
R4500 2.2K_5%_2
R4502 2.2K_5%_2_DY
R4501 1K_5%_2
41D5 OUT H_SNB_IVB#
NV_CLE OUT 52B2
PLACE CLOSE TO CPT AND NVRAM CONNECTOR

PROCESS STRAP SETTING	
SANDY BRIDGE ONLY	STUFF R4502
SANDY BRIDGE/IVY BRIDGE	STUFF R4500/R4501

DMI&FDI TERMINATIONVOLTAGE	
NV_CLE	SET TOVSS WHEN LOW(DEFAULT)
	SET TOVCC WHEN HIGH

P1V05S
R4503 62_5%_2
21C3 11B7 OUT CPU_PROCHOT# R4504 56_5%_2 CPU_PROCHOT#_R
C4500 CSC0402_DY
40A4 52C1 OUT PM_THRMTRIP#

P1V5S
R4505 200_5%_2
LOW IN C6/C7
49A3 BI H_PM_SYNC
52C2 IN H_CPUPWRGD
49B7 IN PM_DRAM_PWRGD
R4506 130_1%_2
PM_DRAM_PWRGD_R
31C6 IN PLT_RST#
R4507 1.5K_5%_2
R4508 750_1%_2
R4509 10K_5%_2

CN4500

41D8 OUT H_SNB_IVB#	C26	PROC_SELECT#	MISC
TP4500 TP24	AN34	SKTOCC#	
TP4501 TP24	AL33	CATERR#	THERMAL
52C2 21A6 OUT H_PECI	AN33	PECI	
21C3 11B7 OUT CPU_PROCHOT#	AL32	PROCHOT#	
40A4 52C1 OUT PM_THRMTRIP#	AN32	THERMTRIP#	
49A3 BI H_PM_SYNC	AM34	PM_SYNC	PWR MANAGEMENT
52C2 IN H_CPUPWRGD	AP33	UNCOREPWRGOOD	
49B7 IN PM_DRAM_PWRGD_R	V8	SM_DRAMPWROK	
31C6 IN PLT_RST#	AR33	RESET#	

LOTES_ACA_ZIF_069_P01_989P

CLOCKS
BCLK A28 CLK_DMI_PCH_DP IN 48B3
BCLK# A27 CLK_DMI_PCH_DN IN 48B3
DPLL_REF_CLK A16 R4510 1K_5%_2
DPLL_REF_CLK# A15 R4511 1K_5%_2
P1V05S

MISC
SM_DRAMRST# R8 CPU_DRAMRST# OUT 41A5
SM_RCOMP[0] AK1 SM_RCOMP0 R4512 140_1%_2
SM_RCOMP[1] A5 SM_RCOMP1 R4513 25.5_1%_2
SM_RCOMP[2] A4 SM_RCOMP2 R4514 200_1%_2

JTAG & BPM
PRDY# AP29 TP30 TP4502 H_PRDY# OUT
PREQ# AP27 TP30 TP4503 H_PREQ# IN 41B2
TCK AR26 TP30 TP4504 H_TCK IN 41B2
TMS AR27 TP30 TP4505 H_TMS IN 41B2
TRST# AP30 TP30 TP4506 H_TRST# IN 41B2
TDI AR28 TP30 TP4507 H_TDI IN 41B2
TDO AP26 TP30 TP4508 H_TDO OUT
DBR# AL35 TP30 TP4509 SYS_RESET# OUT 49B8
BPM#[0] AT28
BPM#[1] AR29
BPM#[2] AR30
BPM#[3] AT30
BPM#[4] AP32
BPM#[5] AR31
BPM#[6] AT31
BPM#[7] AR32

CAD NOTE: ALL DDR_COMP SIGNALS SHOULD BE ROUTED SUCH TAHT
- MAX LENGTH = 500 MILS
- TRACE WIDTH = 15MILS AND
- MB TRACE IMPEDANCE < 68 MOHMS
(WORST CASE RESISTANCE)

P1V05S
41C1 IN H_TMS R4516 51_5%_2
41C1 IN H_TDI R4517 51_5%_2
41C1 IN H_PREQ# R1418 51_5%_2_DY
41C1 IN H_TCK R4519 51_5%_2
41C1 IN H_TRST# R4520 51_5%_2

S3 CIRCUIT: DRAM_RST# TO MEMORY SHOULD BE HIGH DURING S3

P3V3A
R4601 1K_5%_2
45D6 45D8 OUT DRAMRST_CNTRL
48D3 IN DRAMRST_CNTRL_PCH
R4600 0_5%_2
Q4600 SSM3K7002BFU
C4620 0.047UF_16V_2

P1V5
R4602 1K_5%_2
R4603 1K_5%_2
DDR3_DRAMRST# OUT 38C3 39C3
CPU_DRAMRST# IN 41D2
R4604 4.99K_1%_2

INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
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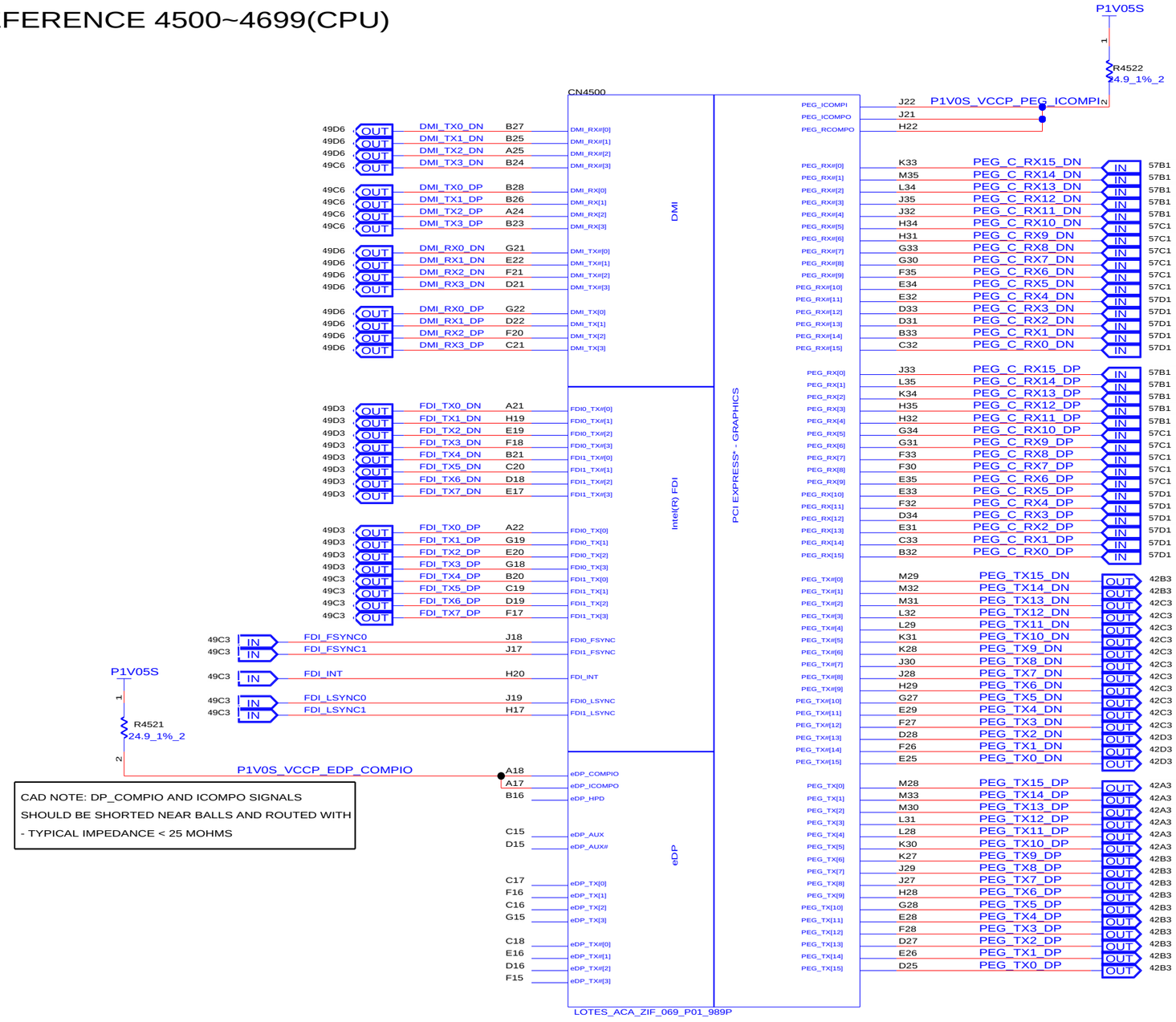
REFERENCE 4500~4699(CPU)



CAD NOTE: DP_COMPIO AND ICOMPO SIGNALS
SHOULD BE SHORTED NEAR BALLS AND ROUTED WITH
- TYPICAL IMPEDANCE < 25 MOHMS

CAD NOTE: PEG_ICOMPI AND RCOMPO SIGNALS
SHOULD BE SHORTED AND ROUTED WITH
- MAX LENGTH = 500 MILS
- TYPICAL IMPEDANCE = 43 MOHMS

PEG_ICOMPO SIGNALS SHOULD BE ROUTED WITH
- MAX LENGTH = 500 MILS
- TYPICAL IMPEDANCE = 14.5 MOHMS

CLOSE TO CPU

42B4	PEG_TX0_DN	C4580	0.22UF_6.3V_1	PEG_C_TX0_DN	57D6
42B4	PEG_TX1_DN	C4581	0.22UF_6.3V_1	PEG_C_TX1_DN	57D6
42B4	PEG_TX2_DN	C4582	0.22UF_6.3V_1	PEG_C_TX2_DN	57D6
42B4	PEG_TX3_DN	C4583	0.22UF_6.3V_1	PEG_C_TX3_DN	57D6
42B4	PEG_TX4_DN	C4584	0.22UF_6.3V_1	PEG_C_TX4_DN	57D6
42B4	PEG_TX5_DN	C4585	0.22UF_6.3V_1	PEG_C_TX5_DN	57C6
42B4	PEG_TX6_DN	C4586	0.22UF_6.3V_1	PEG_C_TX6_DN	57C6
42B4	PEG_TX7_DN	C4587	0.22UF_6.3V_1	PEG_C_TX7_DN	57C6
42B4	PEG_TX8_DN	C4588	0.22UF_6.3V_1	PEG_C_TX8_DN	57C6
42B4	PEG_TX9_DN	C4589	0.22UF_6.3V_1	PEG_C_TX9_DN	57C6
42B4	PEG_TX10_DN	C4590	0.22UF_6.3V_1	PEG_C_TX10_DN	57C6
42B4	PEG_TX11_DN	C4591	0.22UF_6.3V_1	PEG_C_TX11_DN	57B6
42B4	PEG_TX12_DN	C4592	0.22UF_6.3V_1	PEG_C_TX12_DN	57B6
42C4	PEG_TX13_DN	C4593	0.22UF_6.3V_1	PEG_C_TX13_DN	57B6
42C4	PEG_TX14_DN	C4594	0.22UF_6.3V_1	PEG_C_TX14_DN	57B6
42C4	PEG_TX15_DN	C4595	0.22UF_6.3V_1	PEG_C_TX15_DN	57B6
42A4	PEG_TX0_DP	C4596	0.22UF_6.3V_1	PEG_C_TX0_DP	57D6
42A4	PEG_TX1_DP	C4597	0.22UF_6.3V_1	PEG_C_TX1_DP	57D6
42A4	PEG_TX2_DP	C4598	0.22UF_6.3V_1	PEG_C_TX2_DP	57D6
42A4	PEG_TX3_DP	C4599	0.22UF_6.3V_1	PEG_C_TX3_DP	57D6
42A4	PEG_TX4_DP	C4600	0.22UF_6.3V_1	PEG_C_TX4_DP	57D6
42A4	PEG_TX5_DP	C4601	0.22UF_6.3V_1	PEG_C_TX5_DP	57D6
42A4	PEG_TX6_DP	C4602	0.22UF_6.3V_1	PEG_C_TX6_DP	57C6
42B4	PEG_TX7_DP	C4603	0.22UF_6.3V_1	PEG_C_TX7_DP	57C6
42B4	PEG_TX8_DP	C4604	0.22UF_6.3V_1	PEG_C_TX8_DP	57C6
42B4	PEG_TX9_DP	C4605	0.22UF_6.3V_1	PEG_C_TX9_DP	57C6
42B4	PEG_TX10_DP	C4606	0.22UF_6.3V_1	PEG_C_TX10_DP	57C6
42B4	PEG_TX11_DP	C4607	0.22UF_6.3V_1	PEG_C_TX11_DP	57B6
42B4	PEG_TX12_DP	C4608	0.22UF_6.3V_1	PEG_C_TX12_DP	57B6
42B4	PEG_TX13_DP	C4609	0.22UF_6.3V_1	PEG_C_TX13_DP	57B6
42B4	PEG_TX14_DP	C4610	0.22UF_6.3V_1	PEG_C_TX14_DP	57B6
42B4	PEG_TX15_DP	C4611	0.22UF_6.3V_1	PEG_C_TX15_DP	57B6

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
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SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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REFERENCE 4500~4699(CPU)

SOCKET,CPU,989P,TIN,3.0MM,STR,SMD,TR

CN4500

38D5 BI M_A_DQ<63..0>

0	M_A_DQ<0>	C5	SA_DQ[0]
1	M_A_DQ<1>	D5	SA_DQ[1]
2	M_A_DQ<2>	D3	SA_DQ[2]
3	M_A_DQ<3>	D2	SA_DQ[3]
4	M_A_DQ<4>	D6	SA_DQ[4]
5	M_A_DQ<5>	C6	SA_DQ[5]
6	M_A_DQ<6>	C2	SA_DQ[6]
7	M_A_DQ<7>	C3	SA_DQ[7]
8	M_A_DQ<8>	F10	SA_DQ[8]
9	M_A_DQ<9>	F8	SA_DQ[9]
10	M_A_DQ<10>	G10	SA_DQ[10]
11	M_A_DQ<11>	G9	SA_DQ[11]
12	M_A_DQ<12>	F9	SA_DQ[12]
13	M_A_DQ<13>	F7	SA_DQ[13]
14	M_A_DQ<14>	G8	SA_DQ[14]
15	M_A_DQ<15>	G7	SA_DQ[15]
16	M_A_DQ<16>	K4	SA_DQ[16]
17	M_A_DQ<17>	K5	SA_DQ[17]
18	M_A_DQ<18>	K1	SA_DQ[18]
19	M_A_DQ<19>	J1	SA_DQ[19]
20	M_A_DQ<20>	J5	SA_DQ[20]
21	M_A_DQ<21>	J4	SA_DQ[21]
22	M_A_DQ<22>	J2	SA_DQ[22]
23	M_A_DQ<23>	K2	SA_DQ[23]
24	M_A_DQ<24>	M8	SA_DQ[24]
25	M_A_DQ<25>	N10	SA_DQ[25]
26	M_A_DQ<26>	N8	SA_DQ[26]
27	M_A_DQ<27>	N7	SA_DQ[27]
28	M_A_DQ<28>	M10	SA_DQ[28]
29	M_A_DQ<29>	M9	SA_DQ[29]
30	M_A_DQ<30>	N9	SA_DQ[30]
31	M_A_DQ<31>	M7	SA_DQ[31]
32	M_A_DQ<32>	AG6	SA_DQ[32]
33	M_A_DQ<33>	AG5	SA_DQ[33]
34	M_A_DQ<34>	AK6	SA_DQ[34]
35	M_A_DQ<35>	AK5	SA_DQ[35]
36	M_A_DQ<36>	AH5	SA_DQ[36]
37	M_A_DQ<37>	AH6	SA_DQ[37]
38	M_A_DQ<38>	AJ5	SA_DQ[38]
39	M_A_DQ<39>	AJ6	SA_DQ[39]
40	M_A_DQ<40>	AJ8	SA_DQ[40]
41	M_A_DQ<41>	AK8	SA_DQ[41]
42	M_A_DQ<42>	AJ9	SA_DQ[42]
43	M_A_DQ<43>	AK9	SA_DQ[43]
44	M_A_DQ<44>	AH8	SA_DQ[44]
45	M_A_DQ<45>	AH9	SA_DQ[45]
46	M_A_DQ<46>	AL9	SA_DQ[46]
47	M_A_DQ<47>	AL8	SA_DQ[47]
48	M_A_DQ<48>	AP11	SA_DQ[48]
49	M_A_DQ<49>	AN11	SA_DQ[49]
50	M_A_DQ<50>	AL12	SA_DQ[50]
51	M_A_DQ<51>	AM12	SA_DQ[51]
52	M_A_DQ<52>	AM11	SA_DQ[52]
53	M_A_DQ<53>	AL11	SA_DQ[53]
54	M_A_DQ<54>	AP12	SA_DQ[54]
55	M_A_DQ<55>	AN12	SA_DQ[55]
56	M_A_DQ<56>	AJ14	SA_DQ[56]
57	M_A_DQ<57>	AH14	SA_DQ[57]
58	M_A_DQ<58>	AL15	SA_DQ[58]
59	M_A_DQ<59>	AK15	SA_DQ[59]
60	M_A_DQ<60>	AL14	SA_DQ[60]
61	M_A_DQ<61>	AK14	SA_DQ[61]
62	M_A_DQ<62>	AJ15	SA_DQ[62]
63	M_A_DQ<63>	AH15	SA_DQ[63]

38D8 OUT M_A_BS0 AE10 → SA_BS[0]
38D8 OUT M_A_BS1 AF10 → SA_BS[1]
38D8 OUT M_A_BS2 V6 → SA_BS[2]

38C8 OUT M_A_CAS# AE8 → SA_CAS#
38C8 OUT M_A_RAS# AD9 → SA_RAS#
38C8 OUT M_A_WE# AF9 → SA_WE#

SA_CLK[0] AB6 M_CLK_DDR0_DP OUT 38C8
SA_CLK#[0] AA6 M_CLK_DDR0_DN OUT 38C8
SA_CKE[0] V9 M_CKE0 OUT 38C8

SA_CLK[1] AA5 M_CLK_DDR1_DP OUT 38C8
SA_CLK#[1] AB5 M_CLK_DDR1_DN OUT 38C8
SA_CKE[1] V10 M_CKE1 OUT 38C8

RSVD_TP[1] AB4
RSVD_TP[2] AA4
RSVD_TP[3] W9

RSVD_TP[4] AB3
RSVD_TP[5] AA3
RSVD_TP[6] W10

SA_CS#[0] AK3 M_CS#0 OUT 38D8
SA_CS#[1] AL3 M_CS#1 OUT 38C8
RSVD_TP[7] AG1
RSVD_TP[8] AH1

SA_ODT[0] AH3 M_ODT0 OUT 38C8
SA_ODT[1] AG3 M_ODT1 OUT 38C8
RSVD_TP[9] AG2
RSVD_TP[10] AH2

SA_DQS#[0]	C4	M_A_DQS0_DN	OUT 38B8
SA_DQS#[1]	G6	M_A_DQS1_DN	OUT 38B8
SA_DQS#[2]	J3	M_A_DQS2_DN	OUT 38B8
SA_DQS#[3]	M6	M_A_DQS3_DN	OUT 38B8
SA_DQS#[4]	AL6	M_A_DQS4_DN	OUT 38B8
SA_DQS#[5]	AM8	M_A_DQS5_DN	OUT 38B8
SA_DQS#[6]	AR12	M_A_DQS6_DN	OUT 38B8
SA_DQS#[7]	AM15	M_A_DQS7_DN	OUT 38B8

SA_DQS[0]	D4	M_A_DQS0_DP	OUT 38B8
SA_DQS[1]	F6	M_A_DQS1_DP	OUT 38B8
SA_DQS[2]	K3	M_A_DQS2_DP	OUT 38B8
SA_DQS[3]	N6	M_A_DQS3_DP	OUT 38B8
SA_DQS[4]	AL5	M_A_DQS4_DP	OUT 38B8
SA_DQS[5]	AM9	M_A_DQS5_DP	OUT 38B8
SA_DQS[6]	AR11	M_A_DQS6_DP	OUT 38B8
SA_DQS[7]	AM14	M_A_DQS7_DP	OUT 38B8

M_A_A<15..0> OUT 38D8

SA_MA[0]	AD10	M_A_A<0>	0
SA_MA[1]	W1	M_A_A<1>	1
SA_MA[2]	W2	M_A_A<2>	2
SA_MA[3]	W7	M_A_A<3>	3
SA_MA[4]	V3	M_A_A<4>	4
SA_MA[5]	V2	M_A_A<5>	5
SA_MA[6]	W3	M_A_A<6>	6
SA_MA[7]	W6	M_A_A<7>	7
SA_MA[8]	V1	M_A_A<8>	8
SA_MA[9]	W5	M_A_A<9>	9
SA_MA[10]	AD8	M_A_A<10>	10
SA_MA[11]	V4	M_A_A<11>	11
SA_MA[12]	W4	M_A_A<12>	12
SA_MA[13]	AF8	M_A_A<13>	13
SA_MA[14]	V5	M_A_A<14>	14
SA_MA[15]	V7	M_A_A<15>	15

DDR SYSTEM MEMORY A

LOTES_ACA_ZIF_069_P01_989P

39D5 BI M_B_DQ<63..0>

0	M_B_DQ<0>	C9	SB_DQ[0]
1	M_B_DQ<1>	A7	SB_DQ[1]
2	M_B_DQ<2>	D10	SB_DQ[2]
3	M_B_DQ<3>	C8	SB_DQ[3]
4	M_B_DQ<4>	A9	SB_DQ[4]
5	M_B_DQ<5>	A8	SB_DQ[5]
6	M_B_DQ<6>	D9	SB_DQ[6]
7	M_B_DQ<7>	D8	SB_DQ[7]
8	M_B_DQ<8>	G4	SB_DQ[8]
9	M_B_DQ<9>	F4	SB_DQ[9]
10	M_B_DQ<10>	F1	SB_DQ[10]
11	M_B_DQ<11>	G1	SB_DQ[11]
12	M_B_DQ<12>	G5	SB_DQ[12]
13	M_B_DQ<13>	F5	SB_DQ[13]
14	M_B_DQ<14>	F2	SB_DQ[14]
15	M_B_DQ<15>	G2	SB_DQ[15]
16	M_B_DQ<16>	J7	SB_DQ[16]
17	M_B_DQ<17>	J8	SB_DQ[17]
18	M_B_DQ<18>	K10	SB_DQ[18]
19	M_B_DQ<19>	K9	SB_DQ[19]
20	M_B_DQ<20>	J9	SB_DQ[20]
21	M_B_DQ<21>	J10	SB_DQ[21]
22	M_B_DQ<22>	K8	SB_DQ[22]
23	M_B_DQ<23>	K7	SB_DQ[23]
24	M_B_DQ<24>	M5	SB_DQ[24]
25	M_B_DQ<25>	N4	SB_DQ[25]
26	M_B_DQ<26>	N2	SB_DQ[26]
27	M_B_DQ<27>	N1	SB_DQ[27]
28	M_B_DQ<28>	M4	SB_DQ[28]
29	M_B_DQ<29>	N5	SB_DQ[29]
30	M_B_DQ<30>	M2	SB_DQ[30]
31	M_B_DQ<31>	M1	SB_DQ[31]
32	M_B_DQ<32>	AM5	SB_DQ[32]
33	M_B_DQ<33>	AM6	SB_DQ[33]
34	M_B_DQ<34>	AR3	SB_DQ[34]
35	M_B_DQ<35>	AP3	SB_DQ[35]
36	M_B_DQ<36>	AN3	SB_DQ[36]
37	M_B_DQ<37>	AN2	SB_DQ[37]
38	M_B_DQ<38>	AN1	SB_DQ[38]
39	M_B_DQ<39>	AP2	SB_DQ[39]
40	M_B_DQ<40>	AP5	SB_DQ[40]
41	M_B_DQ<41>	AN9	SB_DQ[41]
42	M_B_DQ<42>	AT5	SB_DQ[42]
43	M_B_DQ<43>	AT6	SB_DQ[43]
44	M_B_DQ<44>	AP6	SB_DQ[44]
45	M_B_DQ<45>	AN8	SB_DQ[45]
46	M_B_DQ<46>	AR6	SB_DQ[46]
47	M_B_DQ<47>	AR5	SB_DQ[47]
48	M_B_DQ<48>	AR9	SB_DQ[48]
49	M_B_DQ<49>	AJ11	SB_DQ[49]
50	M_B_DQ<50>	AT8	SB_DQ[50]
51	M_B_DQ<51>	AT9	SB_DQ[51]
52	M_B_DQ<52>	AH11	SB_DQ[52]
53	M_B_DQ<53>	AR8	SB_DQ[53]
54	M_B_DQ<54>	AJ12	SB_DQ[54]
55	M_B_DQ<55>	AH12	SB_DQ[55]
56	M_B_DQ<56>	AT11	SB_DQ[56]
57	M_B_DQ<57>	AN14	SB_DQ[57]
58	M_B_DQ<58>	AR14	SB_DQ[58]
59	M_B_DQ<59>	AT14	SB_DQ[59]
60	M_B_DQ<60>	AT12	SB_DQ[60]
61	M_B_DQ<61>	AN15	SB_DQ[61]
62	M_B_DQ<62>	AR15	SB_DQ[62]
63	M_B_DQ<63>	AT15	SB_DQ[63]

39D8 OUT M_B_BS0 AA9 → SB_BS[0]
39D8 OUT M_B_BS1 AA7 → SB_BS[1]
39C8 OUT M_B_BS2 R6 → SB_BS[2]

39C8 OUT M_B_CAS# AA10 → SB_CAS#
39C8 OUT M_B_RAS# AB8 → SB_RAS#
39C8 OUT M_B_WE# AB9 → SB_WE#

SB_CLK[0] AE2 M_CLK_DDR2_DP OUT 39C8
SB_CLK#[0] AD2 M_CLK_DDR2_DN OUT 39C8
SB_CKE[0] R9 M_CKE2 OUT 39C8

SB_CLK[1] AE1 M_CLK_DDR3_DP OUT 39C8
SB_CLK#[1] AD1 M_CLK_DDR3_DN OUT 39C8
SB_CKE[1] R10 M_CKE3 OUT 39C8

RSVD_TP[11] AB2
RSVD_TP[12] AA2
RSVD_TP[13] T9

RSVD_TP[14] AA1
RSVD_TP[15] AB1
RSVD_TP[16] T10

SB_CS#[0] AD3 M_CS#2 OUT 39C8
SB_CS#[1] AE3 M_CS#3 OUT 39C8
RSVD_TP[17] AD6
RSVD_TP[18] AE6

SB_ODT[0] AE4 M_ODT2 OUT 39C8
SB_ODT[1] AD4 M_ODT3 OUT 39C8
RSVD_TP[19] AD5
RSVD_TP[20] AE5

SB_DQS#[0]	D7	M_B_DQS0_DN	OUT 39B8
SB_DQS#[1]	F3	M_B_DQS1_DN	OUT 39B8
SB_DQS#[2]	K6	M_B_DQS2_DN	OUT 39B8
SB_DQS#[3]	N3	M_B_DQS3_DN	OUT 39B8
SB_DQS#[4]	AN5	M_B_DQS4_DN	OUT 39B8
SB_DQS#[5]	AP9	M_B_DQS5_DN	OUT 39B8
SB_DQS#[6]	AK12	M_B_DQS6_DN	OUT 39B8
SB_DQS#[7]	AP15	M_B_DQS7_DN	OUT 39B8

SB_DQS[0]	C7	M_B_DQS0_DP	OUT 39B8
SB_DQS[1]	G3	M_B_DQS1_DP	OUT 39B8
SB_DQS[2]	J6	M_B_DQS2_DP	OUT 39B8
SB_DQS[3]	M3	M_B_DQS3_DP	OUT 39B8
SB_DQS[4]	AN6	M_B_DQS4_DP	OUT 39B8
SB_DQS[5]	AP8	M_B_DQS5_DP	OUT 39B8
SB_DQS[6]	AK11	M_B_DQS6_DP	OUT 39B8
SB_DQS[7]	AP14	M_B_DQS7_DP	OUT 39B8

M_B_A<15..0> OUT

SB_MA[0]	AA8	M_B_A<0>	0
SB_MA[1]	T7	M_B_A<1>	1
SB_MA[2]	R7	M_B_A<2>	2
SB_MA[3]	T6	M_B_A<3>	3
SB_MA[4]	T2	M_B_A<4>	4
SB_MA[5]	T4	M_B_A<5>	5
SB_MA[6]	T3	M_B_A<6>	6
SB_MA[7]	R2	M_B_A<7>	7
SB_MA[8]	T5	M_B_A<8>	8
SB_MA[9]	R3	M_B_A<9>	9
SB_MA[10]	AB7	M_B_A<10>	10
SB_MA[11]	R1	M_B_A<11>	11
SB_MA[12]	T1	M_B_A<12>	12
SB_MA[13]	AB10	M_B_A<13>	13
SB_MA[14]	R5	M_B_A<14>	14
SB_MA[15]	R4	M_B_A<15>	15

DDR SYSTEM MEMORY B

CN4500

LOTES_ACA_ZIF_069_P01_989P

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX	DATE 21-OCT-2002	SHEET 43 of 68	

POWER

REFERENCE 4500~4699(CPU)

CN4500

PVCORE

C4510 C4511 C4512 C4513 — 22UF_6.3V_5
C4514 C4515 C4516 C4517 — 22UF_6.3V_5
C4518 C4519 C4520 C4521 — 22UF_6.3V_5
C4522 C4523 C4524 C4525 — 22UF_6.3V_5

AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26
AF35 AF34 AF33 AF32 AF31 AF30 AF29 AF28 AF27 AF26
AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26
AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26
AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26
Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26
V35 V34 V33 V32 V31 V30 V29 V28 V27 V26
U35 U34 U33 U32 U31 U30 U29 U28 U27 U26
R35 R34 R33 R32 R31 R30 R29 R28 R27 R26
P35 P34 P33 P32 P31 P30 P29 P28 P27 P26

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10
VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20
VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30
VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40
VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50
VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60
VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70
VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80
VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90
VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

CORE SUPPLY

PEG AND DDR

AH13 AH10 AG10 AC10 Y10 U10 P10 L10 J14 J13 J12 J11 H14 H12 H11 G14 G13 G12 F14 F13 F12 F11 E14 E12
E11 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11
J23

VCCIO1 VCCIO2 VCCIO3 VCCIO4 VCCIO5 VCCIO6 VCCIO7 VCCIO8 VCCIO9 VCCIO10 VCCIO11 VCCIO12 VCCIO13 VCCIO14 VCCIO15 VCCIO16 VCCIO17 VCCIO18 VCCIO19 VCCIO20 VCCIO21 VCCIO22 VCCIO23 VCCIO24
VCCIO25 VCCIO26 VCCIO27 VCCIO28 VCCIO29 VCCIO30 VCCIO31 VCCIO32 VCCIO33 VCCIO34 VCCIO35 VCCIO36 VCCIO37 VCCIO38 VCCIO39 VCCIO40

P1V05S

C4531 C4532 C4533 C4534 C4535 C4536 C4537 C4542 C4541 C4540 — 22UF_6.3V_5

PLACE CLOSE TO CPU

P1V05S

R4528 130_1%_2
R4527 75_5%_2

SVID

SVID SIGNAL TO VR

VIDALERT# VIDSCLK VIDSOUT

AJ29 H_CPU_SVIDALRT#
AJ30 H_CPU_SVIDCLK
AJ28 H_CPU_SVIDDAT

R4529 43_5%_2
R4530 0_5%_2
R4531 0_5%_2

VR_SVID_ALERT# OUT 11C7
VR_SVID_CLK OUT 11A3 11C7
VR_SVID_DATA OUT 11A3 11C7

PVCORE

R4532 100_1%_2
R4533 100_1%_2

VCCSENSE OUT 11D6
VSSSENSE OUT 11D6

SENSE LINES

P1V05S

R4534 10_1%_2
R4535 10_1%_2

VCC_SENSE AJ35
VSS_SENSE AJ34
VCCIO_SENSE B10
VSSIO_SENSE A10

VCC_SENSE_VCCIO OUT 9B7
VSS_SENSE_VCCIO OUT 9B7

LOTES_ACA_ZIF_069_P01_989P

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
C	CS	1310xxxxx-0-0	X01

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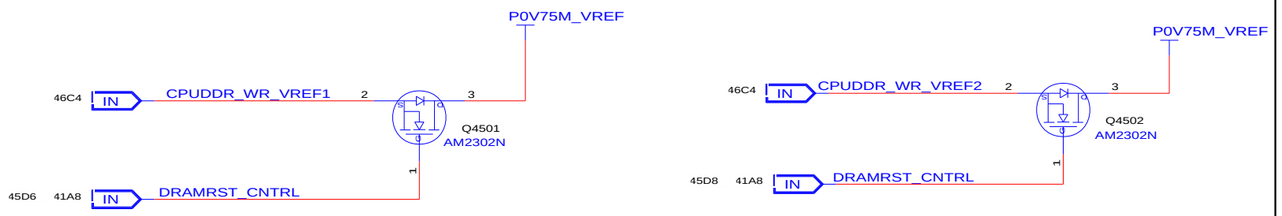
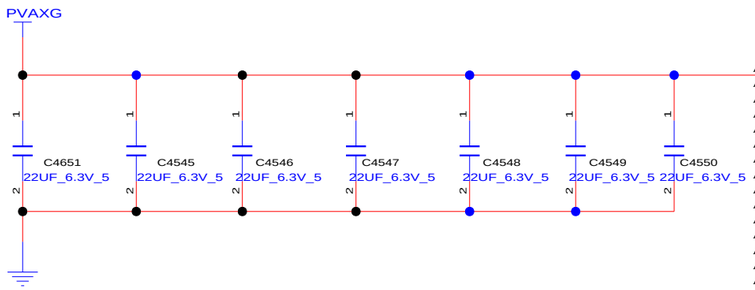
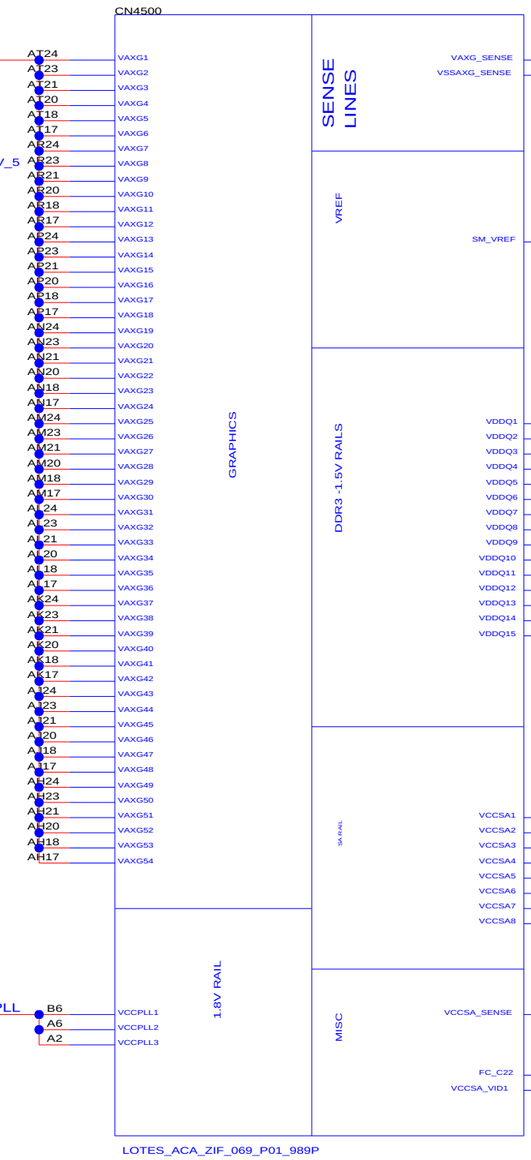
PROCESSOR DRIVEN VREF PATH WAS STUFFED BY DEFAULT:

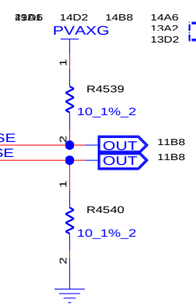
ROUTE WITH MIN. TRACE WIDTH OF 10 MILS

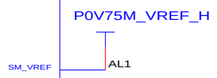


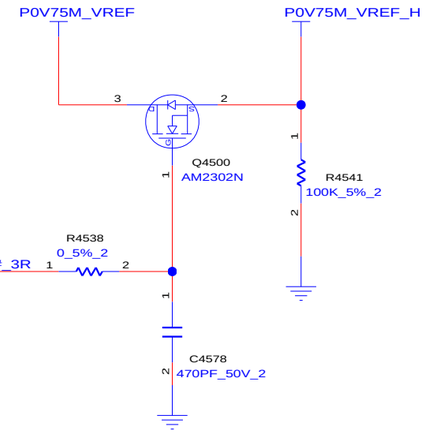
POWER



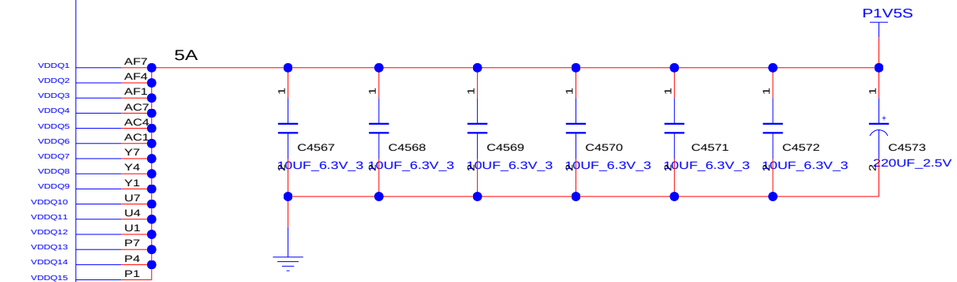


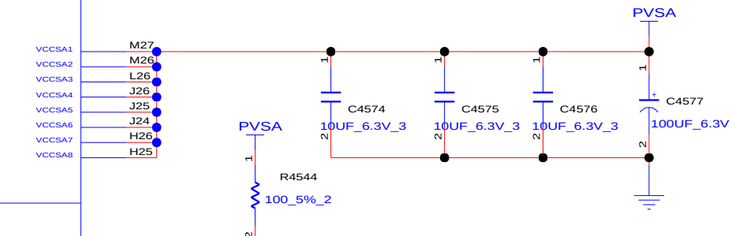




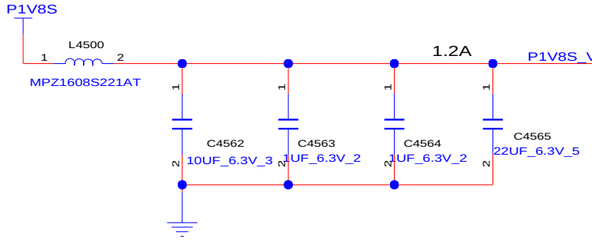


NOTE : DDR_WR_VREF SHOULD HAVE 20/20 MIL WHEREVER POSSIBLE





R4547
SNB:0 OHM
IVB:1K OHM



INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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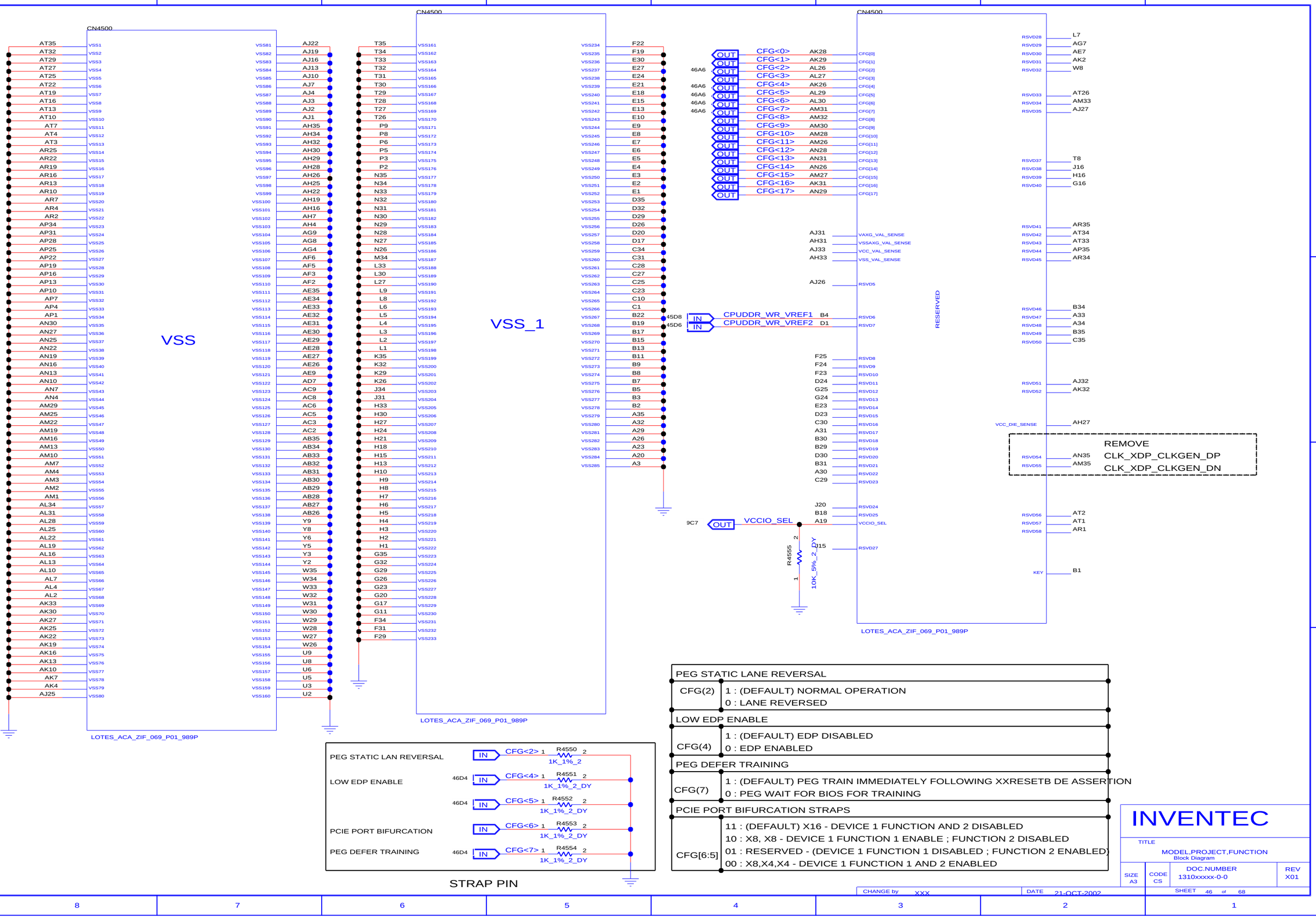
CN4500
VSS
AT35 AT32 AT29 AT27 AT25 AT22 AT19 AT16 AT13 AT10 AT7 AT4 AT3
AR25 AR22 AR19 AR16 AR13 AR10 AR7 AR4 AR2
AP34 AP31 AP28 AP25 AP22 AP19 AP16 AP13 AP10 AP7 AP4 AP1
AN30 AN27 AN25 AN22 AN19 AN16 AN13 AN10 AN7 AN4
AM29 AM25 AM22 AM19 AM16 AM13 AM10 AM7 AM4 AM3 AM2 AM1
AL34 AL31 AL28 AL25 AL22 AL19 AL16 AL13 AL10 AL7 AL4 AL2
AK33 AK30 AK27 AK25 AK22 AK19 AK16 AK13 AK10 AK7 AK4
AJ25
VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 VSS13 VSS14 VSS15 VSS16 VSS17 VSS18 VSS19 VSS20 VSS21 VSS22 VSS23 VSS24 VSS25 VSS26 VSS27 VSS28 VSS29 VSS30 VSS31 VSS32 VSS33 VSS34 VSS35 VSS36 VSS37 VSS38 VSS39 VSS40 VSS41 VSS42 VSS43 VSS44 VSS45 VSS46 VSS47 VSS48 VSS49 VSS50 VSS51 VSS52 VSS53 VSS54 VSS55 VSS56 VSS57 VSS58 VSS59 VSS60 VSS61 VSS62 VSS63 VSS64 VSS65 VSS66 VSS67 VSS68 VSS69 VSS70 VSS71 VSS72 VSS73 VSS74 VSS75 VSS76 VSS77 VSS78 VSS79 VSS80
VSS81 VSS82 VSS83 VSS84 VSS85 VSS86 VSS87 VSS88 VSS89 VSS90 VSS91 VSS92 VSS93 VSS94 VSS95 VSS96 VSS97 VSS98 VSS99 VSS100 VSS101 VSS102 VSS103 VSS104 VSS105 VSS106 VSS107 VSS108 VSS109 VSS110 VSS111 VSS112 VSS113 VSS114 VSS115 VSS116 VSS117 VSS118 VSS119 VSS120 VSS121 VSS122 VSS123 VSS124 VSS125 VSS126 VSS127 VSS128 VSS129 VSS130 VSS131 VSS132 VSS133 VSS134 VSS135 VSS136 VSS137 VSS138 VSS139 VSS140 VSS141 VSS142 VSS143 VSS144 VSS145 VSS146 VSS147 VSS148 VSS149 VSS150 VSS151 VSS152 VSS153 VSS154 VSS155 VSS156 VSS157 VSS158 VSS159 VSS160
AJ22 AJ19 AJ16 AJ13 AJ10 AJ7 AJ4 AJ3 AJ2 AJ1
AH35 AH34 AH32 AH30 AH29 AH28 AH26 AH25 AH22 AH19 AH16 AH7 AH4
AG9 AG8 AG4
AF6 AF5 AF3 AF2
AE35 AE34 AE33 AE32 AE31 AE30 AE29 AE28 AE27 AE26 AE9
AD7
AC9 AC8 AC6 AC5 AC3 AC2
AB35 AB34 AB33 AB32 AB31 AB30 AB29 AB28 AB27 AB26
Y9 Y8 Y6 Y5 Y3 Y2
W35 W34 W33 W32 W31 W30 W29 W28 W27 W26
U9 U8 U6 U5 U3 U2
LOTES_ACA_ZIF_069_P01_989P
CN4500
VSS_1
T35 T34 T33 T32 T31 T30 T29 T28 T27 T26
P9 P8 P6 P5 P3 P2
N35 N34 N33 N32 N31 N30 N29 N28 N27 N26
M34
L33 L30 L27 L9 L8 L6 L5 L4 L3 L2 L1
K35 K32 K29 K26
J34 J31
H33 H30 H27 H24 H21 H18 H15 H13 H10 H9 H8 H7 H6 H5 H4 H3 H2 H1
G35 G32 G29 G26 G23 G20 G17 G11
F34 F31 F29
VSS161 VSS162 VSS163 VSS164 VSS165 VSS166 VSS167 VSS168 VSS169 VSS170 VSS171 VSS172 VSS173 VSS174 VSS175 VSS176 VSS177 VSS178 VSS179 VSS180 VSS181 VSS182 VSS183 VSS184 VSS185 VSS186 VSS187 VSS188 VSS189 VSS190 VSS191 VSS192 VSS193 VSS194 VSS195 VSS196 VSS197 VSS198 VSS199 VSS200 VSS201 VSS202 VSS203 VSS204 VSS205 VSS206 VSS207 VSS208 VSS209 VSS210 VSS211 VSS212 VSS213 VSS214 VSS215 VSS216 VSS217 VSS218 VSS219 VSS220 VSS221 VSS222 VSS223 VSS224 VSS225 VSS226 VSS227 VSS228 VSS229 VSS230 VSS231 VSS232 VSS233
VSS234 VSS235 VSS236 VSS237 VSS238 VSS239 VSS240 VSS241 VSS242 VSS243 VSS244 VSS245 VSS246 VSS247 VSS248 VSS249 VSS250 VSS251 VSS252 VSS253 VSS254 VSS255 VSS256 VSS257 VSS258 VSS259 VSS260 VSS261 VSS262 VSS263 VSS264 VSS265 VSS266 VSS267 VSS268 VSS269 VSS270 VSS271 VSS272 VSS273 VSS274 VSS275 VSS276 VSS277 VSS278 VSS279 VSS280 VSS281 VSS282 VSS283 VSS284 VSS285
F22 F19 E30 E27 E24 E21 E18 E15 E13 E10 E9 E8 E7 E6 E5 E4 E3 E2 E1 D35 D32 D29 D26 D20 D17 C34 C31 C28 C27 C25 C23 C10 C1 B22 B19 B17 B15 B13 B11 B9 B8 B7 B5 B3 B2 A35 A32 A29 A26 A23 A20 A3
LOTES_ACA_ZIF_069_P01_989P
CN4500
RESERVED
46A6 CFG<0> AK28 CFG[0]
CFG<1> AK29 CFG[1]
46A6 CFG<2> AL26 CFG[2]
46A6 CFG<3> AL27 CFG[3]
46A6 CFG<4> AK26 CFG[4]
46A6 CFG<5> AL29 CFG[5]
46A6 CFG<6> AL30 CFG[6]
46A6 CFG<7> AM31 CFG[7]
CFG<8> AM32 CFG[8]
CFG<9> AM30 CFG[9]
CFG<10> AM28 CFG[10]
CFG<11> AM26 CFG[11]
CFG<12> AN28 CFG[12]
CFG<13> AN31 CFG[13]
CFG<14> AN26 CFG[14]
CFG<15> AM27 CFG[15]
CFG<16> AK31 CFG[16]
CFG<17> AN29 CFG[17]
OUT
AJ31 VAXG_VAL_SENSE
AH31 VSSAXG_VAL_SENSE
AJ33 VCC_VAL_SENSE
AH33 VSS_VAL_SENSE
AJ26 RSVD5
45D8 45D6 IN CPUDDR_WR_VREF1 B4 RSVD6
IN CPUDDR_WR_VREF2 D1 RSVD7
F25 RSVD8
F24 RSVD9
F23 RSVD10
D24 RSVD11
G25 RSVD12
G24 RSVD13
E23 RSVD14
D23 RSVD15
C30 RSVD16
A31 RSVD17
B30 RSVD18
B29 RSVD19
D30 RSVD20
B31 RSVD21
A30 RSVD22
C29 RSVD23
J20 RSVD24
B18 RSVD25
9C7 OUT VCCIO_SEL A19 VCCIO_SEL
R4555 2 1 10K_5%_2_DY D15 RSVD27
RSVD28 L7
RSVD29 AG7
RSVD30 AE7
RSVD31 AK2
RSVD32 W8
RSVD33 AT26
RSVD34 AM33
RSVD35 AJ27
RSVD37 T8
RSVD38 J16
RSVD39 H16
RSVD40 G16
RSVD41 AR35
RSVD42 AT34
RSVD43 AT33
RSVD44 AP35
RSVD45 AR34
RSVD46 B34
RSVD47 A33
RSVD48 A34
RSVD49 B35
RSVD50 C35
RSVD51 AJ32
RSVD52 AK32
VCC_DIE_SENSE AH27
REMOVE
RSVD54 AN35 CLK_XDP_CLKGEN_DP
RSVD55 AM35 CLK_XDP_CLKGEN_DN
RSVD56 AT2
RSVD57 AT1
RSVD58 AR1
KEY B1
LOTES_ACA_ZIF_069_P01_989P
PEG STATIC LAN REVERSAL
LOW EDP ENABLE
PCIE PORT BIFURCATION
PEG DEFER TRAINING
IN CFG<2> 1 R4550 2 1K_1%_2
46D4 IN CFG<4> 1 R4551 2 1K_1%_2_DY
46D4 IN CFG<5> 1 R4552 2 1K_1%_2_DY
IN CFG<6> 1 R4553 2 1K_1%_2_DY
46D4 IN CFG<7> 1 R4554 2 1K_1%_2_DY
STRAP PIN
PEG STATIC LANE REVERSAL
CFG(2) 1 : (DEFAULT) NORMAL OPERATION
0 : LANE REVERSED
LOW EDP ENABLE
CFG(4) 1 : (DEFAULT) EDP DISABLED
0 : EDP ENABLED
PEG DEFER TRAINING
CFG(7) 1 : (DEFAULT) PEG TRAIN IMMEDIATELY FOLLOWING XXRESETB DE ASSERTION
0 : PEG WAIT FOR BIOS FOR TRAINING
PCIE PORT BIFURCATION STRAPS
CFG[6:5] 11 : (DEFAULT) X16 - DEVICE 1 FUNCTION AND 2 DISABLED
10 : X8, X8 - DEVICE 1 FUNCTION 1 ENABLE ; FUNCTION 2 DISABLED
01 : RESERVED - (DEVICE 1 FUNCTION 1 DISABLED ; FUNCTION 2 ENABLED)
00 : X8,X4,X4 - DEVICE 1 FUNCTION 1 AND 2 ENABLED
INVENTEC
TITLE
MODEL,PROJECT,FUNCTION
Block Diagram
SIZE A3
CODE CS
DOC.NUMBER 1310xxxxx-0-0
REV X01
CHANGE by XXX
DATE 21-OCT-2002
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REFERENCE 4700~4949(PCH)

P3V3AL
P3V3_RTC
D4700
BAT54C_30V_0.2A
R4700
1K_5%_2
TP4705
TP30
CN4700
LOTES_AAA_BAT_063_P02_A_2P

P3V3_RTC
R4703
20K_1%_2
R4704
20K_1%_2
1UF_6.3V_2
C4701
C4700
1UF_6.3V_2
R4705
1M_5%_2
C4702
1UF_6.3V_2
P3V3_RTC
R4707
330K_5%_3
R4706
0_5%_2_DY

RTCX2
C4703
18PF_50V_2
R4708
10M_5%_2
X4700
32.768KHZ
RTCX1
C4704
18PF_50V_2

P3V3A
R4736
0_5%_2_DY
P1V05S
R4737
RSC_0402_DY
R4738
R4740
R4742
R4739
R4741
R4743
RSC_0402_DY
47A6 OUT PCH_TDI
47B6 OUT PCH_TMS
47A6 OUT PCH_TDO

P3V3S
R4744
10K_5%_2
BI 21E3 27B7

U4700
A20 RTCX1
C20 RTCX2
D20 RTCRST#
G22 SRTCRST#
K22 INTRUDER#
C17 INTVRMEN
RTC

INTVRMEN-INTEGRATE (SUS 1.05V VRM ENABLE
1:ENABLE INTERNAL VRS
0:ENABLE EXTERNAL VRS

STRAPPING

LPC
FWH0/LAD0 C38 LPC_3S_AD<0> BI 21E3 27C3
FWH1/LAD1 A38 LPC_3S_AD<1> BI 21E3 27C3
FWH2/LAD2 B37 LPC_3S_AD<2> BI 21E3 27C3
FWH3/LAD3 C37 LPC_3S_AD<3> BI 21E3 27C3
FWH4/LFRAME# D36 LPC_3S_FRAME# OUT 21E3 27C3
LDRQ0# E36
LDRQ1#/GPIO23 K36
SERIRQ V5 PCI_3S_SERIRQ BI 21E3 27B7

24A2 BI HDA_3S_BITCLK R4709 33_5%_2 HDA_3S_BITCLK_R N34 HDA_BCLK
24B2 BI HDA_3S_SYNC R4711 33_5%_2 HDA_3S_SYNC_R L34 HDA_SYNC
STRAPPING
24B1 OUT PCSPKR_PCH_3 T10 SPKR
24B2 OUT HDA_3S_RST# R4712 33_5%_2 HDA_3S_RST#_R K34 HDA_RST#
24A2 IN HDA_3S_SDIN0 E34 HDA_SDIN0
G34 HDA_SDIN1
C34 HDA_SDIN2
A34 HDA_SDIN3
IHDA

PCSPKR_PCH_3(NO REBOOT)
1 : NO REBOOT ENABLED
0 : (DEFAULT) NO REBOOT DISABLED

STRAP
47B8 21D3 IN FLASH_OVERRIDE R4715 1K_5%_2
24A2 OUT HDA_3S_SDOUT R4716 33_5%_2 A36 HDA_SDO
STRAPPING
C36 HDA_DOCK_EN#/GPIO33
IN EC_SMI N32 HDA_DOCK_RST#/GPIO13

FLASH OVERRIDE
FLASH DESCRIPTOR SECURITY OVERIDE
1:ENABLE
0:DISABLE : (DEFAULT INTERNAL PULL-DOWN)
21D3 47B7 OUT FLASH_OVERRIDE R4720 10K_5%_2_DY P3V3A

OUT HDA_3S_SYNC_R R4714 1K_5%_2
HDA_3S_SYNC_R(PLL ODVR VOLTAGE)
1 : VCC VRM = 1.6V
0 : VCC VRM = 1.8V(DEFAULT)

R4718
RSC_0402_DY
OUT TP4720 TP30 PCH_TCK J3 JTAG_TCK
47D3 OUT TP4721 TP30 PCH_TMS H7 JTAG_TMS
47D3 OUT TP4722 TP30 PCH_TDI K5 JTAG_TDI
47D3 OUT TP4723 TP30 PCH_TDO H1 JTAG_TDO
JTAG

21D6 21C7 OUT EC_SPI_CLK T3 SPI_CLK
21D6 21C8 OUT EC_SPI_CS0# Y14 SPI_CS0#
21C8 OUT EC_SPI_CS1# T1 SPI_CS1#
21C7 21C6 OUT EC_SPI_SI V4 SPI_MOSI
21C8 21C6 OUT EC_SPI_SO U3 SPI_MISO
SPI
R4734
RSC_0402_DY

SATA 6G
SATA0RXN AM3
SATA0RXP AM1
SATA0TXN AP7
SATA0TXP AP5
SATA1RXN AM10 SATA_HDD_RX_DN IN 29D5
SATA1RXP AM8 SATA_HDD_RX_DP IN 29D5
SATA1TXN AP11 SATA_HDD_TX_DN OUT 29D5
SATA1TXP AP10 SATA_HDD_TX_DP OUT 29D5
SATA2RXN AD7 SATA_MINICARD_RX_DN IN 28C7
SATA2RXP AD5 SATA_MINICARD_RX_DP IN 28C7
SATA2TXN AH5 SATA_MINICARD_TX_DN OUT 28C7
SATA2TXP AH4 SATA_MINICARD_TX_DP OUT 28C7
SATA3RXN AB8
SATA3RXP AB10
SATA3TXN AF3
SATA3TXP AF1
SATA4RXN Y7
SATA4RXP Y5
SATA4TXN AD3
SATA4TXP AD1
SATA5RXN Y3 SATA_ODD_RX_DN IN 29A7
SATA5RXP Y1 SATA_ODD_RX_DP IN 29A7
SATA5TXN AB3 SATA_ODD_TX_DN OUT 29A7
SATA5TXP AB1 SATA_ODD_TX_DP OUT 29A7
SATA

SATAICOMPO Y11
SATAICOMPI Y10 P1V05S_SATARCOMPO R4747 37.4_1%_2 P1V05S
SATA3RCOMPO AB12
SATA3COMPI AB13 P1V05S_SATA3RCOMPO R4748 49.9_1%_2 P1V05S
SATA3RBIAS AH1 R4749 750_1%_2
SATALED# P3
SATA0GP/GPIO21 V14
SATA1GP/GPIO19 STRAPPING P1
R4751 R4750 R4752 10K_5%_2 P3V3S

ITL_PANTHERPOINT_FCBGA_989P

INVENTEC

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REFERENCE 4700~4949(PCH)

U4700

PCI-E*

PCIE_LAN_RX_DN / PCIE_LAN_RX_DP / PCIE_LAN_TX_DN / PCIE_LAN_TX_DP — 0.1UF_16V_2 — PCIE_LAN_TX_C_DN / PCIE_LAN_TX_C_DP

PCIE_WLAN_RX_DN / PCIE_WLAN_RX_DP / PCIE_WLAN_TX_DN / PCIE_WLAN_TX_DP — 0.1UF_16V_2 — PCIE_WLAN_TX_C_DN / PCIE_WLAN_TX_C_DP

PCIE_USB3_RX_DN / PCIE_USB3_RX_DP / PCIE_USB3_TX_DN / PCIE_USB3_TX_DP — 0.1UF_16V_2 — PCIE_USB3_TX_C_DN / PCIE_USB3_TX_C_DP

CLKREQ_LAN# — R4775 10K_5%_2_DY

CLKREQ_WLAN# — R4776 10K_5%_2_DY

CLKREQ_LAN# — R4773 10K_5%_2 — P3V3A

CLKREQ_WLAN# — R4772 10K_5%_2 — P3V3S

CLOCK TERMINATION FOR FICM
STUFF FOR INTEGRATED CLK

CLKIN_DMI_PCH_DN — R4777 10K_5%_2
CLKIN_DMI_PCH_DP — R4778 10K_5%_2
CLKIN_BUF_DOT96_DN — R4779 10K_5%_2
CLKIN_BUF_DOT96_DP — R4780 10K_5%_2
CLKIN_PCH14 — R4781 10K_5%_2
CLKIN_SATA1_DP — R4782 10K_5%_2
CLKIN_SATA1_DN — R4783 10K_5%_2

CLK_PCIE_LAN_DN / CLK_PCIE_LAN_DP
CLKREQ_LAN# — PCIECLKRQ0#/GPIO73
CLK_PCIE_WLAN_DN / CLK_PCIE_WLAN_DP
CLKREQ_WLAN# — PCIECLKRQ1#/GPIO18
CLK_PCIE_USB3_DN / CLK_PCIE_USB3_DP
CLKREQ_USB3# — PCIECLKRQ2#/GPIO20

TP4703 / TP4704

P3V3A — R4789 10K_5%_2_DY — PCIECLKRQ3#/GPIO25
R4790 10K_5%_2_DY — PCIECLKRQ4#/GPIO26
R4791 10K_5%_2_DY — PCIECLKRQ5#/GPIO44
R4792 10K_5%_2_DY — PEG_B_CLKRQ#/GPIO56
R4793 10K_5%_2_DY — PCIECLKRQ6#/GPIO45
R4794 10K_5%_2_DY — PCIECLKRQ7#/GPIO46

P3V3S / P3V3A / P5V0S
R4784 2.2K_5%_2 / R4785 2.2K_5%_2 / R4786 2.2K_5%_2 / R4787 2.2K_5%_2
PCH_3S_SMCLK — Q4700 SSM3K7002BFU
PCH_3A_SMCLK
PCH_3A_SMDATA — Q4701 SSM3K7002BFU
PCH_3S_SMDATA

SMBUS

SMB_ALERT# — R4795 10K_5%_2 — P3V3A
SMBCLK — PCH_3A_SMCLK
SMBDATA — PCH_3A_SMDATA
SML0ALERT#/GPIO60 — DRAMRST_CNTRL_PCH
SML0CLK — PCH_3A_ALERT_CLK
SML0DATA — PCH_3A_ALERT_DAT
SML1ALERT#/PCHHOT#/GPIO74 — SML1ALERT#
SML1CLK/GPIO58 — SML1_CLK
SML1DATA/GPIO75 — SML1_DATA

Link Controller

CL_CLK1 — M7
CL_DATA1 — T11
CL_RST1# — P10

CLKREQ_GPU# — R4753 10K_5%_2 — P3V3A

PEG_A_CLKRQ#/GPIO47 — CLKREQ_GPU#
CLKOUT_PEG_A_N / CLKOUT_PEG_A_P — CLK_PEG_REF_DN / CLK_PEG_REF_DP
CLKOUT_DMI_N / CLKOUT_DMI_P — CLK_DMI_PCH_DN / CLK_DMI_PCH_DP
CLKOUT_DP_N / CLKOUT_DP_P — AM12 / AM13
CLKIN_DMI_N / CLKIN_DMI_P — CLKIN_DMI_PCH_DN / CLKIN_DMI_PCH_DP
CLKIN_GND1_N / CLKIN_GND1_P — BJ30 / BG30 — R4837 10K_5%_2
CLKIN_DOT_96N / CLKIN_DOT_96P — CLKIN_BUF_DOT96_DN / CLKIN_BUF_DOT96_DP
CLKIN_SATA_N / CLKIN_SATA_P — CLKIN_SATA1_DN / CLKIN_SATA1_DP
REFCLK14IN — CLKIN_PCH14
CLKIN_PCILOOPBACK — CLKIN_PCI_FB
XTAL25_IN / XTAL25_OUT
XCLK_RCOMP — R4802 90.9_1%_2 — P1V05S — CLOSE TO PCH

CLOCKS

FLEX CLOCKS

CLKOUTFLEX0/GPIO64 — TP4700
CLKOUTFLEX1/GPIO65 — TP4701
CLKOUTFLEX2/GPIO66 — TP4702
CLKOUTFLEX3/GPIO67

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SML1ALERT# — R4796 10K_5%_2 — P3V3A
R4797 2.2K_5%_2
R4798 2.2K_5%_2
PCH_3A_ALERT_CLK — R4799 2.2K_5%_2
PCH_3A_ALERT_DAT — R4800 2.2K_5%_2
SML1_CLK — Q4702 SSM3K7002FU_DY
EC_SMB3_CLK
SML1_DATA — Q4703 SSM3K7002FU_DY
EC_SMB3_DATA

XTAL25_OUT — R4801 1M_5%_2 — XTAL25_IN
X4701 25MHZ
C4728 18PF_50V_2 / C4729 18PF_50V_2

SMB_ALERT# — B500 PASSWORD_0805

INVENTEC

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DSWVRMEN - DEEP S4/S5 WELL ON-DIE VOLTAGE REGULATOR ENABLE

HIGH-ENABLED(DEFAULT)
LOW-DISABLED

U4700

DMI

FDI

System Power Management

ITL_PANTHERPOINT_FCBGA_989P

STRAPPING

P1V05S
R4812 49.9_1%_2

R4814 750_1%_2

P3V3S
R4815 10K_5%_2

R4816 0_5%_2_DY

P3V3A
R4820 10K_5%_2_DY

R4822 8.2K_5%_2

R4823 10K_5%_2

P3V3_RTC
R4829 330K_5%_2
R4830 330K_5%_2_DY

P3V3A
R4832 1K_5%_2_DY

R4831 0_5%_2

P3V3_LDO
R4883 10K_5%_2_DY

R4834 10K_5%_2

R4710 100K_5%_2

Q4713 SSM3K7002FU_DY

Q4714 SSM3K7002BFU

U4704 TC7SZ08FU

D4706 BAT54_30V_0.2A

D4707 BAT54_30V_0.2A

R4824 10K_5%_2

R4825 10K_5%_2

R4826 10K_5%_2

R4827 10K_5%_2

R4828 8.2K_5%_2

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REFERENCE 4700~4949(PCH)

P3V3S

R4856 2.2K_5%_2

R4857 2.2K_5%_2

R4855 100K_5%_2

PCH_LVDS_DDCDATA - LVDS DETECT

HIGH-LVDS ENABLED

LOW-LVDS DISABLED (DEFAULT)

R4858 2.37K_1%_2

U4700

21E7 OUT PCH_LCM_BKLTEN J47 L_BKLTEN

34D7 OUT PCH_LCM_VDDEN M45 L_VDD_EN

34B5 OUT PCH_INV_PWM_3 P45 L_BKLTCTL

34C5 OUT PCH_LVDS_DDCCLK T40 L_DDC_CLK

34C5 OUT PCH_LVDS_DDCDATA K47 L_DDC_DATA

T45 L_CTRL_CLK

P39 L_CTRL_DATA

WHEN (#1): LVDS IS DETECTED

AF37 LVD_IBG

AF36 LVD_VBG

AE48 LVD_VREFH

AE47 LVD_VREFL

LVDS

34B8 OUT PCH_LVDS_TXCL_DN AK39 LVDSA_CLK#

34B8 OUT PCH_LVDS_TXCL_DP AK40 LVDSA_CLK

34B8 OUT PCH_LVDS_TXDL0_DN AN48 LVDSA_DATA#0

34B8 OUT PCH_LVDS_TXDL1_DN AM47 LVDSA_DATA#1

34B8 OUT PCH_LVDS_TXDL2_DN AK47 LVDSA_DATA#2

AJ48 LVDSA_DATA#3

34B8 OUT PCH_LVDS_TXDL0_DP AN47 LVDSA_DATA0

34B8 OUT PCH_LVDS_TXDL1_DP AM49 LVDSA_DATA1

34B8 OUT PCH_LVDS_TXDL2_DP AK49 LVDSA_DATA2

AJ47 LVDSA_DATA3

AF40 LVDSB_CLK#

AF39 LVDSB_CLK

AH45 LVDSB_DATA#0

AH47 LVDSB_DATA#1

AF49 LVDSB_DATA#2

AF45 LVDSB_DATA#3

AH43 LVDSB_DATA0

AH49 LVDSB_DATA1

AF47 LVDSB_DATA2

AF43 LVDSB_DATA3

Digital Display Interface

SDVO_TVCLKINN AP43

SDVO_TVCLKINP AP45

SDVO_STALLN AM42

SDVO_STALLP AM40

SDVO_INTN AP39

SDVO_INTP AP40

SDVO_CTRLCLK P38

SDVO_CTRLDATA M39

DDPB_AUXN AT49

DDPB_AUXP AT47

DDPB_HPD AT40

DDPB_0N AV42

DDPB_0P AV40

DDPB_1N AV45

DDPB_1P AV46

DDPB_2N AU48

DDPB_2P AU47

DDPB_3N AV47

DDPB_3P AV49

DDPC_CTRLCLK P46 PCH_HDMI_DDCCLK BI 36D8

DDPC_CTRLDATA P42 PCH_HDMI_DDCDATA BI 36D8

DDPC_AUXN AP47

DDPC_AUXP AP49

DDPC_HPD AT38 PCH_HPDET IN 36B5

DDPC_0N AY47 PCH_HDMI_TX2_DN OUT 36A5

DDPC_0P AY49 PCH_HDMI_TX2_DP OUT 36A5

DDPC_1N AY43 PCH_HDMI_TX1_DN OUT 36A5

DDPC_1P AY45 PCH_HDMI_TX1_DP OUT 36A5

DDPC_2N BA47 PCH_HDMI_TX0_DN OUT 36A5

DDPC_2P BA48 PCH_HDMI_TX0_DP OUT 36A5

DDPC_3N BB47 PCH_HDMI_TXC_DN OUT 36A5

DDPC_3P BB49 PCH_HDMI_TXC_DP OUT 36A5

DDPD_CTRLCLK M43

DDPD_CTRLDATA M36

DDPD_AUXN AT45

DDPD_AUXP AT43

DDPD_HPD BH41

DDPD_0N BB43

DDPD_0P BB45

DDPD_1N BF44

DDPD_1P BE44

DDPD_2N BF42

DDPD_2P BE42

DDPD_3N BJ42

DDPD_3P BG42

35D8 OUT PCH_CRTB N48 CRT_BLUE

35D8 OUT PCH_CRTG P49 CRT_GREEN

35D8 OUT PCH_CRTR T49 CRT_RED

CRT

35A2 OUT PCH_CRT_DDCCLK T39 CRT_DDC_CLK

35A2 OUT PCH_CRT_DDCDATA M40 CRT_DDC_DATA

35B2 OUT PCH_CRT_HSYNC M47 CRT_HSYNC

35B2 OUT PCH_CRT_VSYNC M49 CRT_VSYNC

T43 DAC_IREF

T42 CRT_IRTN

R4859 150_1%_2

R4860 150_1%_2

R4861 150_1%_2

R4862 1K_1%_2

CLOSE TO PCH

ITL_PANTHERPOINT_FCBGA_989P

INVENTEC

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Block Diagram

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A3	CS	1310xxxxx-0-0	X01

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REFERENCE 4700~4949(PCH)

GPIO51 BBS_BIT1	GPIO19 BBS_BIT0	BOOT BIOS DESTINATION
0	1	RESERVED(NAND)
1	0	------
1	1	SPI (DEFAULT)
0	0	LPC

P3V3S

R4874 1 2 8.2K_5%_2 PCI_3S_INTA# BI 51B6
R4875 1 2 8.2K_5%_2 PCI_3S_INTB# BI 51B6
R4876 1 2 8.2K_5%_2 PCI_3S_INTC# BI 51B6
R4877 1 2 8.2K_5%_2 PCI_3S_INTD# BI 51B6
R4878 1 2 8.2K_5%_2 RUNSCI0#_3 IN 21E3 52D6

R4880 1 2 10K_5%_2 DGPU_HOLD_RST# IN 51B6
R4881 1 2 10K_5%_2 PCI_3S_REQ2# IN 51B6
R4882 1 2 10K_5%_2 DGPU_PWR_EN# IN 51B6

R4838 1 2 10K_5%_2 SATA_ODD_DA# IN 29A5 51B6
R4956 1 2 10K_5%_2 PCI_3S_PIRQG# IN 51B6
R4879 1 2 10K_5%_2 PCI_3S_PIRQH# IN 51B6

BBS STRAPING

BBS_BIT1
STP_A16OVR
R4885 1K_5%_2_DY
R4886 1K_5%_2_DY

LOW=A16 SWAP OVERRIDE
STP_A16OVR
TOP-BLOCK SWAP OVERRIDE
HIGH=DEFAULT

P3V3A
R4887 2 P3V3A_PME# K10 PME# INT. PU 20K
10K_5%_2_DY

41C7 PLT_RST# BI C6 PLTRST#

P3V3A
U4705 TC7SZ08FU
28C3 27C3 21E3 27C7 57A6 BUF_PLT_RST# BI
R4888 100K_5%_2

21E3 OUT CLK_KBPCI R4889 22_5%_2 CLK_KBPCI_R H49 CLKOUT_PCI0
48A3 OUT CLKIN_PCI_FB R4890 22_5%_2 CLK_PCI_FB_R H43 CLKOUT_PCI1
J48 CLKOUT_PCI2
27C7 OUT CLK_PCI_DEBUG R4891 22_5%_2 TP24 TP4717 K42 CLKOUT_PCI3
CLK_PCI_DEBUG_R H40 CLKOUT_PCI4

ROUTE WITH 90 OHMS IMPEDANCE
TOTAL LENGTH NO LONGER THAN 11 INCHES

32D7 33B5 BI USB3_PCH_RX1_DN BE28 USB3RN1
33B5 BI USB3_PCH_RX2_DN BC30 USB3RN2
BE32 USB3RN3
BJ32 USB3RN4
32D7 33B5 BI USB3_PCH_RX1_DP BC28 USB3RP1
33B5 BI USB3_PCH_RX2_DP BE30 USB3RP2
BF32 USB3RP3
BG32 USB3RP4
32D7 33B5 BI USB3_PCH_TX1_DN AV26 USB3TN1
33B5 BI USB3_PCH_TX2_DN BB26 USB3TN2
AU28 USB3TN3
AY30 USB3TN4
32D7 33B5 BI USB3_PCH_TX1_DP AU26 USB3TP1
33B5 BI USB3_PCH_TX2_DP AY26 USB3TP2
AV28 USB3TP3
AW30 USB3TP4

51D7 BI PCI_3S_INTA# K40 PIRQA#
51C7 BI PCI_3S_INTB# K38 PIRQB#
51C7 BI PCI_3S_INTC# H38 PIRQC#
51C7 BI PCI_3S_INTD# G38 PIRQD#
51C7 OUT DGPU_HOLD_RST# C46 REQ1#/GPIO50
51C7 OUT PCI_3S_REQ2# C44 REQ2#/GPIO52
51C7 OUT DGPU_PWR_EN# E40 REQ3#/GPIO54
D47 GNT1#/GPIO51
E42 GNT2#/GPIO53
F46 GNT3#/GPIO55
USED AS GPIO ONLY. INT. PU 20K

31C7 BI USB3_SMI# G42 PIRQE#/GPIO2
31C6 29A5 BI SATA_ODD_DA# G40 PIRQF#/GPIO3
51C7 BI PCI_3S_PIRQG# C42 PIRQG#/GPIO4
51C7 51B7 BI PCI_3S_PIRQH# D44 PIRQH#/GPIO5

U4700
BG26 TP1
BJ26 TP2
BH25 TP3
BJ16 TP4
BG16 TP5
AH38 TP6
AH37 TP7
AK43 TP8
AK45 TP9
C18 TP10
N30 TP11
H3 TP12
AH12 TP13
AM4 TP14
AM5 TP15
Y13 TP16
K24 TP17
L24 TP18
AB46 TP19
AB45 TP20
B21 TP21
M20 TP22
AY16 TP23
BG46 TP24

RSVD
NVRAM
PCI
USB
ITL_PANTHERPOINT_FCBGA_989P

RSVD1 AY7
RSVD2 AV7
RSVD3 AU3
RSVD4 BG4
RSVD5 AT10
RSVD6 BC8
RSVD7 AU2
RSVD8 AT4
RSVD9 AT3
RSVD10 AT1
RSVD11 AY3
RSVD12 AT5
RSVD13 AV3
RSVD14 AV1
RSVD15 BB1
RSVD16 BA3
RSVD17 BB5
RSVD18 BB3
RSVD19 BB7
RSVD20 BE8
RSVD21 BD4
RSVD22 BF6
RSVD23 AV5
RSVD24 AV10
RSVD25 AT8
RSVD26 AY5
RSVD27 BA2
RSVD28 AT12
RSVD29 BF3

NOTE:
USB2.0/3.0 COMBO-USB2.0 PORT 0,1 MAPPEDUSB3.0 PORT 1,2

DEBUG PORT
USBP0N C24 USB_P0_DN BI 32C8 32B8
USBP0P A24 USB_P0_DP BI 32C8 32B8
USBP1N C25 USB_P1_DN BI 33C5
USBP1P B25 USB_P1_DP BI 33C5
USBP2N C26 USB_P2_DN BI 30C6
USBP2P A26 USB_P2_DP BI 30C6

P0.P1 RESERVER FOR USB3.0

USBP3N K28
USBP3P H28
USBP4N E28
USBP4P D28
USBP5N C28
USBP5P A28
USBP6N C29
USBP6P B29
USBP7N N28
USBP7P M28
USBP8N L30 USB_CR_DN BI 26A8
USBP8P K30 USB_CR_DP BI 26A8 CARD READER
USBP9N G30 USB_WLAN_DN BI 27B3
USBP9P E30 USB_WLAN_DP BI 27B3 WLAN
USBP10N C30 USB_CAM_DN BI 34B3
USBP10P A30 USB_CAM_DP BI 34B3 WEBCAM
USBP11N L32
USBP11P K32
USBP12N G32
USBP12P E32
USBP13N C32 USB_3G_DN BI 28C3
USBP13P A32 USB_3G_DP BI 28C3 3G

USBRBIAS# C33 R4835 1 2 22.6_1%_3 CLOSE TO PCH
USBRBIAS B33

OC0#/GPIO59 A14 MACHINE_ID0 IN 51A4 51A5
OC1#/GPIO40 K20 MACHINE_ID1 IN 51A4 51A5
OC2#/GPIO41 B17 MACHINE_ID2 IN 51A4 51A5
OC3#/GPIO42 C16 MACHINE_ID3 IN 51A4 51A5
OC4#/GPIO43 L16 MACHINE_ID4 IN 51A4 51A5
OC5#/GPIO9 A16 MACHINE_ID5 IN 51A4 51A5
OC6#/GPIO10 D14 MACHINE_ID6 IN 51A4 51A5
OC7#/GPIO14 C14 MACHINE_ID1_DB IN 51A4 51A5

TO BE USED AS GPIO

P3V3A

51A4 51A2 OUT MACHINE_ID0 R4892 1 2 10K_5%_2_DY
51A4 51A2 OUT MACHINE_ID1 R4893 1 2 10K_5%_2_DY
51A4 51A2 OUT MACHINE_ID2 R4894 1 2 10K_5%_2_DY
51A4 51A2 OUT MACHINE_ID3 R4895 1 2 10K_5%_2_DY
51A4 51A2 OUT MACHINE_ID4 R4896 1 2 10K_5%_2_DY
51A4 51A2 OUT MACHINE_ID5 R4897 1 2 10K_5%_2_DY
51A4 51A2 OUT MACHINE_ID6 R4898 1 2 10K_5%_2_DY
51A4 51A2 OUT MACHINE_ID1_DB R4899 1 2 10K_5%_2_DY

NOTE:10K_5%(60130B1030ZT)

51A5 51A2 OUT MACHINE_ID0 R4900 1 2 10K_5%_2_DY
51A5 51A2 OUT MACHINE_ID1 R4901 1 2 10K_5%_2_DY
51A5 51A2 OUT MACHINE_ID2 R4902 1 2 10K_5%_2_DY
51A7 51A5 OUT MACHINE_ID3 R4903 1 2 10K_5%_2_DY
MACHINE_ID4 R4904 1 2 10K_5%_2_DY
51A5 51A2 OUT MACHINE_ID5 R4905 1 2 10K_5%_2_DY
MACHINE_ID6 R4906 1 2 10K_5%_2_DY
51A2 51A5 OUT MACHINE_ID1_DB R4907 1 2 10K_5%_2_DY

NOTE:10K_5%(60130B1030ZT)

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REFERENCE 4700~4949(PCH)

P3V3A
R4927 1 2 10K_5%_2_DY PCH_GPIO6 OUT 52D6
R4908 1 2 1K_5%_2_DY PCH_GPIO15 OUT 52C6
R4909 1 2 10K_5%_2 PCH_GPIO8 OUT 52D6
R4910 1 2 10K_5%_2_DY PCH_GPIO12 OUT 52C6

P3V3S
R4916 1 2 10K_5%_2_DY PCH_GPIO22 OUT 52C6 52C7
R4917 1 2 10K_5%_2_DY PCH_GPIO38 OUT 52B6
R4915 1 2 10K_5%_2_DY PCH_GPIO16 OUT 52C6
R4919 1 2 10K_5%_2 SATA_ODD_PRSNT# OUT 29A5 52B6

R4727 1 2 10K_5%_2_DY PCH_GPIO23 OUT 52C6 52D7

GFX_CRB_DET(GPIO39)
INTERNAL GFX :100K PD
EXTERNAL GFX :10K PU
P3V3S
R4920 1 2 10K_5%_2_DY PCH_GPIO39 OUT 52B6
R4926 1 2 100K_5%_2

FDI_OVRVLTG(GPIO37)
LOW- TX,RXTERMINATED TO SAME VOLTAGE
(DC COUPLING MODE) DEFAULT
P3V3S
R4934 1 2 1K_5%_2_DY PCH_GPIO37 OUT 52B6
R4935 1 2 100K_5%_2

PLL_ODVR_EN(PLL ON DIE VR ENABLE)(GPIO28)
HIGH-ENABLED (DEFAULT)
LOW-DISABLED
P3V3A
R4950 1 2 10K_5%_2 PLL_ODVR_EN IN 52C6
R4936 1 2 10K_5%_2_DY
STRAP

P3V3S
R4721 1 2 33K_5%_2_DY

U4700

GPIO

IN MSATA_DET T7 BMBUSY#/GPIO0
28C2 IN 3G_ON# A42 TACH1/GPIO1
52D7 IN PCH_GPIO6 H36 TACH2/GPIO6
51C7 21E3 IN RUNSCI0#_3 E38 TACH3/GPIO7
52D7 OUT PCH_GPIO8 C10 GPIO8 INT. PU 20K
52D7 OUT PCH_GPIO12 C4 LAN_PHY_PWR_CTRL/GPIO12
52D7 OUT PCH_GPIO15 G2 GPIO15 INT. PD 20K STRAPPING
52D7 OUT PCH_GPIO16 U2 SATA4GP/GPIO16 INT. PU 20K
13C8 13B2 IN DGPU_PWRGD D40 TACH0/GPIO17
52D7 52C7 OUT PCH_GPIO22 T5 SCLOCK/GPIO22
OUT KBLED_ID E8 GPIO24
R4928 1 2 10K_5%_2_DY E16 GPIO27 INT.PD 20K
52A7 OUT PLL_ODVR_EN STRAPPING P8 GPIO28 INT. PU 20K
P3V3S
R4929 1 2 10K_5%_2_DY K1 STP_PCI#/GPIO34
R4930 1 2 10K_5%_2_DY K4 GPIO35
R4932 1 2 10K_5%_2_DY V8 SATA2GP/GPIO36
52B7 OUT PCH_GPIO37 STRAPPING M5 SATA3GP/GPIO37 INT. PD 20K
52D7 OUT PCH_GPIO38 N2 SLOAD/GPIO38
52B7 OUT PCH_GPIO39 STRAPPING M3 SDATAOUT0/GPIO39
TP4907 1 TP24 V13 SDATAOUT1/GPIO48 STRAPPING
52D7 29A5 OUT SATA_ODD_PRSNT# V3 SATA5GP/GPIO49/TEMP_ALERT#
27C7 27B7 OUT BTIFON# D6 GPIO57

CPU/MISC

TACH4/GPIO68 C40 SATA_ODD_PWREN OUT 29B8
TACH5/GPIO69 B41 R4724 1 2 10K_5%_2_DY
TACH6/GPIO70 C41 R4725 1 2 10K_5%_2_DY
TACH7/GPIO71 A40 R4726 1 2 10K_5%_2_DY
INT. PU 20K
P3V3S

A20GATE P4 EC_3S_A20GATE IN 21E2
PECI AU16 PCH_PECI 1 R4940 2 0_5%_2_DY H_PECI OUT 21A6 41D5
RCIN# P5 KBRST# IN 21D2
PROCPWRGD AY11 H_CPUPWRGD OUT 41C5
THRMTRIP# AY10 THRMTRIP#_R
INIT3_3V# T14
STRAPPING TVS AY1
TS_VSS1 AH8
TS_VSS2 AK11
TS_VSS3 AH10
TS_VSS4 AK10
NC_1 P37
FOLLOW EDS1.0

P1V05S
R4942 1 2 56_5%_2
R4941 1 2 390_5%_2
R4943 1 2 0_5%_2_DY
BOTH THESE SHOULD BE CLOSE TO PCH
P1V05S
R4944 1 2 56_5%_2
PM_THRMTRIP# IN 40A4 41D5

NV_CLE OUT 41D6

NCTF

A4 VSS_NCTF_1
A44 VSS_NCTF_2
A45 VSS_NCTF_3
A46 VSS_NCTF_4
A5 VSS_NCTF_5
A6 VSS_NCTF_6
B3 VSS_NCTF_7
B47 VSS_NCTF_8
BD1 VSS_NCTF_9
BD49 VSS_NCTF_10
BE1 VSS_NCTF_11
BE49 VSS_NCTF_12
BF1 VSS_NCTF_13
BF49 VSS_NCTF_14
VSS_NCTF_15 BG2
VSS_NCTF_16 BG48
VSS_NCTF_17 BH3
VSS_NCTF_18 BH47
VSS_NCTF_19 BJ4
VSS_NCTF_20 BJ44
VSS_NCTF_21 BJ45
VSS_NCTF_22 BJ46
VSS_NCTF_23 BJ5
VSS_NCTF_24 BJ6
VSS_NCTF_25 C2
VSS_NCTF_26 C48
VSS_NCTF_27 D1
VSS_NCTF_28 D49
VSS_NCTF_29 E1
VSS_NCTF_30 E49
VSS_NCTF_31 F1
VSS_NCTF_32 F49
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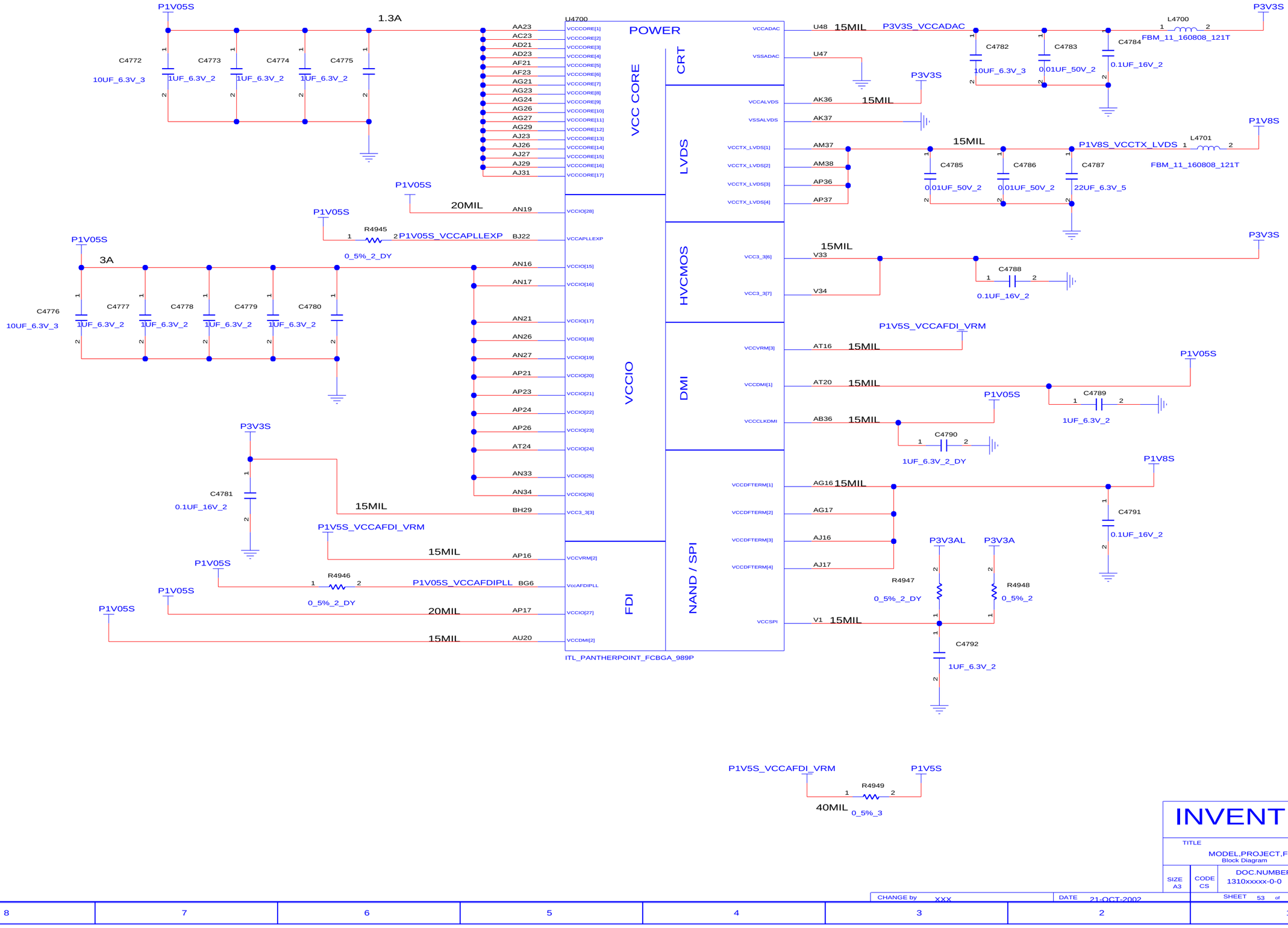

INVENTEC

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REFERENCE 4700~4949(PCH)

POWER

Clock and Miscellaneous

USB

PCI/GPIO/LPC

SATA

MISC

CPU

RTC

HDA

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TITLE: MODEL,PROJECT,FUNCTION
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REFERENCE 4700~4949(PCH)

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H5	VSS[0]	VSS[80]	AK38
AA17	VSS[1]	VSS[81]	AK4
AA2	VSS[2]	VSS[82]	AK42
AA3	VSS[3]	VSS[83]	AK46
AA33	VSS[4]	VSS[84]	AK8
AA34	VSS[5]	VSS[85]	AL16
AB11	VSS[6]	VSS[86]	AL17
AB14	VSS[7]	VSS[87]	AL19
AB39	VSS[8]	VSS[88]	AL2
AB4	VSS[9]	VSS[89]	AL21
AB43	VSS[10]	VSS[90]	AL23
AB5	VSS[11]	VSS[91]	AL26
AB7	VSS[12]	VSS[92]	AL27
AC19	VSS[13]	VSS[93]	AL31
AC2	VSS[14]	VSS[94]	AL33
AC21	VSS[15]	VSS[95]	AL34
AC24	VSS[16]	VSS[96]	AL48
AC33	VSS[17]	VSS[97]	AM11
AC34	VSS[18]	VSS[98]	AM14
AC48	VSS[19]	VSS[99]	AM36
AD10	VSS[20]	VSS[100]	AM39
AD11	VSS[21]	VSS[101]	AM43
AD12	VSS[22]	VSS[102]	AM45
AD13	VSS[23]	VSS[103]	AM46
AD19	VSS[24]	VSS[104]	AM7
AD24	VSS[25]	VSS[105]	AN2
AD26	VSS[26]	VSS[106]	AN29
AD27	VSS[27]	VSS[107]	AN3
AD33	VSS[28]	VSS[108]	AN31
AD34	VSS[29]	VSS[109]	AP12
AD36	VSS[30]	VSS[110]	AP19
AD37	VSS[31]	VSS[111]	AP28
AD38	VSS[32]	VSS[112]	AP30
AD39	VSS[33]	VSS[113]	AP32
AD4	VSS[34]	VSS[114]	AP38
AD40	VSS[35]	VSS[115]	AP4
AD42	VSS[36]	VSS[116]	AP42
AD43	VSS[37]	VSS[117]	AP46
AD45	VSS[38]	VSS[118]	AP8
AD46	VSS[39]	VSS[119]	AR2
AD8	VSS[40]	VSS[120]	AR48
AE2	VSS[41]	VSS[121]	AT11
AE3	VSS[42]	VSS[122]	AT13
AF10	VSS[43]	VSS[123]	AT18
AF12	VSS[44]	VSS[124]	AT22
AD14	VSS[45]	VSS[125]	AT26
AD16	VSS[46]	VSS[126]	AT28
AF16	VSS[47]	VSS[127]	AT30
AF19	VSS[48]	VSS[128]	AT32
AF24	VSS[49]	VSS[129]	AT34
AF26	VSS[50]	VSS[130]	AT39
AF27	VSS[51]	VSS[131]	AT42
AF29	VSS[52]	VSS[132]	AT46
AF31	VSS[53]	VSS[133]	AT7
AF38	VSS[54]	VSS[134]	AU24
AF4	VSS[55]	VSS[135]	AU30
AF42	VSS[56]	VSS[136]	AV16
AF46	VSS[57]	VSS[137]	AV20
AF5	VSS[58]	VSS[138]	AV24
AF7	VSS[59]	VSS[139]	AV30
AF8	VSS[60]	VSS[140]	AV38
AG19	VSS[61]	VSS[141]	AV4
AG2	VSS[62]	VSS[142]	AV43
AG31	VSS[63]	VSS[143]	AV8
AG48	VSS[64]	VSS[144]	AW14
AH11	VSS[65]	VSS[145]	AW18
AH3	VSS[66]	VSS[146]	AW2
AH36	VSS[67]	VSS[147]	AW22
AH39	VSS[68]	VSS[148]	AW26
AH40	VSS[69]	VSS[149]	AW28
AH42	VSS[70]	VSS[150]	AW32
AH46	VSS[71]	VSS[151]	AW34
AH7	VSS[72]	VSS[152]	AW36
AJ19	VSS[73]	VSS[153]	AW40
AJ21	VSS[74]	VSS[154]	AW48
AJ24	VSS[75]	VSS[155]	AV11
AJ33	VSS[76]	VSS[156]	AY12
AJ34	VSS[77]	VSS[157]	AY22
AK12	VSS[78]	VSS[158]	AY28
AK3	VSS[79]		

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AY4	VSS[159]	VSS[259]	H46
AY42	VSS[160]	VSS[260]	K18
AY46	VSS[161]	VSS[261]	K26
AY8	VSS[162]	VSS[262]	K39
B11	VSS[163]	VSS[263]	K46
B15	VSS[164]	VSS[264]	K7
B19	VSS[165]	VSS[265]	L18
B23	VSS[166]	VSS[266]	L2
B27	VSS[167]	VSS[267]	L20
B31	VSS[168]	VSS[268]	L26
B35	VSS[169]	VSS[269]	L28
B39	VSS[170]	VSS[270]	L36
B7	VSS[171]	VSS[271]	L48
F45	VSS[172]	VSS[272]	M12
BB12	VSS[173]	VSS[273]	P16
BB16	VSS[174]	VSS[274]	M18
BB20	VSS[175]	VSS[275]	M22
BB22	VSS[176]	VSS[276]	M24
BB24	VSS[177]	VSS[277]	M30
BB28	VSS[178]	VSS[278]	M32
BB30	VSS[179]	VSS[279]	M34
BB38	VSS[180]	VSS[280]	M38
BB4	VSS[181]	VSS[281]	M4
BB46	VSS[182]	VSS[282]	M42
BC14	VSS[183]	VSS[283]	M46
BC18	VSS[184]	VSS[284]	M8
BC2	VSS[185]	VSS[285]	N18
BC22	VSS[186]	VSS[286]	P30
BC26	VSS[187]	VSS[287]	N47
BC32	VSS[188]	VSS[288]	P11
BC34	VSS[189]	VSS[289]	P18
BC36	VSS[190]	VSS[290]	T33
BC40	VSS[191]	VSS[291]	P40
BC42	VSS[192]	VSS[292]	P43
BC48	VSS[193]	VSS[293]	P47
BD46	VSS[194]	VSS[294]	P7
BD5	VSS[195]	VSS[295]	R2
BE22	VSS[196]	VSS[296]	R48
BE26	VSS[197]	VSS[297]	T12
BE40	VSS[198]	VSS[298]	T31
BF10	VSS[199]	VSS[299]	T37
BF12	VSS[200]	VSS[300]	T4
BF16	VSS[201]	VSS[301]	W34
BF20	VSS[202]	VSS[302]	T46
BF22	VSS[203]	VSS[303]	T47
BF24	VSS[204]	VSS[304]	T8
BF26	VSS[205]	VSS[305]	V11
BF28	VSS[206]	VSS[306]	V17
BD3	VSS[207]	VSS[307]	V26
BF30	VSS[208]	VSS[308]	V27
BF38	VSS[209]	VSS[309]	V29
BF40	VSS[210]	VSS[310]	V31
BF8	VSS[211]	VSS[311]	V36
BG17	VSS[212]	VSS[312]	V39
BG21	VSS[213]	VSS[313]	V43
BG33	VSS[214]	VSS[314]	V7
BG44	VSS[215]	VSS[315]	W17
BG8	VSS[216]	VSS[316]	W19
BH11	VSS[217]	VSS[317]	W2
BH15	VSS[218]	VSS[318]	W27
BH17	VSS[219]	VSS[319]	W48
BH19	VSS[220]	VSS[320]	Y12
H10	VSS[221]	VSS[321]	Y38
BH27	VSS[222]	VSS[322]	Y4
BH31	VSS[223]	VSS[323]	Y42
BH33	VSS[224]	VSS[324]	Y46
BH35	VSS[225]	VSS[325]	Y8
BH39	VSS[226]	VSS[328]	BG29
BH43	VSS[227]	VSS[329]	N24
BH7	VSS[228]	VSS[330]	AJ3
D3	VSS[229]	VSS[331]	AD47
D12	VSS[230]	VSS[333]	B43
D16	VSS[231]	VSS[334]	BE10
D18	VSS[232]	VSS[335]	BG41
D22	VSS[233]	VSS[337]	G14
D24	VSS[234]	VSS[338]	H16
D26	VSS[235]	VSS[340]	T36
D30	VSS[236]	VSS[342]	BG22
D32	VSS[237]	VSS[343]	BG24
D34	VSS[238]	VSS[344]	C22
D38	VSS[239]	VSS[345]	AP13
D42	VSS[240]	VSS[346]	M14
D8	VSS[241]	VSS[347]	AP3
E18	VSS[242]	VSS[348]	AP1
E26	VSS[243]	VSS[349]	BE16
G18	VSS[244]	VSS[350]	BC16
G20	VSS[245]	VSS[351]	BG28
G26	VSS[246]	VSS[352]	BJ28
G28	VSS[247]		
G36	VSS[248]		
G48	VSS[249]		
H12	VSS[250]		
H18	VSS[251]		
H22	VSS[252]		
H24	VSS[253]		
H26	VSS[254]		
H30	VSS[255]		
H32	VSS[256]		
H34	VSS[257]		
F3	VSS[258]		

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THAMES (6019B0917601)

P3V3S_DGPU

R5016 10K_5%_2 GPIO0 OUT 56D5
R5010 10K_5%_2 GPIO1 OUT 56D5
R5011 10K_5%_2 GPIO2 OUT 56D5
R5028 RSC_0402_DY GPIO5 OUT 56D5
R5037 RSC_0402_DY GPIO9 OUT 56D5
R5014 10K_5%_2 GPIO11 OUT 56D5
R5030 10K_5%_2 VGA_CRT_HSYNC OUT 36B2
R5031 10K_5%_2 VGA_CRT_VSYNC OUT 36B2
R5027 10K_5%_2_DY GPIO22 OUT 56C5
R5056 10K_5%_2 PWRCNTL_0 OUT 13C6 56D5
R5017 10K_5%_2 PWRCNTL_1 OUT 13C6 56C5

GPIO11:MEMORY APERTURE SIZE 256M

MEM_ID3	MEM_ID2	MEM_ID1	MEM_ID0	
0	0	0	0	HYNIX
0	1	0	0	SAMSUNG

PIN BASE STRAPS		
GPIO_0	TRANSMITTER POWER SAVING ENABLE	0 : 50% TX OUTPUT SWING (DEFAULT) 1 : FULL TX OUTPUT SWING
GPIO_1	PCIE TRANSMITTER DE-EMPHASIS	0 : DE-EMPHASIS DISABLED (DEFAULT) 1 : DE-EMPHASIS ENABLED
GPIO_2	GEN1/GEN2 ENABLE	0 : GEN1 (DEFAULT) 1 : GEN2
GPIO_8 GPIO_21	MUST BE LOW DURING RESET	LEFT UNCONNECTED
GPIO_9	VGA DISABLE	0 : ENABLE (DEFAULT) 1 : DISABLE
GPIO_[11:13]	MEMORY APERTURE SIZE	GPIO_13 GPIO_12 GPIO_11 → MEMORY APERTURE SIZE: 0 0 0 → 128M 0 0 1 → 256M 0 1 0 → 64M 0 1 1 → 32M
GPIO_22	ENABLE EXTERNAL BIOS ROM DEVICE	0 : DISABLE (DEFAULT) 1 : ENABLE
HSYNC[1] VSYNC[0]	AUDIO[1:0]	00 : NO AUDIO FUNCTION 01 : AUDIO FOR DP ONLY 10 : AUDIO FOR DP AND HDMI IF DONGLE IS DETECTED 11 : AUDIO FOR BOTH DP AND HDMI

P3V3S_DGPU
Q5001 SSM3K7002BFU
2TO8 21D2 5A7 BI EC_SMB2_CLK 3 R5004 10K_5%_2 GPU_SIC BI 56D5

P3V3S_DGPU
Q5002 SSM3K7002BFU
2TO3 21D2 5A7 BI EC_SMB2_DATA 3 R5005 10K_5%_2 GPU_SID BI 56D5

P1V8S_DGPU
R5006 10K_5%_2_DY MEM_ID0
R5007 10K_5%_2_DY MEM_ID1
R5008 10K_5%_2_DY MEM_ID2
R5009 10K_5%_2_DY MEM_ID3

U5001

MUTI GFX
AR8 DVPCNTL_MVP_0
AU8 DVPCNTL_MVP_1
AP8 DVPCNTL_0
AW8 DVPCNTL_1
AR3 DVPCNTL_2
AR1 DVPCLK
AU1 DVPDATA_0
AU3 DVPDATA_1
AW3 DVPDATA_2
AP6 DVPDATA_3
AW5 DVPDATA_4
AU5 DVPDATA_5
AR6 DVPDATA_6
AW6 DVPDATA_7
AU6 DVPDATA_8
AT7 DVPDATA_9
AV7 DVPDATA_10
AN7 DVPDATA_11
AV9 DVPDATA_12
AT9 DVPDATA_13
AR10 DVPDATA_14
AW10 DVPDATA_15
AU10 DVPDATA_16
AP10 DVPDATA_17
AV11 DVPDATA_18
AT11 DVPDATA_19
AR12 DVPDATA_20
AW12 DVPDATA_21
AU12 DVPDATA_22
AP12 DVPDATA_23
AJ21 SWAPLOCKA
AK21 SWAPLOCKB

I2C
34C5 BI VGA_LVDS_DDCCLK AK26 SCL
34C5 BI VGA_LVDS_DDCDATA AJ26 SDA

GENERAL PURPOSE I/O
56F7 IN GPIO0 AH20 GPIO_0
56F7 IN GPIO1 AH18 GPIO_1
56F7 IN GPIO2 AN16 GPIO_2
56C7 BI GPU_SID AH23 GPIO_3_SMBDATA
56D7 BI GPU_SIC AJ23 GPIO_4_SMBCLK
56F7 IN GPIO5 AH17 GPIO_5_AC_BATT
AJ17 GPIO_6
21E7 OUT VGA_LCM_BKLTEN AK17 GPIO_7_BLON
AJ13 GPIO_8_ROMSO
56F7 IN GPIO9 AH15 GPIO_9_ROMSI
AJ16 GPIO_10_ROMSCK
56F7 IN GPIO11 AK16 GPIO_11
AL16 GPIO_12
AM16 GPIO_13
AM14 GPIO_14_HPD2
AM13 GPIO_15_PWRCNTL_0
OUT PWRCNTL_0 AK14 GPIO_16
AG30 GPIO_17_THERMAL_INT
AN14 GPIO_18_HPD3
AM17 GPIO_19_CTF
13C6 OUT PWRCNTL_1 AL13 GPIO_20_PWRCNTL_1
56F7 IN GPIO22 AJ14 GPIO_21_BB_EN
AK13 GPIO_22_ROMCSB
AN13 GPIO_23_CLKREQB
AM23 JTAG_TRSTB
AN23 JTAG_TDI
AK23 JTAG_TCK
AL24 JTAG_TMS
AM24 JTAG_TDO
AJ19 GENERICA
AK19 GENERICB
AJ20 GENERICC
AK20 GENERICD
AJ24 GENERICE_HPD4
AH26 GENERICF_HPD5
AH24 GENERICG_HPD6

P1V8S_DGPU
36B5 IN VGA_HPDET AK24 HPD1
R5004 499_1%_2
P0V6S_VREFG
R5003 249_1%_2 C5010 0.1UF_16V_2
AH13 VREFG

PLL/CLOCK
AM32 DPLL_PVDD
AN32 DPLL_PVSS
AN31 DPLL_VDDC
AV33 XTALIN
AU34 XTALOUT
AW34 XO_IN
AW35 XO_IN2

THERMAL
AF29 DPLUS
AG29 DMINUS
TP5000 TP30 AK32 TS_FDO
AL31 TS_A/NC

AJ32 TSVDD
AJ33 TSVSS

AMD_216_0833002_FCBGA_962P

DPA
TXCAP_DPA3P AU24 VGA_HDMI_TXC_DP OUT 36A5
TXCAM_DPA3N AV23 VGA_HDMI_TXC_DN OUT 36A5
TX0P_DPA2P AT25 VGA_HDMI_TX0_DP OUT 36A5
TX0M_DPA2N AR24 VGA_HDMI_TX0_DN OUT 36A5
TX1P_DPA1P AU26 VGA_HDMI_TX1_DP OUT 36A5
TX1M_DPA1N AV25 VGA_HDMI_TX1_DN OUT 36A5
TX2P_DPA0P AT27 VGA_HDMI_TX2_DP OUT 36A5
TX2M_DPA0N AR26 VGA_HDMI_TX2_DN OUT 36A5

DPB
TXCBP_DPB3P AR30
TXCBM_DPB3N AT29
TX3P_DPB2P AV31
TX3M_DPB2N AU30
TX4P_DPB1P AR32
TX4M_DPB1N AT31
TX5P_DPB0P AT33
TX5M_DPB0N AU32

DPC
TXCCP_DPC3P AU14
TXCCM_DPC3N AV13
TX0P_DPC2P AT15
TX0M_DPC2N AR14
TX1P_DPC1P AU16
TX1M_DPC1N AV15
TX2P_DPC0P AT17
TX2M_DPC0N AR16

DPD
TXCDP_DPD3P AU20
TXCDM_DPD3N AT19
TX3P_DPD2P AT21
TX3M_DPD2N AR20
TX4P_DPD1P AU22
TX4M_DPD1N AV21
TX5P_DPD0P AT23
TX5M_DPD0N AR22

DAC1
R AD39 VGA_CRTR OUT 35D8 56E2
RB AD37
G AE36 VGA_CRTG OUT 35D8 56E2
GB AD35
B AF37 VGA_CRTB OUT 35D8 56E2
BB AE38
HSYNC AC36 VGA_CRT_HSYNC OUT 36B2
VSYNC AC38 VGA_CRT_VSYNC OUT 36B2
RSET AB34 R5000 499_1%_2
AVDD AE34
AVSSQ
VDD1DI AC33
VSS1DI AC34

DAC2
R2/NC AC30
R2B/NC AC31
G2/NC AD30
G2B/NC AD31
B2/NC AF30
B2B/NC AF31
C/NC AC32
Y/NC AD32
COMP/NC AF32
H2SYNC/GENLK_CLK AD29
V2SYNC/GENLK_VSYNC AC29
VDD2DI/NC AG31
VSS2DI/NC AG32
A2VDD/NC AG33
A2VDDQ/NC AD33
A2VSSQ/TSVSSQ AF33
R2SET/NC AA29

DDC/AUX
DDC1CLK AM26 VGA_HDMI_DDCCLK BI 36D8
DDC1DATA AN26 VGA_HDMI_DDCDATA BI 36D8
AUX1P AM27
AUX1N AL27
DDC2CLK AM19
DDC2DATA AL19
AUX2P AN20
AUX2N AM20
DDCCLK_AUX3P AL30
DDCDATA_AUX3N AM30
DDCCLK_AUX4P AL29
DDCDATA_AUX4N AM29
DDCCLK_AUX5P AN21
DDCDATA_AUX5N AM21
DDC6CLK AJ30 VGA_CRT_DDCCLK BI 35A2
DDC6DATA AJ31 VGA_CRT_DDCDATA BI 35B2
DDCCLK_AUX7P AK30
DDCDATA_AUX7N AK29

PLACE CLOSE TO ASIC
56D3 35D8 IN VGA_CRTR R5072 150_1%_2
56D3 35D8 IN VGA_CRTG R5073 150_1%_2
56D3 35D8 IN VGA_CRTB R5074 150_1%_2

P1V8S_DGPU
I=70MA TRACE WIDTH>=15MIL
L5000 FBM_11_160808_121T
C5001 0.1UF_16V_2
C5000 1UF_6.3V_2
C5005 10UF_6.3V_3

P1V8S_DGPU
I=100MA TRACE WIDTH>=15MIL
L5001 FBM_11_160808_121T
C5003 0.1UF_16V_2
C5002 1UF_6.3V_2
C5004 10UF_6.3V_3

P1V8S_DGPU
L5004 FBM_11_160808_121T
I=75MA TRACE WIDTH>=15MIL
C5013 10UF_6.3V_3
C5011 1UF_6.3V_2
C5012 0.1UF_16V_2

PVPCIE
L5005 FBM_11_160808_121T
I=125MA TRACE WIDTH>=15MIL
C5016 10UF_6.3V_3
C5014 1UF_6.3V_2
C5015 0.1UF_16V_2

R4 1M_5%_2
X5000 27MHZ
C5211 12PF_50V_2
C5212 12PF_50V_2

P1V8S_DGPU
L5006 FBM_11_160808_121T
I=20MA TRACE WIDTH>=15MIL
C5019 10UF_6.3V_3
C5017 1UF_6.3V_2
C5018 0.1UF_16V_2

TITLE	MODEL,PROJECT,FUNCTION Block Diagram
SIZE	C
CODE	CS
DOC.NUMBER	1310xxxxx-0-0
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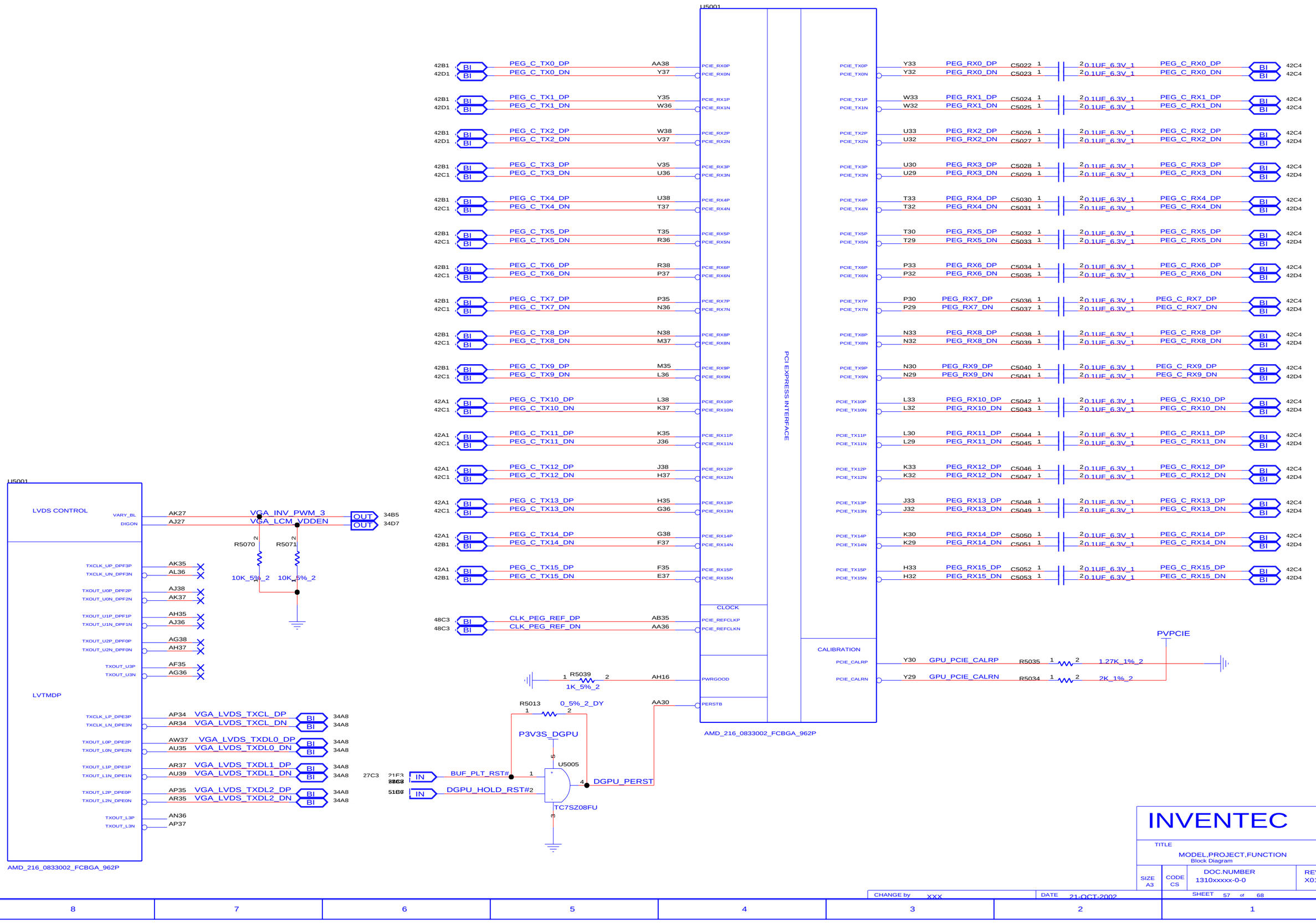
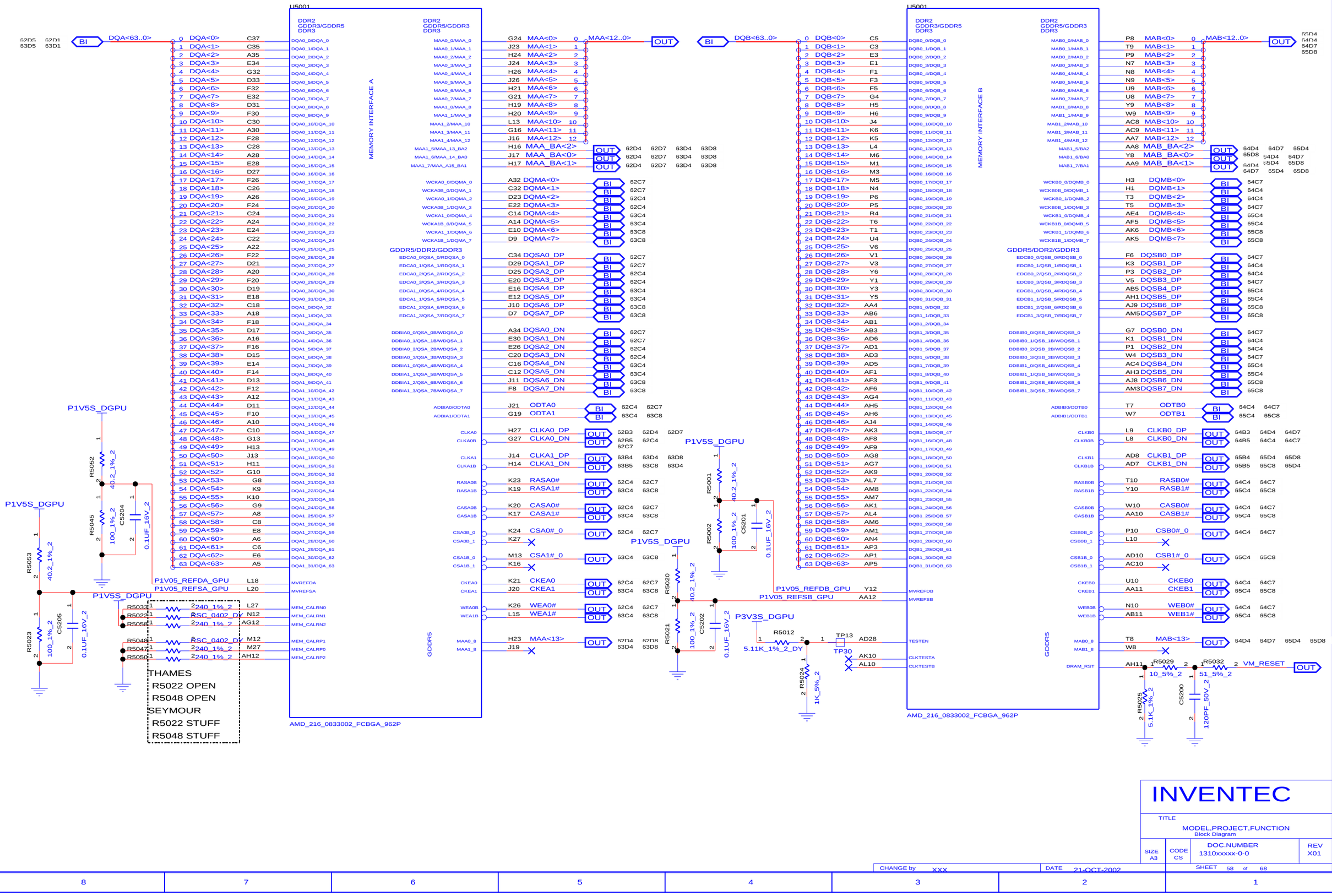
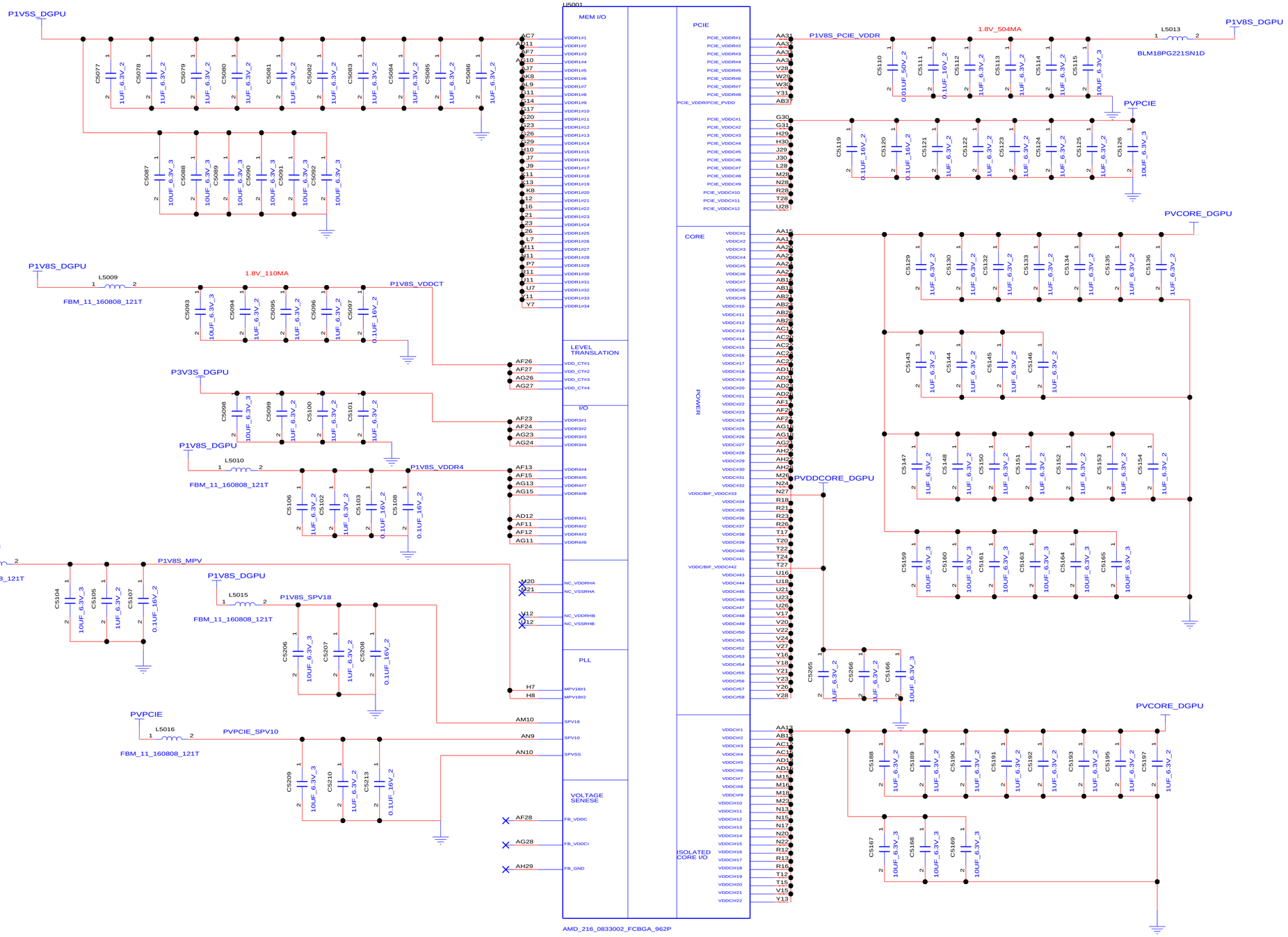
INVENTEC


U5001
PCI EXPRESS INTERFACE
PEG_C_TX0_DP AA38 PCIE_RX0P
PEG_C_TX0_DN Y37 PCIE_RX0N
PEG_C_TX1_DP Y35 PCIE_RX1P
PEG_C_TX1_DN W36 PCIE_RX1N
PEG_C_TX2_DP W38 PCIE_RX2P
PEG_C_TX2_DN V37 PCIE_RX2N
PEG_C_TX3_DP V35 PCIE_RX3P
PEG_C_TX3_DN U36 PCIE_RX3N
PEG_C_TX4_DP U38 PCIE_RX4P
PEG_C_TX4_DN T37 PCIE_RX4N
PEG_C_TX5_DP T35 PCIE_RX5P
PEG_C_TX5_DN R36 PCIE_RX5N
PEG_C_TX6_DP R38 PCIE_RX6P
PEG_C_TX6_DN P37 PCIE_RX6N
PEG_C_TX7_DP P35 PCIE_RX7P
PEG_C_TX7_DN N36 PCIE_RX7N
PEG_C_TX8_DP N38 PCIE_RX8P
PEG_C_TX8_DN M37 PCIE_RX8N
PEG_C_TX9_DP M35 PCIE_RX9P
PEG_C_TX9_DN L36 PCIE_RX9N
PEG_C_TX10_DP L38 PCIE_RX10P
PEG_C_TX10_DN K37 PCIE_RX10N
PEG_C_TX11_DP K35 PCIE_RX11P
PEG_C_TX11_DN J36 PCIE_RX11N
PEG_C_TX12_DP J38 PCIE_RX12P
PEG_C_TX12_DN H37 PCIE_RX12N
PEG_C_TX13_DP H35 PCIE_RX13P
PEG_C_TX13_DN G36 PCIE_RX13N
PEG_C_TX14_DP G38 PCIE_RX14P
PEG_C_TX14_DN F37 PCIE_RX14N
PEG_C_TX15_DP F35 PCIE_RX15P
PEG_C_TX15_DN E37 PCIE_RX15N
CLOCK
CLK_PEG_REF_DP AB35 PCIE_REFCLKP
CLK_PEG_REF_DN AA36 PCIE_REFCLKN
R5039 1K_5%_2 AH16 PWRGOOD
R5013 0_5%_2_DY AA30 PERSTB
P3V3S_DGPU
U5005
BUF_PLT_RST#
DGPU_HOLD_RST#2
DGPU_PERST
TC7SZ08FU
AMD_216_0833002_FCBGA_962P
PCIE_TX0P Y33 PEG_RX0_DP C5022 0.1UF_6.3V_1 PEG_C_RX0_DP
PCIE_TX0N Y32 PEG_RX0_DN C5023 0.1UF_6.3V_1 PEG_C_RX0_DN
PCIE_TX1P W33 PEG_RX1_DP C5024 0.1UF_6.3V_1 PEG_C_RX1_DP
PCIE_TX1N W32 PEG_RX1_DN C5025 0.1UF_6.3V_1 PEG_C_RX1_DN
PCIE_TX2P U33 PEG_RX2_DP C5026 0.1UF_6.3V_1 PEG_C_RX2_DP
PCIE_TX2N U32 PEG_RX2_DN C5027 0.1UF_6.3V_1 PEG_C_RX2_DN
PCIE_TX3P U30 PEG_RX3_DP C5028 0.1UF_6.3V_1 PEG_C_RX3_DP
PCIE_TX3N U29 PEG_RX3_DN C5029 0.1UF_6.3V_1 PEG_C_RX3_DN
PCIE_TX4P T33 PEG_RX4_DP C5030 0.1UF_6.3V_1 PEG_C_RX4_DP
PCIE_TX4N T32 PEG_RX4_DN C5031 0.1UF_6.3V_1 PEG_C_RX4_DN
PCIE_TX5P T30 PEG_RX5_DP C5032 0.1UF_6.3V_1 PEG_C_RX5_DP
PCIE_TX5N T29 PEG_RX5_DN C5033 0.1UF_6.3V_1 PEG_C_RX5_DN
PCIE_TX6P P33 PEG_RX6_DP C5034 0.1UF_6.3V_1 PEG_C_RX6_DP
PCIE_TX6N P32 PEG_RX6_DN C5035 0.1UF_6.3V_1 PEG_C_RX6_DN
PCIE_TX7P P30 PEG_RX7_DP C5036 0.1UF_6.3V_1 PEG_C_RX7_DP
PCIE_TX7N P29 PEG_RX7_DN C5037 0.1UF_6.3V_1 PEG_C_RX7_DN
PCIE_TX8P N33 PEG_RX8_DP C5038 0.1UF_6.3V_1 PEG_C_RX8_DP
PCIE_TX8N N32 PEG_RX8_DN C5039 0.1UF_6.3V_1 PEG_C_RX8_DN
PCIE_TX9P N30 PEG_RX9_DP C5040 0.1UF_6.3V_1 PEG_C_RX9_DP
PCIE_TX9N N29 PEG_RX9_DN C5041 0.1UF_6.3V_1 PEG_C_RX9_DN
PCIE_TX10P L33 PEG_RX10_DP C5042 0.1UF_6.3V_1 PEG_C_RX10_DP
PCIE_TX10N L32 PEG_RX10_DN C5043 0.1UF_6.3V_1 PEG_C_RX10_DN
PCIE_TX11P L30 PEG_RX11_DP C5044 0.1UF_6.3V_1 PEG_C_RX11_DP
PCIE_TX11N L29 PEG_RX11_DN C5045 0.1UF_6.3V_1 PEG_C_RX11_DN
PCIE_TX12P K33 PEG_RX12_DP C5046 0.1UF_6.3V_1 PEG_C_RX12_DP
PCIE_TX12N K32 PEG_RX12_DN C5047 0.1UF_6.3V_1 PEG_C_RX12_DN
PCIE_TX13P J33 PEG_RX13_DP C5048 0.1UF_6.3V_1 PEG_C_RX13_DP
PCIE_TX13N J32 PEG_RX13_DN C5049 0.1UF_6.3V_1 PEG_C_RX13_DN
PCIE_TX14P K30 PEG_RX14_DP C5050 0.1UF_6.3V_1 PEG_C_RX14_DP
PCIE_TX14N K29 PEG_RX14_DN C5051 0.1UF_6.3V_1 PEG_C_RX14_DN
PCIE_TX15P H33 PEG_RX15_DP C5052 0.1UF_6.3V_1 PEG_C_RX15_DP
PCIE_TX15N H32 PEG_RX15_DN C5053 0.1UF_6.3V_1 PEG_C_RX15_DN
CALIBRATION
PCIE_CALRP Y30 GPU_PCIE_CALRP R5035 1.27K_1%_2 PVPCIE
PCIE_CALRN Y29 GPU_PCIE_CALRN R5034 2K_1%_2
U5001
LVDS CONTROL
VARY_BL AK27 VGA_INV_PWM_3
DIGON AJ27 VGA_LCM_VDDEN
R5070 10K_5%_2
R5071 10K_5%_2
TXCLK_UP_DPF3P AK35
TXCLK_UN_DPF3N AL36
TXOUT_U0P_DPF2P AJ38
TXOUT_U0N_DPF2N AK37
TXOUT_U1P_DPF1P AH35
TXOUT_U1N_DPF1N AJ36
TXOUT_U2P_DPF0P AG38
TXOUT_U2N_DPF0N AH37
TXOUT_U3P AF35
TXOUT_U3N AG36
LVTMDP
TXCLK_LP_DPE3P AP34 VGA_LVDS_TXCL_DP
TXCLK_LN_DPE3N AR34 VGA_LVDS_TXCL_DN
TXOUT_L0P_DPE2P AW37 VGA_LVDS_TXDL0_DP
TXOUT_L0N_DPE2N AU35 VGA_LVDS_TXDL0_DN
TXOUT_L1P_DPE1P AR37 VGA_LVDS_TXDL1_DP
TXOUT_L1N_DPE1N AU39 VGA_LVDS_TXDL1_DN
TXOUT_L2P_DPE0P AP35 VGA_LVDS_TXDL2_DP
TXOUT_L2N_DPE0N AR35 VGA_LVDS_TXDL2_DN
TXOUT_L3P AN36
TXOUT_L3N AP37
AMD_216_0833002_FCBGA_962P
INVENTEC
TITLE
MODEL,PROJECT,FUNCTION
Block Diagram
SIZE A3
CODE CS
DOC.NUMBER 1310xxxxx-0-0
REV X01
CHANGE by XXX
DATE 21-OCT-2002
SHEET 57 of 68



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX	DATE 21-OCT-2002	SHEET 58 of 68	



INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
C	C5	1310xxxxx-0-0	X01

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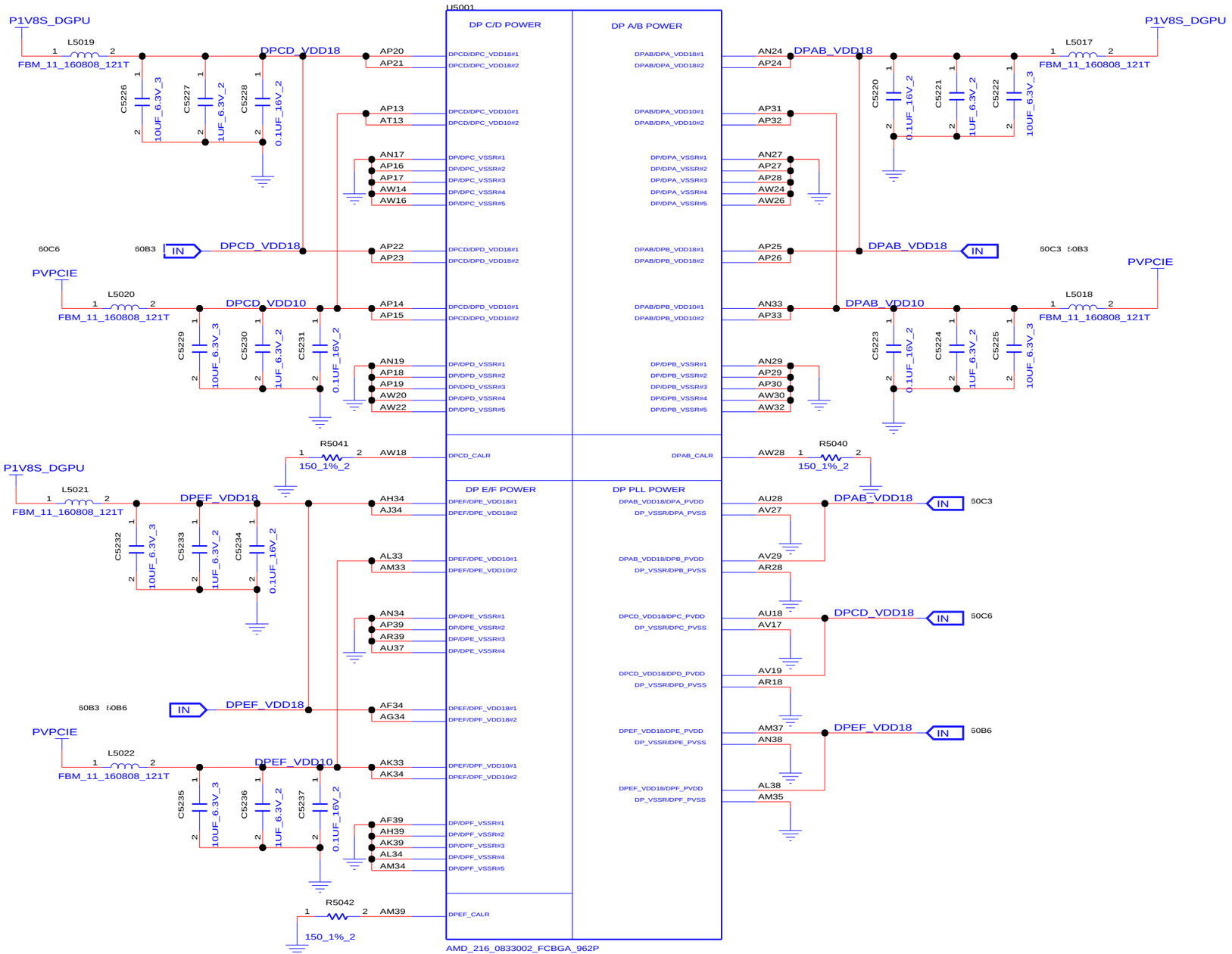

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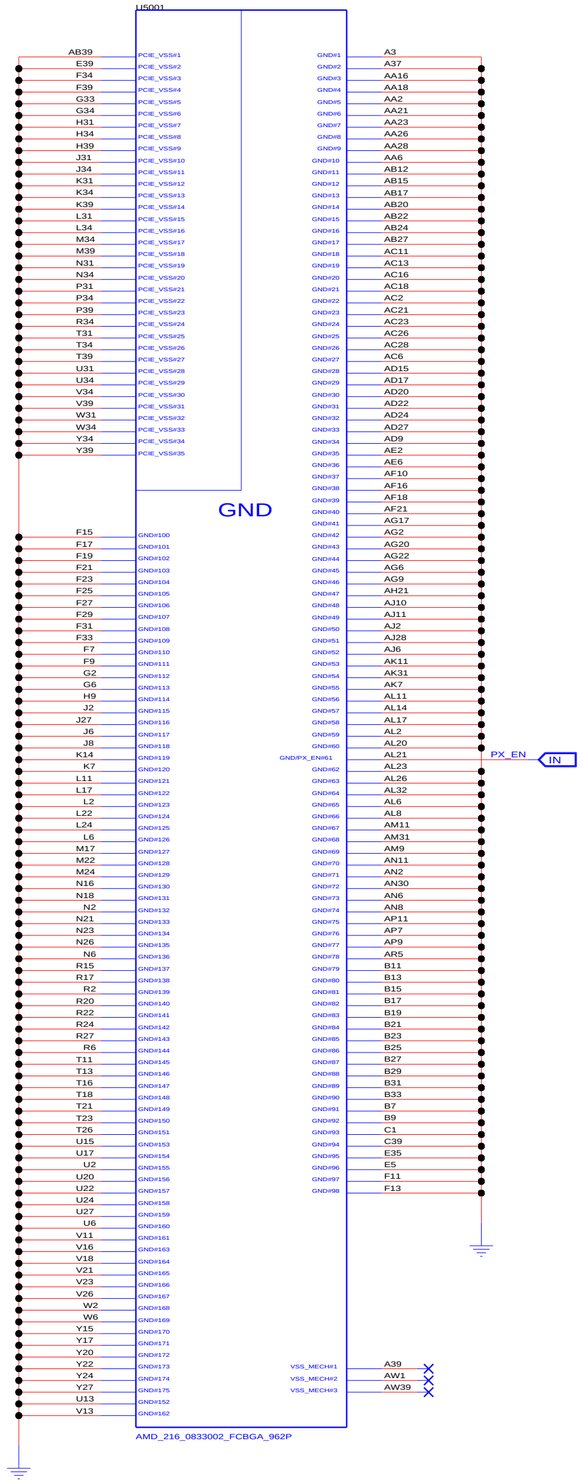
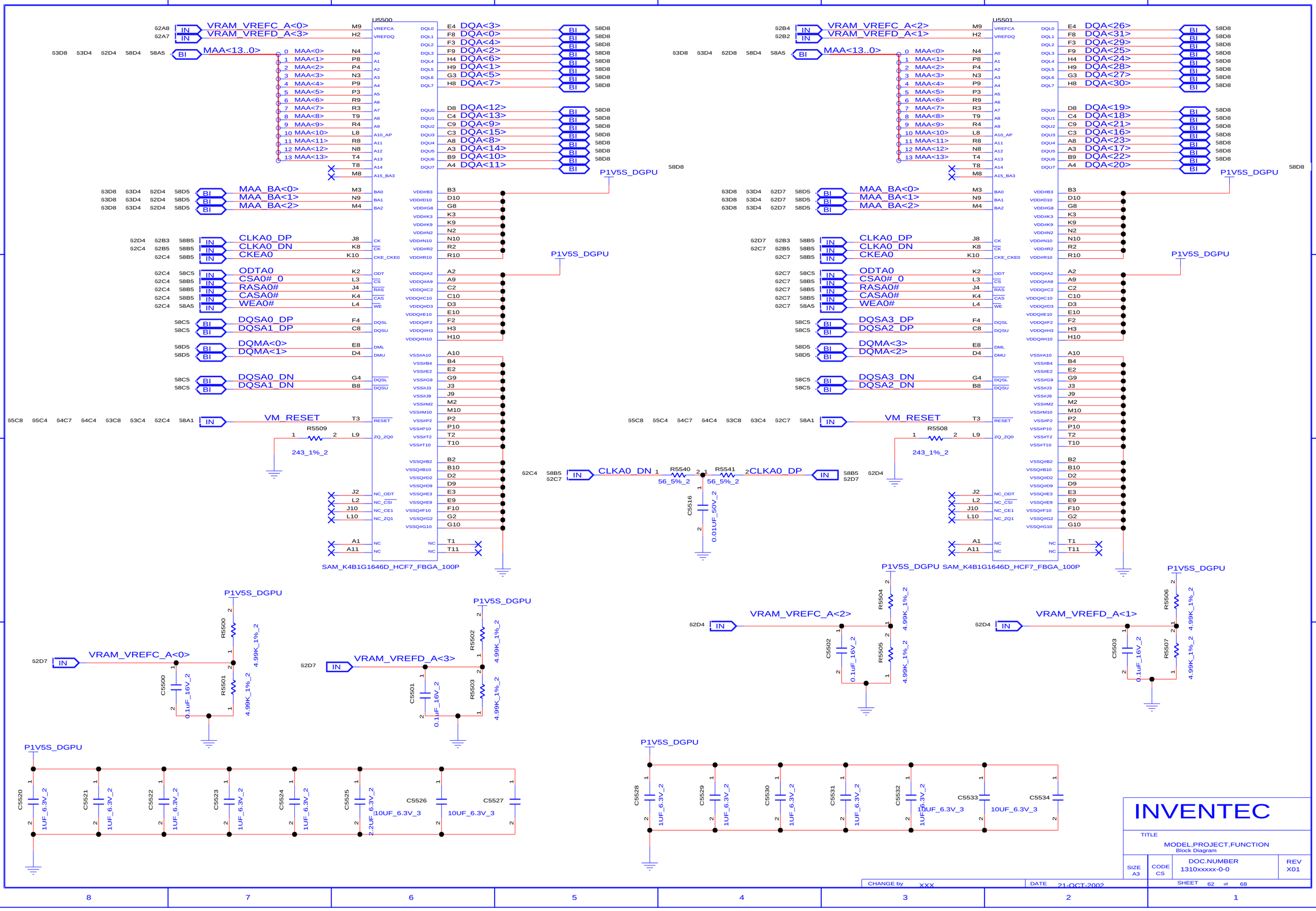
SIZE: A3	CODE: CS	DOC.NUMBER: 1310xxxxx-0-0	REV: X01	
CHANGE by: XXX	DATE: 21-OCT-2002	SHEET: 60 of 68		



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram			
SIZE: C	CODE: CS	DOC.NUMBER: 1310xxxxx-0-0	REV: X01
CHANGE by: XXX	DATE: 21-OCT-2002	SHEET 61 of 68	



TITLE	MODEL,PROJECT,FUNCTION Block Diagram
SIZE A3	CODE CS
DOC.NUMBER	1310xxxxx-0-0
REV	X01
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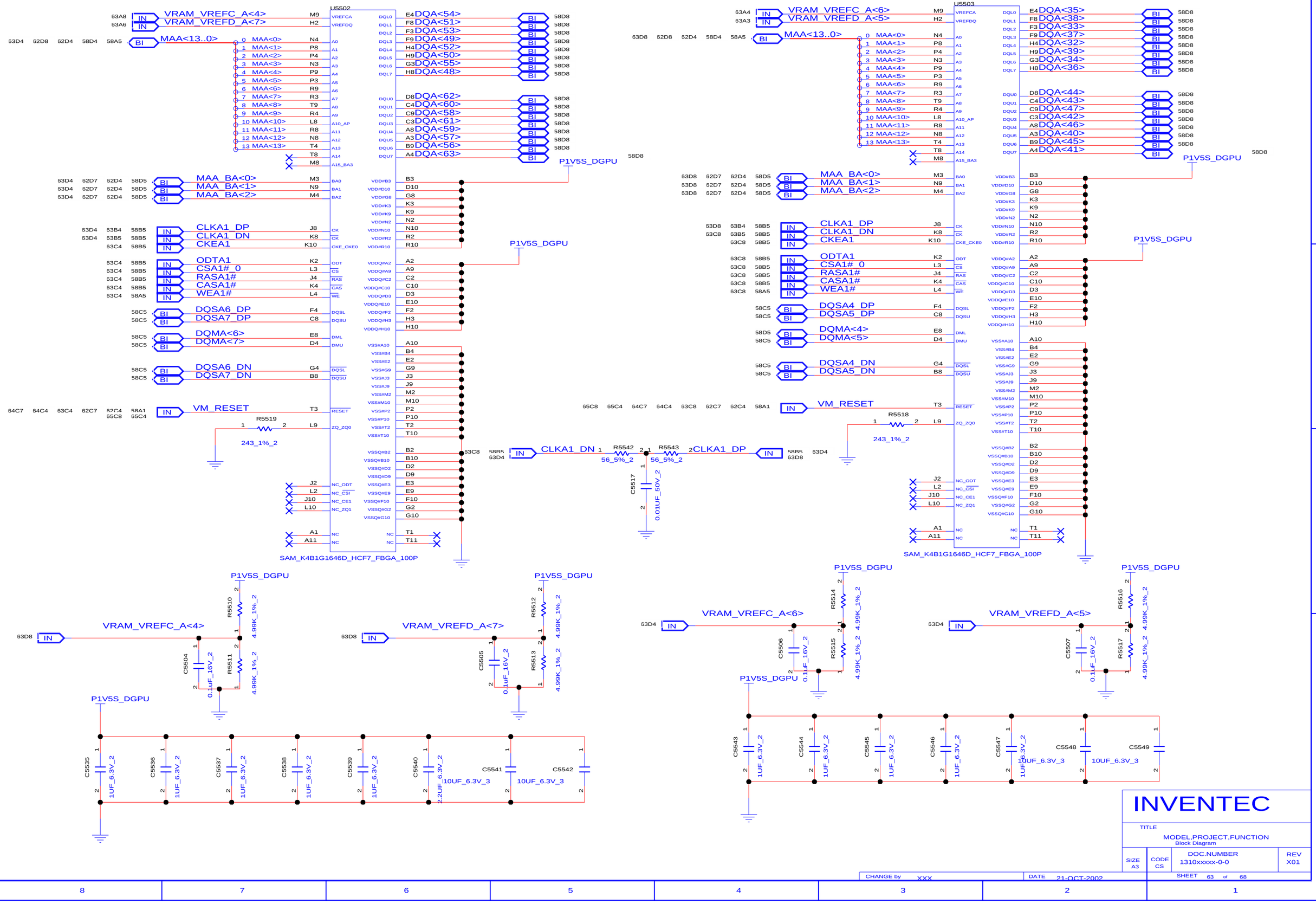
U5502
U5503
SAM_K4B1G1646D_HCF7_FBGA_100P
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VRAM_VREFD_A<7>
VRAM_VREFC_A<6>
VRAM_VREFD_A<5>
MAA<13..0>
MAA_BA<0>
MAA_BA<1>
MAA_BA<2>
CLKA1_DP
CLKA1_DN
CKEA1
ODTA1
CSA1#_0
RASA1#
CASA1#
WEA1#
DQSA6_DP
DQSA7_DP
DQSA4_DP
DQSA5_DP
DQMA<6>
DQMA<7>
DQMA<4>
DQMA<5>
DQSA6_DN
DQSA7_DN
DQSA4_DN
DQSA5_DN
VM_RESET
P1V5S_DGPU
243_1%_2
56_5%_2
0.01UF_50V_2
0.1UF_16V_2
4.99K_1%_2
1UF_6.3V_2
2.2UF_6.3V_3
10UF_6.3V_3
INVENTEC
MODEL,PROJECT,FUNCTION
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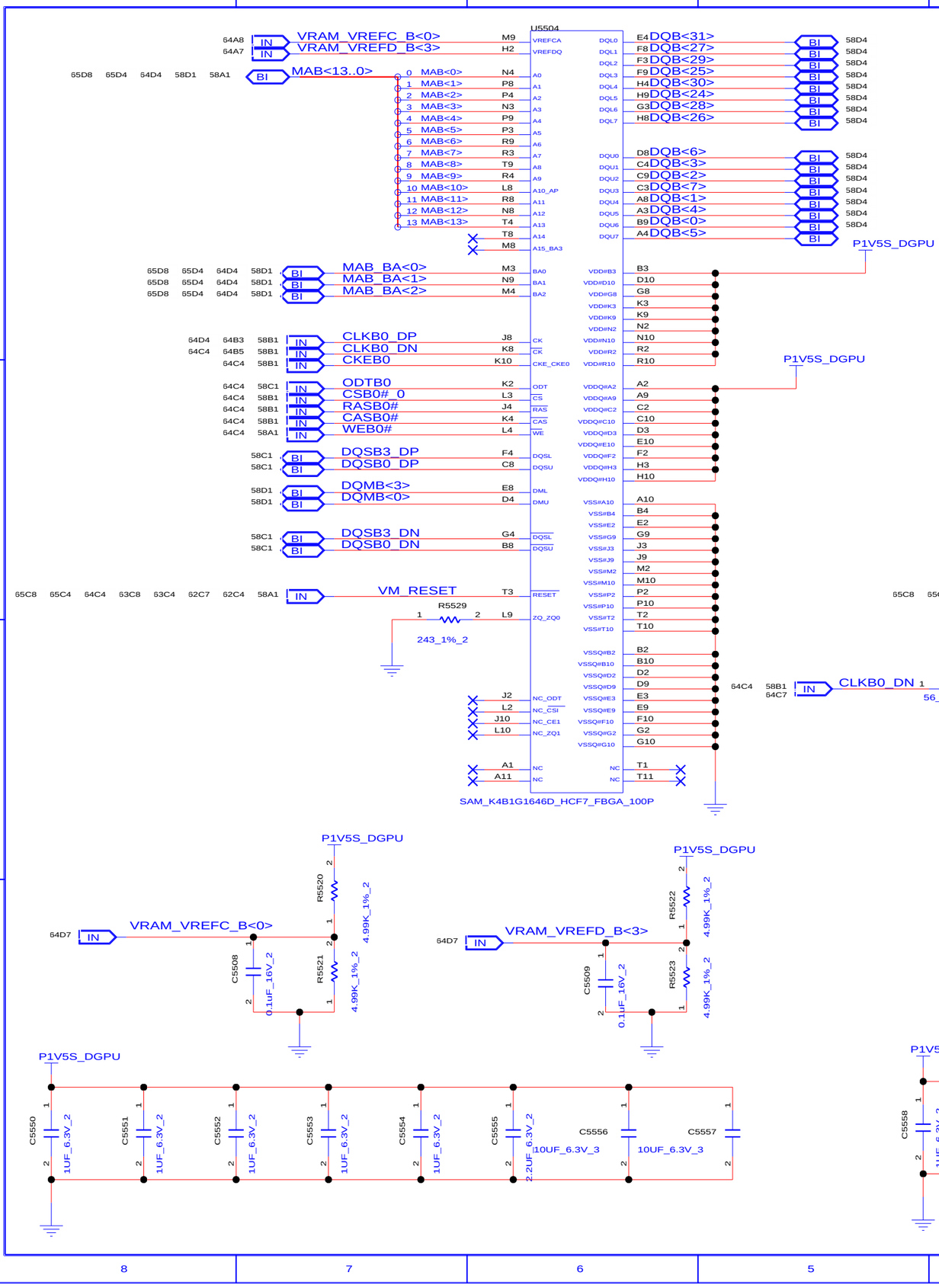

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TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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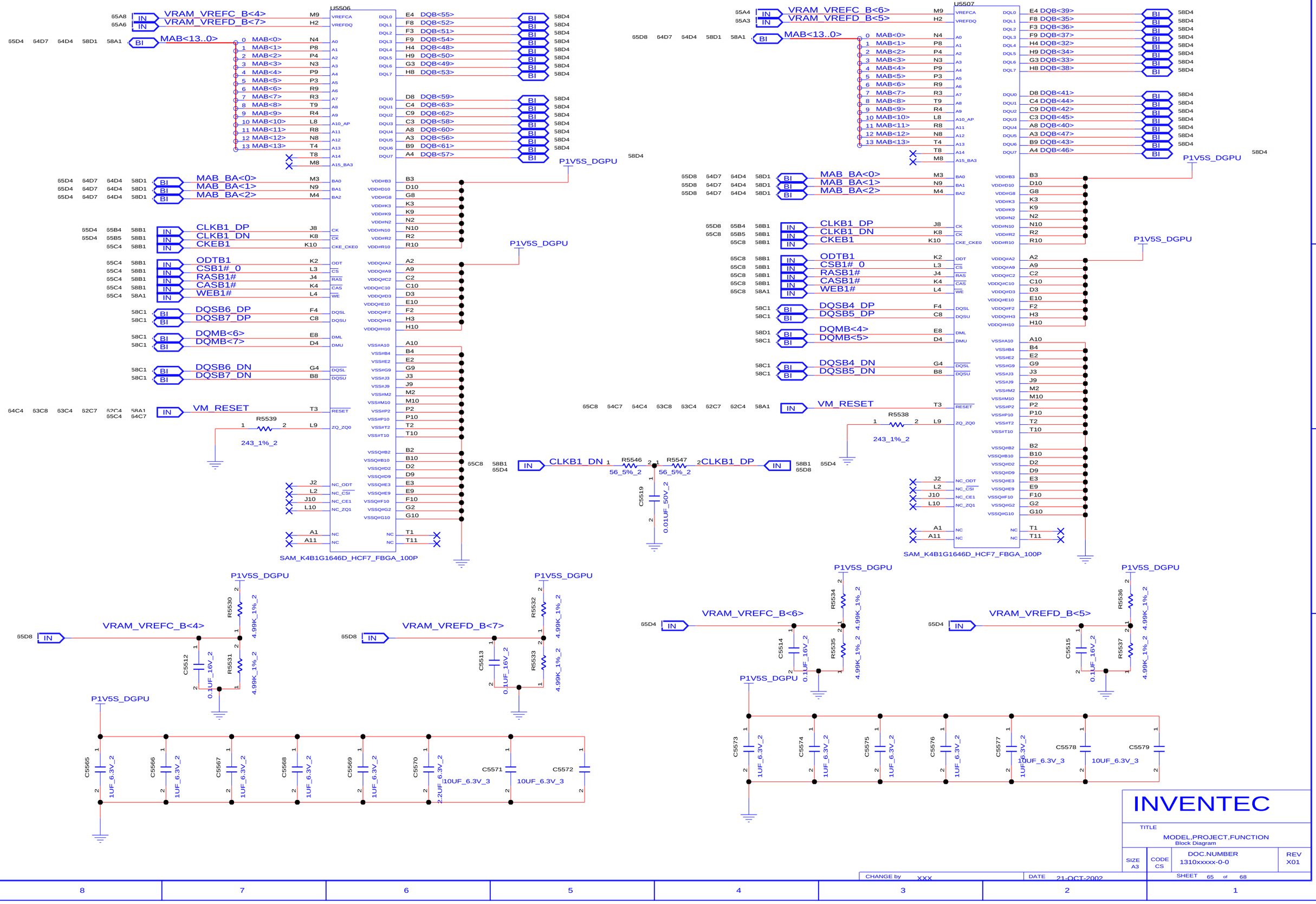
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U5507
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VRAM_VREFD_B<7>
VRAM_VREFC_B<6>
VRAM_VREFD_B<5>
MAB<13..0>
MAB_BA<0>
MAB_BA<1>
MAB_BA<2>
CLKB1_DP
CLKB1_DN
CKEB1
ODTB1
CSB1#_0
RASB1#
CASB1#
WEB1#
DQSB6_DP
DQSB7_DP
DQSB4_DP
DQSB5_DP
DQMB<6>
DQMB<7>
DQMB<4>
DQMB<5>
DQSB6_DN
DQSB7_DN
DQSB4_DN
DQSB5_DN
VM_RESET
P1V5S_DGPU
R5539
R5538
243_1%_2
R5546
R5547
56_5%_2
C5519
0.01UF_50V_2
R5530
R5531
R5532
R5533
R5534
R5535
R5536
R5537
4.99K_1%_2
C5512
C5513
C5514
C5515
0.1UF_16V_2
C5565
C5566
C5567
C5568
C5569
C5570
C5571
C5572
C5573
C5574
C5575
C5576
C5577
C5578
C5579
1UF_6.3V_2
2.2UF_6.3V_2
10UF_6.3V_3
INVENTEC
TITLE
MODEL,PROJECT,FUNCTION
Block Diagram
SIZE A3
CODE CS
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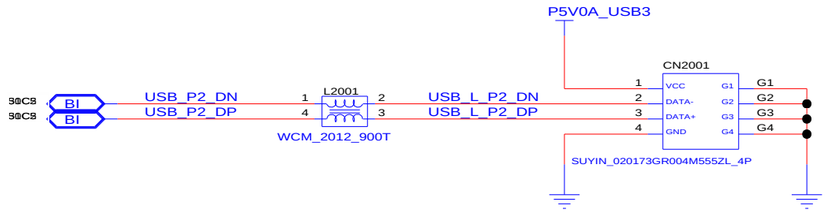

INVENTEC		
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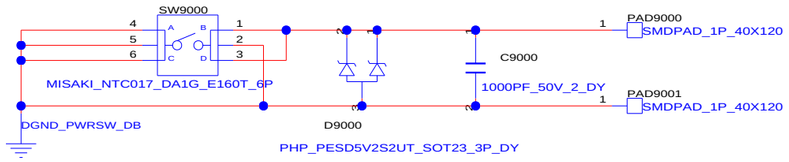
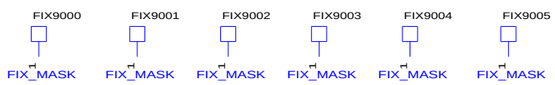
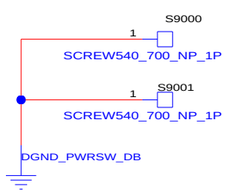
REFERENCE 9000~9999(SMALL BOARD)

POWER BUTTON







INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
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8 7 6 5 4 3 2 1

D C B A

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A3	CS	1310xxxxx-0-0	X01

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8 7 6 5 4 3 2 1