

BREMEN-D

CPU : AMD Caspin
Chip Set : AMD RX881 + SB710
Remarks : Tigris Platform
Park-XT M2

Model Name : Bremen-D
PBA Name : MAIN
PCB Code : GCE :
 NAN :
 HAN :
Dev. Step : PV
Revision : 1.4
T.R. Date : 2009.11.10

Design	CHECK	APPROVAL

■ Owner : SEC Mobile R & D Signature : X

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DRAW	XIE, BIN	DATE	10/10/2008	TITLE	Bremen-D	SAMSUNG
CHECK	GUO, LEI	DEV. STEP	PV	MAIN		ELECTRONICS
APPROVAL	LEE, BC	REV	1.0	COVER		PART NO. BA41-xxxxxA
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POWER DIAGRAM

Rev 0.3

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AC Adapter

Battery DC

VDC

P3.3V_MICOM

MICOM LED SB710

P5.0V_STB

USB N Charger

P12.0V_ALW

KBC3_SUSPWR
(CHP3_S4_STATE*)

P5V_AUX

USB connector

P1.8V_AUX

AMD S1G3
SODIMM (DDR II)

P0.9V_AUX

DDR II-Termination

P1.2V_AUX

SB710

P3.3V_AUX

SB710
WLAN
LAN
THERMAL
LVDS
LED

P1.2V_LAN

LAN

KBC3_PWRON
(CHP3_SLPS3*)

P1.8V

RX881
Park-XT M2 / Madison-LP
gDDR-3 for EGfx
AU6336

P5.0V

THERMAL CRT HDMI
SB710 MICOM AUDIO
ODD HDD CAMERA
TOUCH PAD

EGFX_CORE

Park-XT M2 / Madison-LP

P1.5V

CK505
WLAN
EXPRESS CARD

P1.0V

Park-XT M2 / Madison-LP

P2.5V

S1G3

P3.3V

CK505 THERMAL RX881
DDR2 CRT PARK / MADISON
LVDS HDMI SB710
SPI WLAN LEDS
LAN AUDIO AU6336
HDD BT

KBC3_VRON

CPU_CORE

S1G3

P1.2V

S1G3
RX881
SB710

P1.1V

RX881
Park-XT M2
Madison-LP

Power On/Off Table by S-state

Rail	S0	S3	S4	S5
State				
+V*A(LWS) +V*LAN	ON	ON	ON	ON
+1.8V_AUX +0.9V_AUX	ON	ON	—	—
+V*AUX	ON	ON	—	—
+V	ON	—	—	—
+V* (CORE)	ON	—	—	—

S5-S4

S3

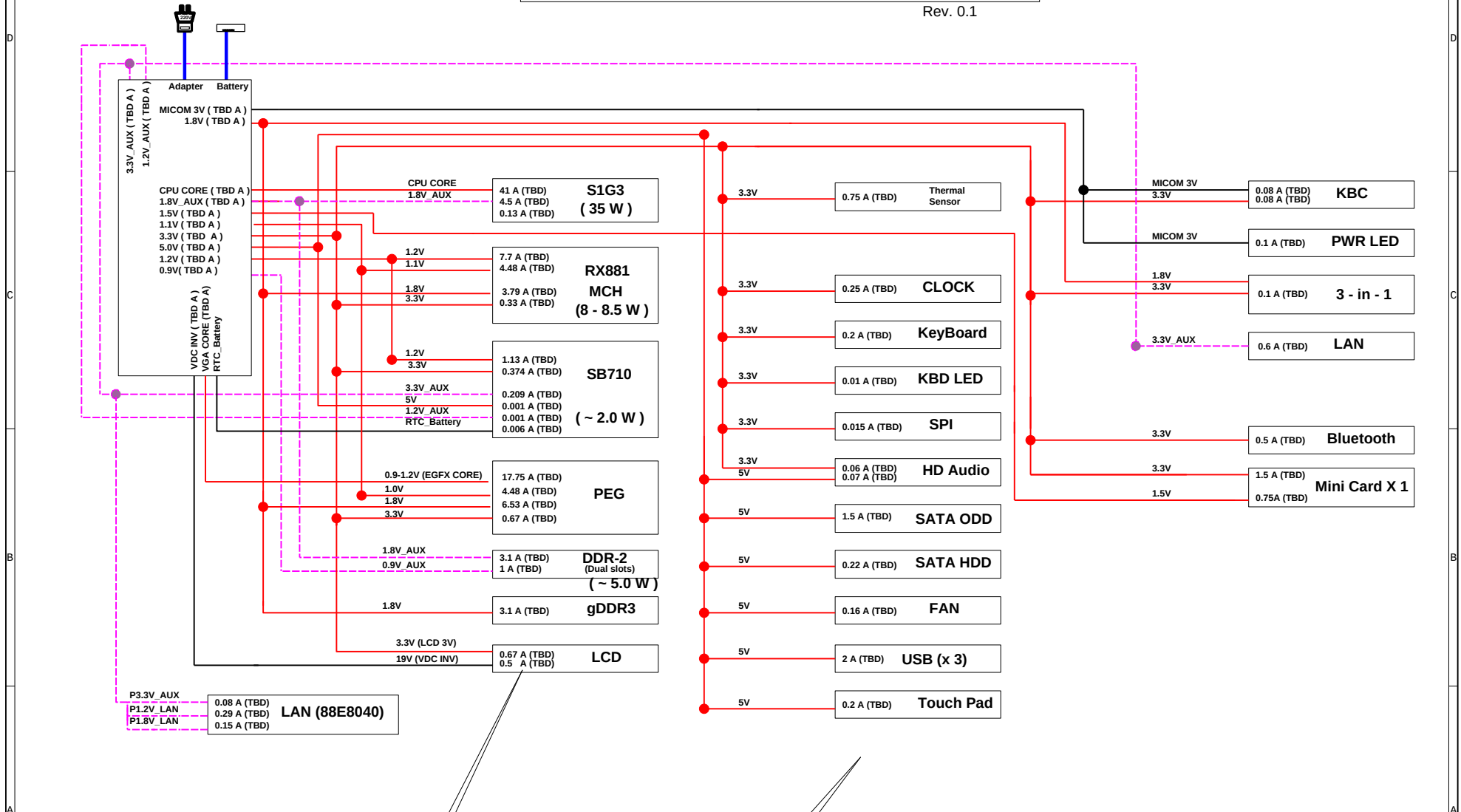
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DRAW	H.J.Ra	DATE	08/18/2009	TITLE	Bremen-D MAIN POWER DIAGRAM	SAMSUNG ELECTRONICS
CHECK	K.Y.Kim	DEV. STEP	ADV1			PART NO. BA41-xxxxxA
APPROVAL	H.K.Park	REV	1.1			
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POWER RAILS ANALYSIS

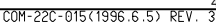
Rev. 0.1

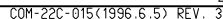


Value by Datasheet/Application notes (Value by measurement)

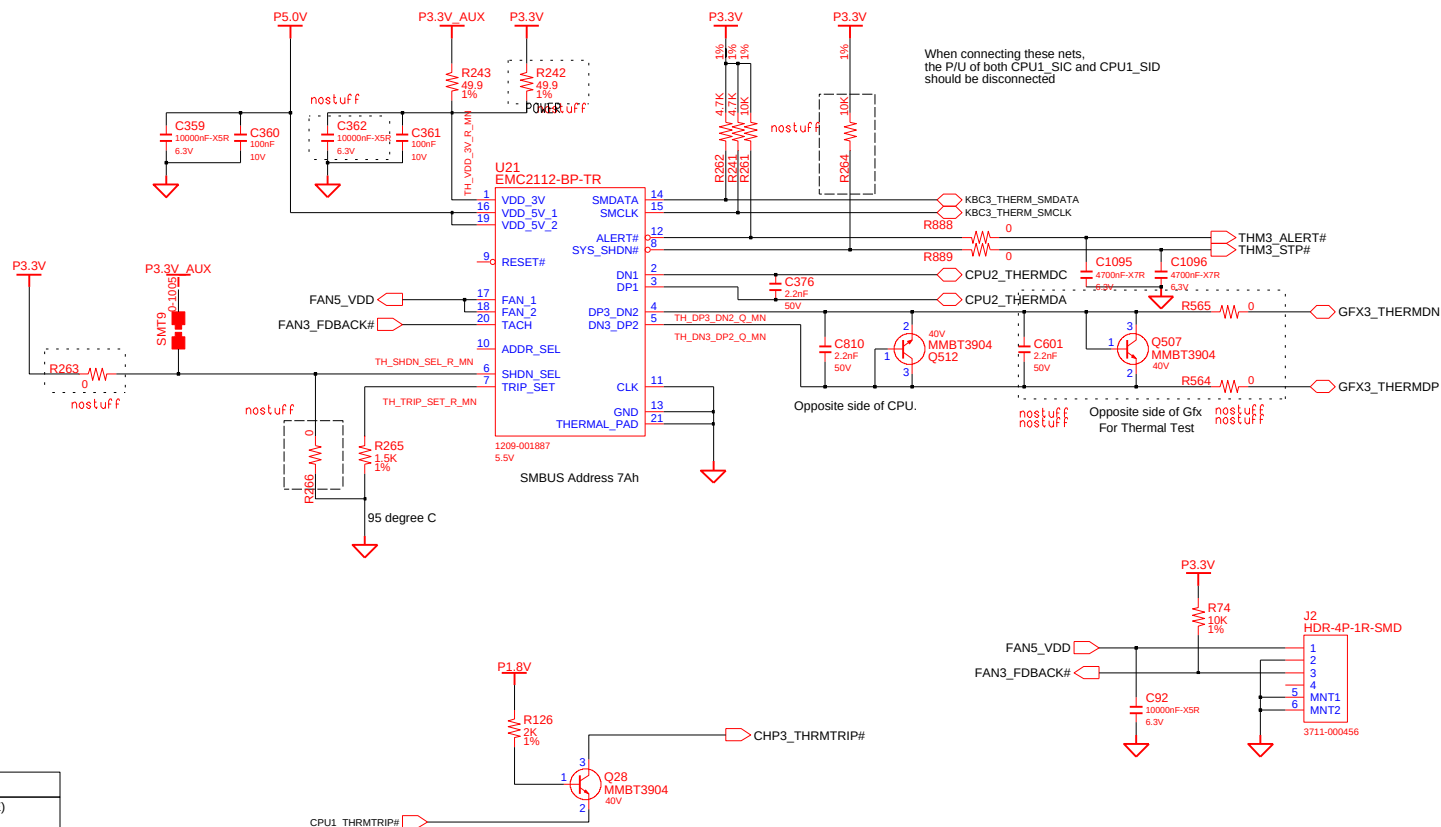
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CHECK	K.Y.Kim	DEV. STEP	ADV1	MAIN	MAIN	ELECTRONICS
APPROVAL	H.K.Park	REV	1.1	POWER RAILS ANALYSIS	PART NO.	BA41-xxxxxA
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Host S5 / ME Boot
(SLPS4* = SLPM*) > S4_STATE* > SLPS3*

D:/users/mobile58/mentor/Bremen-D/Bremen-D_Sub



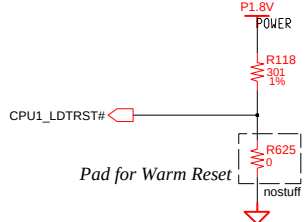
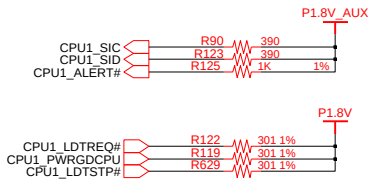
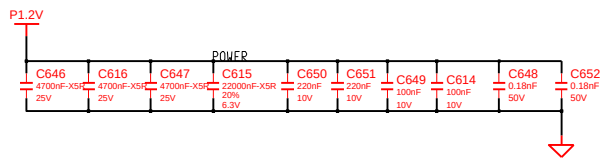
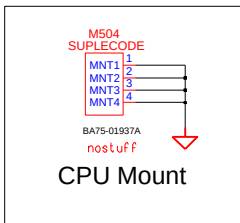
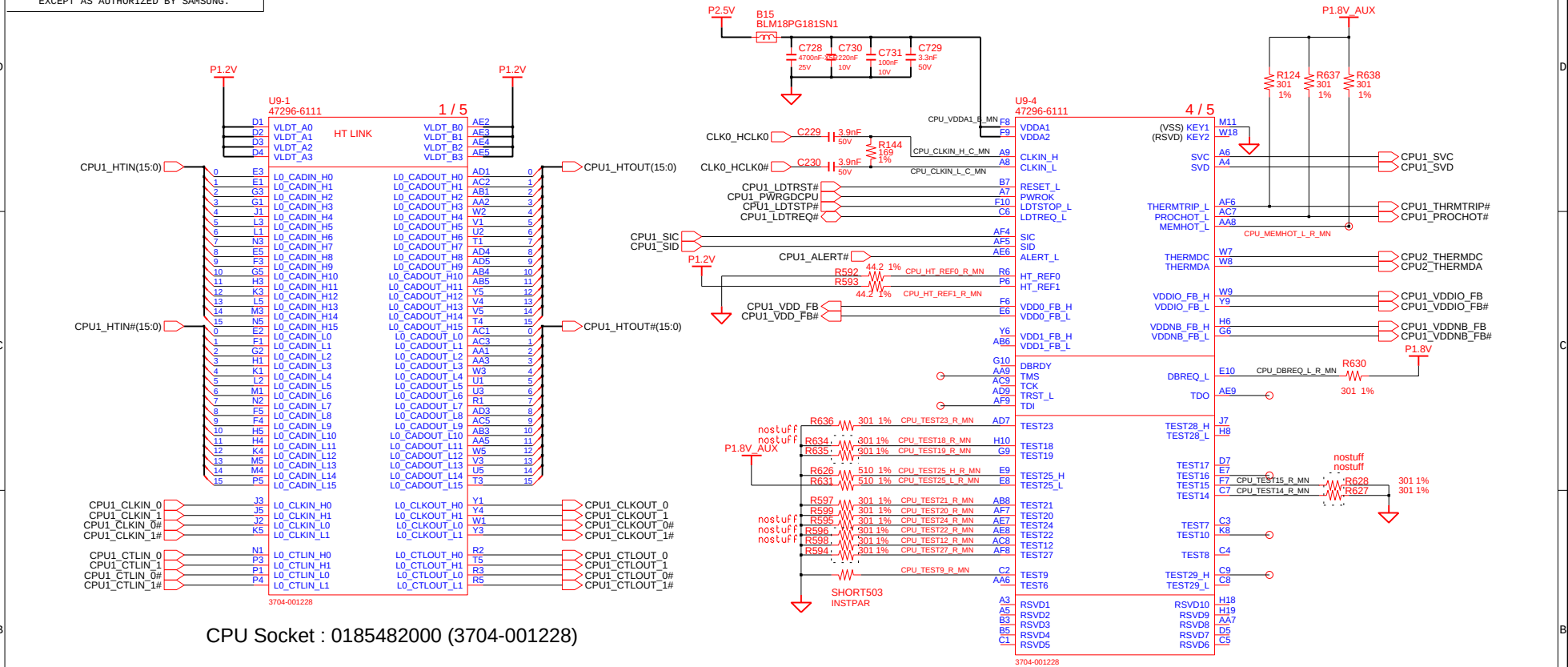
THERMAL SENSOR & FAN CONTROL



DESIGN	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D
CHECK	K.Y.Kim	DEV. STEP	ADV1		THERMAL SENSOR
APPROVAL	H.K.Park	REV	1.1		THERMAL SENSOR EMC2112
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CHECK	K.Y.Kim	DEV. STEP	ADV1			PART NO. BA41-xxxxxA
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE	undefined	LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	9	OF 61

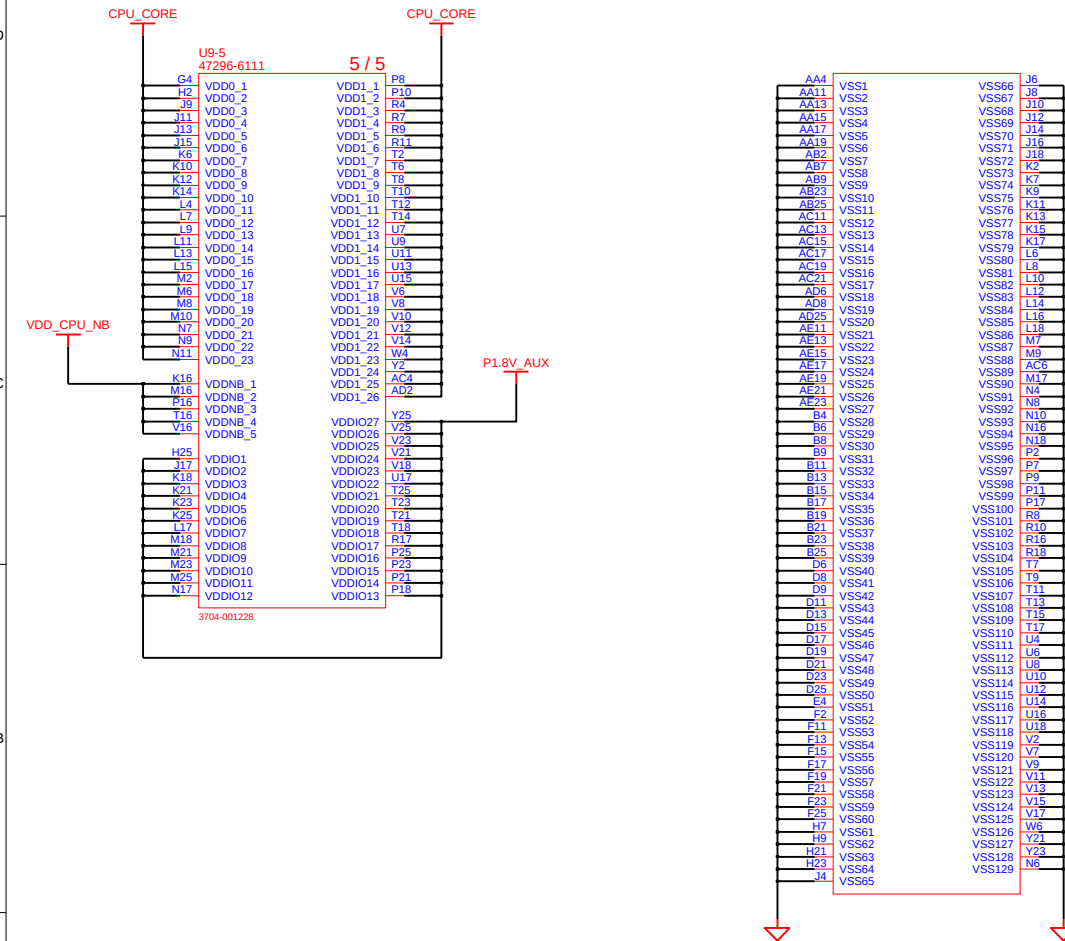
The diagram illustrates the internal circuitry of the SMD6000 board, centered around three main ICs: U9-3 (47296-6111), U9-2 (47296-6111), and U9-1 (47296-6111). These are connected to various power supplies and signal lines.

- Power Supplies:**
 - P0.9V_AUX: Connected to U9-2 and U9-1.
 - P1.8V_AUX: Connected to U9-3.
 - P3.3V: Connected to MCH3_EXTTSO# and MCH3_EXTTST1#.
- Memory Modules:**
 - MEM1_ADM(7:0) and MEM1_ADQ(63:0): Connected to U9-3.
 - MEM1_ADQS(7:0) and MEM1_BDQ(63:0): Connected to U9-3.
 - MEM1_BQM(7:0) and MEM1_BDS(7:0): Connected to U9-3.
 - MEM1_AMA(15:0) and MEM1_ABS(2:0): Connected to U9-2.
 - MEM1_ARAS#, MEM1_ACAS#, MEM1_AWE#: Connected to U9-2.
 - MEM1_ADD0 to MEM1_ADD15: Connected to U9-2.
 - MEM1_BANK0 to MEM1_BANK2: Connected to U9-2.
 - MEM1_RAS_L, MEM1_CAS_L, MEM1_WE_L: Connected to U9-2.
 - MEM1_BRAS#, MEM1_BCAS#, MEM1_BWE#: Connected to U9-2.
- Other Components:**
 - CPU_MEMZP_R_MIN, CPU_MEMZN_R_MIN: Connected to U9-2.
 - RSVD_M1, RSVD_M2: Connected to U9-2.
 - MB_DATA0 to MB_DATA63: Connected to U9-3.
 - MB_DATA0 to MB_DATA63: Connected to U9-2.
 - MB_DATA0 to MB_DATA63: Connected to U9-1.
 - MB_DATA0 to MB_DATA63: Connected to U9-0.

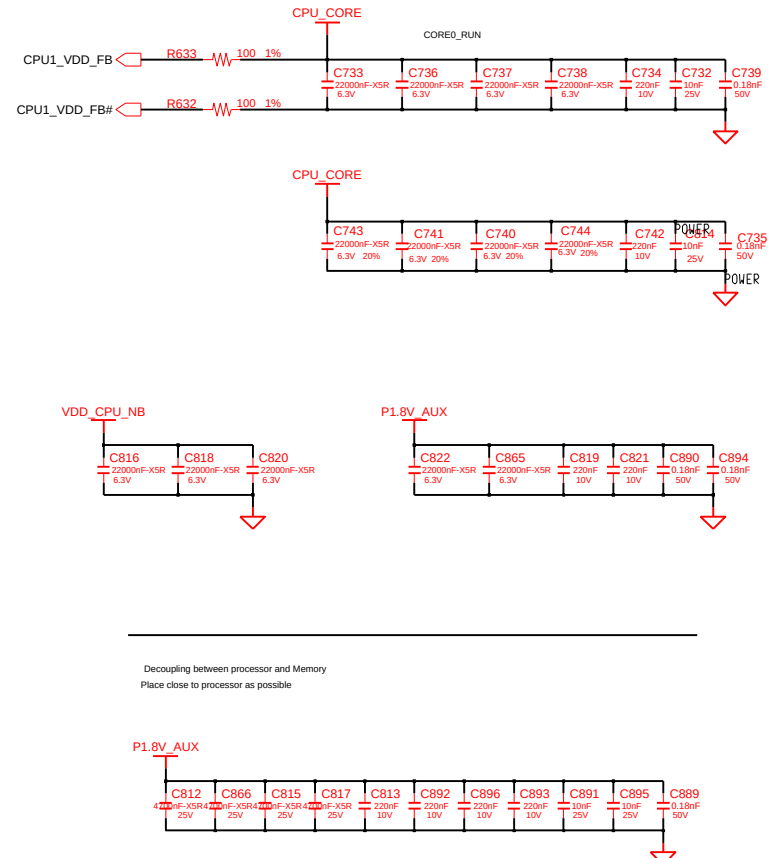
The diagram also shows various capacitors (C823, C824, C242, C241, C260, C261, C236, C238, C234, C231, C237, C235, C232, C233, C259, C228, C239, C240) and resistors (R146, R145, R822, R793) used for timing and signal conditioning.

DRAW	H.J.Ra	DATE	9/23/2008	Bremen-D CPU Caspian (2/3)	SAMSUNG ELECTRONICS				
CHECK	K.Y.Kim	DEV. STEP	ADV1						
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PART NO.			BA41-xxxxxA						
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CPU_Caspian

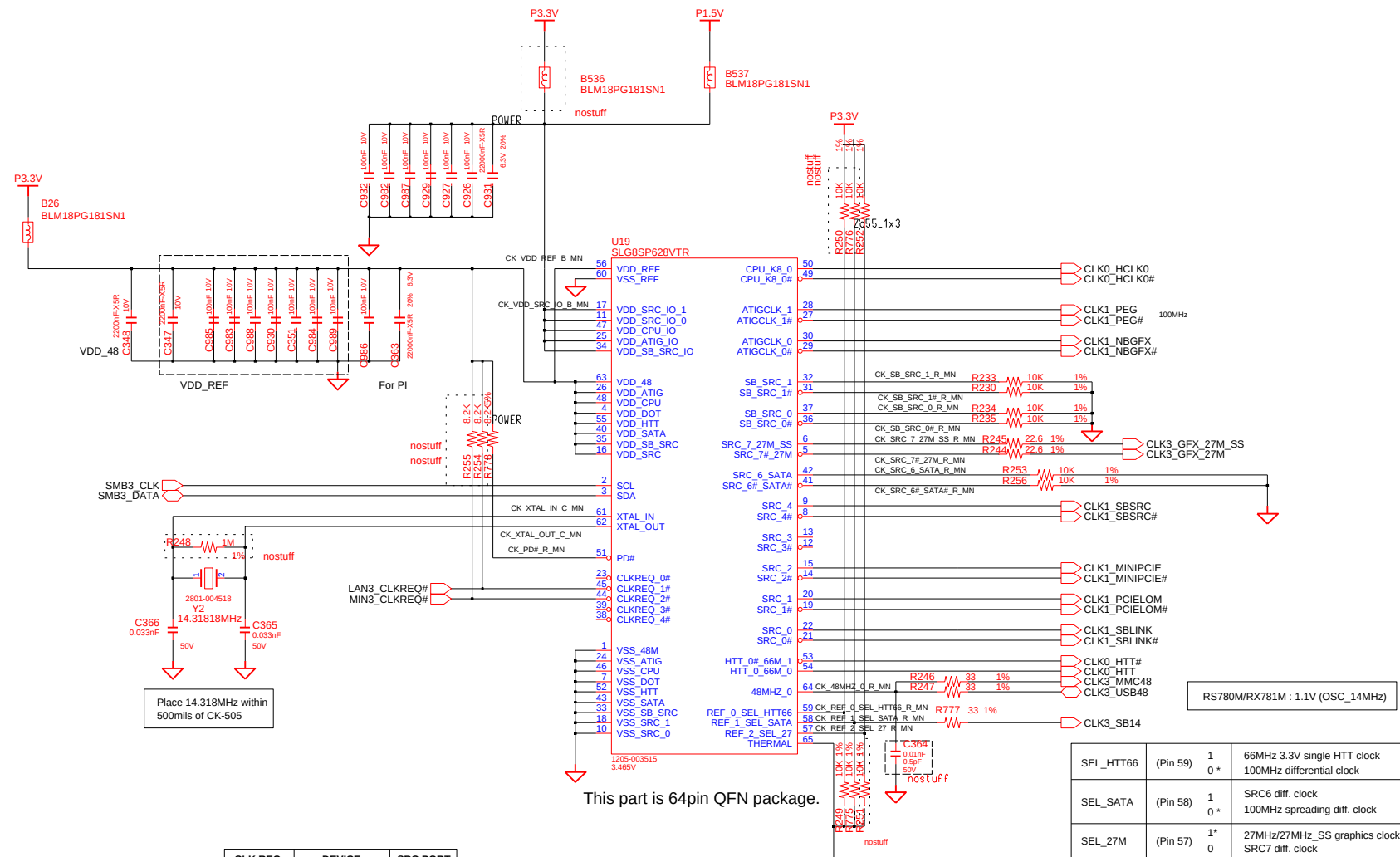


Bottom side decoupling



Decoupling between processor and Memory
Place close to processor as possible

DRAW	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D CPU Caspian (3/3)	SAMSUNG ELECTRONICS
CHECK	K.Y.Kim	DEV. STEP	ADV1			PART NO. BA41-xxxxxA
APPROVAL	H.K.Park	REV	1.1			
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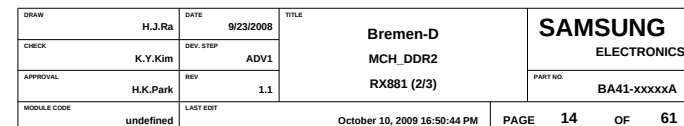
CLK REQ	DEVICE	SRC PORT
CLK REQ 0	-	SB Link
CLK REQ 1	LOM3_CLKREQ#	LOM
CLK REQ 2	MIN3_CLKREQ#	MINI CARD
CLK REQ 3		
CLK REQ 4	-	SB_SRC

SEL_HTT66	(Pin 59)	1 0 *	66MHz 3.3V single HTT clock 100MHz differential clock
SEL_SATA	(Pin 58)	1 0 *	SR6C diff. clock 100MHz spreading diff. clock
SEL_27M	(Pin 57)	1* 0	27MHz/27MHz_SS graphics clock SRC7 diff. clock

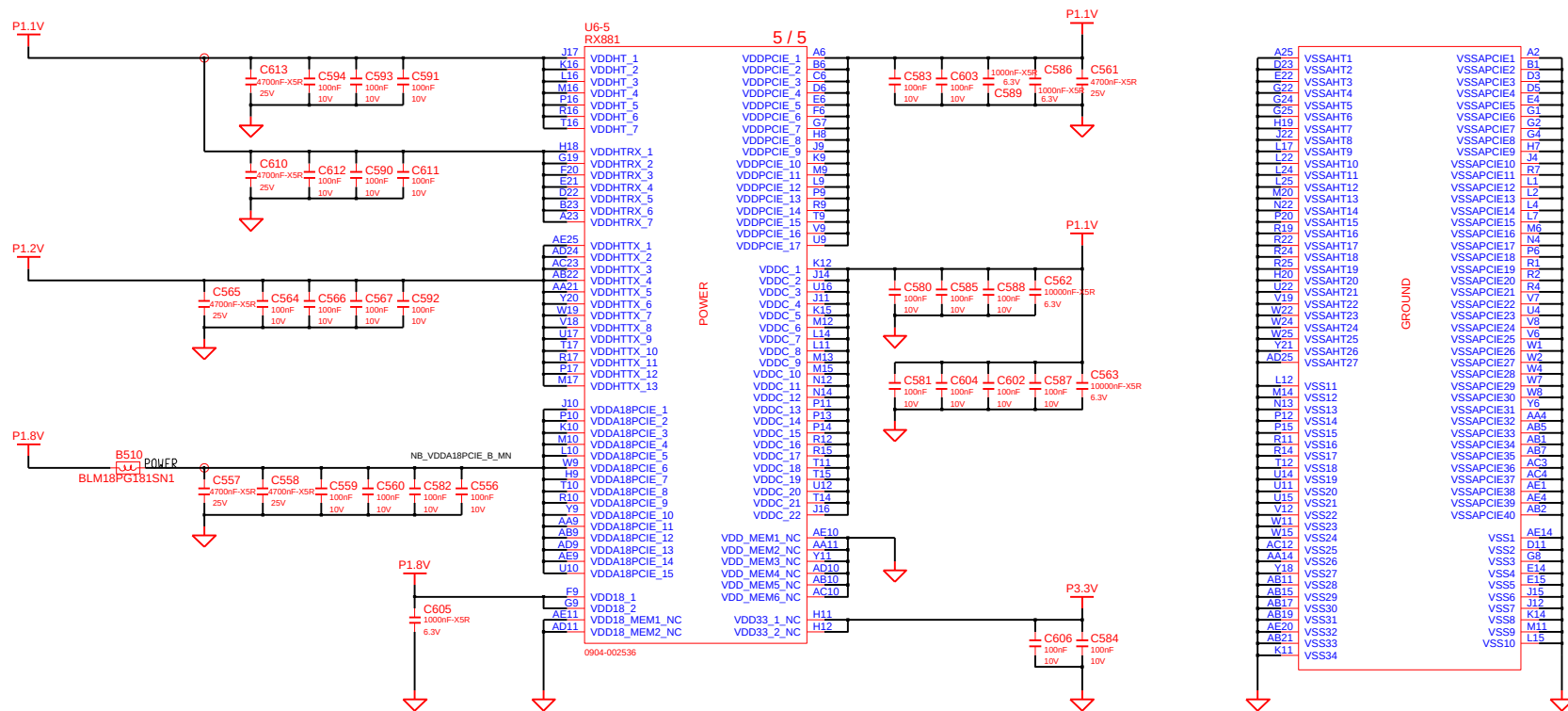
DRAW	H.J.Ra	DATE	9/23/2008	Bremen-D MAIN_CLOCK_CIRCUIT CK_Clock_505M	SAMSUNG ELECTRONICS				
CHECK	K.Y.Kim	DEV_STEP	ADV1						
APPROVAL	H.K.Park	REV	1.1						
					PART NO.	BA41-xxxxxA			
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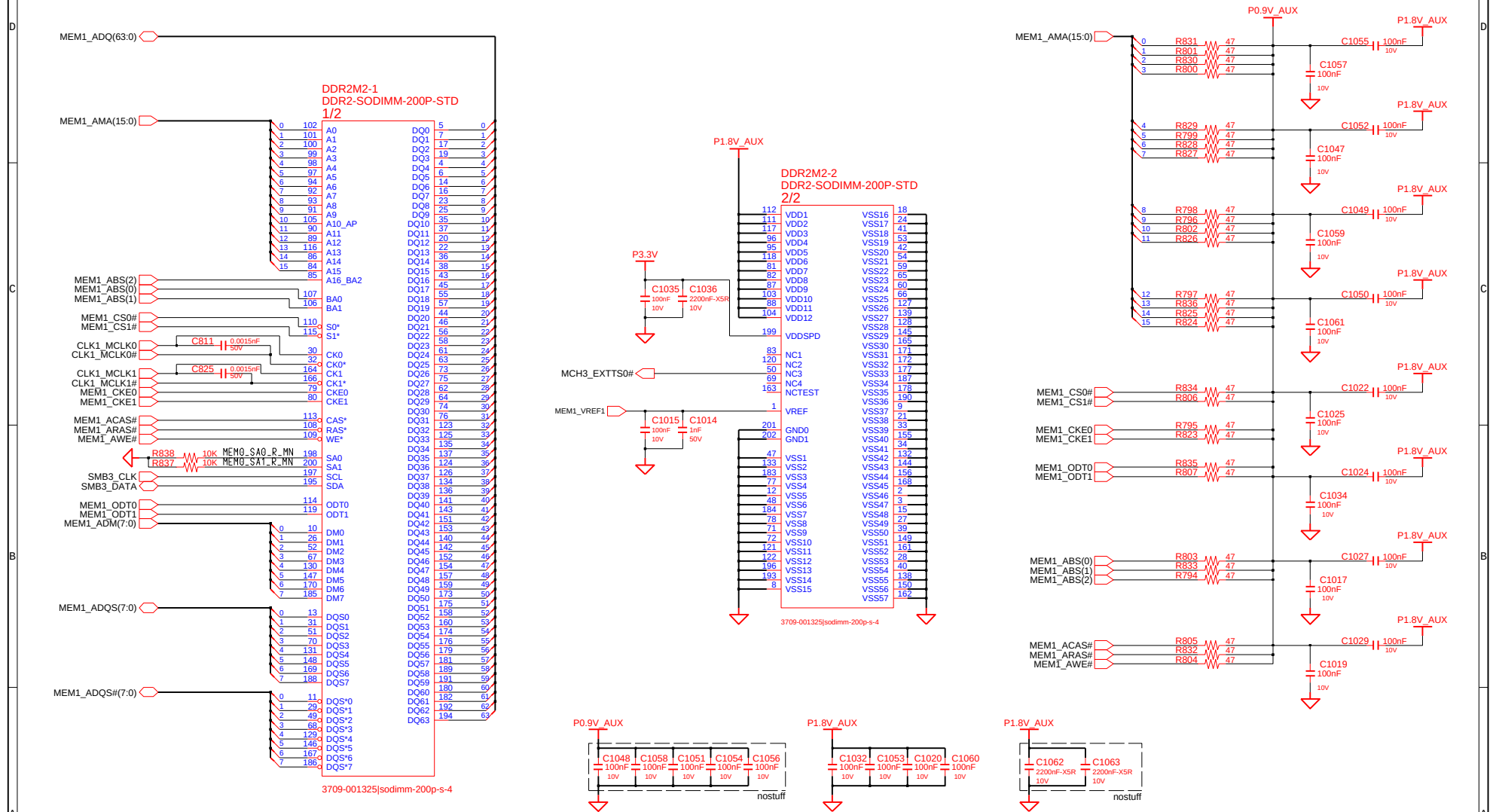
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DRAW	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D	SAMSUNG
CHECK	K.Y.Kim	DEV. STEP	ADV1		MCH_DDR2	ELECTRONICS
APPROVAL	H.K.Park	REV	1.1		RX881 (3/3)	PART NO.
MODULE CODE		LAST EDIT				BA41-xxxxxA
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DDR SO-DIMM #0



Place near SO-DIMM0

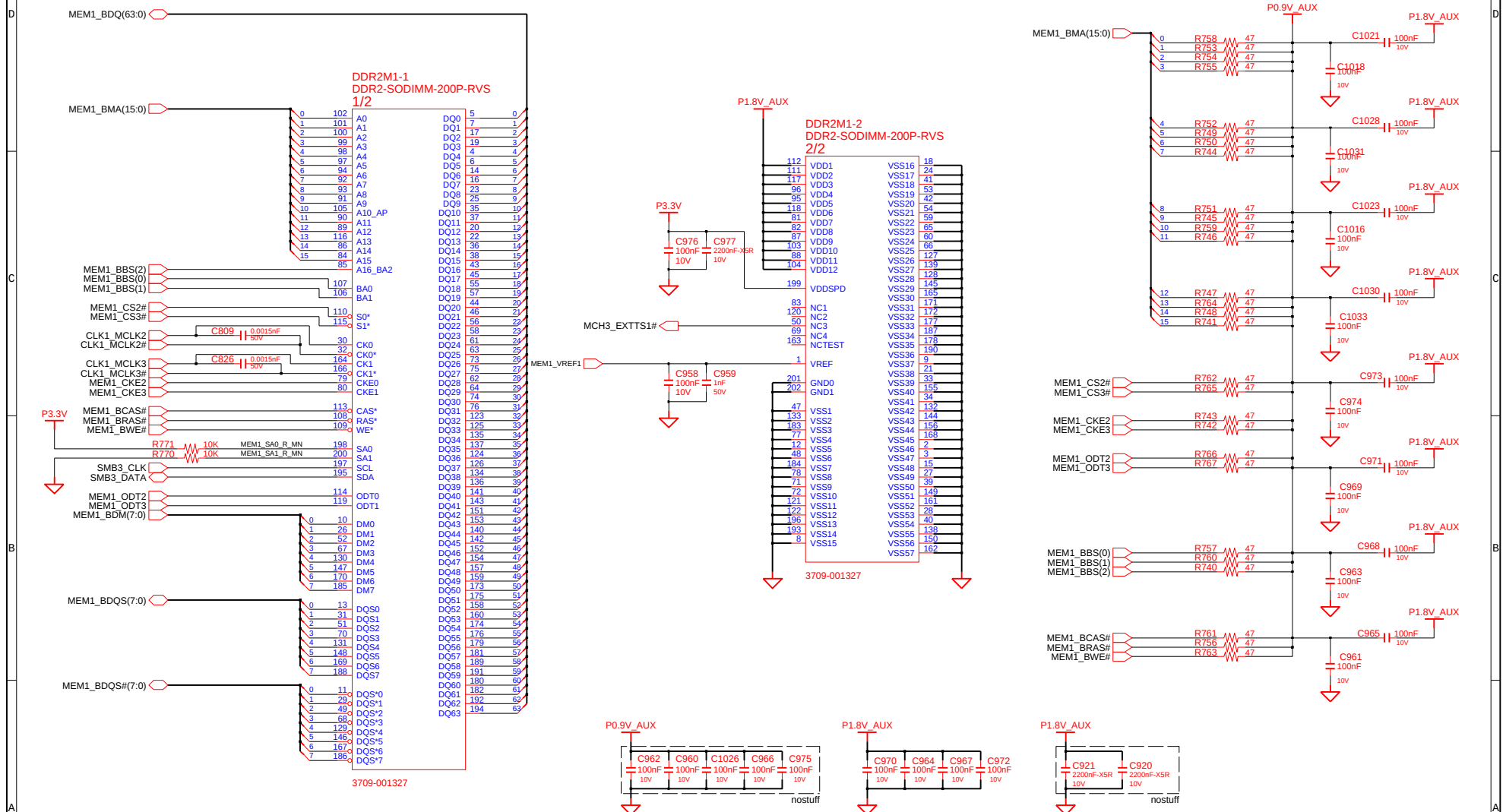
DRAW	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D
CHECK	K.Y.Kim	DEV. STEP	ADV1		SODIMM_DDR2
APPROVAL	H.K.Park	REV	1.1		SODIMM_DDR2 (1/2)
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				October 10, 2009 16:50:44 PM	PAGE 16 OF 61

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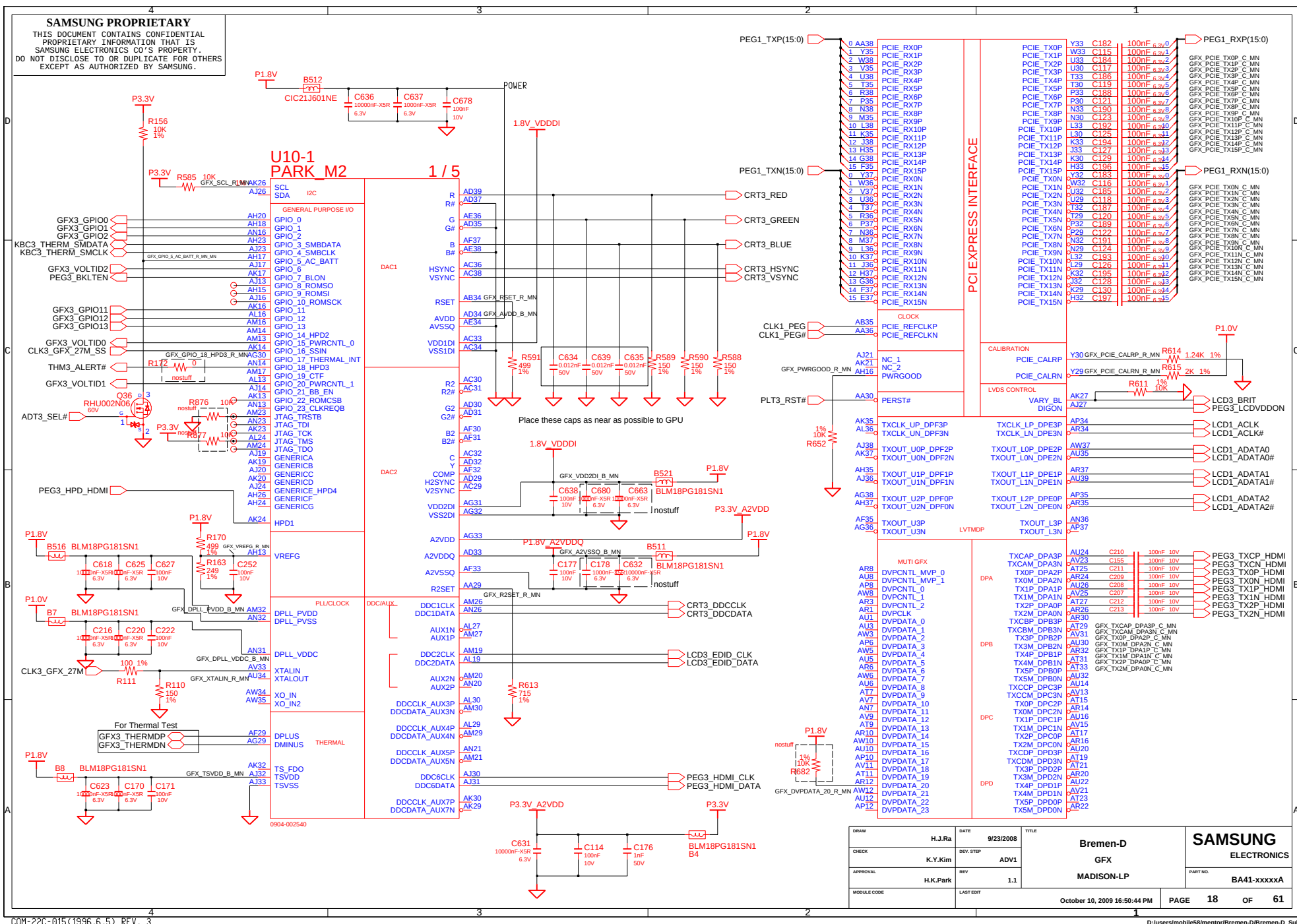
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DDR SO-DIMM #1

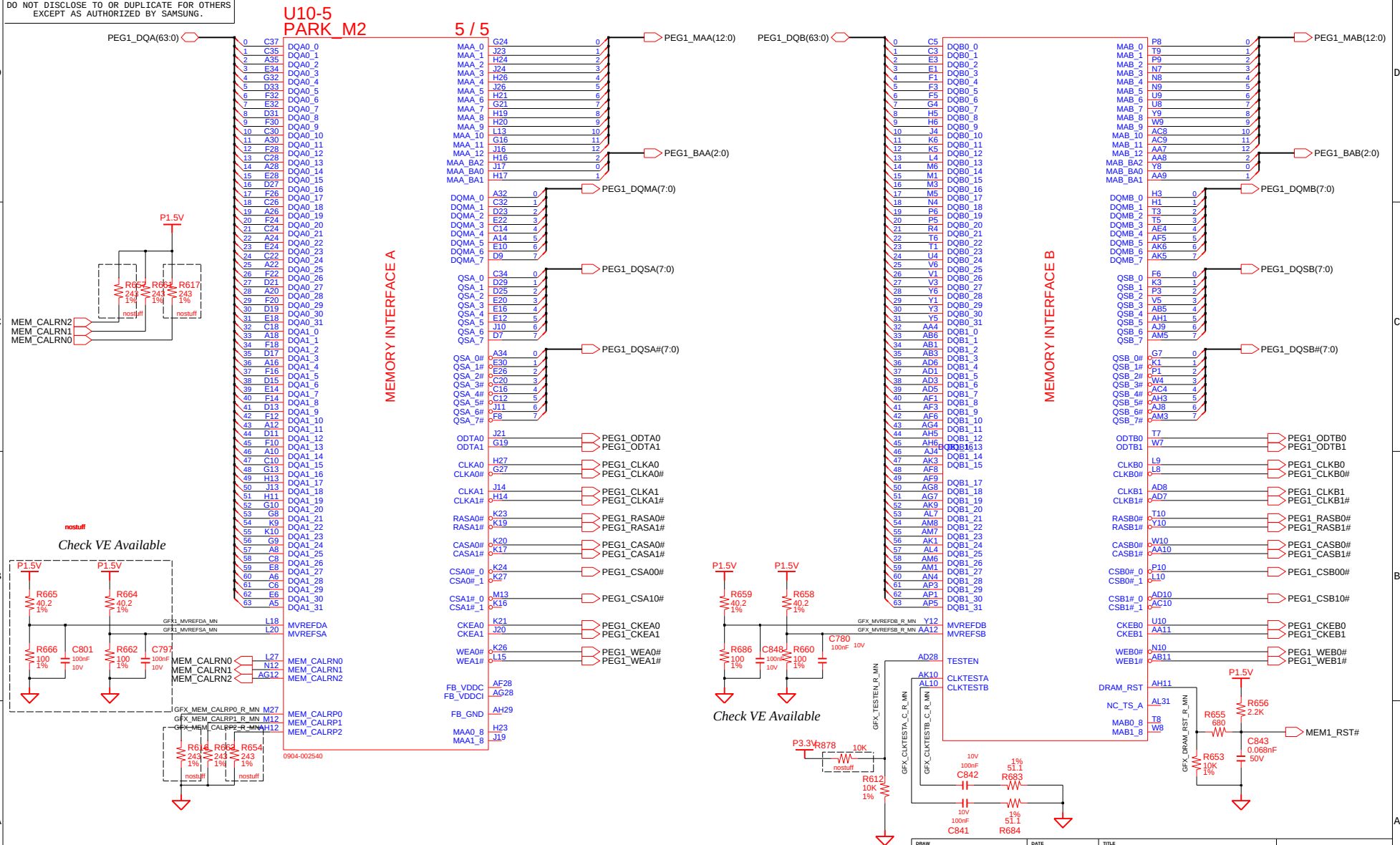


DRAW	H.J.Ra	DATE	9/23/2008	TITLE Bremen-D SODIMM_DDR2 SOCIMM_DDR2 (2/2)			
CHECK	K.Y.Kim	DEV. STEP	ADV1		PART NO.	BA41-xxxxxA	
APPROVAL	H.K.Park	REV	1.1				
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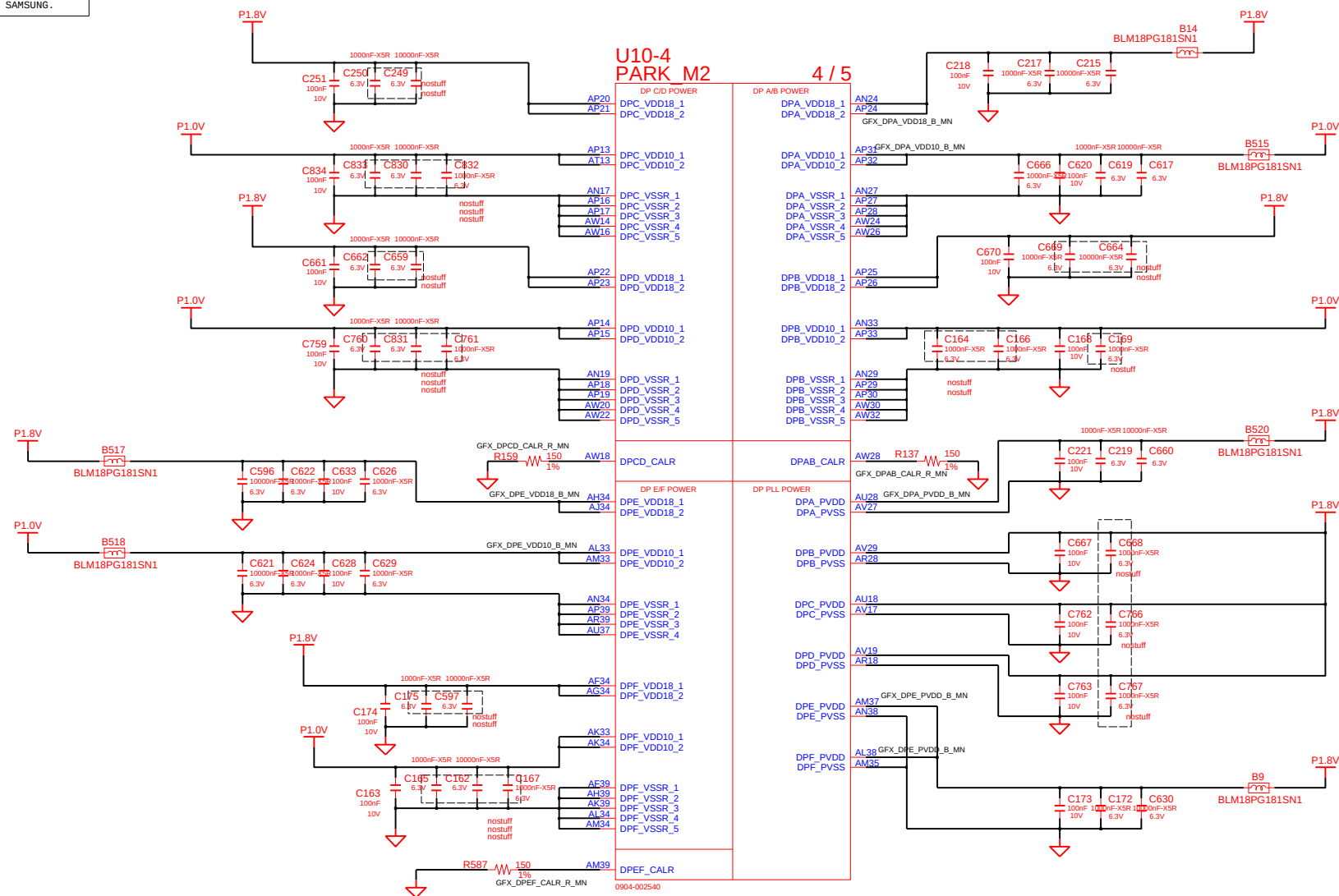


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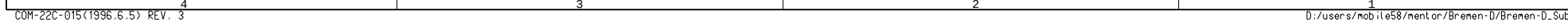
DRAW	H.J.Ra	DATE	9/23/2008	Bremen-D GFX MADISON-LP	SAMSUNG ELECTRONICS				
CHECK	K.Y.Kim	DEV. STEP	ADV1						
APPROVAL	H.K.Park	REV	1.1						
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DESIGN	H.J.Rø	DATE	9/3/2009	TITLE Bremen-D GFX MADISON-LP	SAMSUNG ELECTRONICS
CHECK	K.Y.Kim	DEV. STEP	ADV1		
APPROVAL	H.K.Park	REV	1.1		
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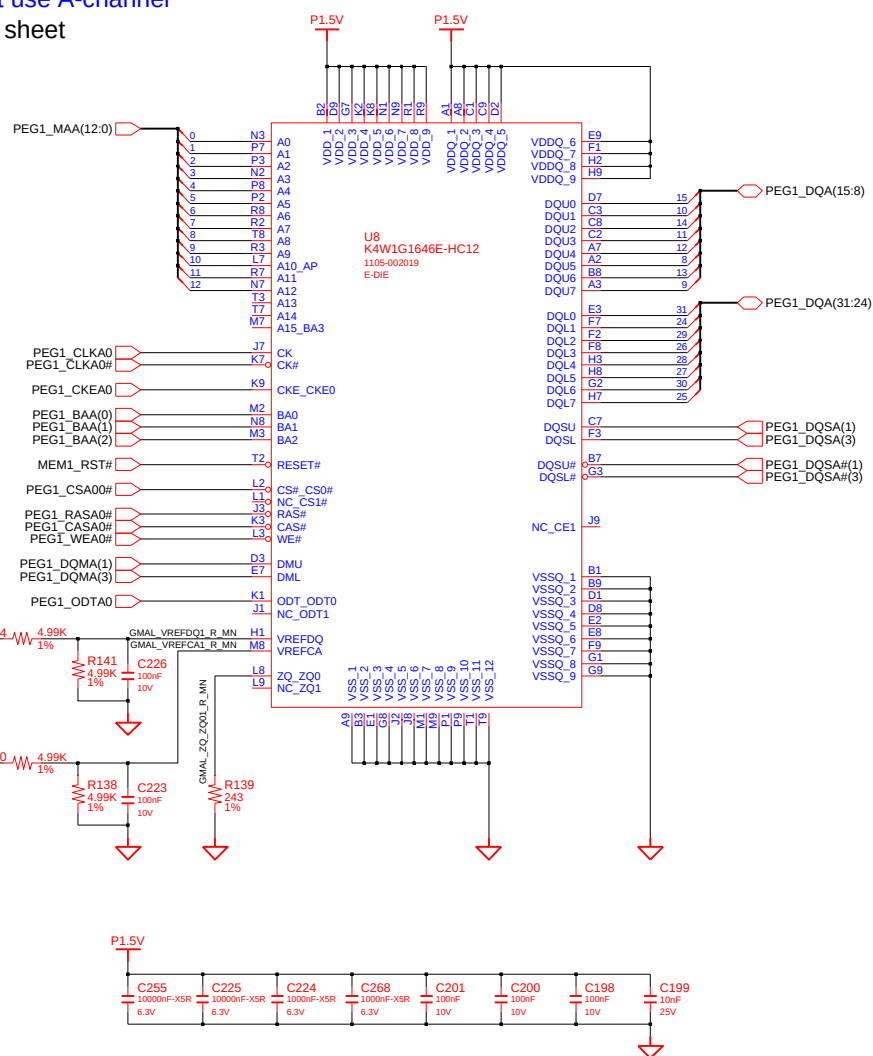


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PARK-XT M2 doesn't use A-channel

Nostuff this sheet

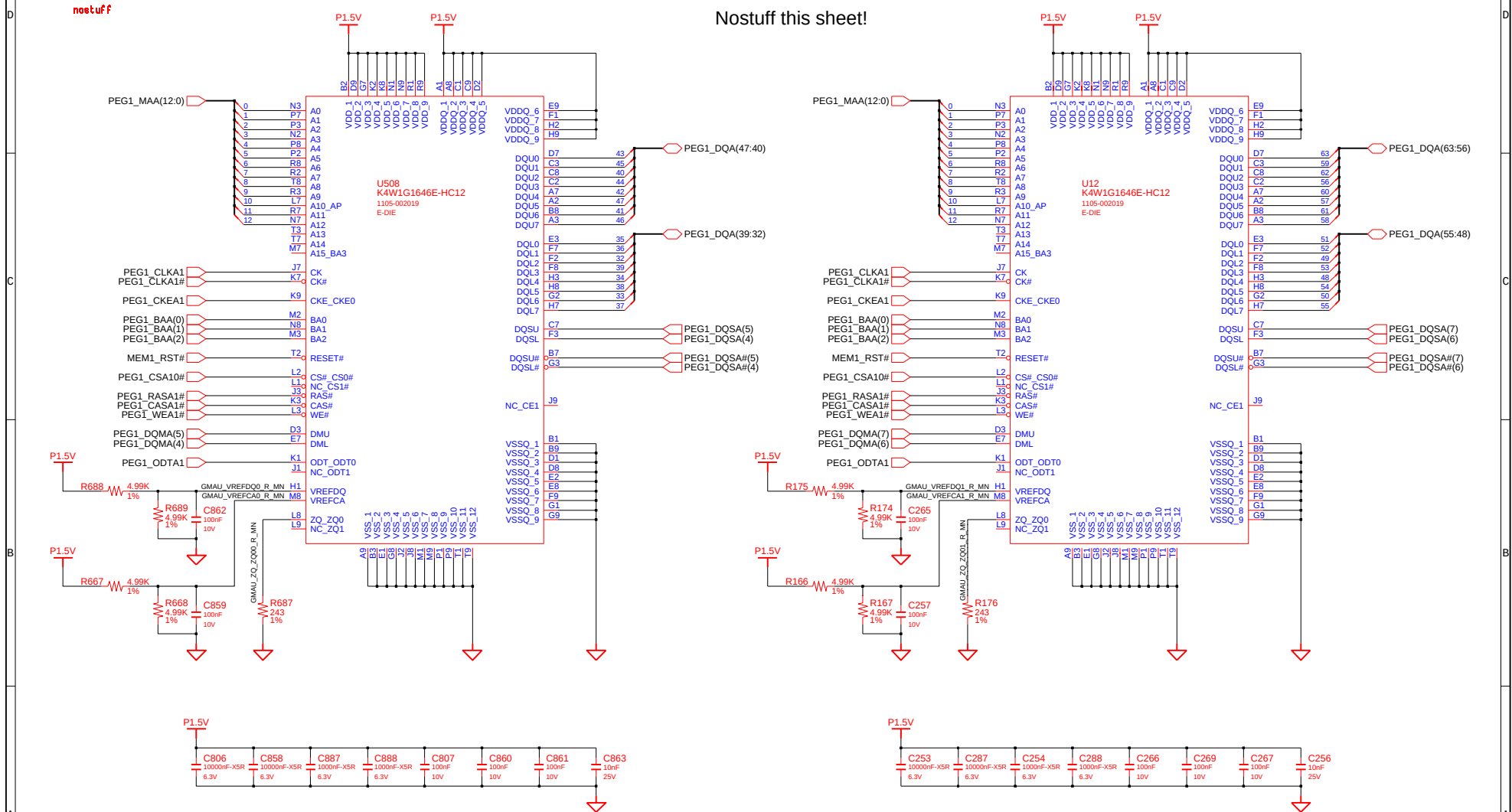


DESIGN	H.J.Rø	DATE	9/3/2009	TITLE Bremen-D GRAPHICS MEMORY gDDR3	SAMSUNG ELECTRONICS
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APPROVAL	H.K.Park	REV	1.1		
PART NO.			BA41-xxxxxA		
MODULE CODE		LAST EDIT		October 10, 2009 16:50:44 PM	PAGE 23 OF 61

A-channel Upper Data

PARK-XP M2 doesn't use A-channel

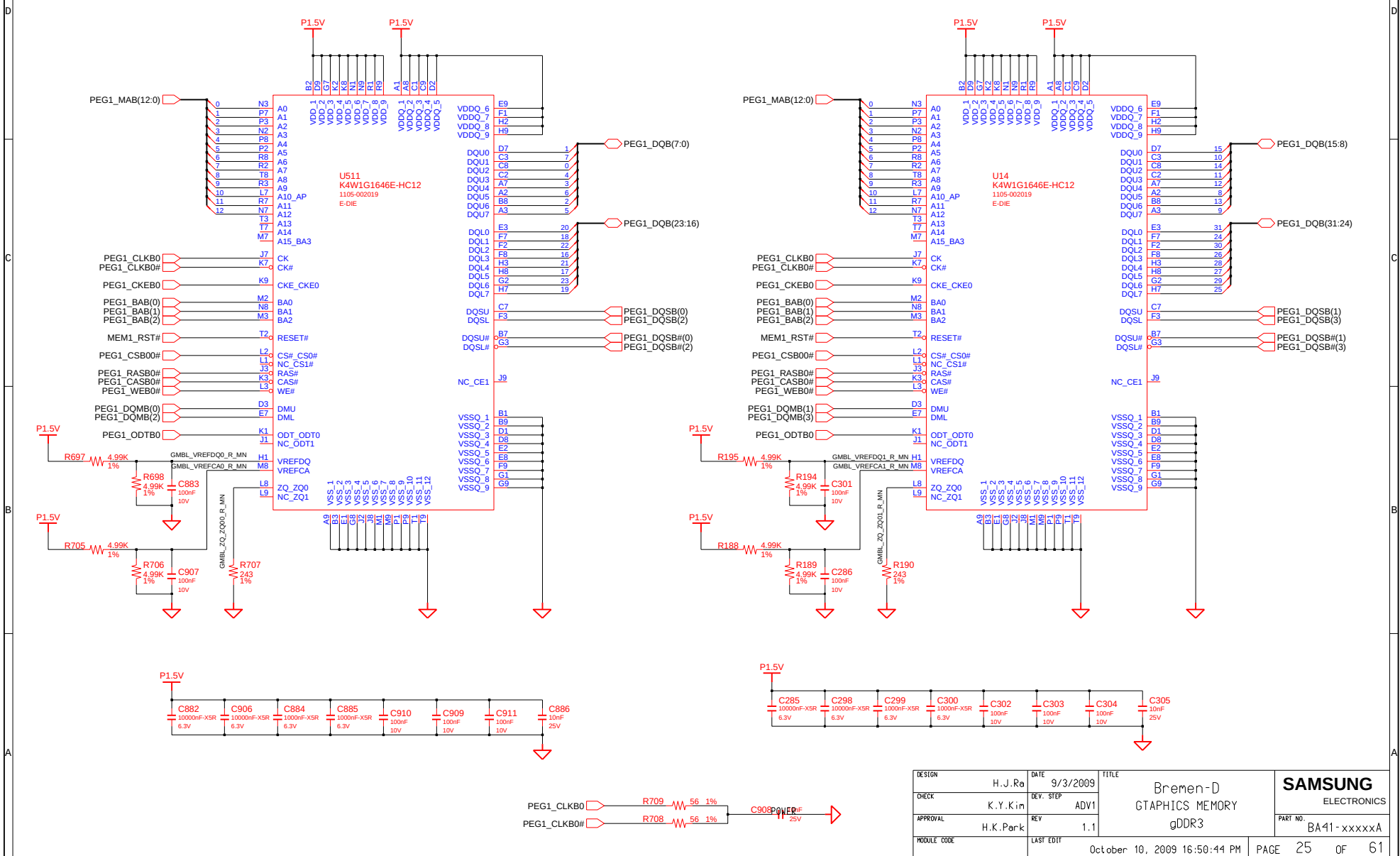
Nostuff this sheet!



PEG1_CLKA1 R178 56 1%
PEG1_CLKA1# R177 56 1%

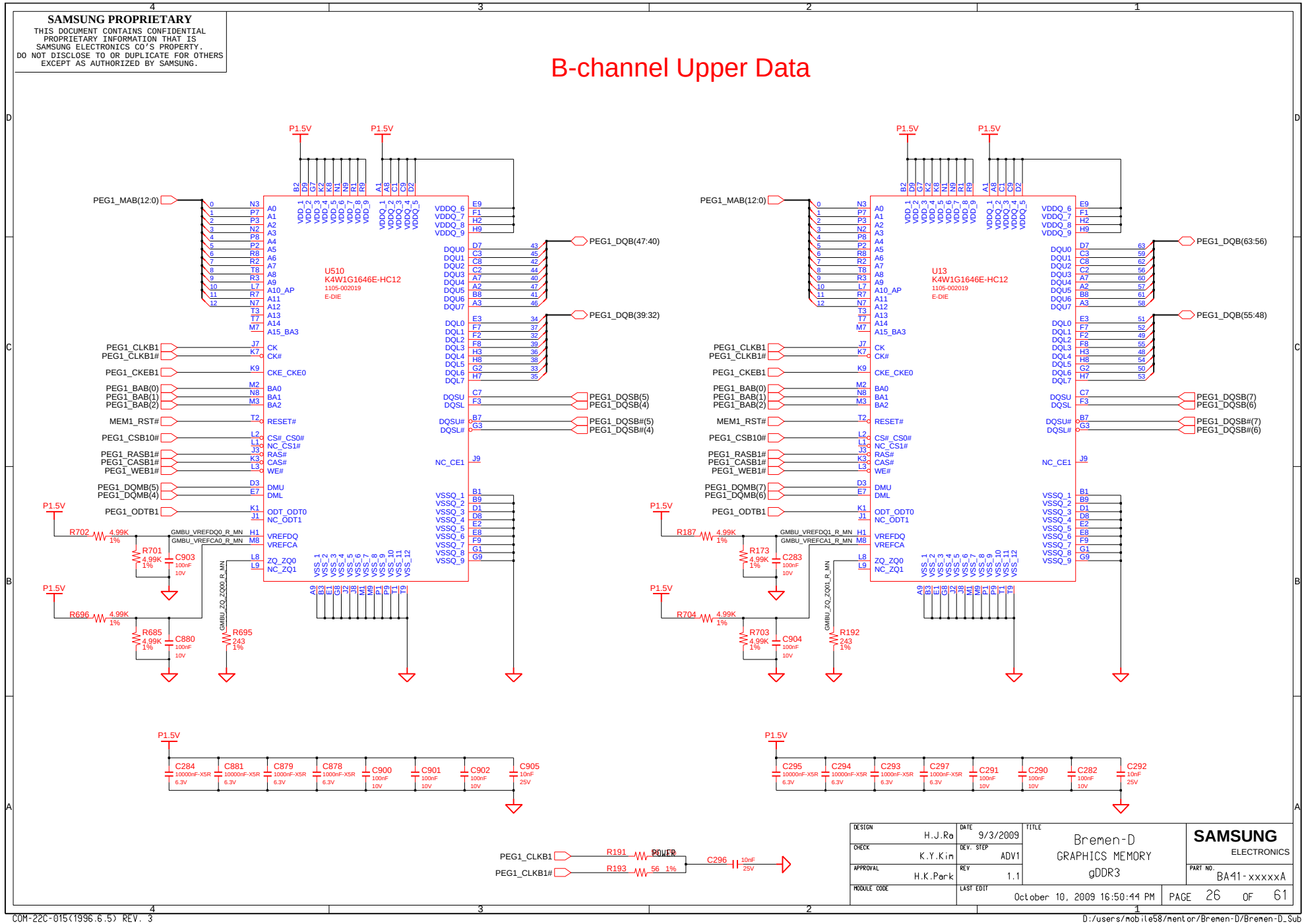
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CHECK	K.Y.Kim	DEV. STEP	ADV1			
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE		LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	24 OF 61	

B-channel Lower Data



DESIGN	H.J.Ro	DATE	9/3/2009	TITLE	Bremen-D GRAPHICS MEMORY gDDR3	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxA
CHECK	K.Y.Kim	DEV. STEP	ADV1			
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE		LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	25 OF 61	

B-channel Upper Data



BIF_GEN2_EN_A
0 : 2.5GT/s CAPABLE FOR PCIe DEVICE
1 : 5.0GT/s CAPABLE FOR PCIe DEVICE
=> 5.0GT/s CAPABILITY WILL BE
CONTROLLED BY SOFTWARE

GFX3_GPIO2

notstuff

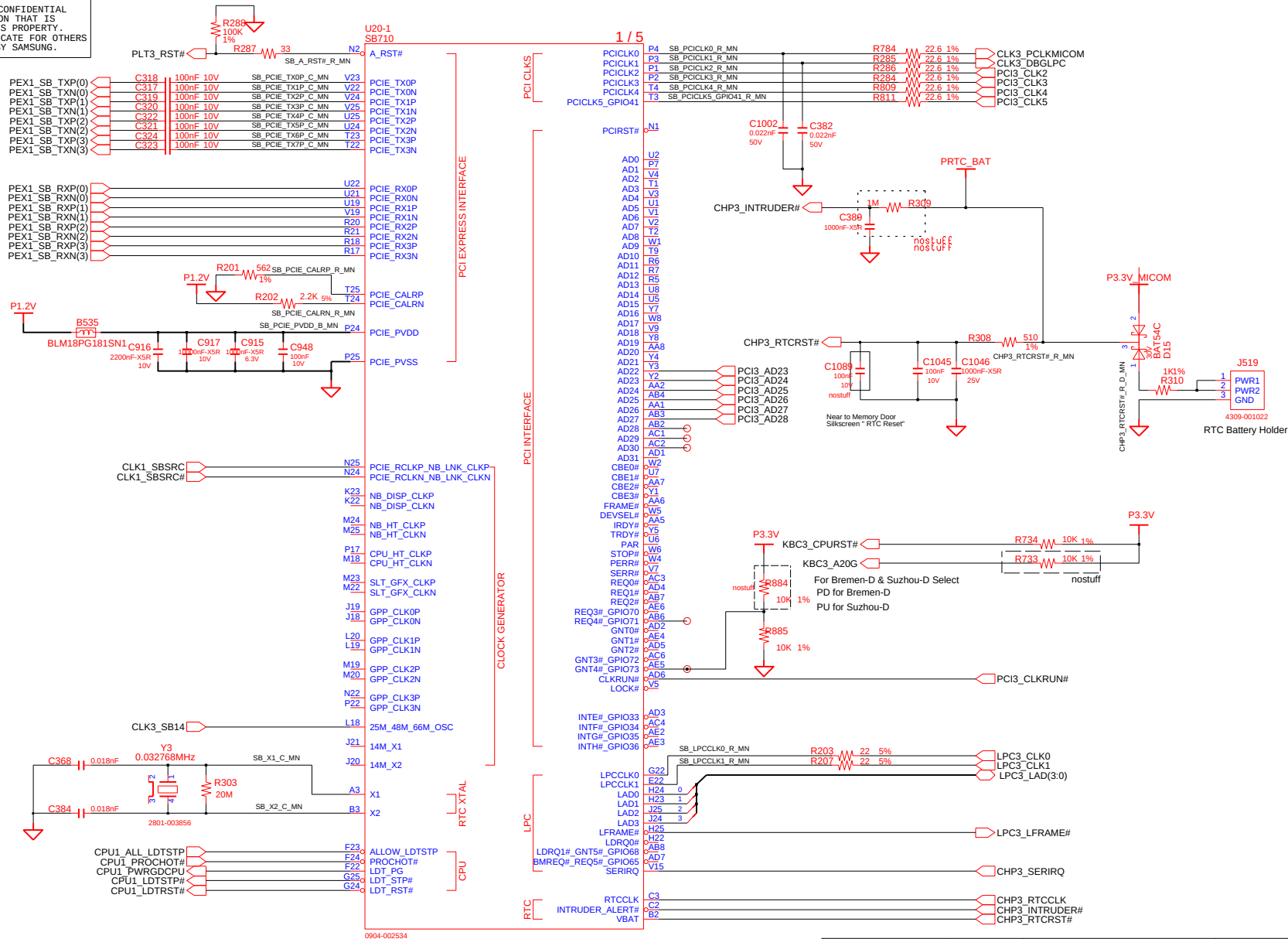
R157 10K 1%

R158 10K 1%

P3.3V

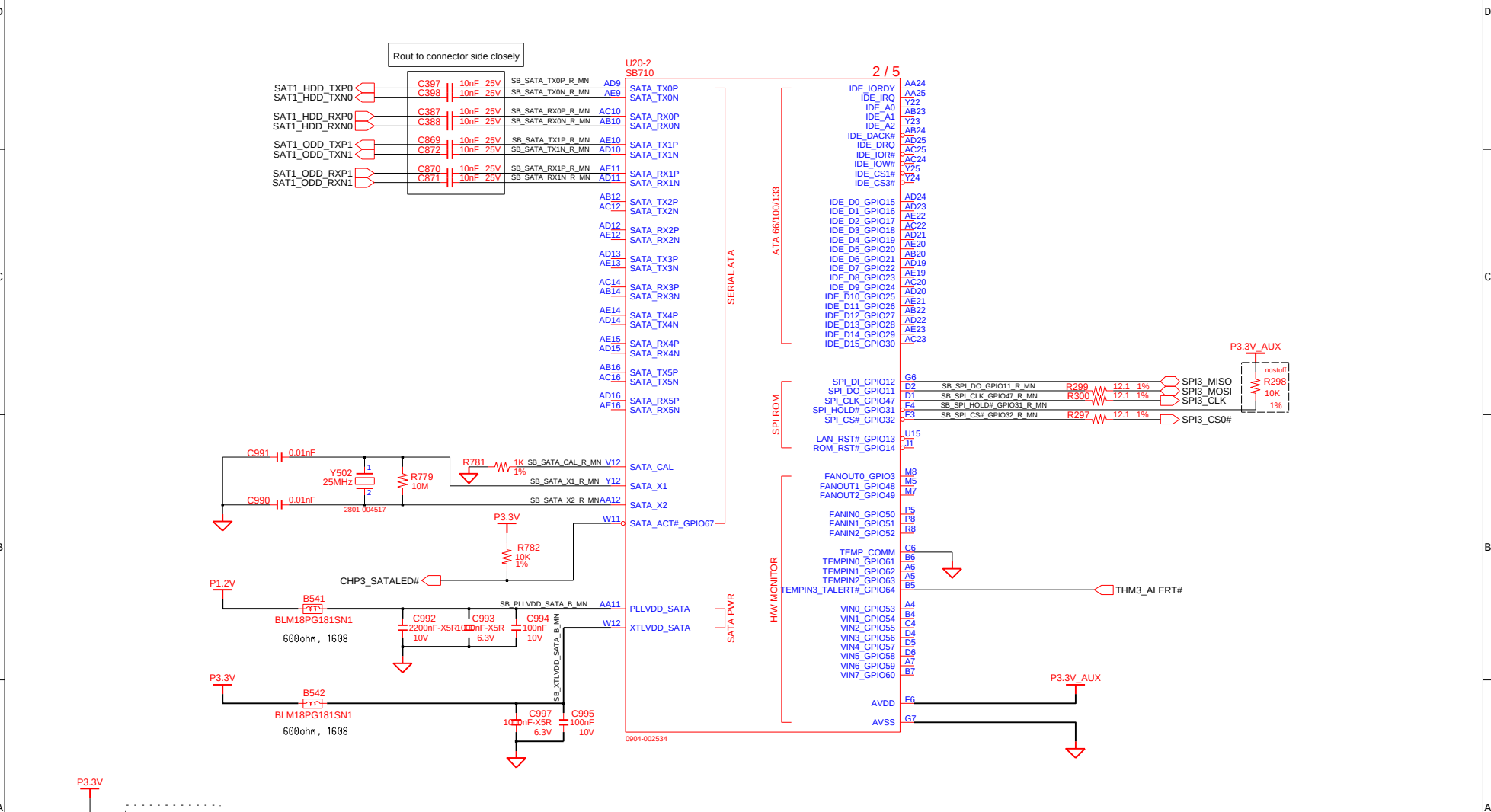
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APPROVAL	H.K.Park	REV	1.1		
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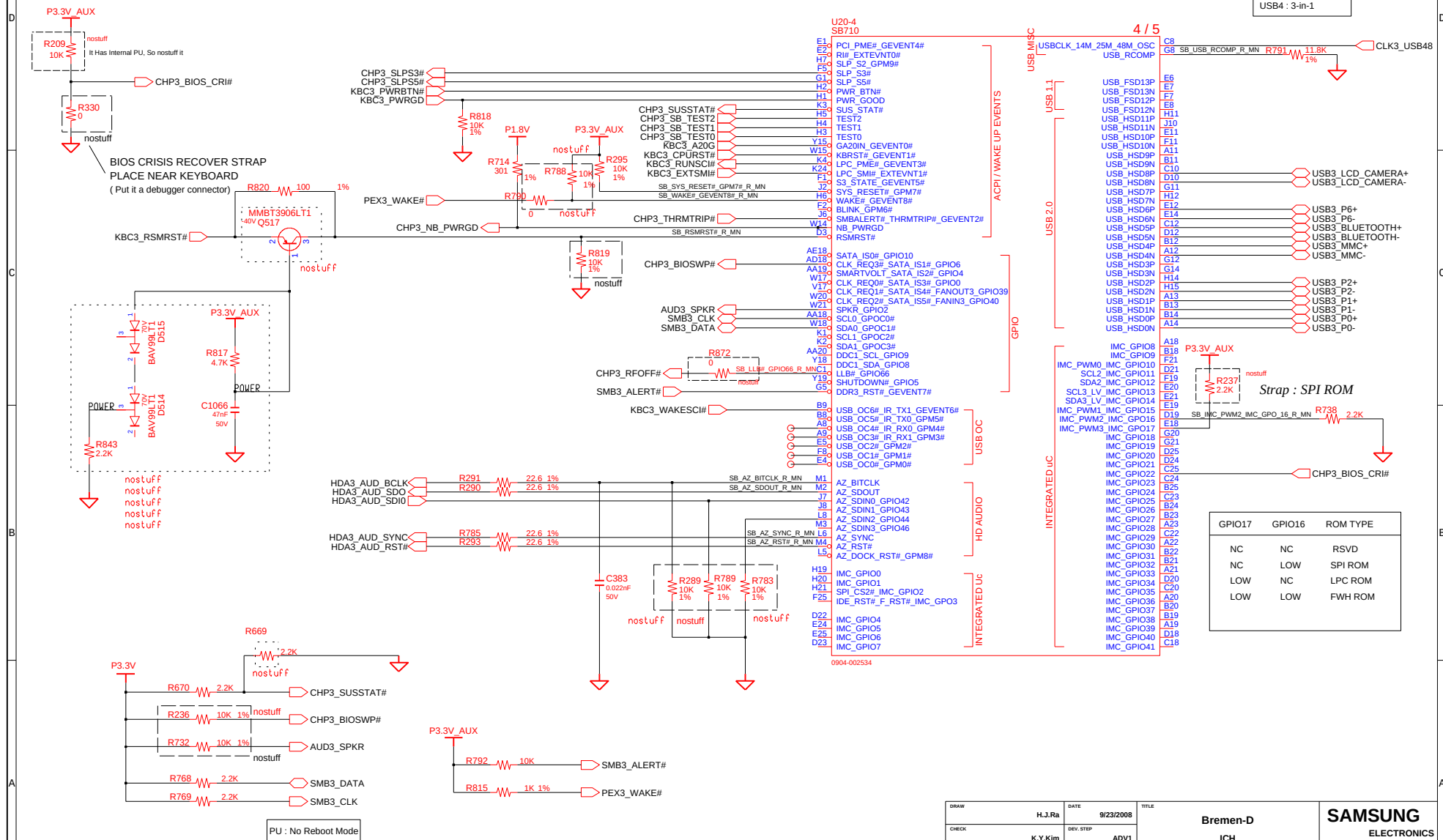
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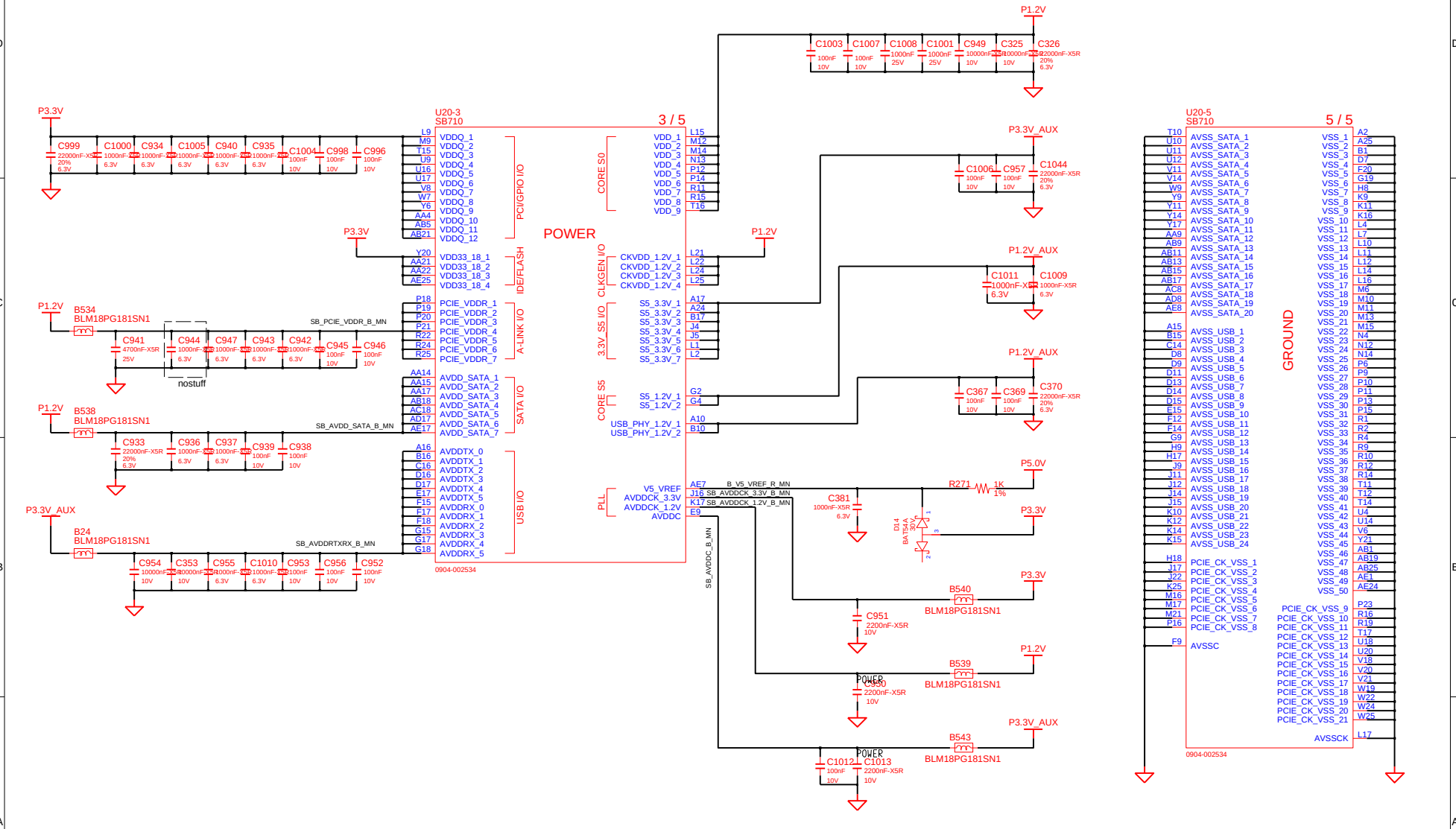
USB1, 6 : Right Port
USB0 : Left Port
USB5 : Bluetooth
USB8 : Camera
USB4 : 3-in-1



GPIO17	GPIO16	ROM TYPE
NC	NC	RSVD
NC	LOW	SPI ROM
LOW	NC	LPC ROM
LOW	LOW	FWH ROM

DRAW	H.J.Ra	DATE	9/23/2008	Bremen-D ICH SB710 (3/5)	SAMSUNG ELECTRONICS
CHECK	K.Y.Kim	DEV. STEP	ADV1		
APPROVAL	H.K.Park	REV	1.1		
			PART NO.		
MODULE CODE		LAST EDIT		October 10, 2009 16:50:44 PM	PAGE 30 OF 61

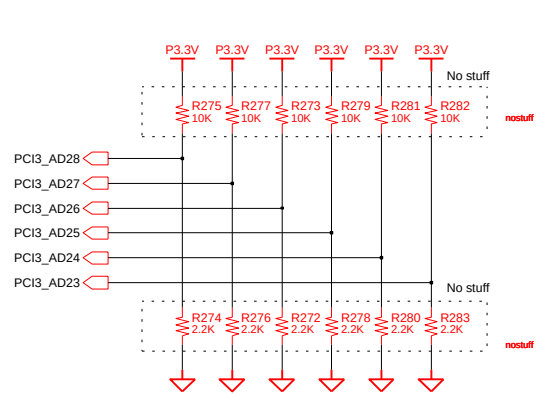
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DRAW	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D
CHECK	K.Y.Kim	DEV. STEP	ADV1		ICH
APPROVAL	H.K.Park	REV	1.1		SB710 (4/5)
MODULE CODE	undefined	LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	31 OF 61

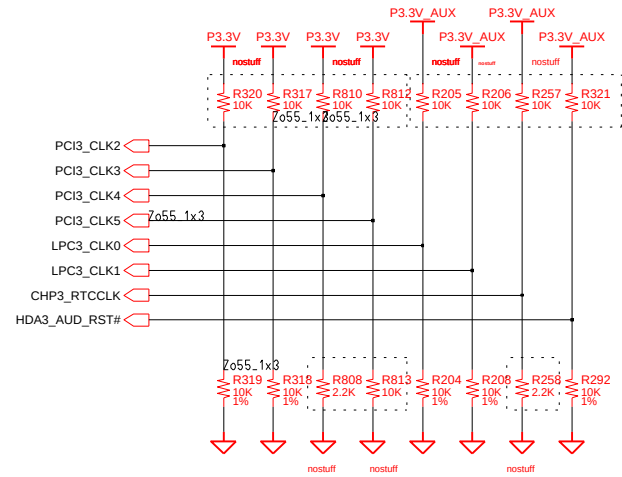
SAMSUNG ELECTRONICS	
PART NO.	BA41-xxxxxA

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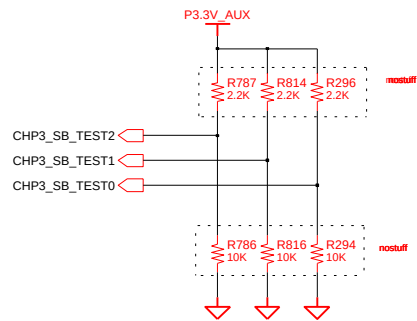


DEBUG STRAPS

	PCI3_AD(28)	PCI3_AD(27)	PCI3_AD(26)	PCI3_AD(25)	PCI3_AD(24)	PCI3_AD(23)
STRAP HIGH	USE LONG RESET	USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS	BOOTFAILTIMER DISABLED
STRAP LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED



	PCI3_CLK2	PCI3_CLK3	PCI3_CLK4	PCI3_CLK5	LPC3_CLK0	LPC3_CLK1	RTC_CLK	AUD_RST#
STRAP HIGH	BOOTFAIL TIMER ENABLED	USER DEBUG STRAPS	RESERVED	RESERVED	EC ENABLED	CLKGEN ENABLED	INTERNAL RTC	ENABLE PCI MEM BOOT
STRAP LOW	BOOTFAIL TIMER DISABLED	IGNORE DEBUG STRAPS	RESERVED	RESERVED	EC DISABLED	CLKGEN DISABLED	EXRERNAL RTC (PD on X1, Apply 32KHz to RTC_CLK)	DISABLE PCI MEM BOOT

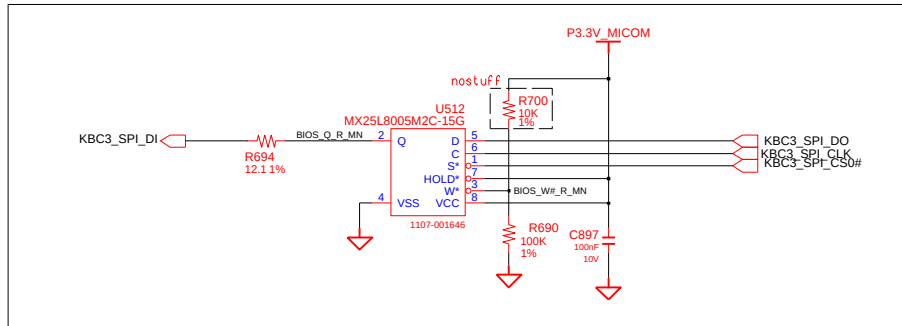


Remove SB_TEST pins for mass production. (For ASIC debug only - AMD)

DRAW	H.J.Ra	DATE	9/23/2008	TITLE Bremen-D ICH SB710 STRAPS (5/5)	SAMSUNG ELECTRONICS		
CHECK	K.Y.Kim	DEV. STEP	ADV1				
APPROVAL	H.K.Park	REV	1.1				
				PART NO.	BA41-XXXXXA		
MODULE CODE	LAST EDIT			October 10, 2009 16:50:44 PM	PAGE	32	OF 61

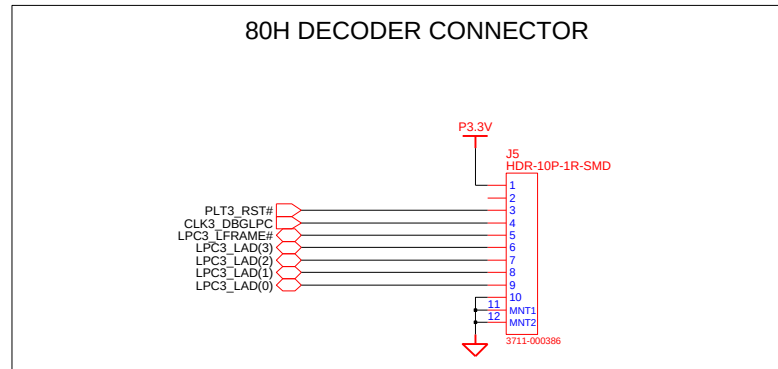
SPI_BIOS_ROM

8MBit

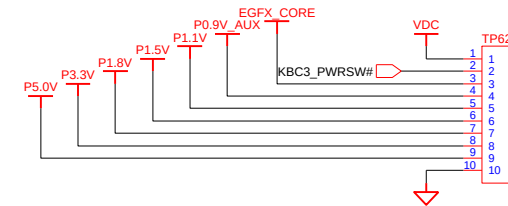


02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT. SYSTEM H/W	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU REG	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD ERROR
0C	INIT. CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
0E	INIT. I/O VALUE	7E	TEST COPROCESSOR IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGER	82	DETECT AND INSTALL EXT RS232C
11	LOAD ALTERNATE REG.	84	DETECT AND INSTALL EXT PARALLEL
13	PCI BUS MASTER RESET	86	RE-INIT. ON-BOARD I/O PORT
WITH INITIAL POST VALUE		88	INIT. BIOS DATA ROM
14	INIT. KEYBOARD CONTROLLER	8A	INIT. EXTENDED BIOS DATA AREA
16	CHECK CHECKSUM	8C	INIT. FDD CONTROLLER
18	8254 TIMER INIT	8E	SHADOW OPTION ROMS
1A	8237 DMA CONTROLLER INIT	9C	SETUP POWER MANAGEMENT
1C	RESET INTERRUPT CONTROLLER	9E	ENABLE H/W INTERRUPT
20	TEST DRAM REFRESH	A0	SET TIME OF DAY
22	TEST 8742 KEYBOARD CONTROLLER	A4	INIT. TYPEMATIC RATE
24	SET ES SEGMENT REG. TO 4GB	A8	ERASE F2 PROMPT
26	ENABLE A20	AA	SCAN FOR F2 KEY STROKE
28	AUTO SIZING DRAM	AC	ENTER SETUP
32	COMPUTE THE CPU SPEED	AE	CLEAR IN POST FLAG
34	TEST CMOS RAM	B0	CHECK FOR ERRORS
38	SHADOW SYSTEM BIOS ROM	B2	POST DONE-PREPARE TO BOOT O/S
3A	AUTO SIZING CACHE	B4	ONE BEEP
3C	CONFIGURE ADVANCED CHIPSET REG.	B6	CHECK PASSWORD (OPTION)
3D	LOAD ALTER REG. WITH CMOS VALUE	B7	ACPI INIT
42	INIT. BIOS INTERRUPT	BA	DMI INIT
44	INIT. BIOS INTERRUPT	BE	CLEAR SCREEN
46	CHECK ROM COPYRIGHT NOTICE	C0	TRY BOOT WITH INT19
47	INIT. I20 SUPPORT IF INSTALLED	D0	INTERRUPT HANDLER ERROR
48	CHECK VIDEO CONFIGURE AGAINST CMOS	D2	UNKNOWN INTERRUPT ERROR
49	INIT. PCI BUS AND DEVICE	D4	PENDING INTERRUPT ERROR
4A	INIT. ALL VIDEO BIOS ROM	D6	SHUTDOWN 5
4C	SHADOW VIDEO BIOS ROM	D8	SHUTDOWN ERROR
50	DISPLAY CPU TYPE AND SPEED	DA	EXTENDED BLOCK MOVE
52	TEST KEYBOARD	DC	SHUTDOWN 10
54	SET KEYCLICK IF ENABLED	D9	ENABLE NMI
56	ENABLE KEYBOARD	90	INIT. HDD CONTROLLER
58	TEST FOR UNEXPECTED INTERRUPTS	91	INIT. LOCAL BUS HDD CONTROLLER
5A	DISPLAY "PRESS SETUP"	92	JUMP TO USER PATCH 2
5C	TEST RAM BETWEEN 512K AND 640K	94	DISABLE A20 ADDRESS LINE
60	TEST EXTENDED MEMORY	96	CLEAR HUGE ES SEGMENT REG.
62	TEST EXTENDED MEMORY ADDRESS LINE	98	SEARCH FOR OPTION ROMS
64	JUMP TO USER PATCH 1		

80H DECODER CONNECTOR



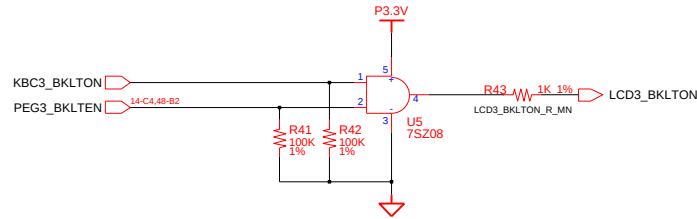
Pins for ICT FREE
should be rearranged.



DRAW	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D	SAMSUNG
CHECK	K.Y.Kim	DEV. STEP	ADV1		SPI_BIOS_ROM	ELECTRONICS
APPROVAL	H.K.Park	REV	1.1		SPI_BIOS_ROM	PART NO.
MODULE CODE		LAST EDIT				BA41-xxxxxA
				October 10, 2009 16:50:44 PM	PAGE	33 OF 61

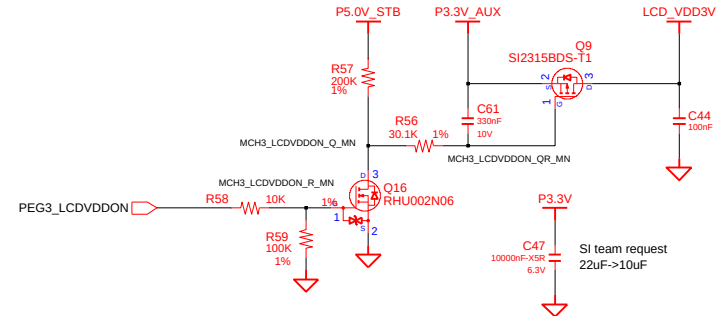
LVDS

Backlight On

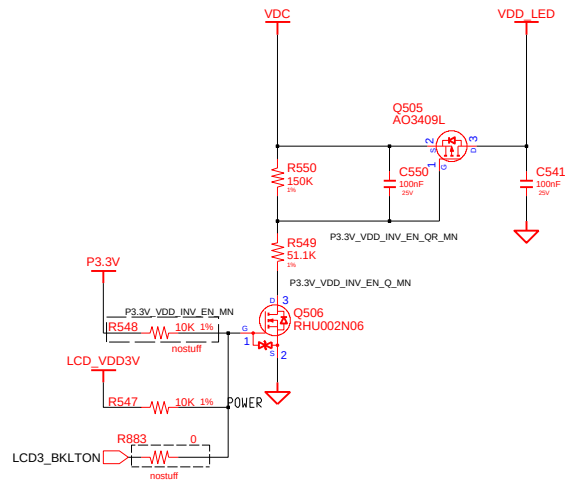


LCD Power

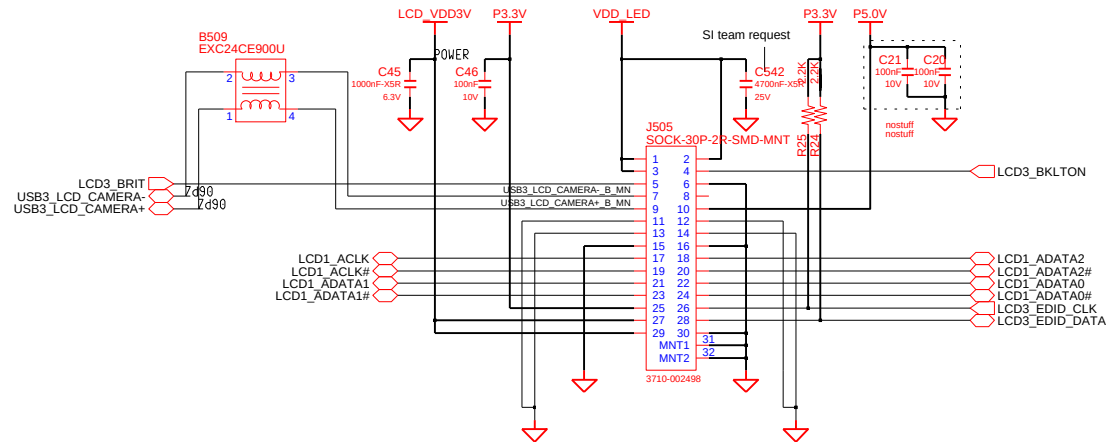
EBL Purpose



LED Power



Camera + LCD Connector



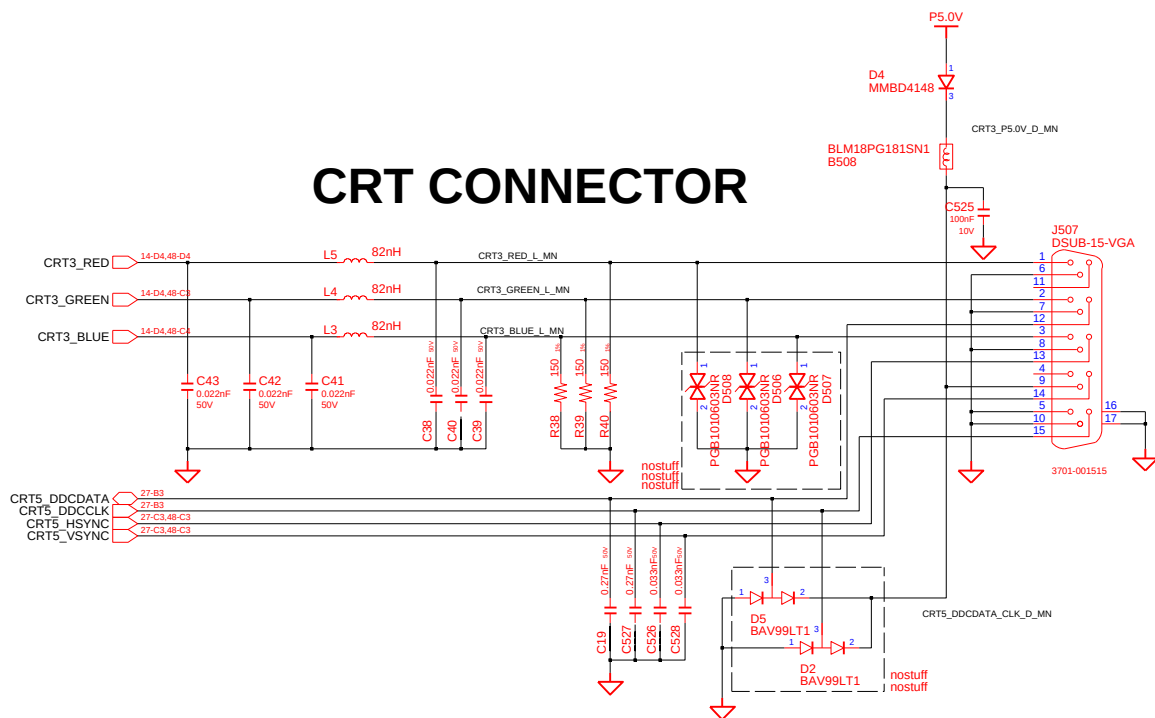
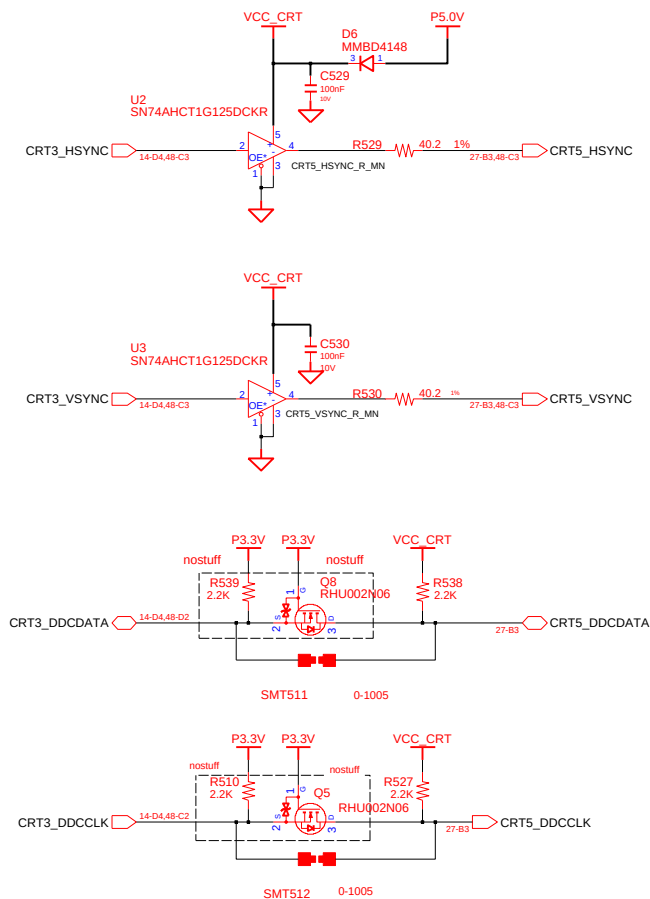
DESIGN	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D	SAMSUNG
CHECK	K.Y.Kim	DEV. STEP	ADV1	GRAPHICS_IF	ELECTRONICS	
APPROVAL	H.K.Park	REV	1.1	LVDS	PART NO.	BA41-xxxxxA
MODULE CODE		LAST EDIT		October 10, 2009 16:50:44 PM	PAGE	34 OF 61

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CRT

CRT CONNECTOR



Check "CRT3_DDCCCLK/DATA" Voltage Level
2N06 Can be replaced with SM6K2

DESIGN	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D
CHECK	K.Y.Kim	DEV. STEP	ADV1	GRAPHICS_IF	
APPROVAL	H.K.Park	REV	1.1	CRT	
MODULE CODE		LAST EDIT			

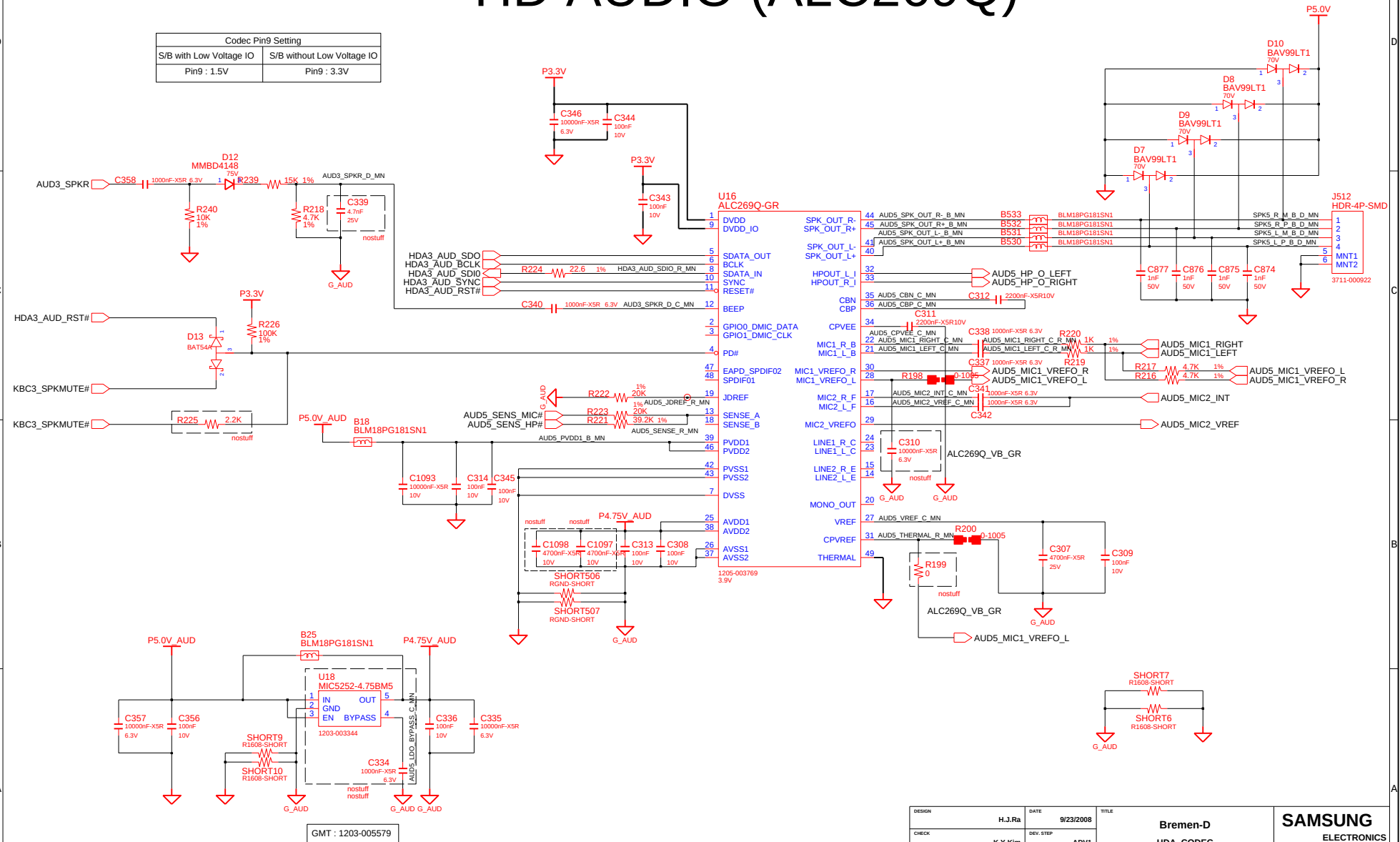
SAMSUNG
ELECTRONICS
PART NO.
BA41-xxxxxA

October 10, 2009 16:50:44 PM PAGE 35 OF 61

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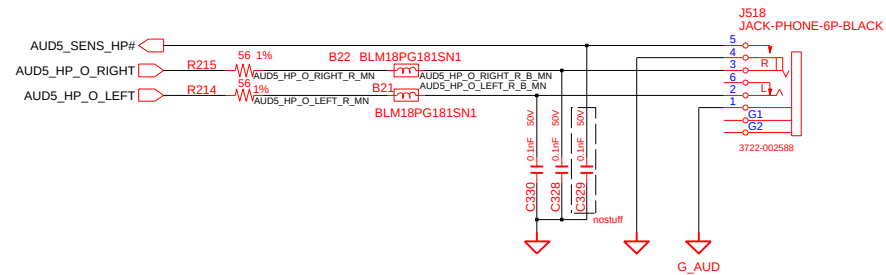
HD AUDIO (ALC269Q)

Codec Pin9 Setting	
S/B with Low Voltage IO	S/B without Low Voltage IO
Pin9 : 1.5V	Pin9 : 3.3V

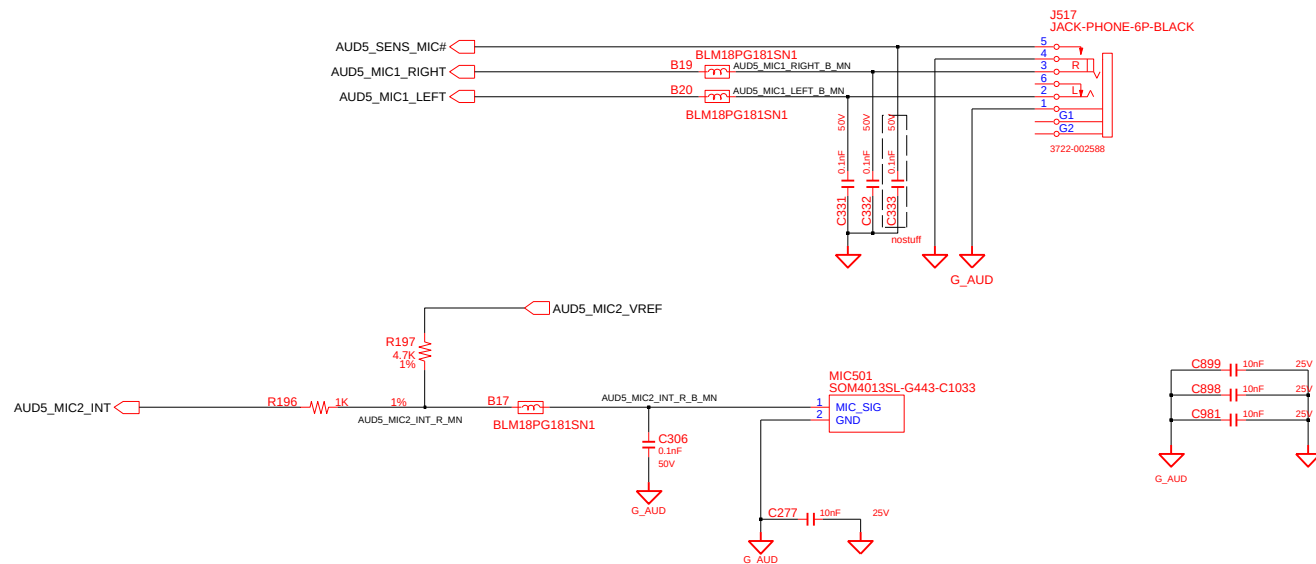


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HEADPHONE(BLACK)



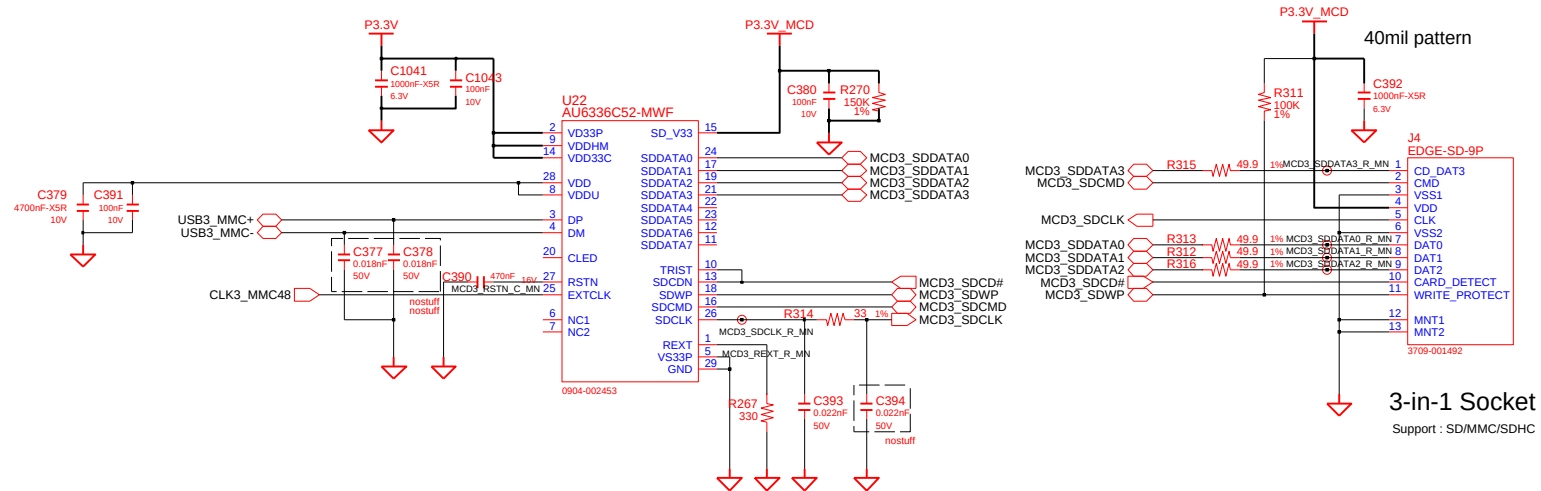
MIC JACK(BLACK)



DESIGN	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D	SAMSUNG
CHECK	K.Y.Kim	DEV. STEP	ADV1	HDA_CODEC	ELECTRONICS	
APPROVAL	H.K.Park	REV	1.1	AUDIO INPUT/OUTPUT	PART NO.	BA41-xxxxxA
MODULE CODE		LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	38	OF 61

D:/users/mobile58/mentor/Bremen-D/Bremen-D Sub

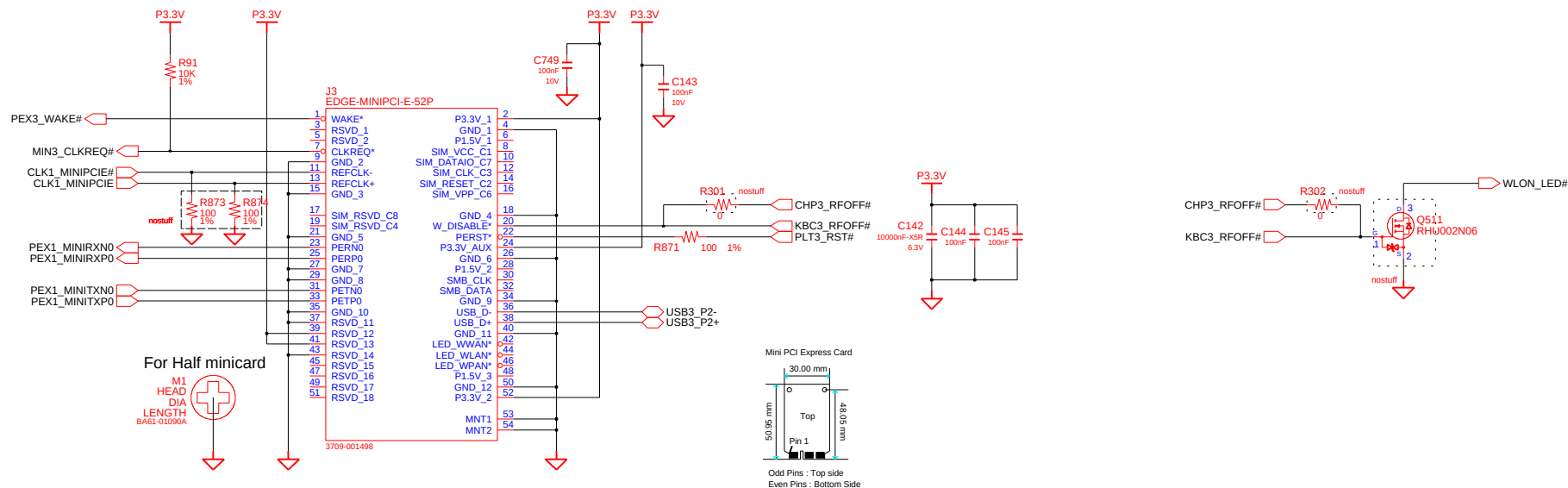
3 IN 1 CARD (AU6336)



DESIGN	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D MULTICARD 3 IN 1 CARD	SAMSUNG ELECTRONICS
CHECK	K.Y.Kim	DEV. STEP	ADV1			PART NO. BA41-xxxxxA
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE		LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	40	OF 61

Wireless LAN

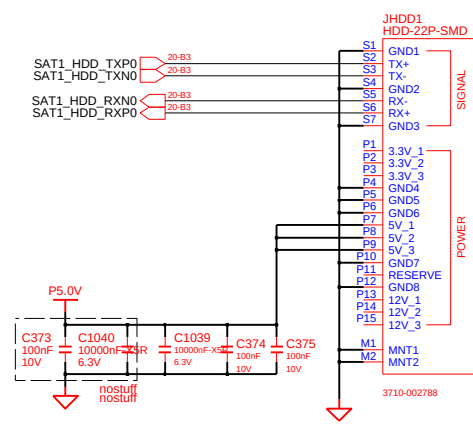
WLAN, 4mm



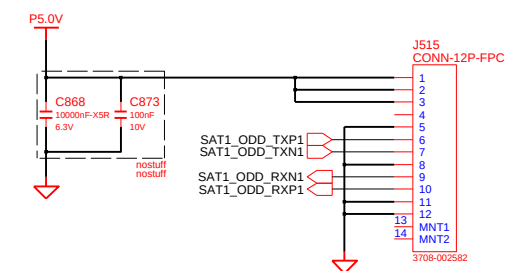
DESIGN	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D MINI_PCIE_CONN WLAN	SAMSUNG ELECTRONICS
CHECK	K.Y.Kim	DEV. STEP	ADV1			PART NO. BA41-xxxxxA
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE		LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	41	OF 61

SATA I/F CONN

SATA HDD CONN

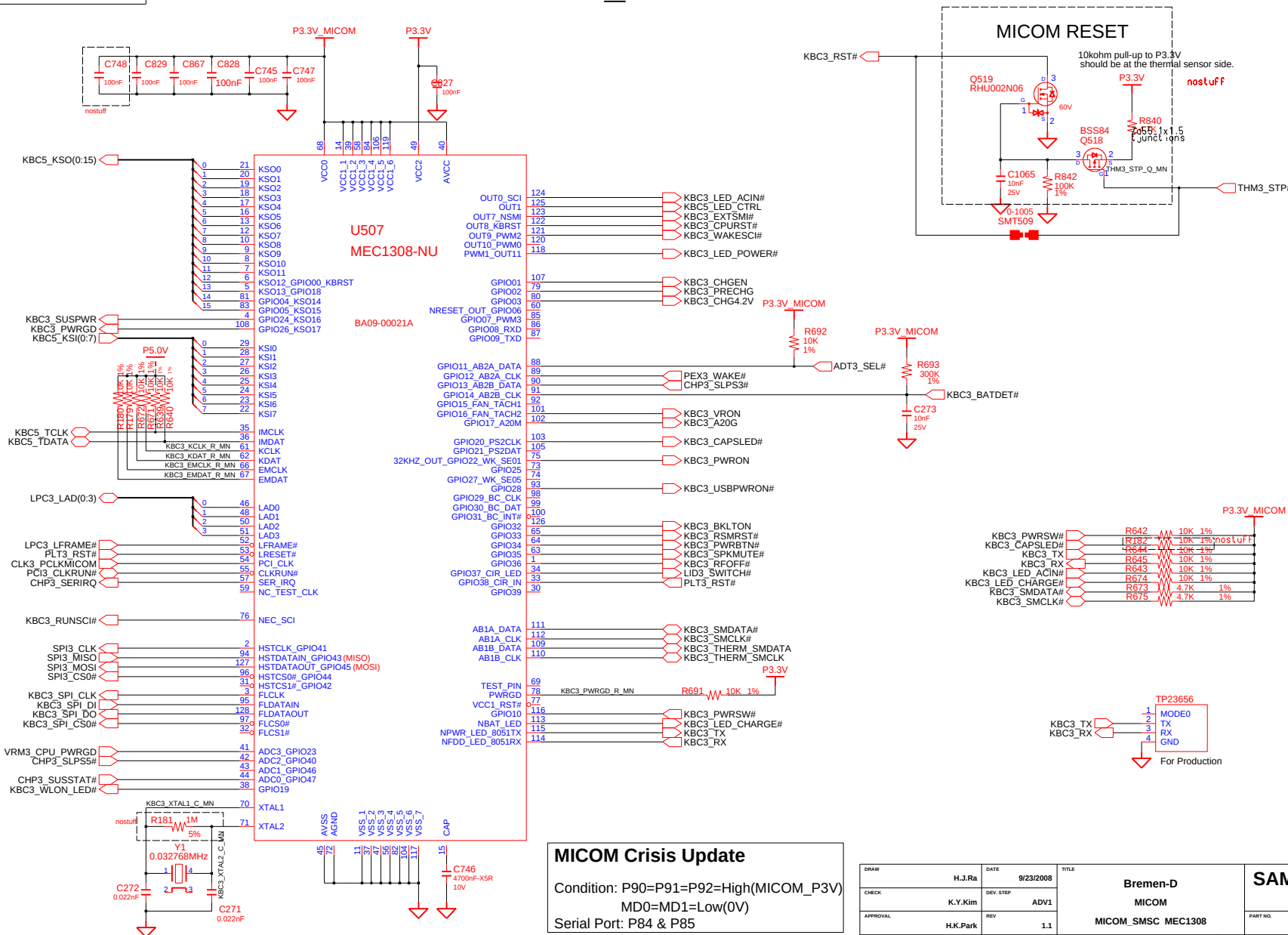


MAIN TO SUB SATA ODD CONN



DESIGN	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D	SAMSUNG
CHECK	K.Y.Kim	DEV. STEP	ADV1	SATA_DEVICES	SATA_DEVICES	ELECTRONICS
APPROVAL	H.K.Park	REV	1.1	HDD & ODD SUB CONNECTOR	PART NO.	BA41-xxxxxA
MODULE CODE	October 10, 2009 16:50:44 PM				PAGE	42 OF 61

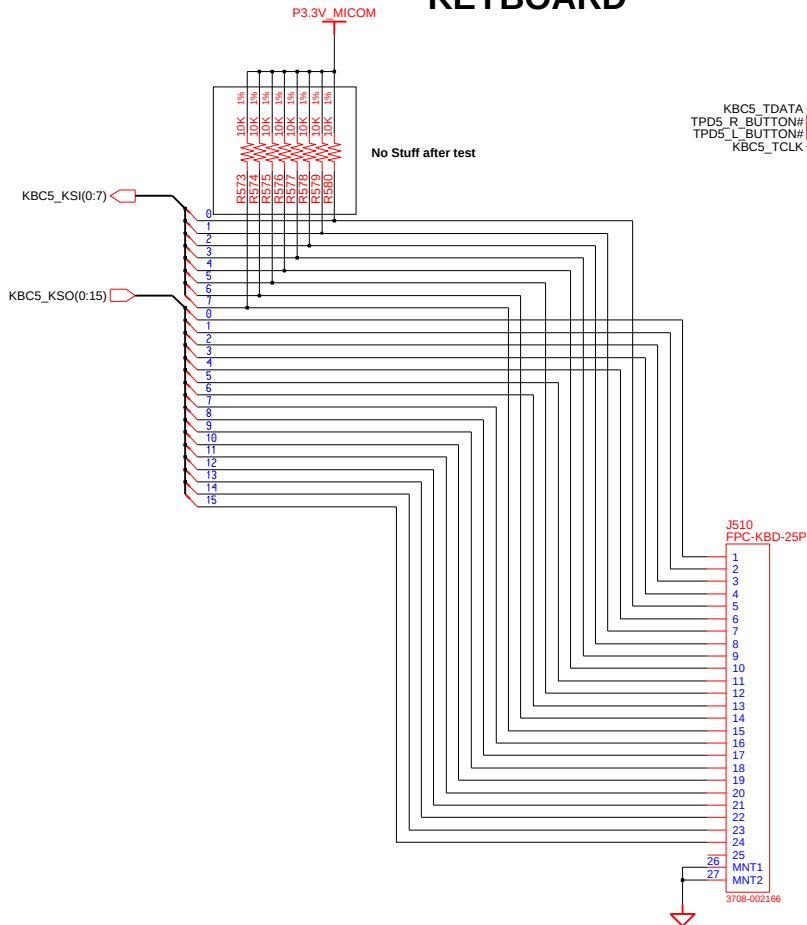
MICOM_MEC1308



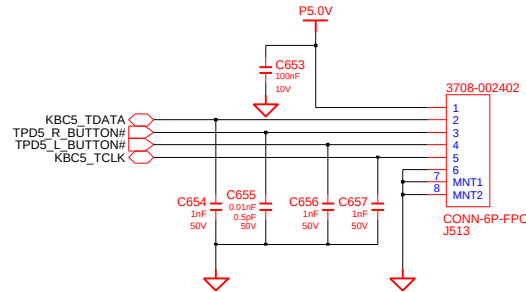
DRAW	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D	SAMSUNG
CHECK	K.Y.Kim	DEV. STEP	ADV1		MICOM	ELECTRONICS
APPROVAL	H.K.Park	REV	1.1		MICOM_SMSC MEC1308	PART NO.
MODULE CODE		LAST EDIT				BA41-xxxxxA
				October 10, 2009 16:50:44 PM	PAGE	43 OF 61

Micom Glue Logic

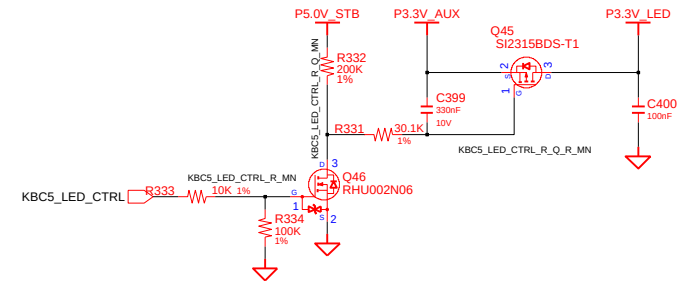
KEYBOARD



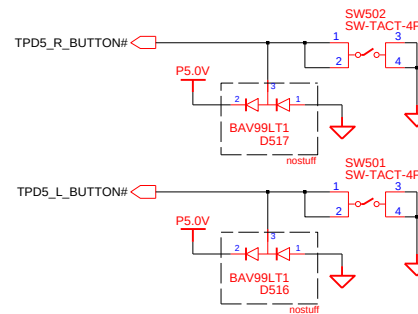
TOUCHPAD



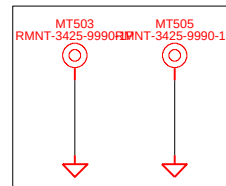
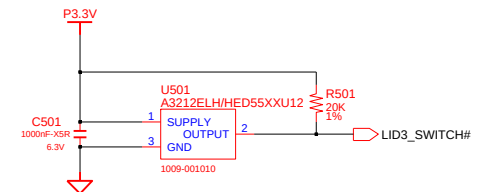
TOUCHPAD LED



TOUCHPAD BUTTON



LID SWITCH

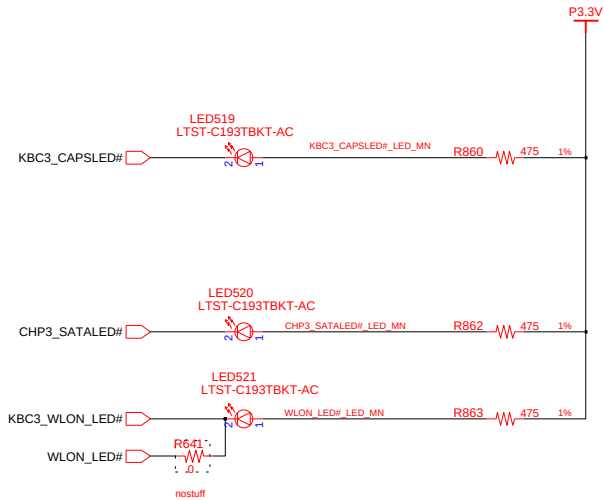


Keyboard Mount(for 15")

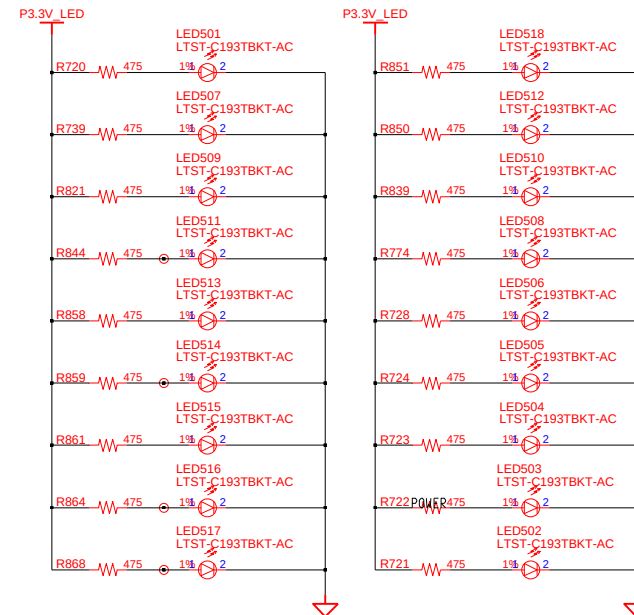
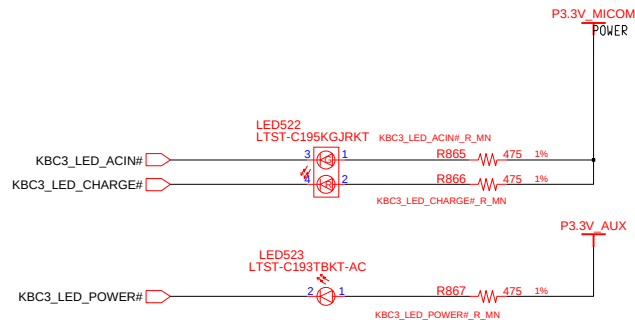
DESIGN	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D MICOM GLUE LOGIC KEYBOARD & TOUCHPAD	SAMSUNG ELECTRONICS
CHECK	K.Y.Kim	DEV. STEP	ADV1			PART NO. BA41-xxxxxA
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE		LAST EDIT		October 10, 2009 16:50:44 PM	PAGE 44 OF 61	

LEDs

FUNCTION KEY LED

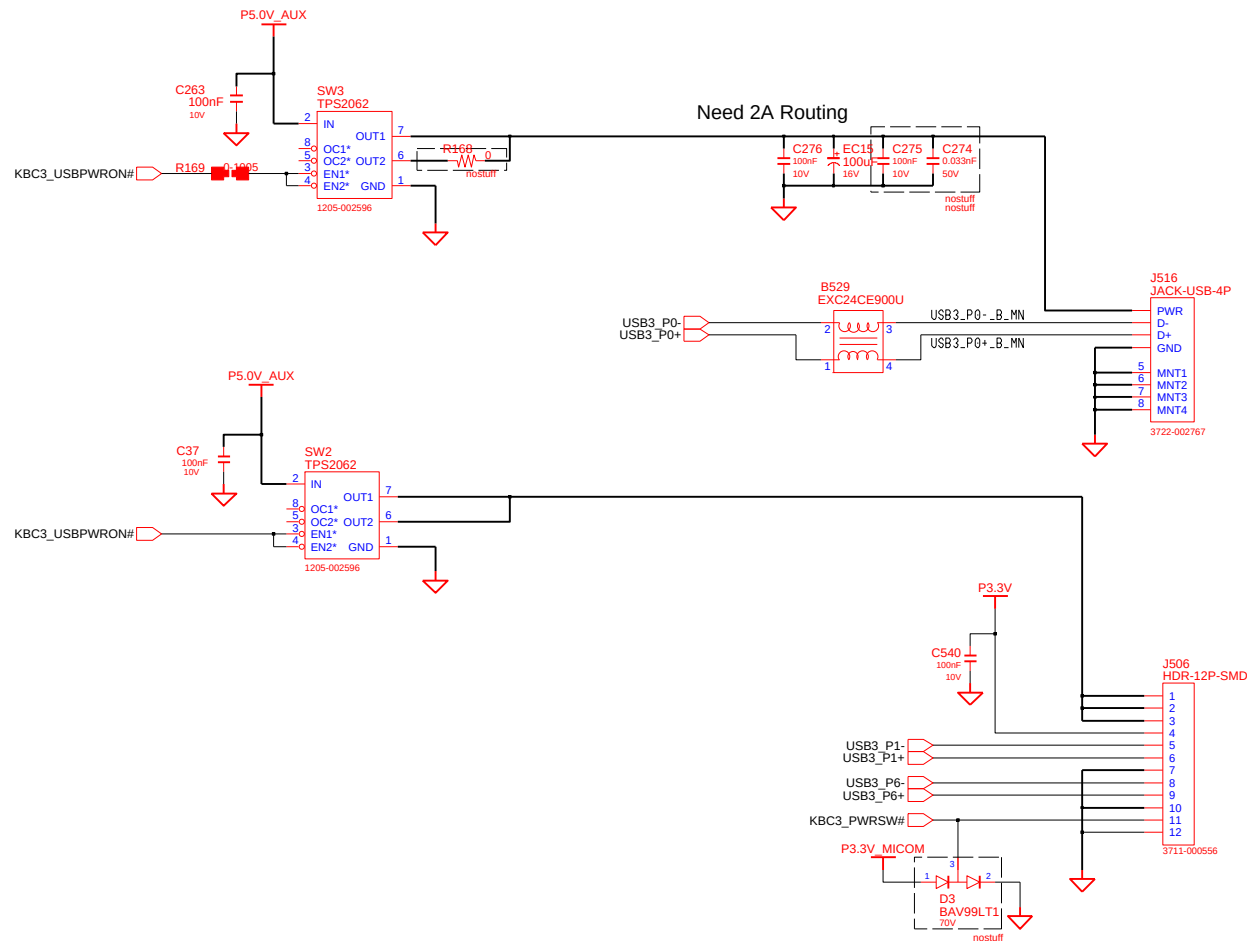


ADAPTERIN/CHARGING LED



DRAW	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D	SAMSUNG
CHECK	K.Y.Kim	DEV. STEP	ADV1	LED_SWITCH	LED_SWITCH	ELECTRONICS
APPROVAL	H.K.Park	REV	1.1	LED_SWITCH		PART NO.
MODULE CODE		LAST EDIT	October 10, 2009 16:50:44 PM			BA41-xxxxxA
				PAGE	45	OF 61

USB Single connector

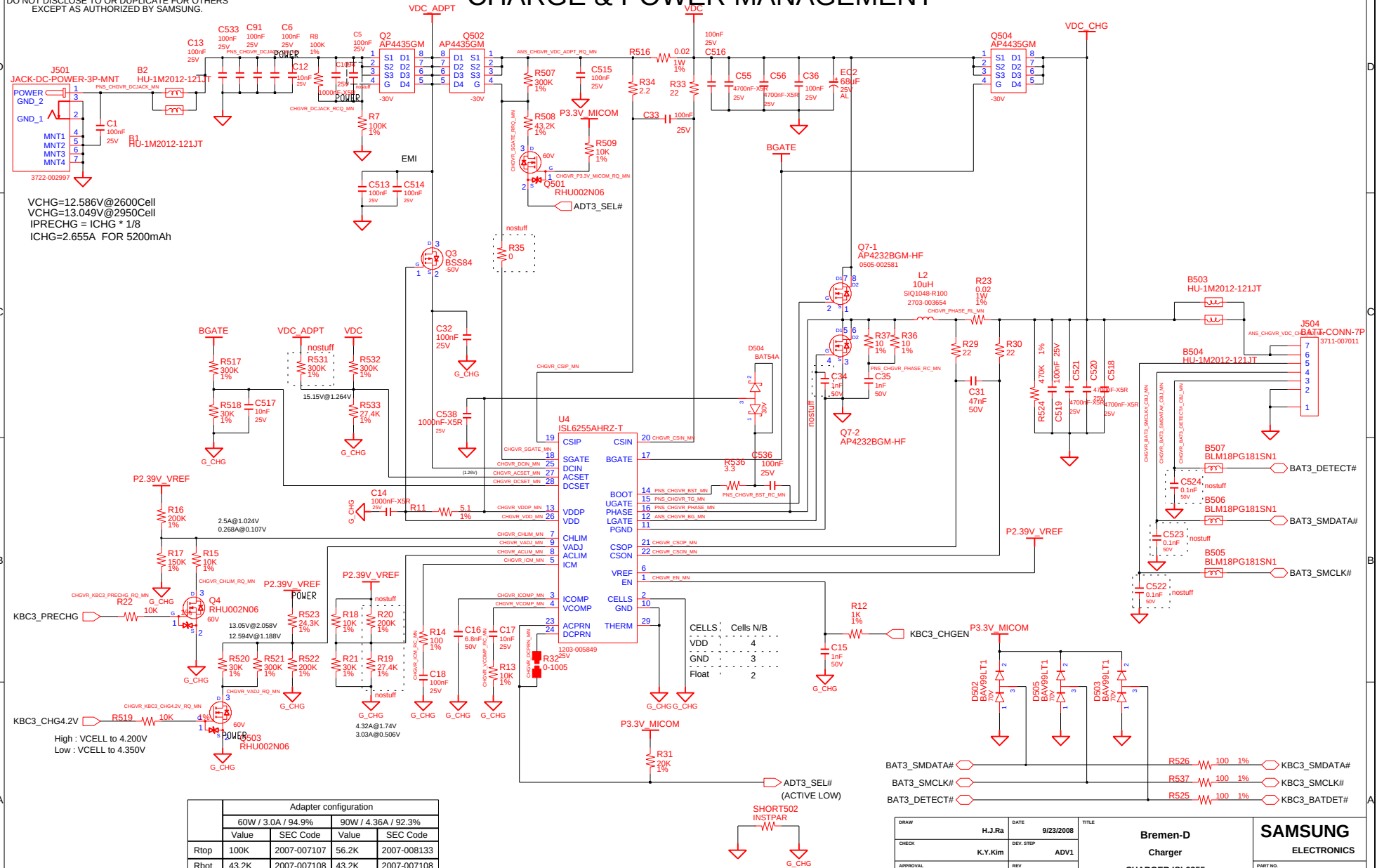


DESIGN	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D	SAMSUNG ELECTRONICS
CHECK	K.Y.Kim	DEV. STEP	ADV1	USB_CONN		
APPROVAL	H.K.Park	REV	1.1	USB		
MODULE CODE		LAST EDIT		October 10, 2009 16:50:44 PM	PAGE 46 OF 61	PART NO. BA41-xxxxxA

A

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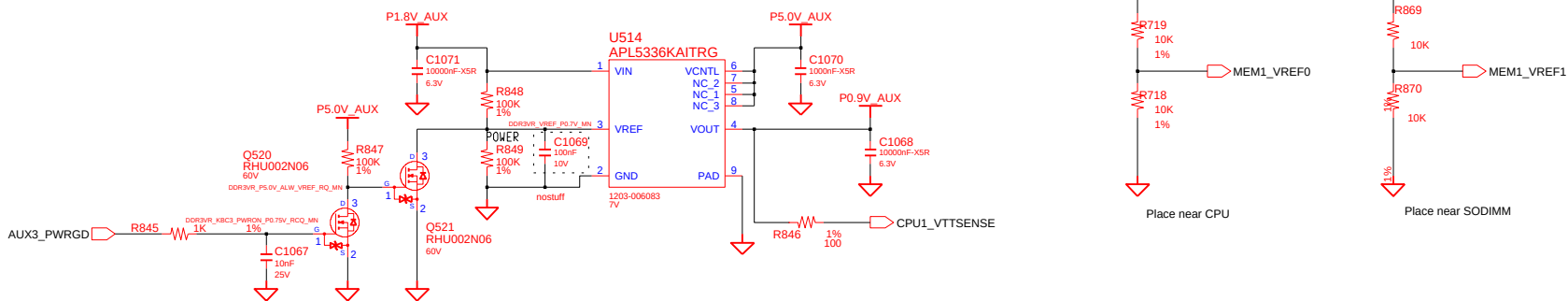
CHARGE & POWER MANAGEMENT



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[illegible]

DDR2 VTT(0.9V_AUX)

D:/users/mobile58/mentor/Bremen-D/Bremen-D_Sub

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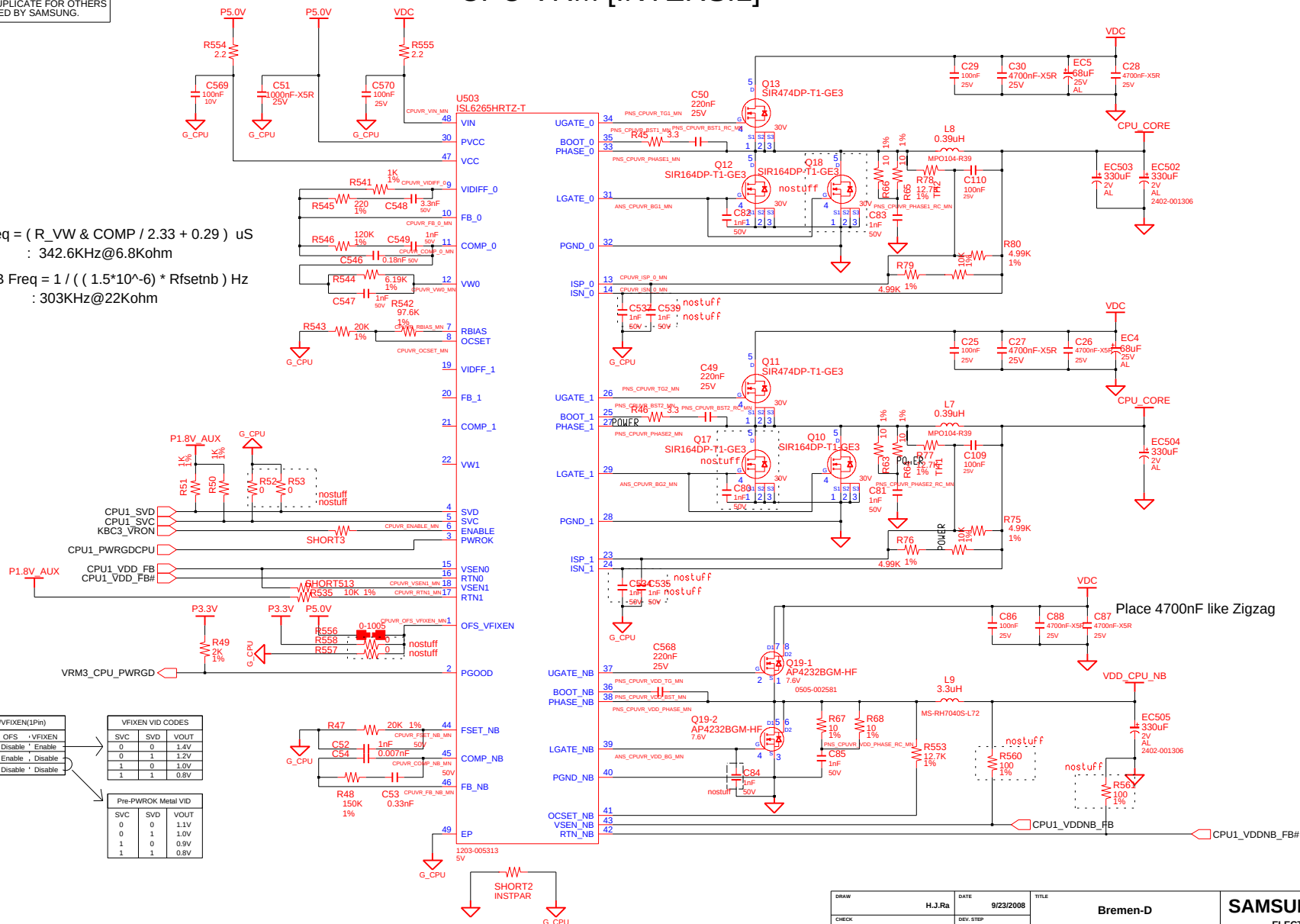
CPU VRM [INTERSIL]

VDD Freq = (R_VW & COMP / 2.33 + 0.29) uS
: 342.6KHz@6.8Kohm

VDD_NB Freq = 1 / ((1.5*10^-6) * Rfsetnb) Hz
: 303KHz@22Kohm

OFS/VFIXEN(1Pin)		VFIXEN VID CODES		
OFS	VFIXEN	SVC	SVD	VOUT
3.3V	Disable	0	0	1.4V
GND	Enable	0	1	1.2V
5V	Disable	1	0	1.0V
	Enable	1	1	0.8V

Pre-PWROK Metal VID		
SVC	SVD	VOUT
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

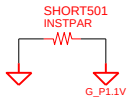


DRAW	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D
CHECK	K.Y.Kim	DEV. STEP	ADV1		PWR CPU MV ISL6265HRT
APPROVAL	H.K.Park	REV	1.1		CPU VRM
MODULE CODE	undefined	LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	51 OF 61

SAMSUNG
ELECTRONICS
PART NO.
BA41-xxxxxA

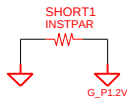
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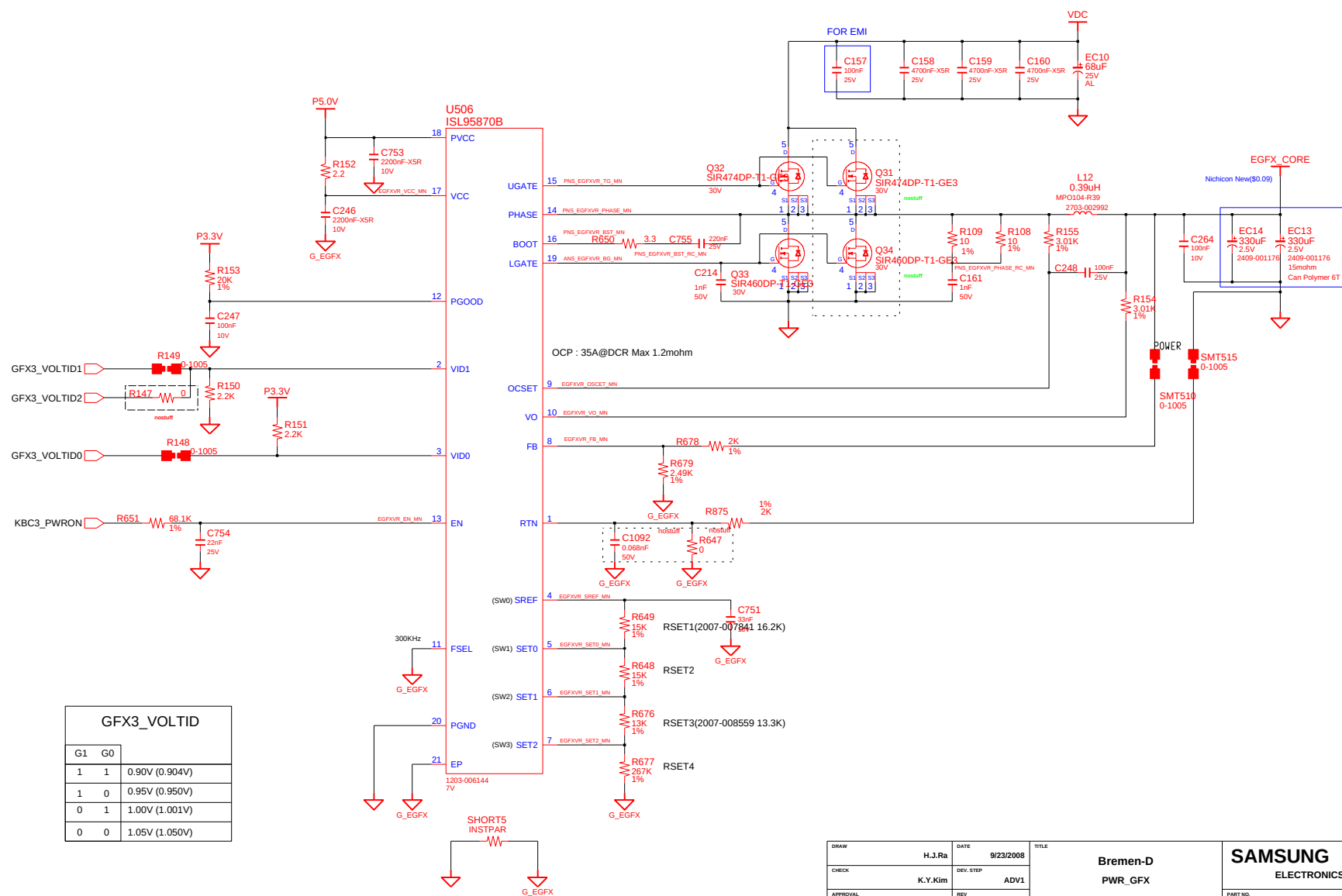


D:/users/mobile58/mentor/Bremen-D/Bremen-D_Sub

1

D:/users/mobile58/mentor/Bremen-D/Bremen-D_Sub

Graphic Core Power

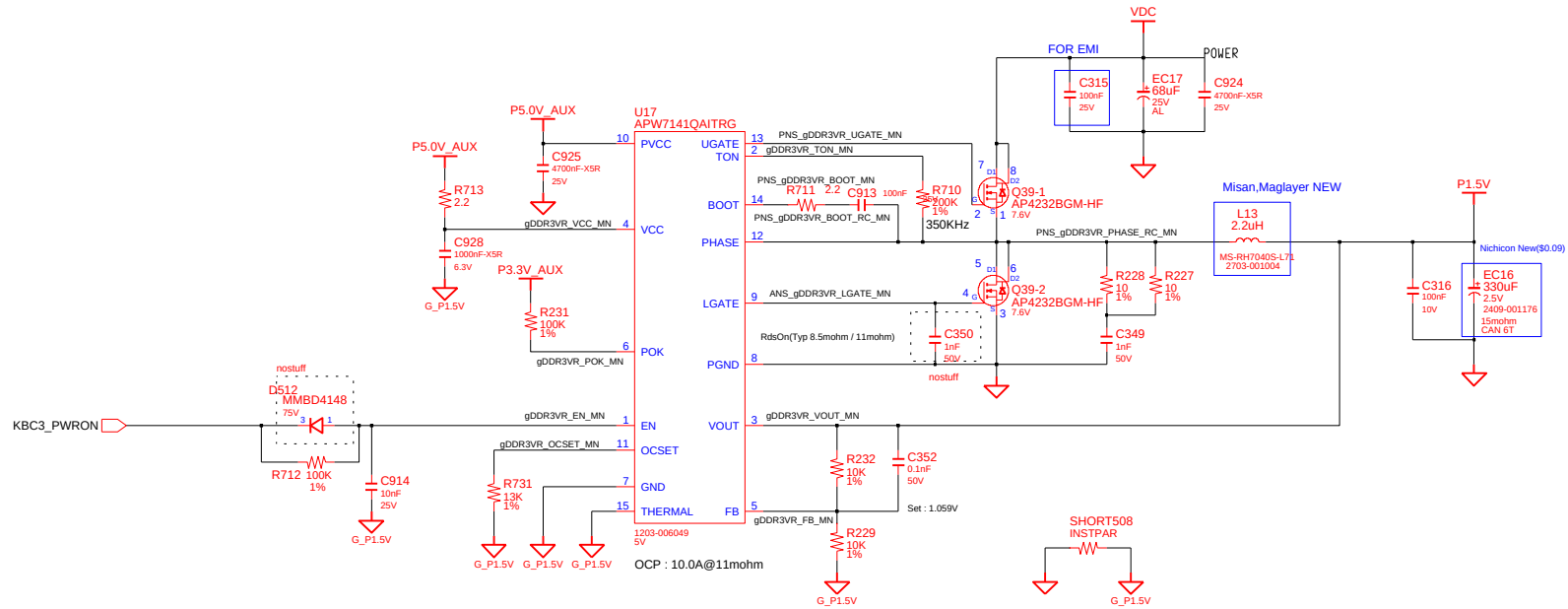


GFX3_VOLTID		
G1	G0	
1	1	0.90V (0.904V)
1	0	0.95V (0.950V)
0	1	1.00V (1.001V)
0	0	1.05V (1.050V)

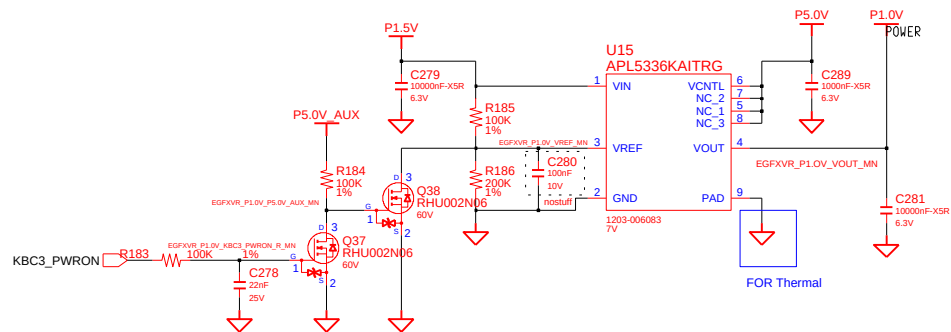
DRAW	H.J.Ra	DATE	9/23/2008	Bremen-D PWR GFX GFX POWER	SAMSUNG ELECTRONICS
CHECK	K.Y.Kim	DEV. STEP	ADV1		
APPROVAL	H.K.Park	REV	1.1		
MODULE CODE	LAST EDIT			October 10, 2009 16:50:44 PM	PART NO. BA41-XXXXXA
				PAGE 54	OF 61

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gDDR3 POWER(P1.5V)



P1.0V



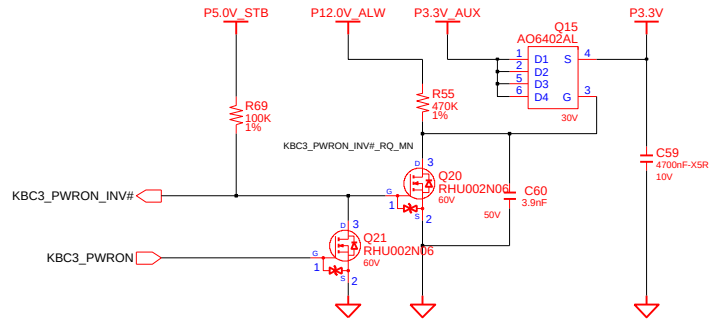
DRAW	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D
CHECK	K.Y.Kim	DEV. STEP	ADV1		PWR GFX MEMORY
APPROVAL	H.K.Park	REV	1.1		gDDR3 POWER
MODULE CODE	undefined	LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	55 OF 61

SAMSUNG	ELECTRONICS
PART NO.	BA41-xxxxxA

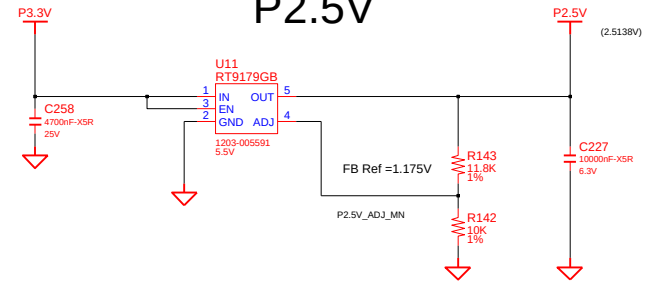
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Switched Power

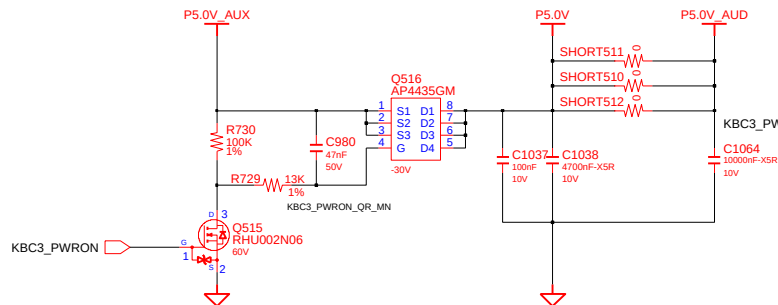
Switched Power On (P3.3V)



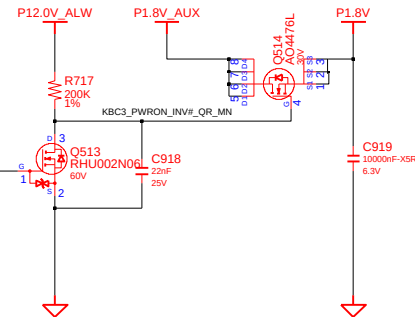
P2.5V



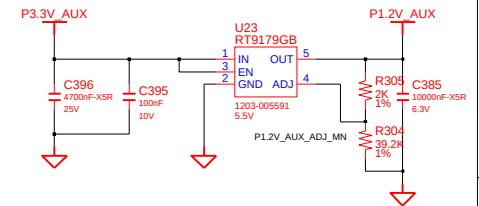
Switched Power On (P5.0V)



Switched Power On (P1.8V)



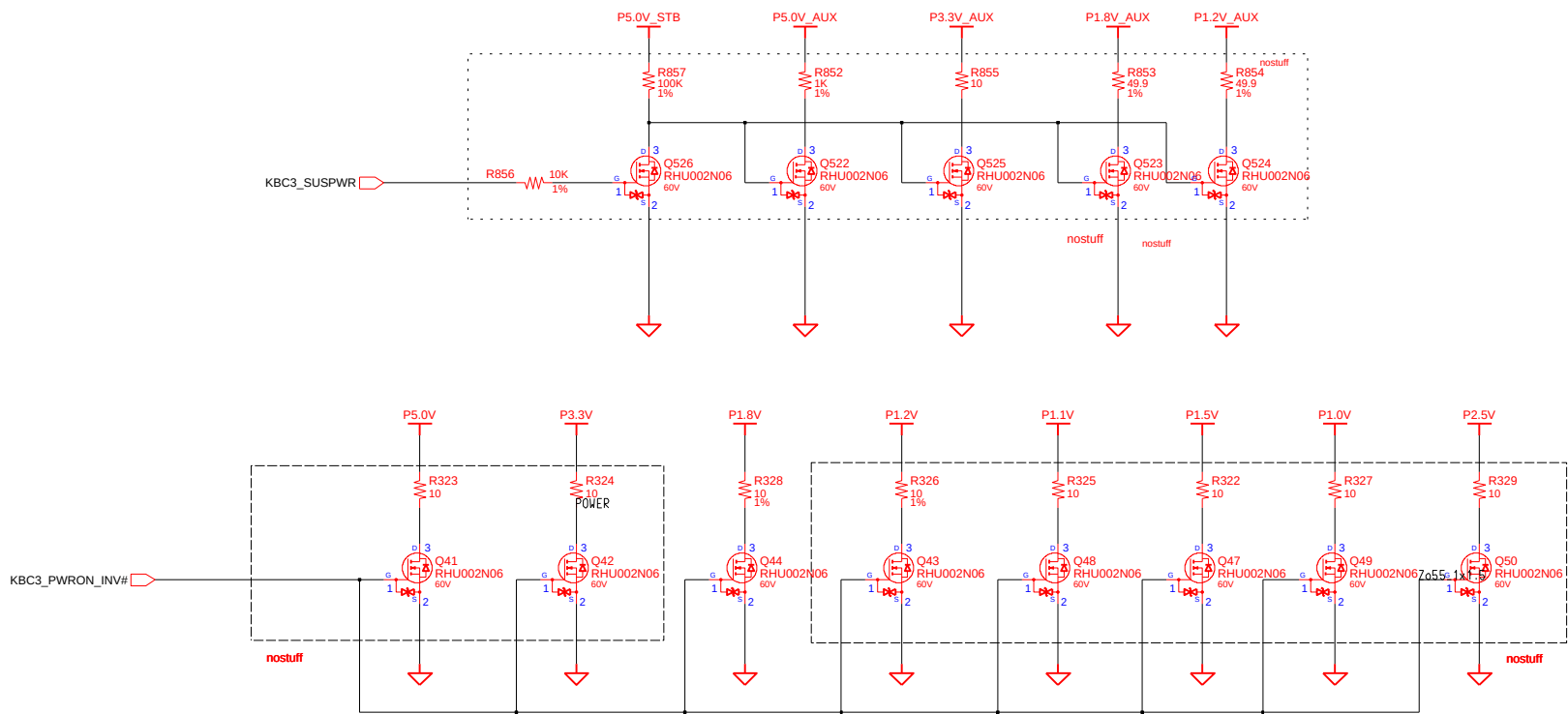
P1.2V_AUX



DESIGN	H.J.Ro	DATE	8/22/2009	TITLE	Bremen-D PWR_MV_SWITCHED SWITCHED POWER	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxA
CHECK	K.Y.Kim	DEV. STEP	ADV1			
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE		LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	56 OF 61	

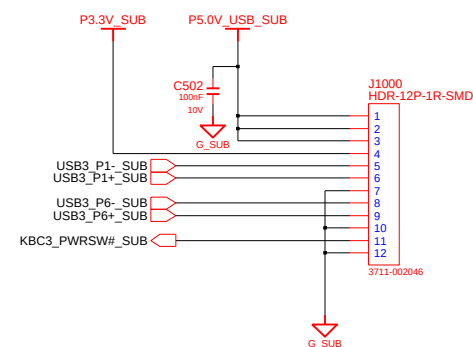
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POWER DISCHARGER

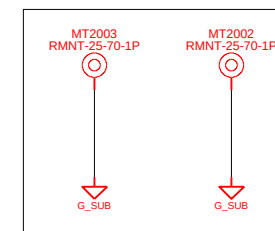


DRAW	H.J.Ra	DATE	9/23/2008	Bremen-D PWR_MV_DISCHARGER DISCHARGER LOGIC		SAMSUNG ELECTRONICS	
CHECK	K.Y.Kim	DEV. STEP	ADV1				
APPROVAL	H.K.Park	REV	1.1				
				PART NO.		BA41-xxxxxA	
MODULE CODE		LAST EDIT		October 10, 2009 16:50:44 PM		PAGE	57 OF 61

2 USB PORT & POWER S/W SUB B'D



Power ON LED

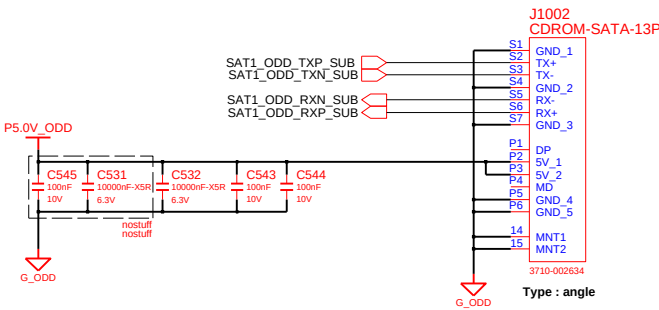


USB sub board mount hole

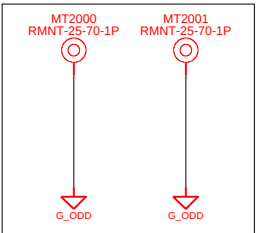
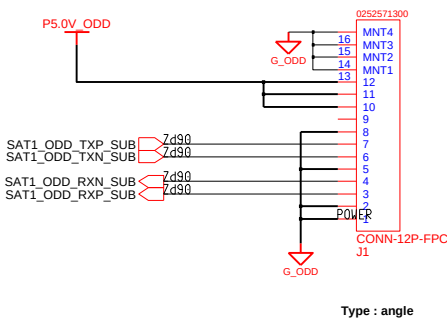
D:/users/mobile58/mentor/Bremen-D/Bremen-D Sub

SATA ODD SUBBOARD

SATA ODD CONN



SUB TO MAIN SATA ODD CONN



ODD sub board mount hole

DRAW	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D SUB BOARD2 SATA ODD SUB BOARD	SAMSUNG ELECTRONICS
CHECK	K.Y.Kim	DEV. STEP	ADV1			PART NO. BA41-xxxxxA
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE	undefined	LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	59	OF 61

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The diagram illustrates 10 connections between various MT (Master Terminal) units. The connections are organized into two rows of five. Each connection is represented by a vertical line with a red circle at the top and a red triangle at the bottom. The labels for each connection are as follows:

- Top Row:
 - MT2006 RMNT-25-70-1P
 - MT509 RMNT-30-90-1P
 - MT502 RMNT-30-90-1P
 - MT510 RMNT-30-90-1P
 - MT506 RMNT-30-90-1P
- Bottom Row:
 - MT504 RMNT-30-90-1P
 - MT501 RMNT-30-90-1P
 - MT508 RMNT-30-90-1P
 - MT511 RMNT-30-90-1P
 - MT507 RMNT-30-90-1P

Diagram showing four callouts for dimensions M503, M502, M501, and M505. Each callout consists of a red circle with a crosshair, a vertical line with a downward-pointing arrow, and text specifying the dimension name and its tolerance.

- M503**
HEAD
DIA LENGTH
BA61-01090A
- M502**
DIA
LENGTH
BA61-01090A
- M501**
DIA
LENGTH
BA61-01090A
- M505**
HEAD
DIA
LENGTH
BA61-01090A

Diagram 1: VDC connected to C1073 (100nF, 25V) to ground.

Diagram 2: VDC connected to C1086 (100nF, 25V) to ground.

Diagram 3: VDC connected to C595 (100nF, 25V) to ground.

Diagram 4: VDC connected to C756 (100nF, 25V) to ground.

Diagram 5: VDC connected to C750 (100nF, 25V) to ground.

VDC

C1090
100nF
25V

VDC

C1091
100nF
25V

P5.0V

C1085
100nF
25V

P5.0V

C1087
100nF
25V

P5.0V

C912
100nF
25V

P5.0V

C401
100nF
25V

P5.0V_AUX

C1042
100nF
25V

P5.0V_AUX

C1072
100nF
25V

P5.0V_AUX

C1088
100nF
25V

DRAW	H.J.Ra	DATE	9/23/2008	Bremen-D MAIN MOUNT HOLE	SAMSUNG ELECTRONICS	
CHECK	K.Y.Kim	DEV. STEP	ADV1			
APPROVAL	H.K.Park	REV	1.1		PART NO.	BA41-XXXXXA
MODULE CODE	LAST EDIT				October 10, 2009 16:50:44 PM	PAGE

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CPU1_LDTRDE#
CPU1_ALL_LD1STP
CPU1_LDTRST#
CPU1_LD1STP#
CPU1_PROCHOT#
CPU1_PWRGDCEP
CPU1_SIC
CPU1_SIO
CPU1_SVC
CPU1_SVO
CPU1_THMRTRIP#
CPU1_VDDIO_FB
CPU1_VDDIO_FB#
CPU1_VDDNB_FB
CPU1_VDDNB_FB#
CPU1_VDD_FB
CPU1_VDD_FB#
CPU1_VTSENSE
CPUVR_COMP_0_MN
CPUVR_COMP_NB_MN
CPUVR_ENABLE_MN
CPUVR_FB_0_MN
CPUVR_FB_NB_MN
CPUVR_FSET_NB_MN
CPUVR_ISP_0_MN
CPUVR_OCSET_MN
CPUVR_OFS_VF1XEN_MN
CPUVR_RBIAS_MN
CPUVR_RIM_MN
CPUVR_VIDIFF_0
CPUVR_VIN_MN
CPUVR_VSEN1_MN
CPUVR_VW0_MN
CPU_VDD0A1_B_MN
CRT3_BLUE
CRT3_BLUE_L_MN
CRT3_DDCCLK
CRT3_DDCDATA
CRT3_GREEN
CRT3_GREEN_L_MN
CRT3_HSYNC
CRT3_P5_OV_D_MN
CRT3_RED
CRT3_RED_L_MN
CRT3_VSYNC
CRT5_DDCCLK
CRT5_DDCDATA
CRT5_DDCDATA_CLK_D_MN
CRT5_HSYNC_R_MN
CRT5_HSYNC_R_MN
DDR3VR_P500D_MN
DDR3VR_KBC3_PWRON_0V_75V_RQ0_MN
DDR3VR_KBC3_SUSPWR_RD0_MN
DDR3VR_P5_OV_ALW_VREF_RQ0_MN
DDR3VR_PGOOD_MN
DDR3VR_TRIP_MN
DDR3VR_TRIP_MN
DDR3VR_VCC_MN
DDR3VR_VFB_MN
EGF_XVR_N0_MN
EGF_XVR_P1_MN
EGF_XVR_P1_OV_P5_OV_AUX_MN
EGF_XVR_P1_OV_VREF_MN
EGF_XVR_P1_OV_VOUT1_MN
EGF_XVR_SETO_MN
EGF_XVR_SE11_MN
EGF_XVR_SE12_MN
EGF_XVR_SREF_MN
EGF_XVR_VCC_MN
EGF_XVR_VO_MN
FAN3_FDBACK#
FANS_VDD
GDDR3VR_EN_MN
GDDR3VR_FB_MN
GDDR3VR_OCSET_MN
GDDR3VR_POK_MN
GDDR3VR_TON_MN
GDDR3VR_TOD_BR1
LC03_EDIO_CLK

KBC3.RPOFF#
KBC3.RSMRST#
KBC3.RST#
KBC3.RUNSCIN#
KBC3.SMCLK#
KBC3.SMDATA#
KBC3.SPT_CLK
KBC3.SPT_CSO#
KBC3.SPT_D1
KBC3.SPT_DO
KBC3.SPKMUTE#
KBC3.SUSPWR#
KBC3.THERM_SMCLK
KBC3.THERM_SMDATA#
KBC3.VBUSVRON#
KBC3.VRON
KBC3.WAKESCIN#
KBC3.WLON_LED#
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KBES.KS1(1)
KBES.KS1(2)
KBES.KS1(3)
KBES.KS1(4)
KBES.KS1(5)
KBES.KS1(6)
KBES.KS1(7)
KBES.KS0(0)
KBES.KS0(1)
KBES.KS0(10)
KBES.KS0(11)
KBES.KS0(12)
KBES.KS0(13)
KBES.KS0(14)
KBES.KS0(15)
KBES.KS0(2)
KBES.KS0(3)
KBES.KS0(4)
KBES.KS0(5)
KBES.KS0(6)
KBES.KS0(7)
KBES.KS0(8)
KBES.KS0(9)
KBES.LED_CTRL
KBES.LED_CTRL_R_MN
KBES.LED_CTRL_R_Q_MN
KBES.LED_CTRL_R_Q_R_MN
KBES.TDATA
LI03_SWITCH#
LP3C.CLK0
LP3C.CLK1
LP3C.LAD(0)
LP3C.LAD(1)
LP3C.LAD(2)
LP3C.LAD(3)
LP3C.RAME#
MCD3.SDCD0
MCD3.SDCLK
MCD3.SDCMD
MCD3.SDDATA0
MCD3.SDDATA1
MCD3.SDDATA2
MCD3.SDDATA3
MCD3.SDWP
MC43.EXITSQ#
MC43.EXITISQ#
MEMO.SAQ_R_MN
MEMO.SA1_R_MN
MEMO.CALRN1
NB.HPCALCN_R_MN
NB.OPIDF0D18_NC_R_MN
NB.KBC3.PWRGD_Q_MN
NB.PCE.CALRN_PCE_BCALRN_R_MN
NB.PCE.CALRP_PCE_BCALRP_R_MN
NB.STREQD00D_R_MN
NB.STREQD100D_R_MN
NB.TESTMODE_R_MN
NB.VDA18HTPL_L_B_MN
NB.VDA18PCEPLL_L_B_MN
P2_5V_ADJ_MN
P2_5V_ADJ_VMN

```

OSB_USB_RCOMP_R_MN
OSB_WAKE#_EVENT8#_R_MN
VRM3_CPU_PWRGD
SMB3_ALERT#
SMB3_CLK
SMB3_DATA
SP13_CLK
SP13_CS0#
SP13_MISO
SP13_MOSI
SYSVR_ENTRIP1_MN
SYSVR_ENTRIP2_MN
SYSVR_FB1_MN
SYSVR_FB2_MN
SYSVR_FSEL_PSEL_MN
SYSVR_TONSEL_MN
SYSVR_VIN_MN
THM3_ALERT#
THM3_STB#
THM3_SPDSQ_MN
TH_SHDN_SEL_R_MN
TH_TRIP_SET_R_MN
TH_VDD_3V_R_MN
TPD5_BUTTON#
TPD5_R_BUTTON#
T1_8V_VDD01
T1_8V_VDD01
BGATE
BGATE
CPU_CORE
CPU_CORE
C_AUD
C_AUD
C_AUD
C_CHG
VCC_CRT
VDC_ADPT
VDC_ADPT
VDC_CHG
VDC_CHG
VDD_CPU_NB
VDD_CPU_NB
C_CPU
C_CPU
C_DDR
C_DDR
C_DFX
C_GFX
C_P1_1V
C_P1_1V
C_P1_2V
C_P1_2V
C_P1_5V
C_P1_5V
C_P3_3V
C_P3_3V
LCD_VDD3V
LCD_VDD3V
PG_9V_AUX
PG_9V_AUX
P1_2V_AUX
P1_2V_AUX
P1_2V_AUX
P1_2V_AUX
P1_2V_LAN
P1_2V_LAN
P1_8V_A2VDD0
P1_8V_A2VDD0
P1_8V_AUX
P1_8V_AUX
P12_0V_ALW
P12_0V_ALW
P2_0V_REF
P2_33V_VREF
P2_33V_VREF
P2_5V
P2_5V
P2_5V_LAN
P2_5V_LAN
P3_3V_A2VDD
P3_3V_A2VDD
P3_3V_A2VDD

```

- ☐ P3_3V_AUX
- ☐ P3_3V_AUX
- ☐ P3_3V_LED
- ☐ P3_3V_MCD
- ☐ P3_3V_MCD
- ☐ P3_3V_MICOM
- ☐ P3_3V_MICOM
- ☐ P4_75V_AUD
- ☐ P4_75V_AUD
- ☐ P5_0V_AUD
- ☐ P5_0V_AUX
- ☐ P5_0V_AUX
- ☐ P5_0V_STB
- ☐ P5_0V_STB
- ☐ PRTC_BA1
- ☐ VCC_CR1
- ☐ VDD_LED