Cambridge

CPU : AMD s1g2
Chip Set : AMD RX781M + SB700
Remarks :

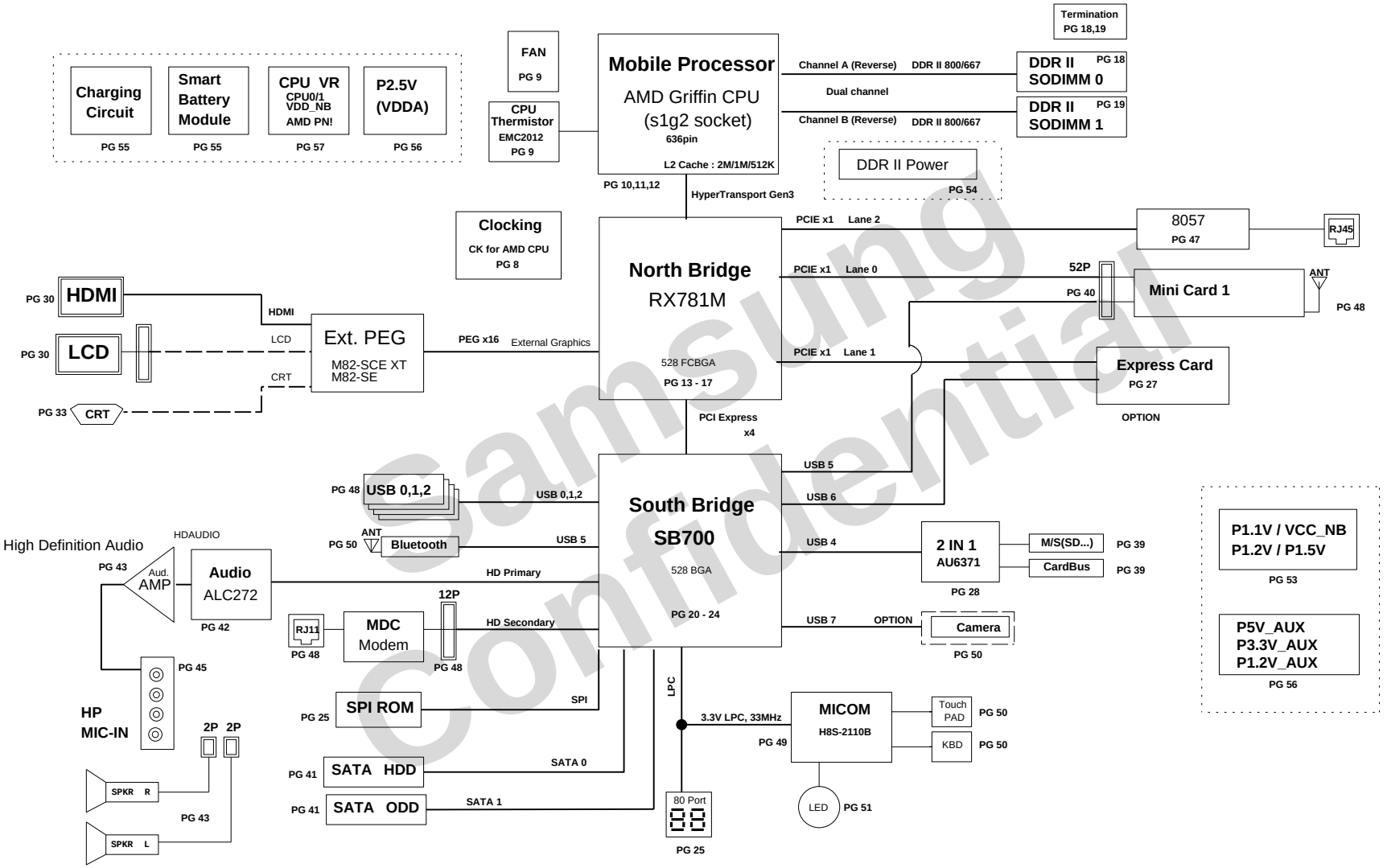
Model Name : Cambridge
PBA Name : MAIN
PCB Code : BA41-00XXXA

Dev. Step : PR
Revision : 1.0
T.R. Date : 2008.08.22

DRAW	CHECK	APPROVAL

■ *Owner : SEC Mobile R & D* *Signature :* *X*

DRAW JM	DATE 1/10/2008	TITLE Cambridge COVER	SAMSUNG ELECTRONICS
CHECK YJ	DEV. STEP PR		
APPROVAL BJ	REV 1.0		PART NO. BA41-009xxA
MODULE CODE	LAST EDIT August 24, 2008 14:34:27 PM	PAGE 1 OF 47	



DRAW JM	DATE 1/10/2008	TITLE Cambridge MAIN OPERATION BLOCK DIAGRAM	SAMSUNG ELECTRONICS
CHECK YJ	DEV. STEP PR		
APPROVAL BJ	REV 1.0		PART NO. BA41-009xxA
MODULE CODE	LAST EDIT August 24, 2008 14:34:27 PM	PAGE 2 OF 47	

BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	3	A,B,C
USB	AD29(internal)	-	USB2.0 #0 (USB0) : A USB2.0 #1 (USB1) : D USB2.0 #2 (USB4) : C USB2.0 #3 (USB5) : E USB2.0 #4 (EHCI) : H
Hub to PCI	AD30(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
Internal MAC	AD24(internal)	-	E
AC Link	-	-	B
GLAN	-	-	F

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core Voltage for CPU
GFX_CORE	Core Voltage for GPU
P1.05V (VCCP)	VTT for CPU, Crestline & ICH8-M
P3.3V_MICOM	3.3V always power rail (for Micom)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail for DDR (off in S4-S5)
P0.9V	0.9V power rail for DDR (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V switched on power rail (off in S4-S5)
P5.0V	5.0V switched power rail (off in S3-S5)
P5.0V_AUX	5.0V switched on power rail (off in S4-S5)
P5.0V_ALW	5.0V always power rail

USB PORT Assign

PORT #	ASSIGNED TO
	SYSTEM PORT 0
	SYSTEM PORT 1
	SYSTEM PORT 2
	NC
	NC
	Bluetooth
	Mini PCI Express 2
	Camera
	NC
	NC

PCI Express Assign

PORT #	ASSIGNED TO
0	NC
1	Mini Card 1 (WLAN)
2	NC
3	LOM
4	Mini Card 2 (ROBSON or DVB-T)
5	NC

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH8-M	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	25MHz	LAN	Intel LAN

LCD Pannel Detect (TBD)

Devices	Resolution	PANNEL_DETECT_0

I C / SMB Address

Devices	Address	Hex	Bus
ICH8-m	Master	-	SMBUS Master
CPU Thermal Sensor	0111 101x	7Ah	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

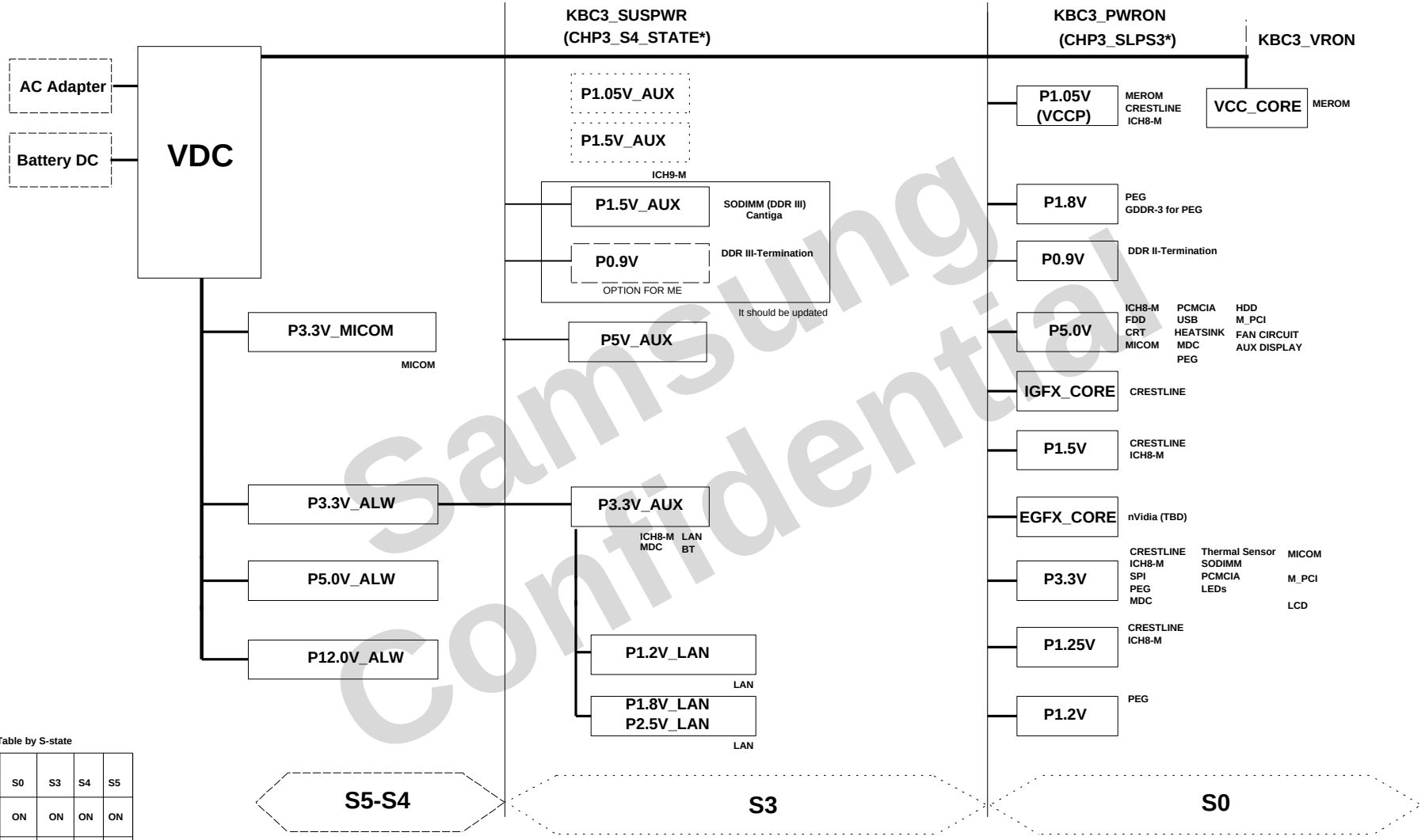
REVISION HISTORY

See rev notes for more information.

DESIGN: JM	DATE: 1/10/2008	TITLE: Cambridge CHIPSET POWER UNDEFINED	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE:	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 3 OF 47	

POWER DIAGRAM

Rev 0.1



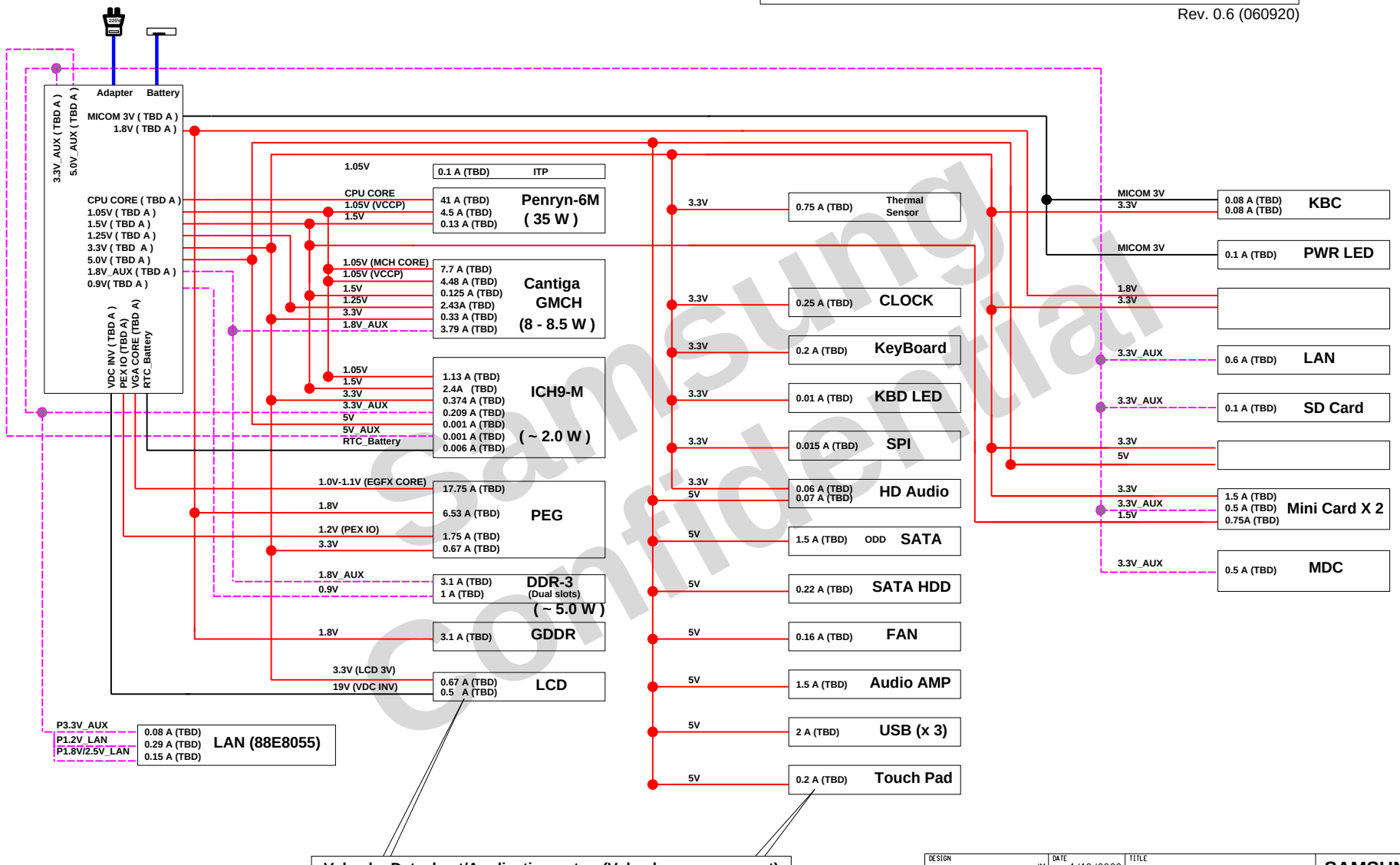
Power On/Off Table by S-state

Rail / State	S0	S3	S4	S5
+V*A(LWS) +V*LAN	ON	ON	ON	ON
+1.8V_AUX +0.9V	ON	ON	—	—
+V*AUX	ON	ON	—	—
+V	ON	—	—	—
+V* (CORE)	ON	—	—	—

DRAW: JM	DATE: 1/10/2008	TITLE: Cambridge MAIN POWER DIAGRAM	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE:	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 4 OF 47	

POWER RAILS ANALYSIS

Rev. 0.6 (060920)



Value by Datasheet/Application notes (Value by measurement)

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CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE:	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 5 OF 47	

POWER SEQUENCE

Rev. 0.7

Host Boot / ME Off
(SLPS4* = S4_STATE*) > (SLPM* = SLPS3*)
M-1) KBC3_DDR_PWRON (TBD) = 8) KBC3_SUSPWR
M-2) KBC3_ME_PWRON = 15) KBC3_PWRON

Host / ME Boot
(SLPS4* = S4_STATE*) > SLPM* > SLPS3*

Host S5 / ME Boot
(SLPS4* = SLPM*) > S4_STATE* > SLPS3*

RTC Battery — PRTC_BAT — CHP3_RTCRST# — 1

POWER S/W — 4) POWER_SW*

KBC — 7
- 7) KBC3_RSMRST#
- 8) CHP3_SLPS5#/4#/3#
- 110ms Delay
- 17) KBC3_PWRGD
- 15)VRM3_CPU_PWRGD
- 5) KBC3_SUSPWR
- 9) KBC3_PWRON
- 13) KBC3_VRON

ICH8-M — Sheet 22-25 — 16
- 10-1) ICH_CORE (P1.05V)
- 6) P3.3V_AUX
- PRTC, PRTC
- LAN100_SLP, INTVRMEN
- 7) P1.05V_AUX
- 7) P1.5V_AUX
- VRMPWRGD
- PWROK
- CL_PWROK
- 16) CLK3_PWRGD → CK-505 — Sheet 8 — 16-1) Clock Running
- 17) KBC3_PWRGD
- 15)VRM3_CPU_PWRGD
- 18) CPU1_PWRGDCPU
- 19) PLT3_RST*
- 19) PCI3_RST*

CPU VRM — DC/DC B'd
- 15) VRM3_CPU_PWRGD
- 11) VCCP3_PWRGD (GM-model)
- 12)GCORE3_PWRGD (PM-model)
- 13) KBC3_VRON (Back-up)
- 14) VCC_CORE

CPU — (Test Option) — Sheet 10-12 — 18, 20
- 10-1) P1.5V
- 10-1) P1.05V
- 20) CPU1_CPURST*

GMCH — Sheet 15-19
- 17) KBC3_PWRGD
- 17) KBC3_PWRGD
- PWROK
- CL_PWROK
- 19) PLT3_RST*
- 6) P1.8V_AUX
- 10-1) P3.3V
- 10) P1.05V (IGFX_CORE) PM-model only

SC486 — DDR2 POWER — Sheet 50 — 6
- 10) P5.0V
- 2) VDC
- 5) KBC3_SUSPWR
- 6) P1.8V_AUX
- 6) MEM1_VREF
- 10-2) 0.9V

Adapter / Battery — AC_DC / Battery — MAX 1909 — 3
- P3.3V_MICOM
- 8) KBC3_SUSPWR
- 9) KBC3_PWRON
- 2) VDC — 2
- 2-1) P12.0V_ALW

SC486 — 10) P1.5V
SC4435 — 10) P5.0V — 10
- 9-1) KBC3_PWRON_INV#

MAX 8734 — P3.3V_AUX & P5V_AUX — 3
- P5.0V_ALW
- P3.3V_MICOM — 6
- 6) P5.0V_AUX
- 6) P3.3V_AUX

ISL6227 — 9-1
- 2) VDC
- 9) KBC3_PWRON
- 10) P1.25
- 10) P1.05V (IGFX_CORE)
- 11) VCCP3_PWRGD

ADP3209 — 11
- 11-1) GFX_CORE
- 12)GCORE_PWRGD — 12

FDS6680A — Sheet 40 — 9-1
- 6) P3.3V_AUX
- 9-1) KBC3_PWRON_INV#
- 10-1) P3.3V

FDS6680A — Sheet 40
- 6) P1.8V_AUX
- 10-1) P1.8V

FDC653N — Sheet 40
- 10-1) P1.25
- 10-1) P1.2V

DDR3 Memory — Sheet 20-21
- 6) P1.8V_AUX
- 10-2) P0.9V

PCIe Devices — 19
- 10-1) P3.3V
- 10-1) P1.8V
- 10) P1.5V

PEG
- 10-1) P1.2V
- 2) VDC
- 10-1) P3.3V

PCI Devices
- 10-1) P3.3V
- 10-1) P1.8V
- 10) P1.5V
- 19) PCI3_RST*

LOM Marvell — Sheet 46-47
- 6-1) P1.2V_LAN
- 6-1) P1.8V/P2.5V_LAN

BCP69 — Sheet 46

TPS51124
- 2) VDC
- 11) KBC3_PWRON
- 12) P1.05V_M
- 12) P1.5

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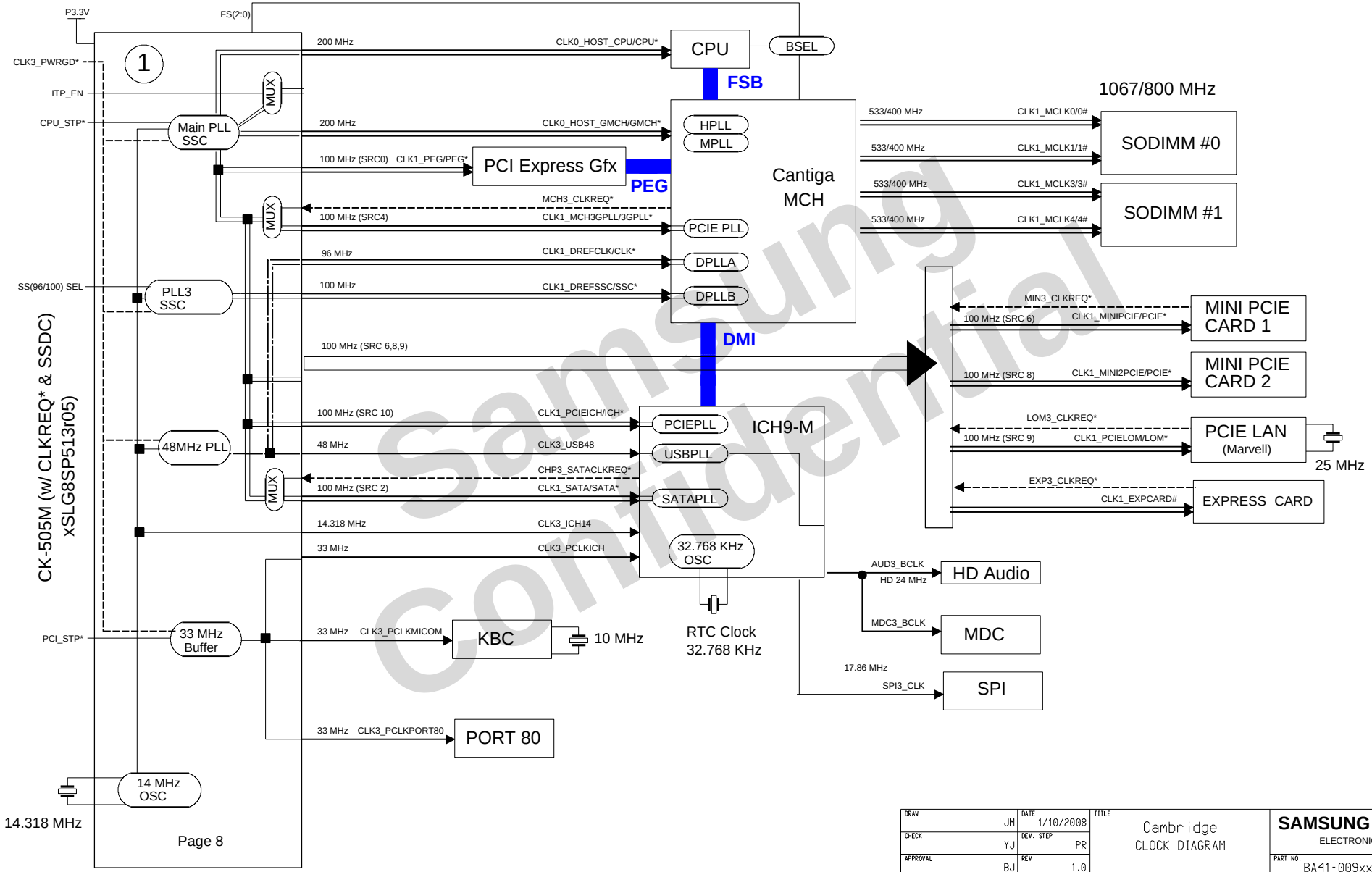
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE:	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 6 OF 47	

CLOCK DISTRIBUTION Rev. 0.1



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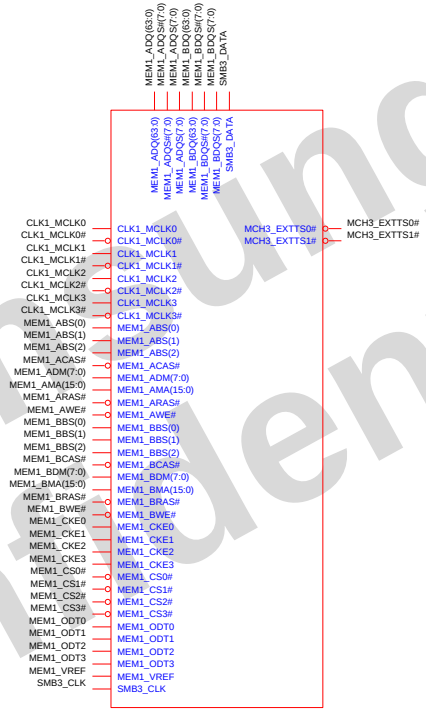
CHECK YJ	DEV. STEP PR		
APPROVAL BJ	REV 1.0		PART NO. BA41-009xxA
MODULE CODE	LAST EDIT August 24, 2008 14:34:27 PM	PAGE 7 OF 47	



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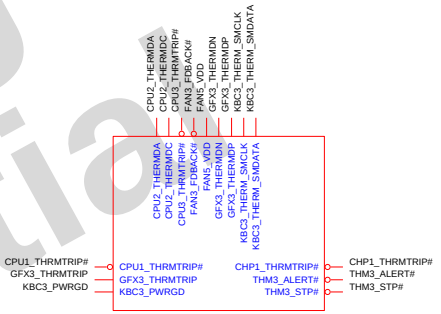
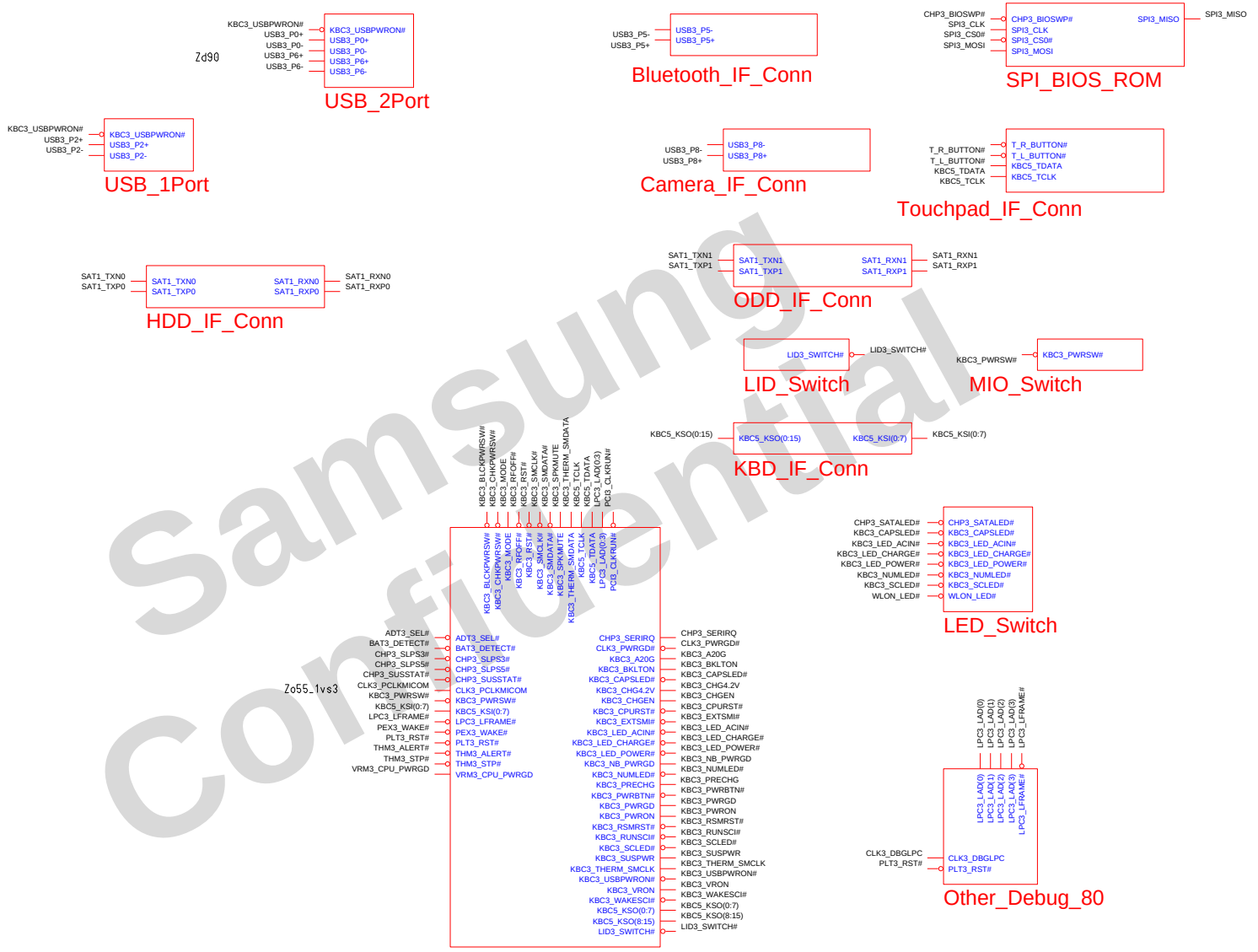


Thermal_Sensor_SMSC_Emc2102

DRAW: JM	DATE: 1/10/2008	TITLE: Cambridge MAIN PENRYN CPU (1/3)	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE:	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 8 OF 47	



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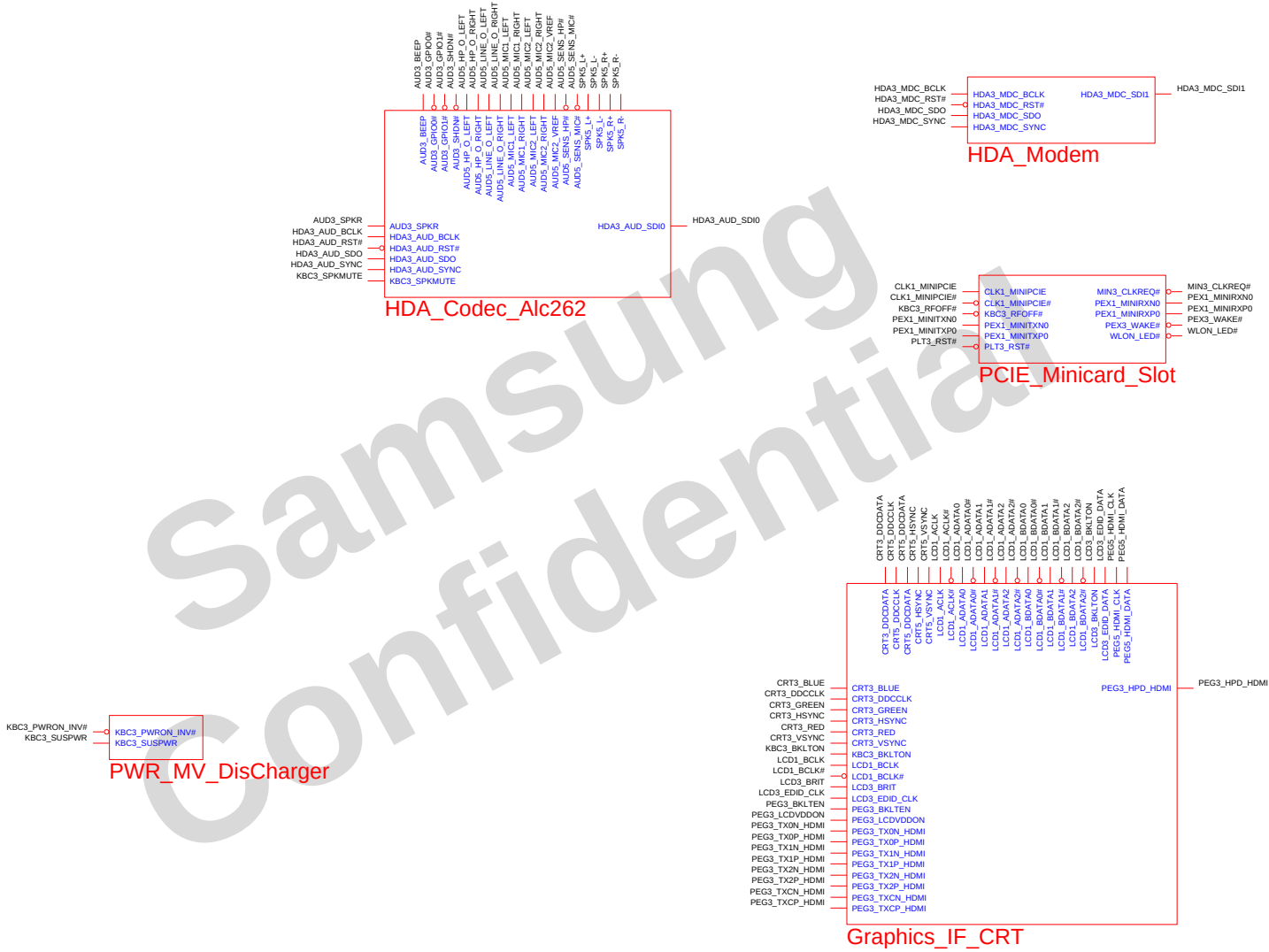
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE:	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 9 OF 47	



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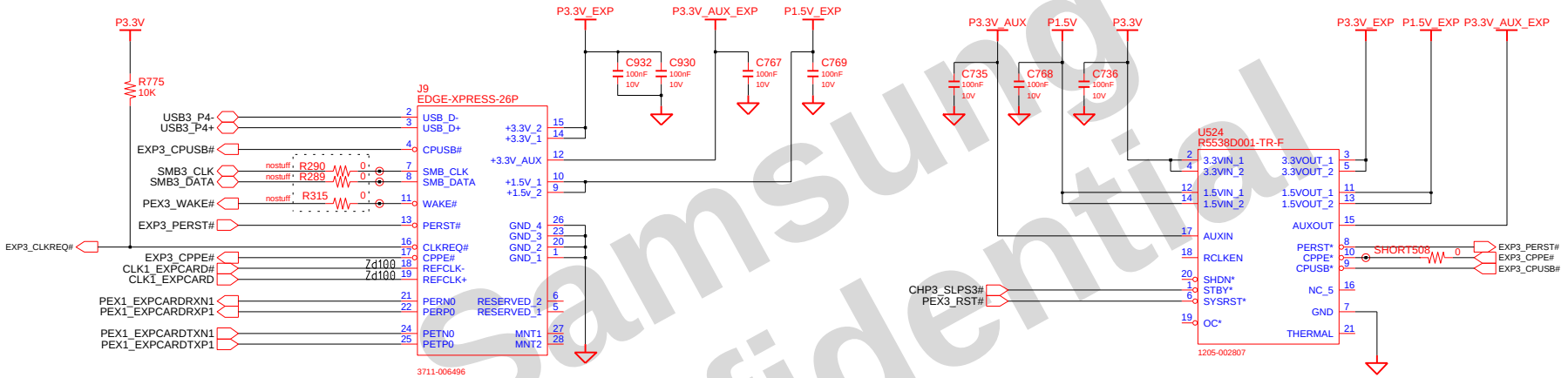
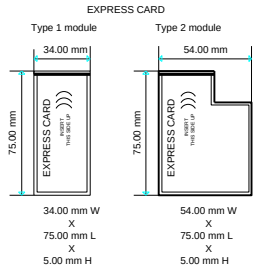
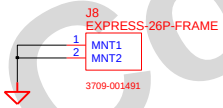
MODULE CODE:	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 10 OF 47	







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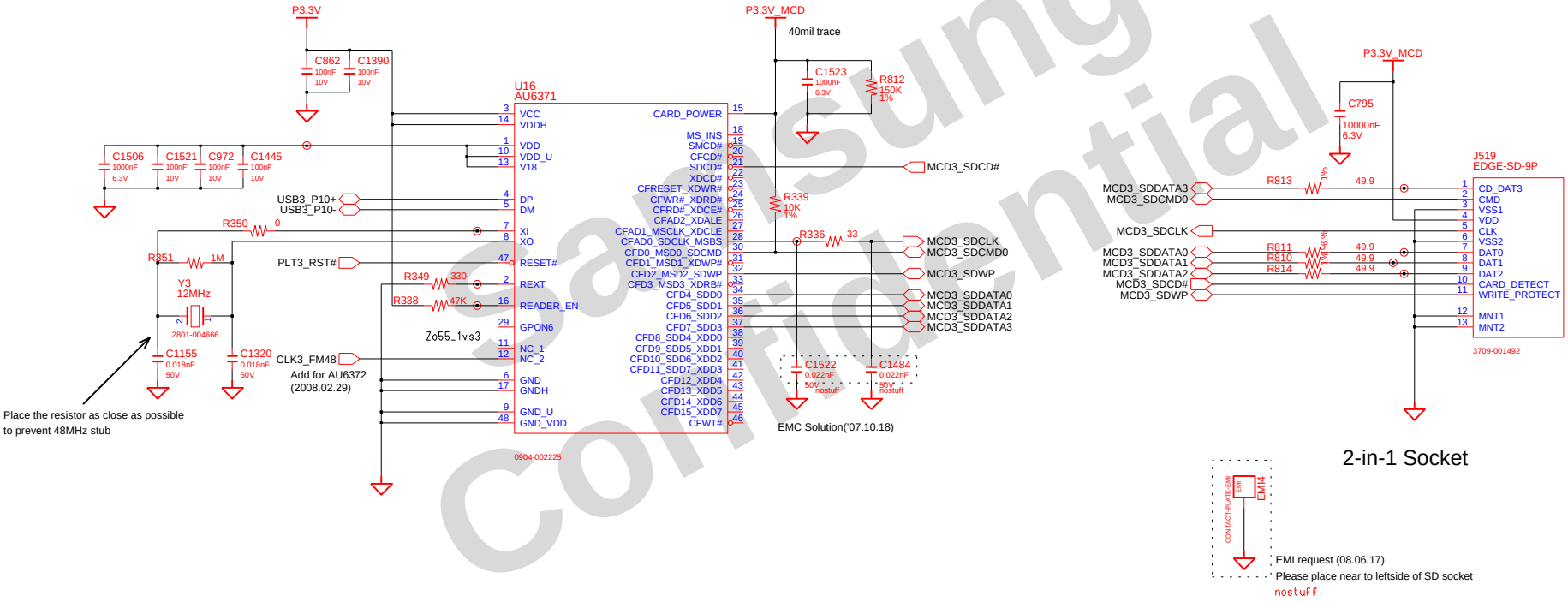
APPROVAL: BJ	REV: 1.0	EXPRESS CARD	PART NO.: BA41-009xxA
MODULE CODE: undefined	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 11 OF 47	

2 IN 1 CARD



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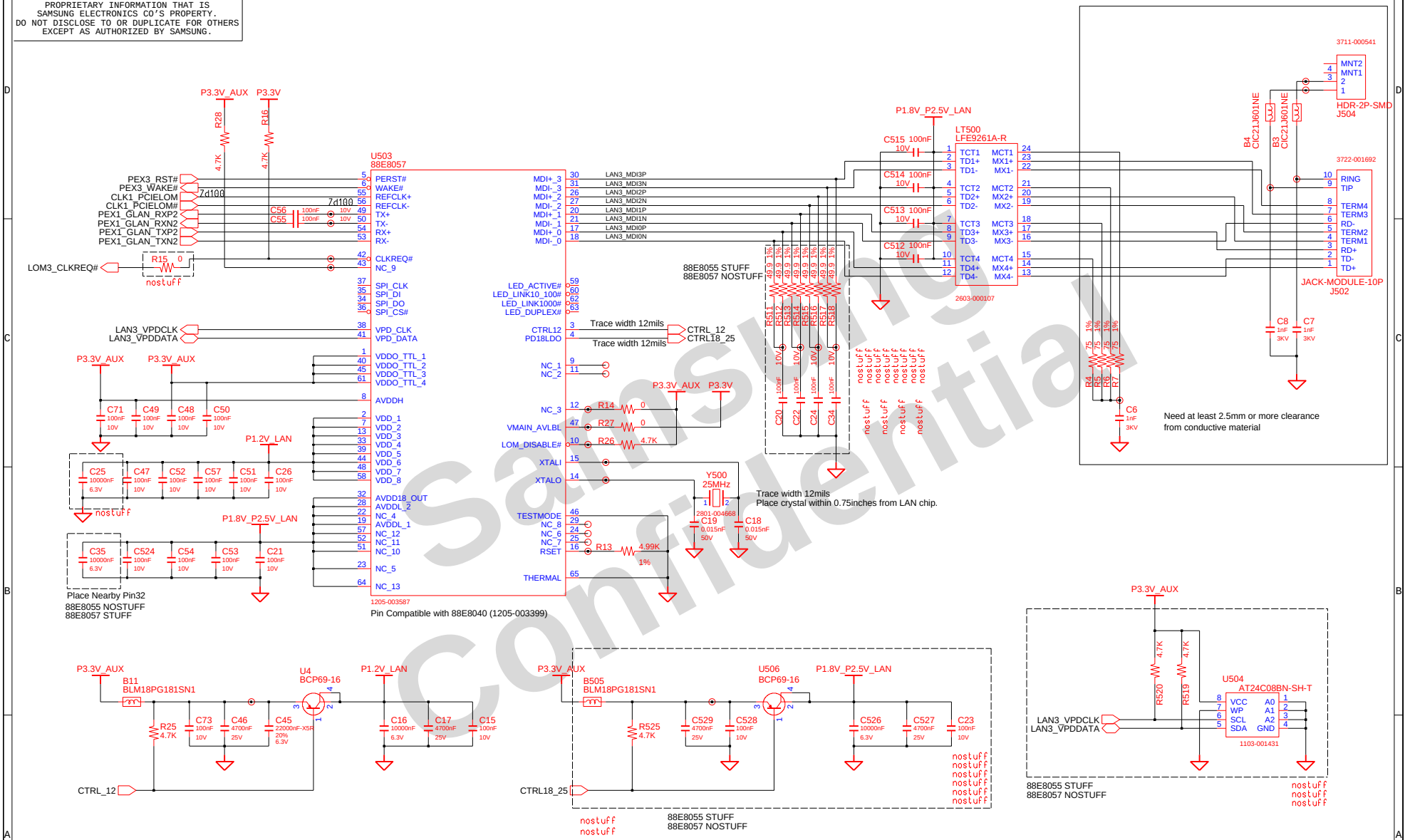
APPROVAL BJ	REV 1.0		PART NO. BA41-009xxA
MODULE CODE	LAST EDIT August 24, 2008 14:34:27 PM	PAGE 12 OF 47	



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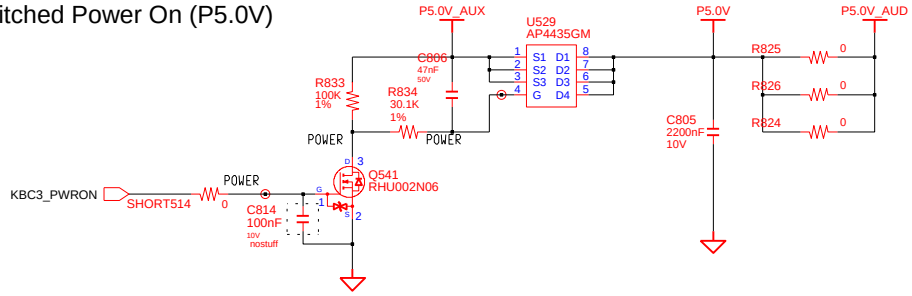
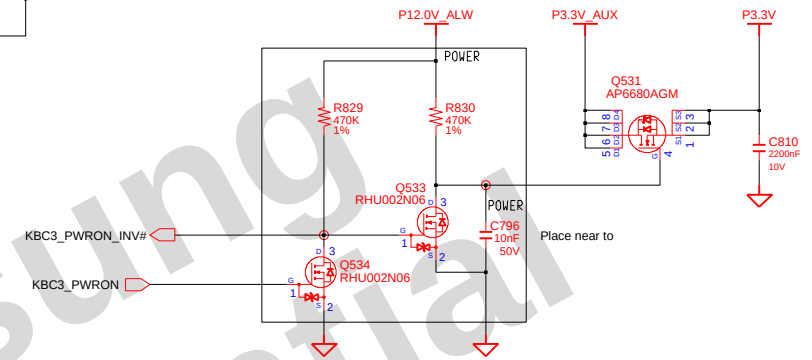
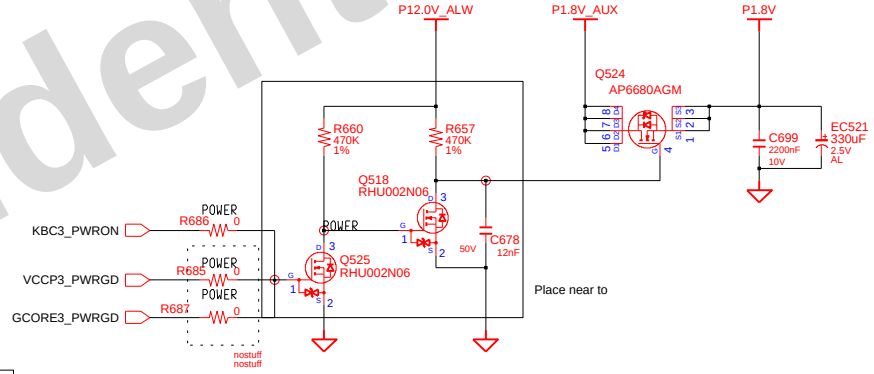
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE: undefined	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 13 OF 47	

Switched Power On (P5.0V)



Switched Power On (P3.3V & 1.8V)





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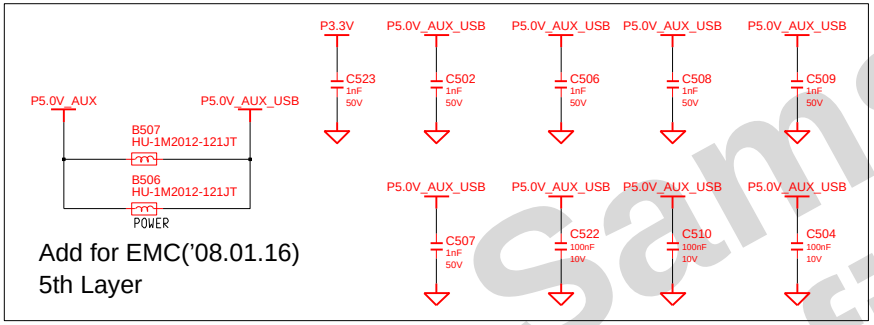
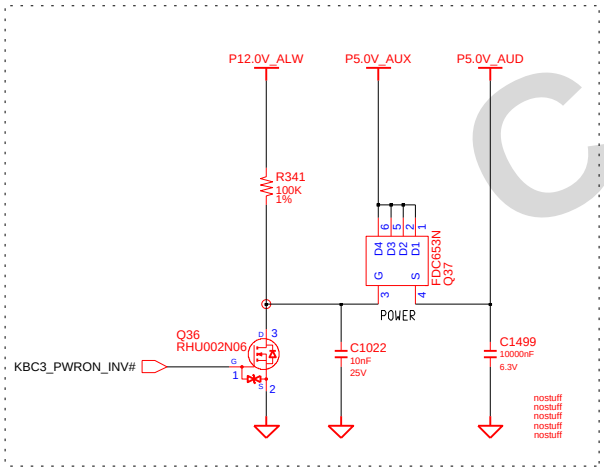
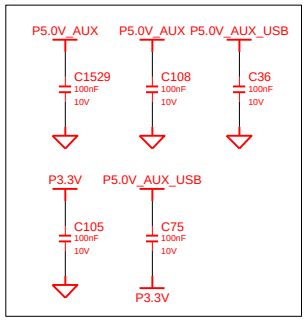
5th Layer



Audio Power (nostuff)

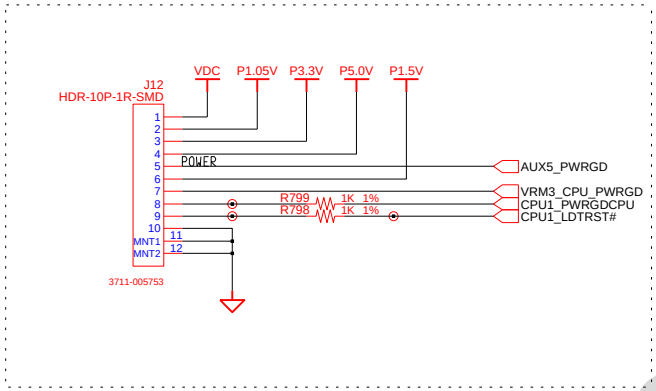




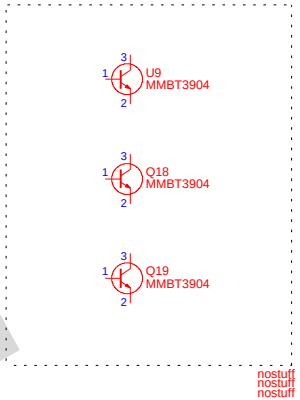
Add for SI(2007.12.6)

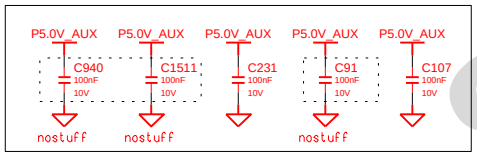
DRAW: JM	DATE: 1/10/2008	TITLE: Cambridge MAIN MICOM & SWITCHED POWER	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE: undefined	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 14 OF 47	

ICT PORT (Need to check net name)



For Debugging





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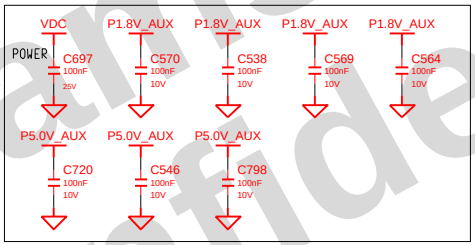

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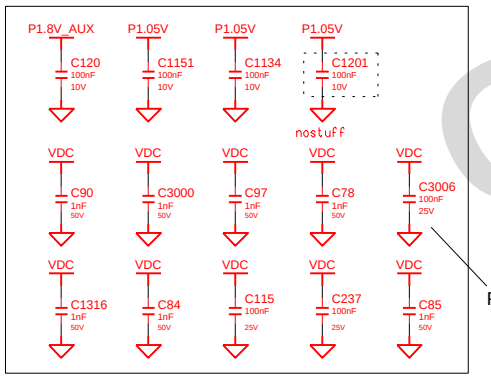
Bottom Side



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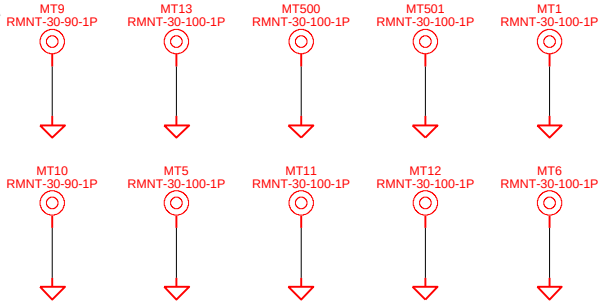
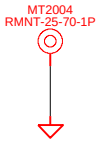
Top Side

EMC Request('08.06.16)

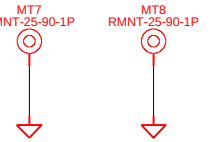
System



Board



Keyboard

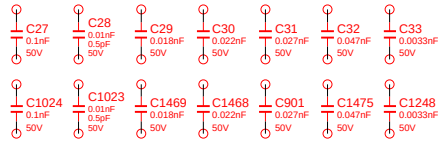


DRAW JM	DATE 1/10/2008	TITLE Cambridge	SAMSUNG ELECTRONICS
CHECK YJ	DEV. STEP PR		
APPROVAL BJ	REV 1.0	ICT PORT	PART NO. BA41-009xxA
MODULE CODE undefined	LAST EDIT August 24, 2008 14:34:27 PM	PAGE 15 OF 47	

REV1

PCB REVISION CONTROL (ICT)

NO	CONNECTION	DATE(YY/MM/DD)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			



DRAW JM	DATE 1/10/2008	TITLE Cambridge	SAMSUNG ELECTRONICS
CHECK YJ	DEV. STEP PR	TP	
APPROVAL BJ	REV 1.0		PART NO. BA41-009xxA
MODULE CODE undefined	LAST EDIT August 24, 2008 14:34:27 PM	PAGE 16 OF 47	

AUX5_PWRGD
CTRL_12
SPK5_L+
SPK5_L-
SPK5_R+
SPK5_R-

CRT3_RED
FAN5_VDD
SMB3_DATA
SPI3_CS0#
SPI3_MISO
SPI3_MOSI
THM3_STP#

WLON_LED#
AUD3_SHDN#
EXP3_CPPE#
KBC3_CHGEN
KBC3_PWRGD
KBC3_PWRON
KBC5_TDATA

CRT3_GREEN
CRT3_HSYNC
CRT3_VSYNC
CRT5_HSYNC
CRT5_VSYNC

SMB3_CLK
SPI3_CLK
PEX3_WAKE#
AUD3_GPIO0#
AUD3_GPIO1#

BAT3_SMCLK#
CHP3_GPIO16
CHP3_GPIO17
CHP3_SERIRQ
CHP3_SLPS3#

CHP3_SLPS5#

CLK3_USB48
Za55_1vs3
ADT3_SEL#
AUD3_BEEP
AUD3_SPKR
KBC3_USBPWRON#
CLK3_FM48

CRT3_BLUE
CTRL18_25
KBC3_A20G
KBC3_RST#
KBC3_VRON
KBC5_TCLK
CLK3_DBGLPC
LCD3_BRIT
MCD3_SDWP

CRT3_DDCCLK
CRT5_DDCCLK
EXP3_CPUSB#
EXP3_PERST#
MEM1_VREF
PLT3_RST#

KBC3_BKLTON
KBC3_PRECHG
KBC3_PWRSW#
KBC3_RFOFF#
KBC3_SCLED#
KBC3_SMCLK#
KBC3_SUSPWR
KBC5_KSI(0)

KBC5_KSI(2)
KBC5_KSI(3)
KBC5_KSI(4)
KBC5_KSI(5)
KBC5_KSI(6)
KBC5_KSI(7)
KBC5_KSO(0)
KBC5_KSO(1)
KBC5_KSO(2)
KBC5_KSO(3)
KBC5_KSO(4)
KBC5_KSO(5)
KBC5_KSO(6)
KBC5_KSO(7)
KBC5_KSO(8)
KBC5_KSO(9)
LAN3_VPDCLK
LCD3_BKLTON
LPC3_LAD(0)
LPC3_LAD(1)
LPC3_LAD(2)
LPC3_LAD(3)
MCD3_SDCMD0

MCD3_SDCD#
MCD3_SDCLK

SMB3_ALERT#
THM3_ALERT#
T_L_BUTTON#
T_R_BUTTON#
VCCP3_PWRGD
BAT3_DETECT#
BAT3_SMDATA#
CHP3_BIOSWP#

CHP3_RTCRST#

KBC5_KSO(14)
KBC5_KSO(15)
LAN3_VPDDATA

CPU2_THERMDA
CPU2_THERMDC
CRT3_DDCDATA
CRT5_DDCDATA
EXP3_CLKREQ#
FAN3_FDBACK#
HDA3_AUD_SDO
HDA3_MDC_SDO
KBC3_CPURST#
KBC3_EXTSMI#
KBC3_NUMLED#
KBC3_PWRBTN#
KBC3_RSMRST#
KBC3_RUNSCI#
KBC3_SMDATA#
KBC3_SPKMUTE
KBC5_KSO(10)
KBC5_KSO(11)
KBC5_KSO(12)
KBC5_KSO(13)
LID3_SWITCH#
LOM3_CLKREQ#
LPC3_LFRAME#
MCD3_SDDATA0
MCD3_SDDATA1
MCD3_SDDATA2
MCD3_SDDATA3

MIN3_CLKREQ#
PCI3_CLKRUN#
AUD5_SENS_HP#

CHP3_SATALED#
PEG5_HDMI_CLK

AUD5_HP_O_LEFT
AUD5_MIC1_LEFT
AUD5_MIC2_LEFT
AUD5_MIC2_VREF
AUD5_SENS_MIC#
CHP3_BIOS_CR#

CHP3_INTRUDER#

CLK3_PCLKMICOM
CPU1_THRMTRIP#
CPU3_THRMTRIP#

HDA3_HDMI_SDI2

KBC3_CHKPWRSW#

LCD3_EDID_DATA
CPU1_PWRGDCPU

HDA3_AUD_BCLK
HDA3_AUD_RST#
HDA3_AUD_SDI0
HDA3_AUD_SYNC

HDA3_MDC_BCLK
HDA3_MDC_RST#
HDA3_MDC_SDI1
HDA3_MDC_SYNC
KBC3_CAPSLED#
KBC3_WAKESCI#
LCD3_EDID_CLK

CHP3_SUSSTAT#

KBC3_BLCKPWRSW#
KBC3_LED_POWER#
KBC3_PWRON_INV#
AUD5_LINE_O_LEFT

KBC3_LED_CHARGE#
KBC3_THERM_SMCLK

AUD5_LINE_O_RIGHT
VRM3_CPU_PWRGD
AUD5_HP_O_RIGHT
AUD5_MIC1_RIGHT
AUD5_MIC2_RIGHT

KBC3_THERM_SMDATA

P3.3V_AUX
P3.3V_AUX
P3.3V_AUX
P3.3V_AUX

VCC_CRT

VDC_CHG

VDC_INV
VDC_INV
VDC_INV
VDC_INV

P3.3V_AUX_EXP

P1.8V_P2.5V_LAN

VDC
VDC
VDC
VDC

VREF
VREF
VREF
VREF
POWER

P5.0V_FILT
POWER

P3.3V_MICOM

P4.75V_AUD

P5.0V_AUX
P5.0V_AUX
P5.0V_AUX
P5.0V_AUX

P12.0V_ALW

CPU_CORE
CPU_CORE
CPU_CORE
CPU_CORE

G_AUD

G_CHG

G_CPU

G_DDR

G_MIC

GROUND
GROUND
GROUND
GROUND
GROUND
GROUND
GROUND
GROUND
GROUND
GROUND

G_P3.3V
POWER

LCD_VDD3V

P0.9V
P0.9V
P0.9V
P0.9V

P1.5V
P1.5V
P1.5V
P1.5V

P3.3V
P3.3V
P3.3V
P3.3V

P5.0V
P5.0V
P5.0V
P5.0V

P1.05V
P1.05V
P1.05V
P1.05V

PRTC_BAT

P1.2V_LAN
P1.2V_LAN
P1.2V_LAN
P1.2V_LAN

P1.5V_AUX
P1.5V_AUX
P1.5V_AUX
P1.5V_AUX

P1.5V_EXP
P1.5V_EXP
P1.5V_EXP
P1.5V_EXP

P1.8V_AUX
P1.8V_AUX
P1.8V_AUX
P1.8V_AUX

P3.3V_EXP

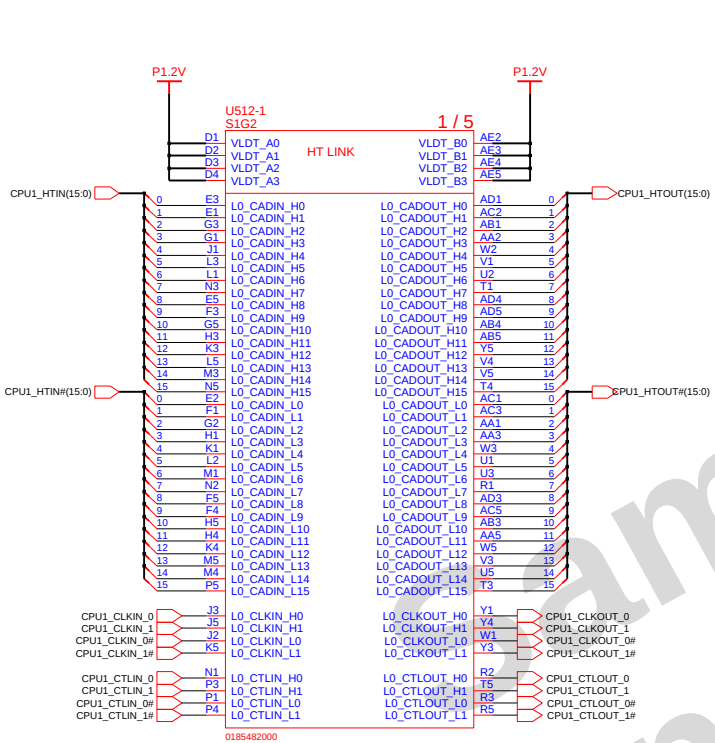
P3.3V_MCD

P5.0V_ALW
POWER
P5.0V_AUD

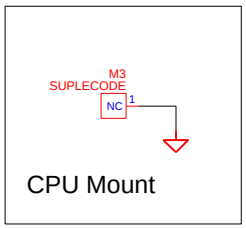
P5.0V_AMP

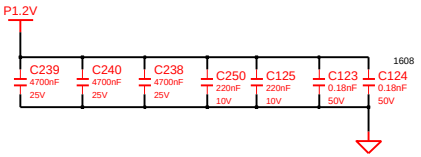
P5.0V_AUX_USB

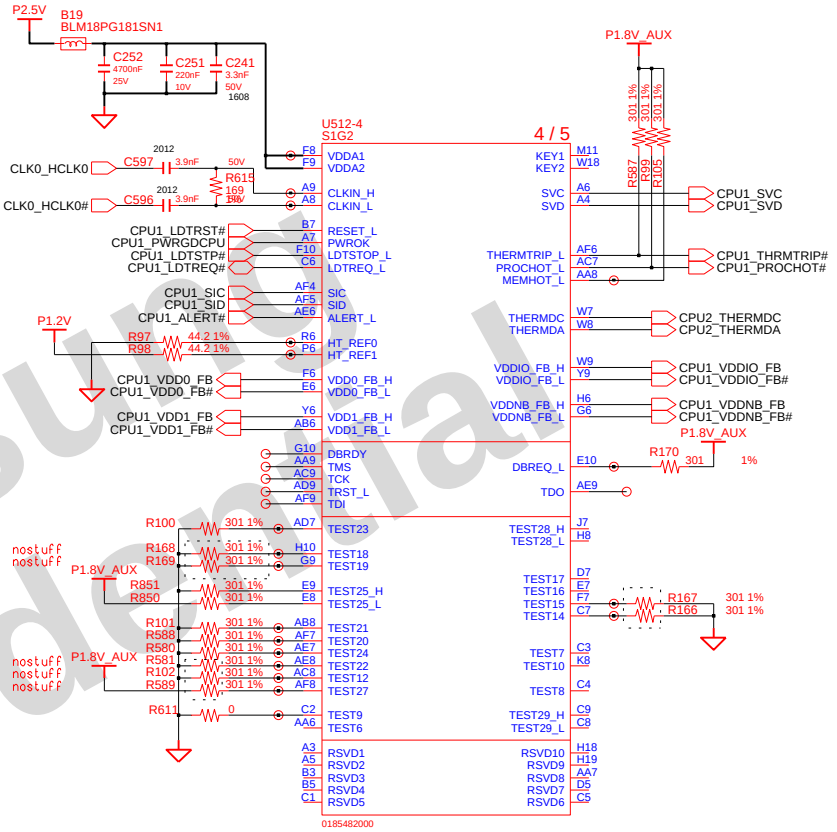
DESIGN: JM	DATE: 1/10/2008	TITLE: Cambridge TP UNDEFINED	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE:	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 17 OF 47	

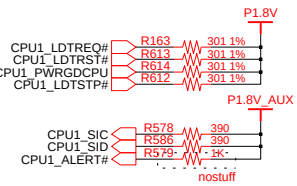


CPU Socket : 0185482000 (3704-001228)

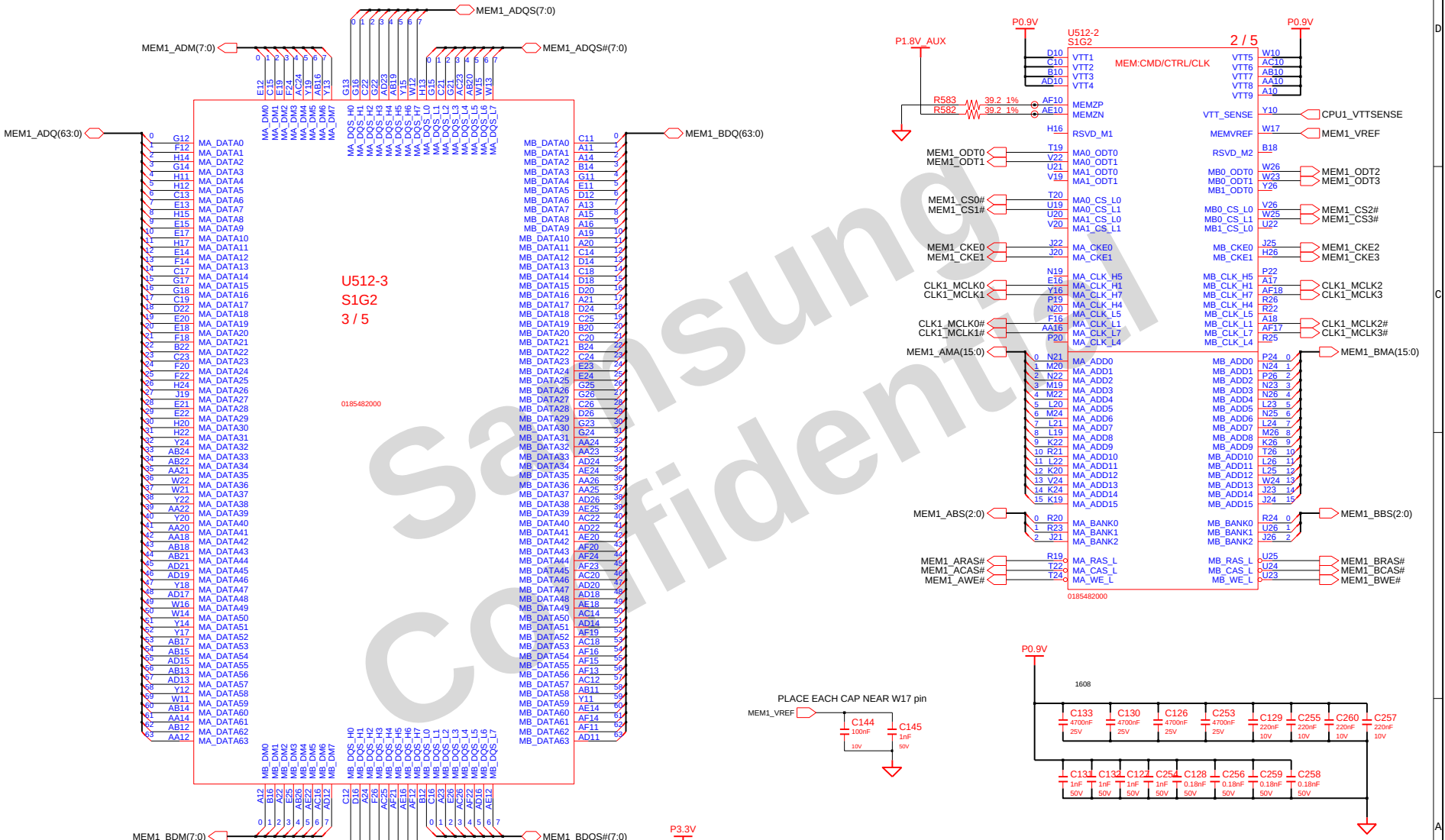






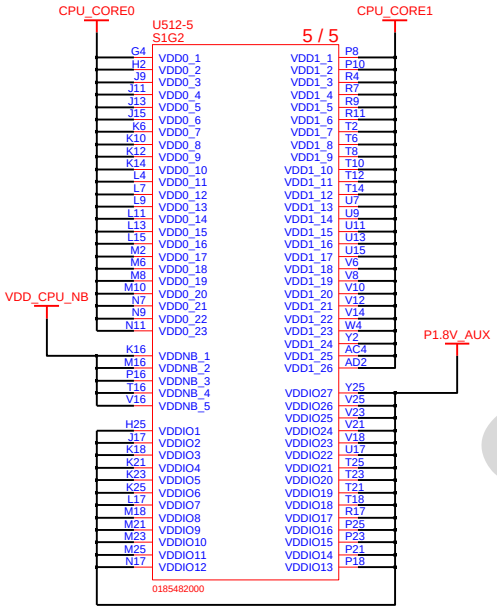


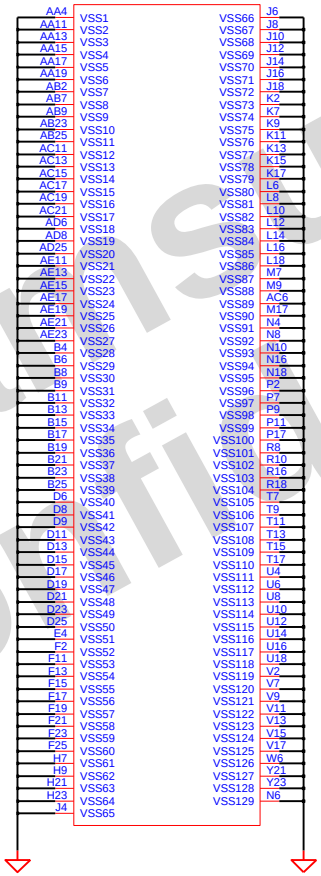
DESIGN: JM	DATE: 3/19/2008	TITLE: Cambridge	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR	s1g2 CPU (1/3)	
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE: undefined	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 18 OF 47	

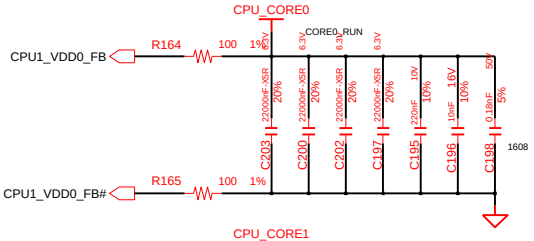


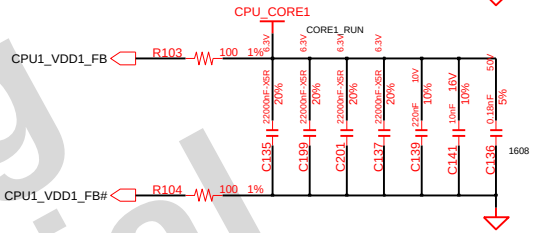
DRAW JM	DATE 1/10/2008	TITLE Cambridge s1g2 CPU (2/3)	SAMSUNG ELECTRONICS
CHECK YJ	DEV. STEP PR		
APPROVAL BJ	REV 1.0		PART NO. BA41-009xxA
MODULE CODE undefined	LAST EDIT August 24, 2008 14:34:27 PM	PAGE 19 OF 47	

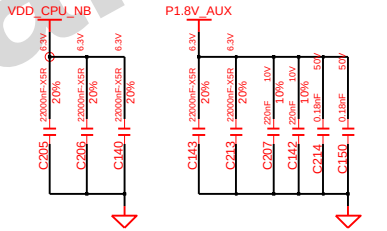
CPU Socket : 0185482000



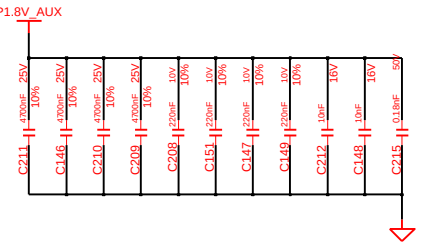




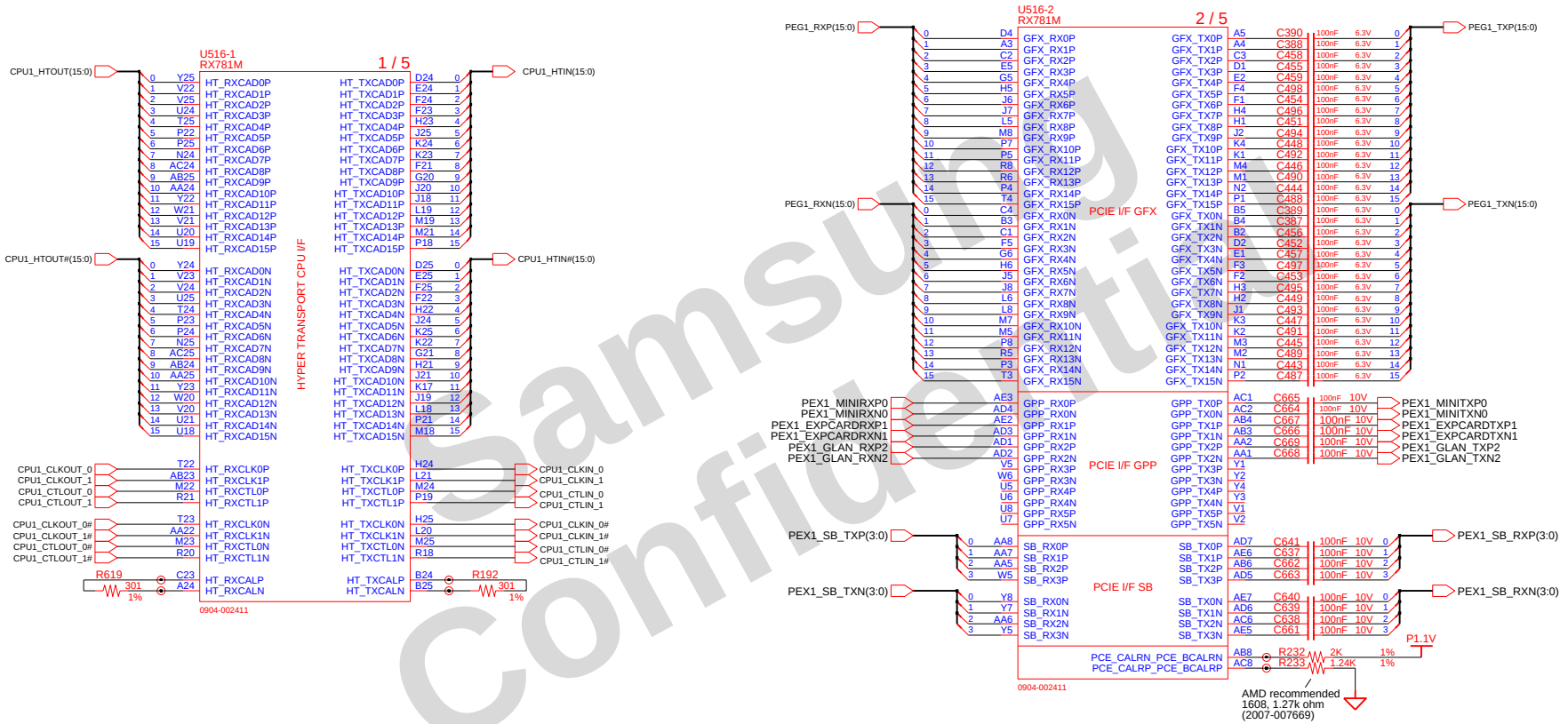




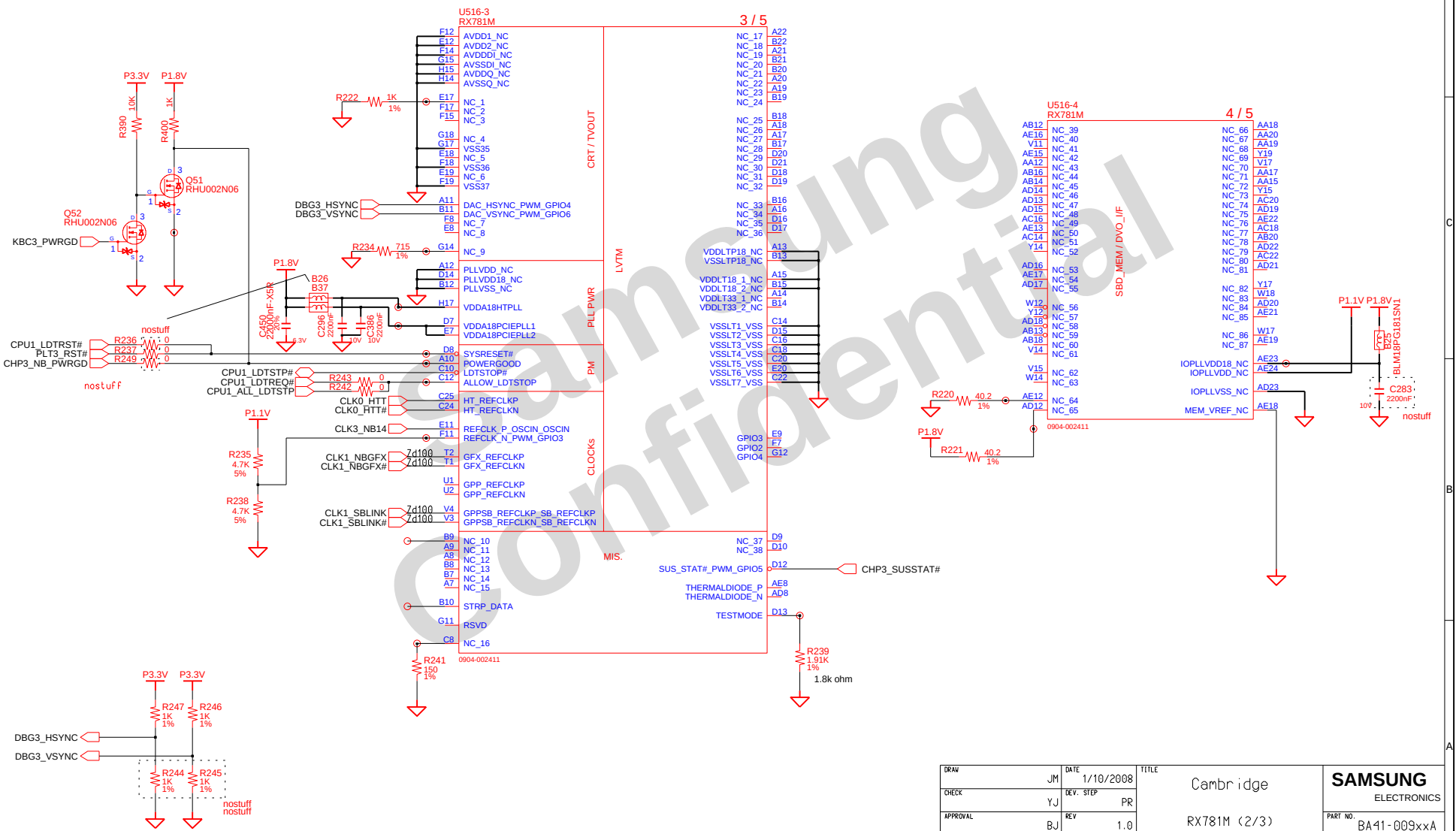
Decoupling between processor and Memory
Place close to processor as possible



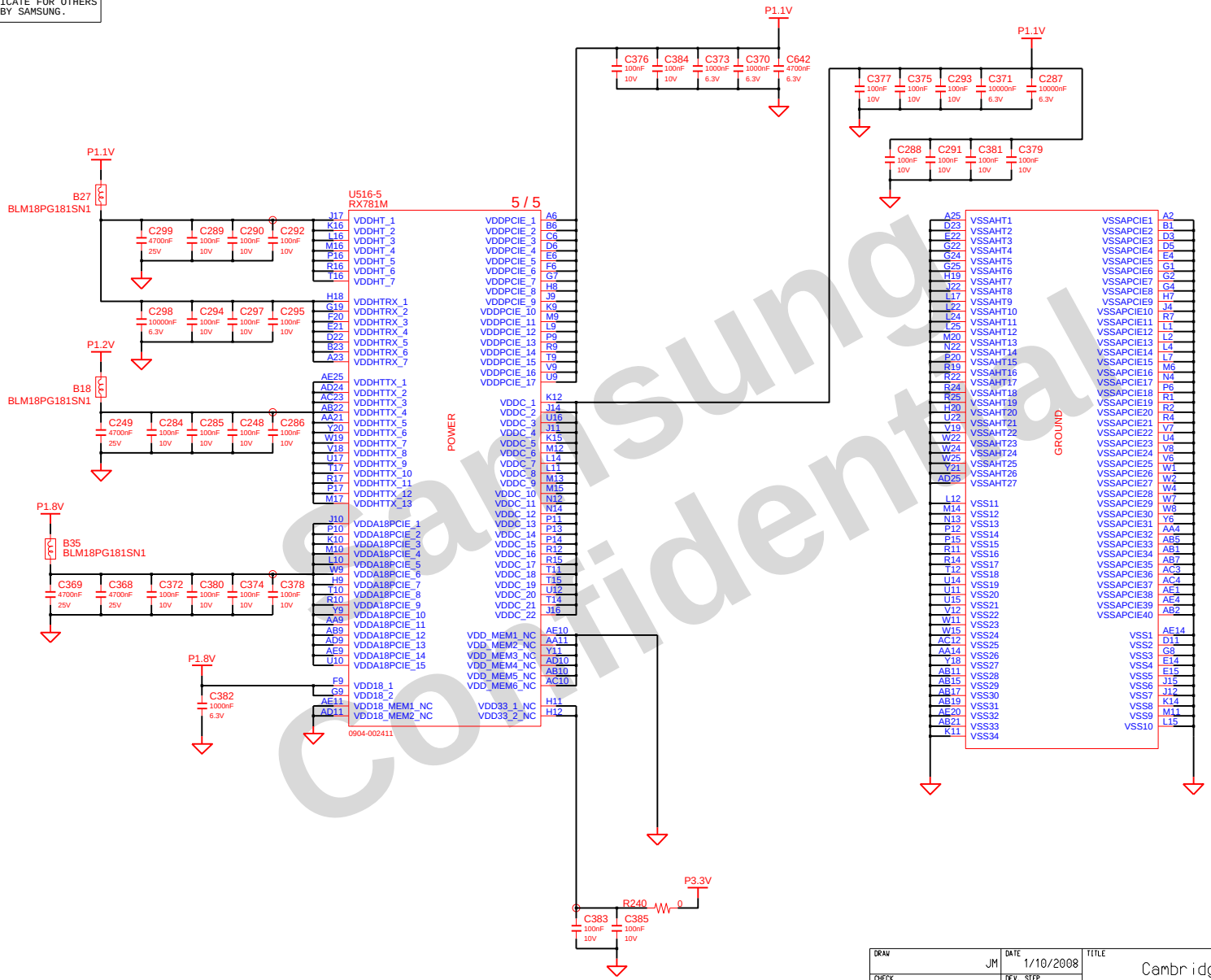
DRAW: JM	DATE: 1/10/2008	TITLE: Cambridge	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0	s1g2 CPU (3/3)	PART NO.: BA41-009xxA
MODULE CODE: undefined	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 20 OF 47	



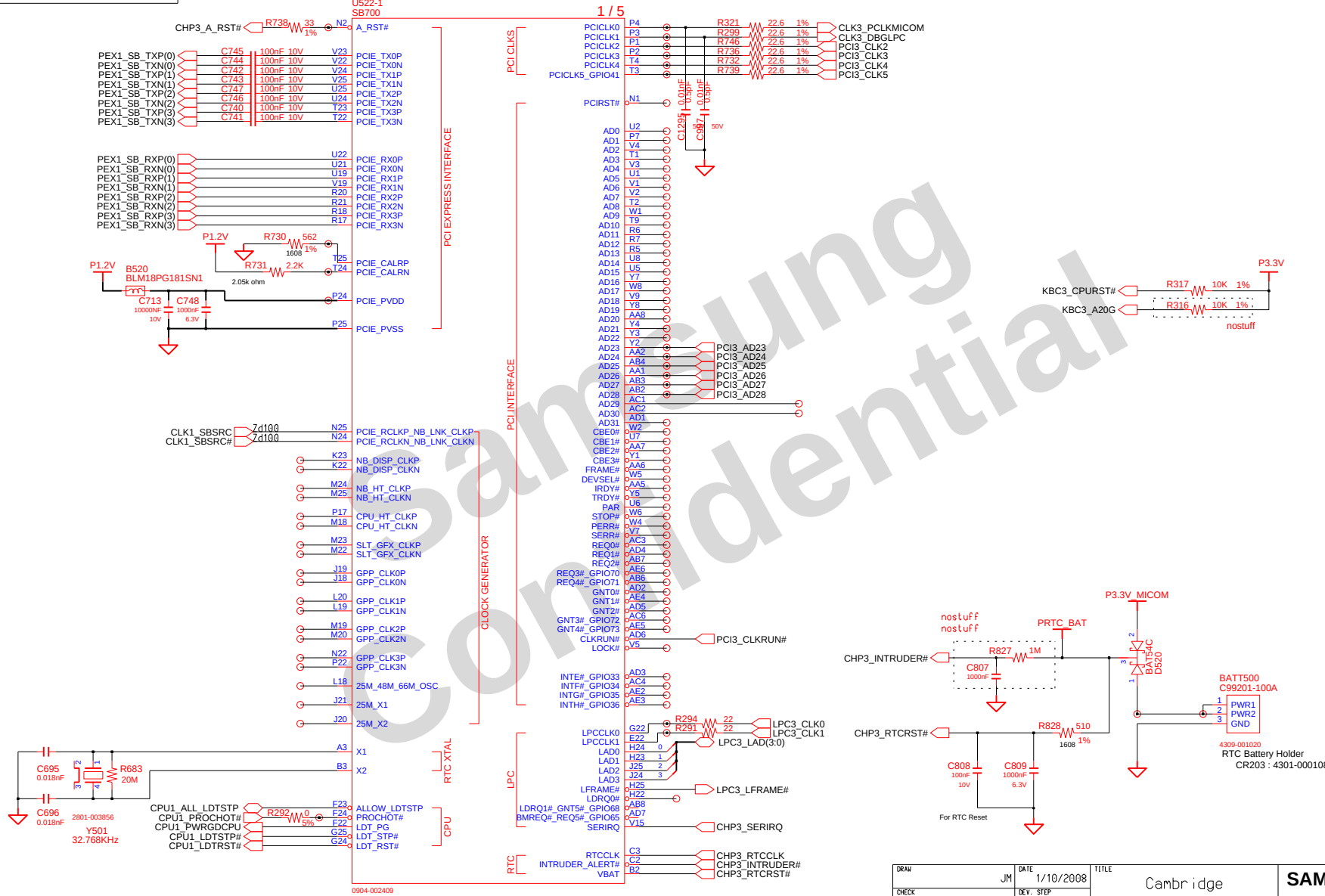
DRAW: JM	DATE: 1/10/2008	TITLE: Cambridge	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR	RX781M (1/3)	PART NO.: BA41-009xxA
APPROVAL: BJ	REV: 1.0		
MODULE CODE:	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 21 OF 47	



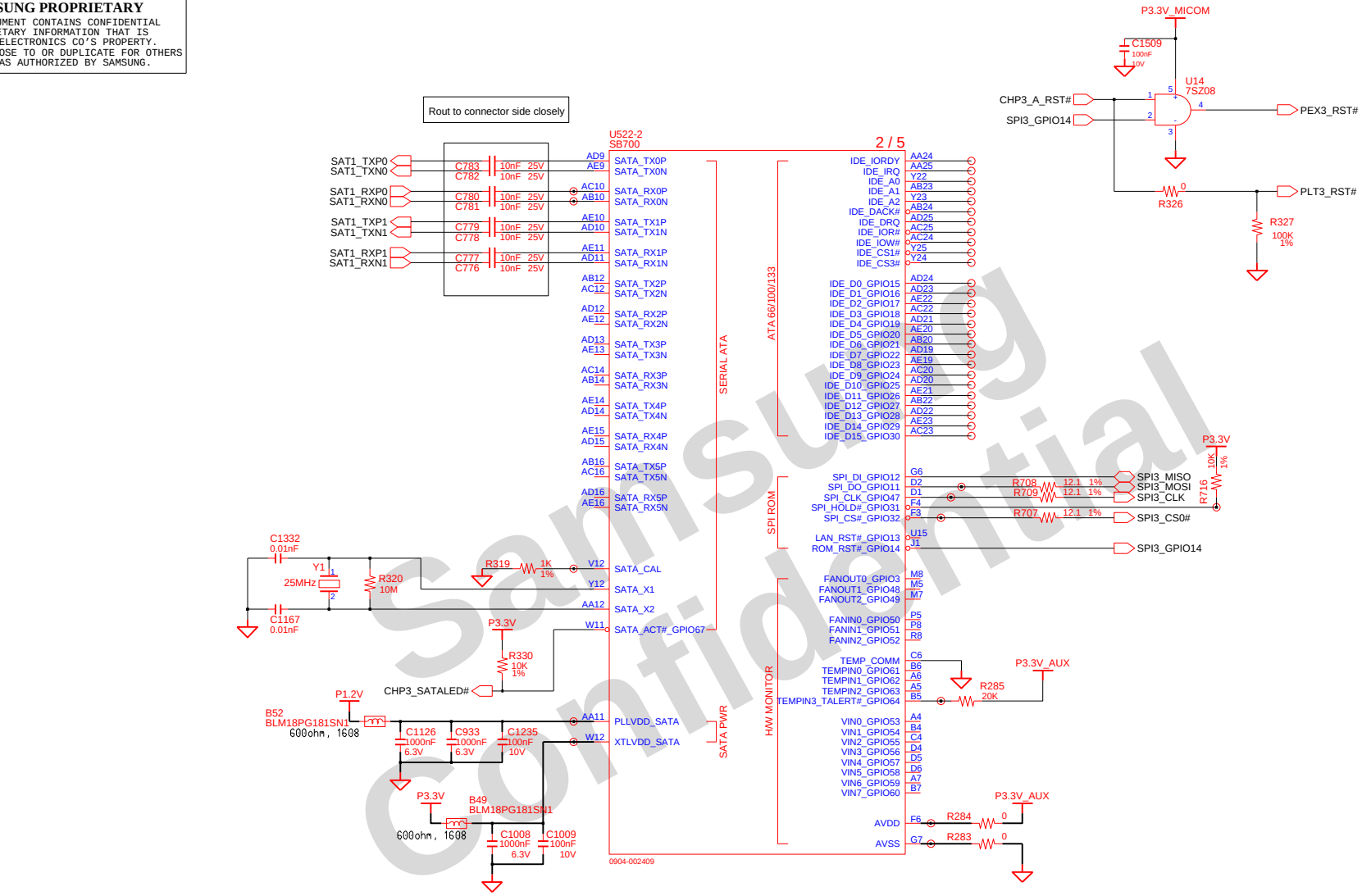
DRAW JM	DATE 1/10/2008	TITLE Cambridge	SAMSUNG ELECTRONICS
CHECK YJ	DEV. STEP PR		
APPROVAL BJ	REV 1.0	RX781M (2/3)	PART NO. BA41-009xxA
MODULE CODE	LAST EDIT August 24, 2008 14:34:27 PM	PAGE 22 OF 47	



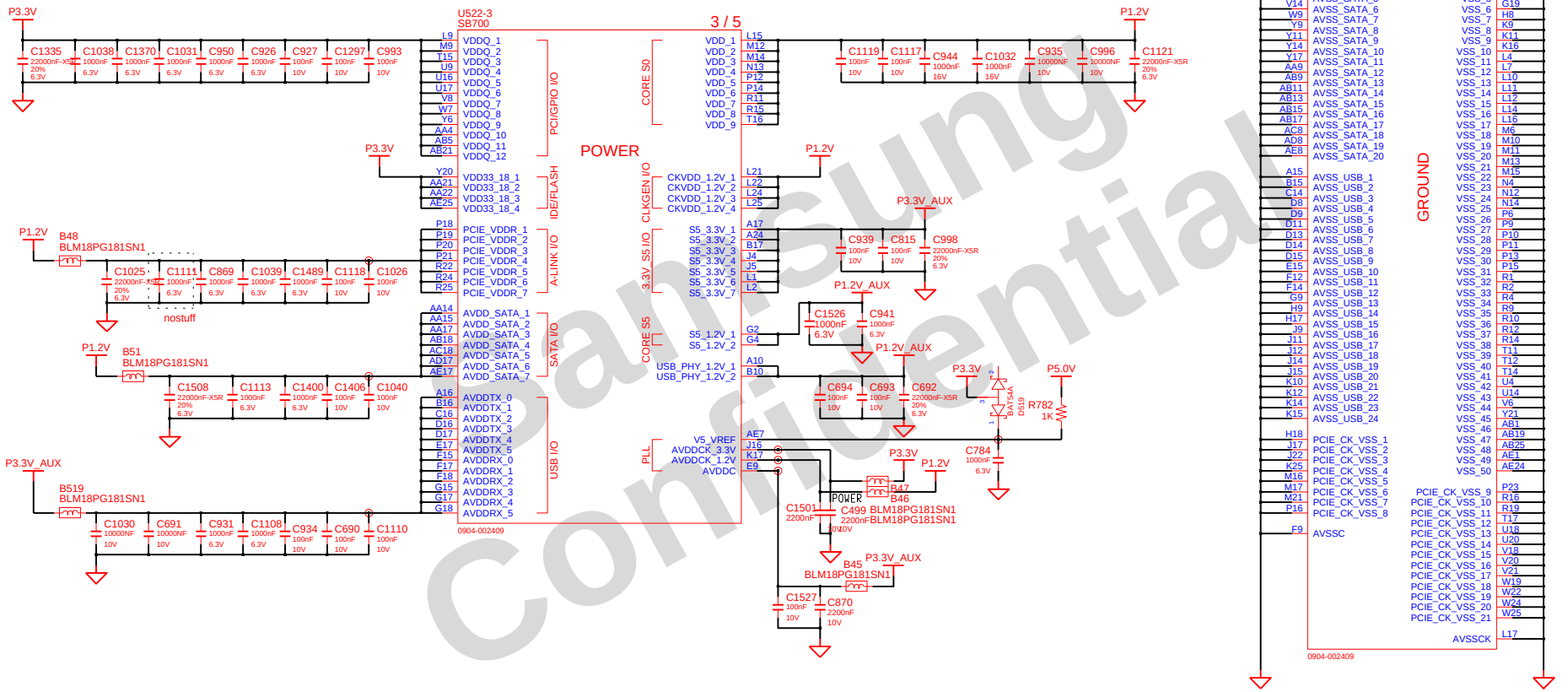
DRAW: JM	DATE: 1/10/2008	TITLE: Cambridge	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR	RX781M (3/3)	
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE:	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 23 OF 47	



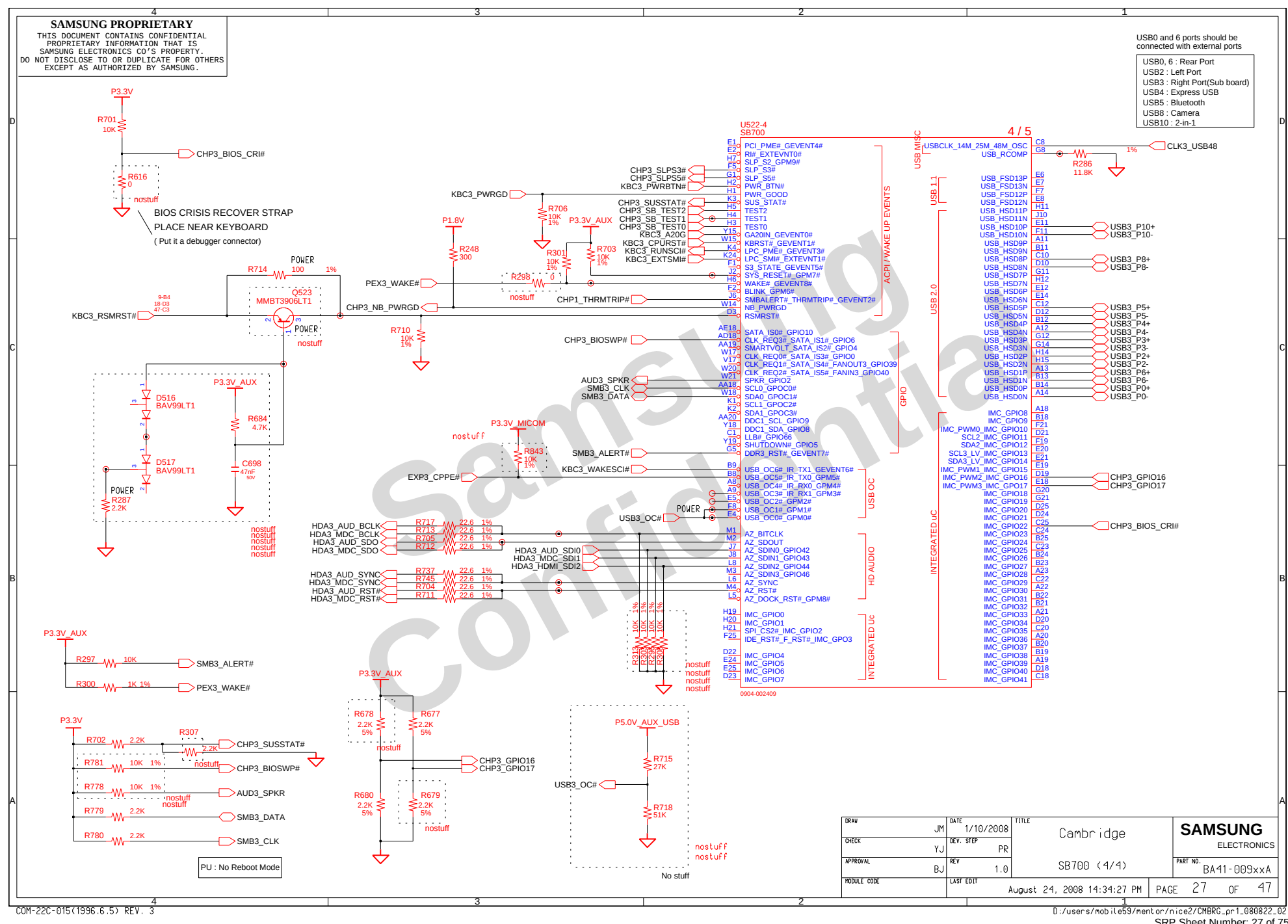
DRAW: JM	DATE: 1/10/2008	TITLE: Cambridge	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0	SB700 (1/4)	PART NO.: BA41-009xxA
MODULE CODE:	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 24 OF 47	



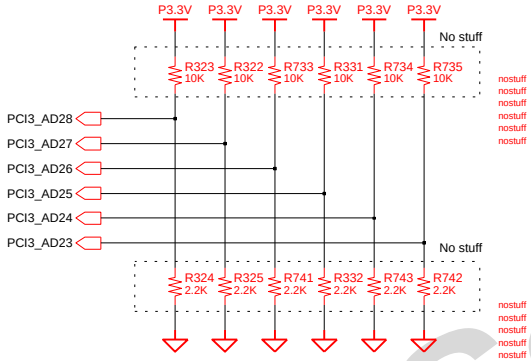
DRAW: JM	DATE: 1/10/2008	TITLE: Cambridge	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR	SB700 (2/4)	
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE:	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 25 OF 47	

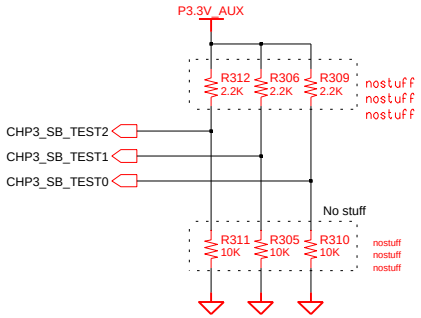


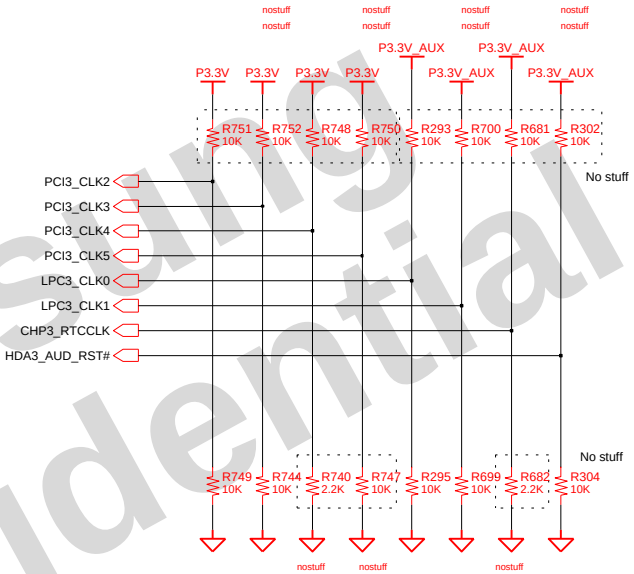
DRAW: JM	DATE: 1/10/2008	TITLE: Cambridge	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0	SB700 (3/4)	PART NO.: BA41-009xxA
MODULE CODE:	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 26 OF 47	



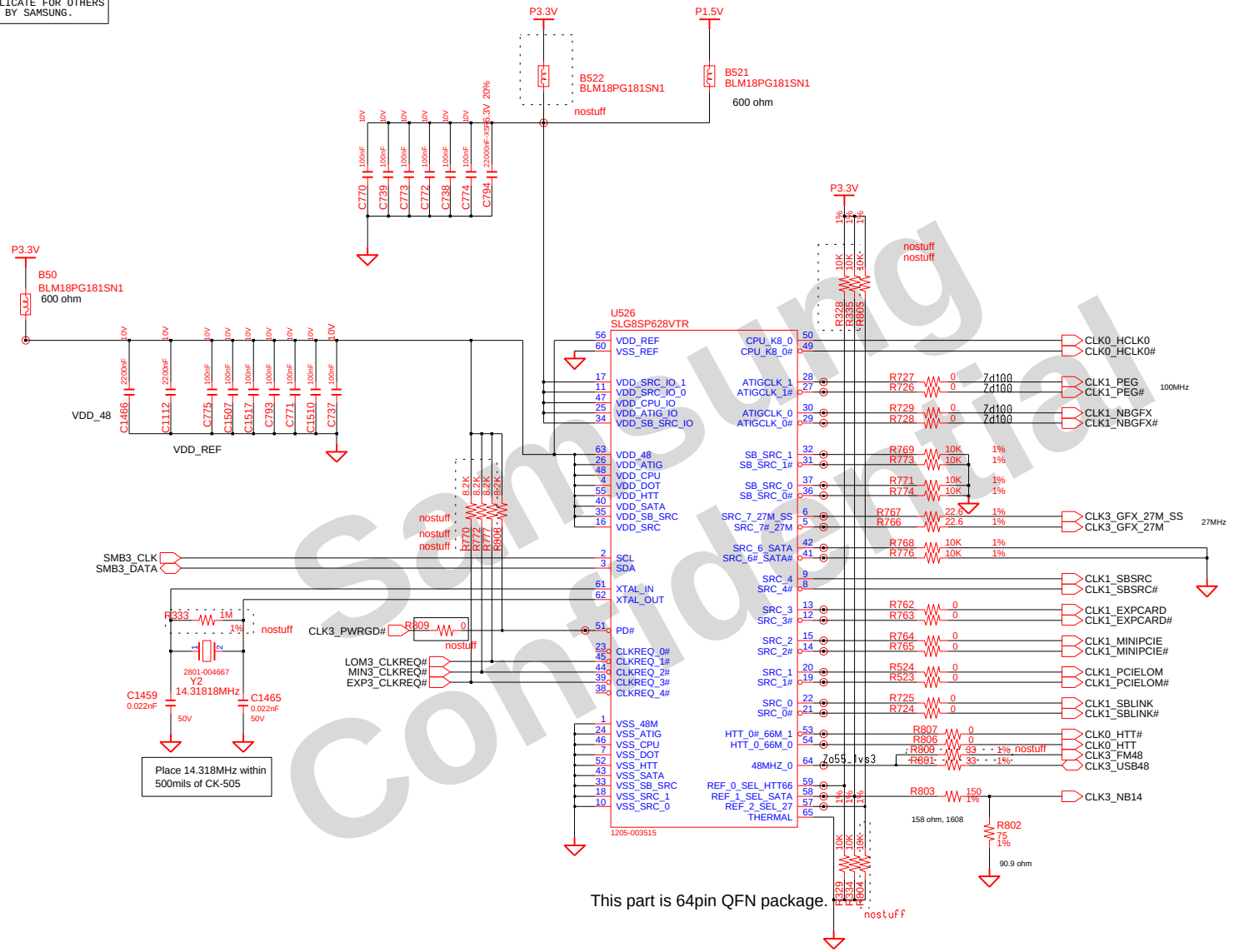
DRAW JM	DATE 1/10/2008	TITLE Cambridge	SAMSUNG ELECTRONICS
CHECK YJ	DEV. STEP PR	SB700 (4/4)	
APPROVAL BJ	REV 1.0		PART NO. BA41-009xxA
MODULE CODE	LAST EDIT August 24, 2008 14:34:27 PM	PAGE 27 OF 47	





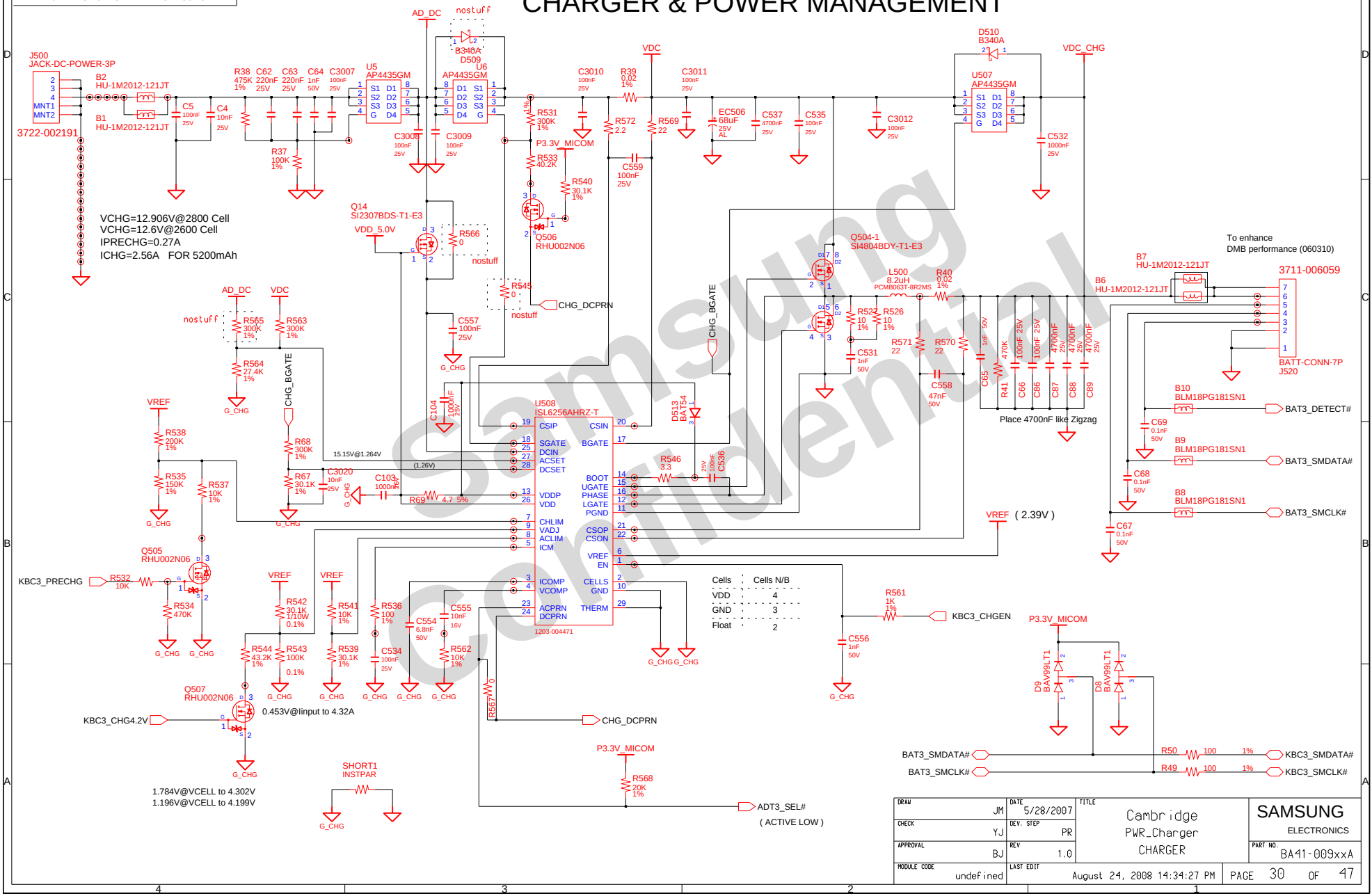


DRAW: JM	DATE: 1/10/2008	TITLE: Cambridge	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0	Strap	PART NO.: BA41-009xxA
MODULE CODE: undefined	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 28 OF 47	



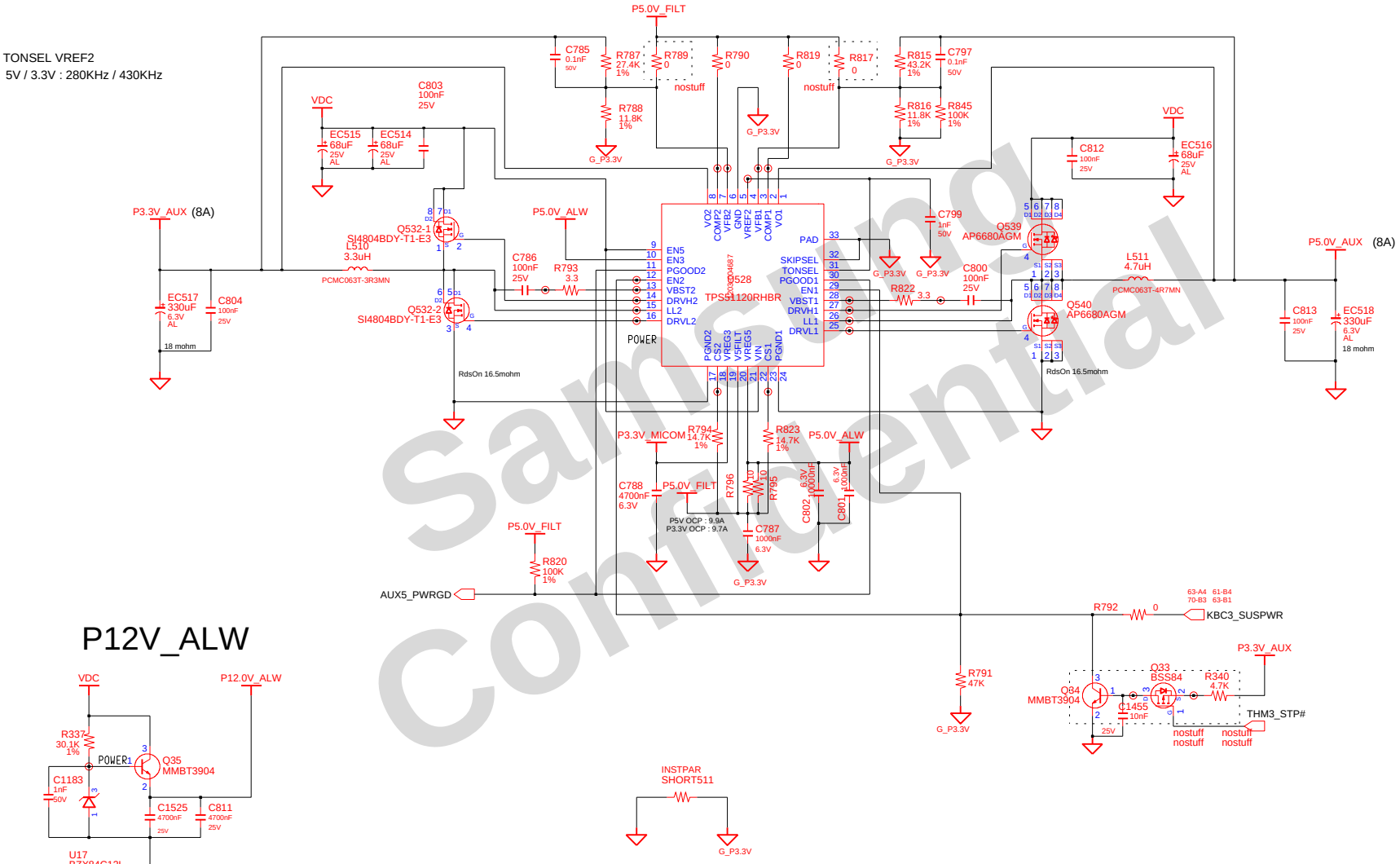
DRAW: JM	DATE: 1/10/2008	TITLE: Cambridge Main_Clock_Circuit CK for AMD CPU	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE: undefined	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 29 OF 47	

CHARGER & POWER MANAGEMENT



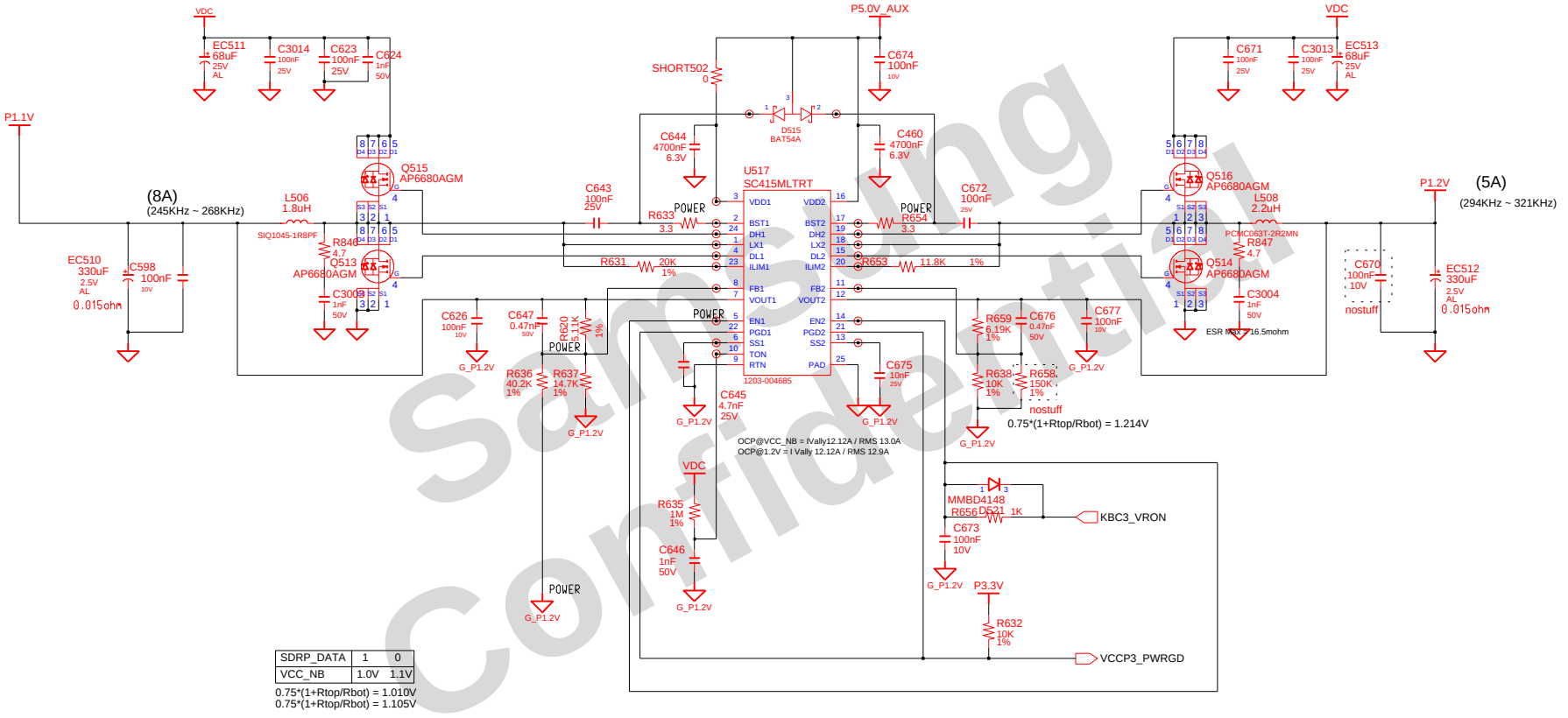
DRAW: JM	DATE: 5/28/2007	TITLE: Cambridge PWR_Charger CHARGER	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE: undefined	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 30 OF 47	

P3.3V_AUX & P5.0V_AUX



DRAW: JM	DATE: 11/8/2006	TITLE: Cambridge PWR_MV_3V_5V P3.3V_AUX / P5.0V_AUX	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE: undefined	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 31 OF 47	

CHIPSET POWER(P1.2V)



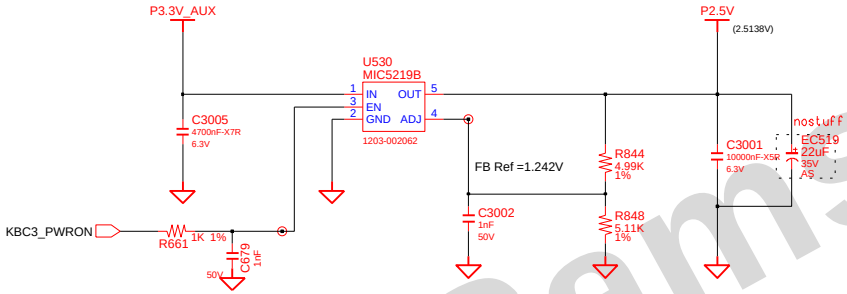
SDRP_DATA	1	0
VCC_NB	1.0V	1.1V

0.75*(1+Rtop/Rbot) = 1.010V
0.75*(1+Rtop/Rbot) = 1.105V

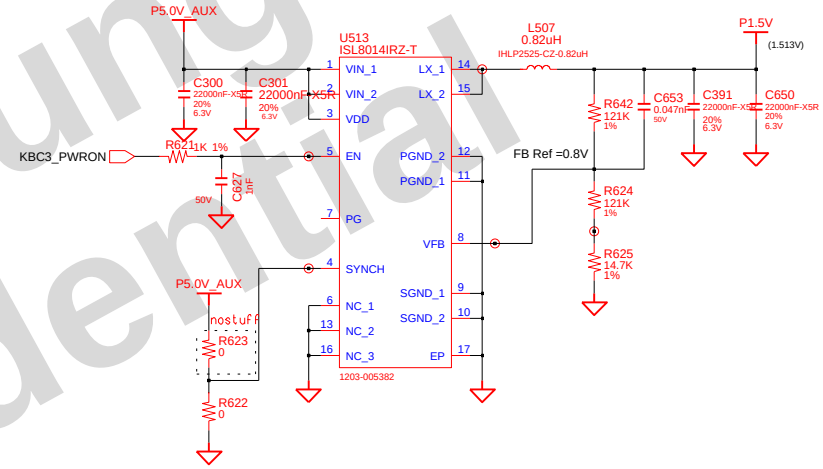
DRAW: JM	DATE: 8/14/2007	TITLE: Cambridge PWR_MV_Cantiga Chipset Power (P1.05V_M,P1.2V)	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE: undefined	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 32 OF 47	

CHIPSET POWER(P2.5V & P1.5V)

P2.5V

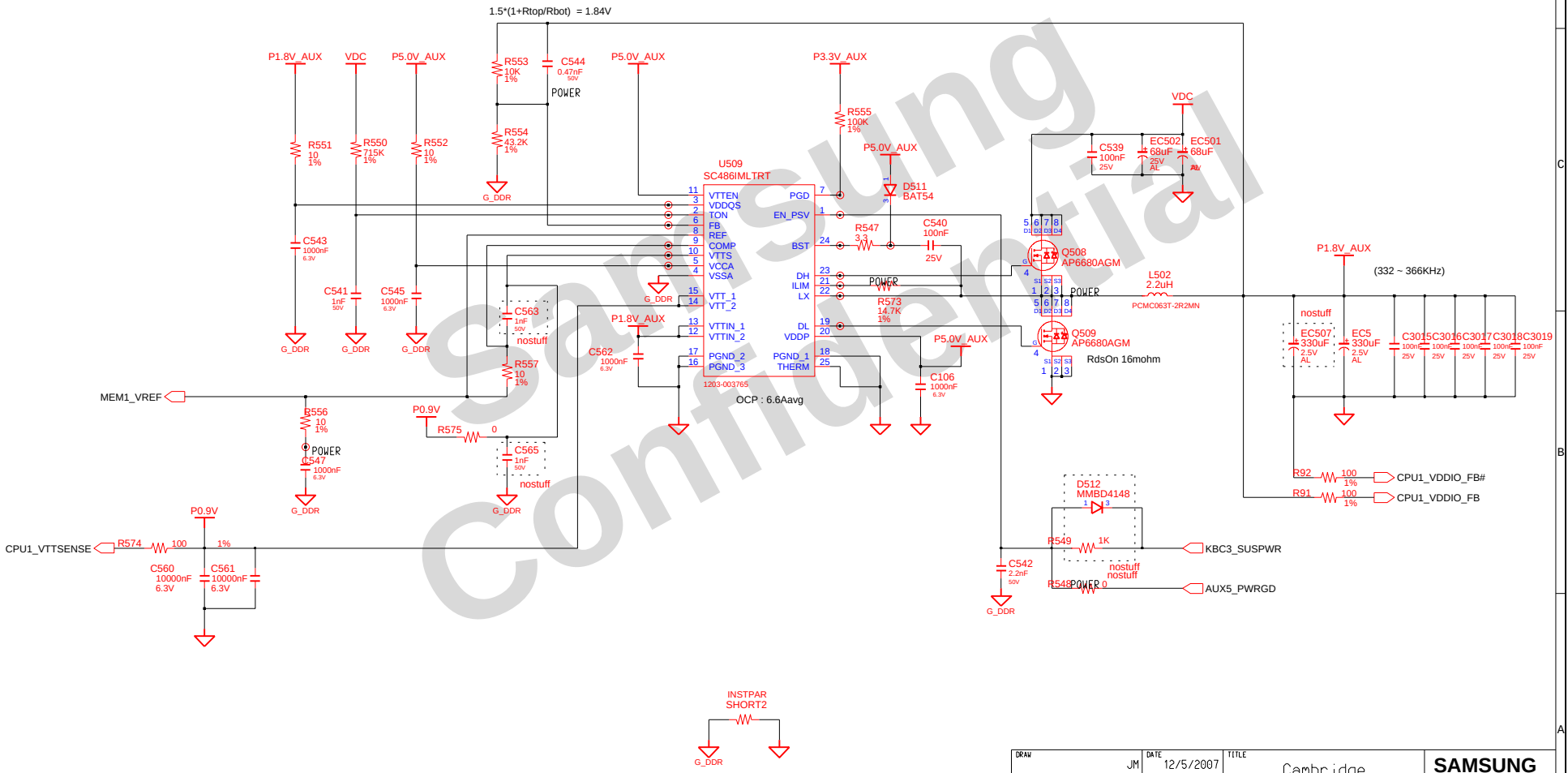


P1.5V



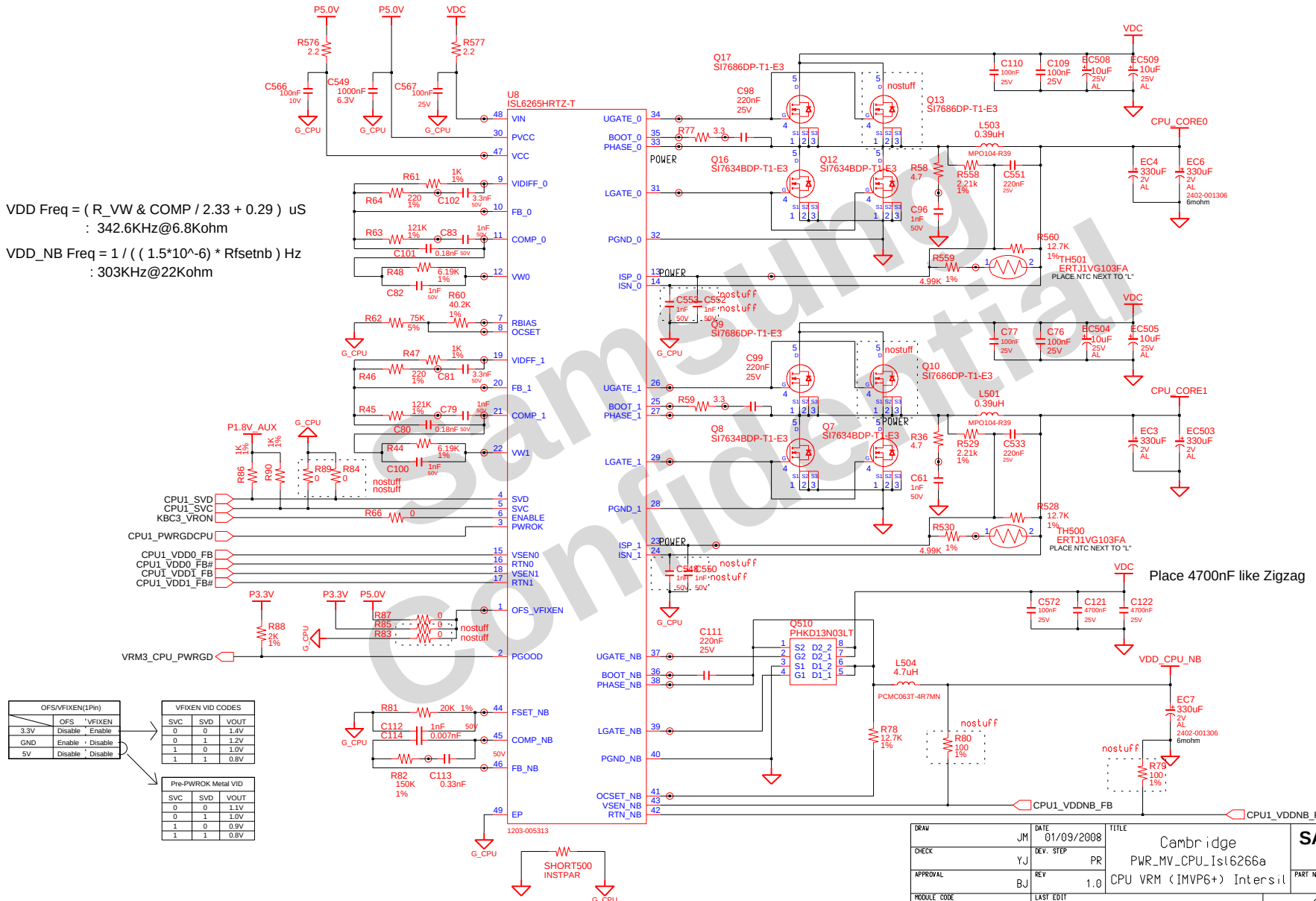
DRAW: JM	DATE: 8/14/2007	TITLE: Cambridge PWR_MV_Cantiga Chipset Power (P1.05V_M,P1.2V)	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE: undefined	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 33 OF 47	

DDR2 Power



DRAW: JM	DATE: 12/5/2007	TITLE: Cambridge SC486 DDR2 POWER	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE: undefined	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 34 OF 47	

CPU VRM [INTERSIL]



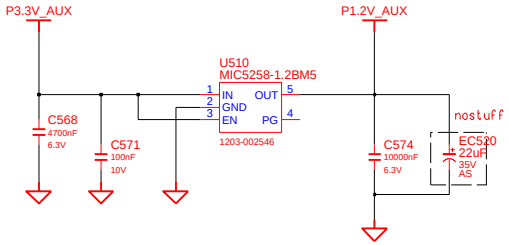
OFS/VFIXEN(1Pin)	OFS	VFIXEN
3.3V	Disable	Enable
GND	Enable	Disable
5V	Disable	Disable

VFIXEN VID CODES		
SVC	SVD	VOUT
0	0	1.4V
0	1	1.2V
1	0	1.0V
1	1	0.8V

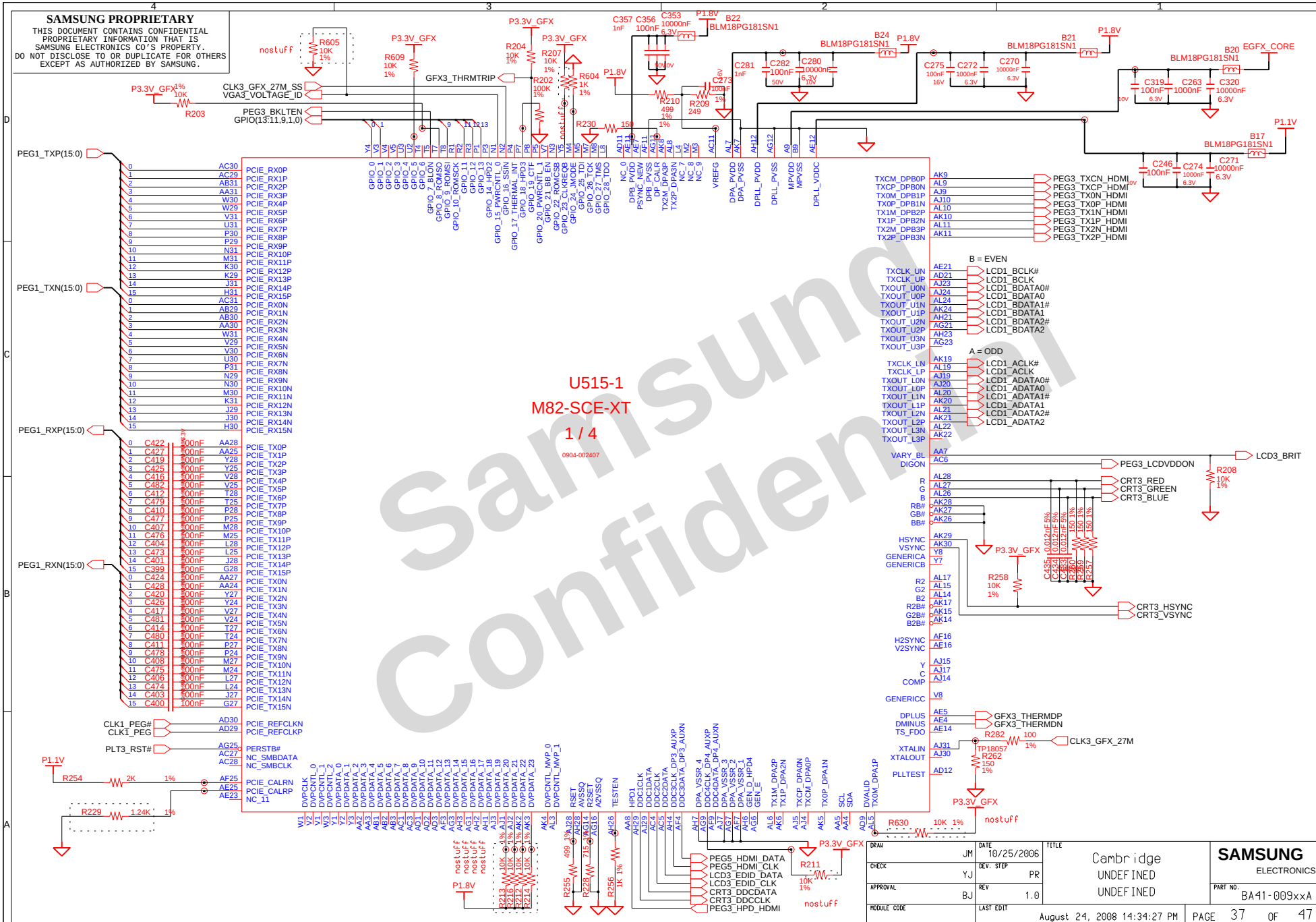
Pre-PWROK Metal VID		
SVC	SVD	VOUT
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

DRAW	JM	DATE 01/09/2008	TITLE Cambridge PWR_MV_CPU_Isl6266a CPU VRM (IMVP6+) Intersil
CHECK	YJ	DEV. STEP PR	SAMSUNG ELECTRONICS
APPROVAL	BJ	REV 1.0	PART NO. BA41-009xxA
MODULE CODE	undefined	LAST EDIT August 24, 2008 14:34:27 PM	PAGE 35 OF 47

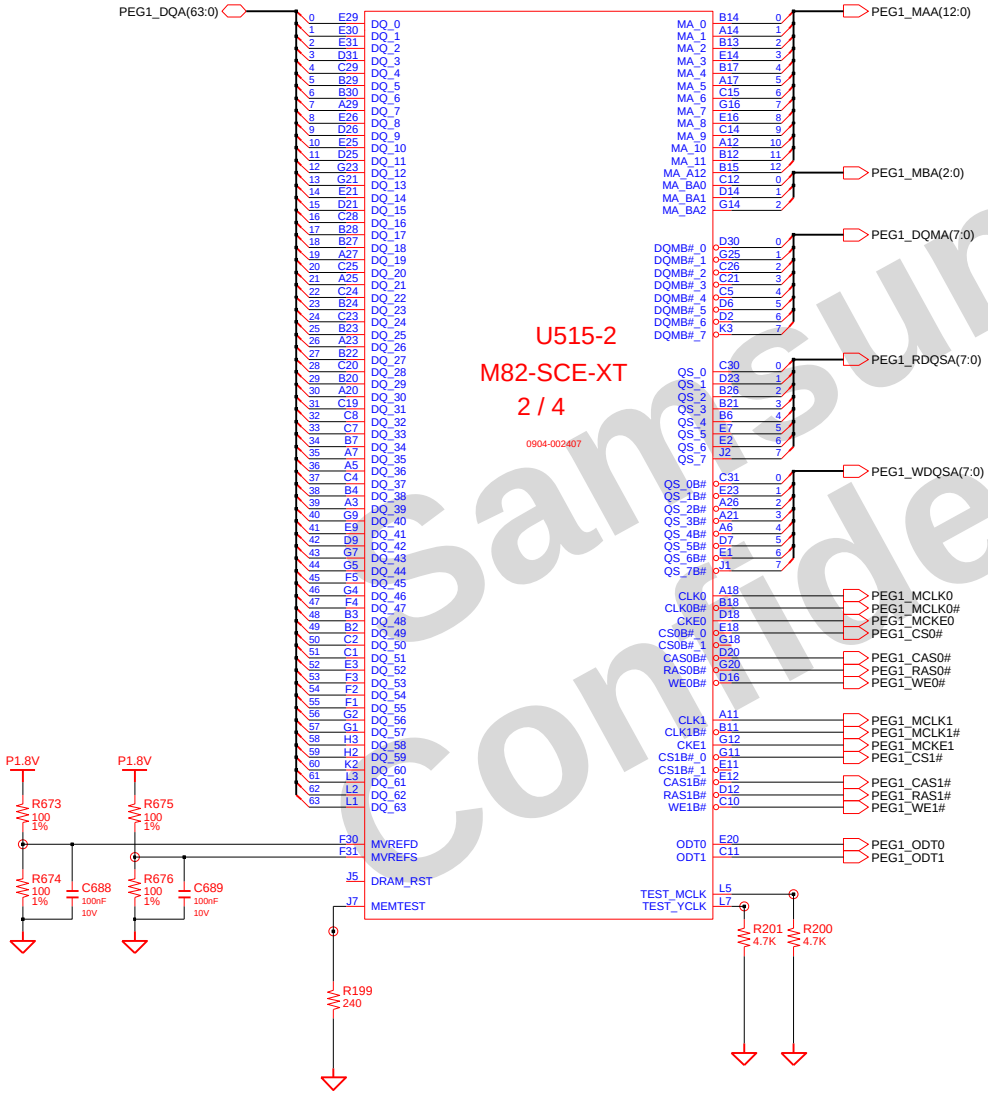
P1.2V_AUX



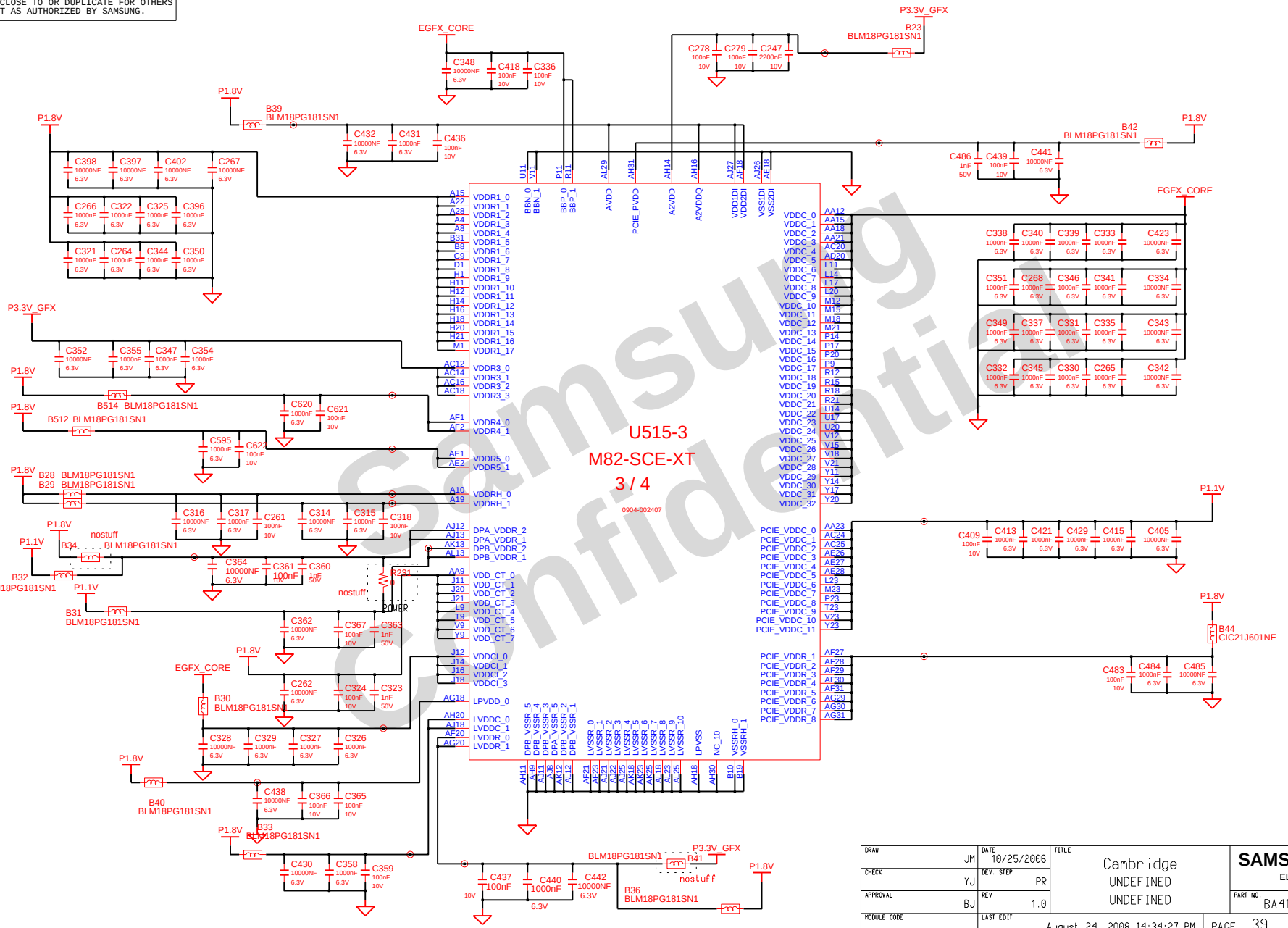
DRAW: JM	DATE: 2/13/2008	TITLE: Cambridge Evaluation Board P1.8V_AUX, P1.5V	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE:	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 36 OF 47	



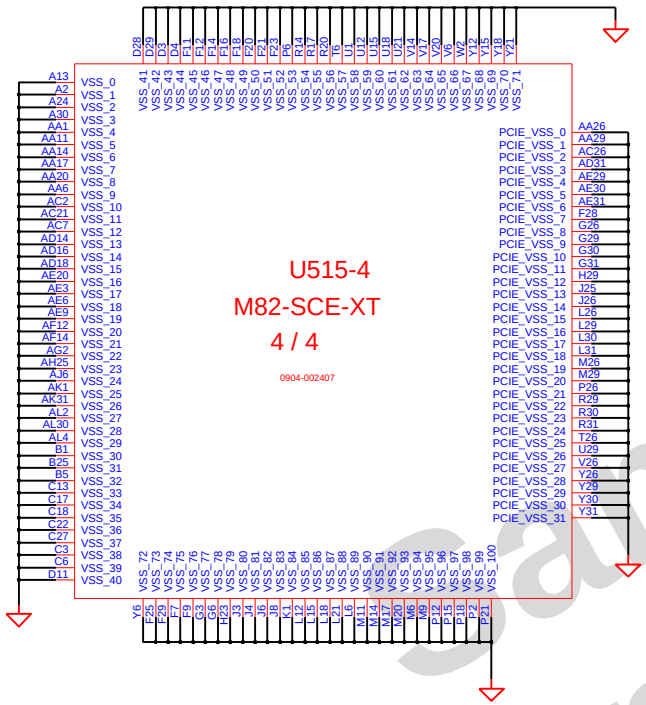
DRAW	JM	DATE 10/25/2006	TITLE Cambridge UNDEFINED UNDEFINED
CHECK	YJ	DEV. STEP PR	SAMSUNG ELECTRONICS
APPROVAL	BJ	REV 1.0	PART NO. BA41-009xxA
MODULE CODE		LAST EDIT August 24, 2008 14:34:27 PM	PAGE 37 OF 47

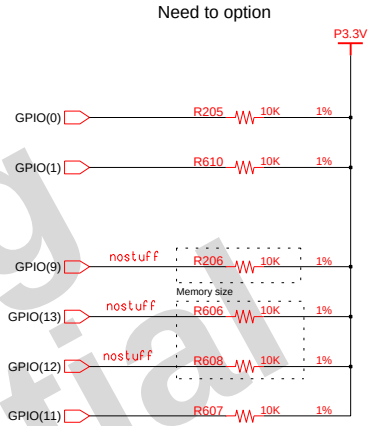


DRAW: JM	DATE: 10/25/2006	TITLE: Cambridge UNDEFINED UNDEFINED	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE:	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 38 OF 47	



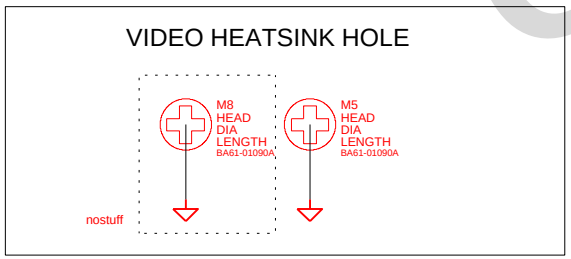
DRAW JM	DATE 10/25/2006	TITLE Cambridge UNDEFINED UNDEFINED	SAMSUNG ELECTRONICS
CHECK YJ	DEV. STEP PR		
APPROVAL BJ	REV 1.0		PART NO. BA41-009xxA
MODULE CODE	LAST EDIT August 24, 2008 14:34:27 PM	PAGE 39 OF 47	





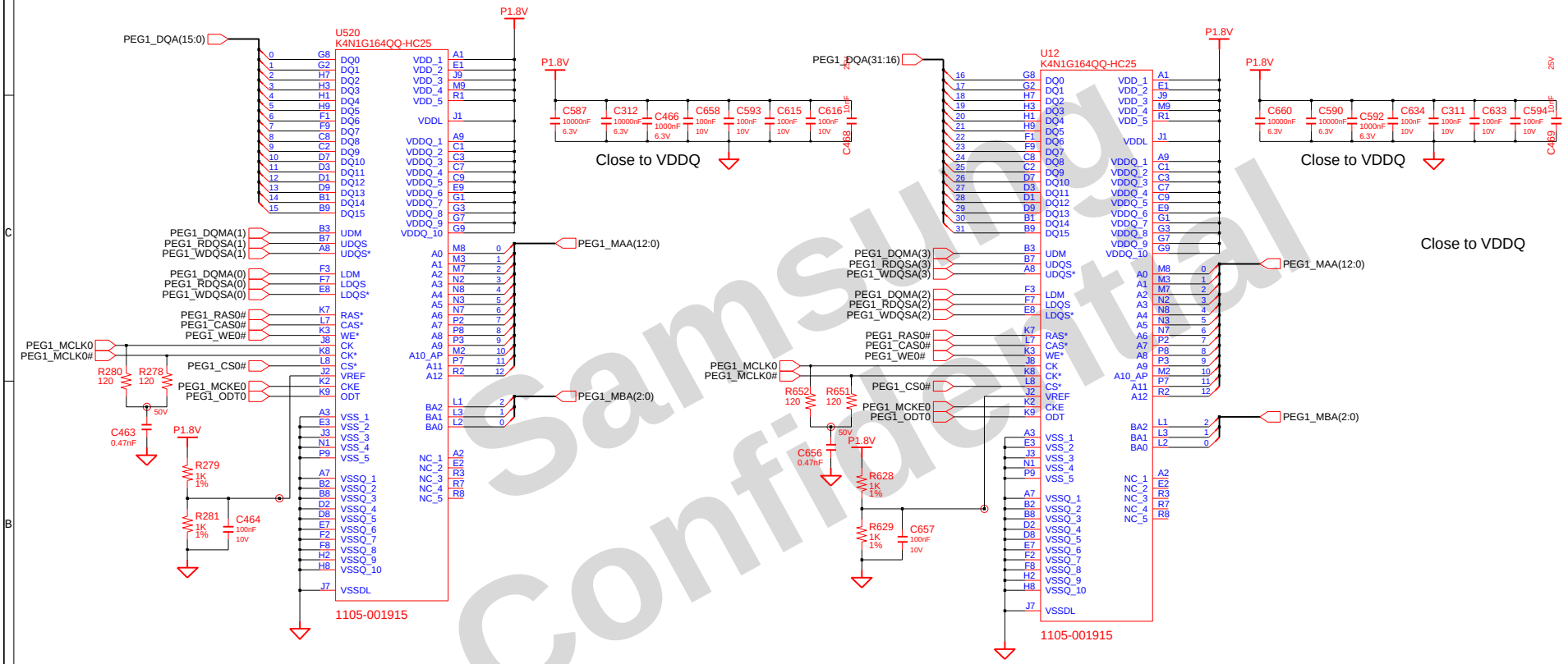
(DEFAULT : pull-down)

STRAP	PIN	DESCRIPTION
TX_PWRS_ENB	GPIO[0]	Transmitter Power Saving Enable 0: 50% Tx output swing 1: full Tx output swing
TX_DEEMPH_EN	GPIO[1]	Transmitter De-emphasis Enable 0: Tx De-emphasis disabled 1: Tx de-emphasis enabled
DEBUG_ACCESS	GPIO[4]	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible.
ROMIDCFG[3:0]	GPIO[9,13:11]	When no ROM is attached, GPIO[9] is set to 0. GPIO[13:12] is used to select the frame buffer aperture size. GPIO[13:12] = 00: 128M frame buffer GPIO[13:12] = 01: 256M frame buffer GPIO[13:12] = 10: 64M frame buffer GPIO[13:12] = 11: reserved



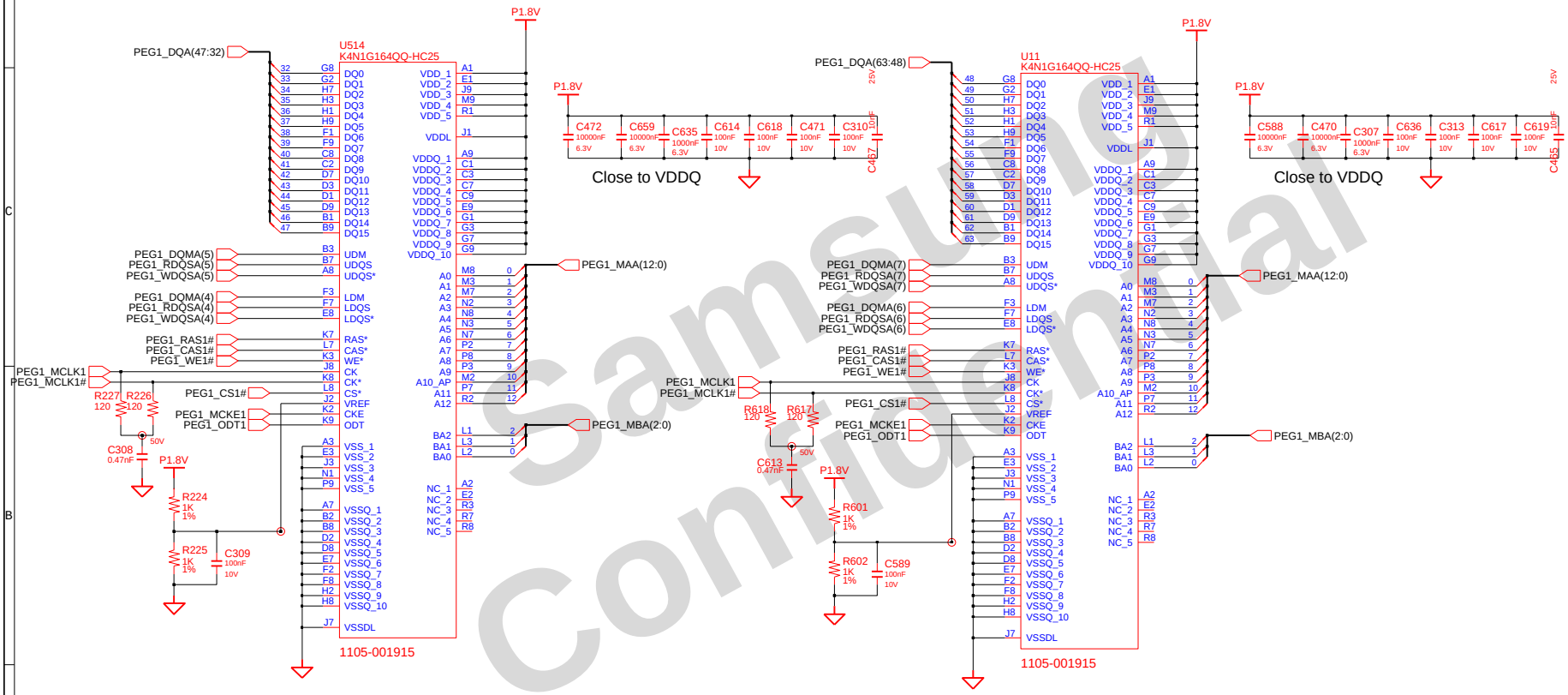
DRAW JM	DATE 10/25/2006	TITLE Cambridge UNDEFINED UNDEFINED	SAMSUNG ELECTRONICS
CHECK YJ	DEV. STEP PR		
APPROVAL BJ	REV 1.0		PART NO. BA41-009xxA
MODULE CODE	LAST EDIT August 24, 2008 14:34:27 PM	PAGE 40 OF 47	

LOWER SUB PARTITION



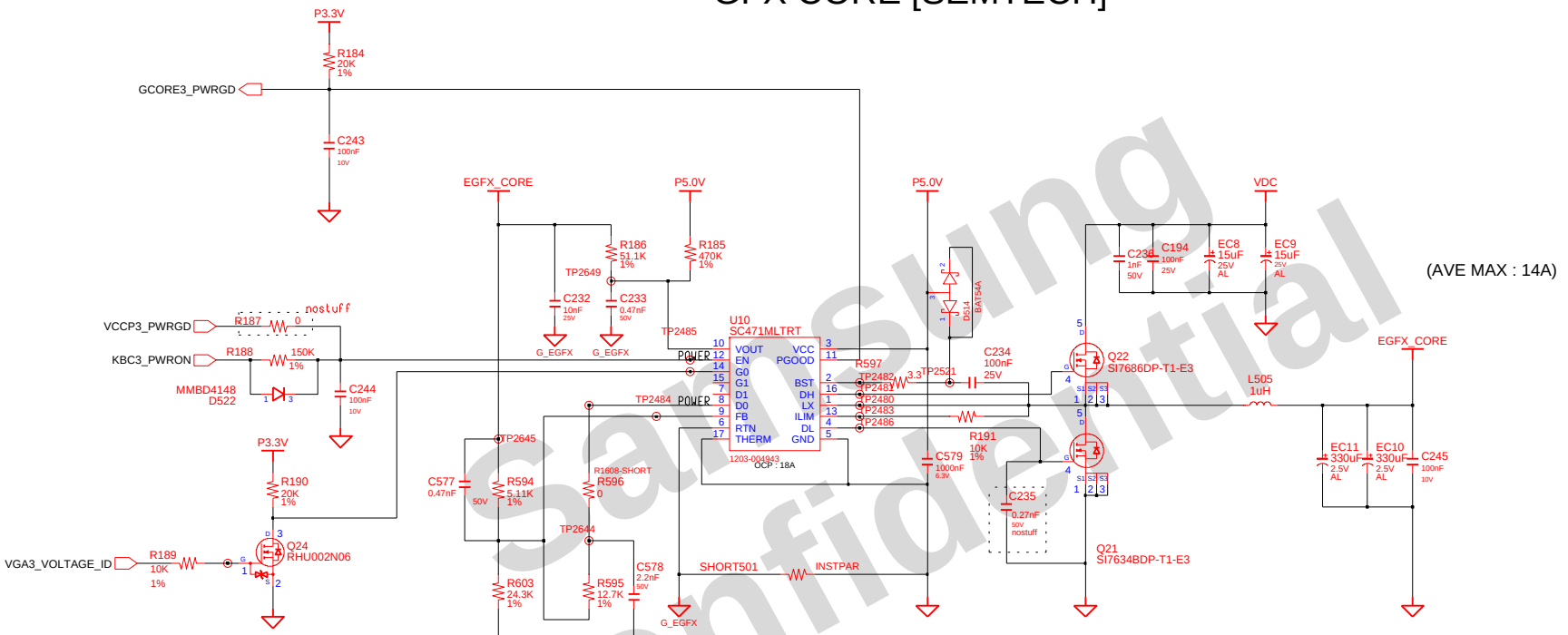
DRAW: JM	DATE: 8/12/2006	TITLE: Cambridge Graphics_Memory(GDDR2) Graphics_Memory_Nvidia #1	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE:	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 41 OF 47	

UPPER SUB PARTITION



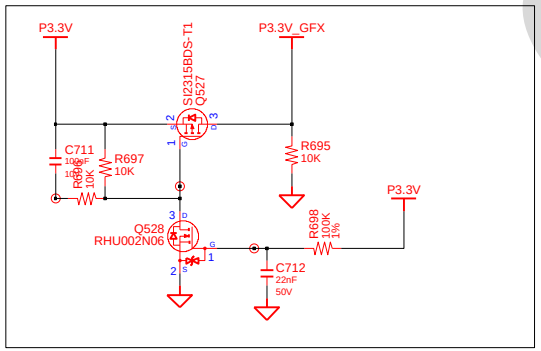
DRAW: JM	DATE: 8/12/2006	TITLE: Cambridge Graphics_Memory(GDDR2) Graphics_Memory_Nvidia #2	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 42 OF 47	

GFX CORE [SEMTECH]



(AVE MAX : 14A)

P3.3V_GFX CONTROL CIRCUIT



M82-S
- H : 0.9V
- L : 1.0V

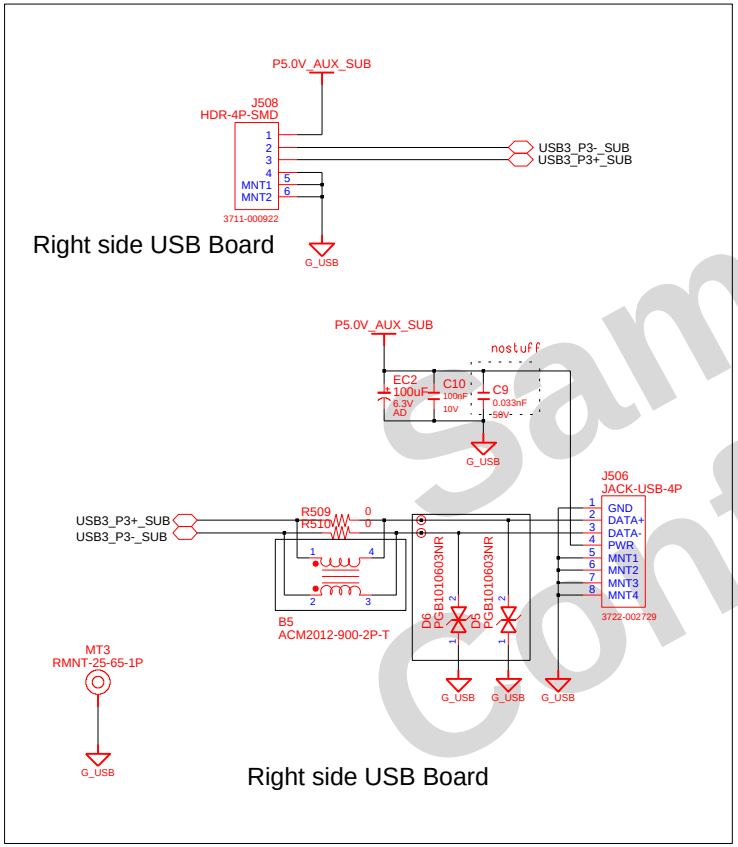
R596 = 27.4K

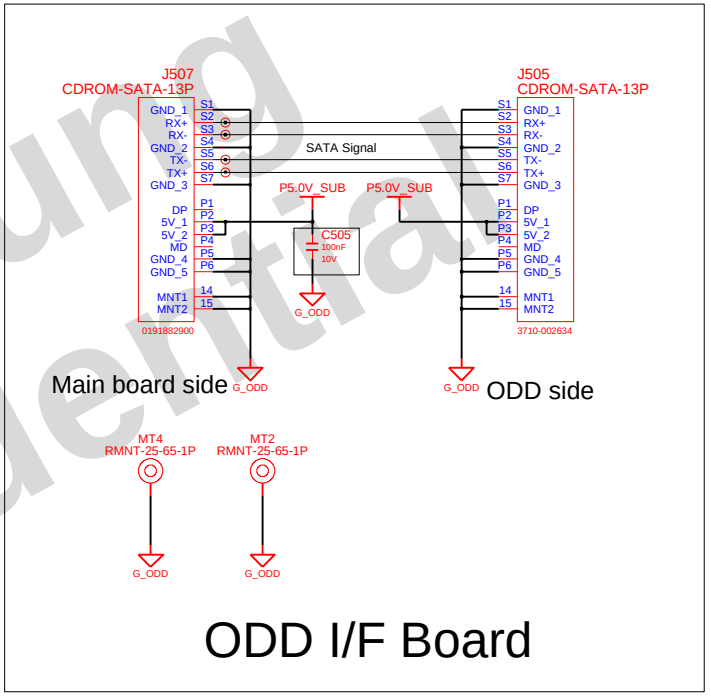
M82-SXT
- H : 0.9V
- L : 1.2V

R596 = 0

DRAW: JM	DATE: 10/26/2006	TITLE: Cambridge UNDEFINED UNDEFINED	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE:	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 43 OF 47	

Sub Board (16" only)





nostuff
nostuff
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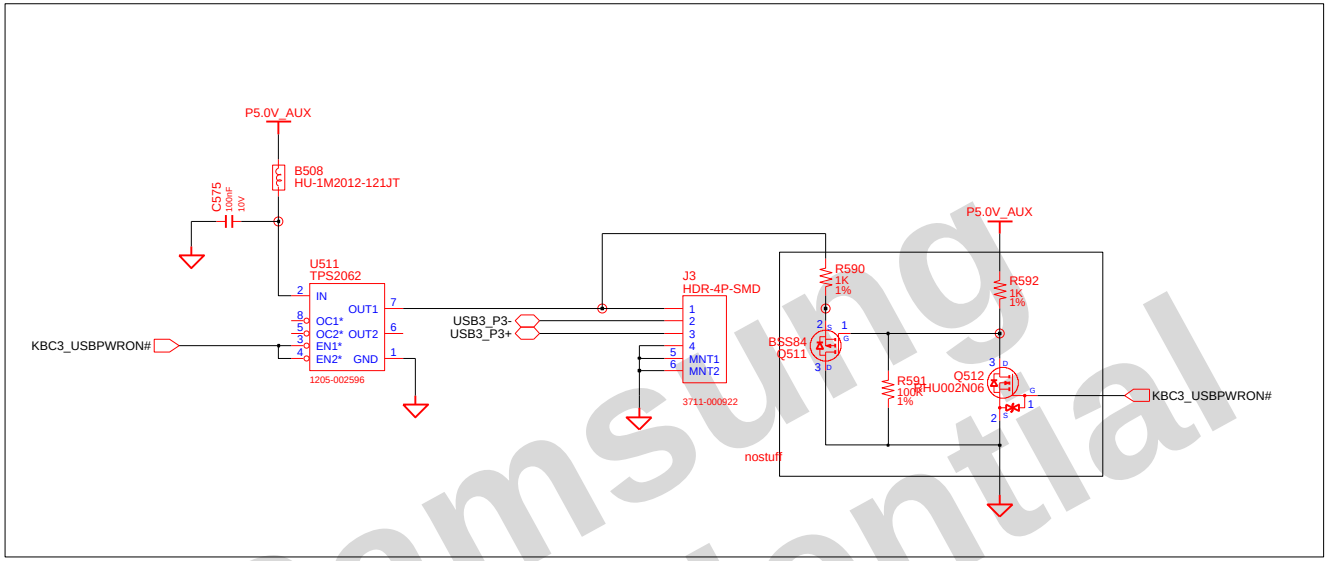
nostuff

DESIGN: JM	DATE: 6/10/2008	TITLE: Cambridge	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE:	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 44 OF 47	

to 4th USB Sub Board Connector (16" Only)



DESIGN: JM	DATE: 6/10/2008	TITLE: Cambridge	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE:	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 45 OF 47	

GPIO(0)
GPIO(1)
GPIO(9)

GPIO(11)
GPIO(12)
GPIO(13)

CHG_BGATE
CHG_DCPRN
CLK3_NB14

LPC3_CLK0
LPC3_CLK1

PCI3_CLK2
PCI3_CLK3
PCI3_CLK4
PCI3_CLK5

PEX3_RST#

CHP3_A_RST#
CHP3_RTCCLK

CLK3_PWRGD#

KBC5_KSI(1)

DBG3_HSYNC
DBG3_VSYNC

G_EGFX
G_P1.2V
P1.2V
P1.8V
P2.5V
P1.2V_AUX
P3.3V_GFX
P5.0V_SUB
P5.0V_AUX_SUB
VDD_5.0V
VDD_CPU_NB
AD_DC
CPU_CORE0
CPU_CORE1
G_ODD
G_USB

PEG3_BKLTEN

VGA3_VOLTAGE_ID

PEG3_HPD_HDMI
PEG3_LCDVDDON

CHP3_NB_PWRGD

CHP3_SB_TEST0
CHP3_SB_TEST2

KBC3_LED_ACIN#
KBC3_NB_PWRGD

PEG5_HDMI_DATA

GCORE3_PWRGD
GFX3_THRMTRIP
GFX3_THERMDN
GFX3_THERMDP

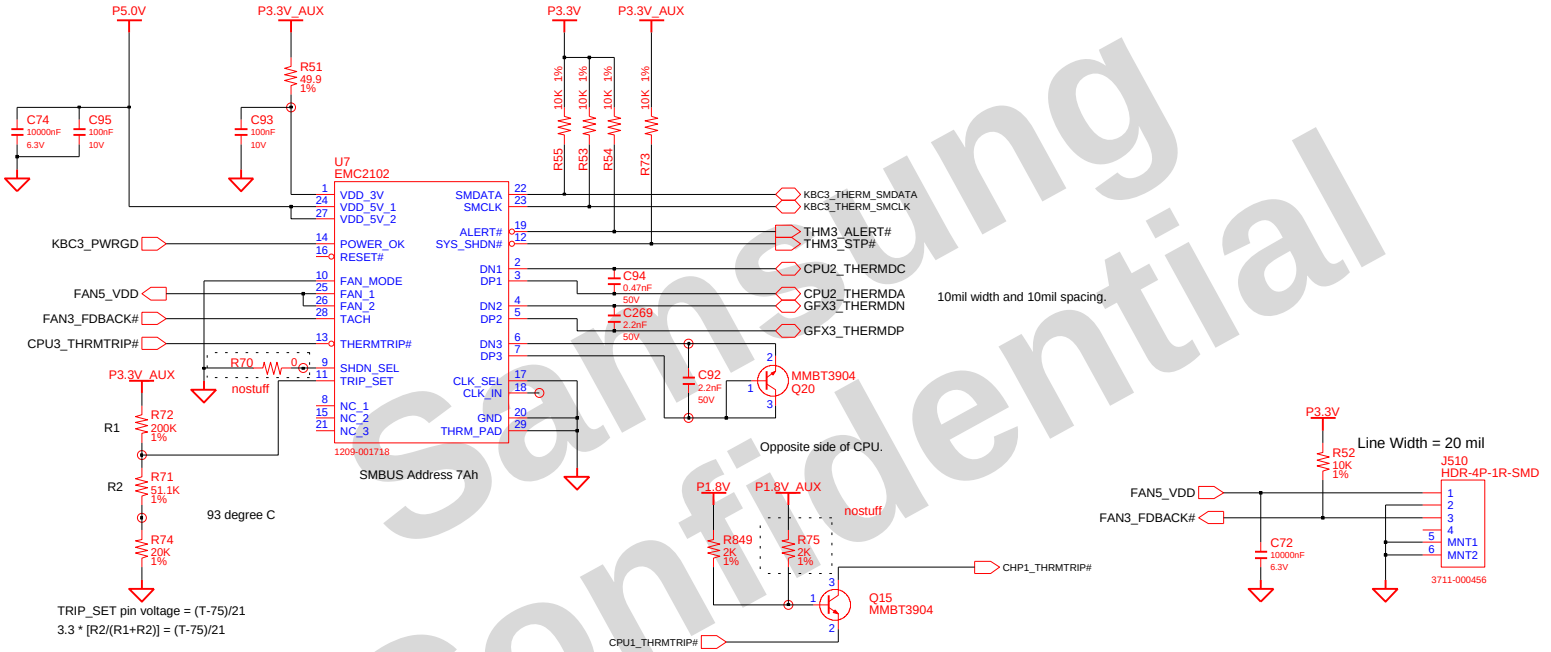
CLK3_GFX_27M_SS

SPI3_GPIO14

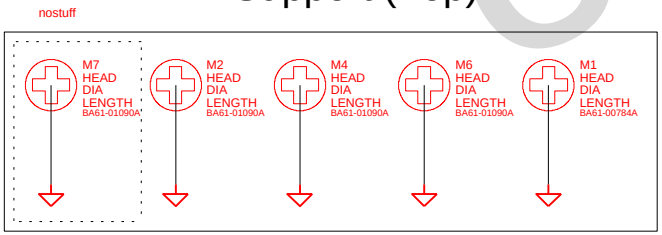
CLK3_GFX_27M

DESIGN: JM	DATE: 6/27/2008	TITLE: Cambridge	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE:	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 46 OF 47	

THERMAL SENSOR & FAN CONTROL



RHE Support (Top)

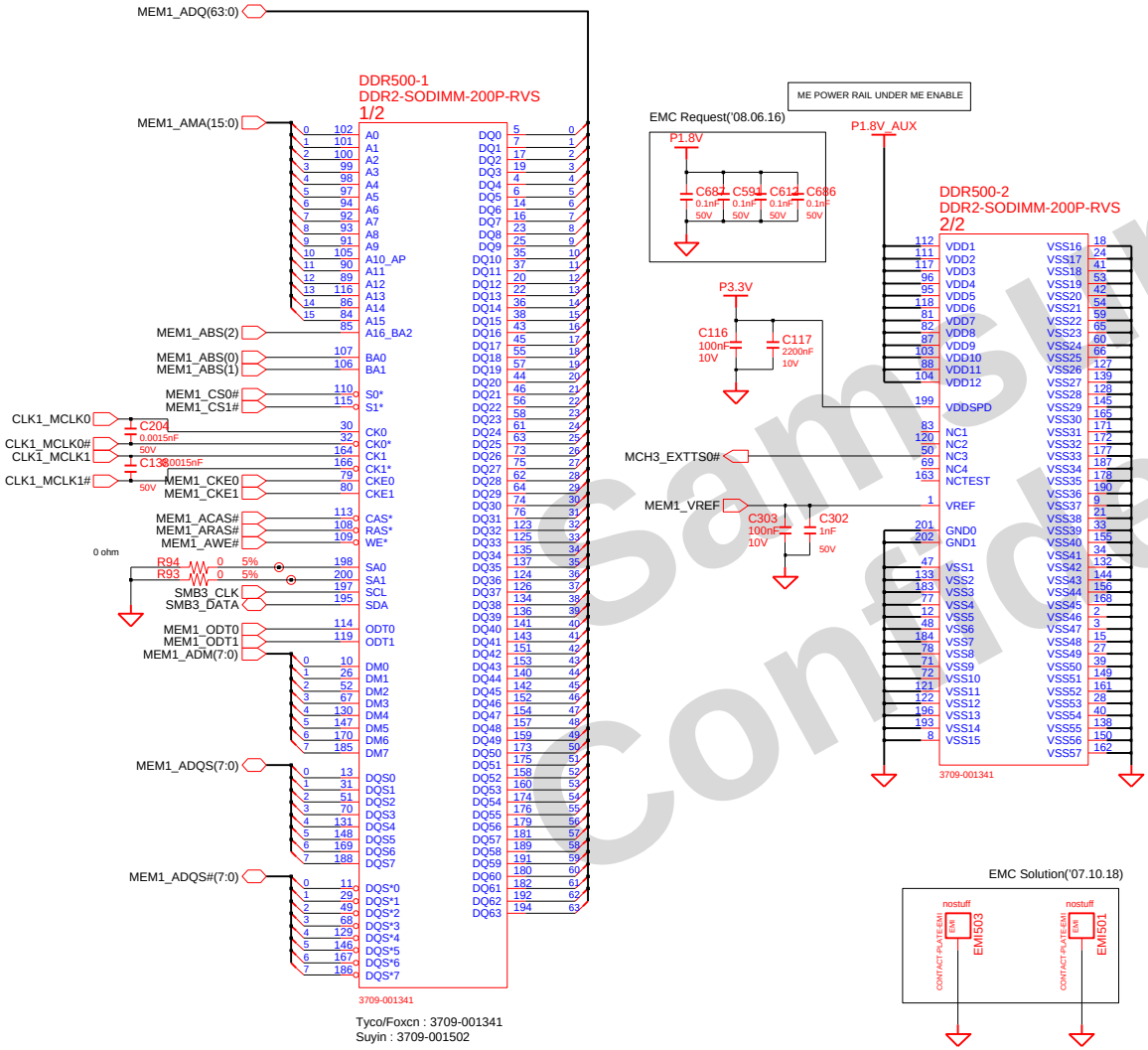


SB thermal plate

DRAW: JM	DATE: 1/10/2008	TITLE: Cambridge	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR	Thermal_Sensor_SMSC_Emc2102	
APPROVAL: BJ	REV: 1.0	Thermal_Sensor_SMSC_Emc2102	PART NO.: BA41-009xxA
MODULE CODE	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 68 OF 64	

DDR SO-DIMM #0

Height : 5.2mm (Reverse)

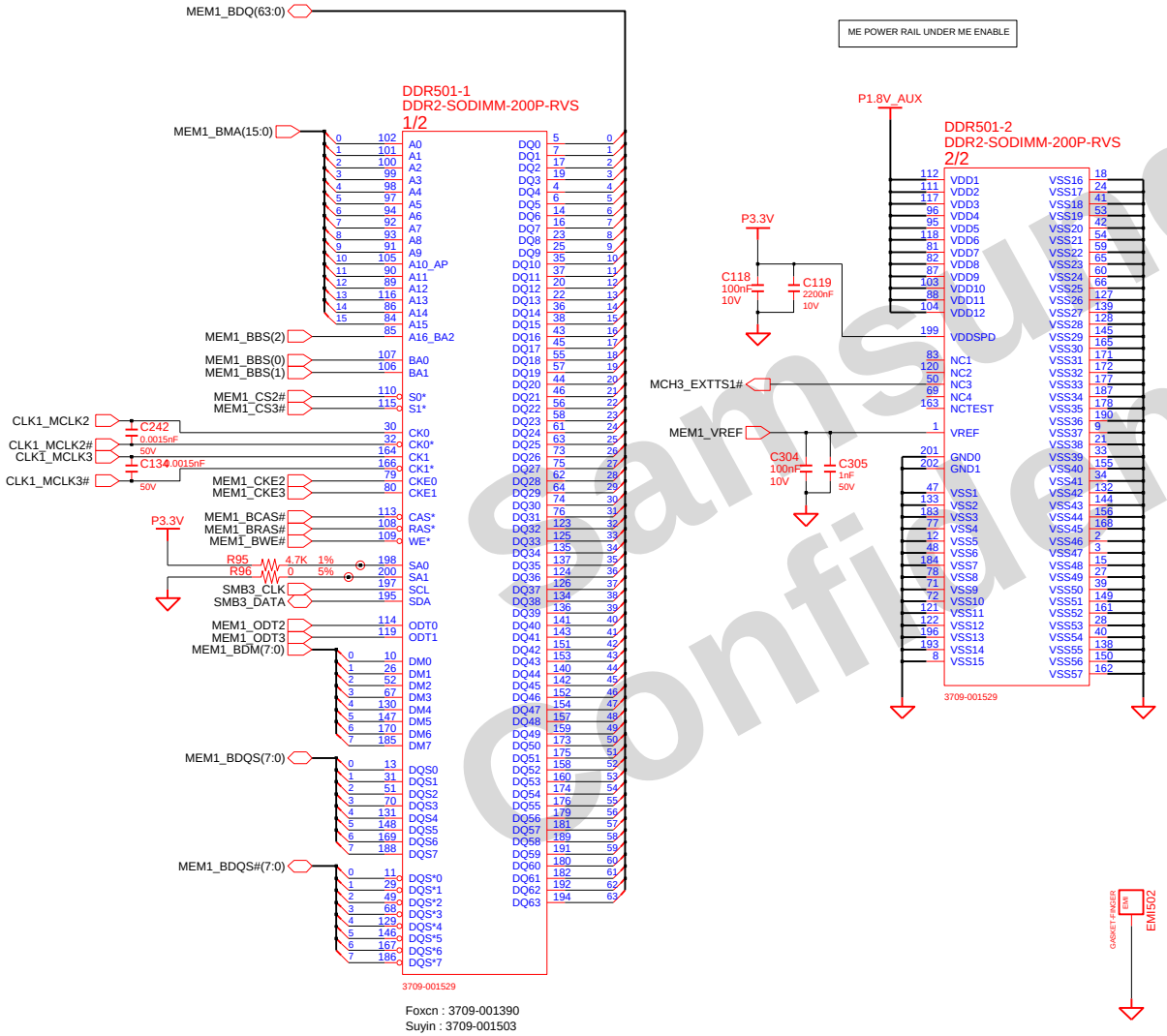


Tyco/Foxcn : 3709-001341
Suyin : 3709-001502

DRAW: JM	DATE: 1/10/2008	TITLE: Cambridge SODIMM_DDR2 SODIMM_DDR2 #1	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE:	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 64 OF 64	

DDR SO-DIMM #1

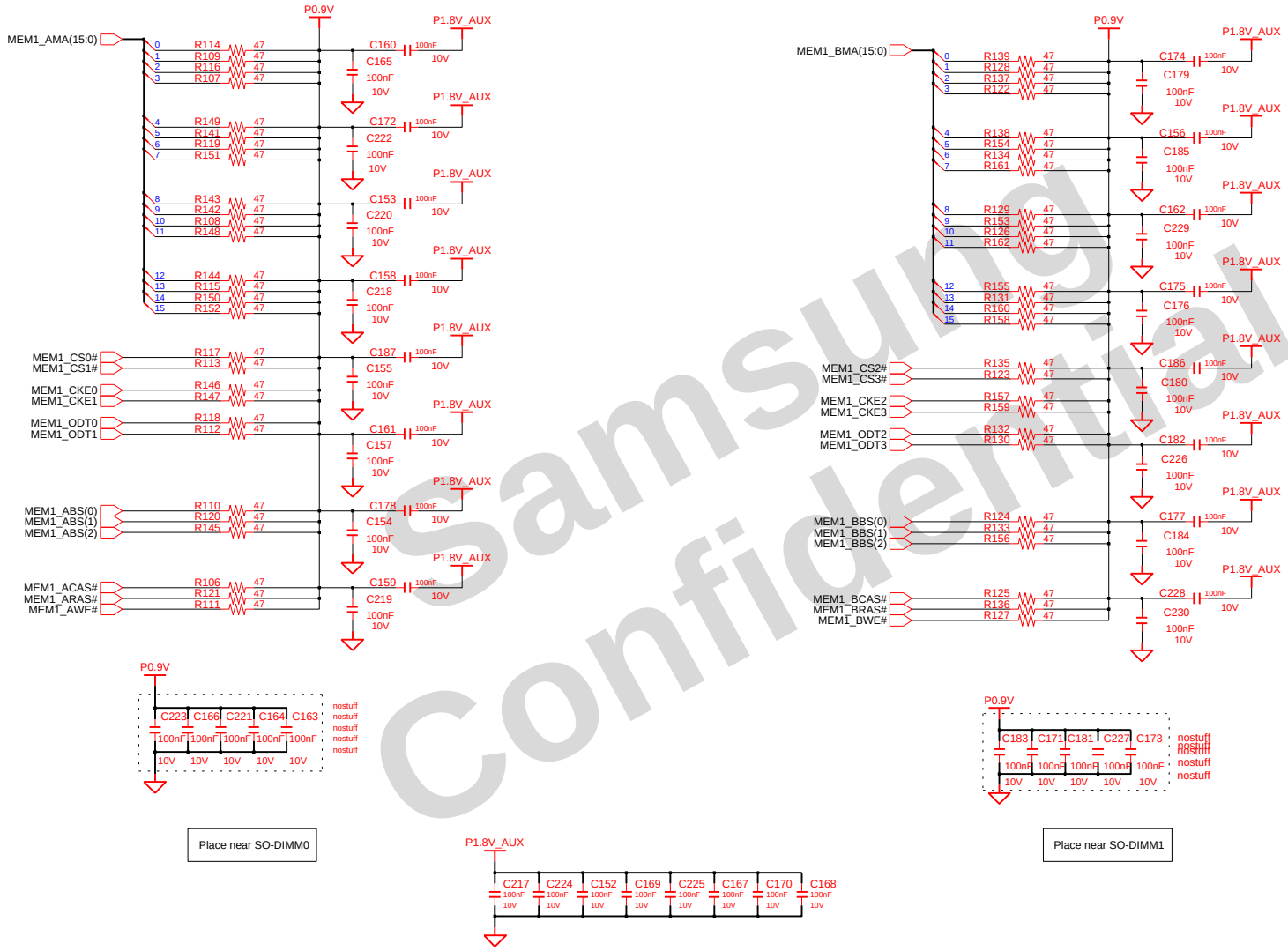
Height : 9.2mm (Reverse)



Foxcn : 3709-001390
Suyin : 3709-001503

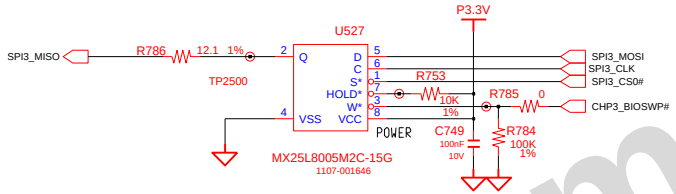
ME POWER RAIL UNDER ME ENABLE

DRAW: JM	DATE: 1/10/2008	TITLE: Cambridge SODIMM_DDR2 SODIMM_DDR2 #2	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE:	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 65 OF 64	



DRAW: JM	DATE: 1/10/2008	TITLE: Cambridge SODIMM_DDR2 SODIMM_DDR2 #3	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE:	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 66 OF 64	

- SPI ROM LIST -

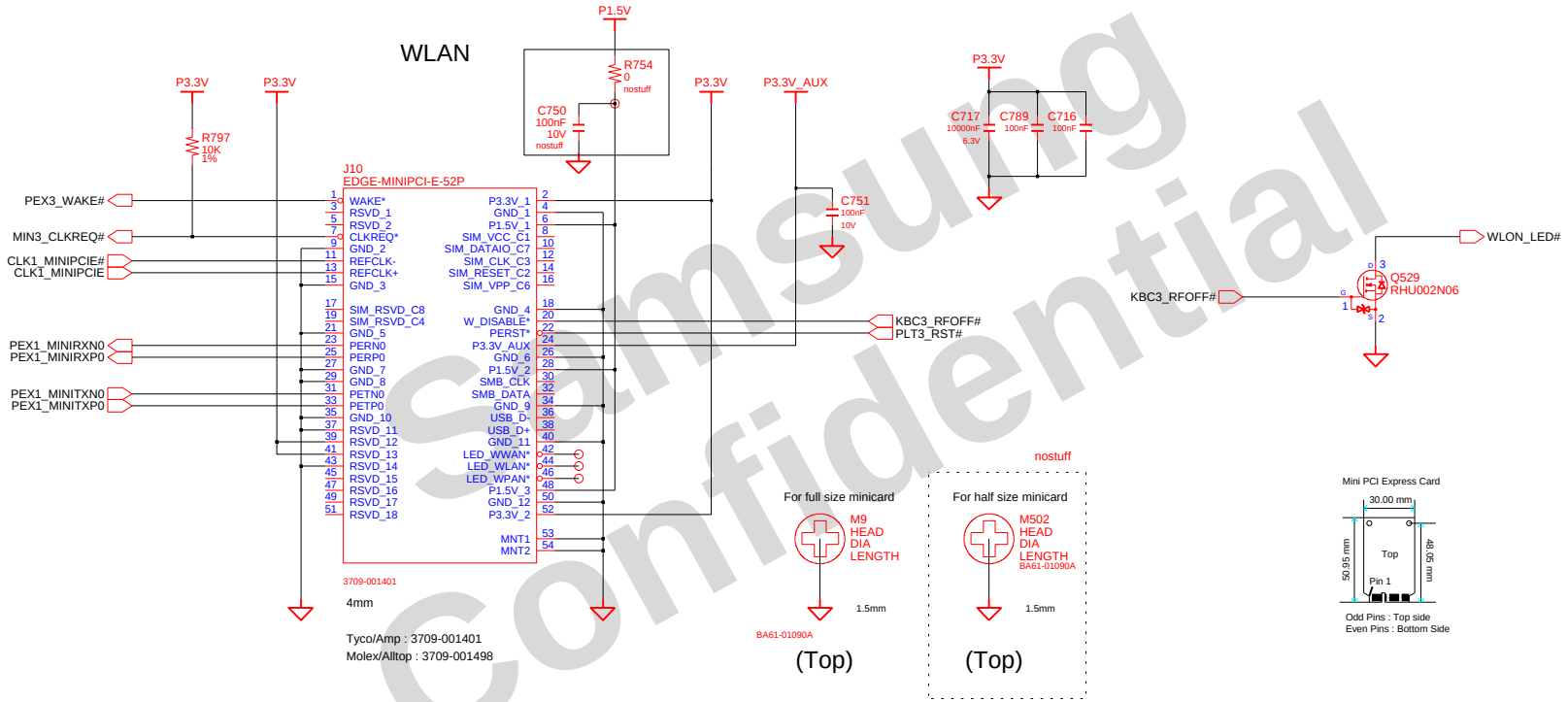


1MB(8Mbit)

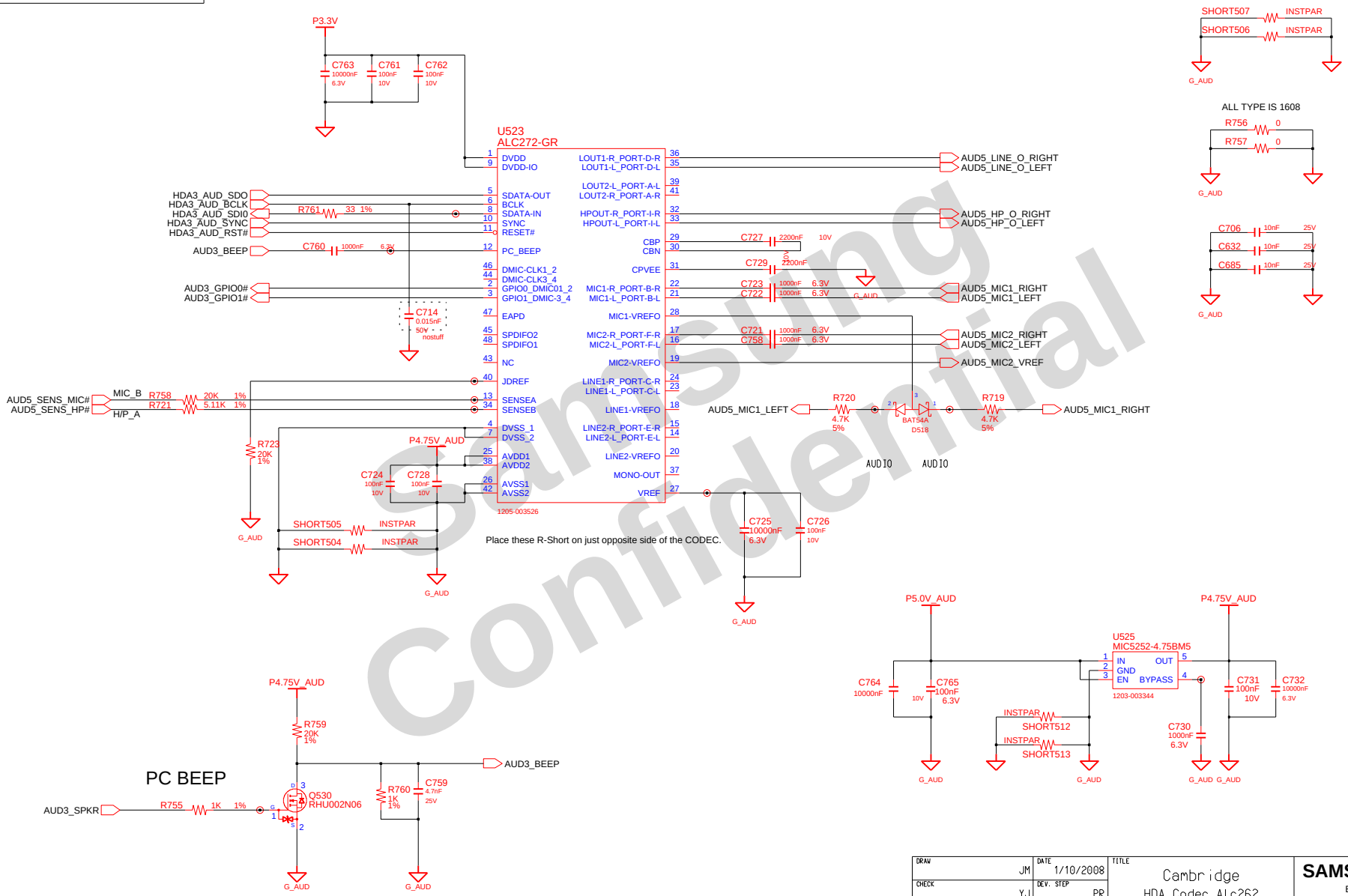
02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT. SYSTEM H/W	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU.REG	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD EERROR
0C	INIT.CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
OE	INIT. I/O VALUE	7E	TEST COPROCESSER IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGER	82	DETECT AND INSTALL EXT.RS232C
11	LOAD ALTERNATE REG.	84	DETECT AND INSTALL EXT.PARALLEL
13	PCI BUS MASTER RESET WITH INITIAL POST VALUE	86	RE-INIT. ON-BOARD I/O PORT
		88	INIT. BIOS DATA ROM
14	INIT. KEYBOARD CONTROLLER	8A	INIT.EXTENDED BIOS DATA AREA
16	CHECK CHECKSUM	8C	INIT. FDD CONTROLLER
18	8254 TIMER INIT.	9A	SHADOW OPTION ROMS
1A	8237 DMA CONTROLLER INIT.	9C	SETUP POWER MANAGEMENT
1C	RESET INTERRUP CONTROLLER	9E	ENABLE H/W INTERRUPT
20	TEST DRAM REFRESH	A0	SET TIME OF DAY
22	TEST 8742 KEYBOARD CONTROLLER	A4	INIT. TYPEMATIC RATE
24	SET ES SEGMENT REG. TO 4GB	A8	ERASE F2 PROMPT
26	ENABLE A20	AA	SCAN FOR F2 KEY STROKE
28	AUTO SIZING DRAM	AC	ENTER SETUP
32	COMPUTE THE CPU SPEED	AE	CLEAR IN POST FLAG
34	TESET CMOS RAM	B0	CHECK FOR ERRORS
38	SHADOW SYSTEM BIOS ROM	B2	POST DONE-PREPARE TO BOOT O/S
3A	AUTO SIZING CACHE	B4	ONE BEEP
3C	CONFIGURE ADVANCED CHIPSET REG.	B6	CHECK PASSWORD (OPTION)
3D	LOAD ALTER REG. WITH CMOS VALUE	B7	ACPI INIT
42	INIT. INTERRUPT VECTOR	BA	DMI INIT
44	INIT. BIOS INTERRUPT	BE	CLEAR SCREEN
46	CHECK ROM COPYRIGHT NOTICE	C0	TRY BOOT WITH INT19
47	INIT. I20 SUPPORT IF INSTALLED	D0	INTERRUPT HANDLER ERROR
48	CHECK VIDEO CONFIGURE AGAINST CMOS	D2	UNKNOWN INTERRUPT ERROR
49	INIT. PCI BUS AND DEVICE	D4	PENDING INTERRUPT ERROR
4A	INIT. ALL VIDEO BIOS ROM	D6	SHUTDOWN 5
4C	SHADOW VIDEO BIOS ROM	D8	SHUTDOWN ERROR
50	DISPLAY CPU TYPE AND SPEED	DA	EXTENDED BLOCK MOVE
52	TEST KEYBOARD	DC	SHUTDOWN 10
54	SET KEYCLICK IF ENABLED	89	ENABLE NMI
56	ENABLE KEYBOARD	90	INIT. HDD CONTROLLER
58	TEST FOR UNEXPECTED INTERRUPTS	91	INIT. LOCAL BUS HDD CONTROLLER
5A	DISPLAY " PRESS ..... SETUP"	92	JUMP TO USER PATCH 2
5C	TEST RAM GETWEEN 512K AND 640K	94	DISABLE A20 ADDRESS LINE
60	TEST EXTENDED MEMORY	96	CLEAR HUGE ES SEGMENT REG.
62	TEST EXTENDED MEMORY ADDRESS LINE	98	SEARCH FOR OPTION ROMS
64	JUMP TO USER PATCH 1		

DRAW: JM	DATE: 1/10/2008	TITLE: Cambridge SPI_BIOS_ROM	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR	SPI_BIOS_ROM	
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE:	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 67 OF 64	

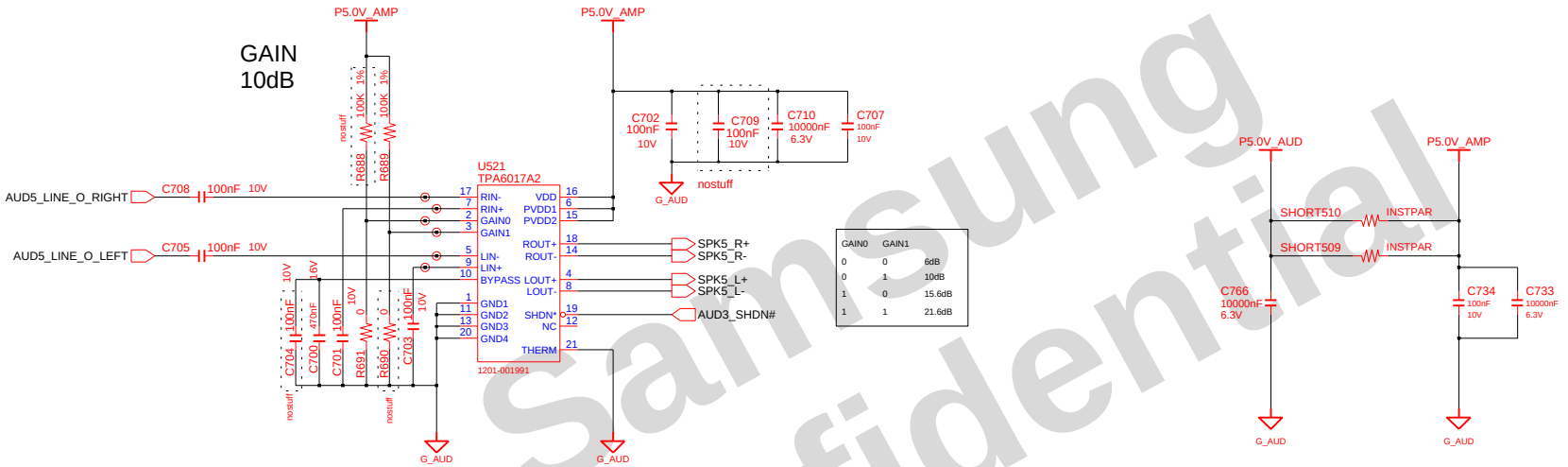
WLAN

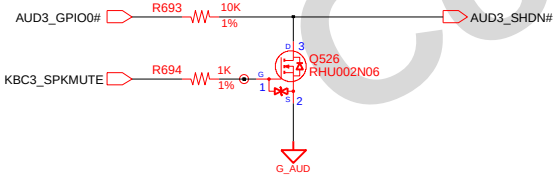


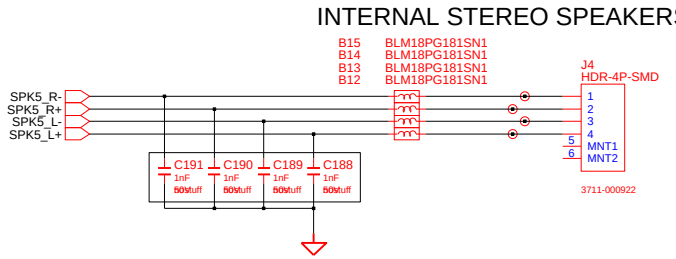
DRAW: JM	DATE: 1/10/2008	TITLE: Cambridge PCIE_Minicard_Slot	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR	PCIE_Minicard_Slot	
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE: undefined	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 62 OF 64	



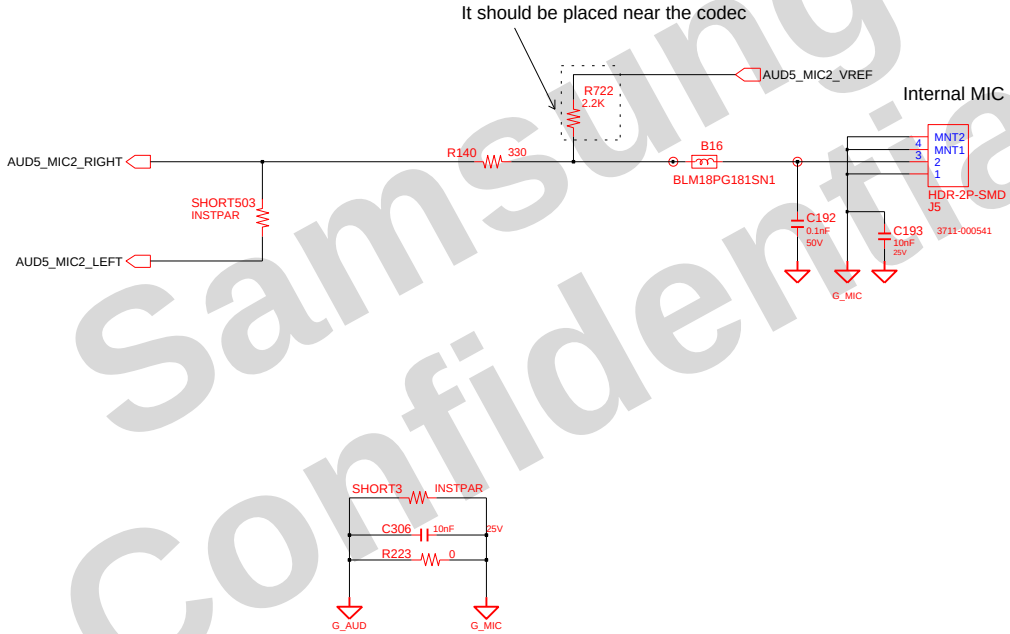
DRAW JM	DATE 1/10/2008	TITLE Cambridge HDA_Codec_Alc262 HDA_Codec_Alc262 #1	SAMSUNG ELECTRONICS
CHECK YJ	DEV. STEP PR		
APPROVAL BJ	REV 1.0		PART NO. BA41-009xxA
MODULE CODE undefined	LAST EDIT August 24, 2008 14:34:27 PM	PAGE 49 OF 64	





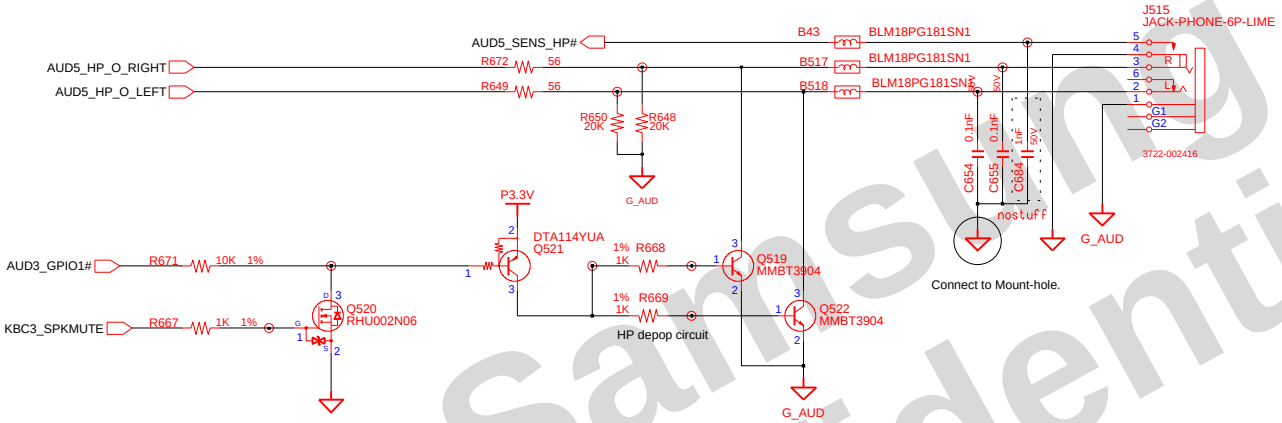


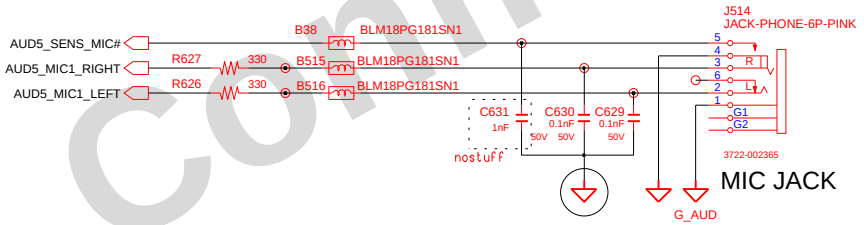
DRAW JM	DATE 1/10/2008	TITLE Cambridge HDA_Codec_Alc262 HDA_Codec_Alc262 #2	SAMSUNG ELECTRONICS
CHECK YJ	DEV. STEP PR		
APPROVAL BJ	REV 1.0		PART NO. BA41-009xxA
MODULE CODE	LAST EDIT August 24, 2008 14:34:27 PM	PAGE 50 OF 64	



DRAW: JM	DATE: 1/10/2008	TITLE: Cambridge HDA_Codec_Alc262 HDA_Codec_Alc262 #3	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE: undefined	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 51 OF 64	

HEADPHONE



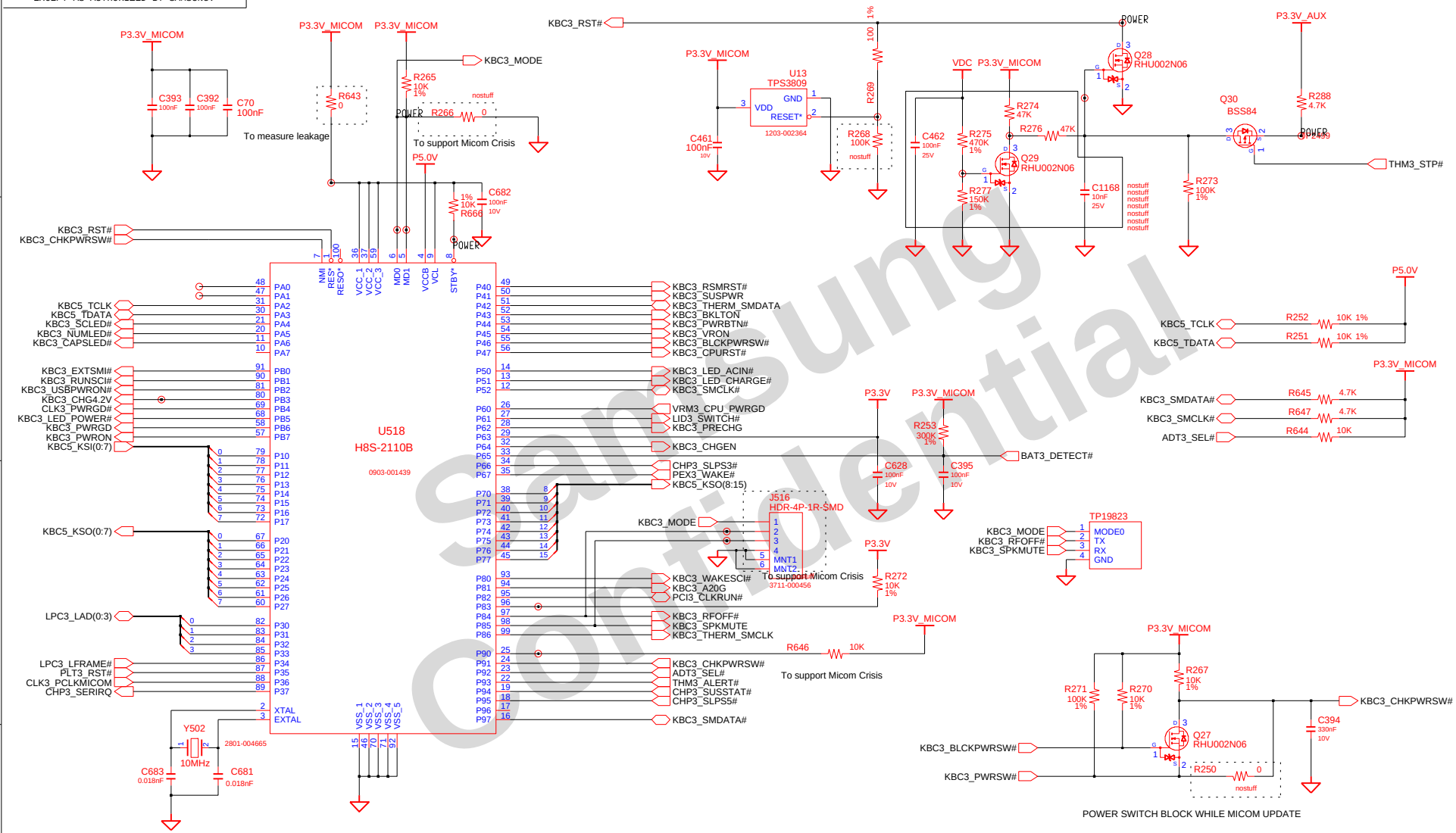


MIC JACK

The traces led to Audio Jacks have the width over 10mil

DRAW: JM	DATE: 1/10/2008	TITLE: Cambridge HDA_Codec_Alc262 HDA_Codec_Alc262 #4	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE:	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 52 OF 64	

MICOM RESET

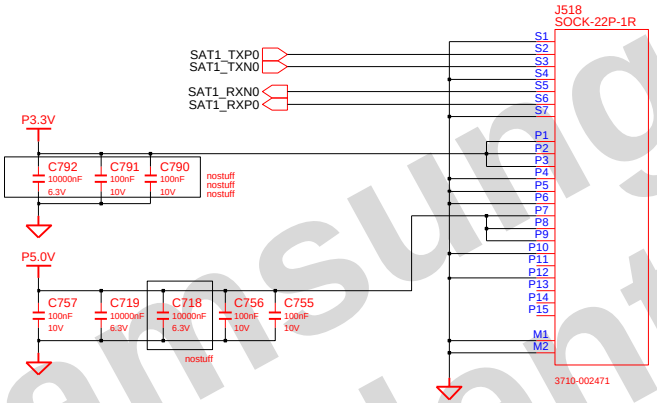


MICOM Crisis Update

Condition: P90=P91=P92=High(MICOM_P3V)
MD0=MD1=Low(0V)
Serial Port: P84 & P85

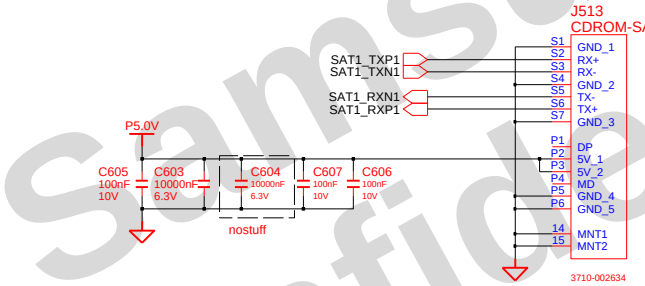
DRAW: JM	DATE: 1/10/2008	TITLE: Cambridge MICOM_Renesas2110_100p	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR	MICOM_Renesas2110_100p	
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 58 OF 64	

Main to HDD



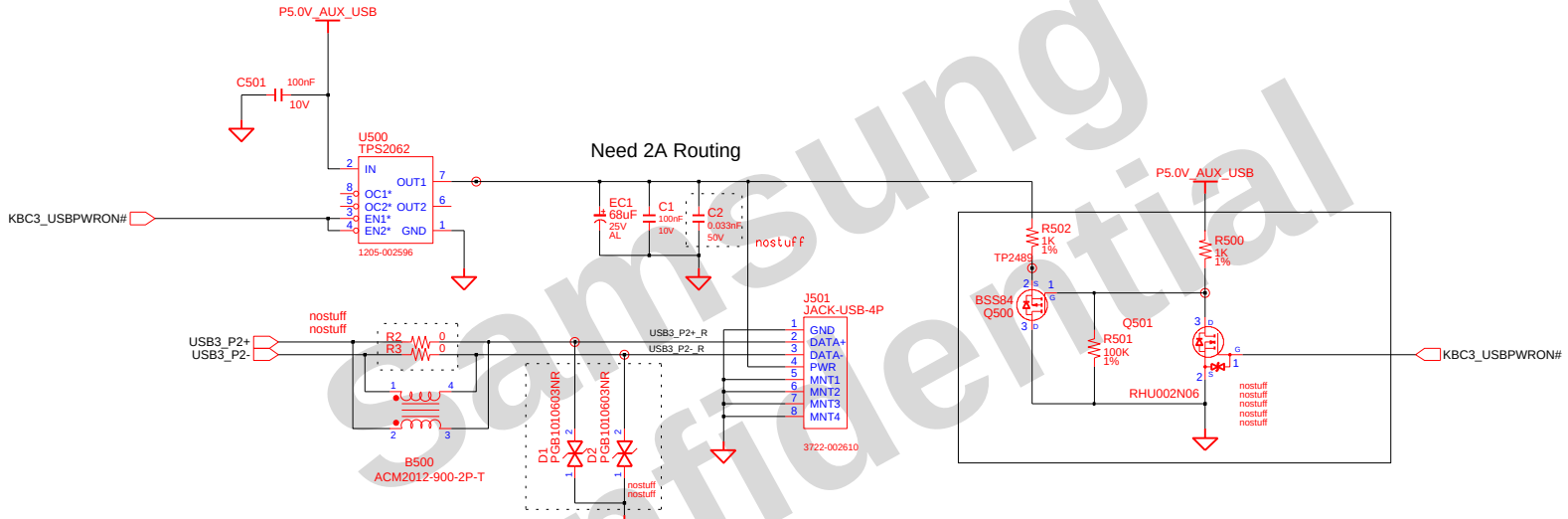
DRAW: JM	DATE: 1/10/2008	TITLE: Cambridge HDD_IF_Conn HDD_IF_Conn	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE:	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 54 OF 64	

SATA ODD



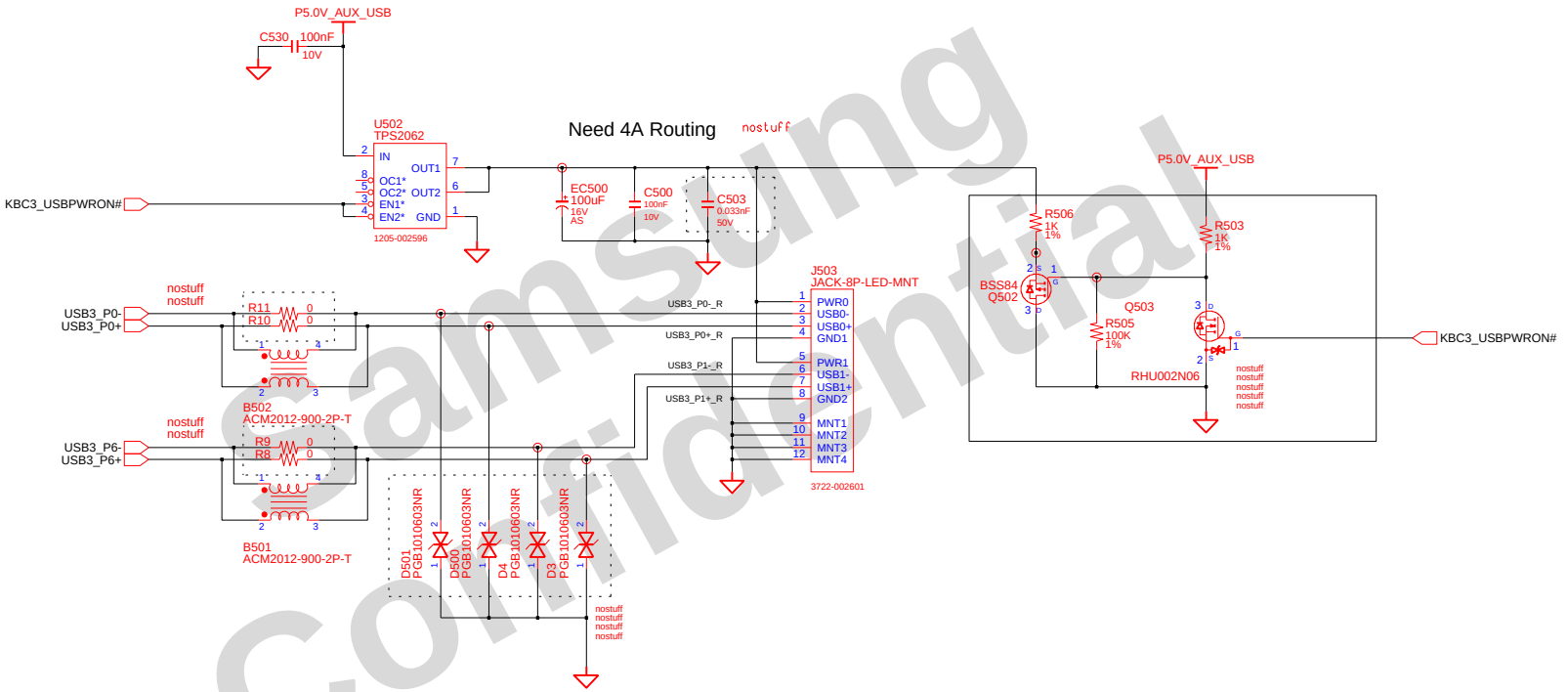
DRAW: JM	DATE: 1/10/2008	TITLE: Cambridge ODD_IF_Conn ODD_IF_Conn	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE:	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 60 OF 64	

1 PORT USB CONNECTOR



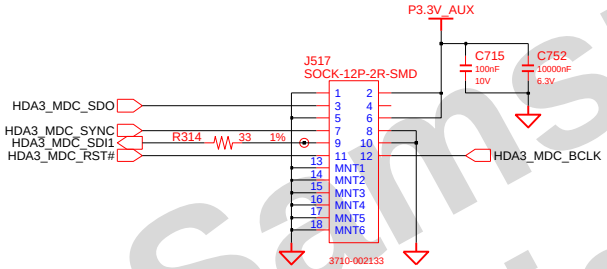
DRAW: JM	DATE: 1/10/2008	TITLE: Cambridge USB_1Port USB_1Port	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE:	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 70 OF 64	

2 PORT USB CONNECTOR



DRAW: JM	DATE: 1/10/2008	TITLE: Cambridge USB_2Port USB_2Port	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE:	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 71 OF 64	

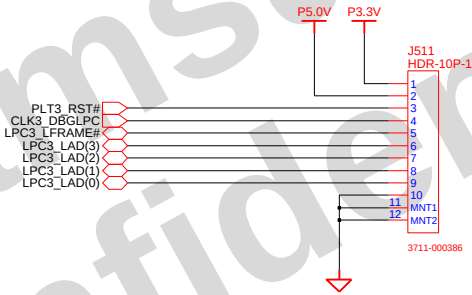
MDC Connecter



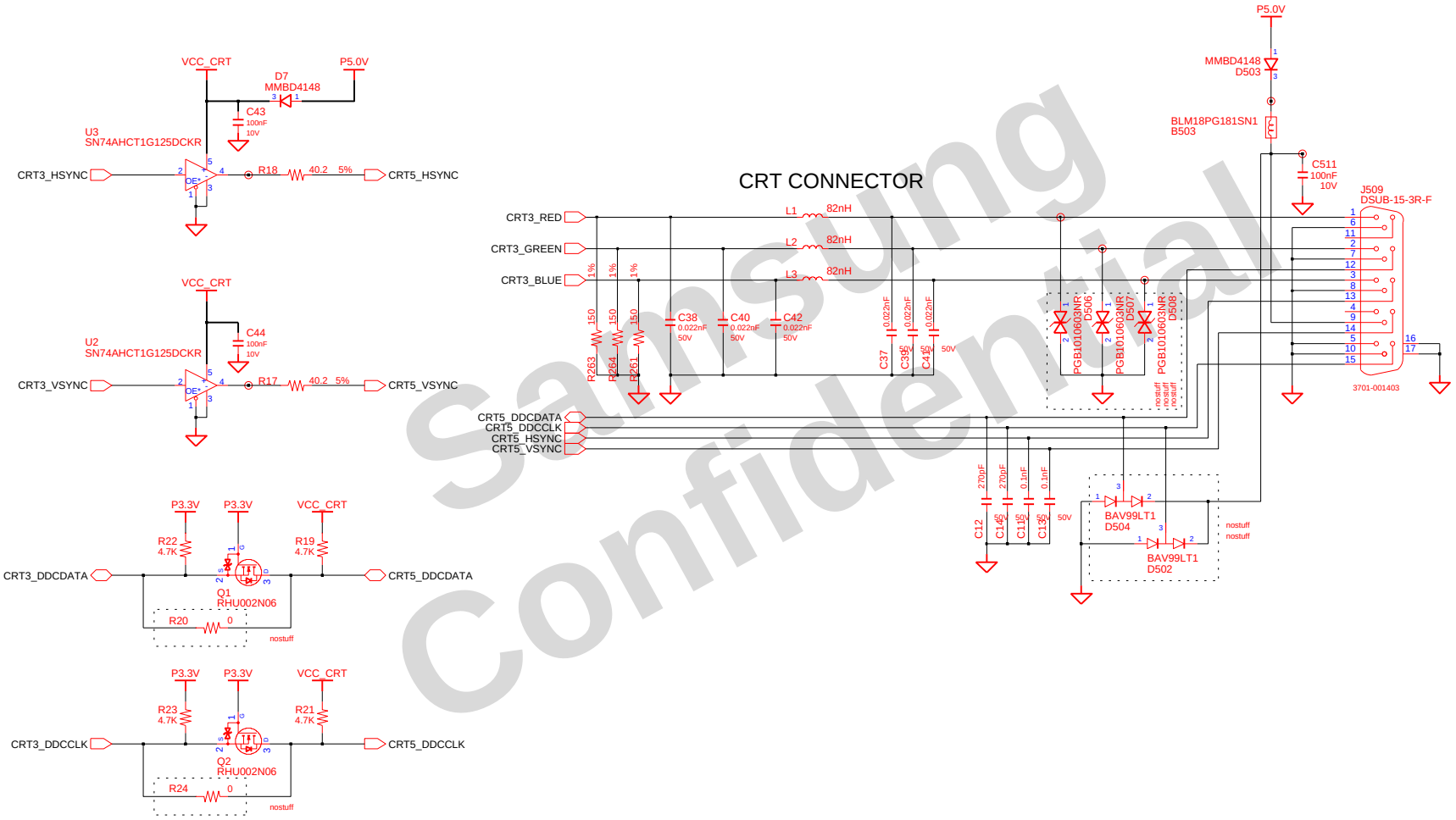
(Bottom)

DRAW: JM	DATE: 1/10/2008	TITLE: Cambridge HDA_Modem HDA_Modem	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE:	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 53 OF 64	

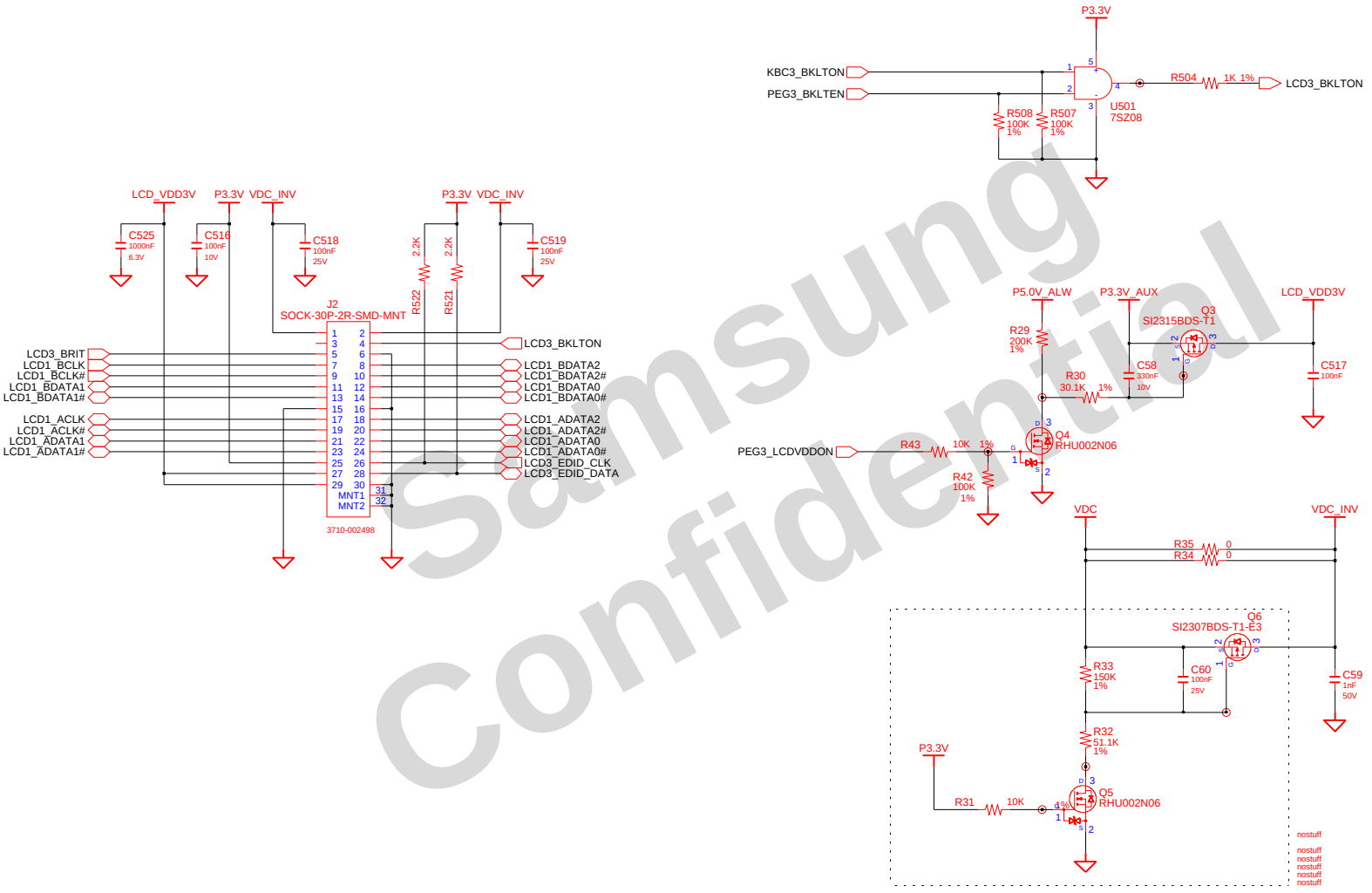
80H DECODER CONNECTOR



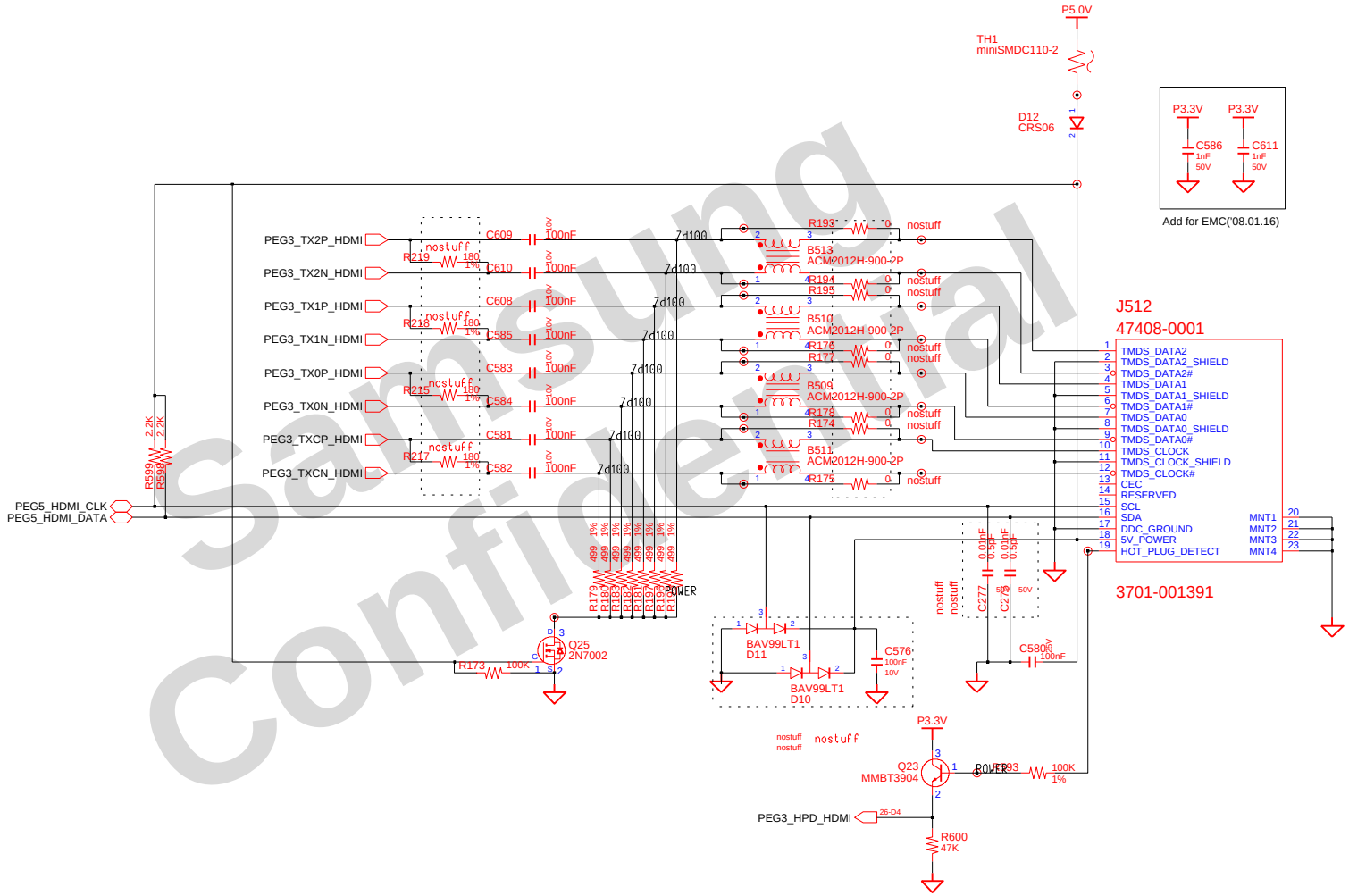
DRAW: JM	DATE: 1/10/2008	TITLE: Cambridge Other_Debug_80 Other_Debug_80	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE:	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 61 OF 64	



DRAW: JM	DATE: 1/10/2008	TITLE: Cambridge Interface_Circuit Graphics_IF_CRT	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE:	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 46 OF 64	



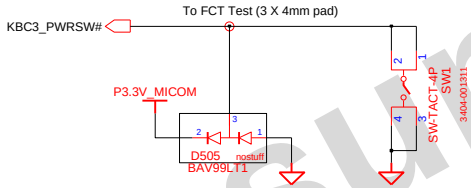
DRAW: JM	DATE: 1/10/2008	TITLE: Cambridge Interface_Circuit Graphics_IF_LCD	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE:	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE: 12	under of ined



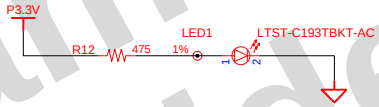
DRAW: JM	DATE: 1/10/2008	TITLE: Cambridge Interface_Circuit Graphics_IF_HDMI	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE:	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE: 13	under ined

Put this LED located near PWRSW from ME recommedation

Power LED, Blue color

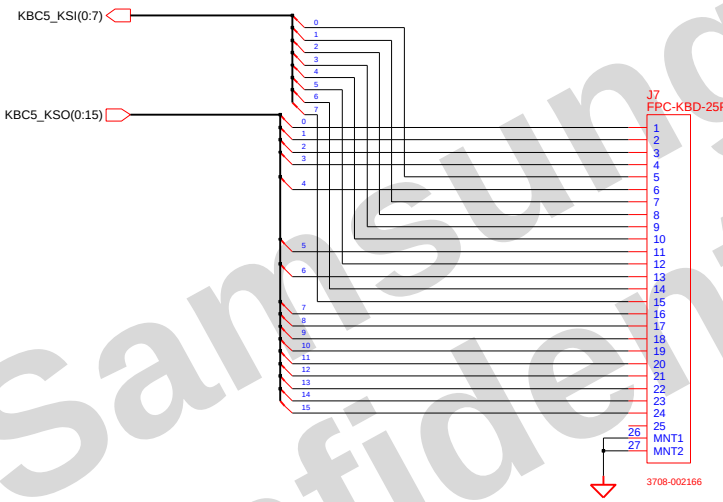


Power On LED



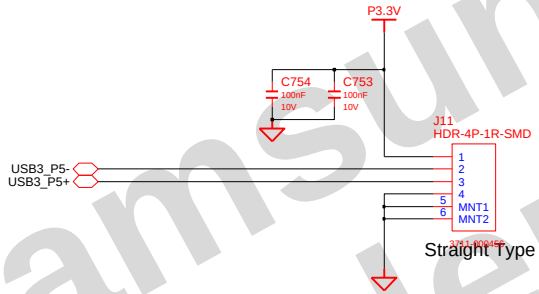
DRAW: JM	DATE: 1/10/2008	TITLE: Cambridge MIO_Switch MIO_Switch	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE:	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 59 OF 64	

KEYBOARD



DRAW: JM	DATE: 1/10/2008	TITLE: Cambridge KBD_IF_Conn KBD_IF_Conn	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE:	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 55 OF 64	

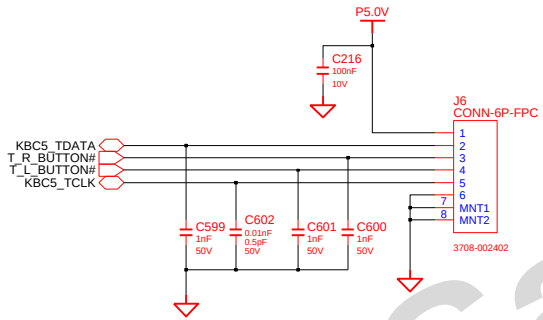
Bluetooth Interface

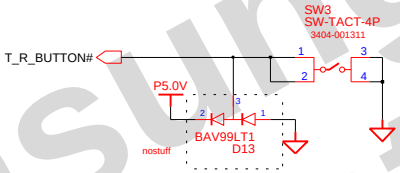


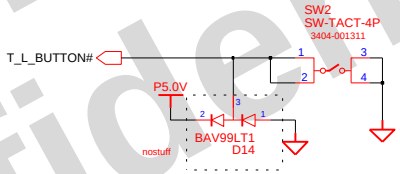
Straight Type

DRAW: JM	DATE: 1/10/2008	TITLE: Cambridge Bluetooth_IF_Conn Bluetooth_IF_Conn	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE:	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 44 OF 64	

TOUCHPAD

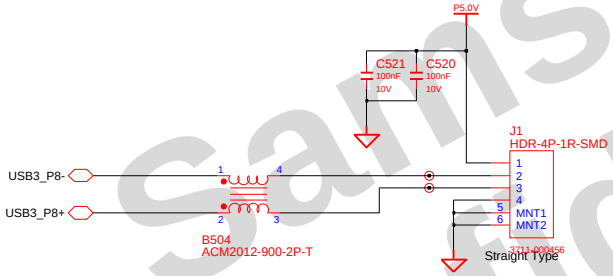




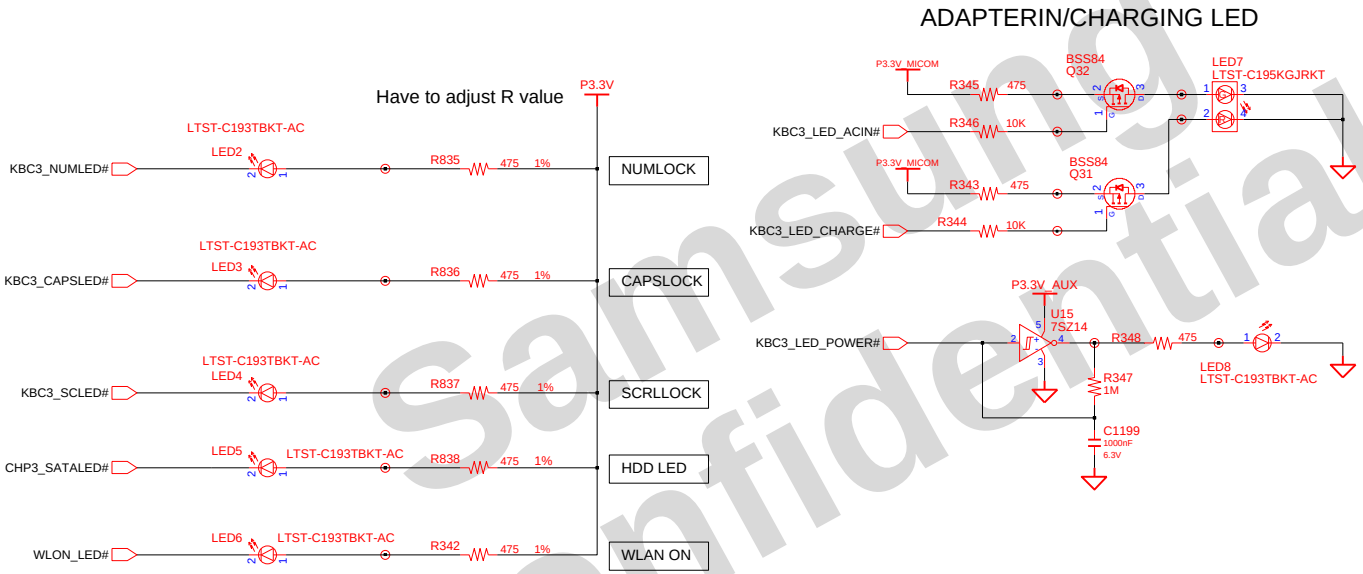


DRAW: JM	DATE: 1/10/2008	TITLE: Cambridge Touchpad_IF_Conn / Touchpad_IF_Conn	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		PART NO.: BA41-009xxA
APPROVAL: BJ	REV: 1.0		
MODULE CODE:	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 69 OF 64	

CAMERA

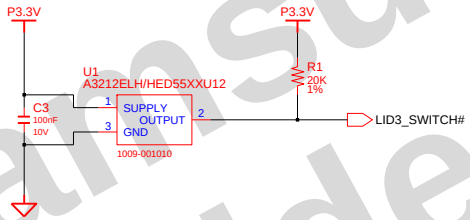


DRAW: JM	DATE: 1/10/2008	TITLE: Cambridge Camera_IF_Conn Camera_IF_Conn	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE:	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 45 OF 64	



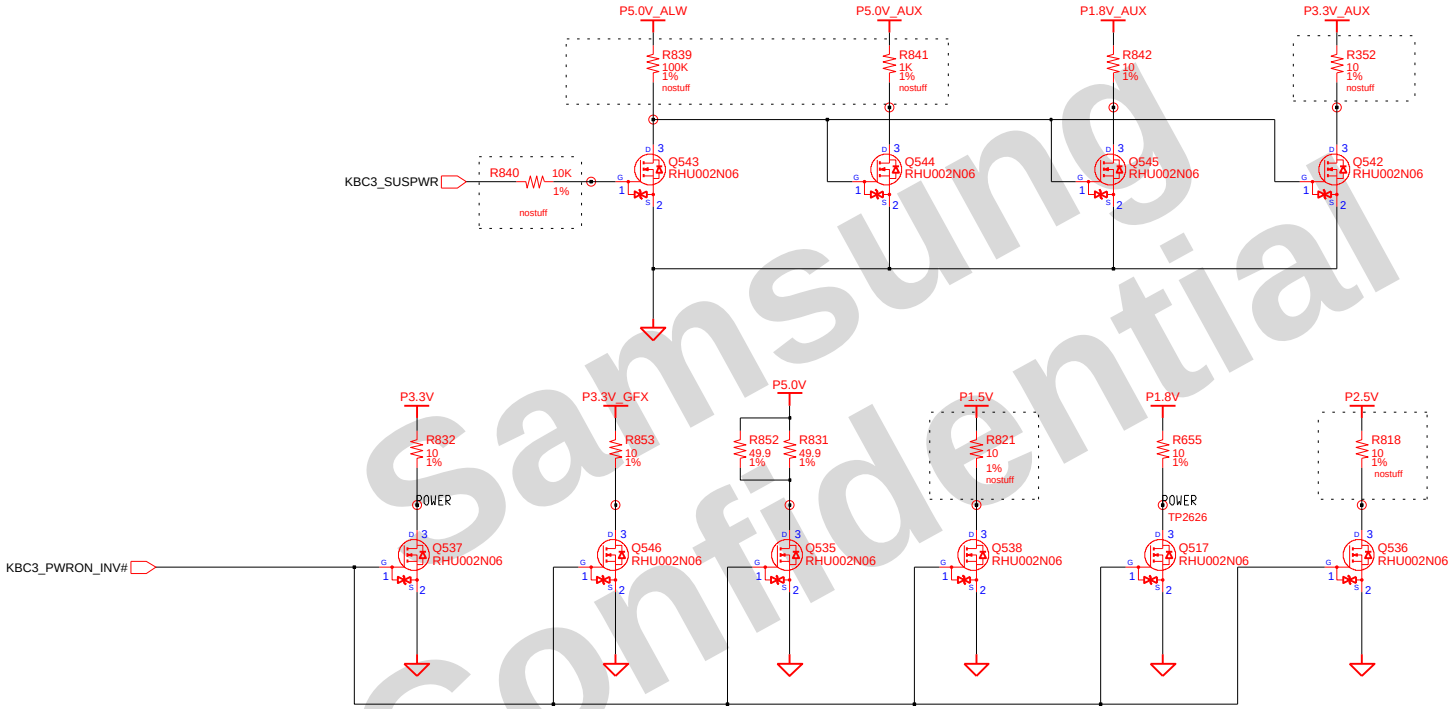
DRAW: JM	DATE: 1/10/2008	TITLE: Cambridge LED_Switch LED_Switch	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE:	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 56 OF 64	

LID_SWITCH



DRAW: JM	DATE: 1/10/2008	TITLE: Cambridge LID_Switch LID_Switch	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE:	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 57 OF 64	

POWER DISCHARGER



DRAW: JM	DATE: 1/10/2008	TITLE: Cambridge PWR_MV_DisCharger DISCHARGING LOGIC	SAMSUNG ELECTRONICS
CHECK: YJ	DEV. STEP: PR		
APPROVAL: BJ	REV: 1.0		PART NO.: BA41-009xxA
MODULE CODE: undefined	LAST EDIT: August 24, 2008 14:34:27 PM	PAGE 63 OF 64	

Index_Page