SuZhou

CPU : Intel Arrandale
Chip Set : Intel Ibex Peak(PM55)
GFX : N11P / M-GE(40nm)
Remarks : Calpella Platform

Model Name : SuZhou-MH
PBA Name : MAIN
PCB Code : BA41-01190A
Dev. Step : PVR
Revision : 1.0
T.R. Date : 2009.11.3

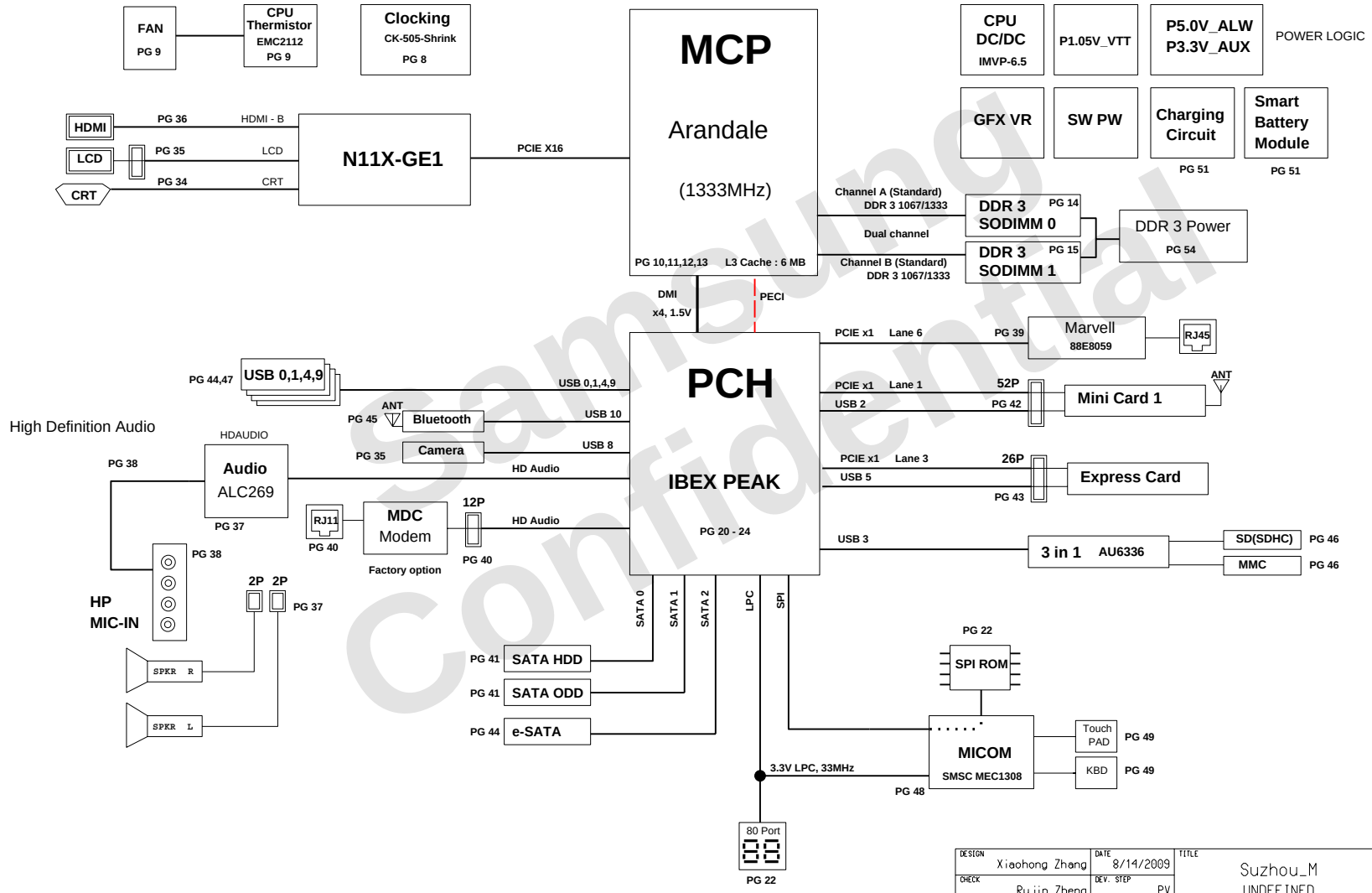
Design	CHECK	APPROVAL
Xiaohong Zhang	Rujin Zheng	BC Lee

■ ***Owner : SEC Mobile R & D*** ***Signature :*** ***X***

Table of Contents

DESIGN: Xiaohong Zhang	DATE: 8/14/2009	TITLE: Suzhou_M	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE:	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 1 OF 62	

BLOCK DIAGRAM



DESIGN: Xiaohong Zhang	DATE: 8/14/2009	TITLE: Suzhou_M UNDEFINED UNDEFINED	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE:	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 2 OF 62	

BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails		Active in
VDC	Primary DC system power supply (7 to 21V)	S4 - S5
P3.3V_MICOM	3.3V always power rail (for Micom)	
P5.0V_ALW	5.0V always power rail	
P5.0V_STB	5.0V always power rail	
P5.0V_AUX	5.0V switched on power rail (off in S4-S5)	S3
P3.3V_AUX	3.3V switched on power rail (off in S4-S5)	
P1.5V_AUX	1.5V power rail for DDR (off in S4-S5)	
P5.0V	5.0V switched power rail (off in S3-S5)	S0
P3.3V	3.3V switched power rail (off in S3-S5)	
P1.8V	1.8V switched power rail (off in S3-S5)	
P1.5V	1.5V switched power rail (off in S3-S5)	
P0.75V	0.9V power rail for DDR (off in S3-S5)	
VCC_CORE	Core Voltage for CPU	S0
EGFX_CORE	Core Voltage for GPU	
P1.05V (VCCP)	VCC for Clarksfield & IBEX Peak	
P1.1V_VTT	VTT for CLARDSFIELD & IBEX Peak	

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	IBEX-PEAK	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	25MHz	LAN	Intel LAN
Crystal	25MHz	IBEX PEAK	

LCD Pannel Detect (TBD)

Devices	Resolution	PANNEL_DETECT_0

I²C / SMB Address

Devices	Address	Hex	Bus
IBEX PEAK	Master	-	SMBUS Master
CPU Thermal Sensor	0111 101x	7Ah	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M Shrink(Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable
Thermal Sensor on board	1101 100x	98h	
Power thermal management TS	1101 011x	96h	

USB PORT Assign

PORT #	ASSIGNED TO
0	SYSTEM PORT 0
1	SYSTEM PORT 1
2	Mini PCI Express 1
3	NC
4	SYSTEM PORT 4
5	EXPRESS CARD
6	NC (N/A WITH HM55)
7	NC (N/A WITH HM55)
8	Multi Memory Card Controller
9	SYSTEM PORT 9
10	Bluetooth
11	Camera
12	NC
13	NC

PCI Express Assign

PORT #	ASSIGNED TO
1	Mini Card 1 (WLAN)
2	NC
3	EXPRESS CARD
4	NC
5	NC
6	NC
7	NC (N/A WITH HM55)
8	NC (N/A WITH HM55)

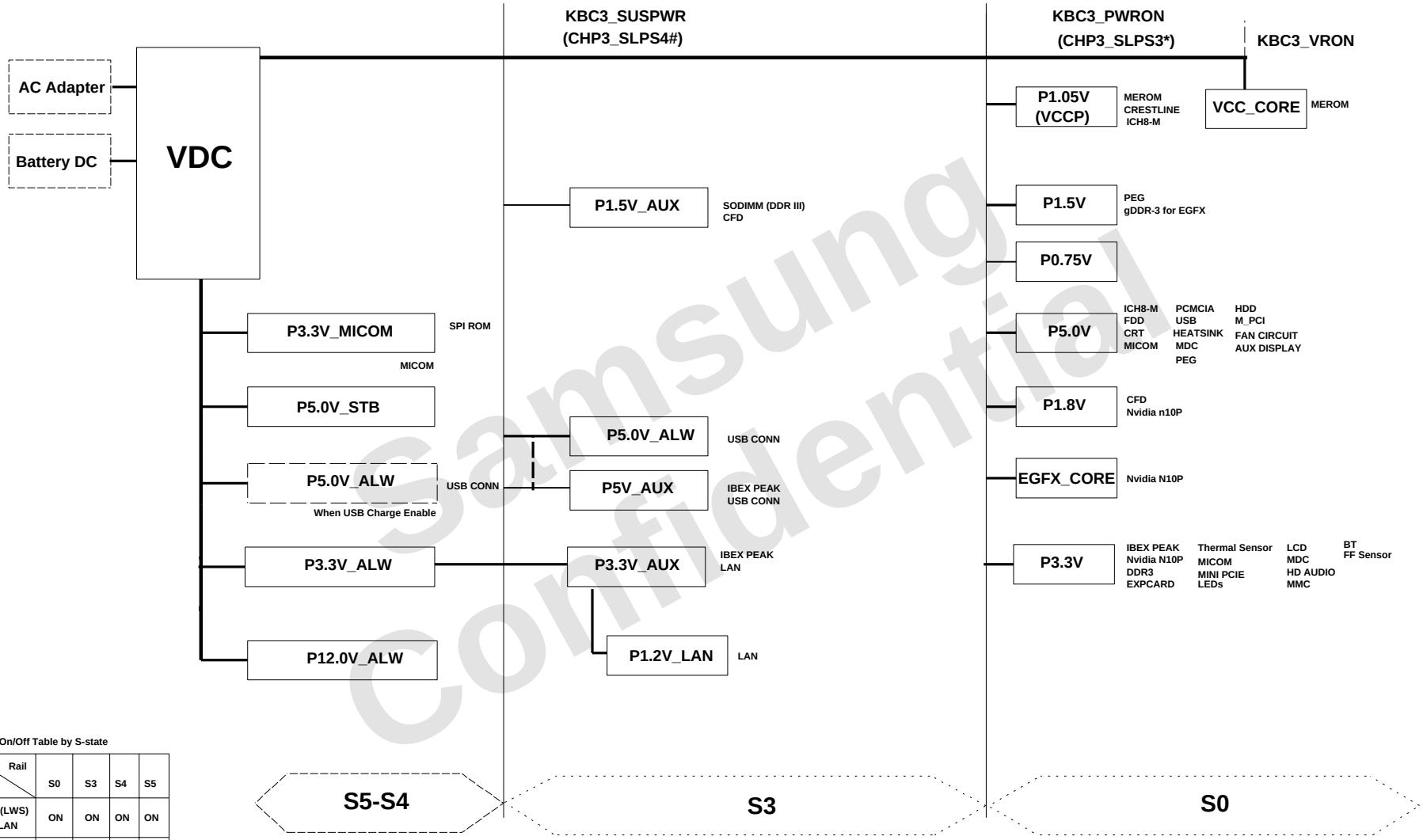
SATA PORT Assign

PORT #	ASSIGNED TO
0	HDD
1	ODD
2	(N/A WITH HM55)
3	(N/A WITH HM55)
4	e-SATA

DESIGN: Xiaohong Zhang	DATE: 8/14/2009	TITLE: Suzhou_M UNDEFINED UNDEFINED	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE:	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 3 OF 62	

POWER DIAGRAM

Rev 0.1



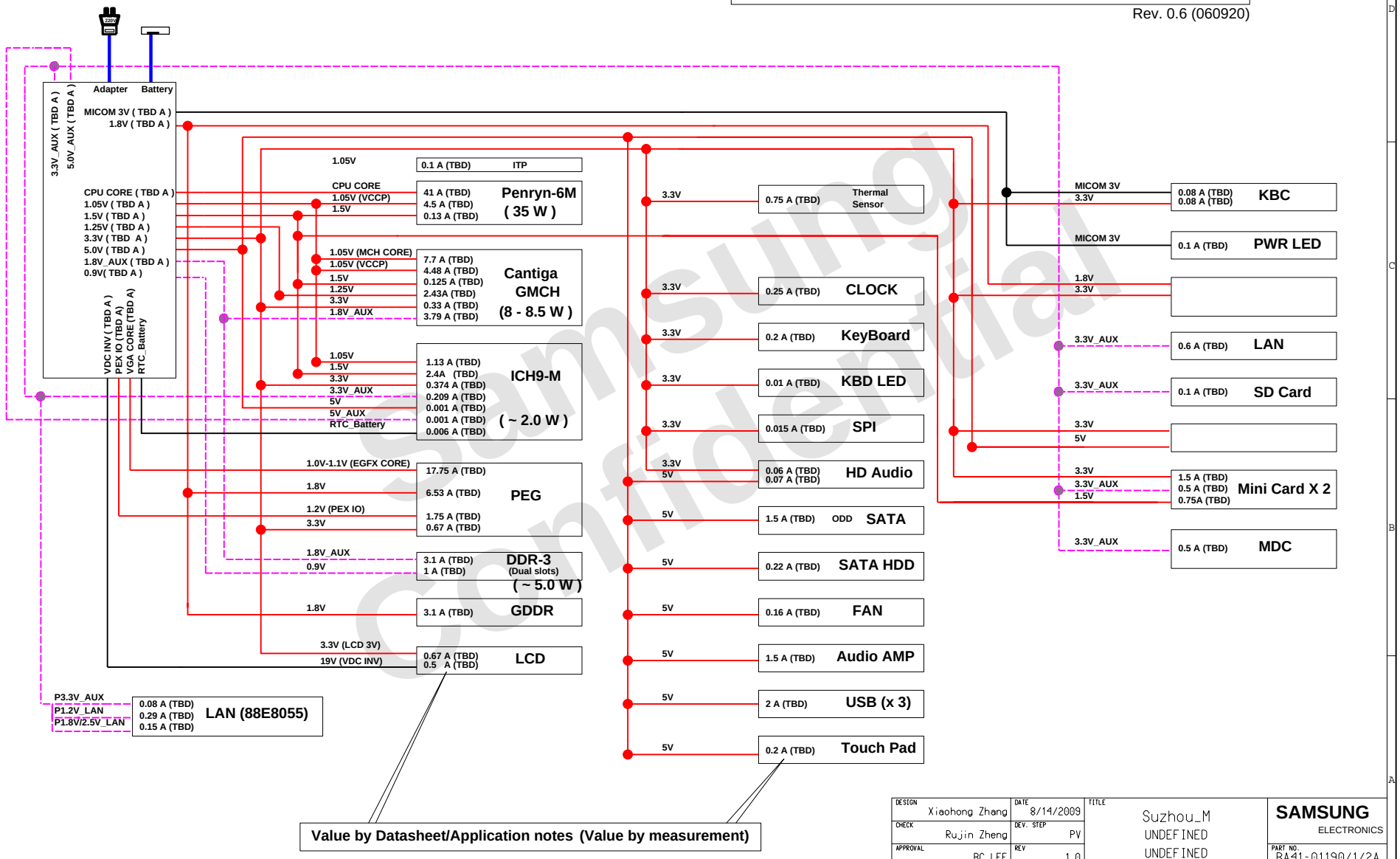
Power On/Off Table by S-state

Rail / State	S0	S3	S4	S5
+V*A(LWS) +V*LAN	ON	ON	ON	ON
+1.8V_AUX +0.9V	ON	ON	—	—
+V*AUX	ON	ON	—	—
+V	ON	—	—	—
+V* (CORE)	ON	—	—	—

DESIGN: Xiaohong Zhang	DATE: 8/14/2009	TITLE: Suzhou_M UNDEFINED UNDEFINED	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE:	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 4 OF 62	

POWER RAILS ANALYSIS

Rev. 0.6 (060920)

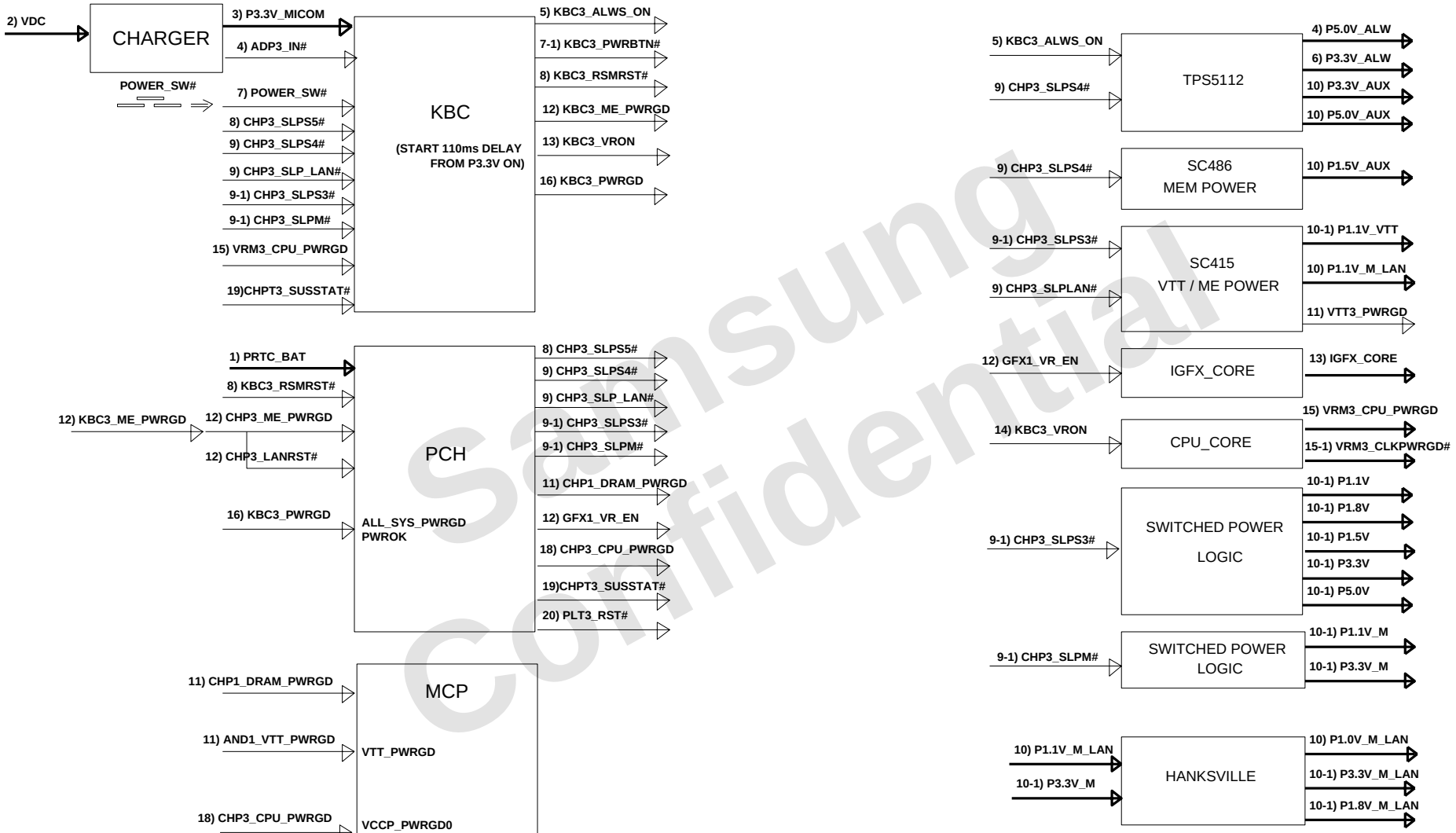


Value by Datasheet/Application notes (Value by measurement)

DESIGN: Xiaohong Zhang	DATE: 8/14/2009	TITLE: Suzhou_M UNDEFINED UNDEFINED	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE:	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 5 OF 62	

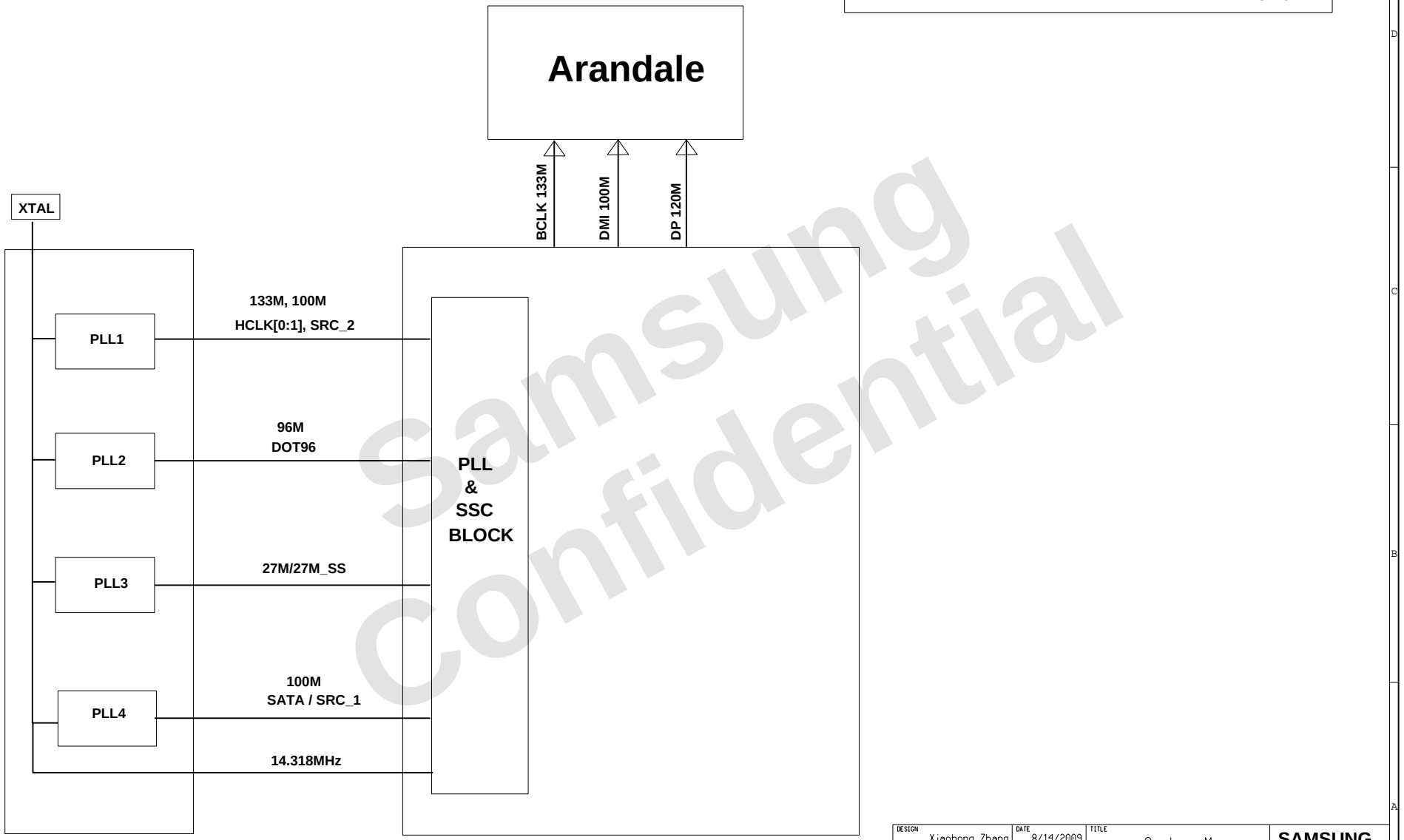
PRELIMINARY

POWER SEQUENCE Rev. 0.5



DESIGN: Xiaohong Zhang	DATE: 8/14/2009	TITLE: Suzhou_M UNDEFINED UNDEFINED	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE:	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 6 OF 62	

CLOCK DISTRIBUTION Rev. 0.1



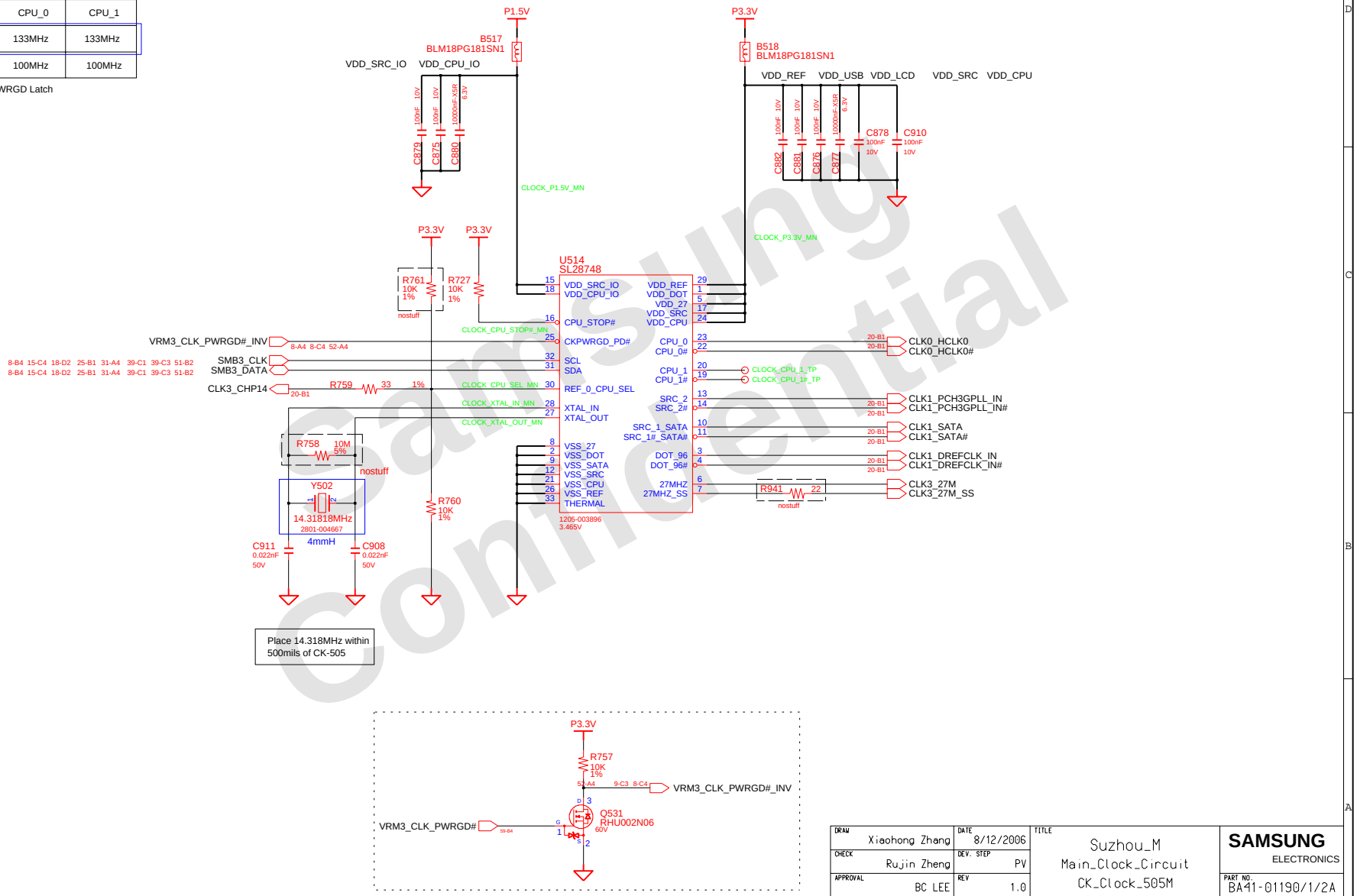
DESIGN: Xiaohong Zhang	DATE: 8/14/2009	TITLE: Suzhou_M UNDEFINED UNDEFINED	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE:	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 7 OF 62	

CK505M SHRINK VERSION

CPU_MODE SEL

Pin 30	CPU_0	CPU_1
CPU_SEL = 0	133MHz	133MHz
CPU_SEL = 1	100MHz	100MHz

*CPU_SEL During CK_PWRGD Latch



DRAW: Xiaohong Zhang	DATE: 8/12/2006	TITLE: Suzhou_M Main_Clock_Circuit CK_Clock_505M	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE: undefined	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 8 OF 62	

THERMAL SENSOR & FAN CONTROL

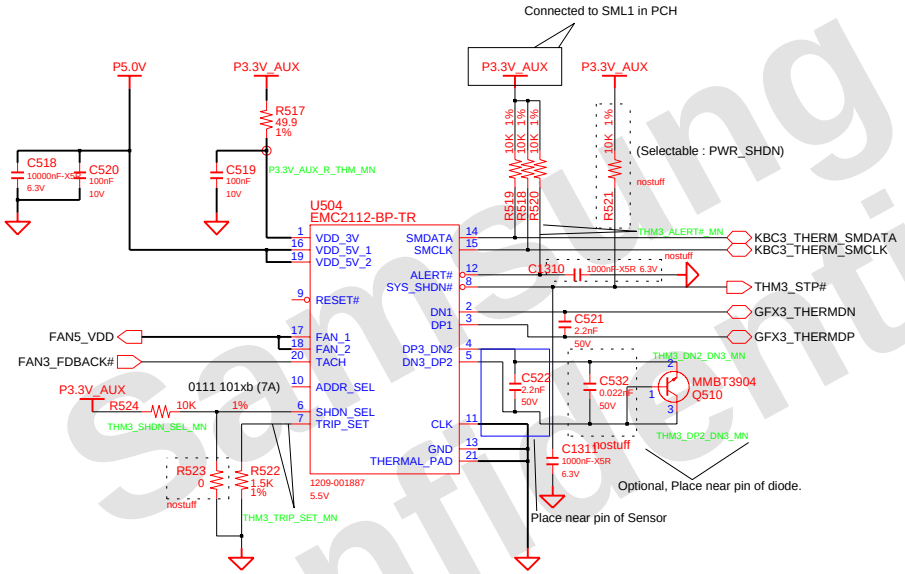
ADDRESSS_SEL MODE	
0	0101 111xb
✓ HIGH Z	0111 101xb (7A)
1	0101 110xb

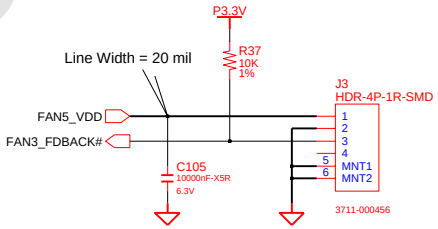
SHDN_SEL MODE	
0	INTEL TR MODE
HIGH Z	AMD CPU/DIODE MODE
✓ 1	EXT.DIODE 2 MODE

TRIP_SET Resistor Setting (60 ~ 122 C)	
60	0.0
95	1500
96	1580
97	1690
98	1820
99	1960
100	2050
101	2210
102	2370
✓ 103	2550
104	2740
105	2940
122	49900

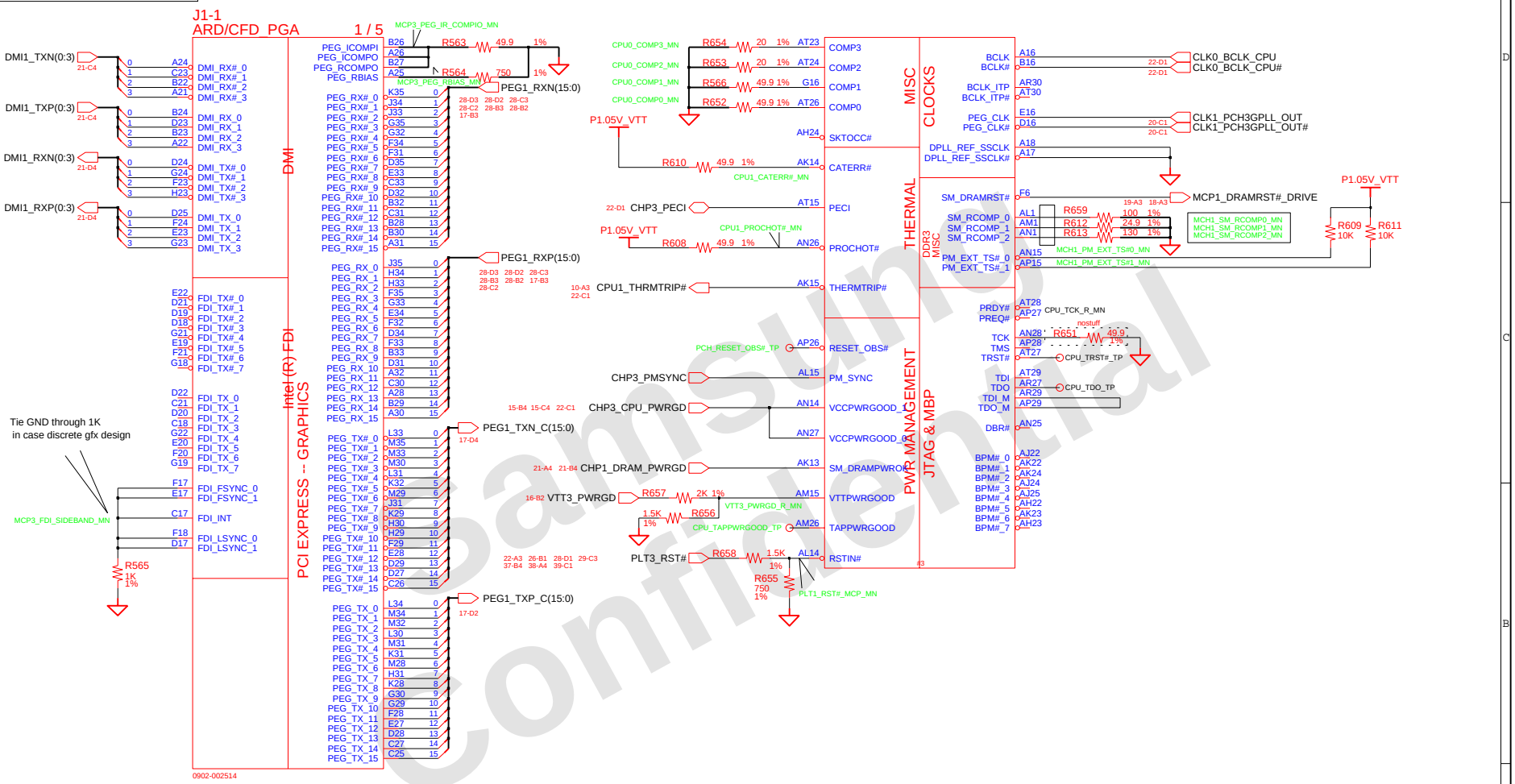
V_Trip = (T_Trip - T_Min) / 80

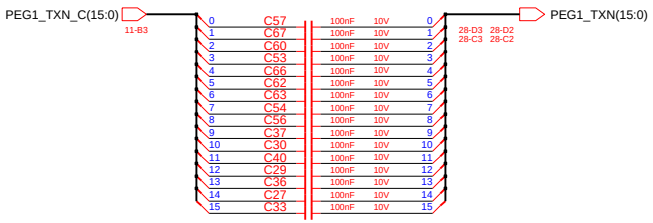
V_TRIP : TRIP_SET Voltage
T_Min : Minimum Temperature

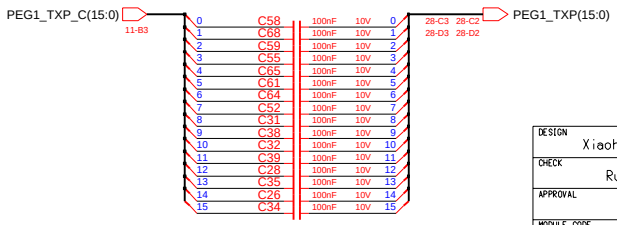




ARRANDALE PROCESSOR (DMI,PEG, FDI)

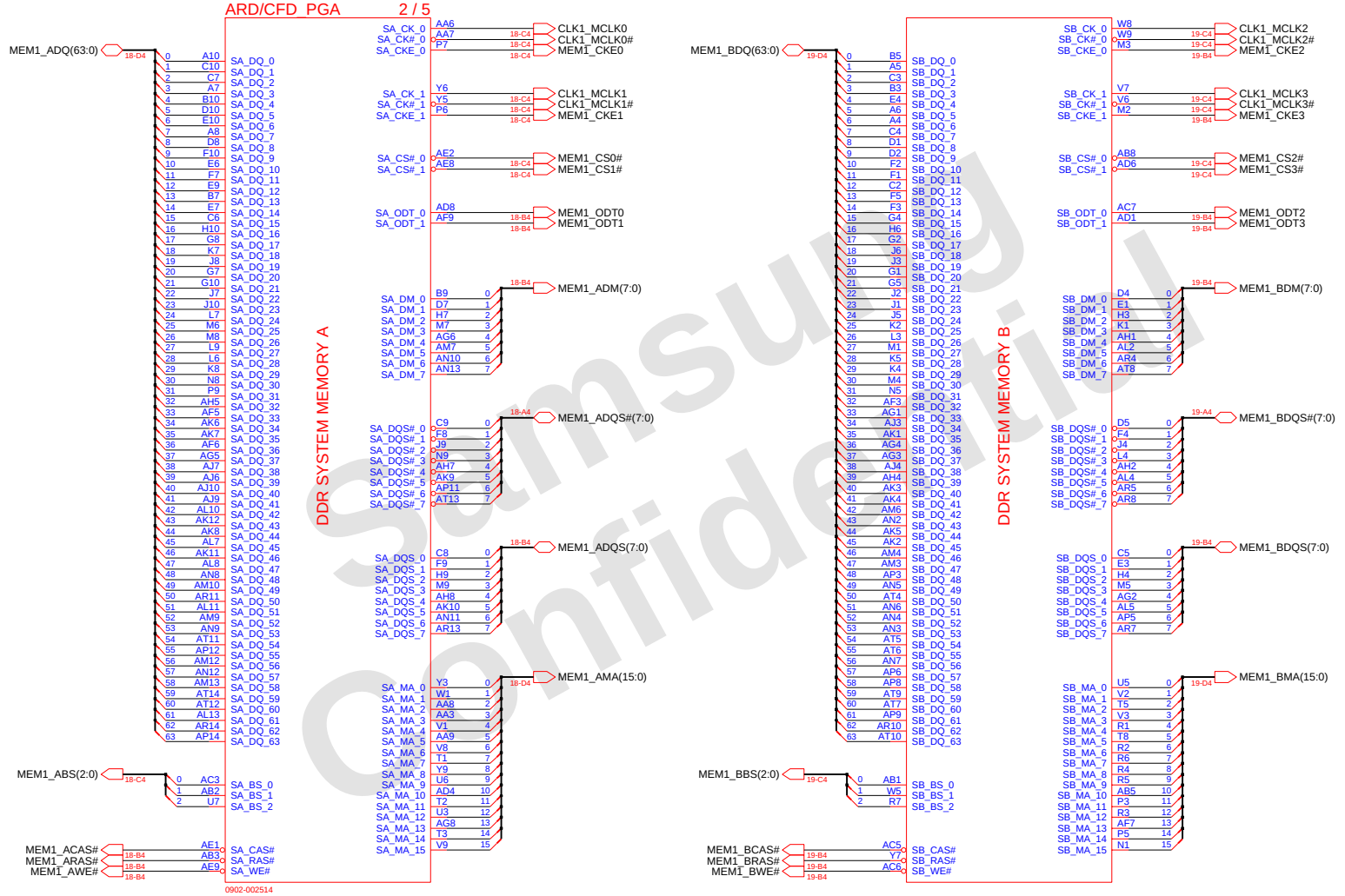






DESIGN: Xiaohong Zhang	DATE: 12/18/2008	TITLE: Suzhou_M CLARKSFIELD 1/5	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		PART NO.: BA41-01190/1/2A
APPROVAL: BC LEE	REV: 1.0		
MODULE CODE	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 10 OF 62	

J1-2
ARD/CFD_PGA 2 / 5



DESIGN: Xiaohong Zhang	DATE: 12/18/2008	TITLE: Suzhou_M CLARKSFIELD 2/5	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		PART NO.: BA41-01190/1/2A
APPROVAL: BC LEE	REV: 1.0		
MODULE CODE:	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 11 OF 62	

ALL VTT DECAP IS SHARED(10uFX9, 22uFx7)

VTT_SEL	VOLTAGE	CPU
1	P1.05V	AUBUNDALE
0	P1.1V	CLARKS FIELD

CPU_CORE — J1-3 ARD/CFD_PGA 3 / 5 — CPU CORE SUPPLY

Under carity of the socket

nostuff

6x 470 uF : CPU VR side

POWER — 1.1V RAIL POWER

P1.05V_VTT

Which 330uF ? 220uF?

J1-4 ARD/CFD_PGA 4 / 5

GRAPHICS — GRAPHICS VIDS — SENSE LINES

ADD 1K PD in discrete GFX design

POWER — DDR3 - 1.5V RAILS

FDI

PEG & DMI

2A ROUTING NEEDED.

1.1V

1.8V

CPU VIDS

SENSE LINES

0902-002514

Samsung Confidential

DESIGN: Xiaohong Zhang	DATE: 12/18/2008	TITLE: Suzhou_M CLARKSFIELD 3/5	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 12 OF 62	

J1-5
ARD/CFD_PGA6 / 5

VSS

VSS

NCTF

RESERVED

R650 3.01K 1%

CPU_CFG_7_R_MN

CPU_VSS_NCTF3
CPU_VSS_NCTF4
CPU_VSS_NCTF5

CPU_RSVD17_TP
CPU_RSVD18_TP

SA_DIMM_VREFDQ_TP
SB_DIMM_VREFDQ_TP

0902-002514

CFG Straps for Processor

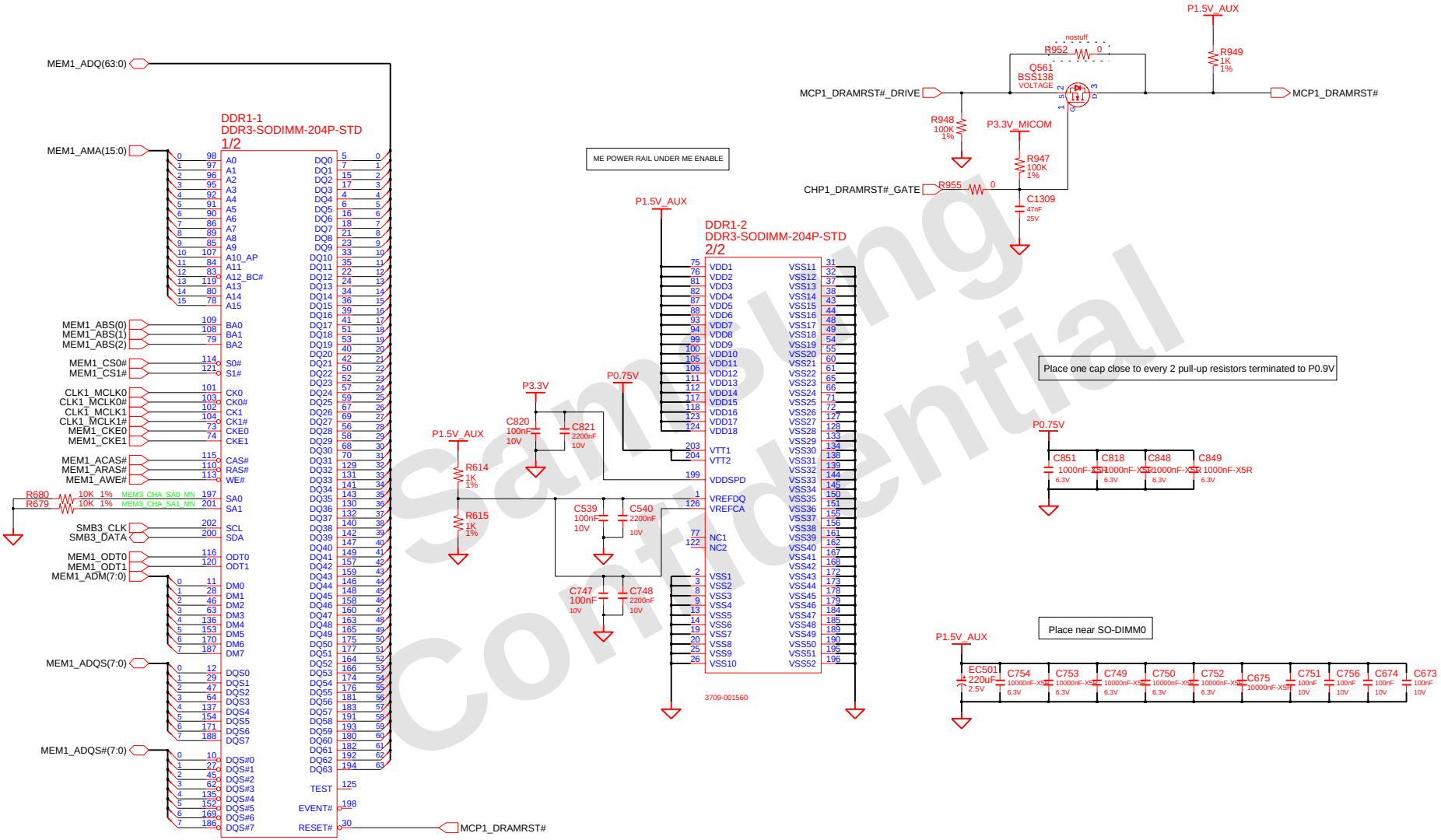
ALL nostuff

PCI Express Configuration Select		
CFG0	1 : Single PEG 0 : Bifunction enabled	
PCI Express Static Lane Reveal		
CFG3	1 : Normal operation 0 : Lane Reversed	
Display Port Presence		
CFG4	1 : Disabled - No DP device is connected to eDP 0 : Enabled - (DP device is connected to eDP	
PCIE 2.O SUPPORT		
CFG7	1 : Normal operation 0 : PCIE2.O Jitter support	

DESIGN: Xiaohong Zhang	DATE: 12/18/2008	TITLE: Suzhou_M CLARKSFIELD 4/5	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 13 OF 62	

DDR SO-DIMM #0

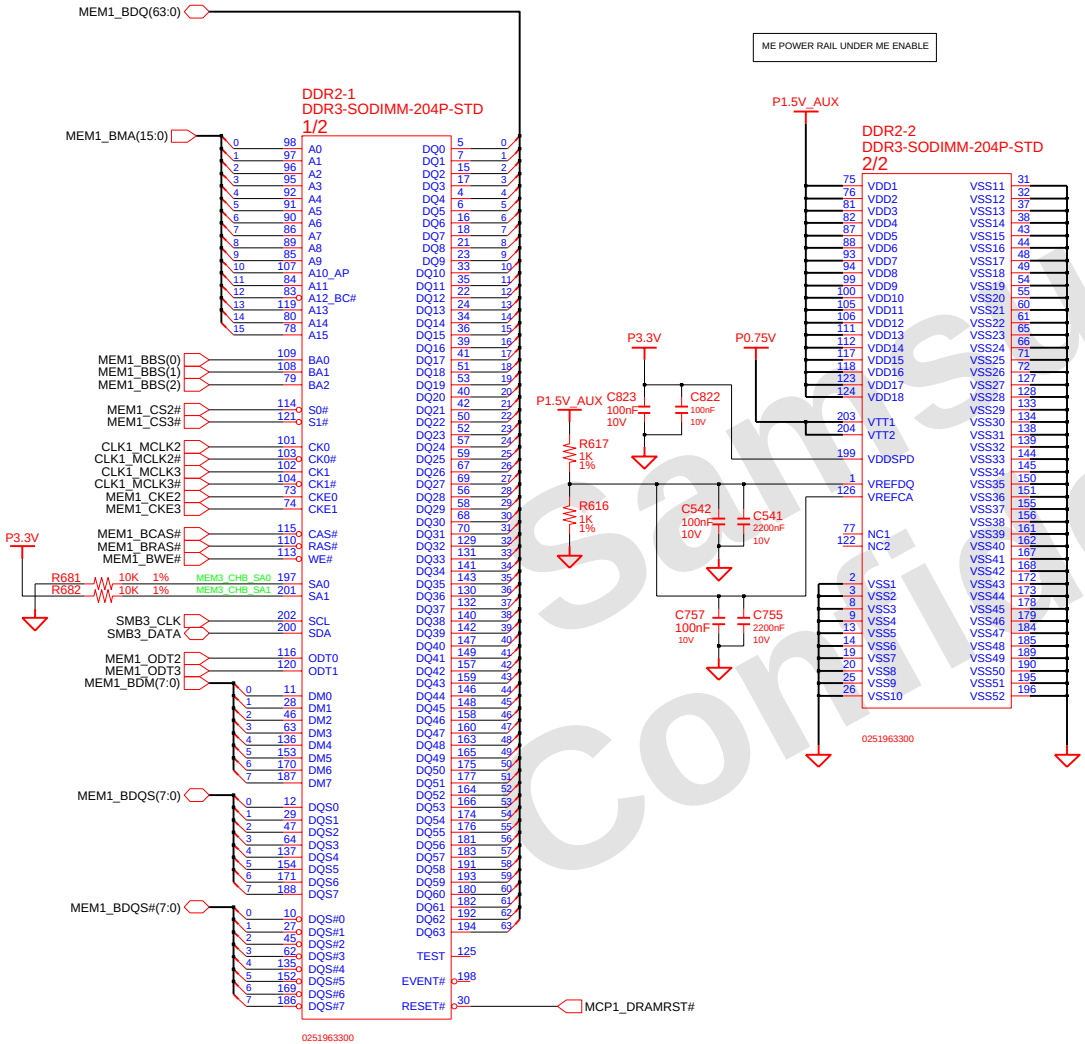
Height : 5.2mm (Reverse)

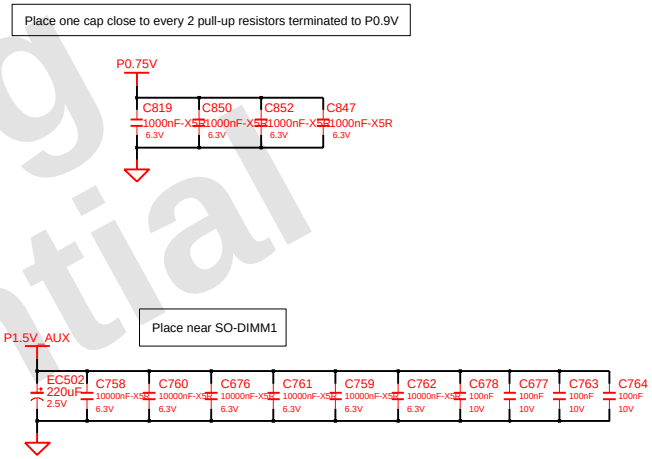


DRAW: Xiaohong Zhang	DATE: 11/8/2006	TITLE: Suzhou_M SODIMM_REV DDR3 CH A	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE:	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 14 OF 62	

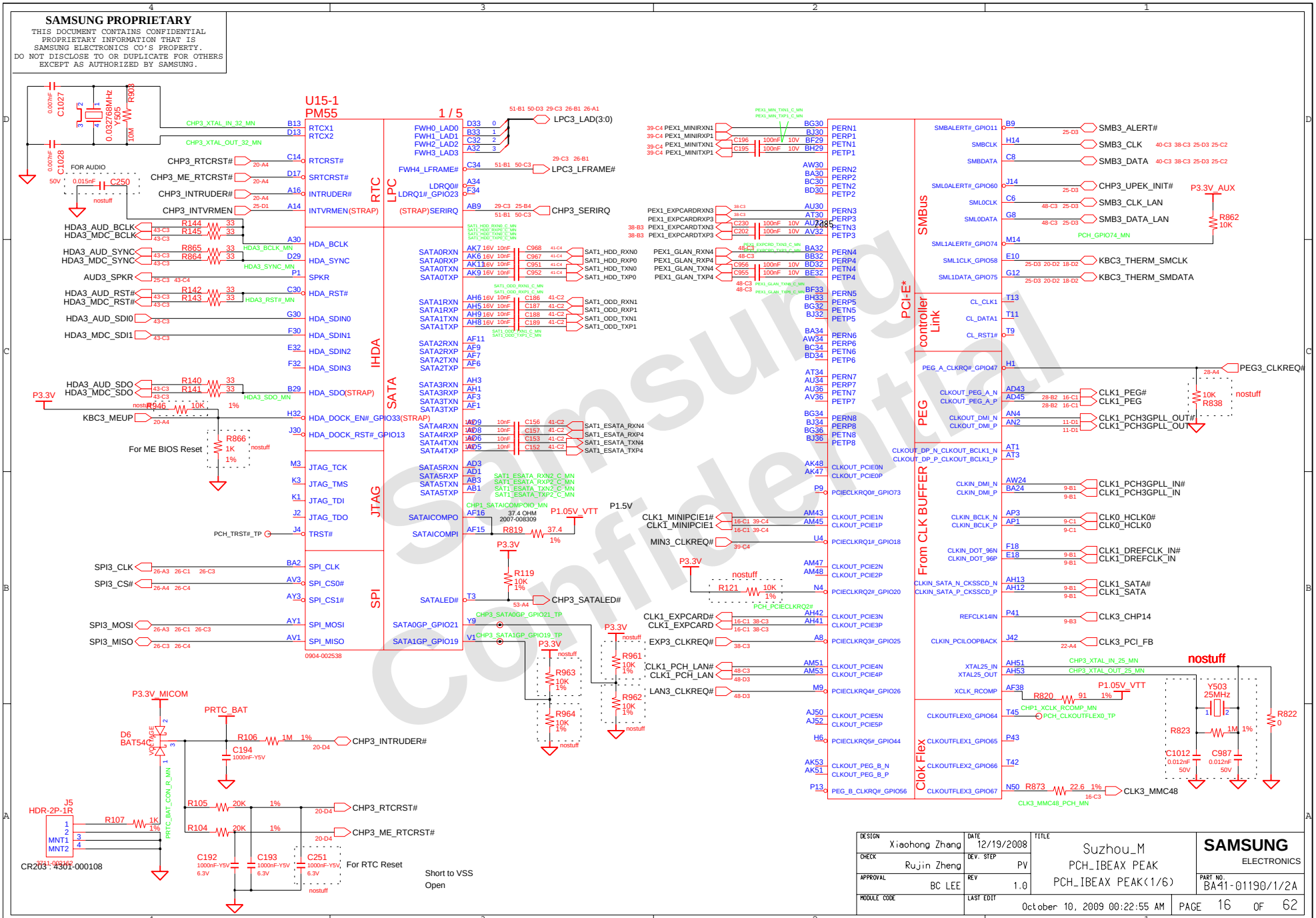
DDR SO-DIMM #1

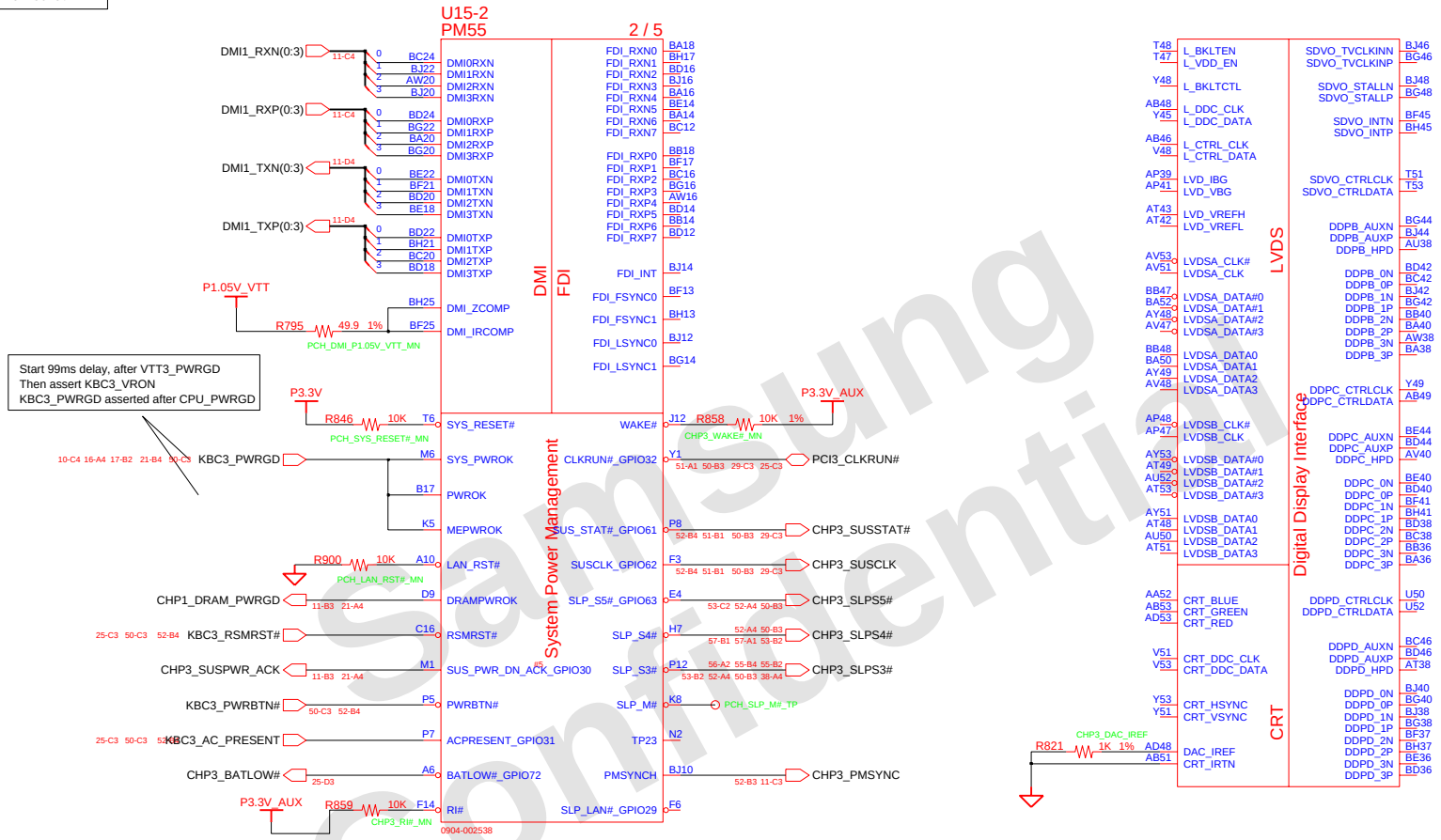
Height : 9.2mm (Reverse)



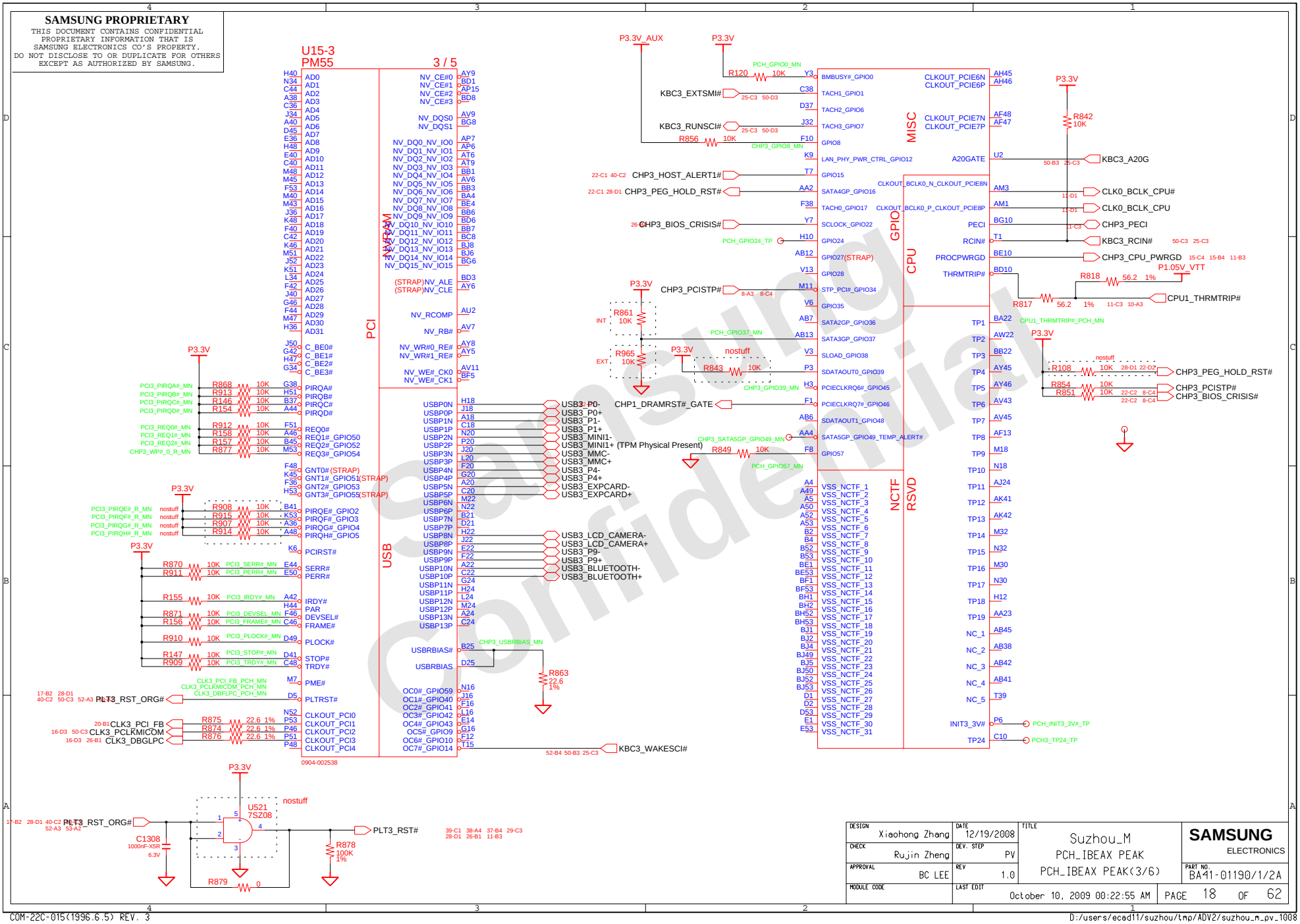


DRAW: Xiaohong Zhang	DATE: 11/8/2006	TITLE: Suzhou_M SODIMM_REV DDR3 CH B	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE:	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 15 OF 62	



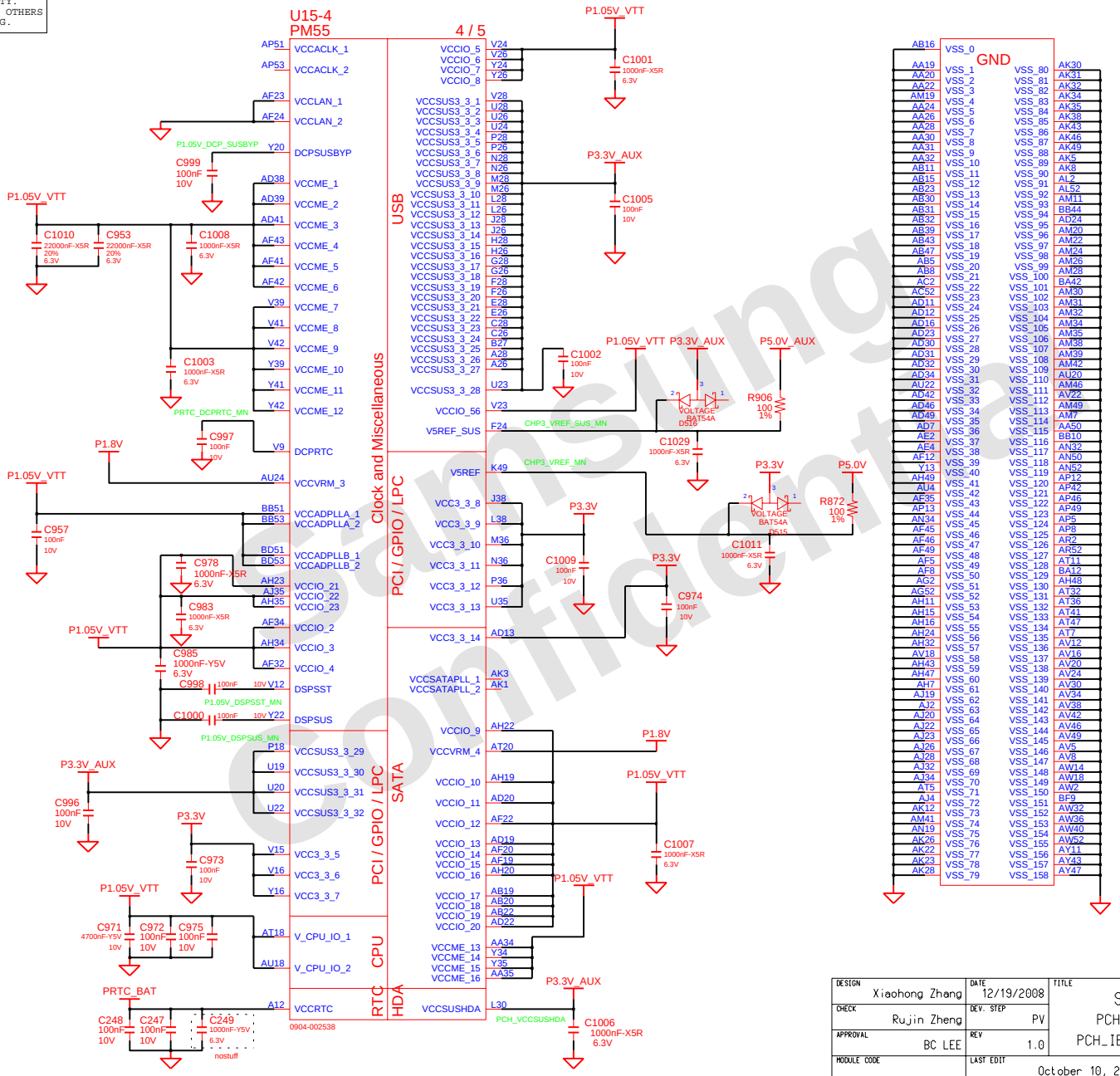


DESIGN: Xiaohong Zhang	DATE: 12/19/2008	TITLE: Suzhou_M PCH_IBEAX PEAK PCH_IBEAX PEAK(2/6)	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE:	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 17 OF 62	

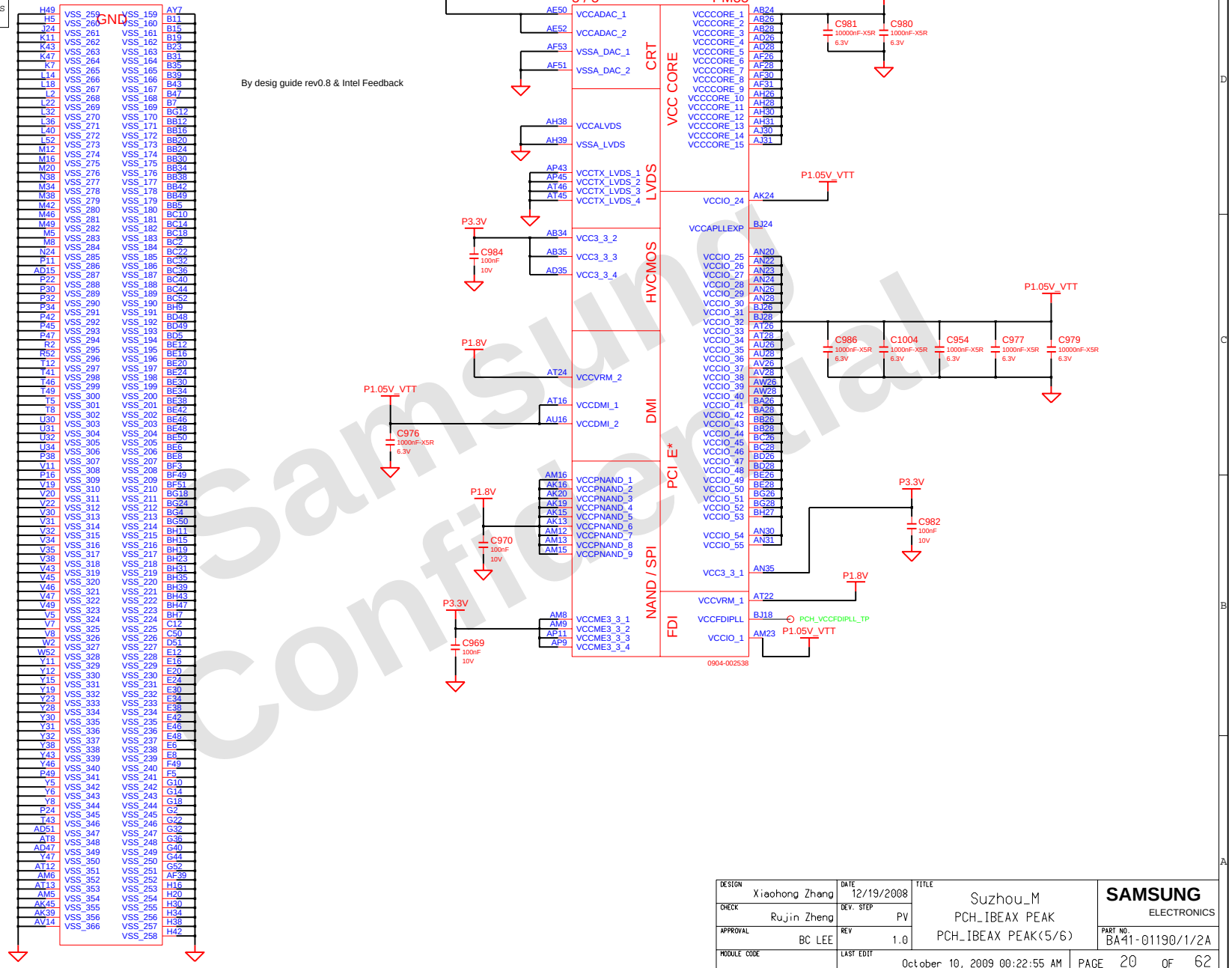


DESIGN: Xiaohong Zhang	DATE: 12/19/2008	TITLE: Suzhou_M PCH_IBEAX PEAK PCH_IBEAX PEAK(3/6)	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE:	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 18 OF 62	

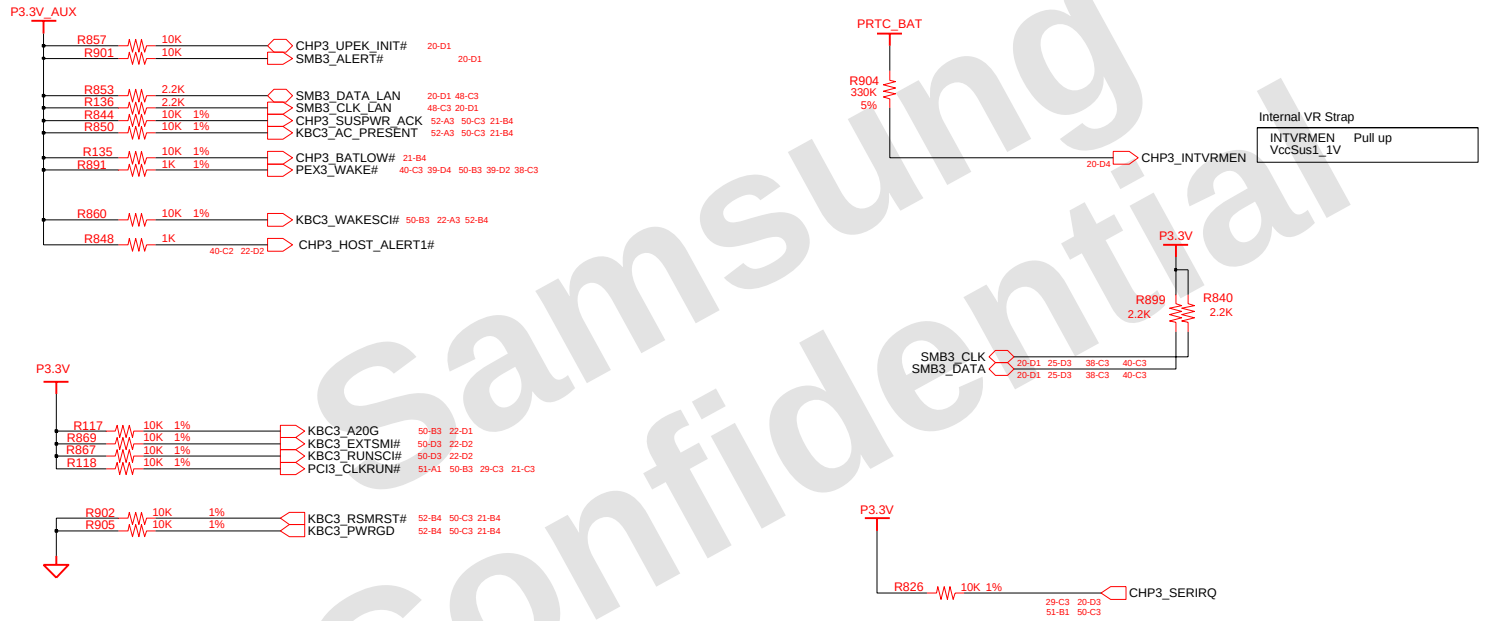
P1.1V,P1.1V_M is P1.05V & P1.05V_M ACTUALLY



DESIGN: Xiaohong Zhang	DATE: 12/19/2008	TITLE: Suzhou_M PCH_IBEAX PEAK PCH_IBEAX PEAK(4/6)	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE:	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 19 OF 62	

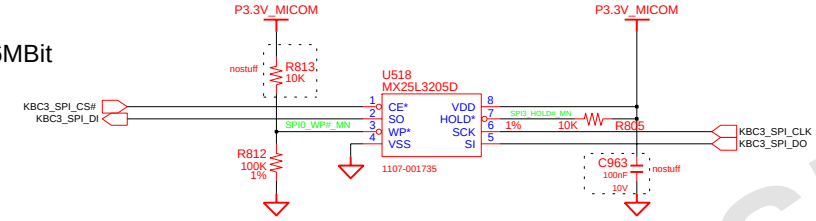


DESIGN: Xiaohong Zhang	DATE: 12/19/2008	TITLE: Suzhou_M	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV	PCH_IBEAX PEAK	
APPROVAL: BC LEE	REV: 1.0	PCH_IBEAX PEAK(5/6)	PART NO.: BA41-01190/1/2A
MODULE CODE:	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 20 OF 62	



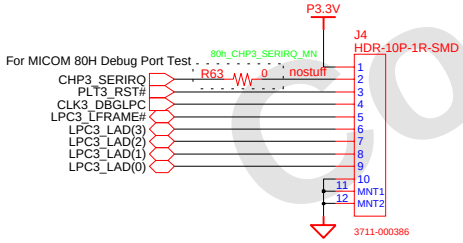
SPI_BIOS_ROM

16MBit



02 VERIFY REAL MODE	66 CONFIGURE ADVANCE CACHE REG.
03 DISABLE NMI	6A DISPLAY EXTERNAL CACHE SIZE
04 GET CPU TYPE	6C DISPLAY SHADOW MESSAGE
06 INIT. SYSTEM H/W	6E DISPLAY NON-DISPOSABLE SEGMENT
08 INIT. CHIPSET REG.	70 DISPLAY ERROR MESSAGE
09 SET IN POST FLAG	72 CHECK FOR CONFIGURATION ERROR
0A INIT CPU REG	74 TEST REAL-TIME CLOCK
0B CPU CACHE ON	76 CHECK FOR KEYBOARD EERROR
0C INIT.CACHE TO POST	7C SETUP HARDWARE INTERRUPT VECTOR
OE INIT. I/O VALUE	7E TEST COPROCESSER IF PRESENT
0F ENABLE THE L-BUS IDE	80 DISABLE ON-BOARD I/O PORT
10 INIT. POWER MANAGER	82 DETECT AND INSTALL EXT.RS232C
11 LOAD ALTERNATE REG.	84 DETECT AND INSTALL EXT.PARALLEL
13 PCI BUS MASTER RESET	86 RE-INIT. ON-BOARD I/O PORT
	88 INIT. BIOS DATA ROM
WITH INITIAL POST VALUE	8A INIT.EXTENDED BIOS DATA AREA
14 INIT. KEYBOARD CONTROLLER	8C INIT.FDD CONTROLLER
16 CHECK CHECKSUM	9A SHADOW OPTION ROMS
18 8254 TIMER INIT.	9C SETUP POWER MANAGEMENT
1A 8237 DMA CONTROLLER INIT.	9E ENABLE H/W INTERRUPT
1C RESET INTERRUP CONTROLLER	A0 SET TIME OF DAY
20 TEST DRAM REFRESH	A4 INIT. TYPEMATIC RATE
22 TEST 8742 KEYBOARD CONTROLLER	A8 ERASE F2 PROMPT
24 SET ES SEGMENT REG. TO 4GB	AA SCAN FOR F2 KEY STROKE
26 ENABLE A20	AC ENTER SETUP
28 AUTO SIZING DRAM	AE CLEAR IN POST FLAG
32 COMPUTE THE CPU SPEED	B0 CHECK FOR ERRORS
34 TESET CMOS RAM	B2 POST DONE-PREPARE TO BOOT O/S
38 SHADOW SYSTEM BIOS ROM	B4 ONE BEEP
3A AUTO SIZING CACHE	B6 CHECK PASSWORD (OPTION)
3C CONFIGURE ADVANCED CHIPSET REG.	B7 ACPI INIT
3D LOAD ALTER REG. WITH CMOS VALUE	BA DMI INIT
42 INIT. INTERRUPT VECTOR	BE CLEAR SCREEN
44 INIT. BIOS INTERRUPT	C0 TRY BOOT WITH INT19
46 CHECK ROM COPYRIGHT NOTICE	D0 INTERRUPT HANDLER ERROR
47 INIT. I20 SUPPORT IF INSTALLED	D2 UNKNOWN INTERRUPT ERROR
48 CHECK VIDEO CONFIGURE AGAINST CMOS	D4 PENDING INTERRUPT ERROR
49 INIT. PCI BUS AND DEVICE	D6 SHUTDOWN 5
4A INIT. ALL VIDEO BIOS ROM	D8 SHUTDOWN ERROR
4C SHADOW VIDEO BIOS ROM	DA EXTENDED BLOCK MOVE
50 DISPLAY CPU TYPE AND SPEED	DC SHUTDOWN 10
52 TEST KEYBOARD	89 ENABLE NMI
54 SET KEYCLICK IF ENABLED	90 INIT. HDD CONTROLLER
56 ENABLE KEYBOARD	91 INIT. LOCAL BUS HDD CONTROLLER
58 TEST FOR UNEXPECTED INTERRUPTS	92 JUMP TO USER PATCH 2
5A DISPLAY " PRESS ..... SETUP"	94 DISABLE A20 ADDRESS LINE
5C TEST RAM GETWEEN 512K AND 640K	96 CLEAR HUGE ES SEGMENT REG.
60 TEST EXTENDED MEMORY	98 SEARCH FOR OPTION ROMS
62 TEST EXTENDED MEMORY ADDRESS LINE	
64 JUMP TO USER PATCH 1	

80H DECODER CONNECTOR



DRAW: Xiaohong Zhang	DATE: 8/12/2006	TITLE: Suzhou_M SPI_BIOS_ROM SPI_BIOS_ROM	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE:	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 22 OF 62	

U5-1
N11P-GE1-B-A3 1 / 5

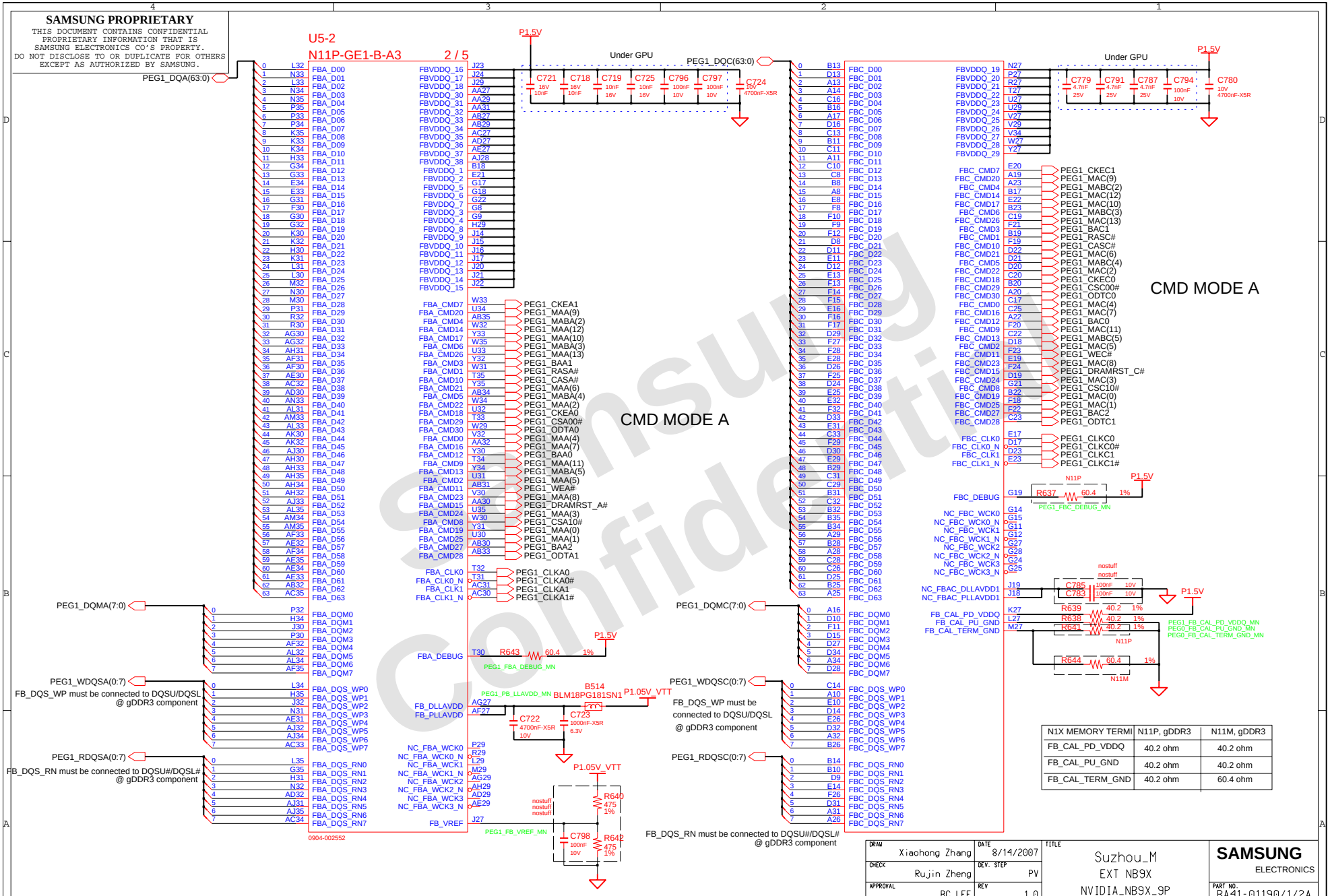
PEG3_LCDVDDON & PEG3_BKLTEN
PDs are locate in connector

VOLTID0, 1 PU & PD ARE LOCATE IN POWER

DRAW: Xiaohong Zhang	DATE: 8/14/2007	TITLE: Suzhou_M EXT NB9X NVIDIA_NB9X_9P	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE:	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 23 OF 62	

U5-2

N11P-GE1-B-A3 2 / 5

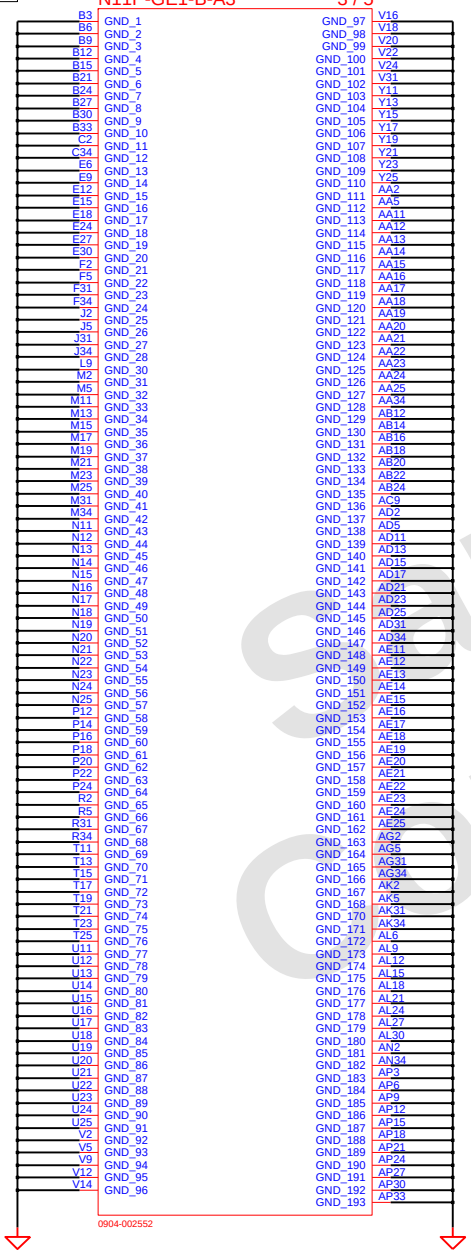


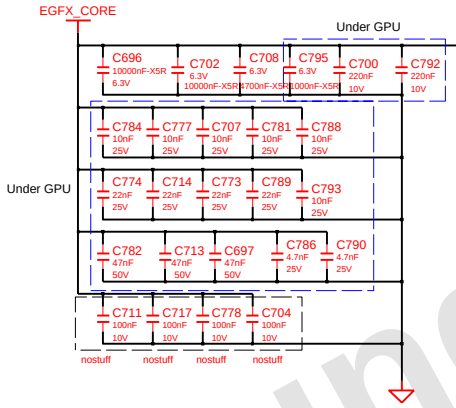
N1X MEMORY TERMI	N11P, gDDR3	N11M, gDDR3
FB_CAL_PD_VDDQ	40.2 ohm	40.2 ohm
FB_CAL_PU_GND	40.2 ohm	40.2 ohm
FB_CAL_TERM_GND	40.2 ohm	60.4 ohm

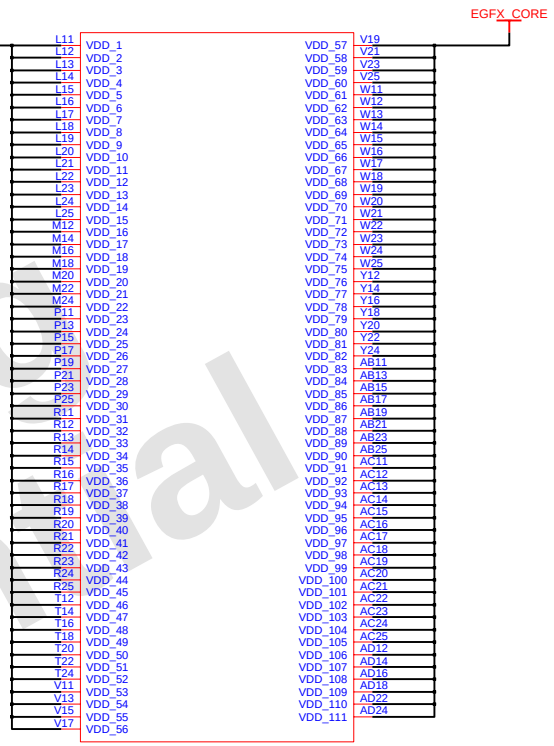
DRAW: Xiaohong Zhang	DATE: 8/14/2007	TITLE: Suzhou_M EXT NB9X NVIDIA_NB9X_9P	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 24 OF 62	

U5-3

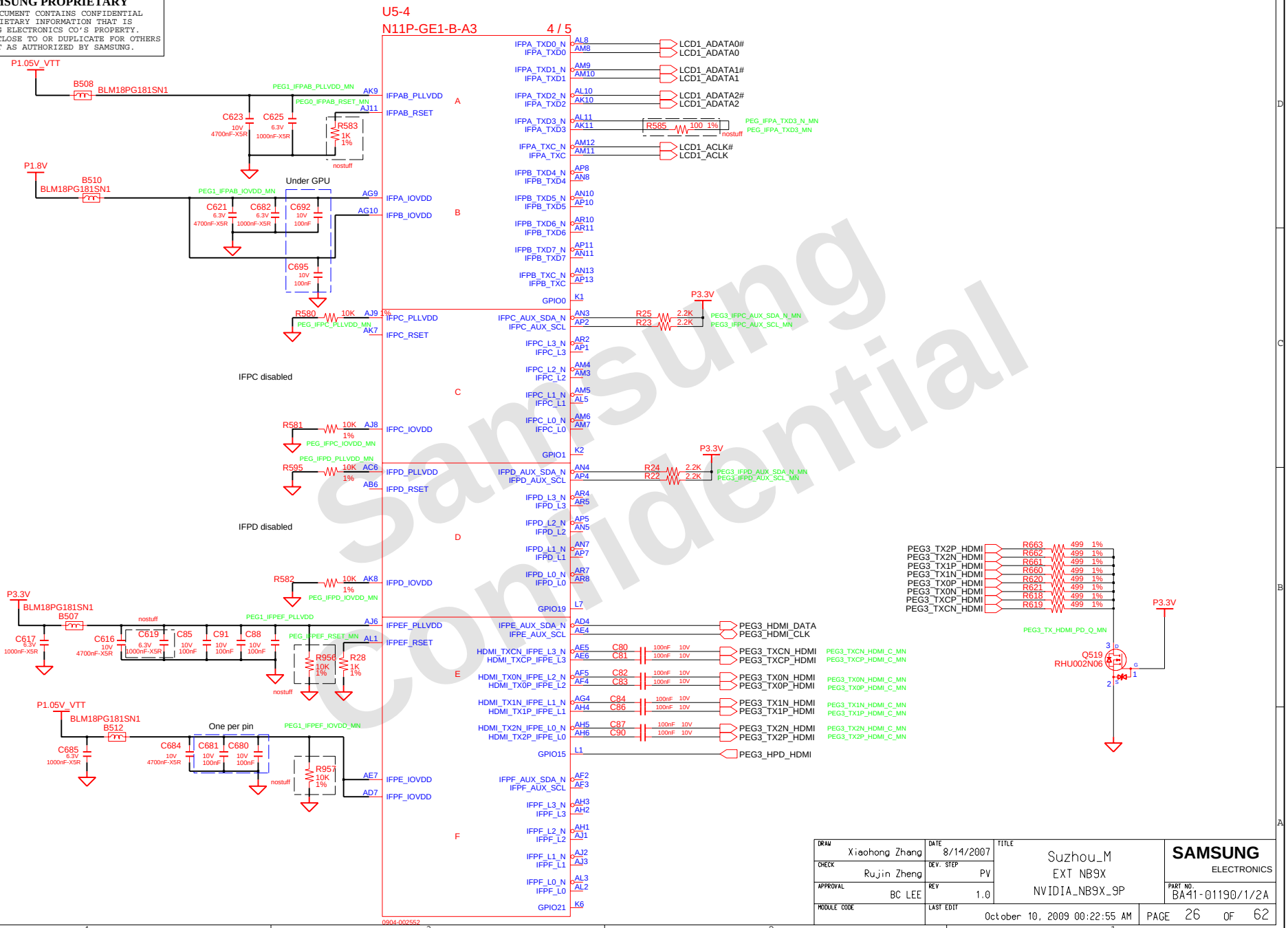
N11P-GE1-B-A3 3 / 5



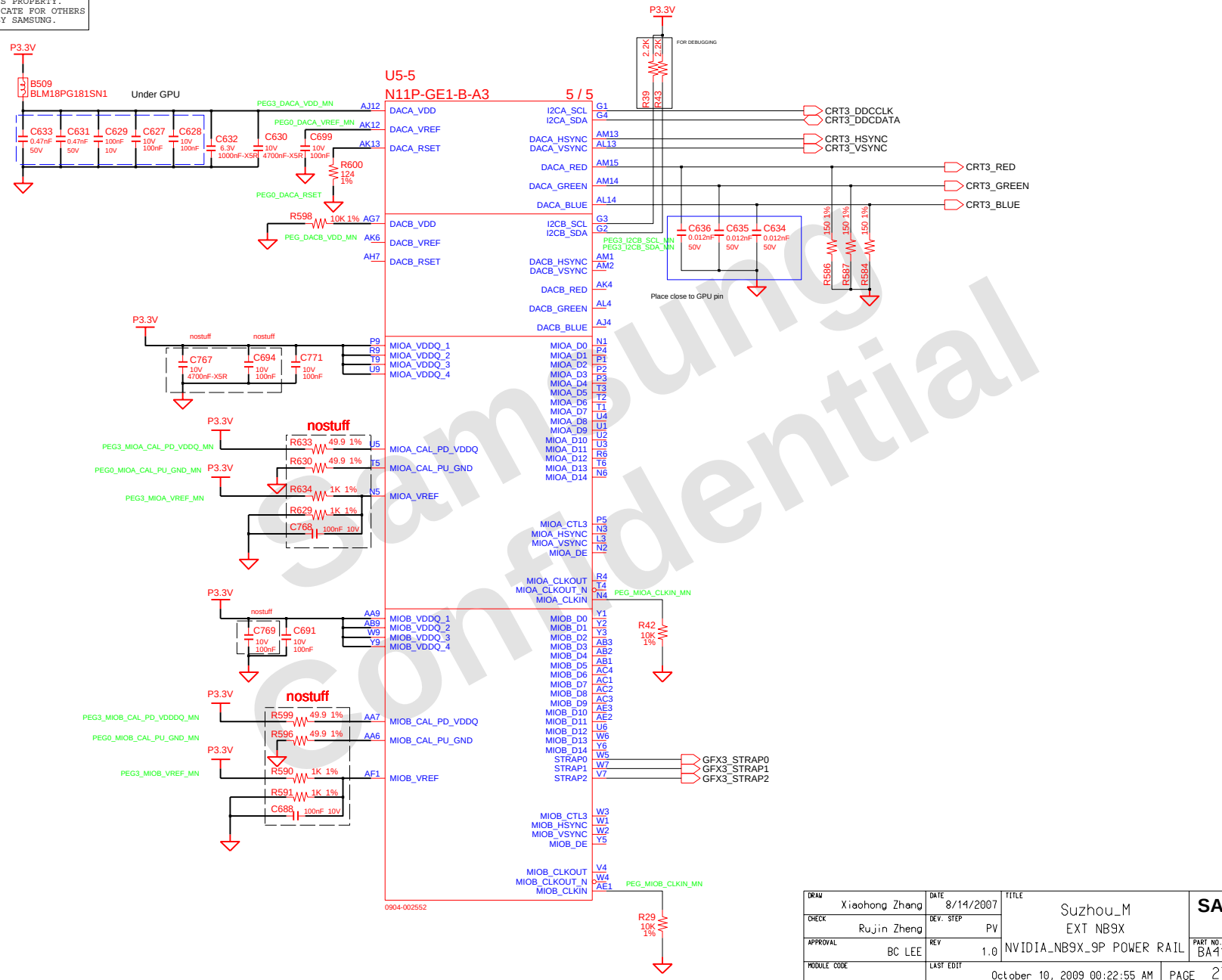




DRAW: Xiaohong Zhang	DATE: 8/14/2007	TITLE: Suzhou_M EXT NB9X NB9X CHIP (3/4)	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE:	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 25 OF 62	



DRAW: Xiaohong Zhang	DATE: 8/14/2007	TITLE: Suzhou_M EXT NB9X NVIDIA_NB9X_9P	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 26 OF 62	



DRAW: Xiaohong Zhang	DATE: 8/14/2007	TITLE: Suzhou_M EXT NB9X NVIDIA_NB9X_9P POWER RAIL	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE:	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 27 OF 62	

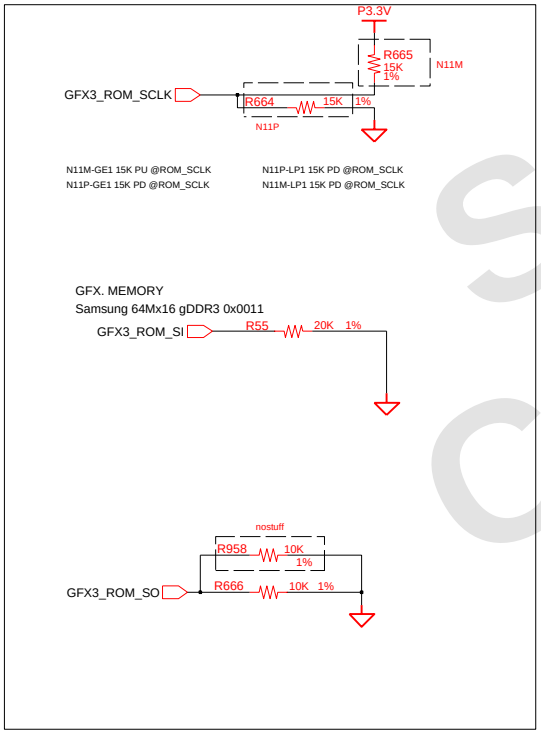
N11x_40nm STRAP

Pin	Description	Activate
GPIO(0)	General Purpose	NC
GPIO(1)	HPD-C	NC
GPIO(2)	LCD0_BL_PWM	High
GPIO(3)	LCD0_VDD	High
GPIO(4)	LCD0_BL_EN	High
GPIO(5)	GPU VID0	00 0.8v 10 0.95v
GPIO(6)	GPU_VID1	01 0.85v 11 1.03v
GPIO(7)	GPU VID2	NC
GPIO(8)	OVERT	LOW
GPIO(9)	ALERT	NC
GPIO(10)	MEM_VREF	NC
GPIO11)	SLI_SYNC	NC

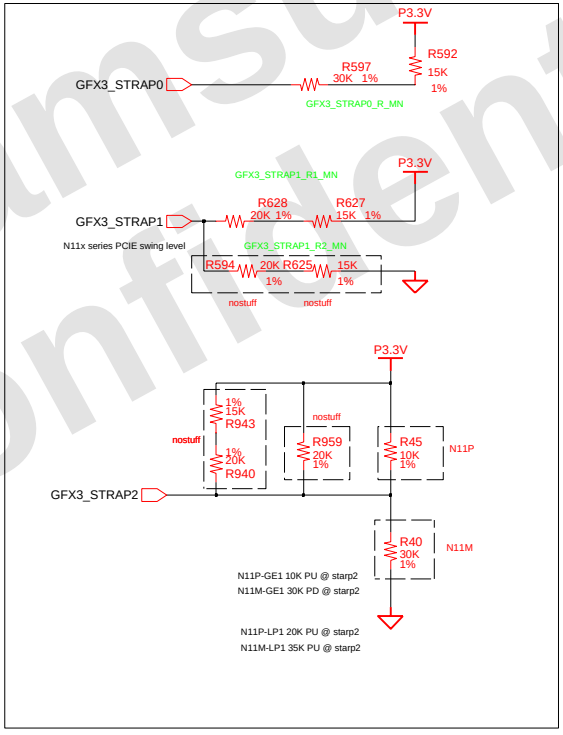
Pin	Description	Activate
GPIO(12)	PWR_LEVEL	NC
GPIO(13)	MEM_VID	NC
GPIO(14)	PWR_CTRL1	NC
GPIO(15)	HPD-E	High
GPIO(16)	FAN_PWM	NC
GPIO(17)	Reserved	NC
GPIO(18)	Reserved	NC
GPIO(19)	HPD-D	NC

STRAP PIN	BIT 3	BIT 2	BIT 1	BIT0
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]

RESISTOR	PULL UP	PULL DOWN
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



N11P-GE1 0xA29
N11M-GE1 0x0A75



N11P-GE1

	Bit3	Bit2	Bit1	Bit0	
ROMSO	0	0	0	1	27M
SCLK	0	0	1	0	DEVICE ID GFX TPYE
SI	0	0	1	1	gDDR3 1Gb
Strap2	1	0	0	1	N11P-GE1 DEVICE ID
Strap1	1	1	1	0	PEG PCIE swing level
Strap0	1	1	1	1	EDID_EN

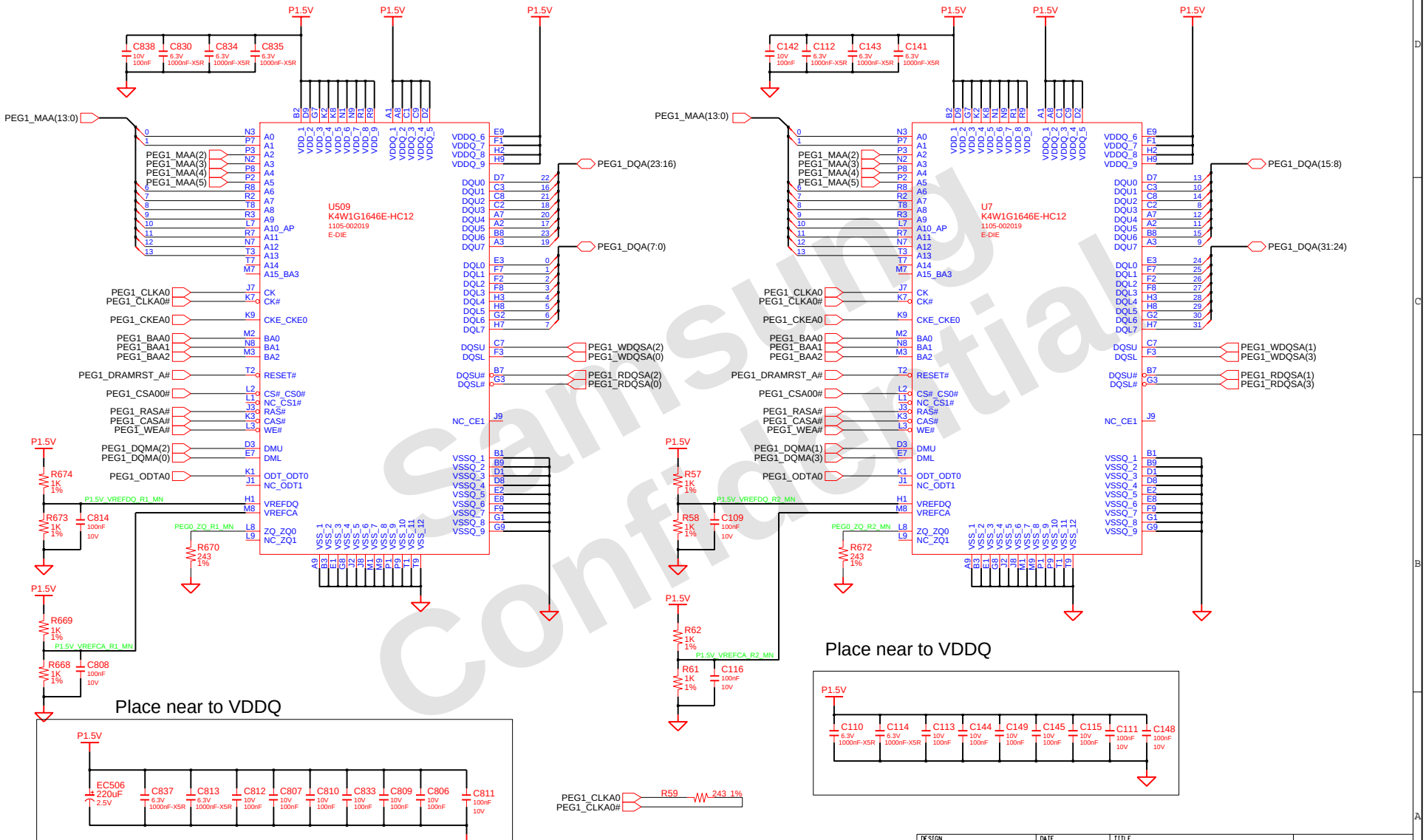
N11P-GE1 0x0A29

N11M-GE1

	Bit3	Bit2	Bit1	Bit0	
ROMSO	0	0	0	1	27M
SCLK	0	0	1	0	DEVICE ID GFX TPYE
SI	0	0	1	1	gDDR3 1Gb
Strap2	0	1	0	1	N11P-GE1 DEVICE ID
Strap1	1	1	1	0	PEG PCIE swing level
Strap0	1	1	1	1	EDID_EN

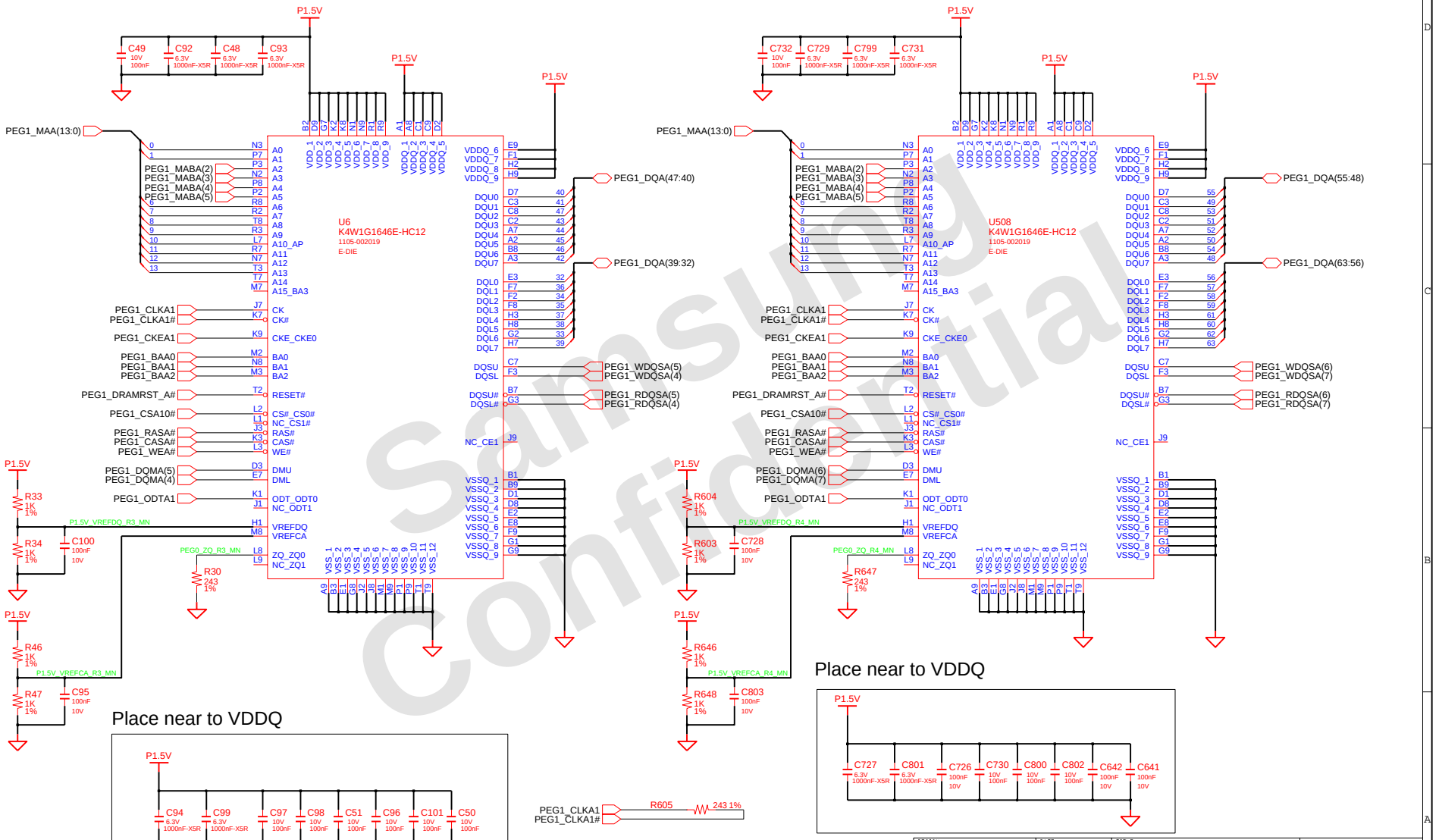
N11M-GE1 0x0A75

A-Channel #0



DESIGN: Xiaohong Zhang	DATE: 04/29/2009	TITLE: Suzhou_M GRAPHIC_MEM_1Gb A#0 gDDR3_1Gb	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 29 OF 62	

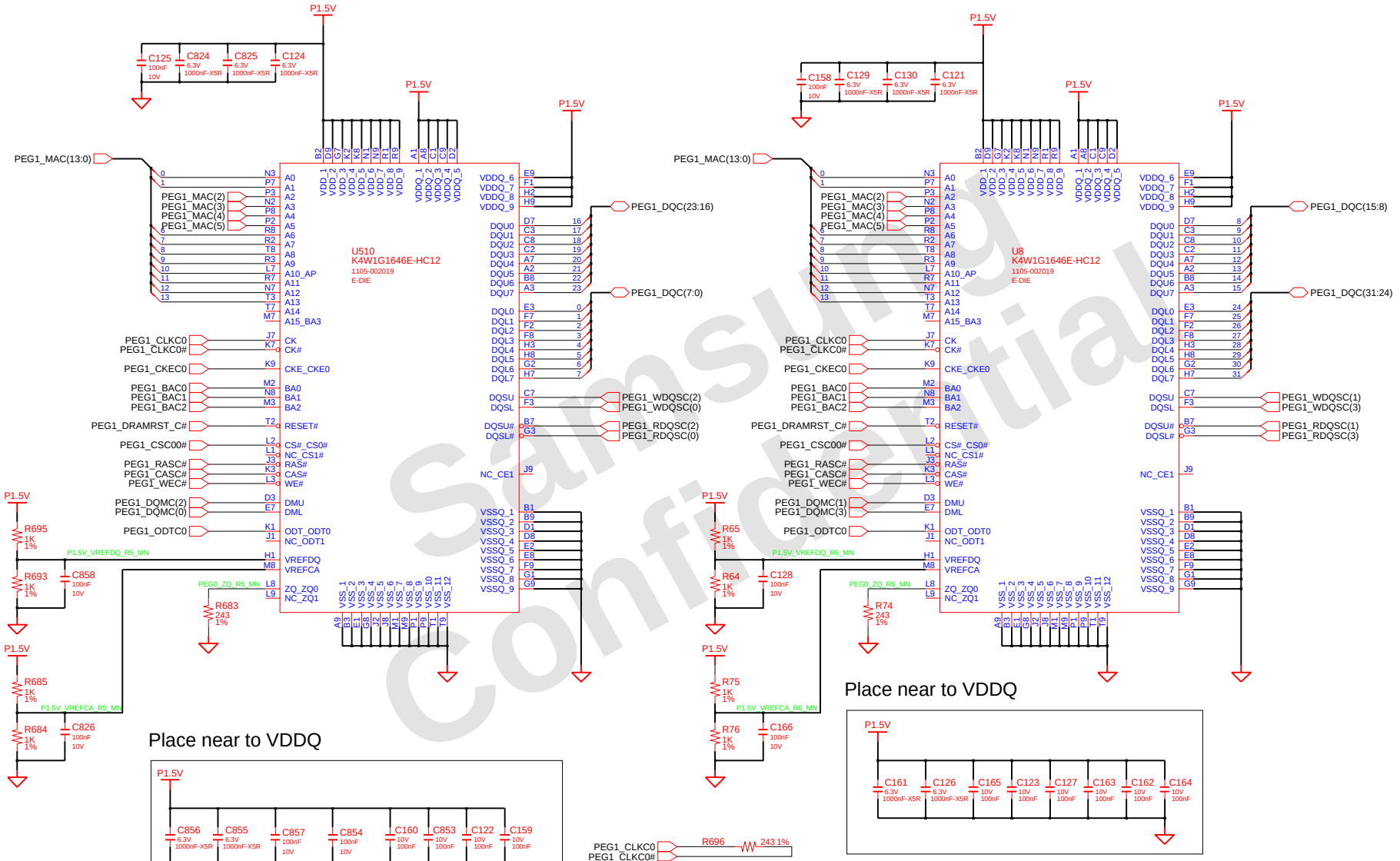
A-Channel #1



DESIGN: Xiaohong Zhang	DATE: 04/29/2009	TITLE: Suzhou_M GRAPHIC_MEM_1Gb A#1 gDDR3_1Gb	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 30 OF 62	

C-Channel #0

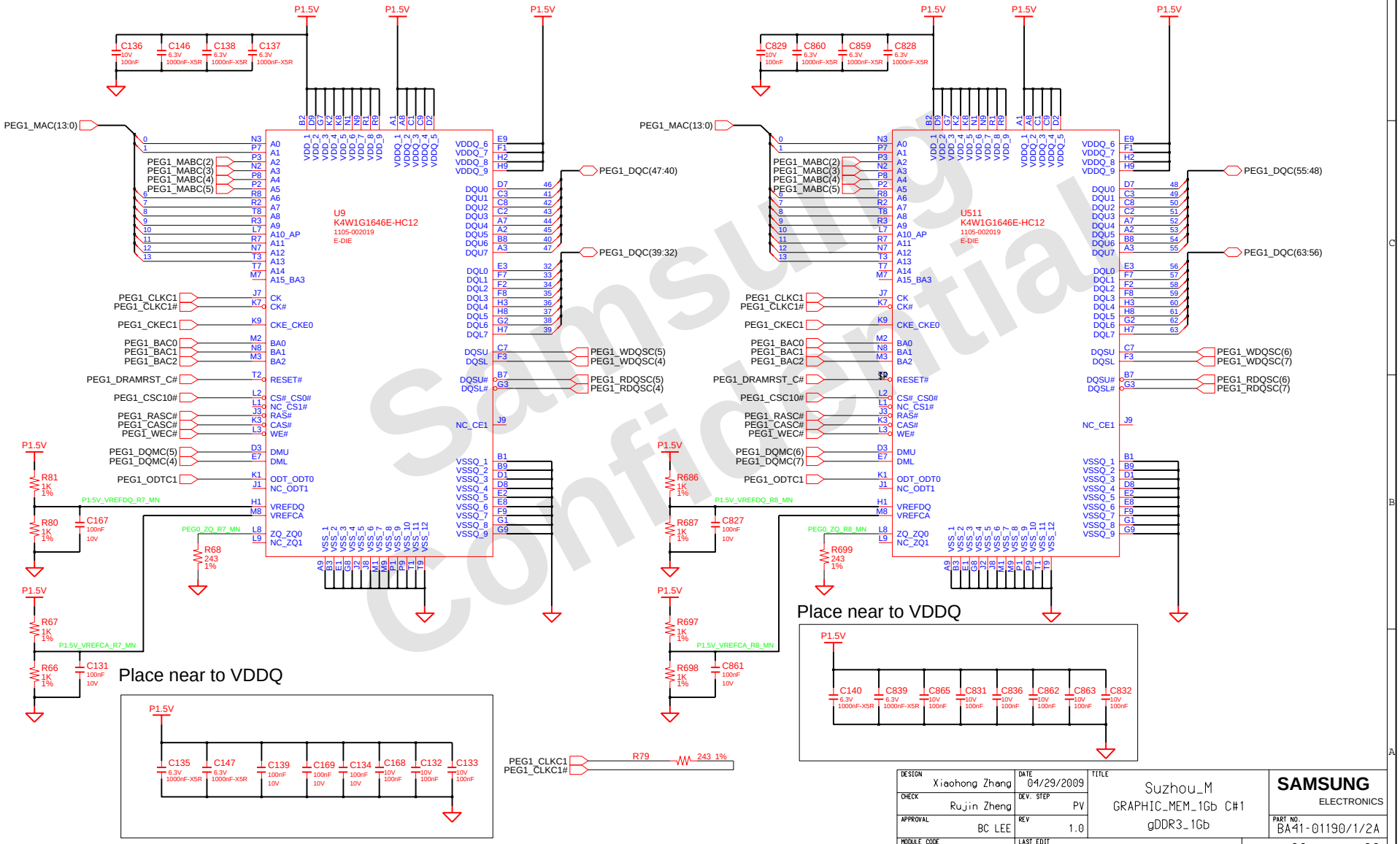
N11P



DESIGN: Xiaohong Zhang	DATE: 04/29/2009	TITLE: Suzhou_M GRAPHIC_MEM_1Gb C#0 gDDR3_1Gb	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 31 OF 62	

C-Channel #1

N11P

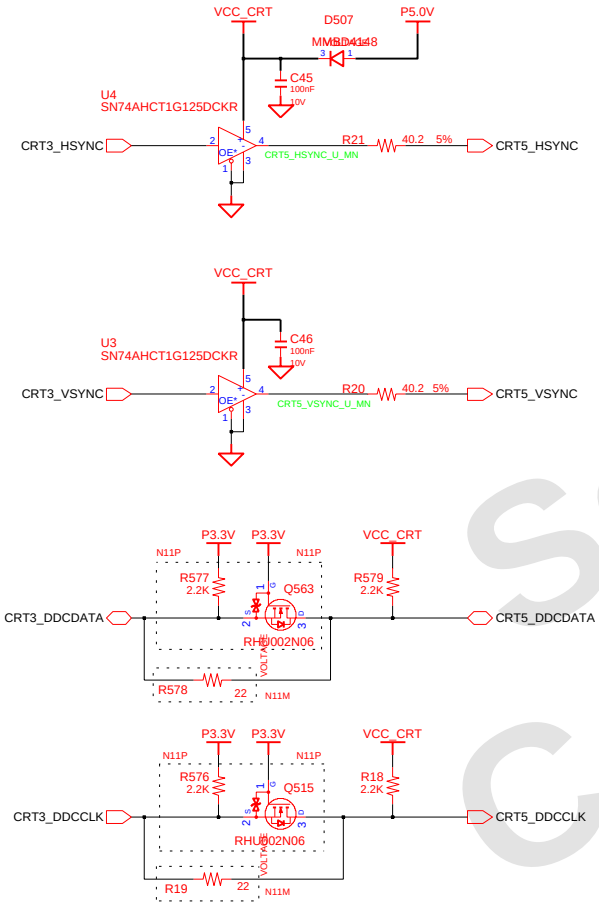


DESIGN: Xiaohong Zhang	DATE: 04/29/2009	TITLE: Suzhou_M GRAPHIC_MEM_1Gb C#1 gDDR3_1Gb	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE:	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 32 OF 62	

gDDR3 Memory PULL UP & PULL DOWN

DESIGN: Xiaohong Zhang	DATE: 03/14/2009	TITLE: Suzhou_M PULL-UP&PULL-DOWN gDDR3_1Gb	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE:	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 33 OF 62	

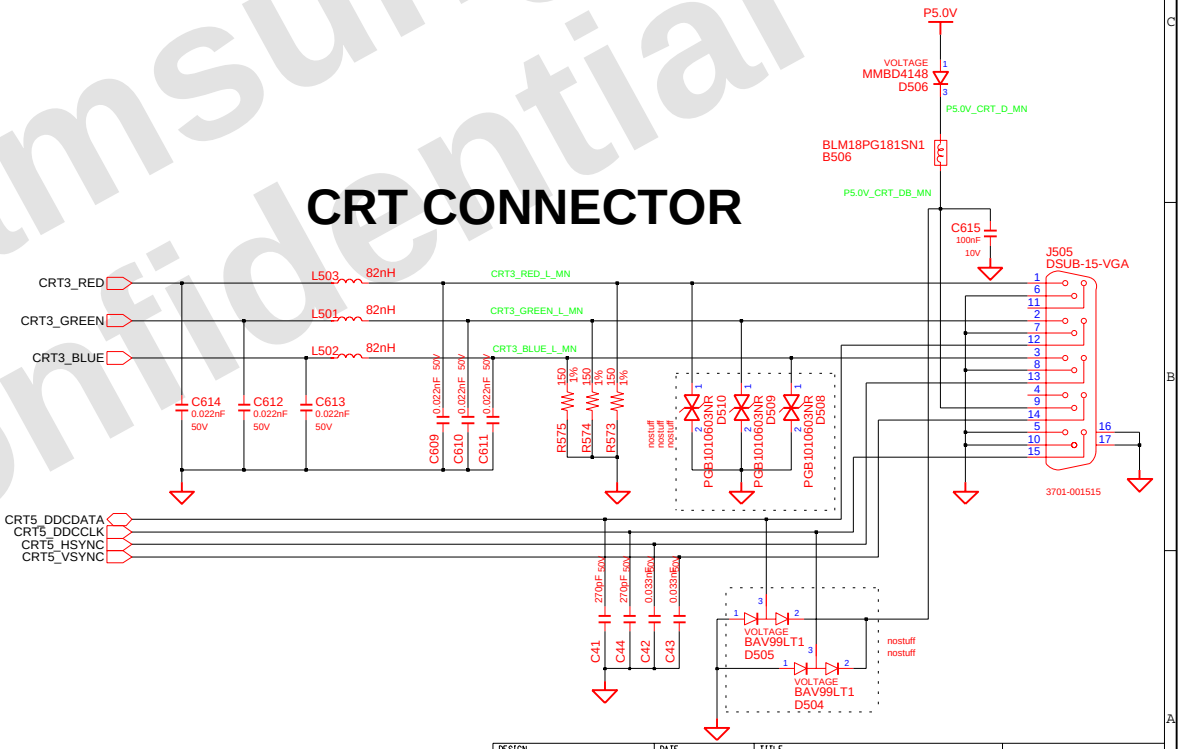
CRT



Check "CRT3_DDCCLK/DATA" Voltage Level

2N06 Can be replaced with SM6K2

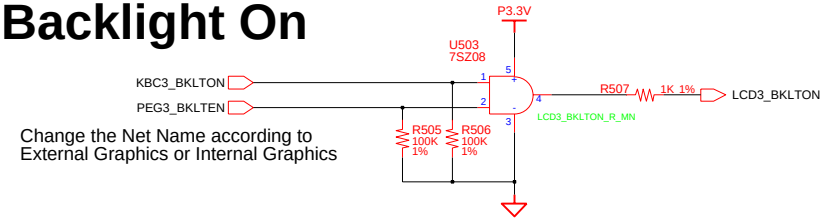
CRT CONNECTOR



DESIGN: Xiaohong Zhang	DATE: 01/08/2009	TITLE: Suzhou_M GRAPHICS_IF CRT	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE:	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 34 OF 62	

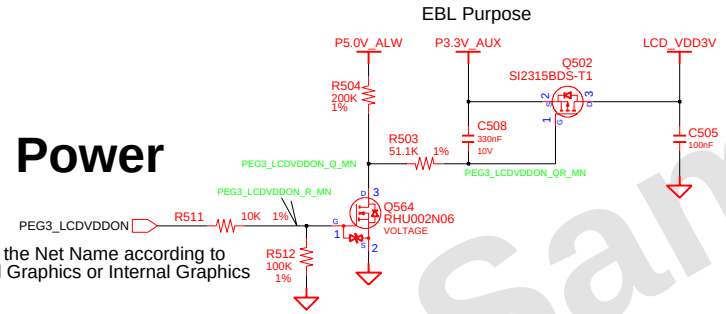
LVDS

Backlight On



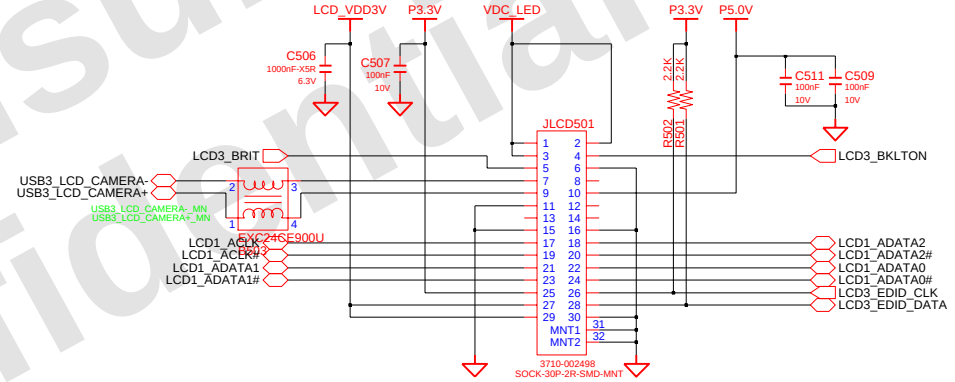
Change the Net Name according to
External Graphics or Internal Graphics

LCD Power

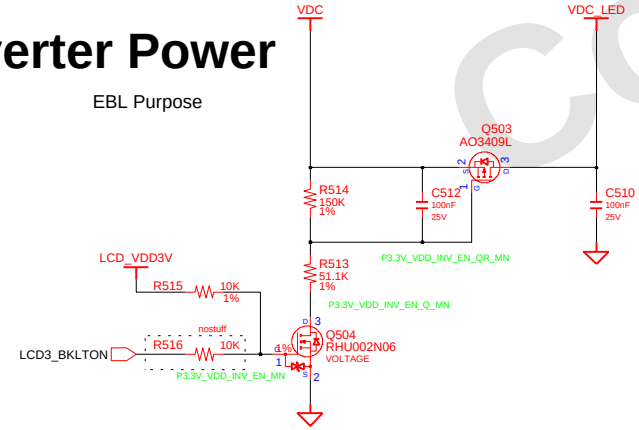


Change the Net Name according to
External Graphics or Internal Graphics

1Ch. LCD Connector



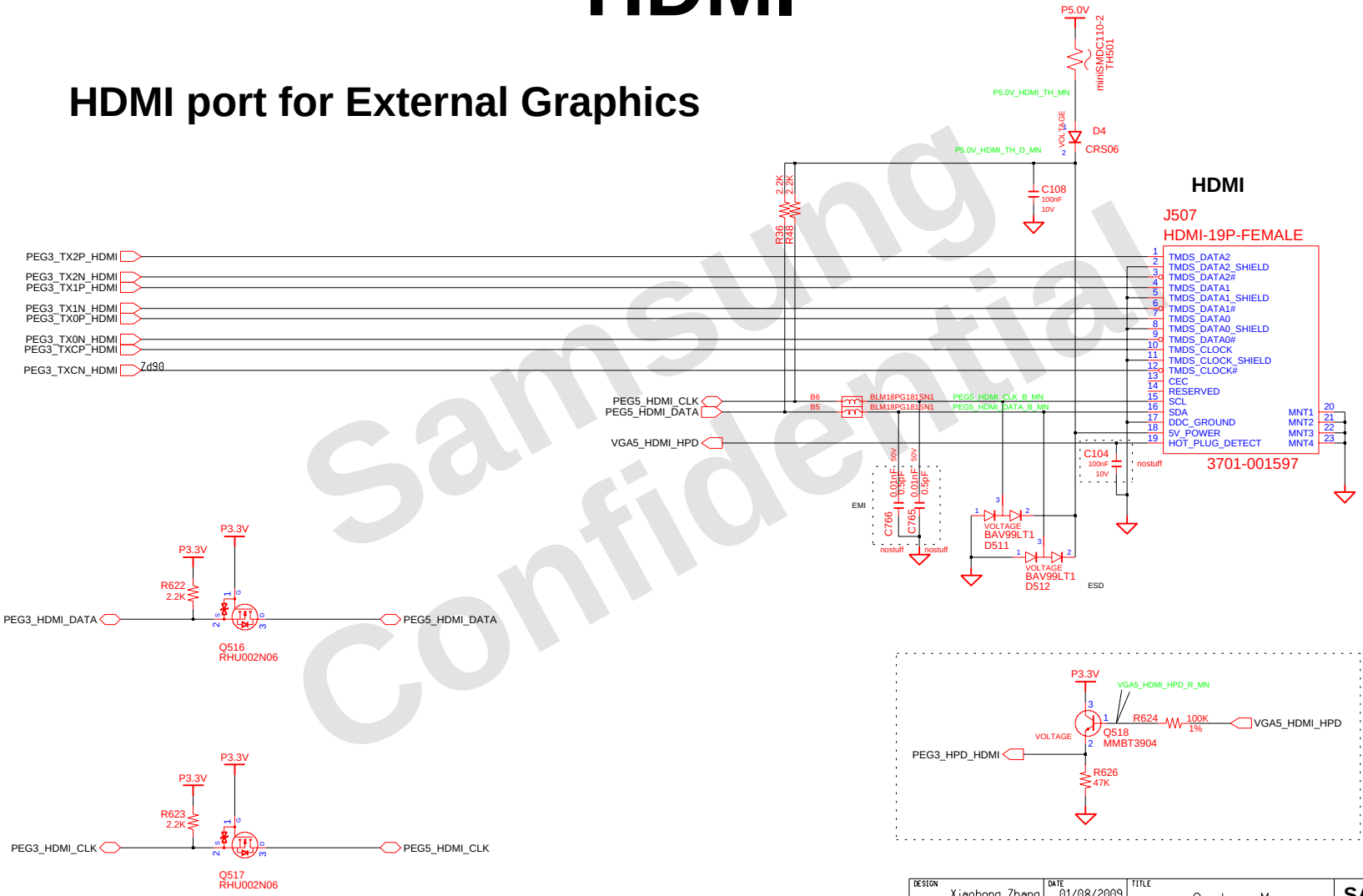
Inverter Power



DESIGN: Xiaohong Zhang	DATE: 01/08/2009	TITLE: Suzhou_M GRAPHICS_IF LVDS	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE:	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 35 OF 62	

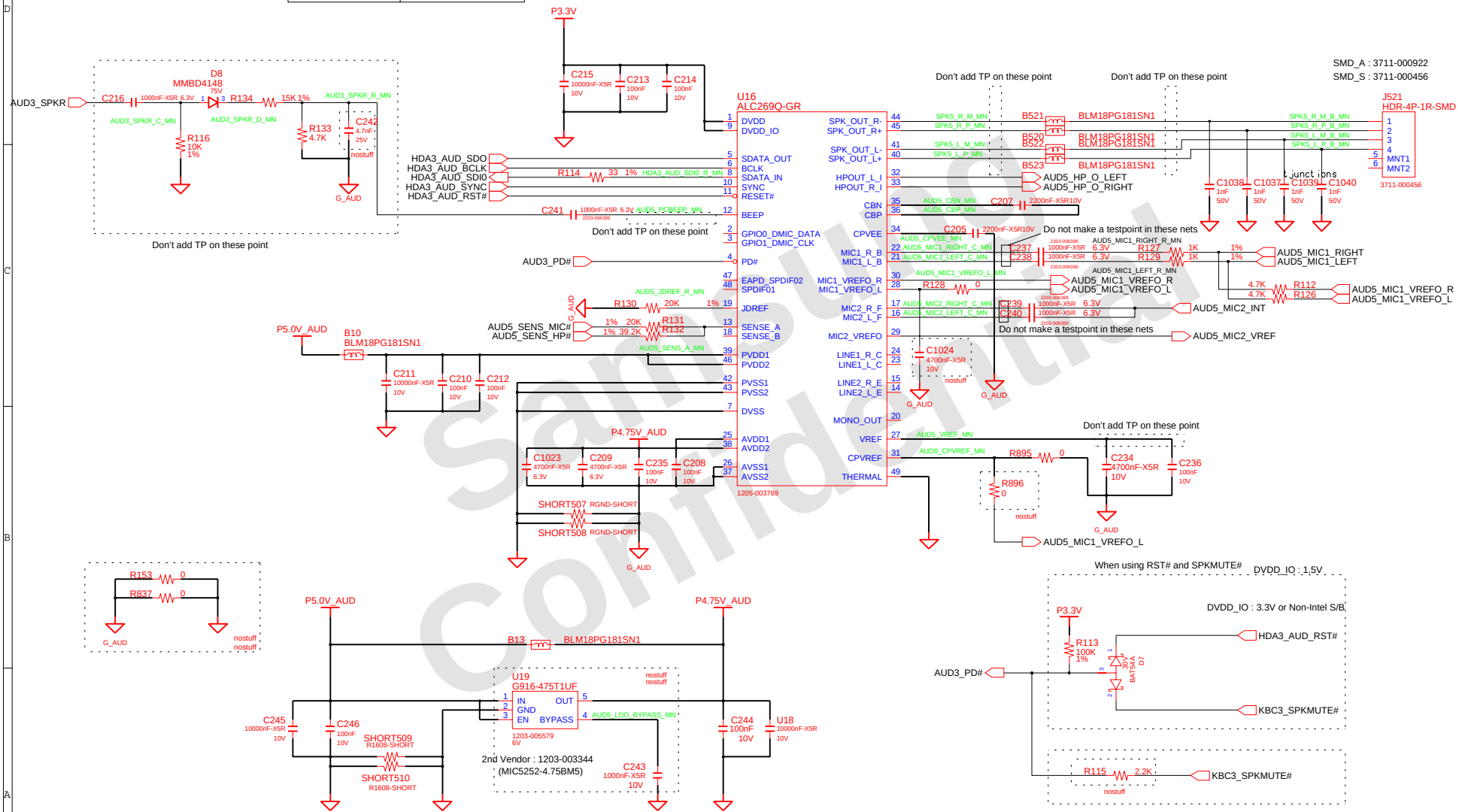
HDMI

HDMI port for External Graphics



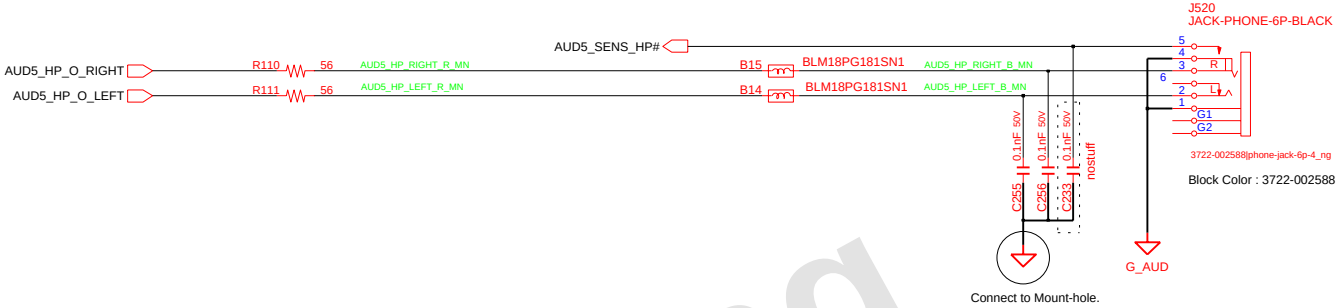
DESIGN: Xiaohong Zhang	DATE: 01/08/2009	TITLE: Suzhou_M GRAPHICS_IF HDMI	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE:	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 36 OF 62	

Codec Pin9 Setting	
S/B with Low Voltage IO	S/B without Low Voltage IO
Pin9 : 1.5V	Pin9 : 3.3V

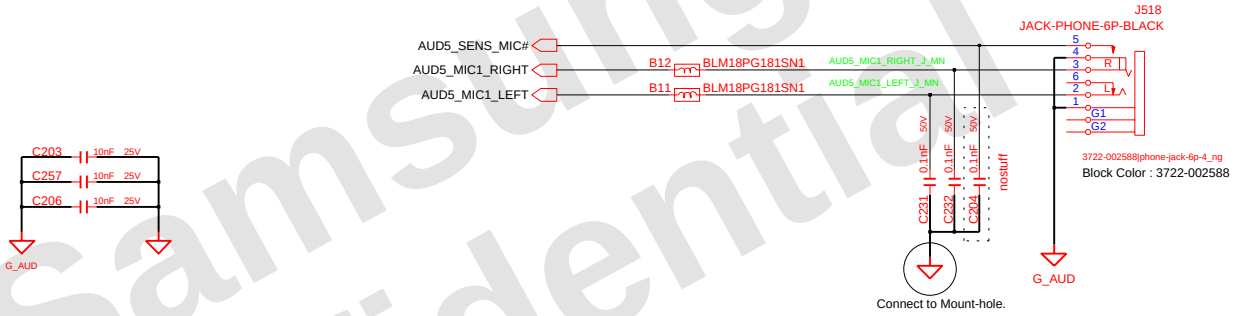


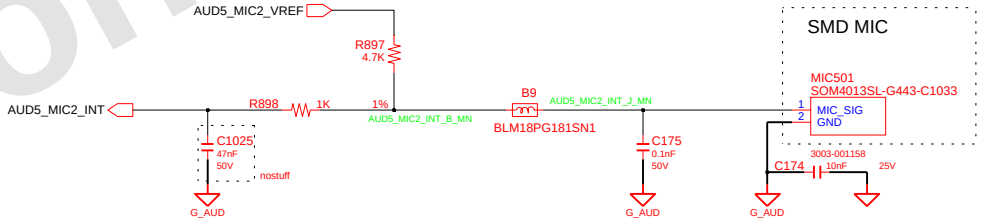
DESIGN: Xiaohong Zhang	DATE: 3/13/2009	TITLE: Suzhou_M HDA_ALC269_GR AUDIO CODEC	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE:	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 37 OF 62	

HEADPHONE

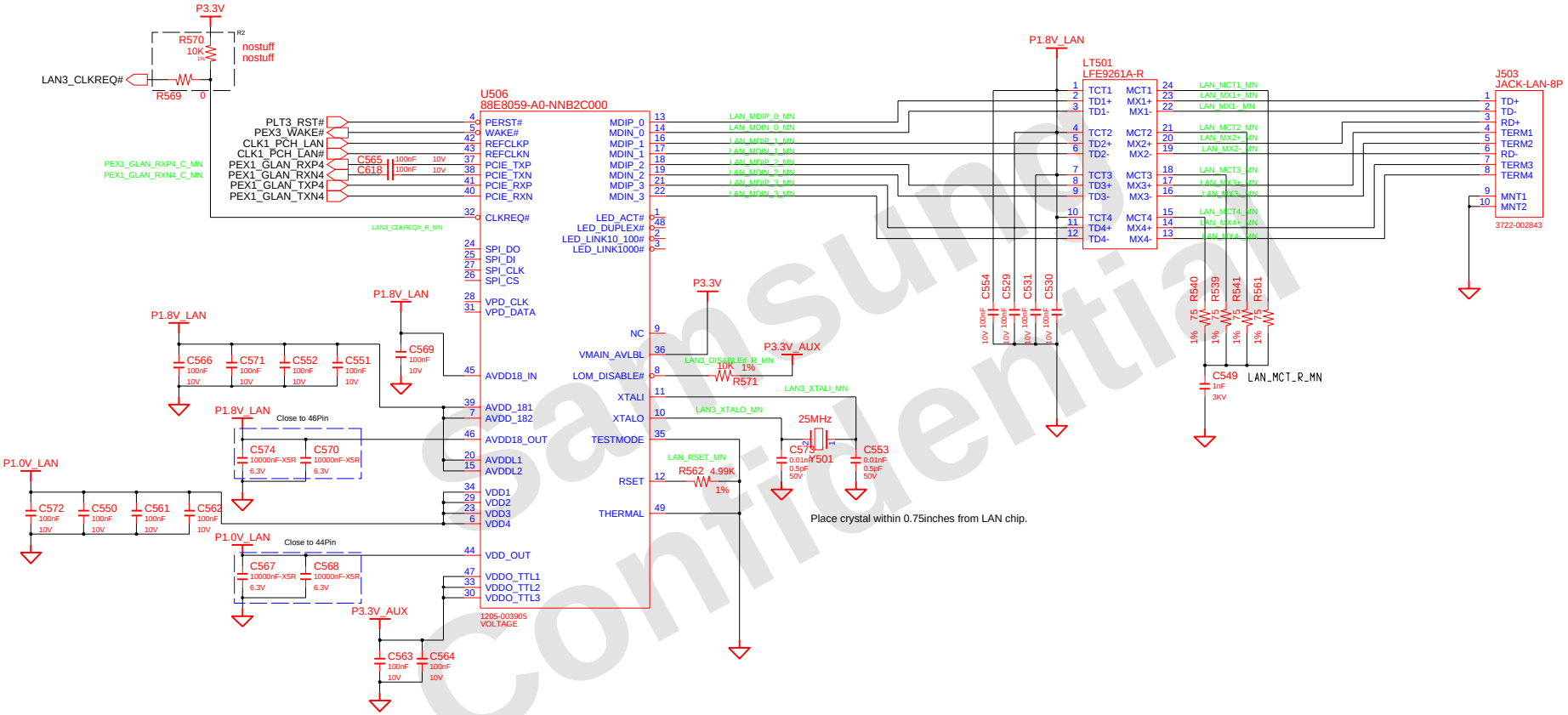


MIC JACK



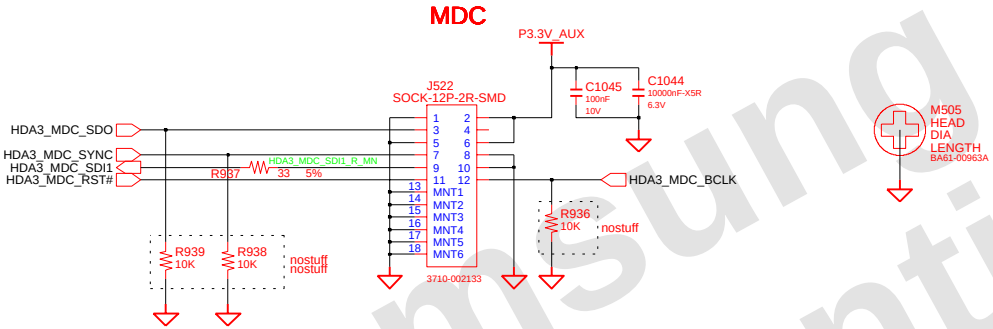


DESIGN: Xiaohong Zhang	DATE: 3/13/2009	TITLE: Suzhou_M HDA_ALC269_GR AUDIO INPUT/OUTPUT	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE:	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 38 OF 62	

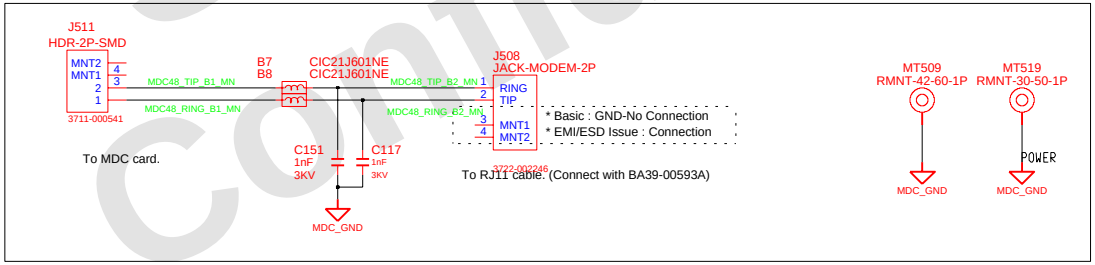


DESIGN: Xiaohong Zhang	DATE: 10/6/2008	TITLE: Suzhou_M	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 39 OF 62	

MDC Connecter



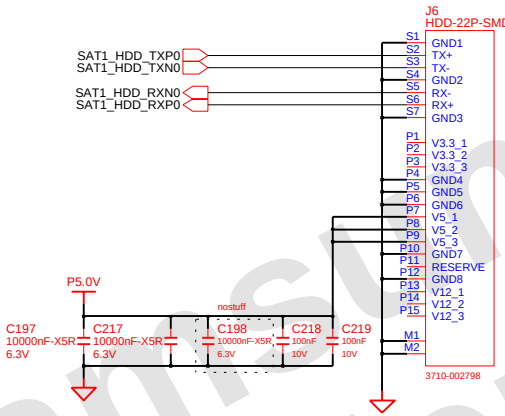
MDC SUB



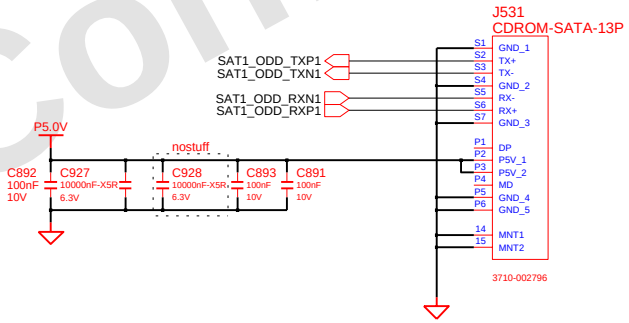
DESIGN: Xiaohong Zhang	DATE: 8/20/2009	TITLE: Suzhou_M UNDEFINED UNDEFINED	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE:	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 40 OF 62	

SATA I/F CONN

SATA HDD CONN

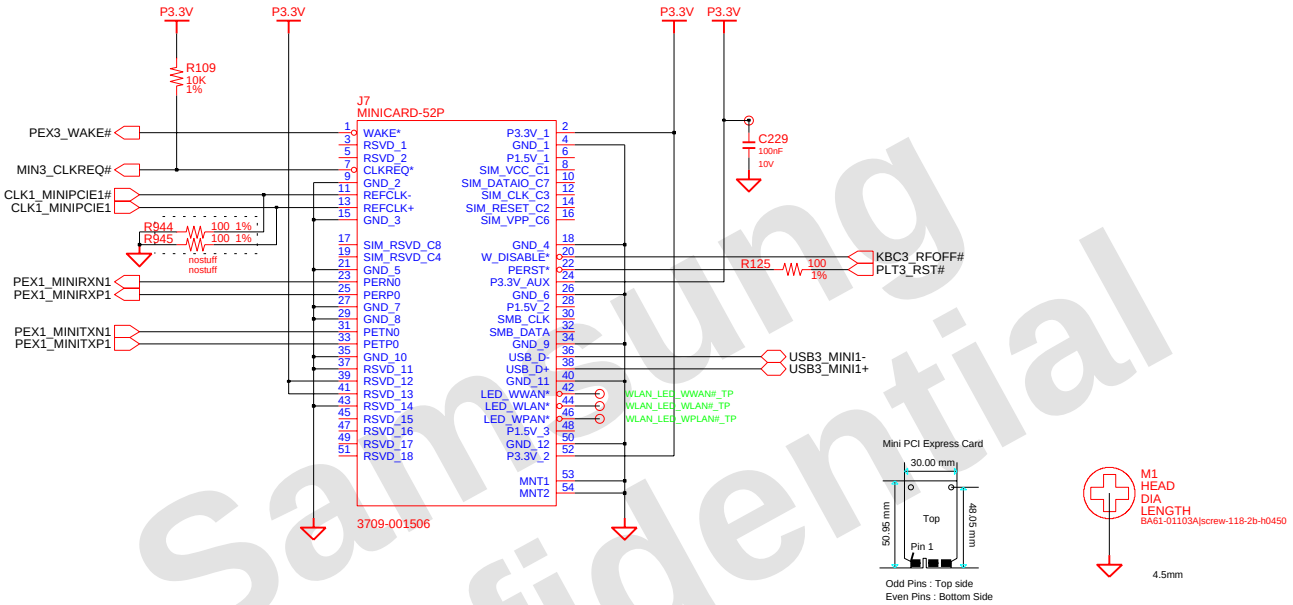


SATA ODD CONN



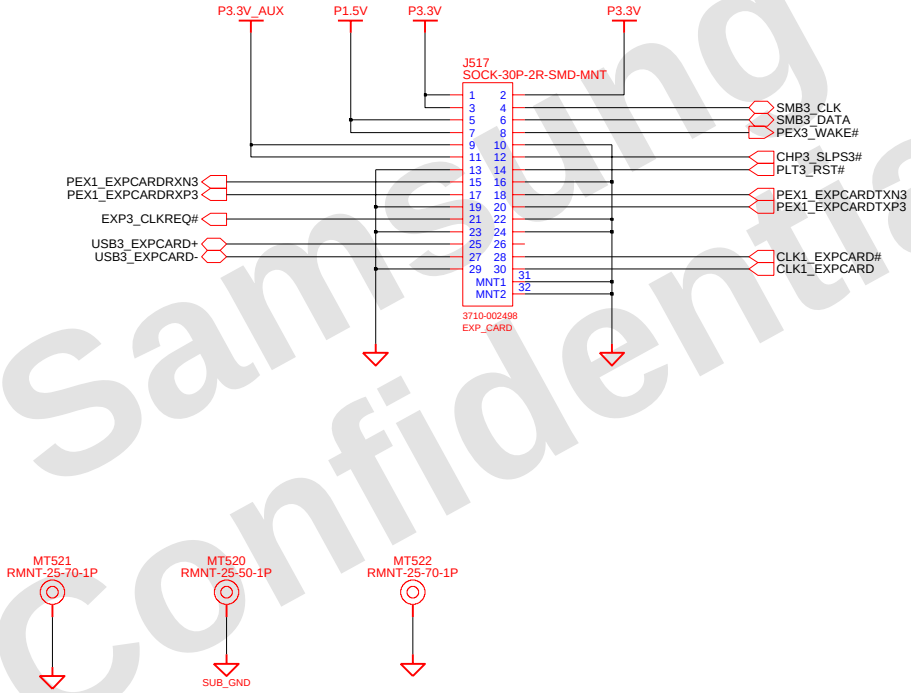
DESIGN: Xiaohong Zhang	DATE: 6/6/2008	TITLE: Suzhou_M SATA_DEVICES	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 41 OF 62	

WLAN, 7mm



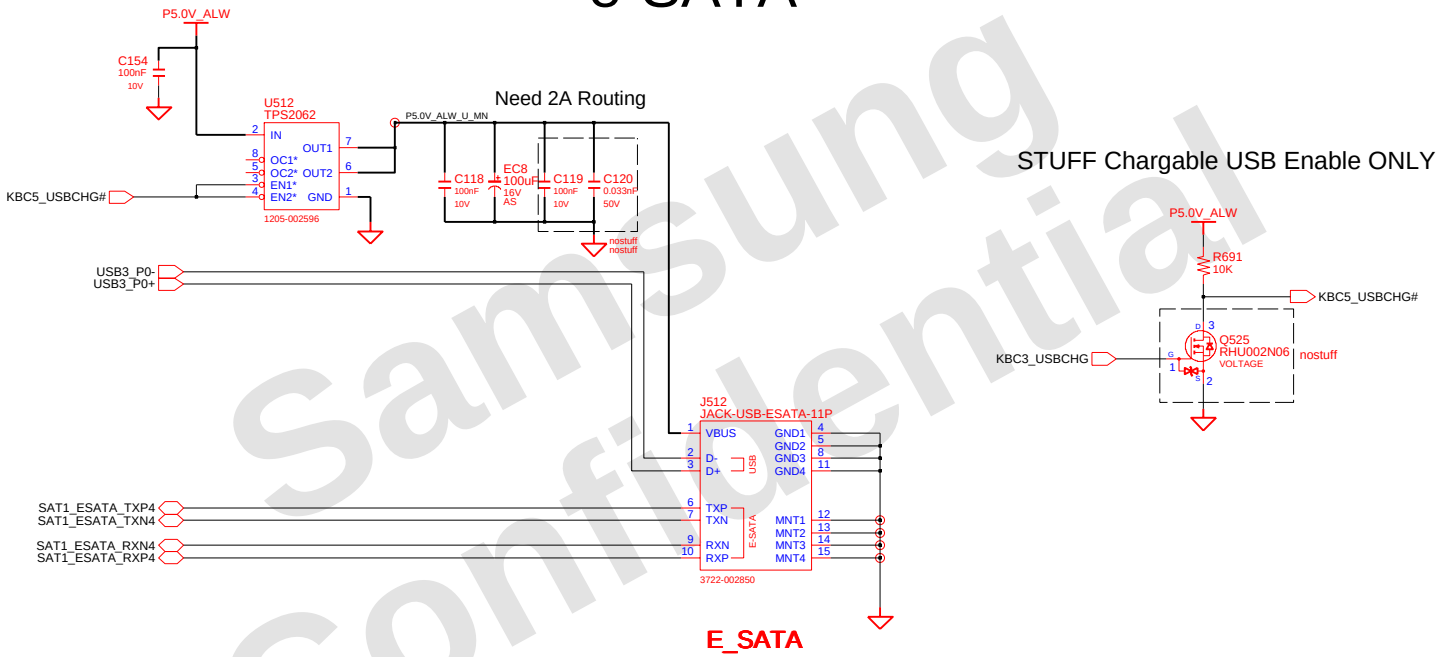
DESIGN: Xiaohong Zhang	DATE: 6/6/2008	TITLE: Suzhou_M MINI_PCIE_CONN	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE:	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 42 OF 62	

Express Card



DESIGN: Xiaohong Zhang	DATE: 7/7/2008	TITLE: Suzhou_M EXPRESS CARD	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE:	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 43 OF 62	

e-SATA

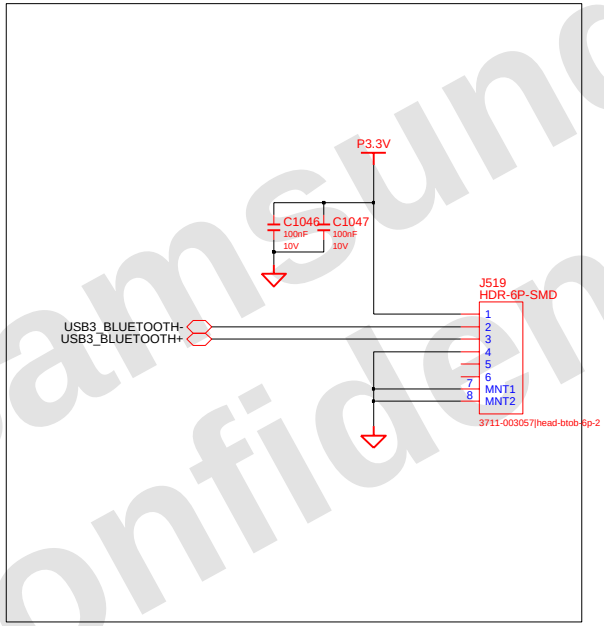


STUFF Chargable USB Enable ONLY

DRAW: Xiaohong Zhang	DATE: 11/8/2006	TITLE: Suzhou_M MINI CARD SILOH & EBRON	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE: undefined	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 44 OF 62	

USB I/F Devices

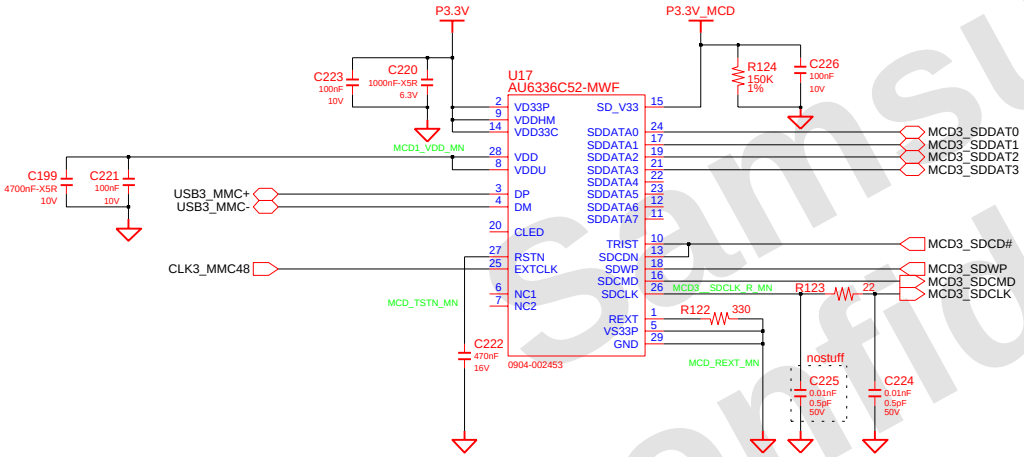
Bluetooth Interface



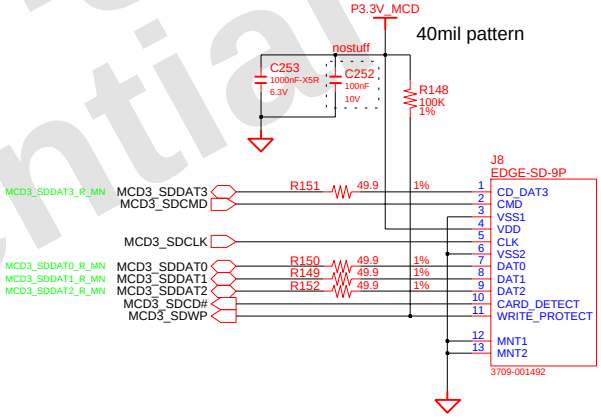
DESIGN: Xiaohong Zhang	DATE: 6/6/2008	TITLE: Suzhou_M USB_DEVICES	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE:	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 45 OF 62	

3 IN 1

P3.3V_MCD distance between R5U880 and socket should be less than 2 inches



40mil pattern



40 mil trace for medica card socket ground

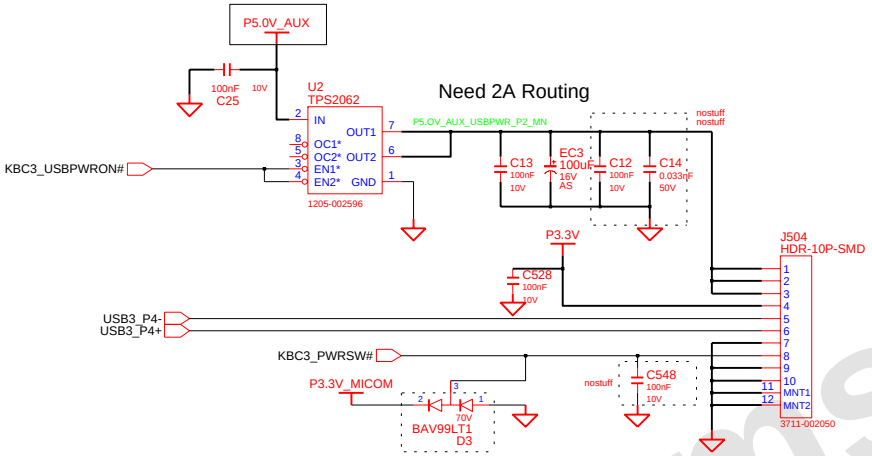
MSEL5	SD Write Protec Selection
Connected to VCC	High Enable
Connected to GND	Low Enable
MSEL7	PLL BASE CLOCK SELECTION
Connected to VCC	12MHz
Connected to GND	48MHz

DESIGN: Xiaohong Zhang	DATE: 10/15/2008	TITLE: Suzhou_M MMC AU6336	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 46 OF 62	

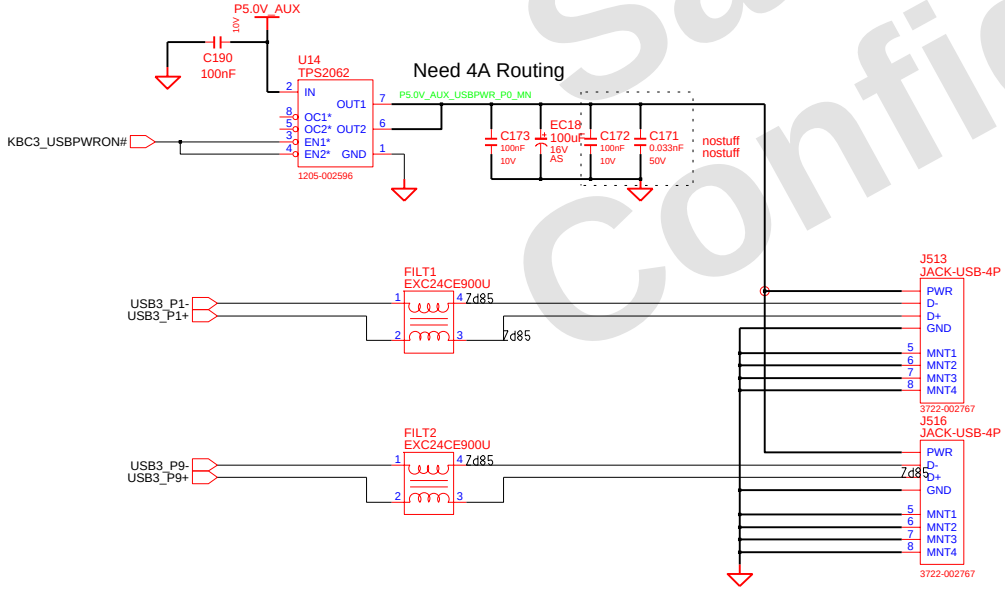
Main board

1 PORT USB CONNECTOR

Adopt P5.0V_ALW when enable chargable USB.

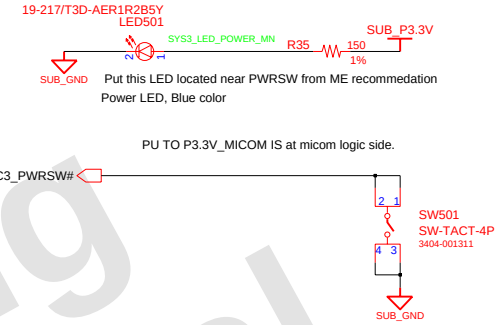


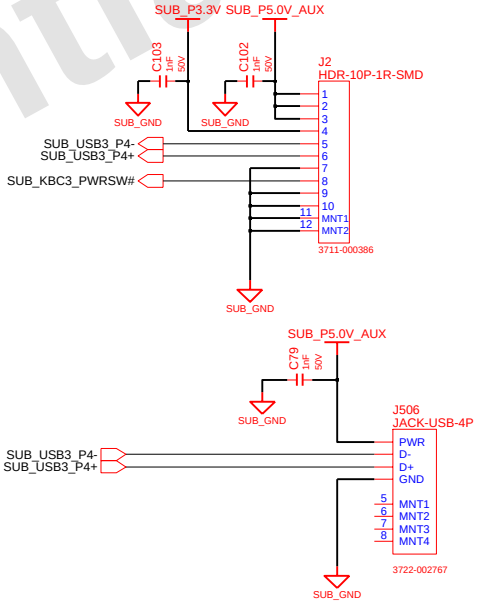
1*2 PORT USB CONNECTOR



Sub board

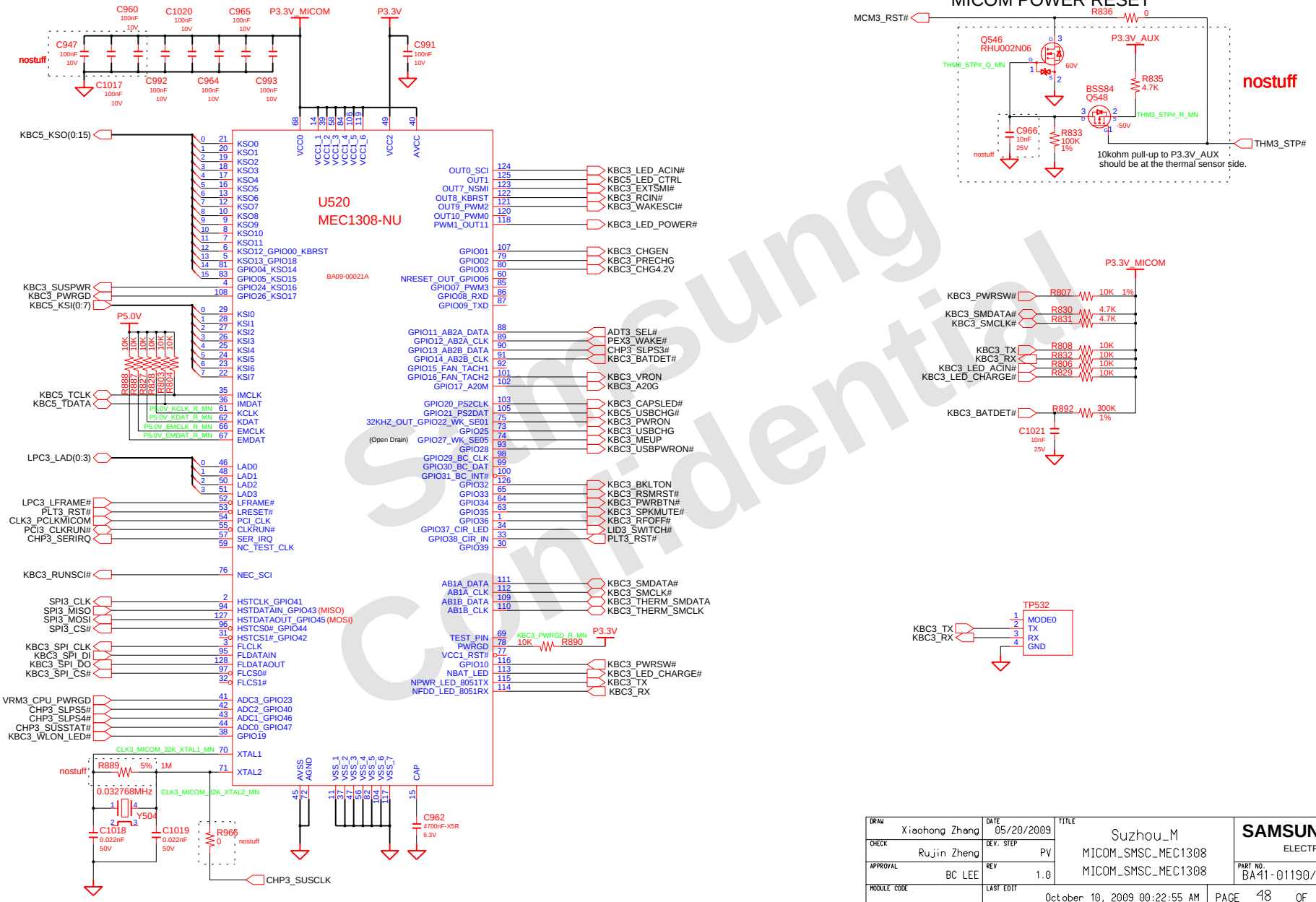
Power Switch Button





DESIGN: Xiaohong Zhang	DATE: 6/6/2008	TITLE: Suzhou_M USB_CONN	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 47 OF 62	

MAIN BOARD (MICOM)

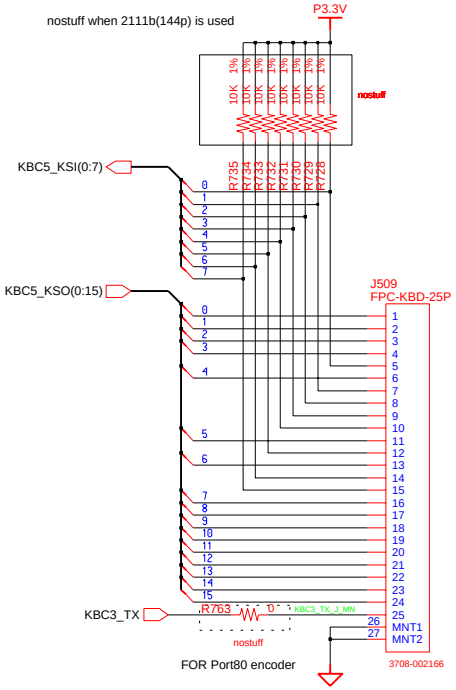


MICOM POWER RESET

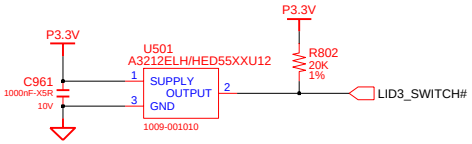
DRAW: Xiaohong Zhang	DATE: 05/20/2009	TITLE: Suzhou_M	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV	MICOM_SMSC_MEC1308	
APPROVAL: BC LEE	REV: 1.0	MICOM_SMSC_MEC1308	PART NO.: BA41-01190/1/2A
MODULE CODE	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 48 OF 62	

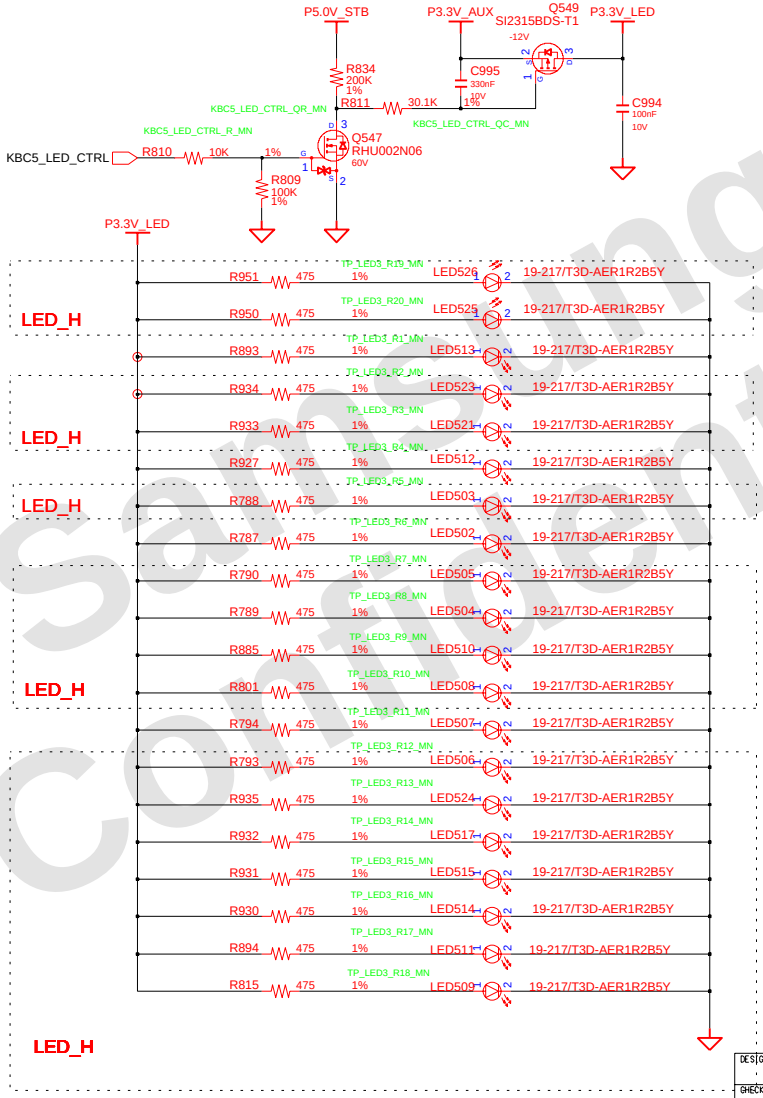
Micom Glue Logic

KEYBOARD

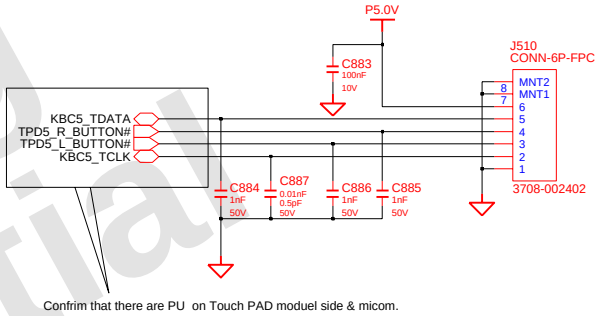


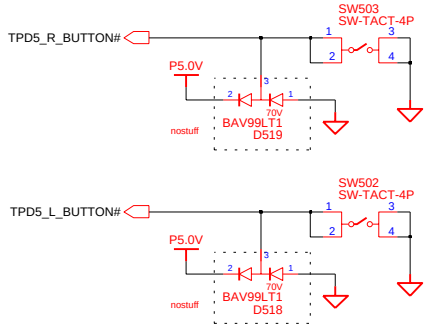
LID_SWITCH





TOUCHPAD





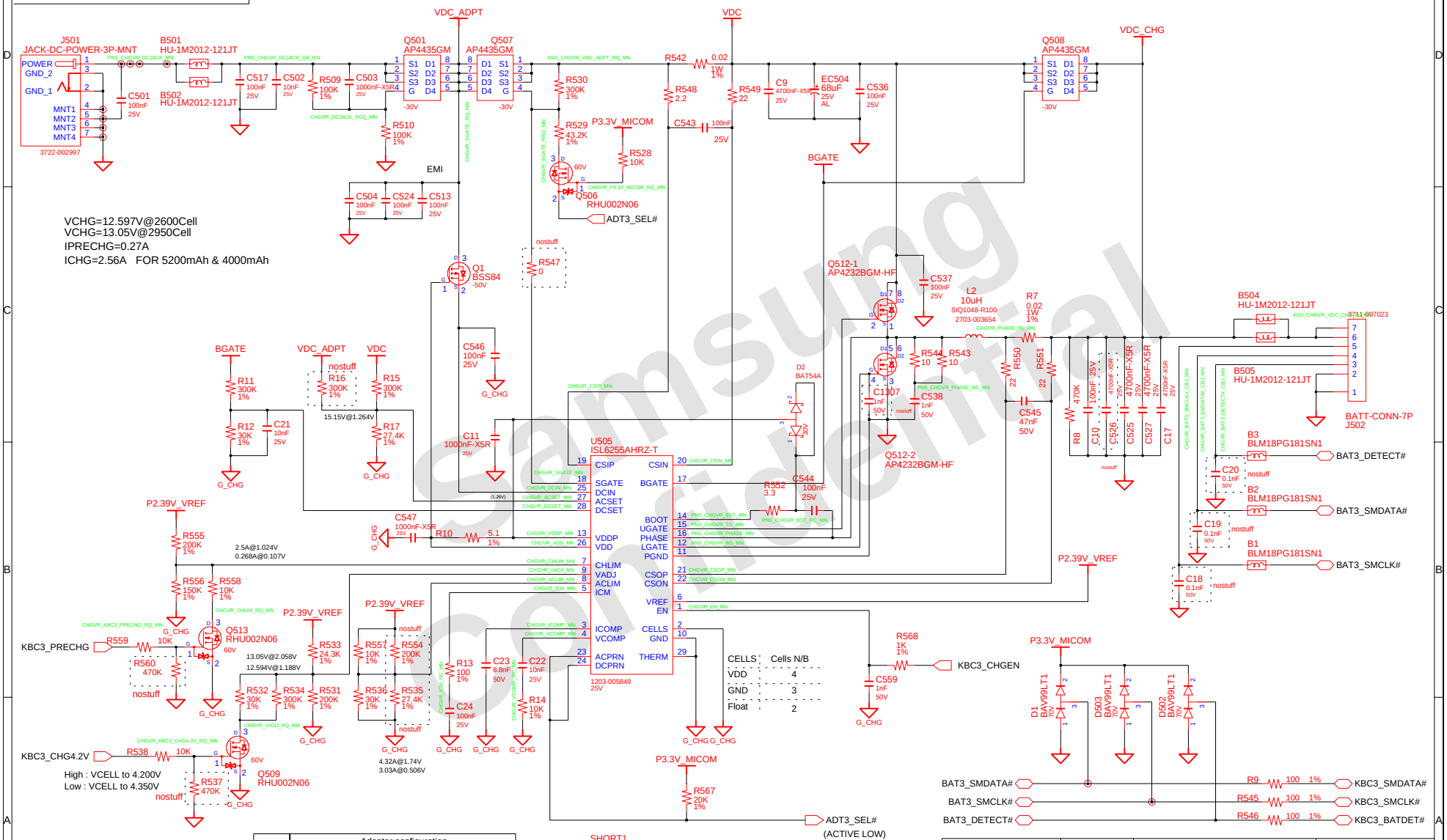
DESIGN: Xiaohong Zhang	DATE: 6/27/2008	TITLE: Suzhou_M	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 49 OF 62	

LED SWITCH LOGIC

Function Key LEDS

DRAW: Xiaohong Zhang	DATE: 8/12/2006	TITLE: Suzhou_M LED_Switch LED_Switch	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 50 OF 62	

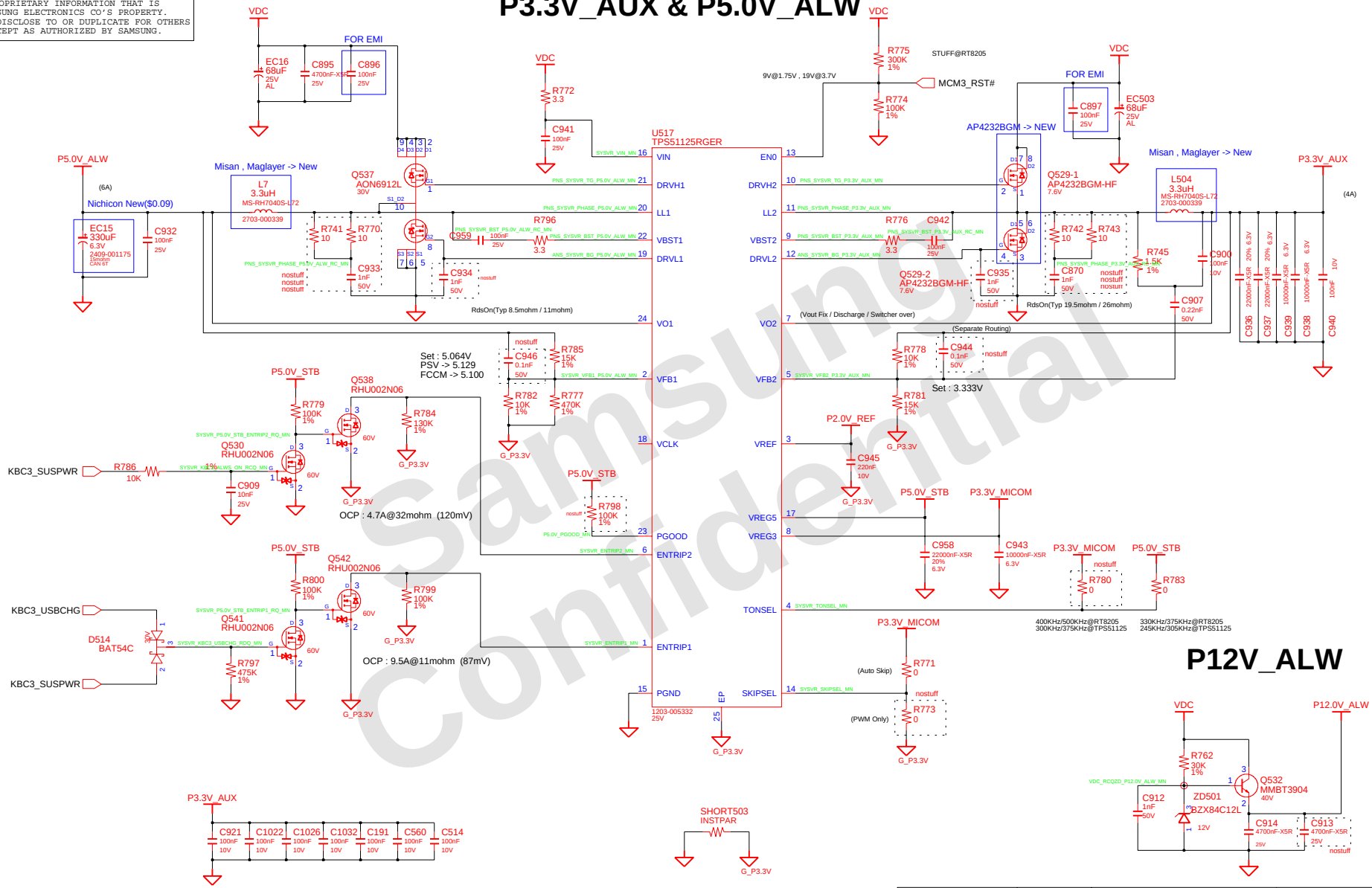
CHARGER & POWER MANAGEMENT



	Adapter configuration			
	60W / 3.03A / 96%		90W / 4.32A / 91.2%	
	Value	SEC Code	Value	SEC Code
Rtop	200K	2007-007334	10K	2007-007142
Rbot	27.4K	2007-007274	30K	2007-008275

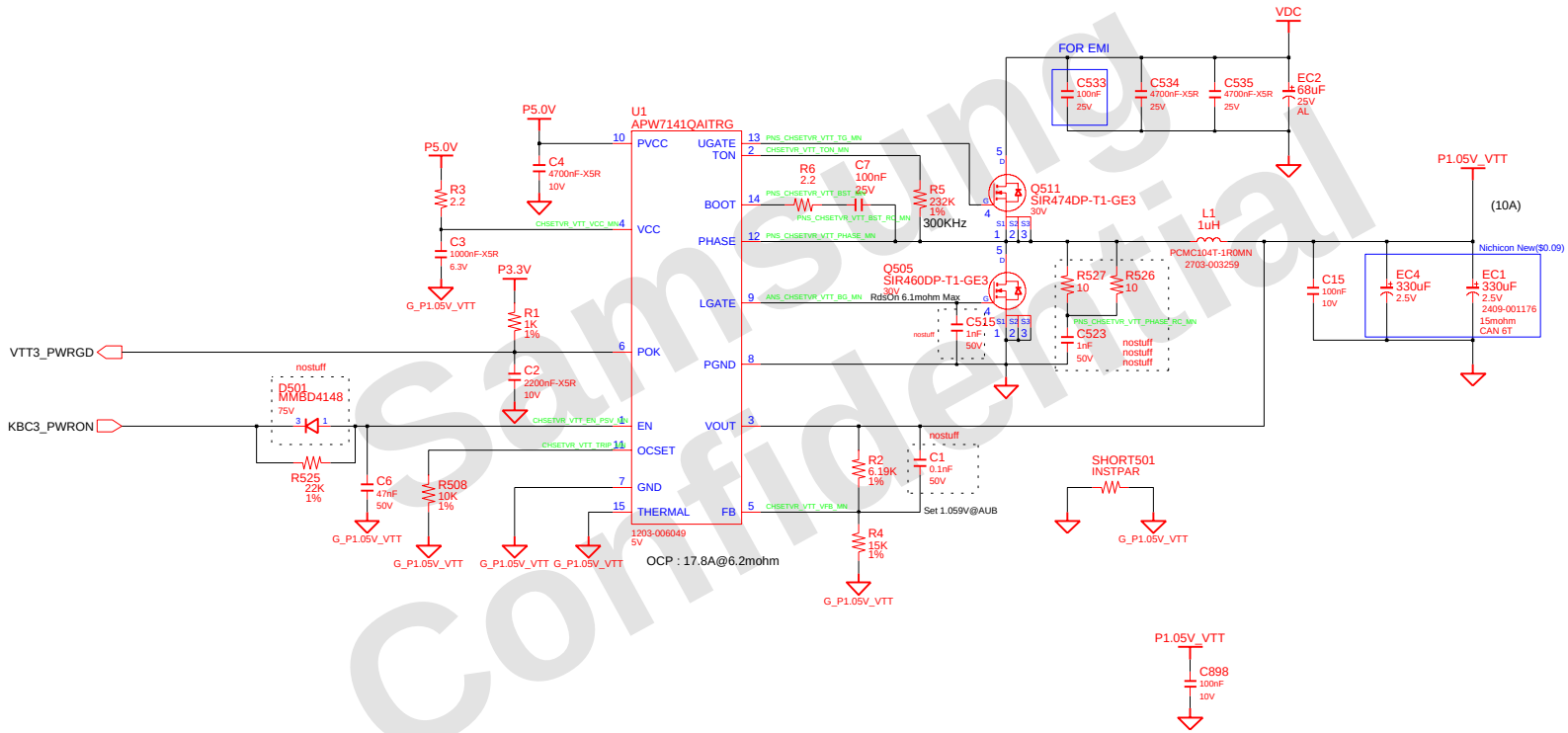
DRAW: Xiaohong Zhang	DATE: 03/11/2009	TITLE: Suzhou_M	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV	PWR_MV_Charger_Isl6256a	
APPROVAL: BC LEE	REV: 1.0	CHARGER (ISL6256A)	PART NO.: BA41-01190/1/2A
MODULE CODE: undefined	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 51 OF 62	

P3.3V_AUX & P5.0V_ALW



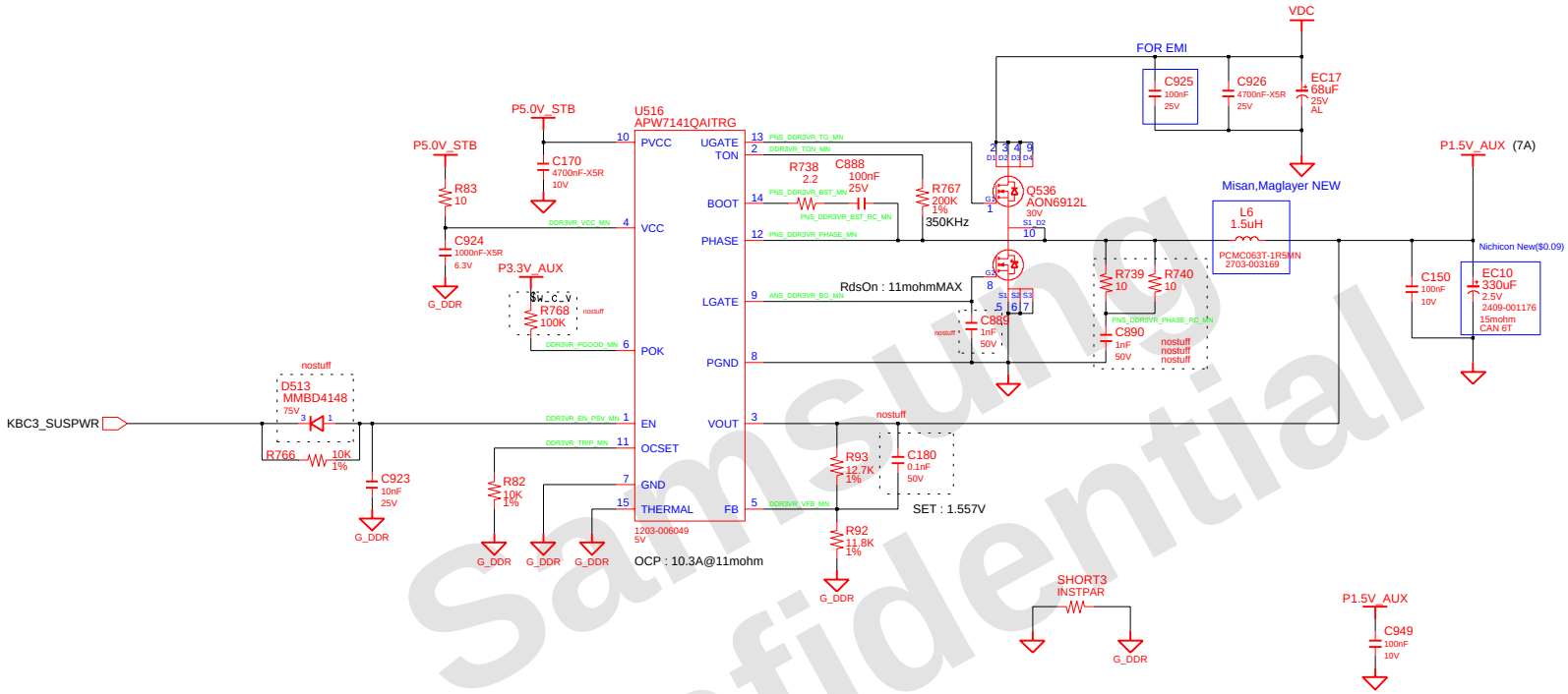
DRAW: Xiaohong Zhang	DATE: 04/01/2009	TITLE: Suzhou_M	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV	PWR_MV_3V_5V_Rt8205a	
APPROVAL: BC LEE	REV: 1.0	P3.3V_AUX / P5.0V_AUX	PART NO.: BA41-01190/1/2A
MODULE CODE: undefined	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 52 OF 62	

CHIPSET POWER(P1.05V_VTT & P1.05V)

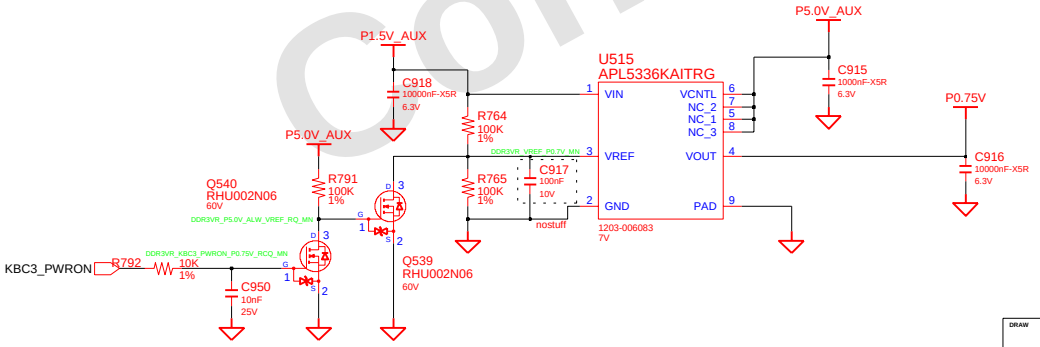


DRAW: Xiaohong Zhang	DATE: 03/11/2009	TITLE: Suzhou_M	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV	PWR_MV_Cantiga	
APPROVAL: BC LEE	REV: 1.0	Chipset Power (P1.05V_M,P1.2V)	PART NO.: BA41-01190/1/2A
MODULE CODE: undefined	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 53 OF 62	

DDR3 Power

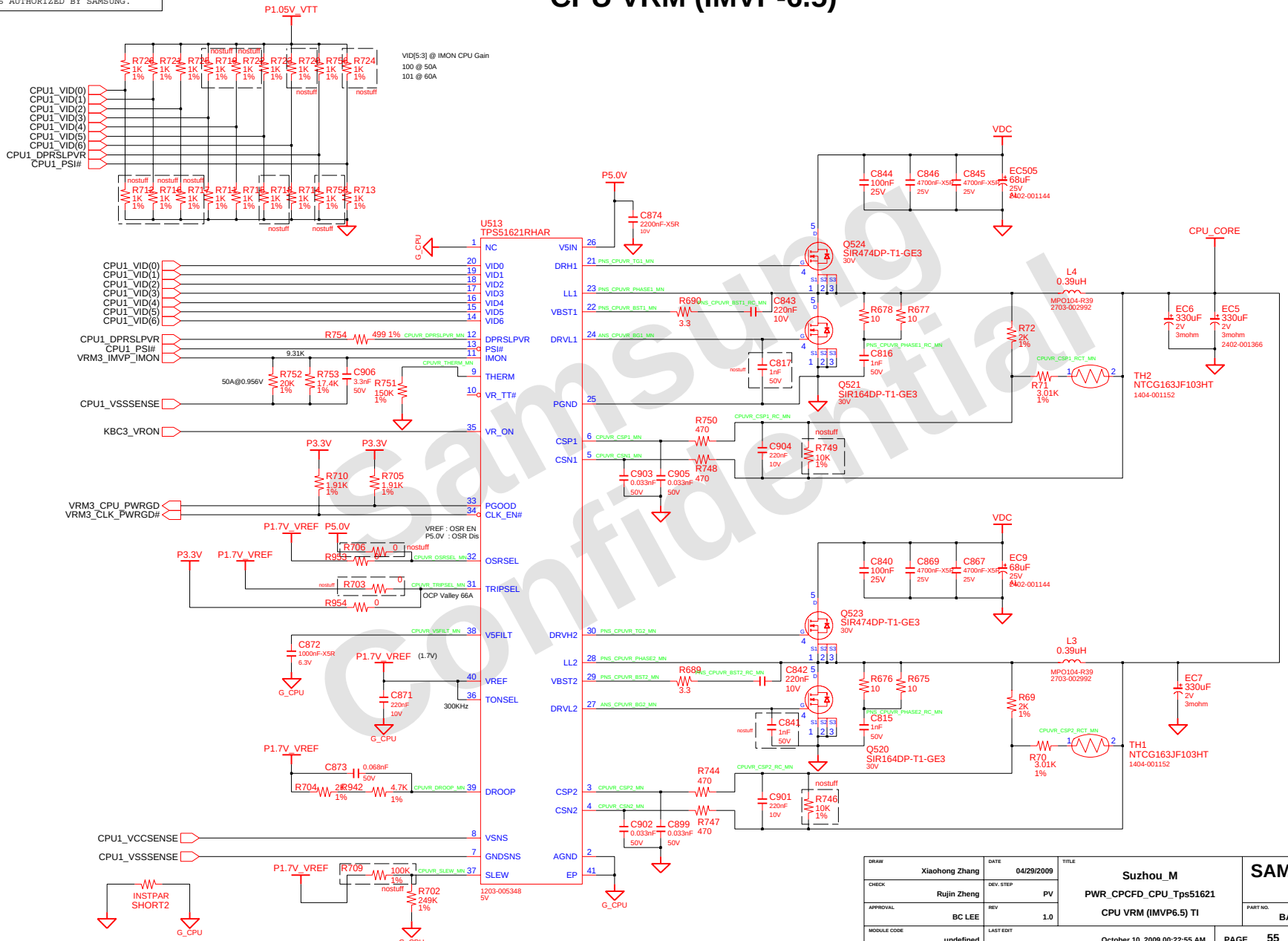


DDR3 VTT(0.75V)



DRAW: Xiaohong Zhang	DATE: 03/13/2009	TITLE: Suzhou_M	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV	PWR_MV_Memory_Rt8207	
APPROVAL: BC LEE	REV: 1.0	DDR3 POWER (P1.5V_AUX)	PART NO.: BA41-01190/1/2A
MODULE CODE: undefined	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 54 OF 62	

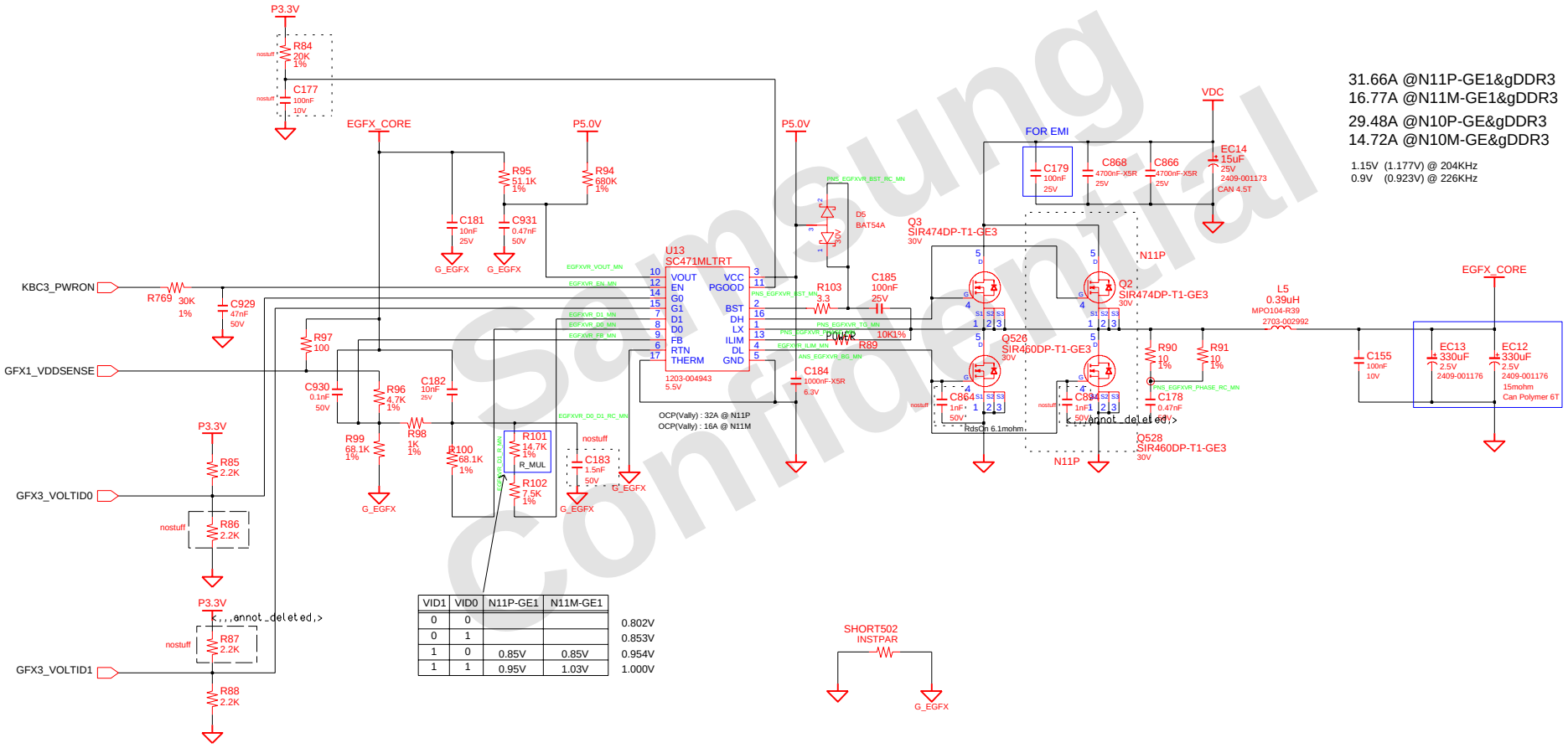
CPU VRM (IMVP-6.5)



DRAW: Xiaohong Zhang	DATE: 04/29/2009	TITLE: Suzhou_M PWR_CPCFD_CPU_Tps51621 CPU VRM (IMVP6.5) TI	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE: undefined	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 55 OF 62	

External Graphic Core Power

N11P-GE1@23.04W N10P-GE@20.97W
N11M-GE1@14.21W N10M-GE@13.36W

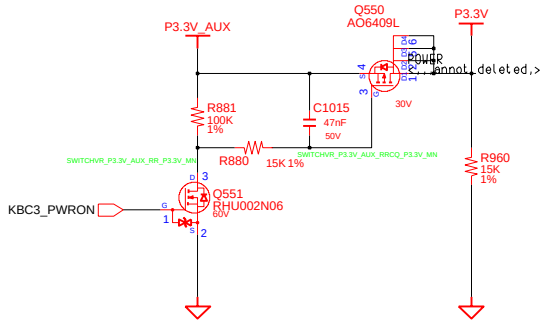


VID1	VID0	N11P-GE1	N11M-GE1	
0	0			0.802V
0	1			0.853V
1	0	0.85V	0.85V	0.954V
1	1	0.95V	1.03V	1.000V

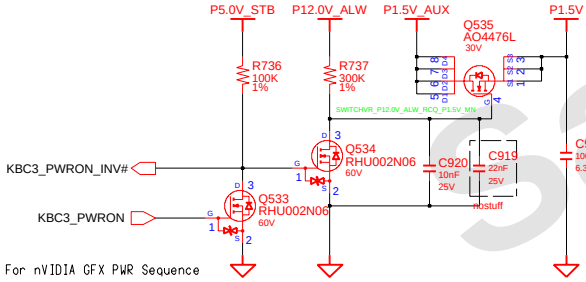
DRAW: Xiaohong Zhang	DATE: 03/11/2009	TITLE: Suzhou_M	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV	PWR_Gfx_MV_Ext	
APPROVAL: BC LEE	REV: 1.0	Ext Gfx Memory(TPS51117)	PART NO.: BA41-01190/1/2A
MODULE CODE	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 56 OF 62	

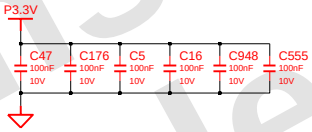
Switched Power

Switched Power On (P3.3V)

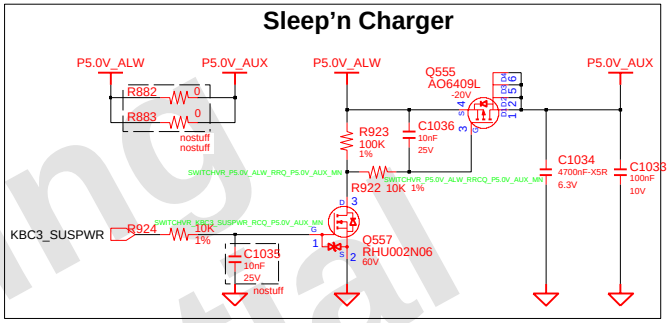


Switched Power On (P1.5V)

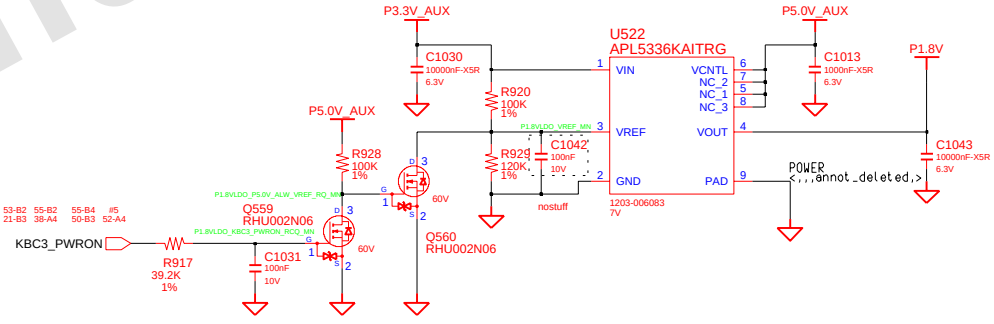




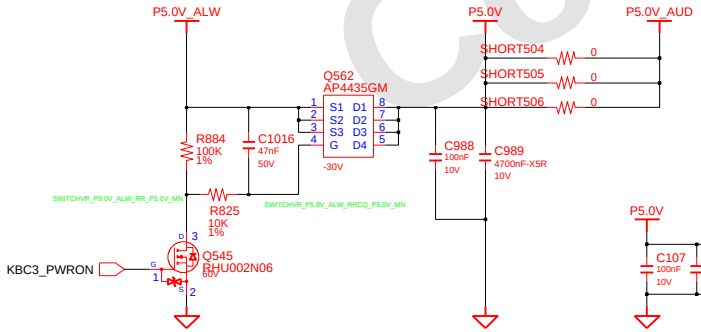
Sleep'n Charger

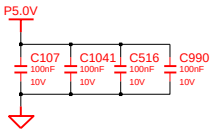


P1.8V(LDO)



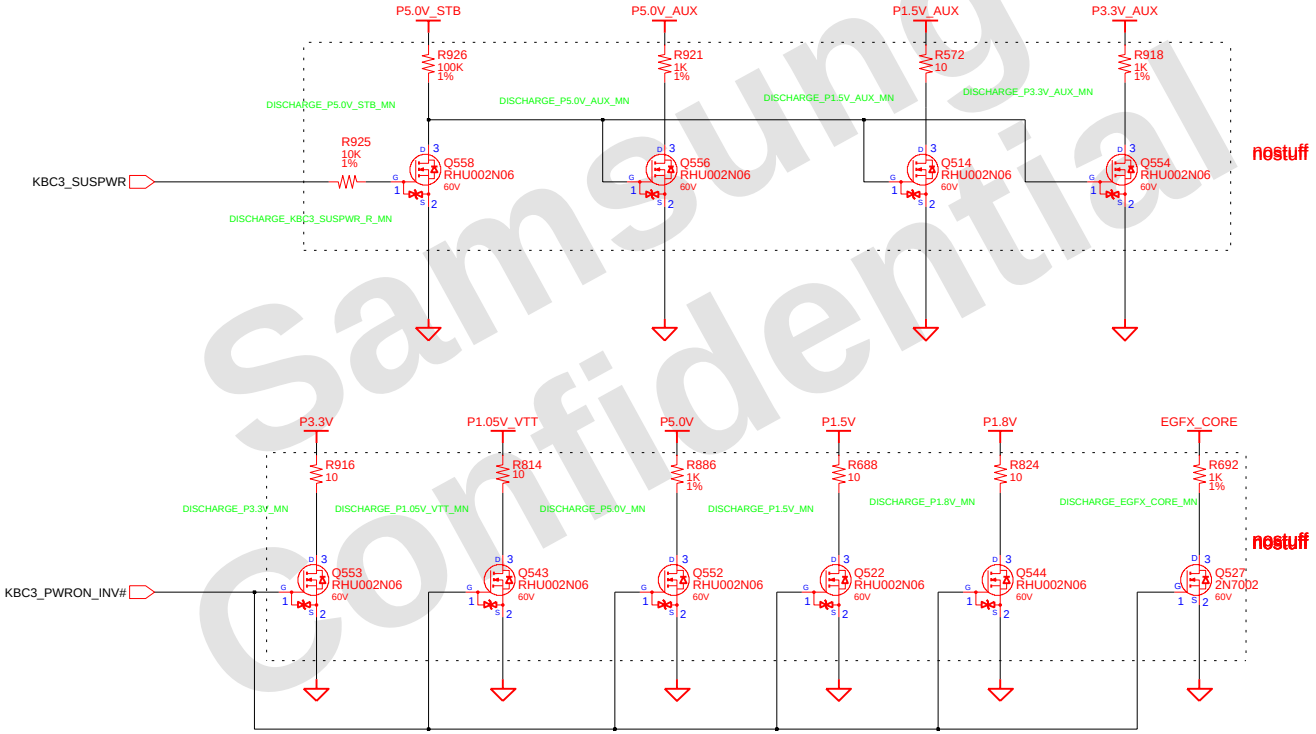
Switched Power On (P5.0V)





DRAW: Xiaohong Zhang	DATE: 03/11/2009	TITLE: Suzhou_M PWR_MV_Switched SWITCHED POWER	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01190/1/2A
MODULE CODE:	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 57 OF 62	

POWER DISCHARGER



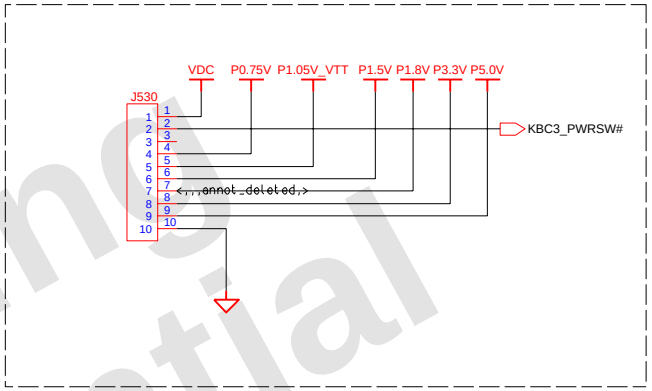
MT502 RMNT-38-70-1P
MT503 RMNT-38-70-1P
MT506 RMNT-38-70-1P
MT507 RMNT-38-70-1P

CPU BRKT MNT

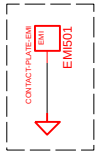
MT501 RMNT-30-76-1P
MT505 RMNT-30-76-1P
MT511 RMNT-30-76-1P
MT512 RMNT-30-76-1P
MT513 RMNT-30-76-1P
MT510 RMNT-30-76-1P
MT504 RMNT-30-76-1P

PCB TOP BOTTOM

ICT PORT



M501 HEAD DIA LENGTH BA61-00932A
M502 HEAD DIA LENGTH BA61-00932A
M504 HEAD DIA LENGTH BA61-00932A
M503 HEAD DIA LENGTH BA61-00932A



MDC

MT508 RMNT-30-76-1P

DRAW: Xiaohong Zhang	DATE: 03/11/2009	TITLE: Suzhou_M	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV	PWR_MV_DisCharger	
APPROVAL: BC LEE	REV: 1.0	DISCHARGING LOGIC	PART NO.: BA41-01190/1/2A
MODULE CODE: undefined	LAST EDIT: October 10, 2009 00:22:55 AM	PAGE 59 OF 62	

GPIO38
AUD3_PD#

FAN5_VDD

SMB3_CLK
SPI3_CLK
SPI3_CS#
ADT3_SEL#
AUD3_SPKR
CHP3_PECI
CPU1_PSI#

KBC3_A20G
KBC3_VRON
KBC5_TCLK
LCD3_BRIT
MCD3_SDWP
MCM3_RST#
PLT3_RST#
SMB3_DATA
SPI3_MISO
SPI3_MOSI

CLK3_CHP14
CLK3_MMC48
CRT3_GREEN
CRT3_HSYNC
CRT3_VSYNC
KBC3_CHGEN
KBC3_PWRGD
KBC3_PWRON
KBC3_RCIN#
KBC5_TDATA
MCD3_SDCD#
MCD3_SDCLK
MCD3_SDCMD
PEX3_WAKE#
VTT3_PWRGD
AUD5_CBN_MN
AUD5_CBP_MN
CHP3_PMSYNC

CHP3_SERIRQ
CHP3_SLPS3#
CHP3_SLPS4#
CHP3_SLPS5#
CLK3_DBGLPC
CLK3_PCI_FB
CPU1_VID(0)
CPU1_VID(1)
CPU1_VID(2)
CPU1_VID(3)
CPU1_VID(4)
CPU1_VID(5)
CPU1_VID(6)
CRT3_DDCCLK
GFX3_ROM_SI
GFX3_ROM_SO

GFX3_STRAP2

KBC3_BKLTON
KBC3_PWRSW#
KBC3_RFOFF#
KBC3_SMCLK#
KBC3_SPI_DI
KBC3_SPI_DO
KBC3_SUSPWR
KBC3_USBCHG
KBC5_KSI(0)
KBC5_KSI(1)
KBC5_KSI(2)
KBC5_KSI(3)
KBC5_KSI(4)
KBC5_KSI(5)
KBC5_KSI(6)
KBC5_KSI(7)
KBC5_KSO(0)
KBC5_KSO(1)

KBC5_KSO(2)
KBC5_KSO(3)
KBC5_KSO(4)
KBC5_KSO(5)
KBC5_KSO(6)
KBC5_KSO(7)
KBC5_KSO(8)
KBC5_KSO(9)

LAN_RSET_MN
LCD3_BKLTON
LPC3_LAD(0)
LPC3_LAD(1)
LPC3_LAD(2)
LPC3_LAD(3)
MCD3_SDDAT0
MCD3_SDDAT1
MCD3_SDDAT2
MCD3_SDDAT3
PEG3_BKLTEN

SMB3_ALERT#
SPI0_WP#_MN
BAT3_DETECT#
CHP3_BATLOW#

CHP3_RTCRST#
CHP3_VREF_MN
CPU_TCK_R_MN
CRT3_DDCDATA

EGFXVR_EN_MN
EGFXVR_FB_MN
EXP3_CLKREQ#
FAN3_FDBACK#
GFX3_THERMDN
GFX3_THERMDP
GFX3_VOLTID0
GFX3_VOLTID1
HDA3_AUD_SDO
HDA3_BCLK_MN
HDA3_MDC_SDO

KBC3_BATDET#
KBC3_CHG4.2V
KBC3_EXTSM#
KBC3_PWRBTN#
KBC3_RSMRST#
KBC3_RUNSCI#
KBC3_SMDATA#
KBC3_SPI_CLK
KBC3_SPI_CS#

KBC3_TX_J_MN
KBC5_KSO(10)
KBC5_KSO(11)
KBC5_KSO(12)
KBC5_KSO(13)
KBC5_KSO(14)
KBC5_KSO(15)
KBC5_USBCHG#
LAN3_CLKREQ#

LID3_SWITCH#
LPC3_LFRAME#
MEM3_CHB_SA0
MEM3_CHB_SA1
MIN3_CLKREQ#
PCH_GPIO0_MN
PCI3_CLKRUN#

AUD5_CPVEE_MN
AUD5_SENS_HP#

CHP3_SATALED#
CHP3_SUSSTAT#

CPU0_COMP0_MN
CPU0_COMP1_MN
CPU0_COMP2_MN
CPU0_COMP3_MN
CPU1_DPRSLPVR
CPU1_VCCSENSE
CPU1_VSSSENSE
CPUVR_CSN1_MN
CPUVR_CSN2_MN
CPUVR_CSP1_MN
CPUVR_CSP2_MN

DDR3VR_TON_MN

GFX1_VDDSENSE
GFX3_ROM_SCLK
HDA3_AUD_BCLK
HDA3_AUD_RST#
HDA3_AUD_SDI0
HDA3_AUD_SYNC
HDA3_MDC_BCLK
HDA3_MDC_RST#
HDA3_MDC_SDI1
HDA3_MDC_SYNC
KBC3_CAPSLED#
KBC3_SPKMUTE#
KBC3_WAKESCI#
KBC5_LED_CTRL

LCD3_EDID_CLK
MCP1_DRAMRST#
PCH_GPIO36_MN

PCH_GPIO48_MN

PCI3_IRDY#_MN
PCI3_PERR#_MN

PCI3_REQ1#_MN
PCI3_REQ2#_MN

PEG0_ZQ_R1_MN
PEG0_ZQ_R2_MN
PEG0_ZQ_R3_MN
PEG0_ZQ_R4_MN
PEG0_ZQ_R5_MN

PEG0_ZQ_R7_MN

VGA5_HDMI_HPD
AUD0_CPVREF_MN
AUD5_HP_O_LEFT
AUD5_MIC2_VREF
AUD5_SENS_A_MN
AUD5_SENS_MIC#
CHP3_CPU_PWRGD
CHP3_GPIO39_MN
CHP3_INTRUDER#
CLK3_PCLKMICOM
CLOCK_P1.5V_MN
CLOCK_P3.3V_MN
CPU1_THRMTRIP#

PEG3_HDMI_CLK
PEG3_HPD_HDMI
PEG3_LCDVDDON
PEG3_SPDIF_MN
PEG3_VDD33_MN
PEG5_HDMI_CLK
PLT3_RST_ORG#

SPI3_HOLD#_MN
TP_LED3_R1_MN
TP_LED3_R2_MN
TP_LED3_R3_MN
TP_LED3_R4_MN
TP_LED3_R5_MN
TP_LED3_R6_MN
TP_LED3_R7_MN
TP_LED3_R8_MN
TP_LED3_R9_MN
CPUVR_DROOP_MN
CPUVR_THERM_MN
CPU_CFG_7_R_MN
DDR3VR_TRIP_MN

EGFXVR_D1_R_MN
EGFXVR_ILIM_MN
EGFXVR_VOUT_MN
KBC3_LED_ACIN#
KBC3_USBPWRON#
KBC3_WLON_LED#
LCD3_EDID_DATA

PCI3_FRAME#_MN
PCI3_PIRQA#_MN
PCI3_PIRQB#_MN
PCI3_PIRQC#_MN
PCI3_PIRQD#_MN

PEG1_PLLVDD_MN
PEG3_HDMI_DATA
PEG5_HDMI_DATA

THM3_STP#_Q_MN
THM3_STP#_R_MN
TPD5_L_BUTTON#
TPD5_R_BUTTON#
TP_LED3_R10_MN
TP_LED3_R11_MN
TP_LED3_R12_MN
TP_LED3_R13_MN
TP_LED3_R14_MN
TP_LED3_R15_MN
TP_LED3_R16_MN
TP_LED3_R17_MN
TP_LED3_R18_MN
VRM3_CPU_PWRGD
VRM3_IMVP_IMON
ANS_CHGVR_BG_MN
AUD5_HP_O_RIGHT
AUD5_JDREF_R_MN
CHP1_DRAM_PWRGD
CHP3_ME_RTCRST#
CHP3_SUSPWR_ACK

CHP3_WP#_0_R_MN

CPUVR_V5FILT_MN
DDR3VR_PGOOD_MN

KBC3_LED_POWER#
KBC3_PWRGD_R_MN
KBC3_PWRON_INV#
MDC48_TIP_B1_MN
MDC48_TIP_B2_MN
MEM3_CHA_SA0_MN
MEM3_CHA_SA1_MN

PCH_PCIECLKRQ2#

PNS_CHGVR_TG_MN
SUB_KBC3_PWRSW#
SYSVR_TONSEL_MN

THM3_DN2_DN3_MN
THM3_DP2_DN3_MN
VRM3_CLK_PWRGD#
VTT3_PWRGD_R_MN
ANS_CPUVR_BG1_MN
ANS_CPUVR_BG2_MN
ANS_DDR3VR_BG_MN
ANS_EGFXVR_BG_MN

CHP3_VREF_SUS_MN
CLOCK_CPU_SEL_MN
CLOCK_XTAL_IN_MN

CPUVR_CSP1_RC_MN
CPUVR_CSP2_RC_MN
CPUVR_TRIPSEL_MN
DDR3VR_EN_PSV_MN

HDD3_LED#_LED_MN
KBC3_LED_CHARGE#
KBC3_THERM_SMCLK

MDC48_RING_B1_MN
MDC48_RING_B2_MN

PEG0_BUFRST_N_MN
PEG3_DACA_VDD_MN

PEG3_TESTMODE_MN
PEG3_XTAL_OUT_MN

PLT1_RST#_MCP_MN
PNS_CPUVR_TG1_MN
PNS_CPUVR_TG2_MN
PNS_DDR3VR_TG_MN
PNS_EGFXVR_TG_MN

SYSVR_ENTRIP1_MN
SYSVR_ENTRIP2_MN
SYSVR_SKIPSEL_MN
THM3_SHDN_SEL_MN
THM3_TRIP_SET_MN

AUD5_HP_LEFT_B_MN
AUD5_HP_LEFT_R_MN

CLK3_MMC48_PCH_MN
CLOCK_CPU_STOP#_MN
CLOCK_XTAL_OUT_MN

LAN3_CLKREQ#_R_MN
MCH1_SM_RCOMP0_MN
MCH1_SM_RCOMP1_MN
MCH1_SM_RCOMP2_MN
MCP3_PEG_RBIAS_MN

PEG1_FBA_DEBUG_MN
PEG1_FBC_DEBUG_MN
PEG1_IFPEF_PLLVDD
PEG1_PB_LLAVDD_MN
PEG1_SP_PLLVDD_MN

PNS_CPUVR_BST1_MN

PNS_DDR3VR_BST_MN
PNS_EGFXVR_BST_MN
PRTC_BAT_CON_R_MN
SYS3_LED_POWER_MN
80H_CHP3_SERIRQ_MN
AUD5_HP_RIGHT_B_MN

AUD5_MIC2_INT_B_MN
AUD5_MIC2_INT_J_MN
CHGVR_SGATE_RRQ_MN
CHP1_DRAM_PWRGF_MN

CHP3_PEG_HOLD_RST#
CHP3_XTAL_IN_25_MN

CHSETVR_VTT_TON_MN
CHSETVR_VTT_VCC_MN
CHSETVR_VTT_VFB_MN
CLK3_DBFLPC_PCH_MN
CLK3_PCI_FB_PCH_MN
EGFXVR_D0_D1_RC_MN

HDA3_MDC_SDI1_R_MN
KBC5_LED_CTRL_R_MN
LAN3_DISABLE#_R_MN
P1.5V_VREFCA_R1_MN
P1.5V_VREFCA_R2_MN
P1.5V_VREFCA_R3_MN
P1.5V_VREFCA_R4_MN
P1.5V_VREFCA_R5_MN
P1.5V_VREFCA_R6_MN
P1.5V_VREFCA_R7_MN
P1.5V_VREFCA_R8_MN
P1.5V_VREFDQ_R1_MN
P1.5V_VREFDQ_R2_MN
P1.5V_VREFDQ_R3_MN
P1.5V_VREFDQ_R4_MN
P1.5V_VREFDQ_R5_MN
P1.5V_VREFDQ_R6_MN

P1.5V_VREFDQ_R8_MN

PEG5_HDMI_CLK_B_MN

PEG_IFPC_PLLVDD_MN
VGA5_HDMI_HPD_R_MN
AUD5_MIC1_LEFT_C_MN
AUD5_MIC1_LEFT_J_MN
AUD5_MIC1_LEFT_R_MN
AUD5_MIC2_LEFT_C_MN
CHP3_XTAL_OUT_25_MN

CHSETVR_VTT_TRIP_MN

KBC5_LED_CTRL_QC_MN
KBC5_LED_CTRL_QR_MN

PEG1_IFPAB_IOVDD_MN
PEG1_IFPEF_IOVDD_MN
PEG3_JTAG_TRST_N_MN

- PNS_CPUVR_PHASE1_MN
- PNS_CPUVR_PHASE2_MN
- PNS_DDR3VR_PHASE_MN
- PNS_EGFXVR_PHASE_MN
- VRM3_CLK_PWRGD#_INV
- AUD5_MIC1_RIGHT_C_MN
- AUD5_MIC1_RIGHT_J_MN
- AUD5_MIC1_RIGHT_R_MN
- AUD5_MIC1_VREFO_L_MN
- AUD5_MIC2_RIGHT_C_MN
- CHP1_SATAICOMPOIO_MN

- DDR3VR_VREF_P0.7V_MN
- KBC3_CAPSLED#_LED_MN
- MCP3_FDI_SIDEBAND_MN

- PEG3_PEX_SVDD_SVS_MN
- PEG3_TX_HDMI_PD_Q_MN
- PEG3_XTAL_OUTBUFF_MN
- PNS_CPUVR_BST1_RC_MN

- PNS_DDR3VR_BST_RC_MN
- PNS_EGFXVR_BST_RC_MN
- ANS_CHSETVR_VTT_BG_MN
- CHSETVR_VTT_EN_PSV_MN

- CPU1_THRMTRIP#_PCH_MN

- KBC3_WLON_LED#_LED_MN
- MCP3_PEG_IR_COMPIO_MN
- PCH_DMI_P1.05V_VTT_MN

- PEG3_LCD3_EDID_CLK_MN

- PEX1_EXPCRD_TXN3_C_MN
- PEX1_EXPCRD_TXP3_C_MN
- PNS_CHSETVR_VTT_TG_MN
- P5.0V_AUX_USBPWR_P2_MN

- PEG3_LCD3_EDID_DATA_MN
- PNS_CHSETVR_VTT_BST_MN
- PNS_CPUVR_PHASE1_RC_MN
- PNS_CPUVR_PHASE2_RC_MN
- PNS_DDR3VR_PHASE_RC_MN
- CLK3_MICOM_32K_XTAL1_MN
- CLK3_MICOM_32K_XTAL2_MN

- SYSVR_VFB1_P5.0V_ALW_MN
- SYSVR_VFB2_P3.3V_AUX_MN

- PNS_CHSETVR_VTT_PHASE_MN
- SYSVR_KBC3_USBCHG_RDQ_MN

- SYSVR_VOUT2_P3.3V_AUX_MN
- ANS_SYSVR_BG_P3.3V_AUX_MN
- ANS_SYSVR_BG_P5.0V_ALW_MN

- PNS_CHSETVR_VTT_BST_RC_MN
- PNS_SYSVR_TG_P3.3V_AUX_MN
- PNS_SYSVR_TG_P5.0V_ALW_MN
- SYSVR_KBC3_ALWS_ON_RCQ_MN
- P1.8VLDO_KBC3_PWRON_RCQ_MN
- PNS_SYSVR_BST_P3.3V_AUX_MN
- PNS_SYSVR_BST_P5.0V_ALW_MN

- DDR3VR_P5.0V_ALW_VREF_RQ_MN
- PNS_CHSETVR_VTT_PHASE_RC_MN

- PNS_SYSVR_PHASE_P3.3V_AUX_MN
- PNS_SYSVR_PHASE_P5.0V_ALW_MN
- P1.8VLDO_P5.0V_ALW_VREF_RQ_MN
- PNS_SYSVR_BST_P3.3V_AUX_RC_MN
- PNS_SYSVR_BST_P5.0V_ALW_RC_MN
- SYSVR_P5.0V_STB_ENTRIP1_RQ_MN
- SYSVR_P5.0V_STB_ENTRIP2_RQ_MN
- SWITCHVR_P5.0V_ALW_RR_P5.0V_MN
- DDR3VR_KBC3_PWRON_P0.75V_RCQ_MN
- PNS_SYSVR_PHASE_P3.3V_AUX_RC_MN
- PNS_SYSVR_PHASE_P5.0V_ALW_RC_MN
- SWITCHVR_P3.3V_AUX_RRCQ_P3.3V_MN
- SWITCHVR_P5.0V_ALW_RRQ_P5.0V_AUX_MN

- SWITCHVR_KBC3_SUSPWR_RCQ_P5.0V_AUX_MN

- BGATE
- CPU_CORE
- CPU_CORE
- CPU_CORE
- EGFX_CORE
- EGFX_CORE
- EGFX_CORE
- G_AUD
- G_AUD
- G_CHG
- G_CHG
- G_CPU

- G_DDR
- G_DDR
- G_EGFX
- G_EGFX
- G_P3.3V
- G_P3.3V
- G_P1.05V_VTT
- G_P1.05V_VTT
- LCD_VDD3V
- LCD_VDD3V
- MDC_GND
- MDC_GND
- P1.5V
- P1.5V
- P1.5V
- P1.8V
- P1.8V
- P1.8V
- P3.3V
- P3.3V
- P3.3V
- P3.3V
- P5.0V
- P5.0V
- P5.0V
- P0.75V
- P0.75V
- P1.0V_LAN
- P1.0V_LAN
- P1.5V_AUX
- P1.5V_AUX

- P1.8V_LAN
- P2.0V_REF

- P5.0V_ALW
- P5.0V_ALW
- P5.0V_AUD
- P5.0V_AUD
- P5.0V_AUX
- P5.0V_AUX
- P5.0V_STB
- P5.0V_STB
- P1.05V_VTT
- P1.05V_VTT
- P1.05V_VTT
- P1.05V_VTT

- P12.0V_ALW
- P12.0V_ALW
- P4.75V_AUD
- P4.75V_AUD
- P2.39V_VREF

- P3.3V_MICOM
- P3.3V_MICOM
- SUB_GND
- SUB_GND
- SUB_P3.3V
- SUB_P3.3V
- SUB_P5.0V_AUX
- SUB_P5.0V_AUX
- VDC
- VDC
- VDC
- VDC
- VCC_CRT
- VCC_CRT
- VDC_LED
- VDC_LED
- VDC_ADPT
- VDC_ADPT