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BRIGHTON

CPU : VIA ISAIAH
Chip Set : VIA VX800
Remarks :

Model Name : BRIGHTON MAIN

PCB Part No :

Dev. Step : PV

Revision : 1.0

T.R. Date : 2008.11.07

DRAW	CHECK	APPROVAL

Table of Contents

Page. 1 ---- COVER
Page. 2 ---- OPERATION BLOCK DIAGRAM
Page. 3 ---- POWER DIAGRAM
Page. 4 ---- TIMING DIAGRAM (POWER ON)
Page. 5 ---- CLOCK DISTRIBUTION
Page. 6 ---- BOARD INFORMATION

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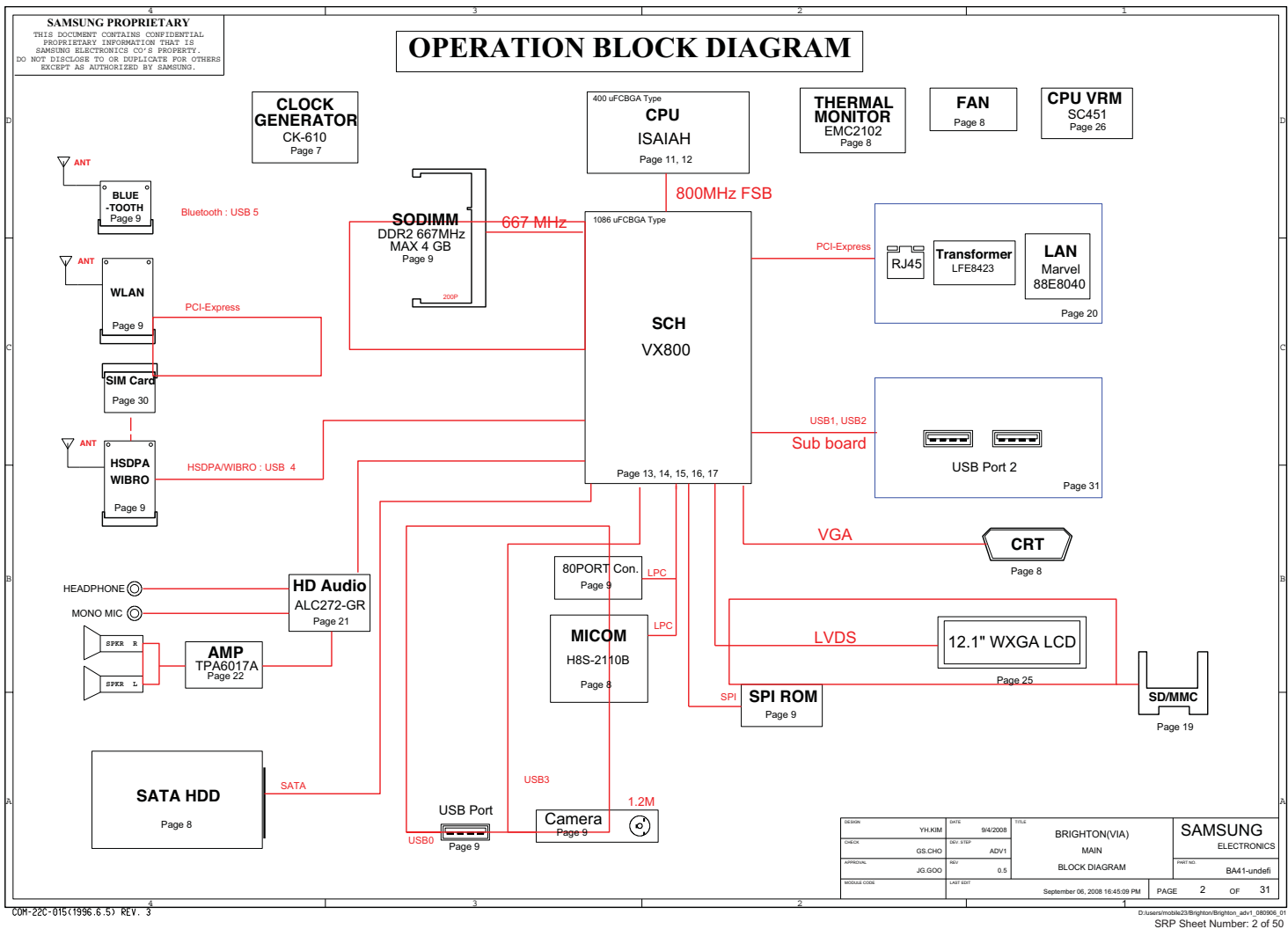
Page. 7 ---- CLOCK GENERATOR
Page. 8 ---- BLOCK1 - MICOM, THERMAL,
SATA_IF, CRT_IF
Page. 9 ---- BLOCK2 - WLAN, HSDPA, DDR2 SODIMM,
SPI ROM, LED SWITCH, USB(1),
DEBUG PORT, KBD,
BLUETOOTH, CAMERA, TOUCHPAD
Page. 10 ---- BLOCK3 - CHARGER, 3V 5V, DDR POWER
CHIPSET POWER
Page. 11 ---- VIA ISAIAH CPU(1/2)
Page. 12 ---- VIA ISAIAH CPU(2/2)
Page. 13~17- VX800
Page. 18 ---- VX800 STRAP
Page. 19 ---- MULTI CARD IF
Page. 20 ---- LAN(88E8040)
Page. 21~24- AUDIO CODEC(ALC272)
Page. 25 ---- LVDS
Page. 26 ---- CPU VRM POWER
Page. 27 ---- SWITCHED POWER
Page. 28 ---- DISCHARGER
Page. 29 ---- MOUNT HOLE
Page. 30 ---- SIM CARD & SUB BD CONNECTOR
Page. 31 ---- SUB BOARD (USB 2PORT)
Page. 32 ---- TEST POINTS

DESIGN	YH.KIM	DATE	9/4/2008	TITLE	BRIGHTON(VIA)	SAMSUNG
CHECK	GS.CHO	DEV. STEP	ADV1	MAIN		ELECTRONICS
APPROVAL	JG.GOO	REV	0.5	COVER		PART NO.
MODULE CODE		LAST EDIT				BA41-undefi
				September 06, 2008 16:45:09 PM	PAGE	1 OF 31

8. Block Diagram and Schematic

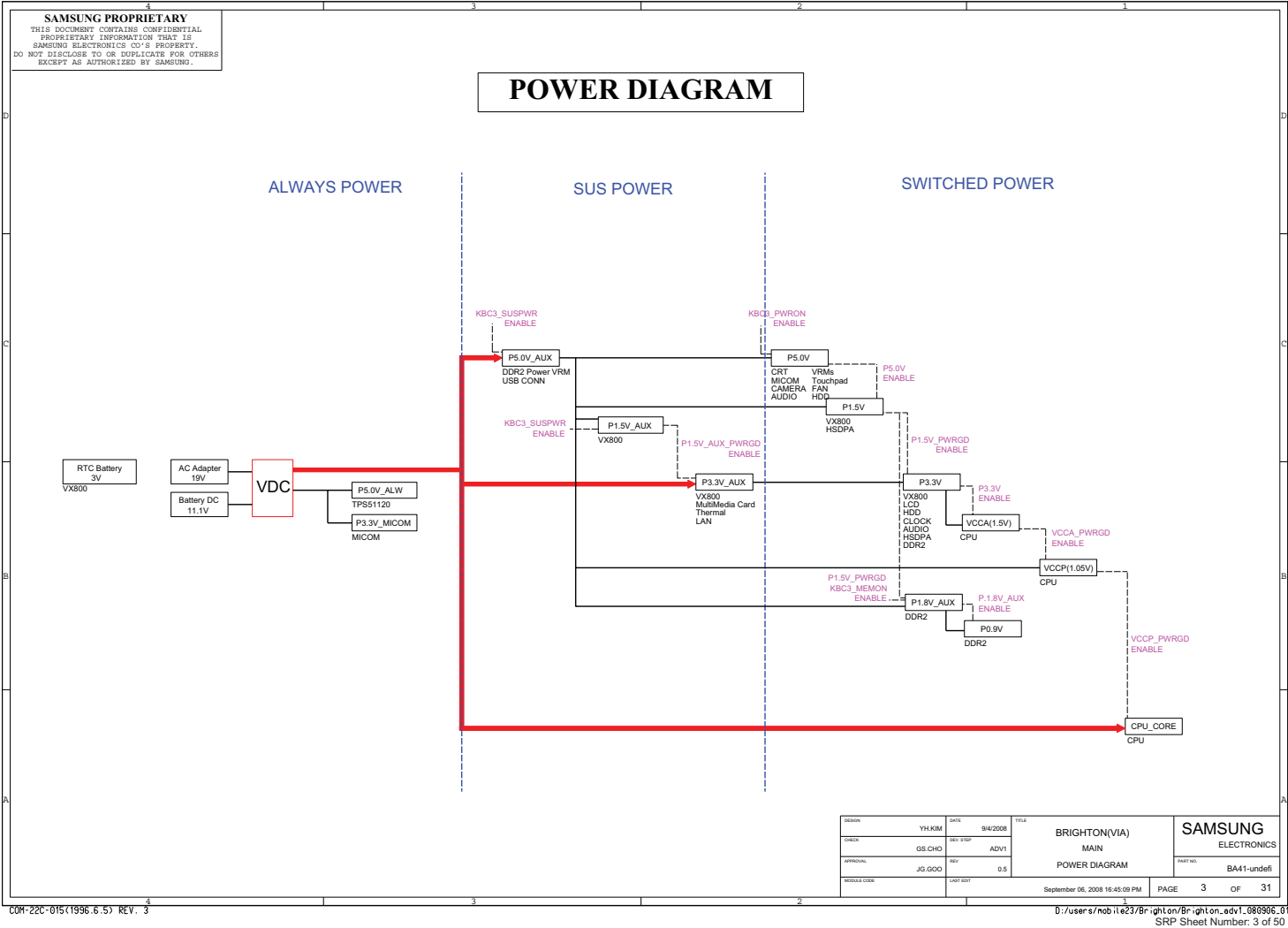
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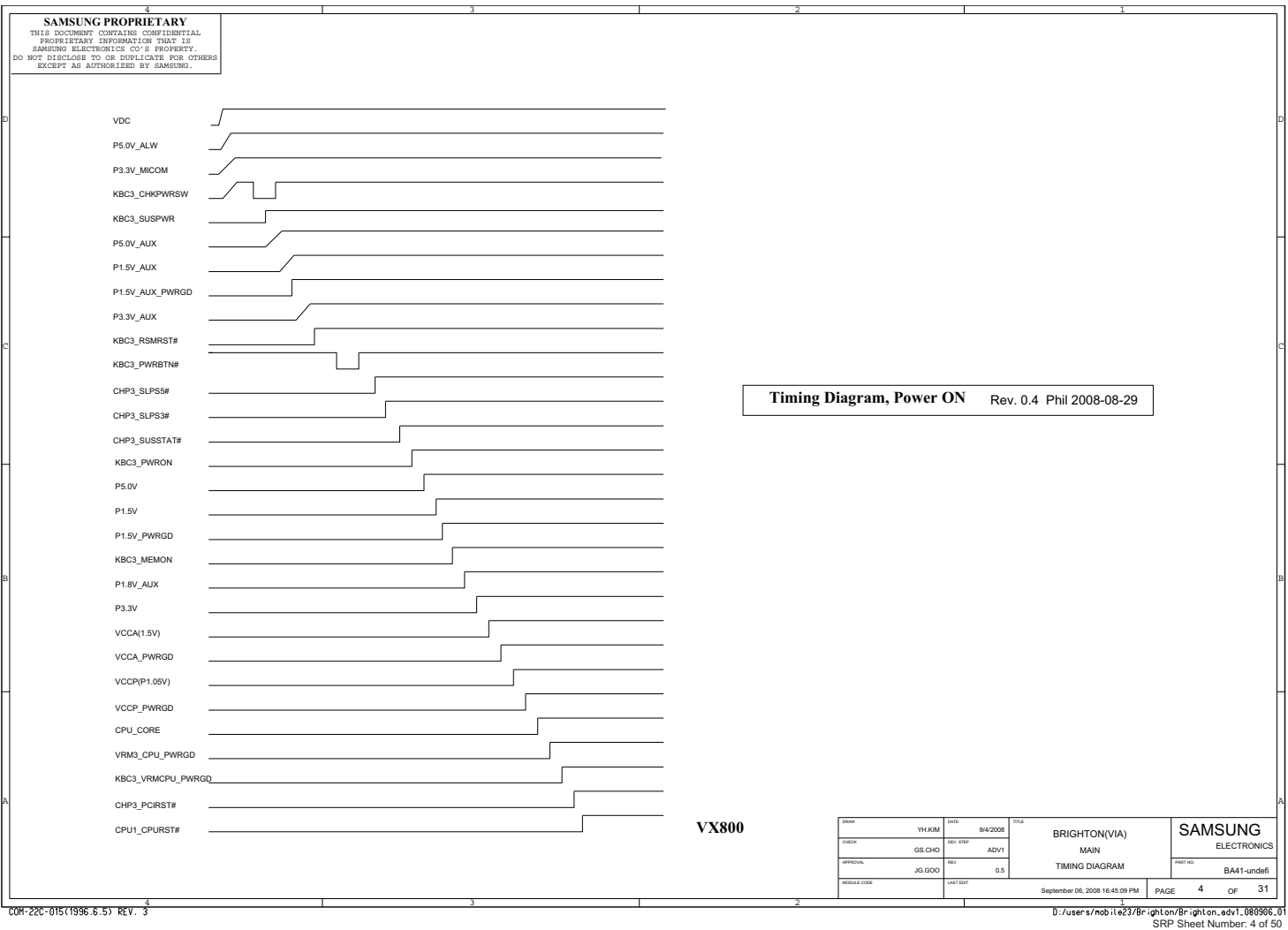
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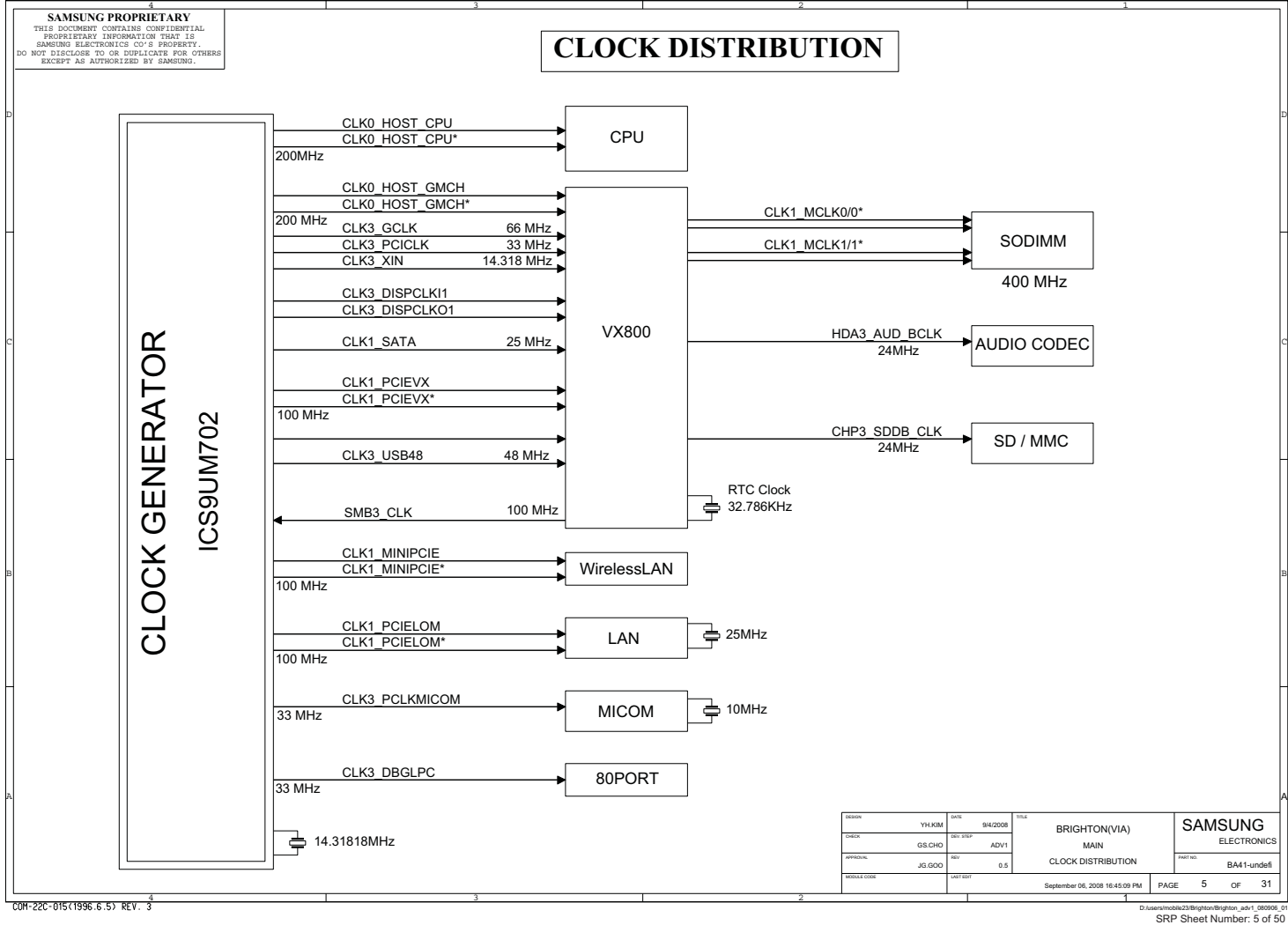
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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Power Rail	Devices (Page Number)
PSV	FAN(8) MICOM(8) CRT(8) CAMERA(8) AUDIO(20) VRM(25) TOUCHPAD(9) HDD(8)
P3.3V	VX800(13) LCD(24) HDD(8) CLOCK(7) AUDIO(20) HSDPA(9) DDR2(9)
P1.5V	VX800(13) HSDPA(9)
VCCA(P1.5V)	CPU(11)
VCCP(1.05V)	CPU(11)
PSV_AUX	DDR2 PWR VRM(10) USB(9,30)
P3.3V_AUX	VX800(13) MULTIMEDIA CARD(18) THERMAL(8) LAN(19)
P1.8V_AUX	DDR2(9)
P1.5V_AUX	VX800(13)
CPU_CORE	CPU(11)

Power Rail	Descriptions
PRTC_BAT VDC	3.3V (can drop to 2.0V min. in G3 state) supply for the RTC well. Primary DC system power supply (6 to 19V)
PSV_AUX	5.0V power rail (off in S4-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P1.5V_AUX	GMCHDDR II Power Source (off in S4-S5)
P1.5V_AUX	GMCH Power Source (off in S4-S5)
PSV	5.0V switched power rail (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
VCCA(1.5V)	1.5V CPU power rail (off in S3-S5)
VCCP(1.05V)	1.05V CPU power rail (off in S3-S5)
CPU_CORE	Core voltage via VIO NANO CPU
P3.3V_MICOM	3.3V always on power rail for MICOM
LCD_VDD03.3V	3.3V (LCD)
VCC_OST	5V (CRT)
2.5V_LAN	2.5V (88E8040)
P47S_AUD	4.75V (ALC272)
P5.0V_AUD	5V (ALC272)
P5.0V_AMP	5V (Audio AMP)

VID5	VID4	VID3	VID2	VID1	VID0	Voltage	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	0	0	0	0	0	1.708 V	1	0	0	0	0	0	1.196 V
0	0	0	0	0	1	1.692 V	1	0	0	0	0	1	1.180 V
0	0	0	0	1	0	1.676 V	1	0	0	0	1	0	1.164 V
0	0	0	0	1	1	1.660 V	1	0	0	0	1	1	1.148 V
0	0	0	1	0	0	1.644 V	1	0	0	1	0	0	1.132 V
0	0	0	1	0	1	1.628 V	1	0	0	1	0	1	1.116 V
0	0	0	1	1	0	1.612 V	1	0	0	1	1	0	1.100 V
0	0	0	1	1	1	1.596 V	1	0	0	1	1	1	1.084 V
0	0	1	0	0	0	1.580 V	1	0	1	0	0	0	1.068 V
0	0	1	0	0	1	1.564 V	1	0	1	0	0	1	1.052 V
0	0	1	0	1	0	1.548 V	1	0	1	0	1	0	1.036 V
0	0	1	0	1	1	1.532 V	1	0	1	0	1	1	1.020 V
0	0	1	1	0	0	1.516 V	1	0	1	1	0	0	1.004 V
0	0	1	1	0	1	1.500 V	1	0	1	1	0	1	0.988 V
0	0	1	1	1	0	1.484 V	1	0	1	1	1	0	0.972 V
0	0	1	1	1	1	1.468 V	1	0	1	1	1	1	0.956 V
0	1	0	0	0	0	1.452 V	1	0	1	0	0	0	0.940 V
0	1	0	0	0	1	1.436 V	1	0	1	0	0	1	0.924 V
0	1	0	0	1	0	1.420 V	1	0	1	0	1	0	0.908 V
0	1	0	0	1	1	1.404 V	1	0	1	0	1	1	0.892 V
0	1	0	1	0	0	1.388 V	1	0	1	1	0	0	0.876 V
0	1	0	1	0	1	1.372 V	1	0	1	1	0	1	0.860 V
0	1	0	1	1	0	1.356 V	1	0	1	1	1	0	0.844 V
0	1	0	1	1	1	1.340 V	1	0	1	1	1	1	0.828 V
0	1	1	0	0	0	1.324 V	1	1	0	0	0	0	0.812 V
0	1	1	0	0	1	1.308 V	1	1	0	0	0	1	0.796 V
0	1	1	0	1	0	1.292 V	1	1	1	0	0	0	0.780 V
0	1	1	0	1	1	1.276 V	1	1	1	0	0	1	0.764 V
0	1	1	1	0	0	1.260 V	1	1	1	1	0	0	0.748 V
0	1	1	1	0	1	1.244 V	1	1	1	1	0	1	0.732 V
0	1	1	1	1	0	1.228 V	1	1	1	1	0	1	0.716 V
0	1	1	1	1	1	1.212 V	1	1	1	1	1	0	0.700 V
						Refer to case7?							
													DOTHAN-ULV Base Stealely
													HIGH FREQUENCY Mode
													DOTHAN-ULV Base Stealely
													LOW FREQUENCY Mode

SRP Sheet Number: 6 of 50

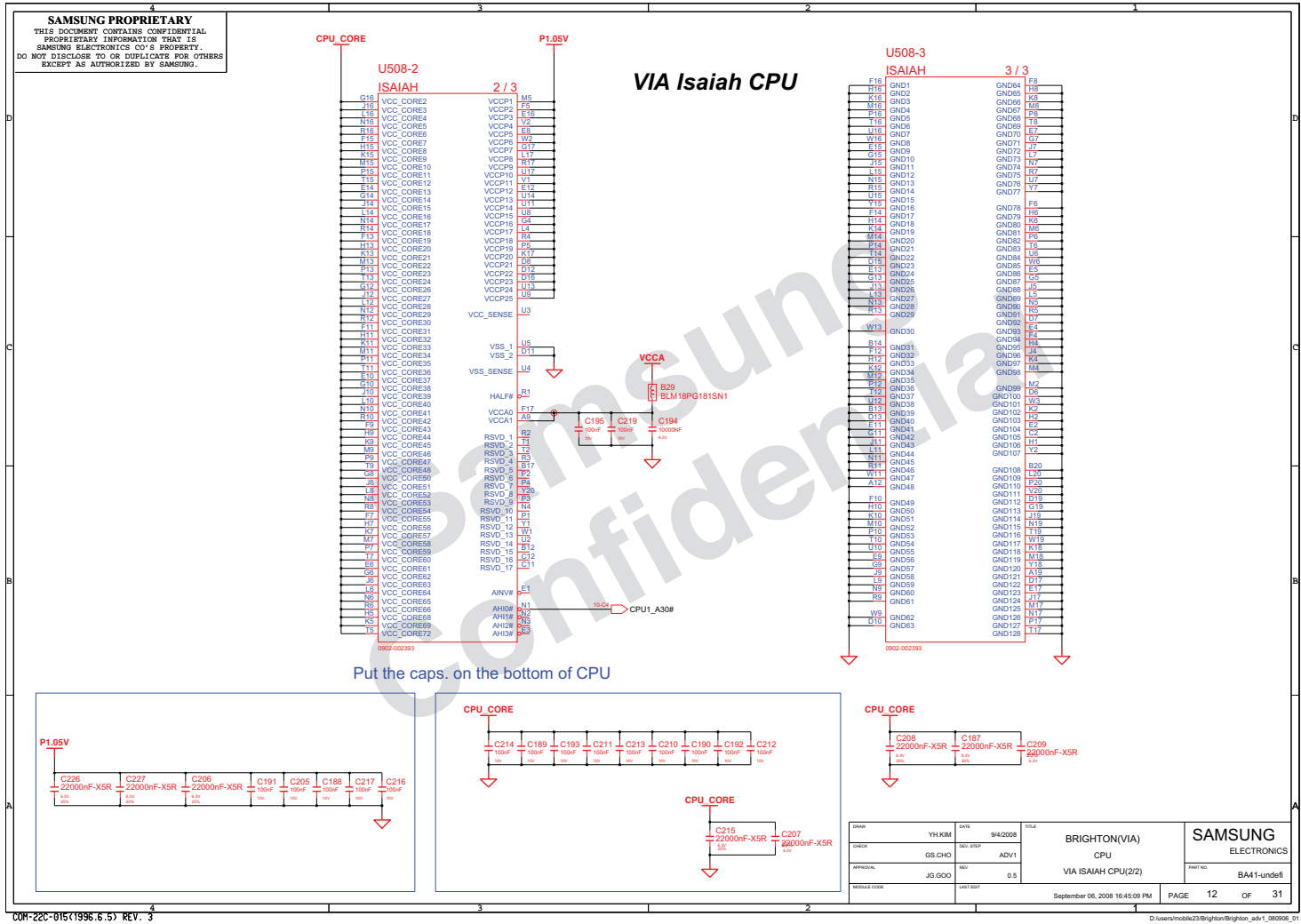
- ## 8. Block Diagram and Schematic



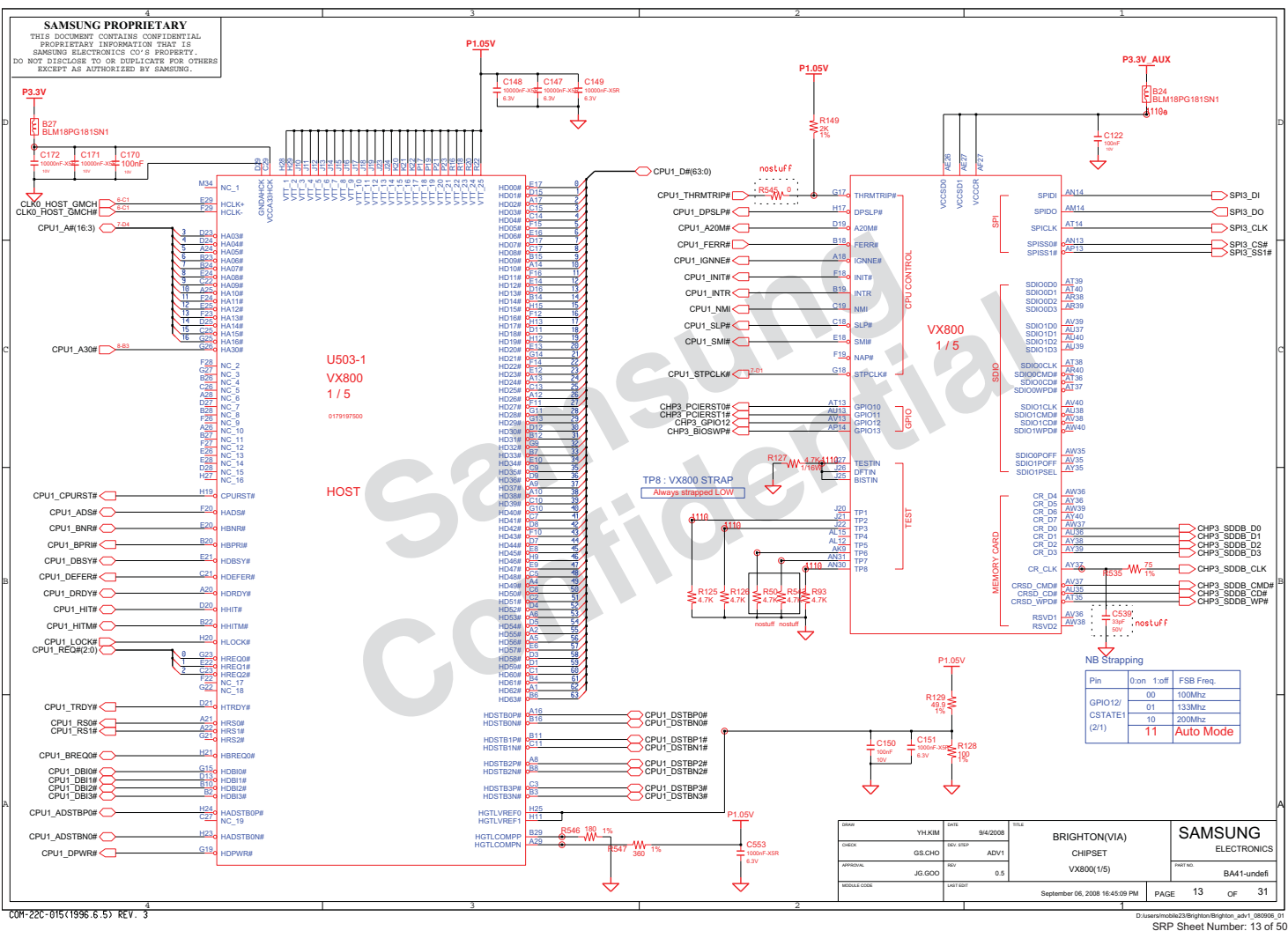
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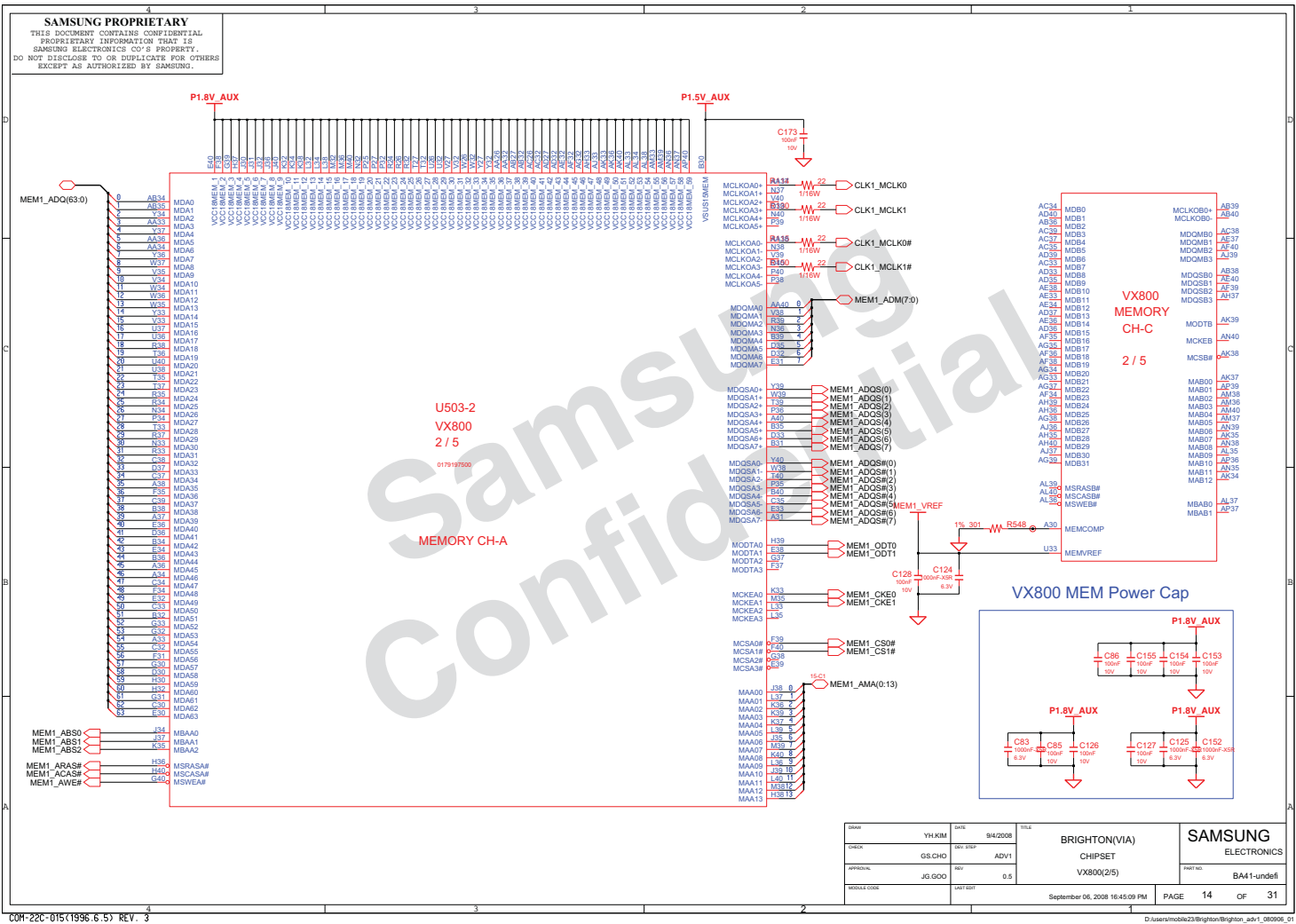
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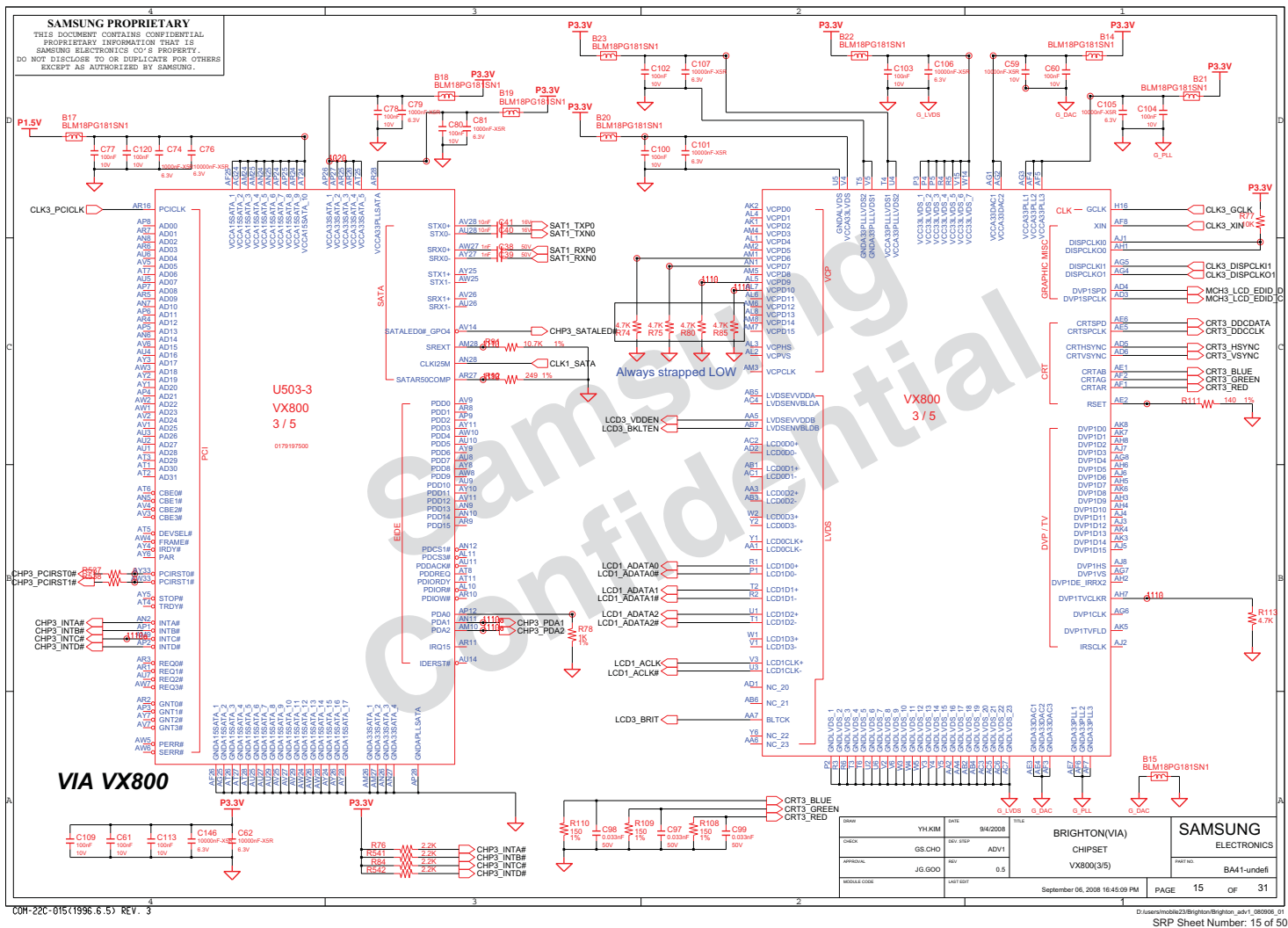
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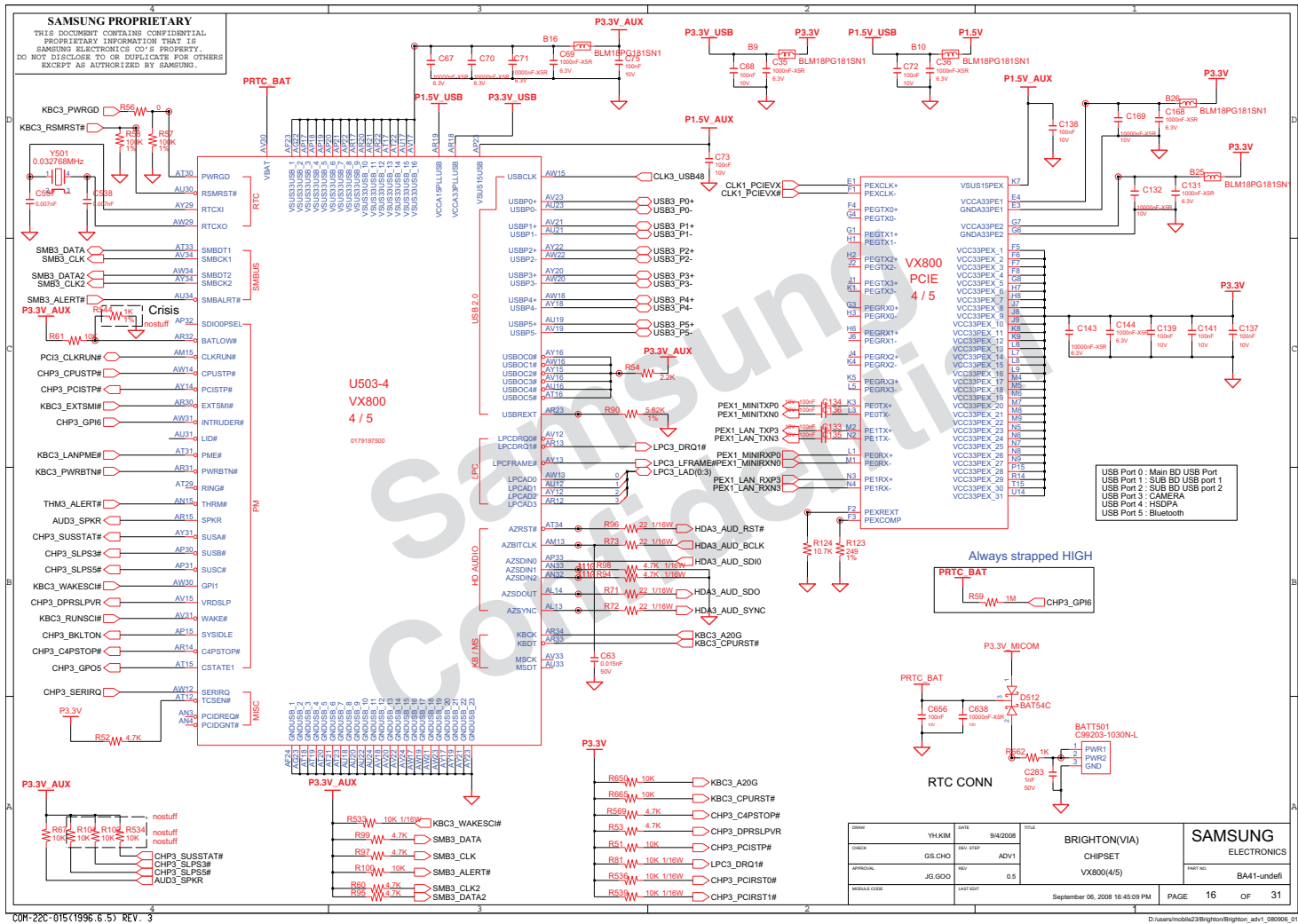
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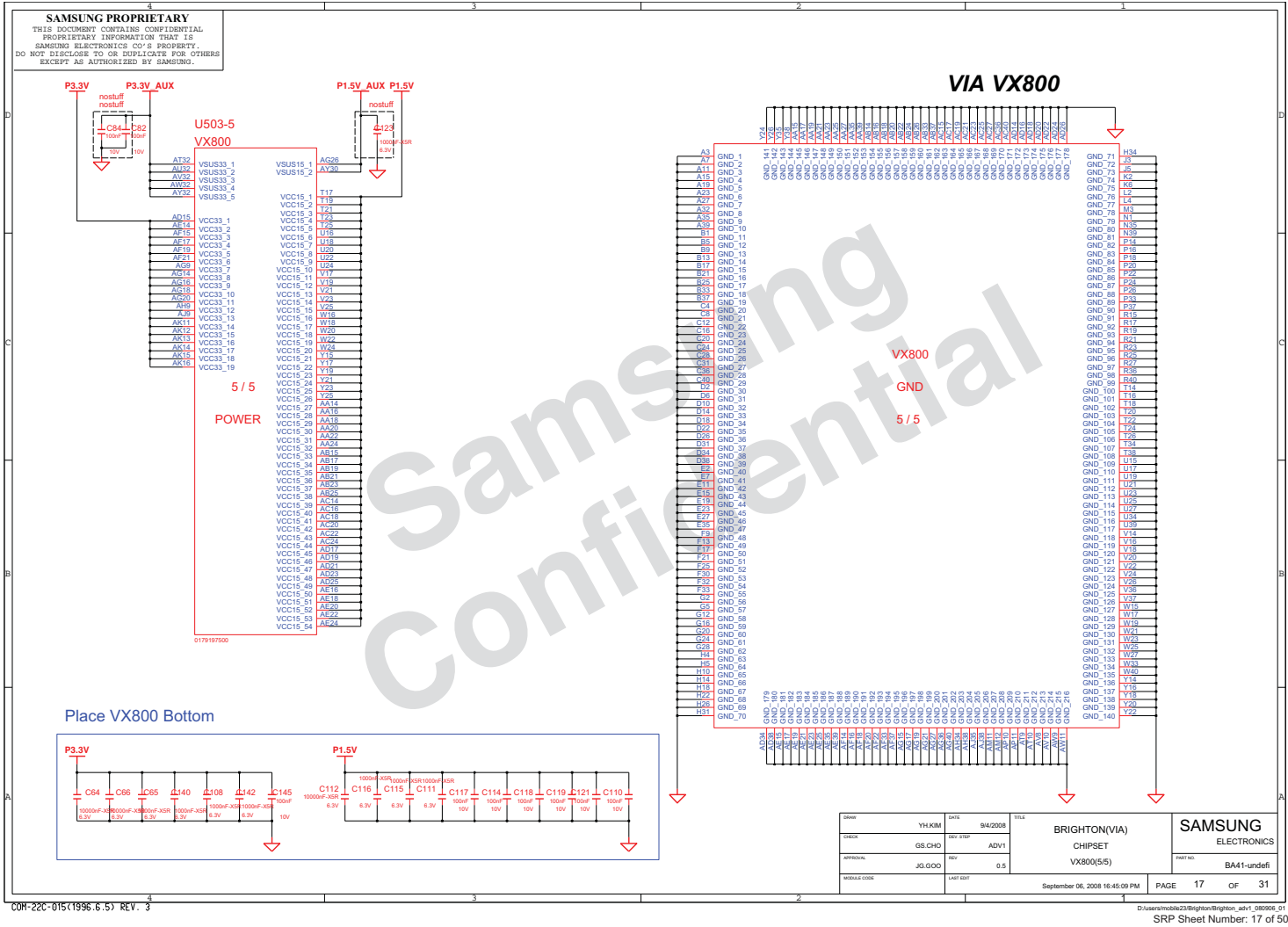
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	Signal	Ball#	Function	Description
	GPIO12 CSTATE1	AV13 AT15	FSB Clock AT15	State(GPIO12 : CSTATE1) Mode(MHz) LL 100MHz LH 133MHz HL 200MHz HH Auto
	SYSIDLE	AP15	IO Queue Depth	L : 12-level deep H : 1-level deep
	GPIO13	AP14	GTL Pull-up	L : Enable internal GTL Pull-up H : Disable internal GTL Pull-up
	PDA1	AN11	Dual Processor Configuration	L : Single Processor H : Dual Processor
	PDA2	AM10	PLL_OK Source Selection	L : PLL_OK from PLL H : PLL_OK_from logic counter
	AZSDOUT	AL14	Auto Reboot	L : Enable H : Disable
	AZSYNC	AL13	LPC FWH Command	L : Enable H : Disable
	AZBITCLK	AM13	SPI/LPC ROM Select	L : LPC ROM H : SPI ROM
	SPISS[1:0]#	AP13 AN13	IDE Controller [sata table support]	State(SPISS[1:0]#) Mode LL IDE Reserved

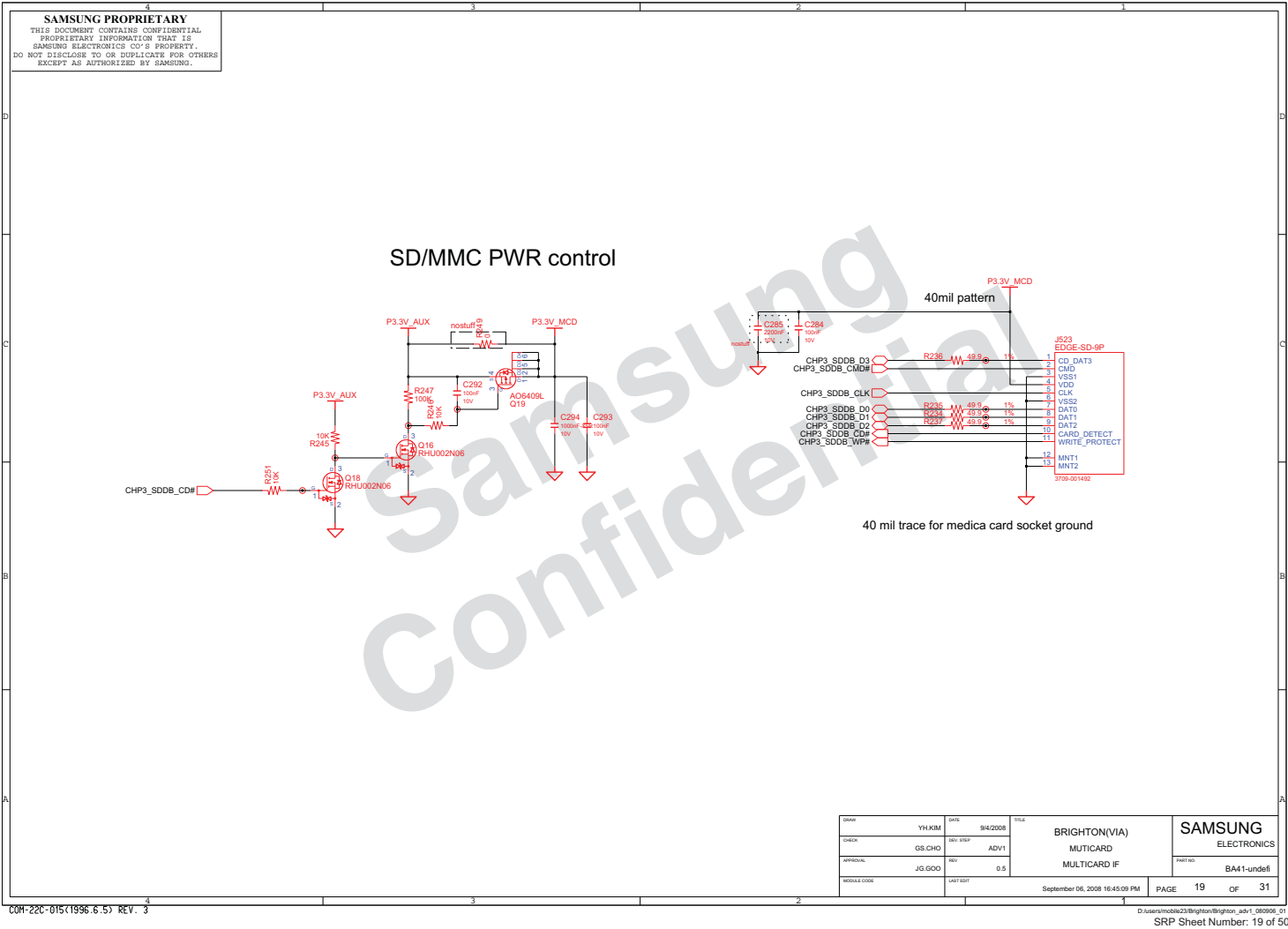
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APPROVAL	JG.GOO	REV		0.5	VX800 STRAP	PART NO. BA41-undefi
REWORK CODE		LAST EDIT	September 06, 2008 16:45:09 PM	PAGE	18	OF 31

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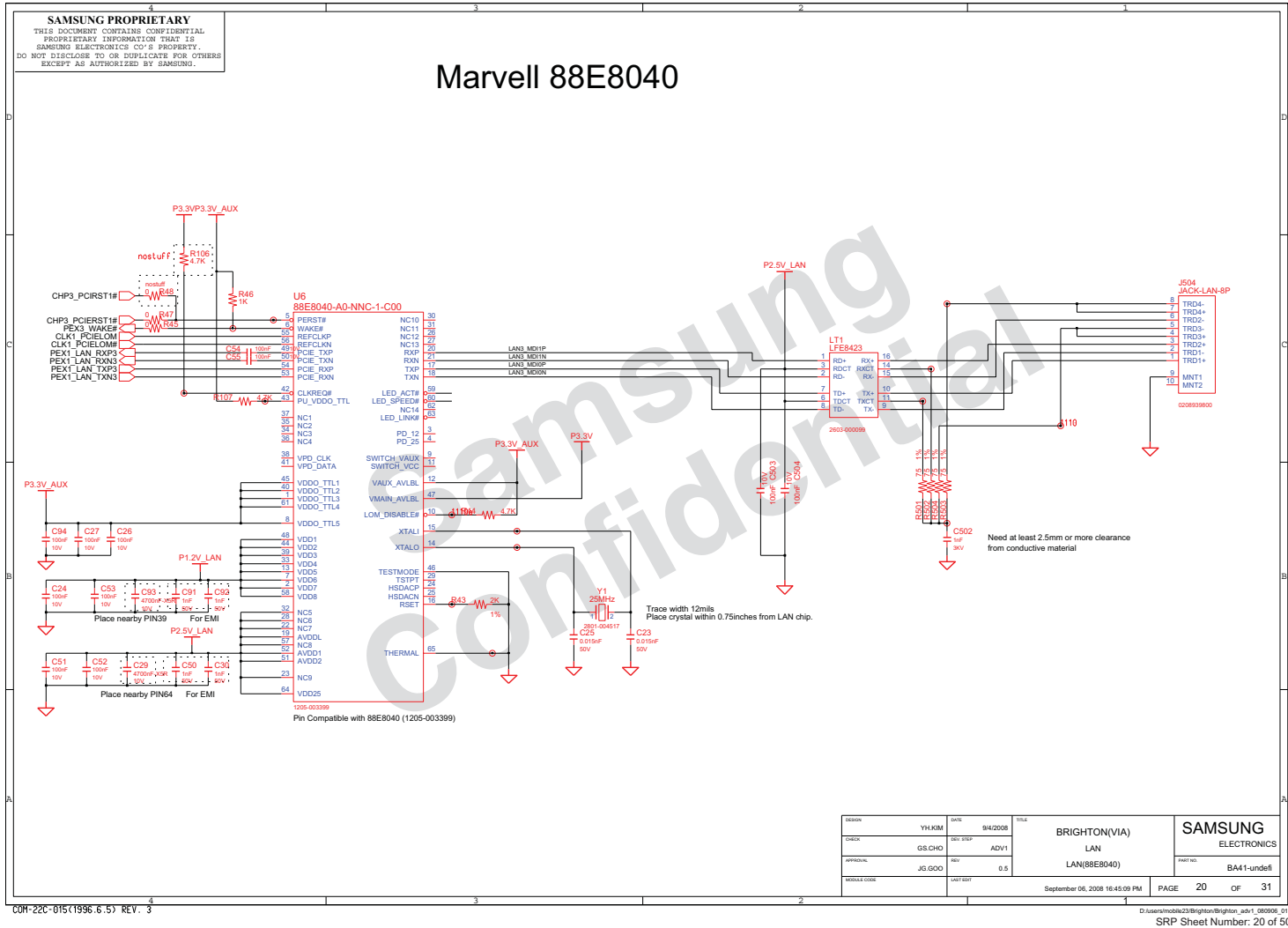
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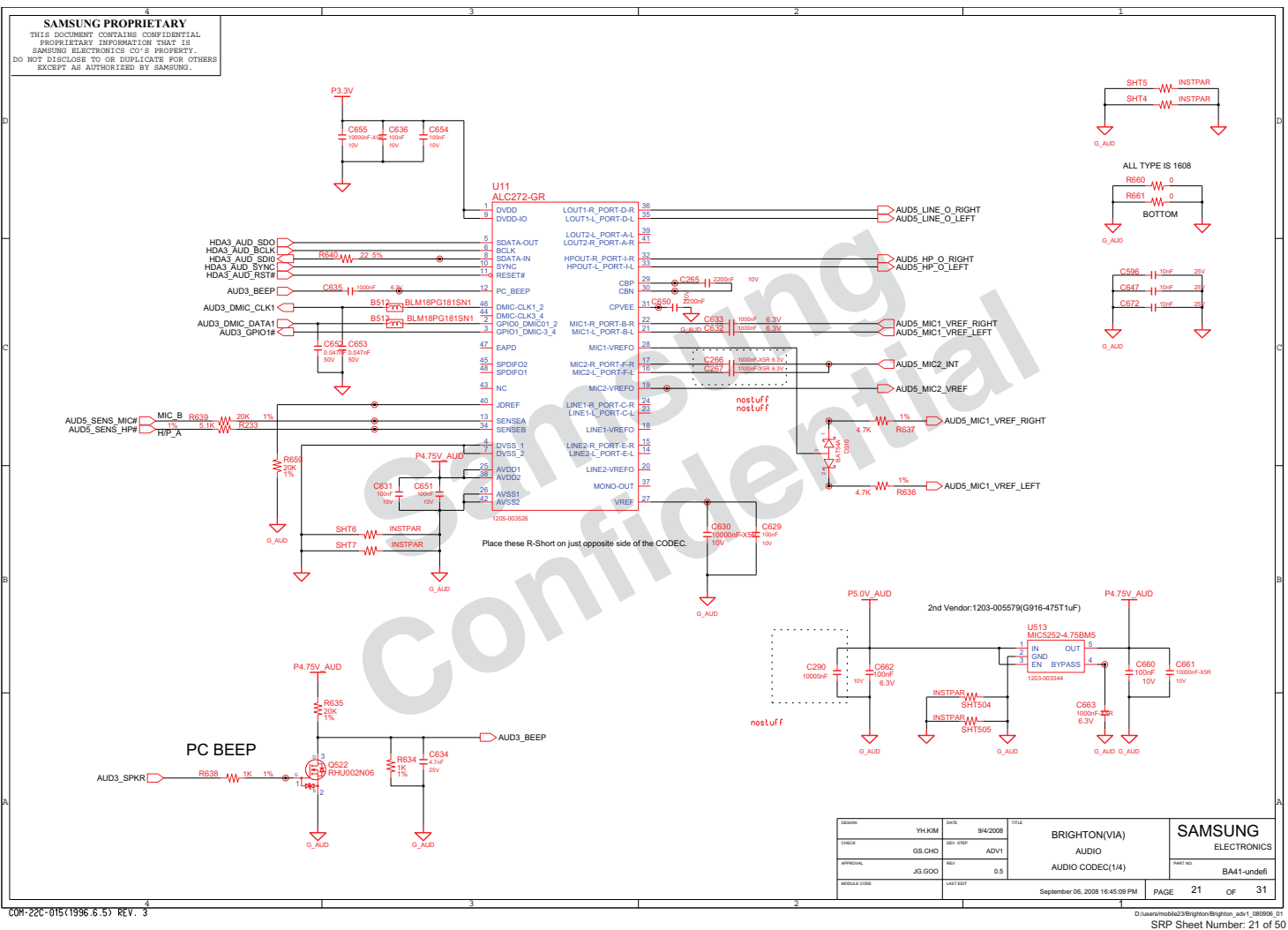
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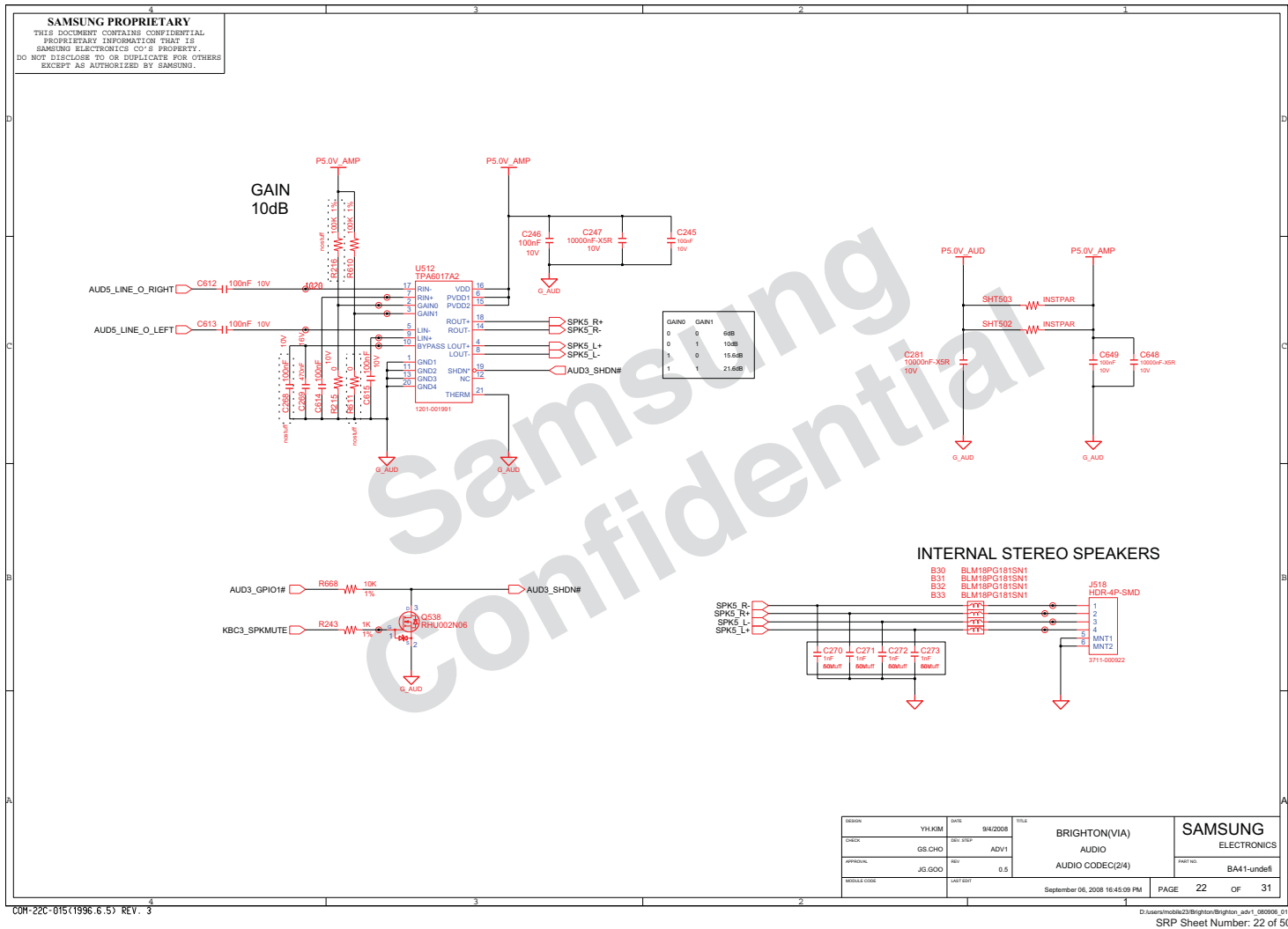
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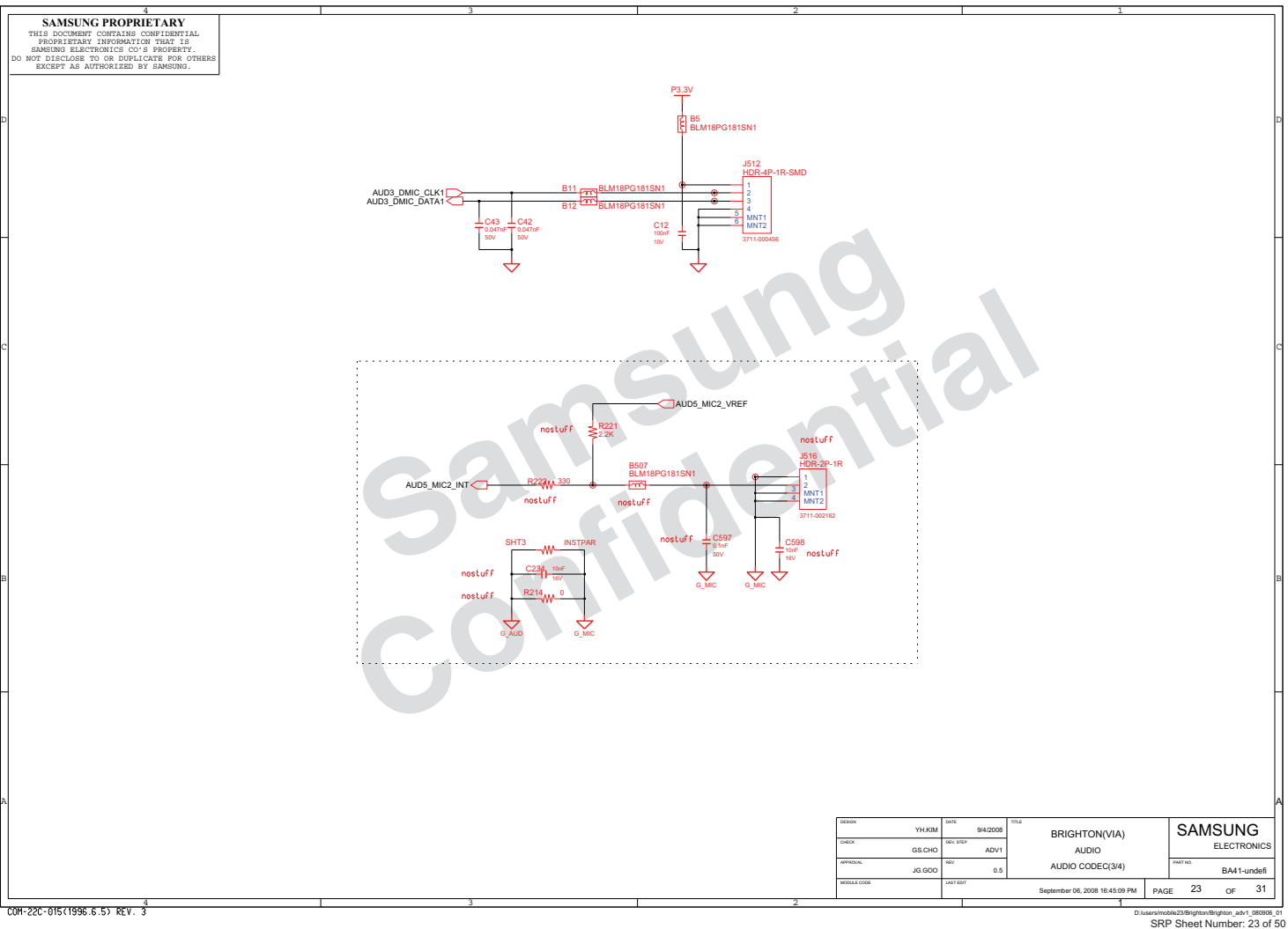


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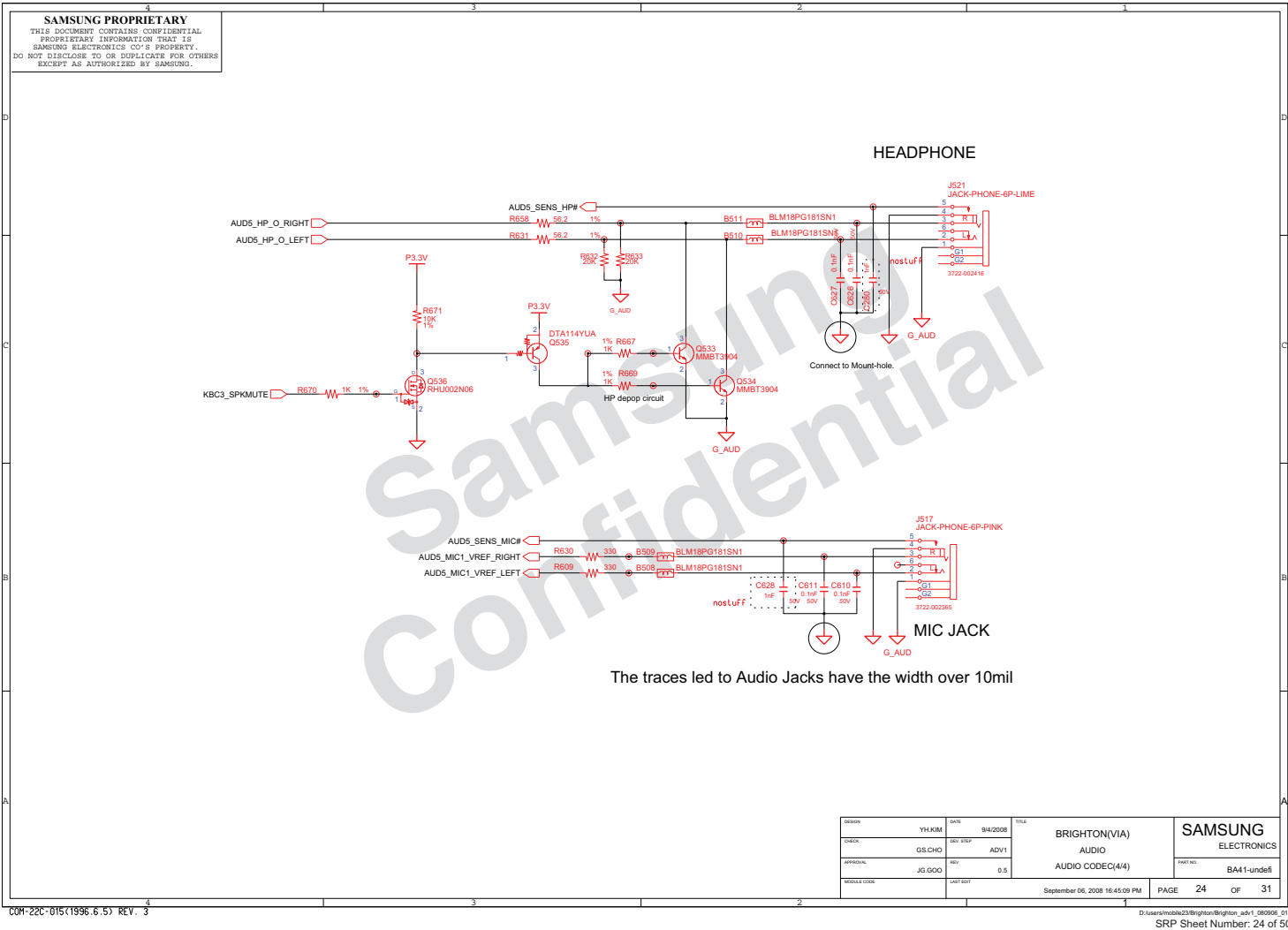
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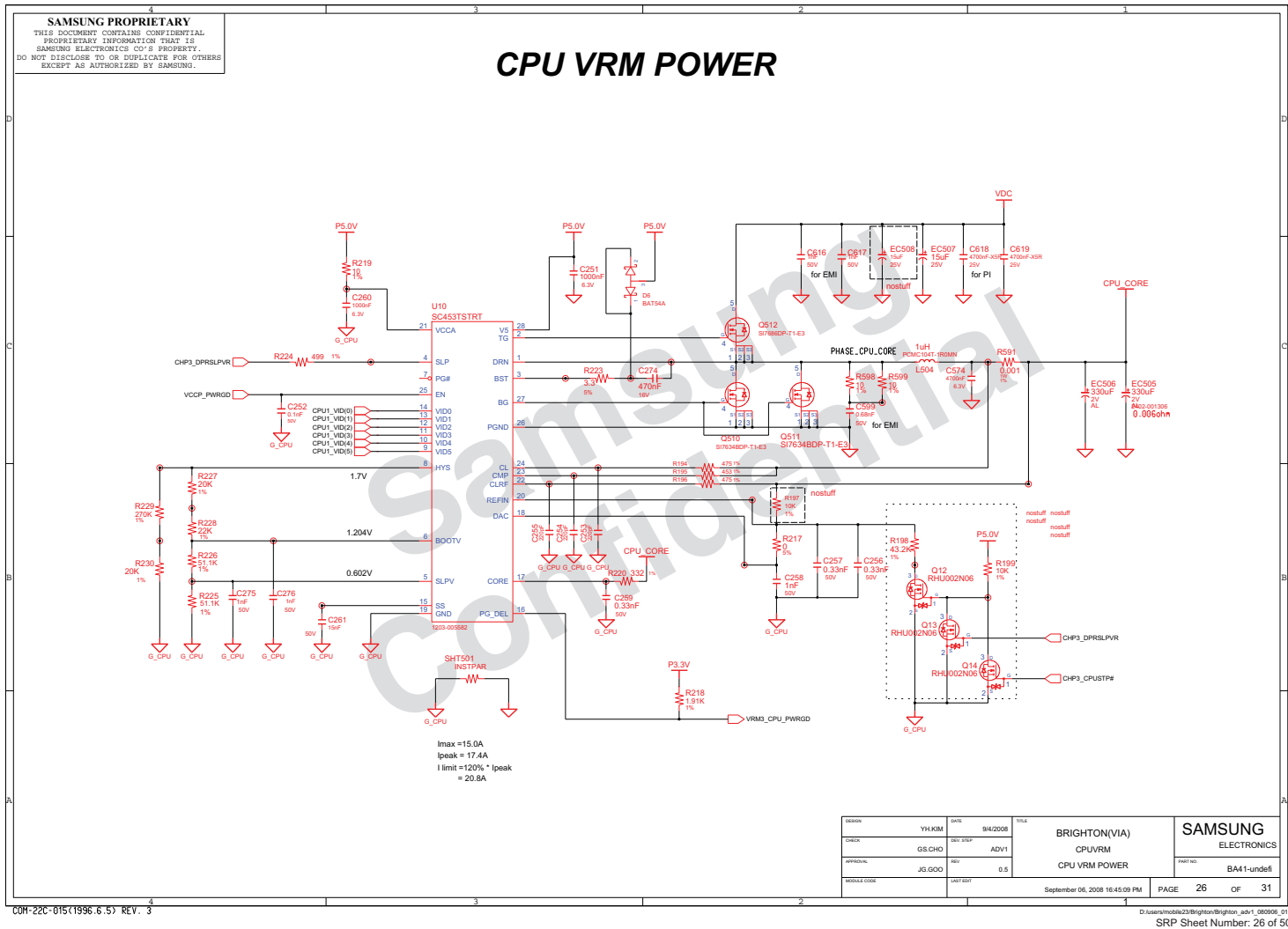
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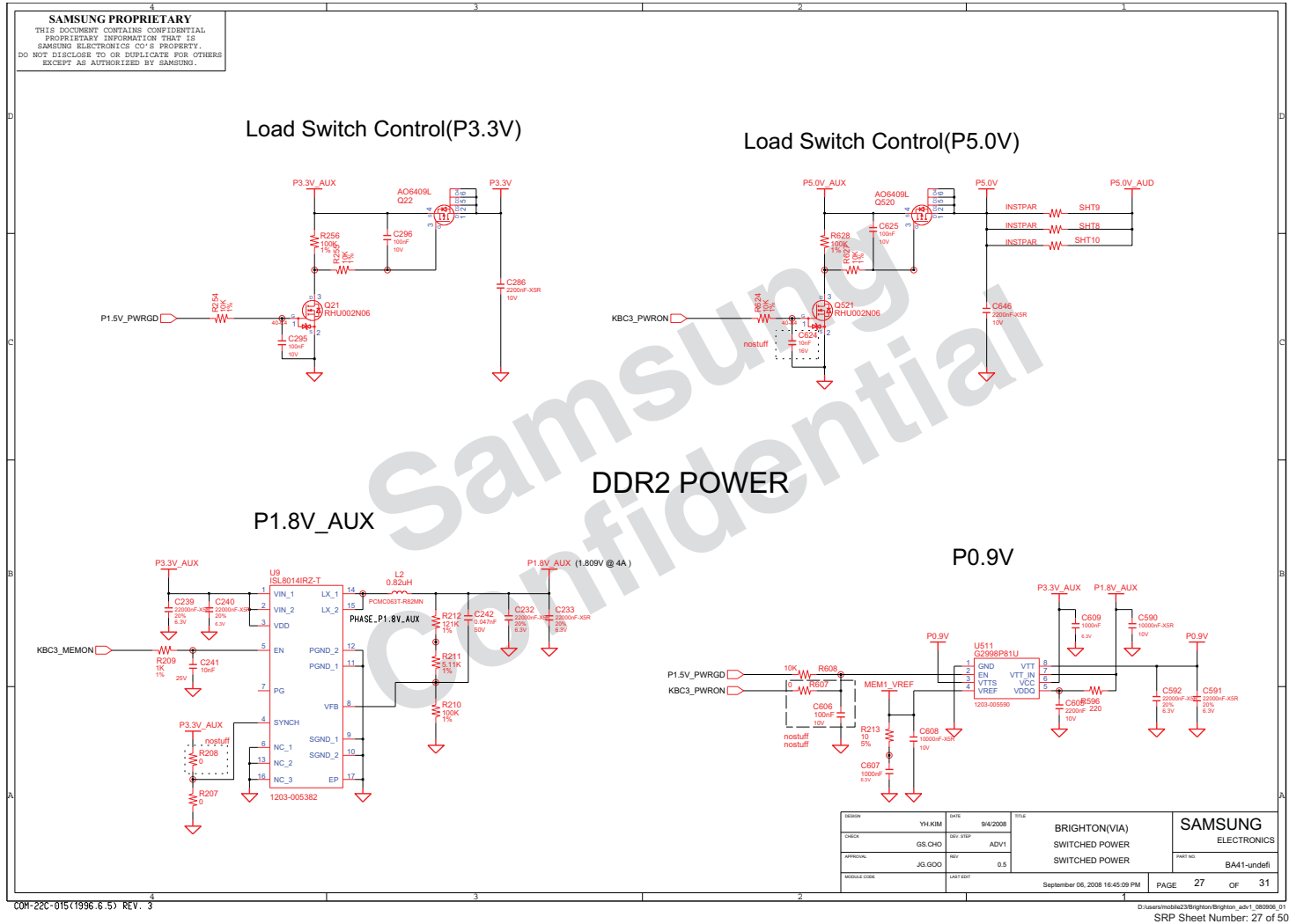


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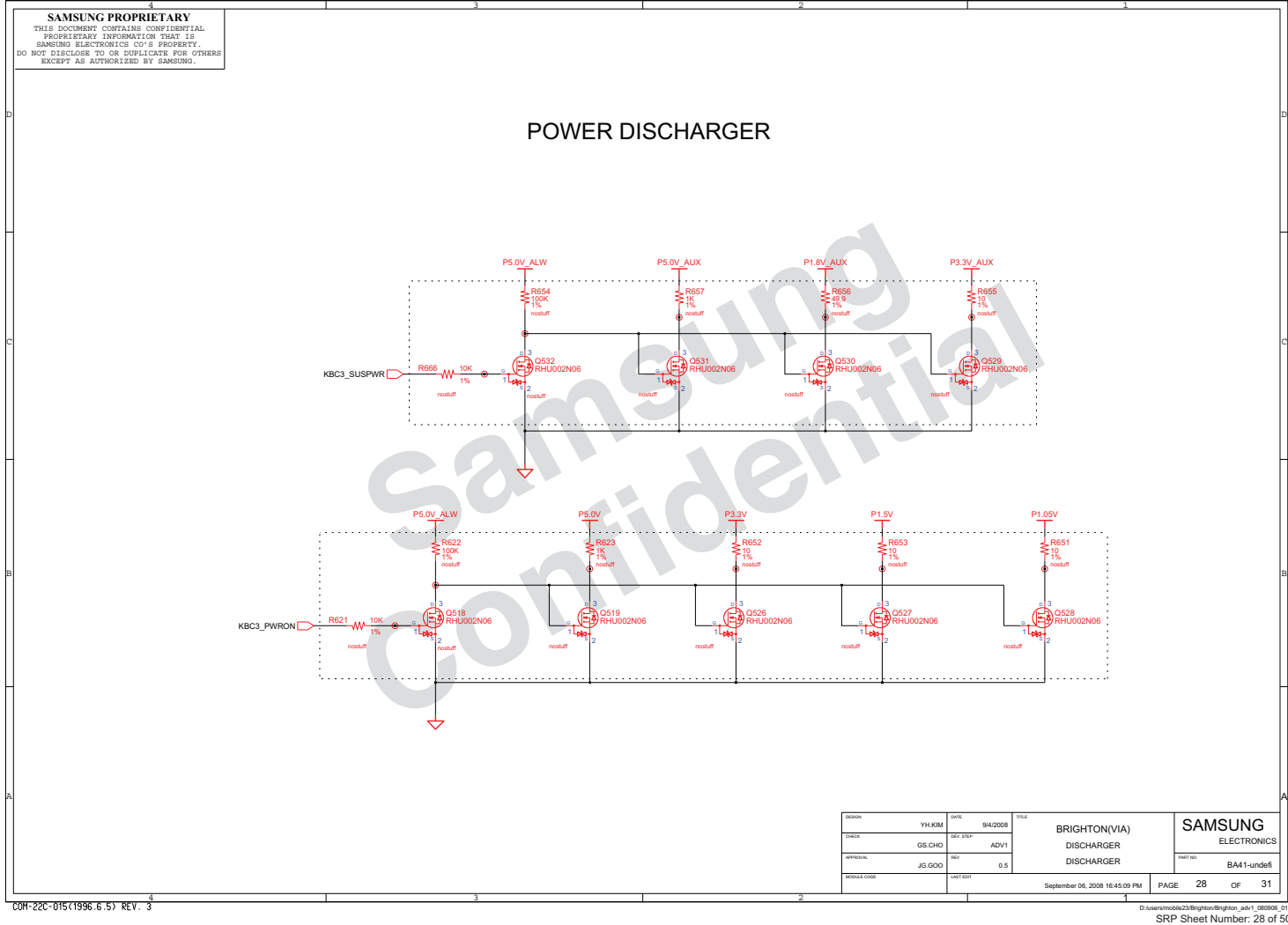
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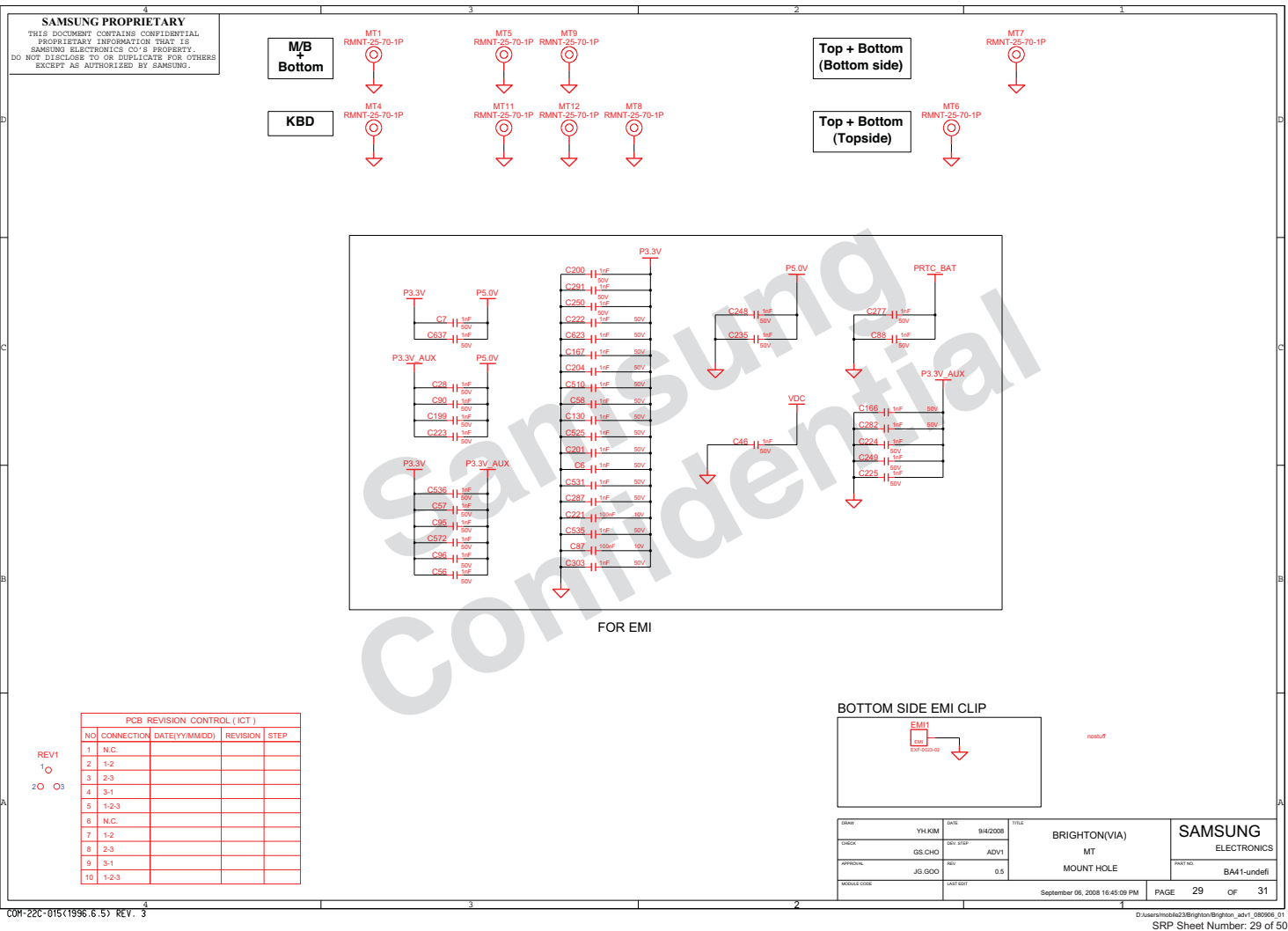
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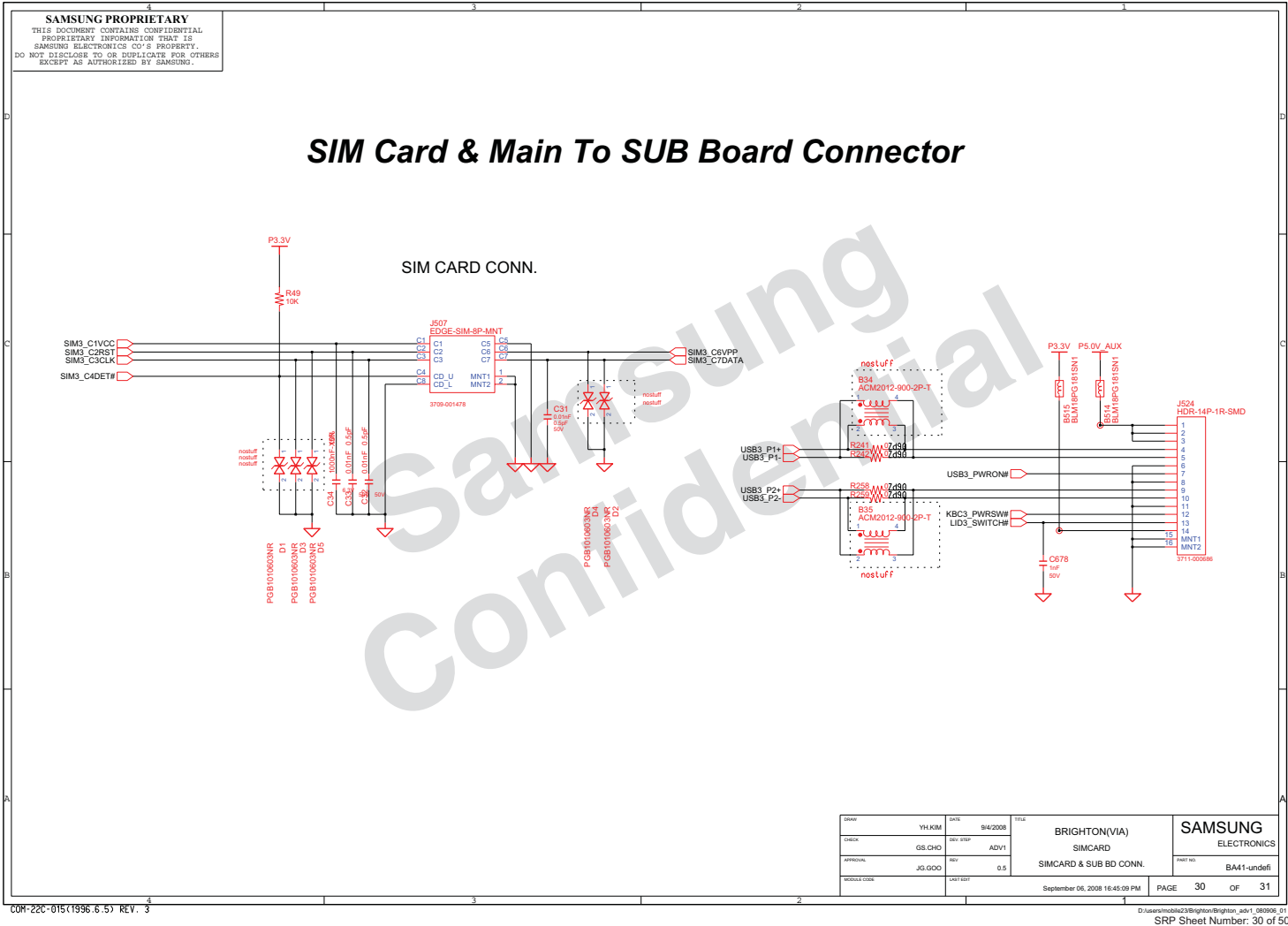
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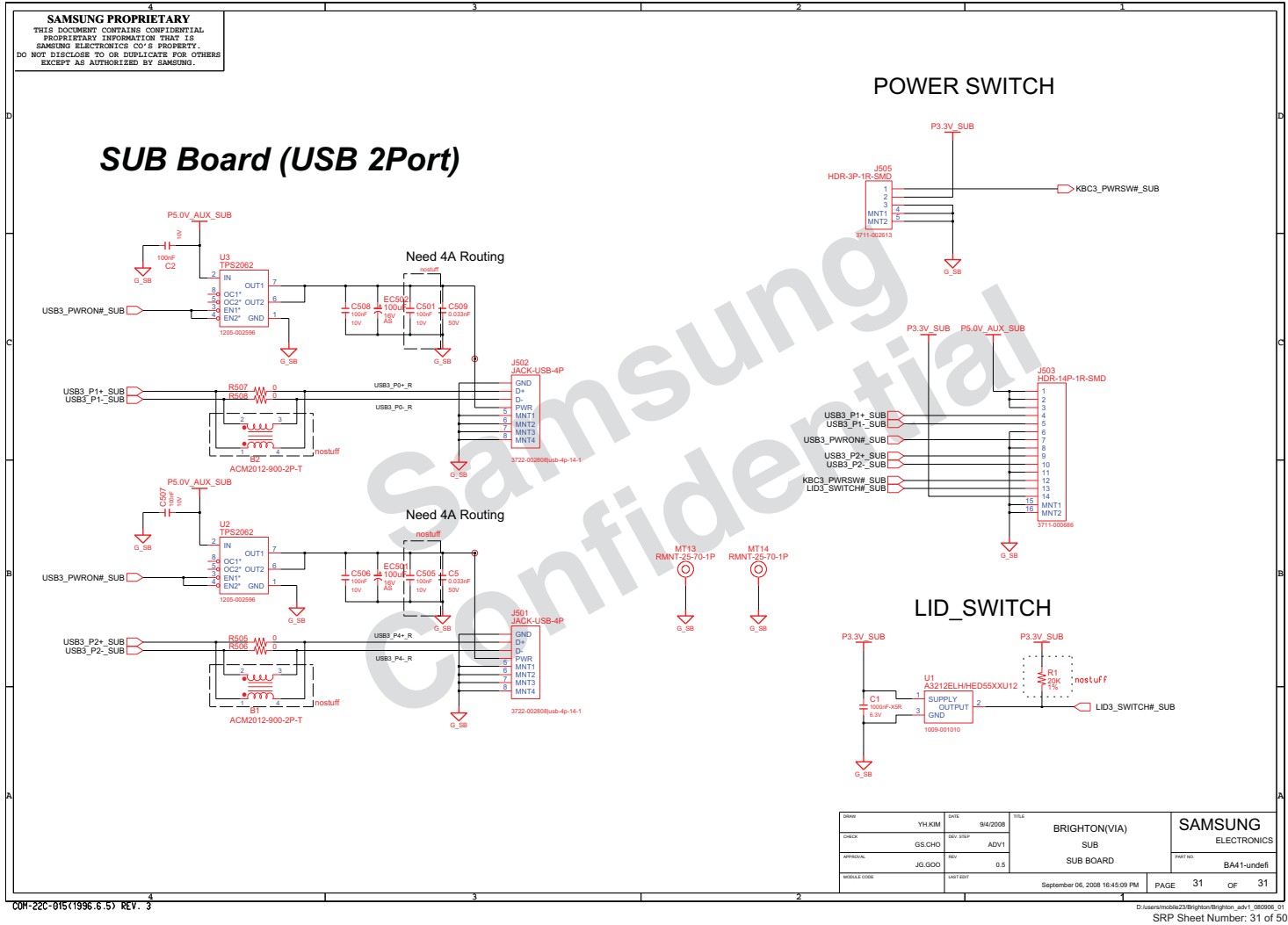
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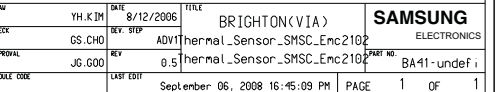


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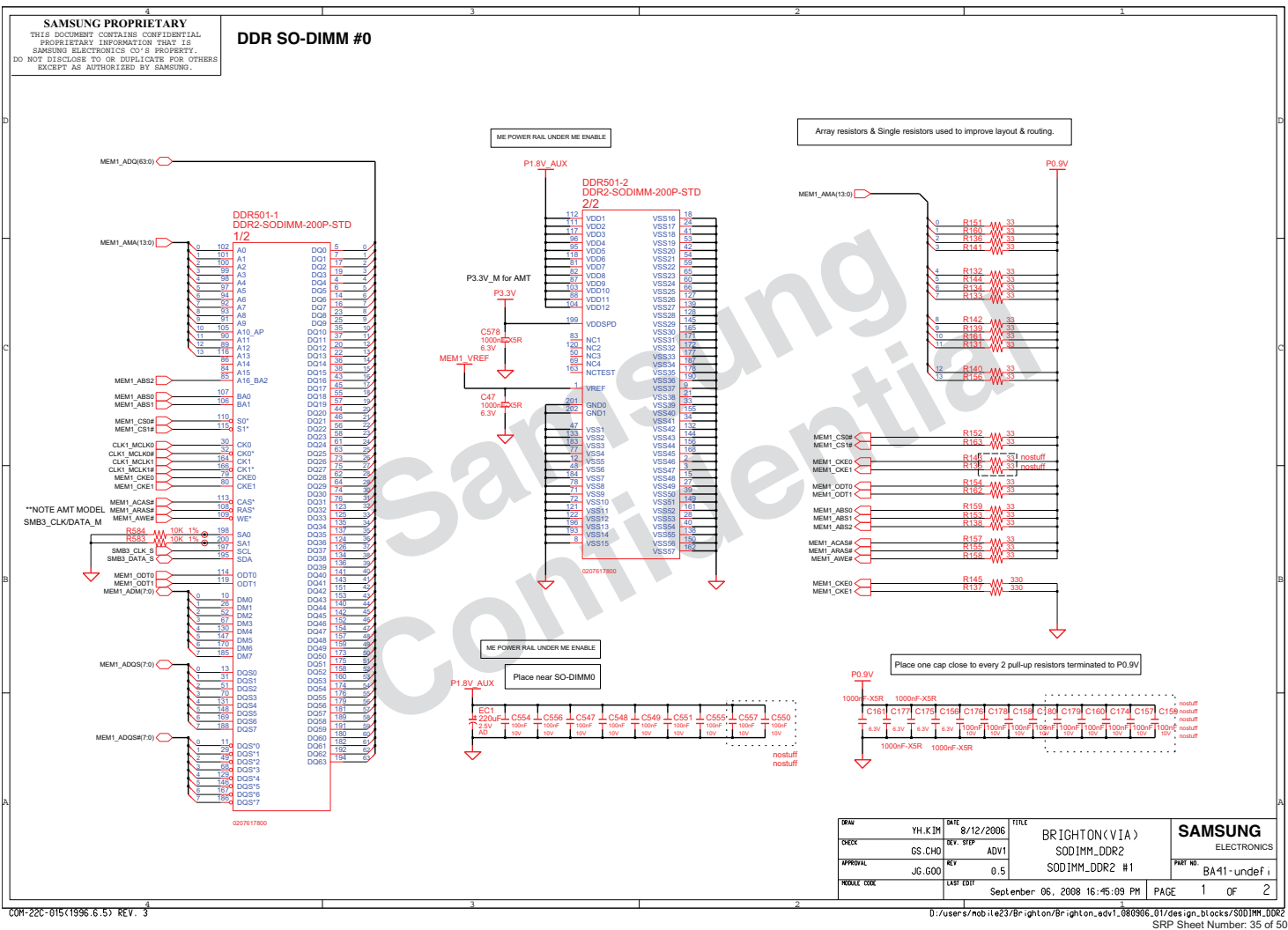


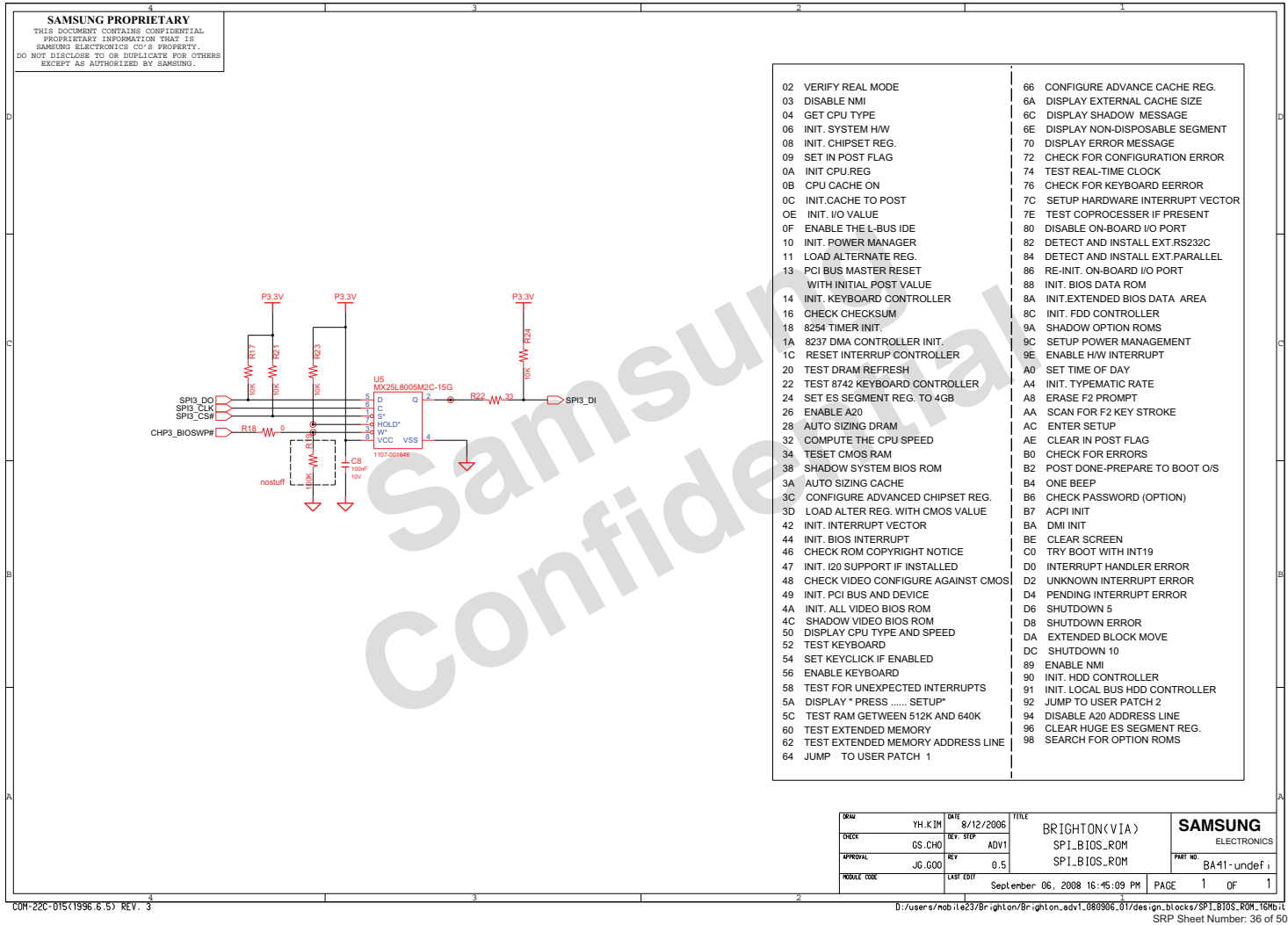
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- ## 8. Block Diagram and Schematic



8. Block Diagram and Schematic

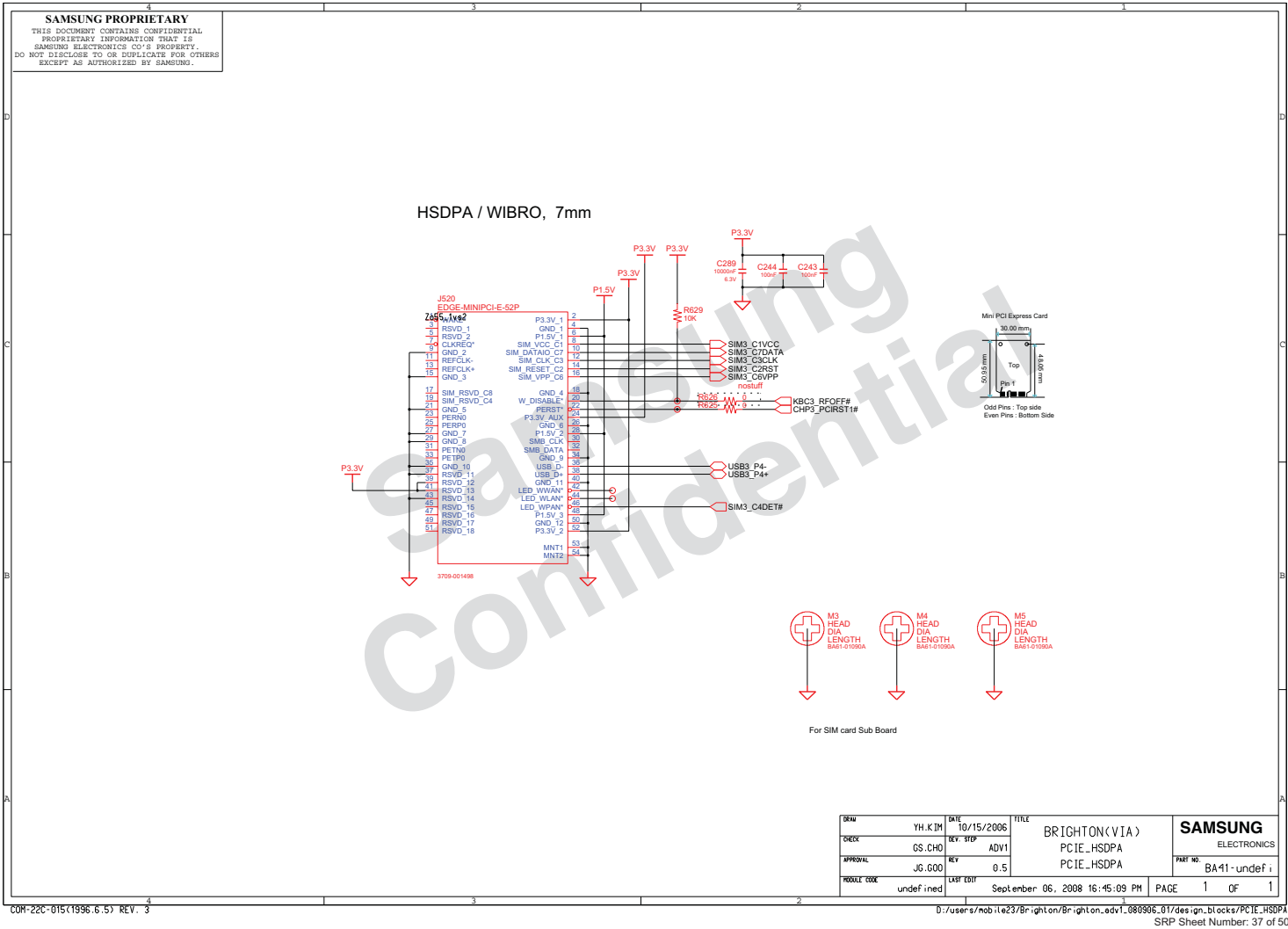




8. Block Diagram and Schematic

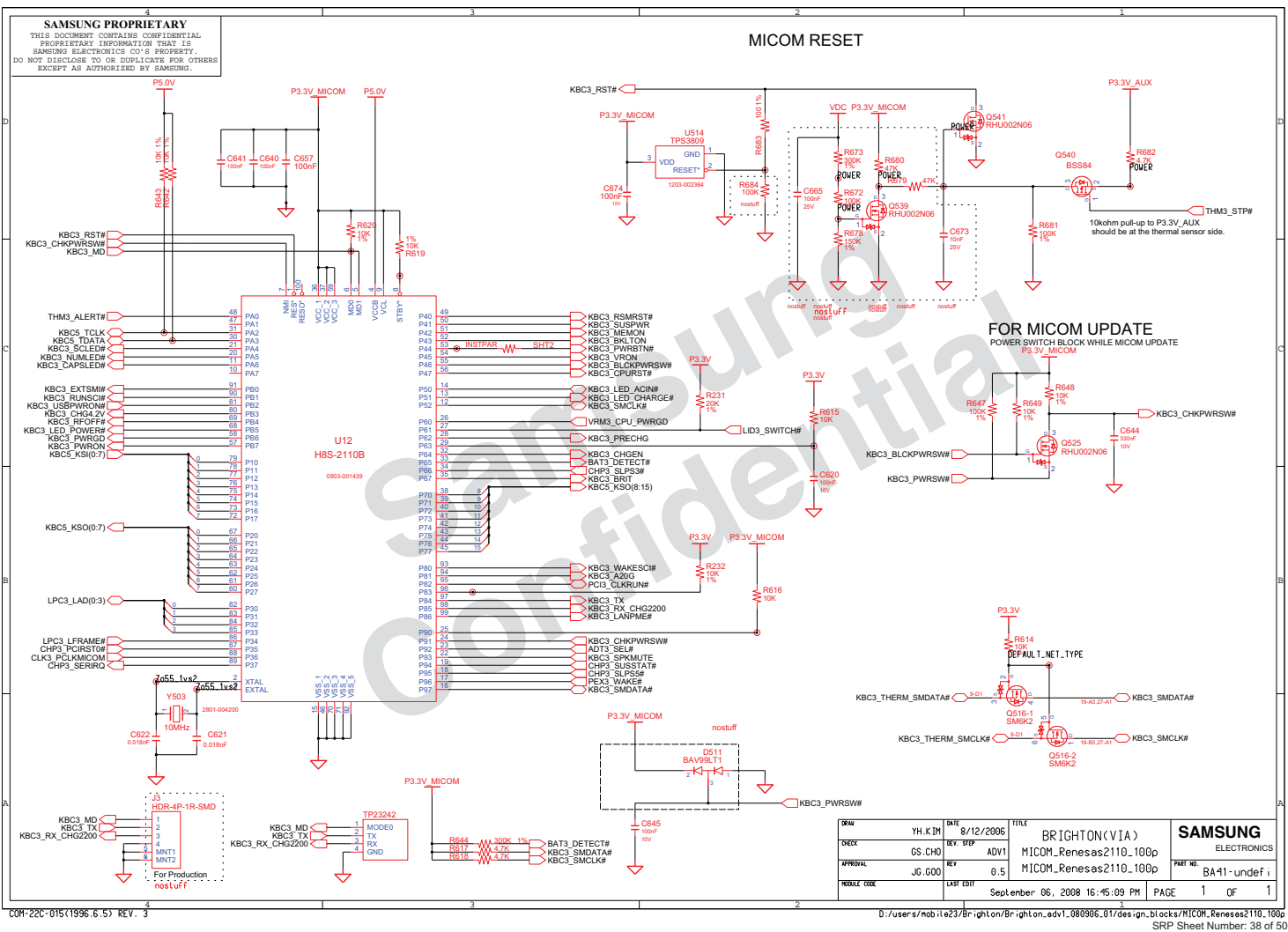
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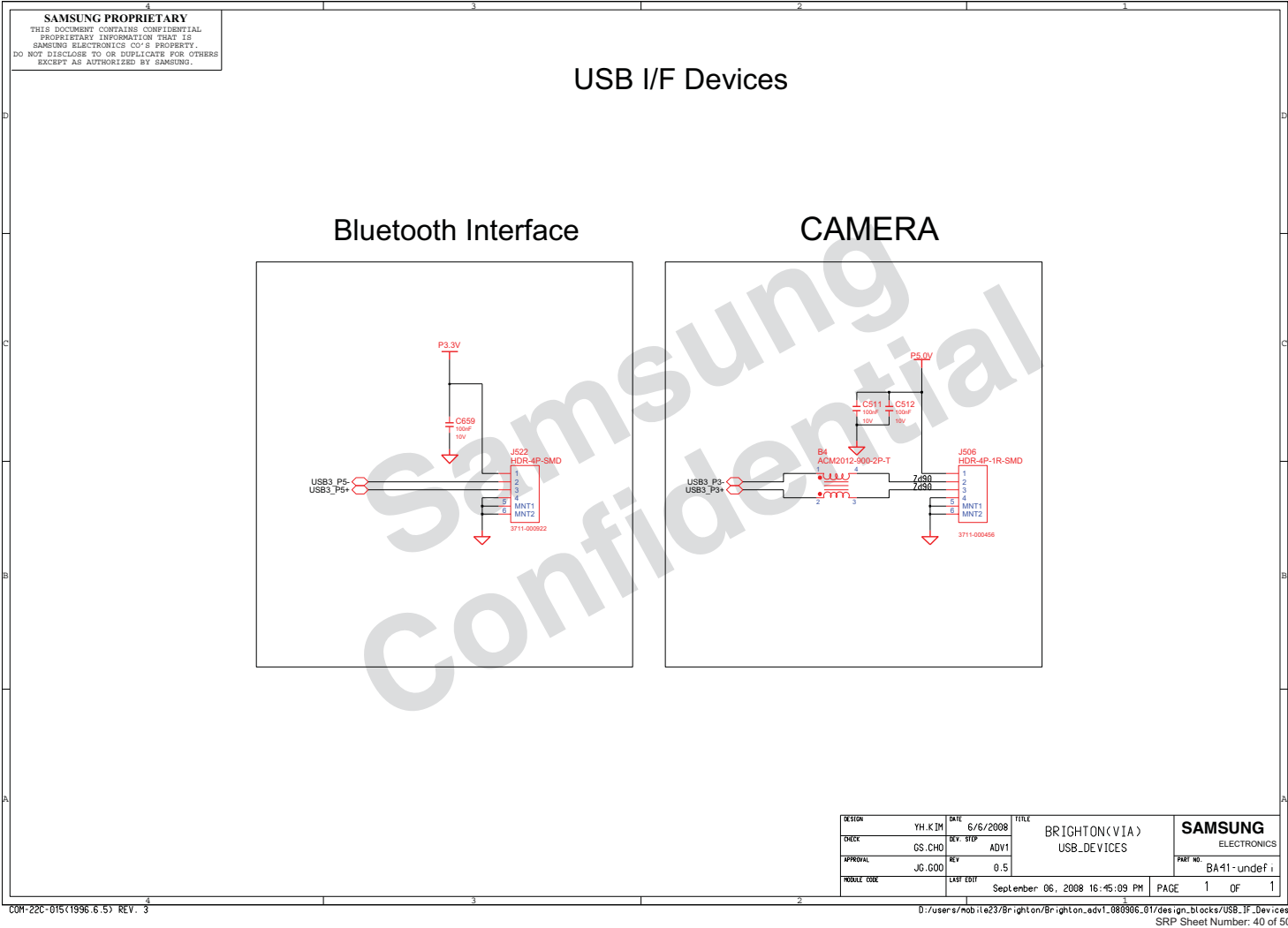
8. Block Diagram and Schematic





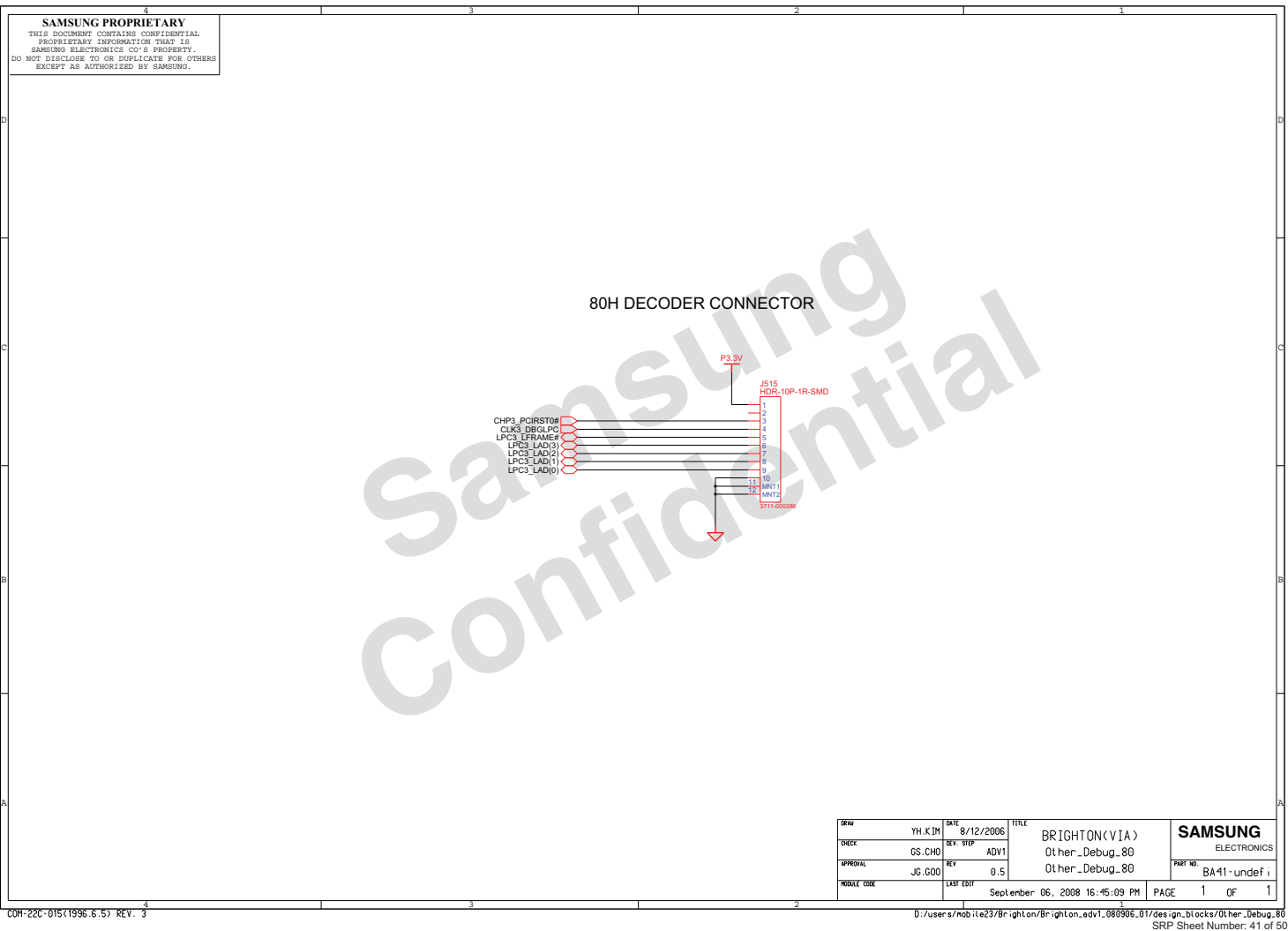
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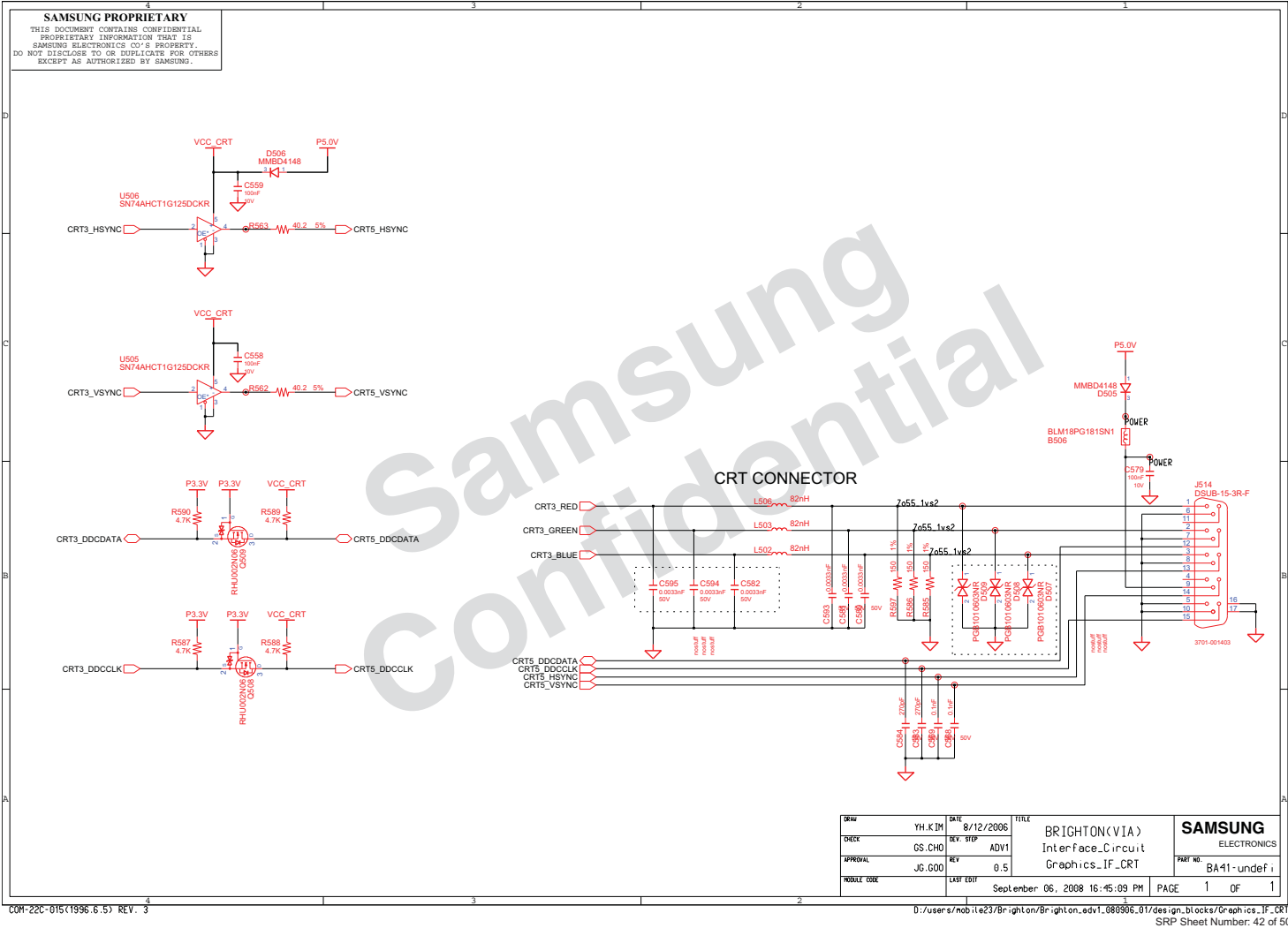


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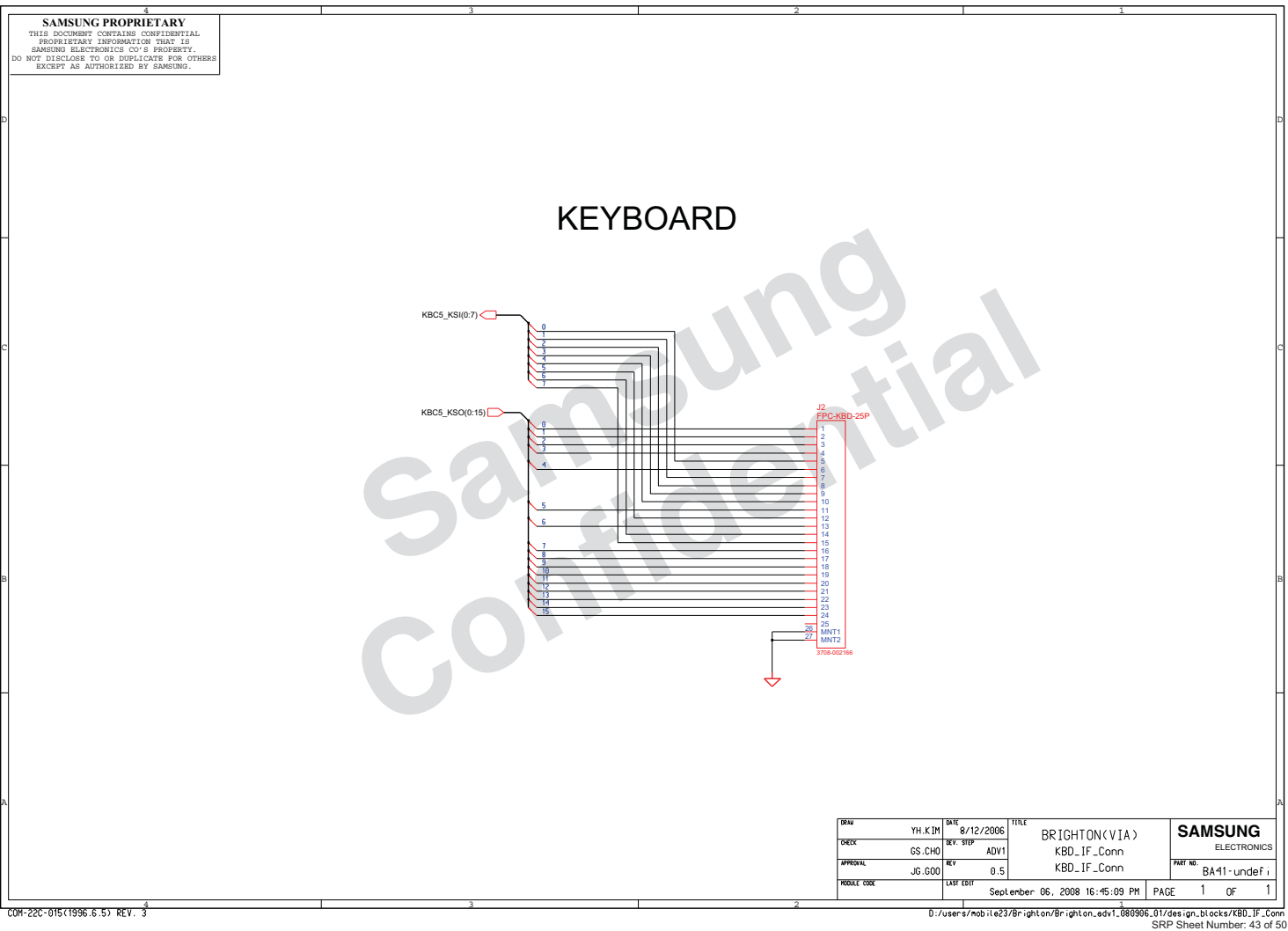


8. Block Diagram and Schematic



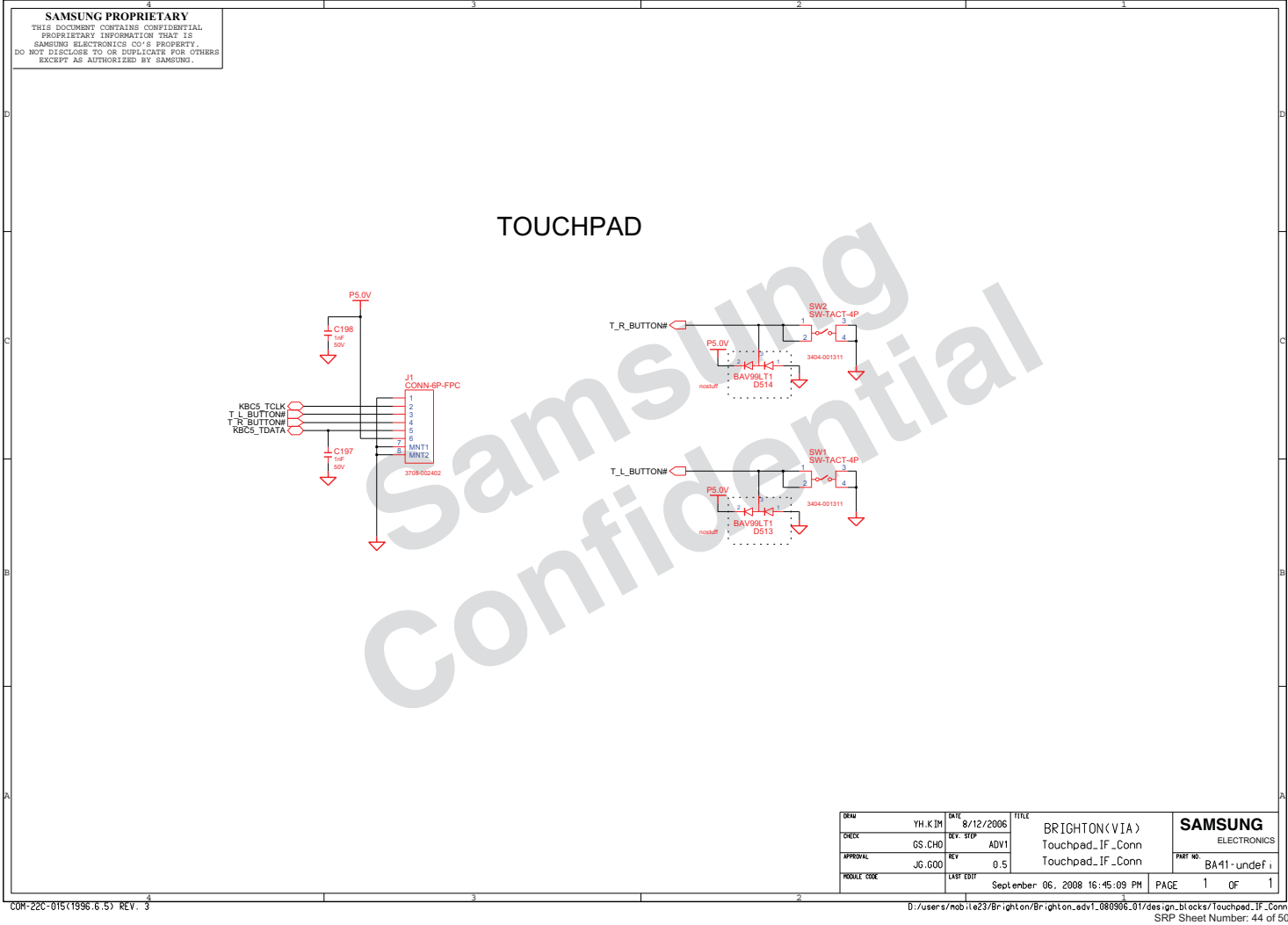
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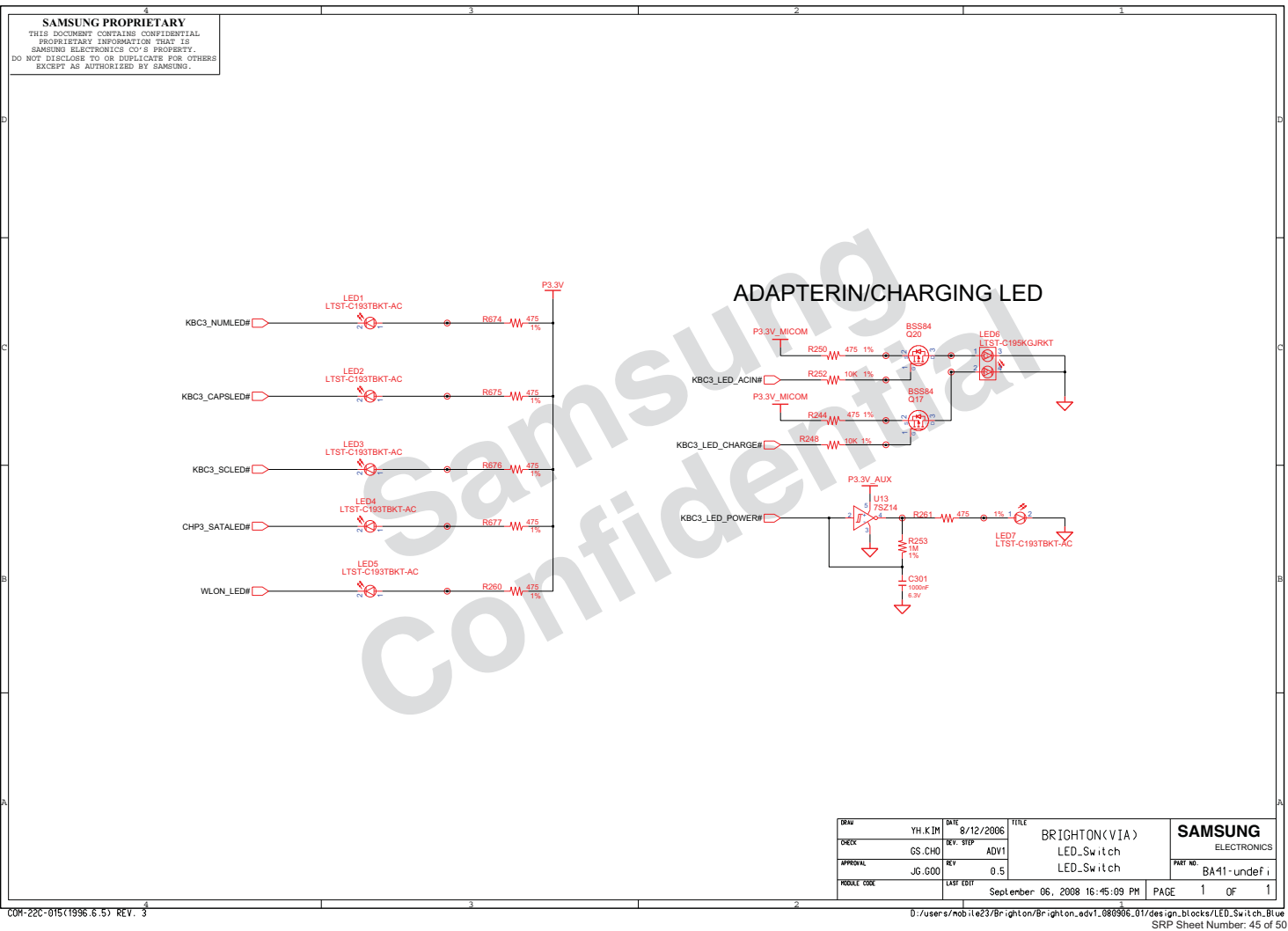


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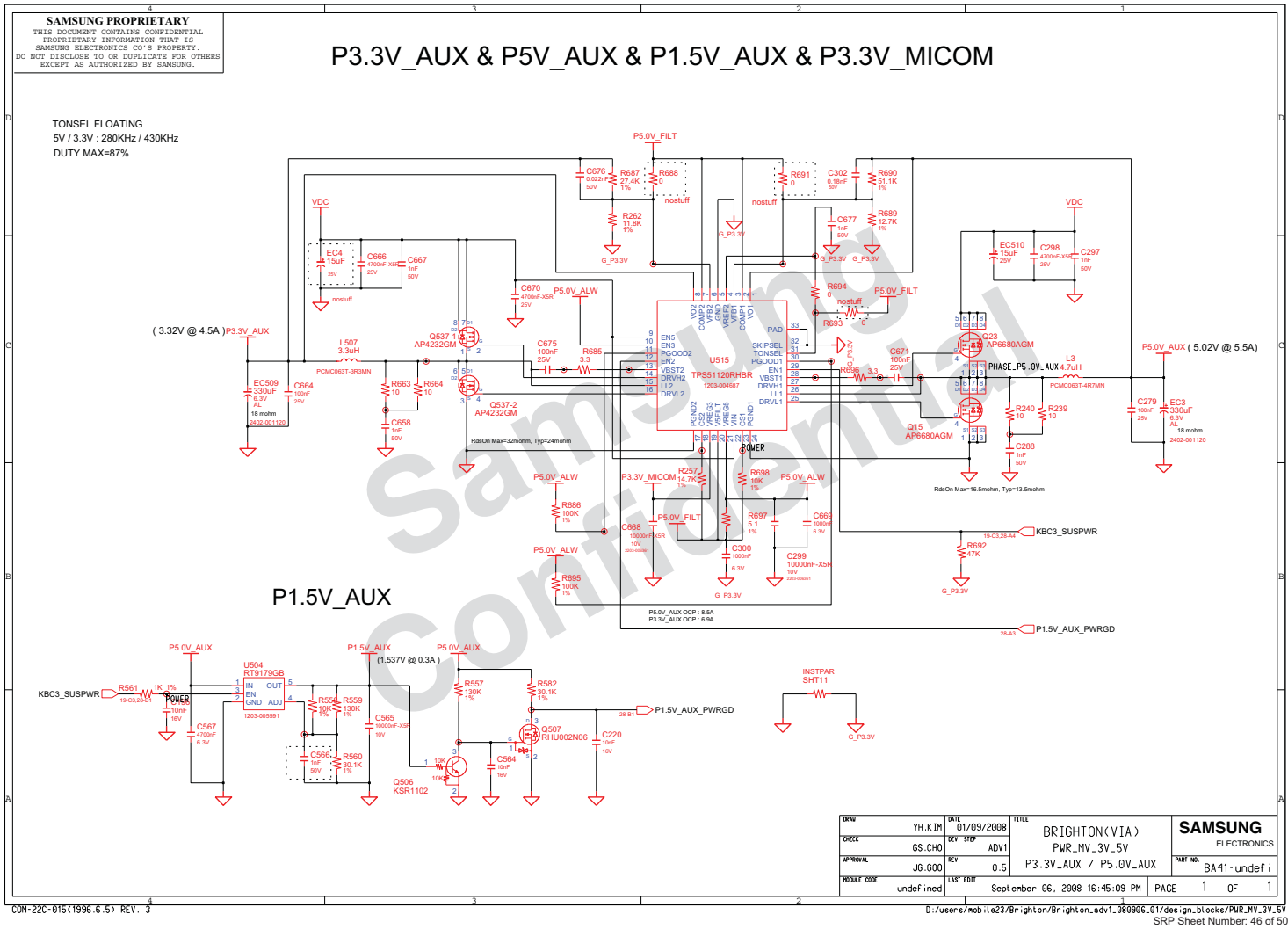
8. Block Diagram and Schematic



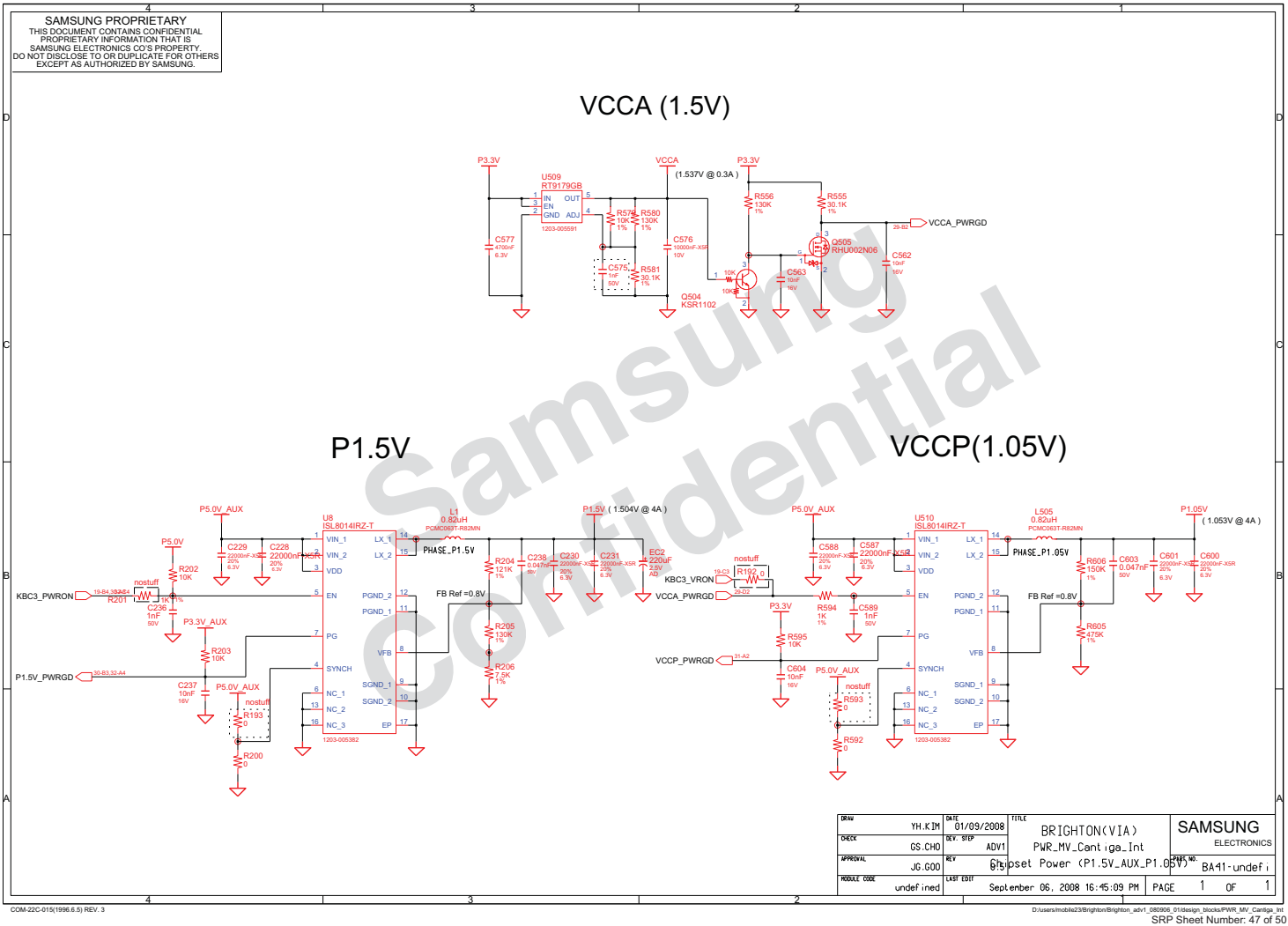
8. Block Diagram and Schematic



8. Block Diagram and Schematic

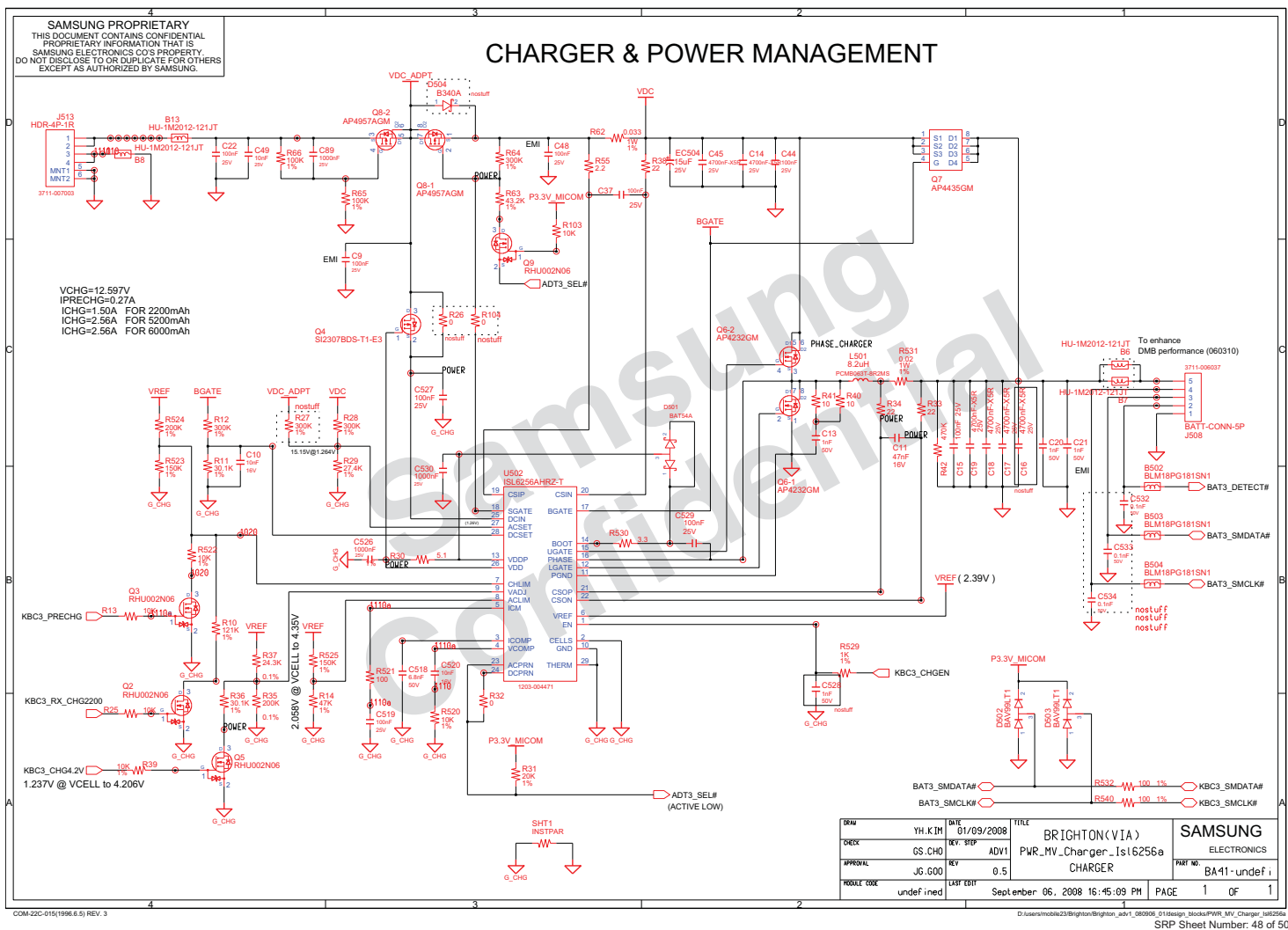


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