

MONACO-R

CPU : MEROM
Chip Set : ATI RS600ME & SB600
Remarks : DESKNOTE

Model Name : MONACO-R
PBA Name : MAIN
PCB Code : BA41-00720A
Dev. Step : PR
Revision : 1.1
T.R. Date : 2007.01.03

DRAW	CHECK	APPROVAL
SON, C.W	LEE, S.P	LIM, J.G

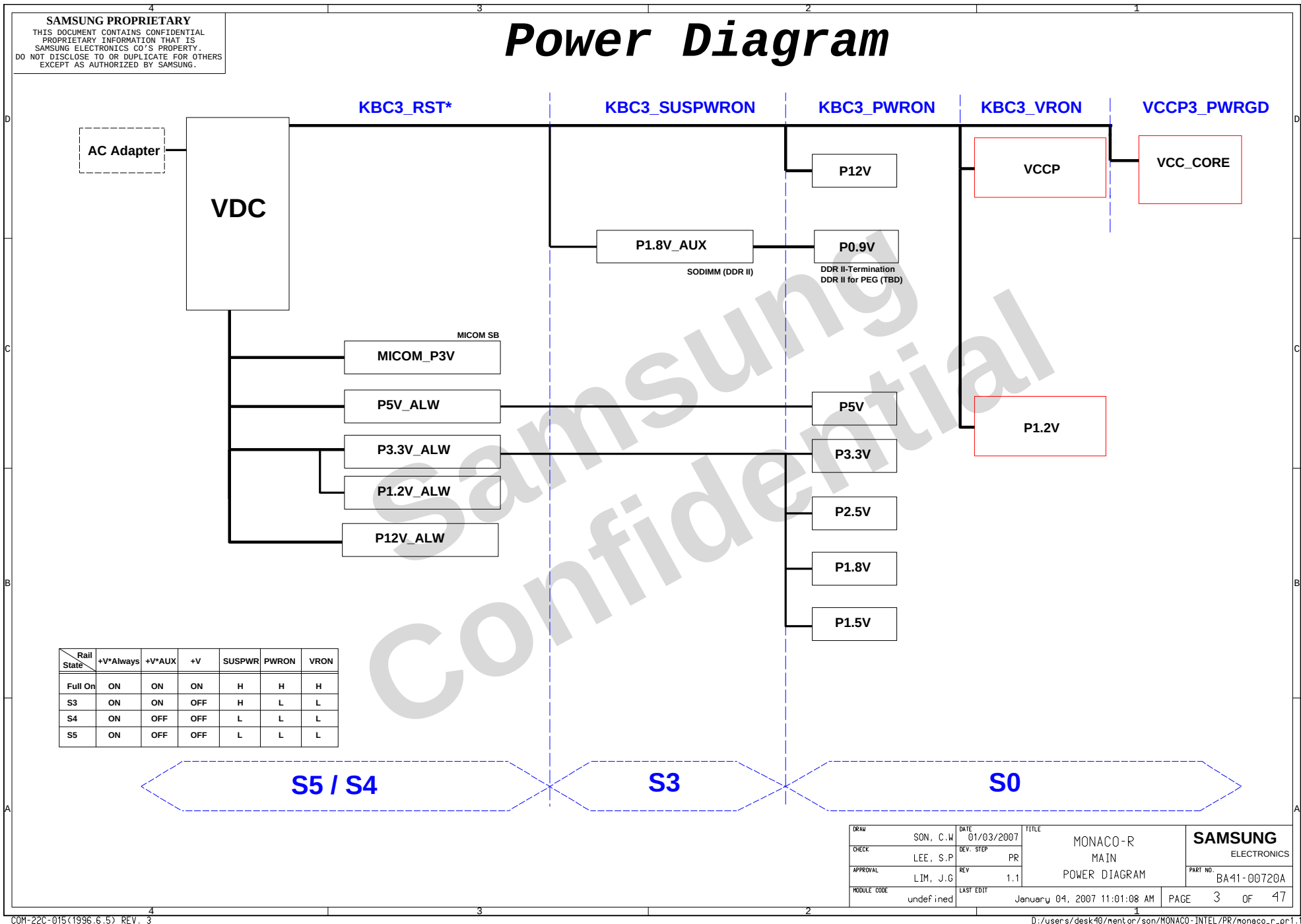
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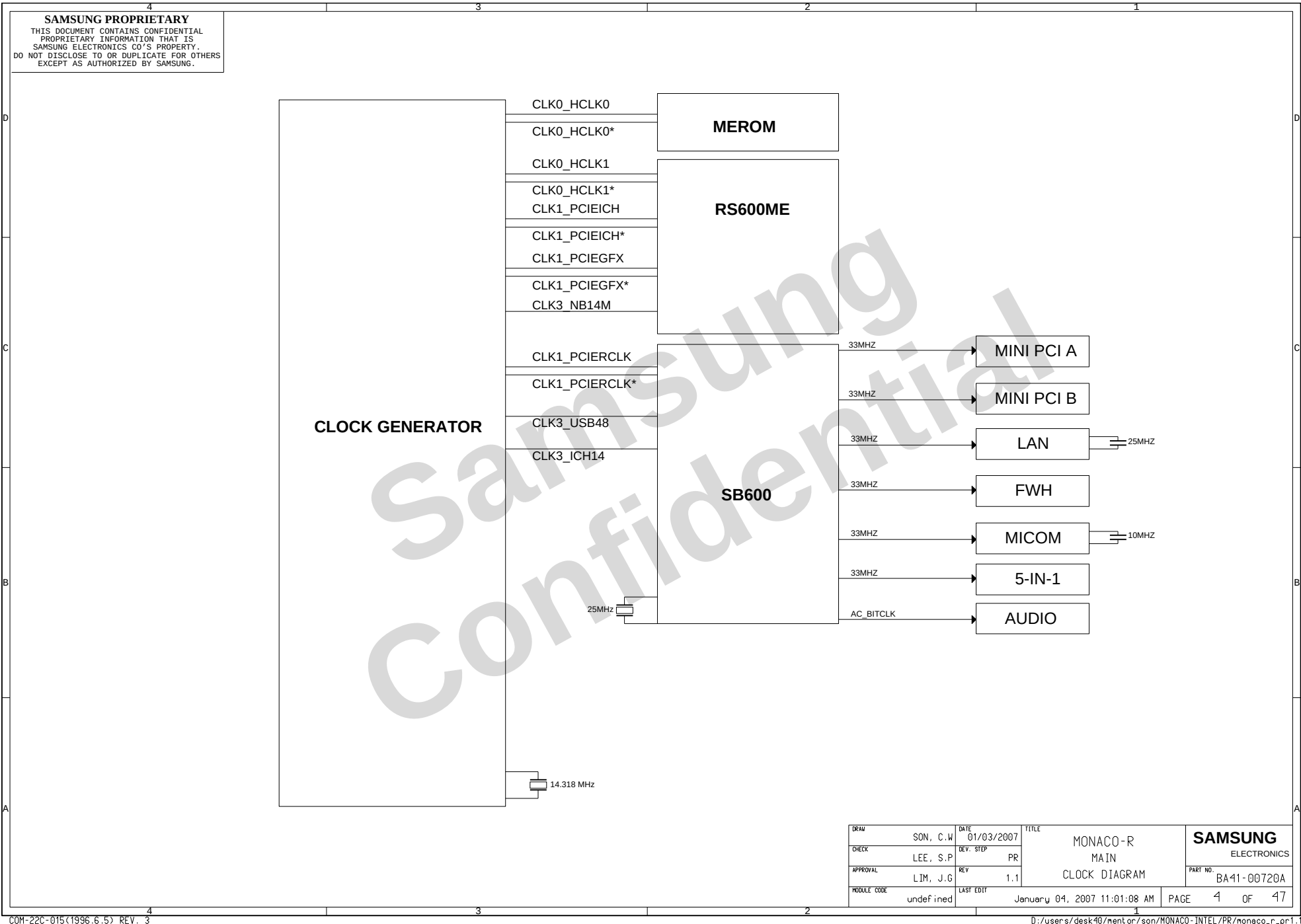
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CHECK	LEE, S.P	DEV. STEP	PR	MAIN		ELECTRONICS
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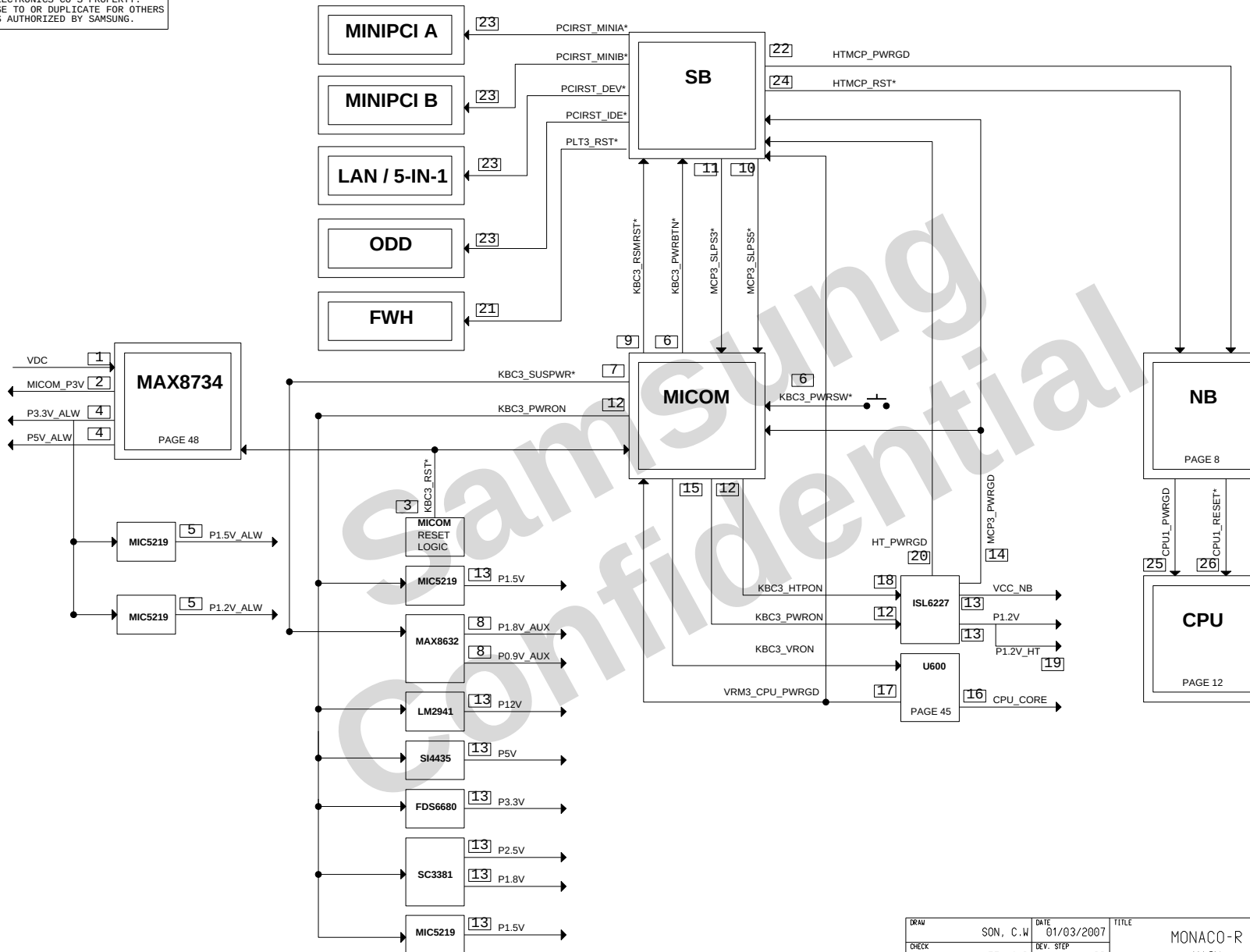
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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

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PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
MINIPCI A	AD21	0	A,B
MINIPCI B	AD22	1	C,D
LAN	AD23	2	D
5-IN-1	AD24	3	B
USB	AD30(internal)		
Hub to PCI	AD31(internal)		
LPC bridge/IDE/AC97/SMBUS	AD31(internal)		
Internal MAC	AD31(internal)		

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	25MHz	MCP51	MCP51 REF CLOCK
Crystal	32.768KHz	MCP51	Real Time Clock
Crystal	10MHz	MICOM	H8S-2110B
Crystal	27MHz	C51MV	TV OUT
Crystal	25MHz	LAN	RTL8110CL

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
CPU CORE	Core voltage for AMD SEMPRON (1.308~1.068V)
VCC_NB	SEMPRON Processor Hyper Transport (1.2V)
	North Bridge Core Voltage
P0.9V_AUX	0.9V switched power rail (off in S4-S5)
P1.2V	1.2V switched power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail(off in S4-S5)
P2.5V	2.5V switched power rail (off in S3-S5)
MICOM_P3V	3.3V always on power rail for MICOM
P3.3V	3.3V switched power rail (off in S3-S5)
P5V	5.0V switched power rail (off in S3-S5)
P5V_ALWS	5V power rail (Always On)
P3.3V_ALWS	3.3V power rail (Always On)
P1.5V_ALWS	1.5V power rail (Always On)

CPU Core Voltage Table

VID(5:0)	Voltage	VID(5:0)	Voltage
0 0 0 0 0 0	1.5500 V	1 0 0 0 0 0	0.7625 V
0 0 0 0 0 1	1.5250 V	1 0 0 0 0 1	0.7500 V
0 0 0 0 1 0	1.5000 V	1 0 0 0 1 0	0.7375 V
0 0 0 0 1 1	1.4750 V	1 0 0 0 1 1	0.7250 V
0 0 0 1 0 0	1.4500 V	1 0 0 1 0 0	0.7125 V
0 0 0 1 0 1	1.4250 V	1 0 0 1 0 1	0.7000 V
0 0 0 1 1 0	1.4000 V	1 0 0 1 1 0	0.6875 V
0 0 0 1 1 1	1.3750 V	1 0 0 1 1 1	0.6750 V
0 0 1 0 0 0	1.3500 V	1 0 1 0 0 0	0.6625 V
0 0 1 0 0 1	1.3250 V	1 0 1 0 0 1	0.6500 V
0 0 1 0 1 0	1.3000 V	1 0 1 0 1 0	0.6375 V
0 0 1 0 1 1	1.2750 V	1 0 1 0 1 1	0.6250 V
0 0 1 1 0 0	1.2500 V	1 0 1 1 0 0	0.6125 V
0 0 1 1 0 1	1.2250 V	1 0 1 1 0 1	0.6000 V
0 0 1 1 1 0	1.2000 V	1 0 1 1 1 0	0.5875 V
0 0 1 1 1 1	1.1750 V	1 0 1 1 1 1	0.5750 V
0 1 0 0 0 0	1.1500 V	1 1 0 0 0 0	0.5625 V
0 1 0 0 0 1	1.1250 V	1 1 0 0 0 1	0.5500 V
0 1 0 0 1 0	1.1000 V	1 1 0 0 1 0	0.5375 V
0 1 0 0 1 1	1.0750 V	1 1 0 0 1 1	0.5250 V
0 1 0 1 0 0	1.0500 V	1 1 0 1 0 0	0.5125 V
0 1 0 1 0 1	1.0250 V	1 1 0 1 0 1	0.5000 V
0 1 0 1 1 0	1.0000 V	1 1 0 1 1 0	0.4875 V
0 1 0 1 1 1	0.9750 V	1 1 0 1 1 1	0.4750 V
0 1 1 0 0 0	0.9500 V	1 1 1 0 0 0	0.4625 V
0 1 1 0 0 1	0.9250 V	1 1 1 0 0 1	0.4500 V
0 1 1 0 1 0	0.9000 V	1 1 1 0 1 0	0.4375 V
0 1 1 0 1 1	0.8750 V	1 1 1 0 1 1	0.4250 V
0 1 1 1 0 0	0.8500 V	1 1 1 1 0 0	0.4125 V
0 1 1 1 0 1	0.8250 V	1 1 1 1 0 1	0.4000 V
0 1 1 1 1 0	0.8000 V	1 1 1 1 1 0	0.3875 V
0 1 1 1 1 1	0.7750 V	1 1 1 1 1 1	0.3750 V

2

I C / SMB Address

Devices	Address	Hex	Bus
SB600	Master	-	SMBUS Master
W83L786NG(CPU Thermal Sensor)	1001 110X	9Ch	Thermal Sensor

USB PORT Assign

PORT NUMBER	ASSIGNED TO
0	SYSTEM PORT A
2, 3	SYSTEM PORT B
4, 5	SYSTEM PORT C
6	DMB

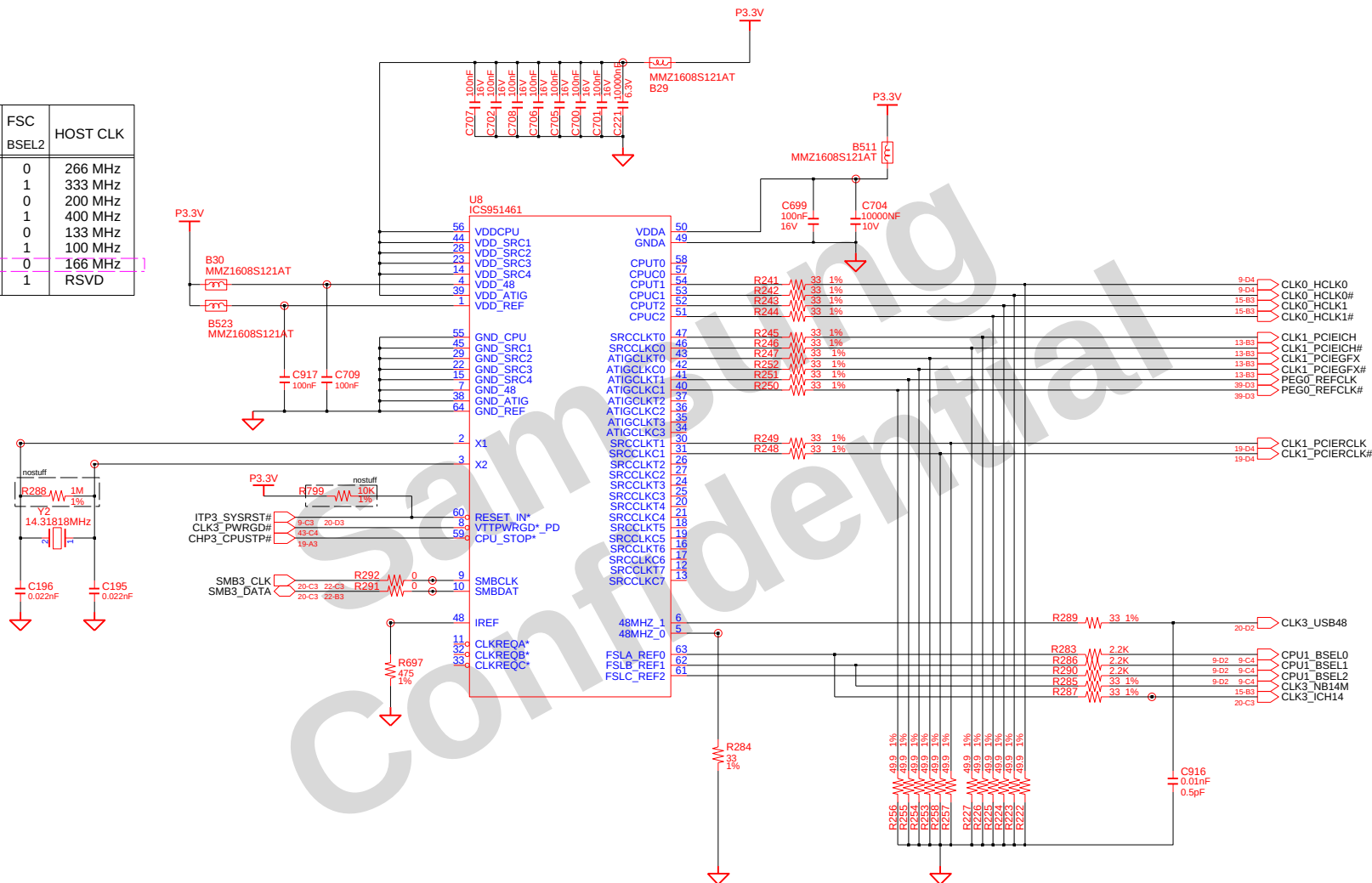
System Power States

- CHP3_SLP1S* S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped. The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other critical subsystems. Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.
- CHP3_SLP3S* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits. Memory is retained, and refreshes continue. All clocks stop except RTC clock.
- CHP3_SLP4S* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume. Externally appears same as S5, but may have different wake events.
- CHP3_SLP5S* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

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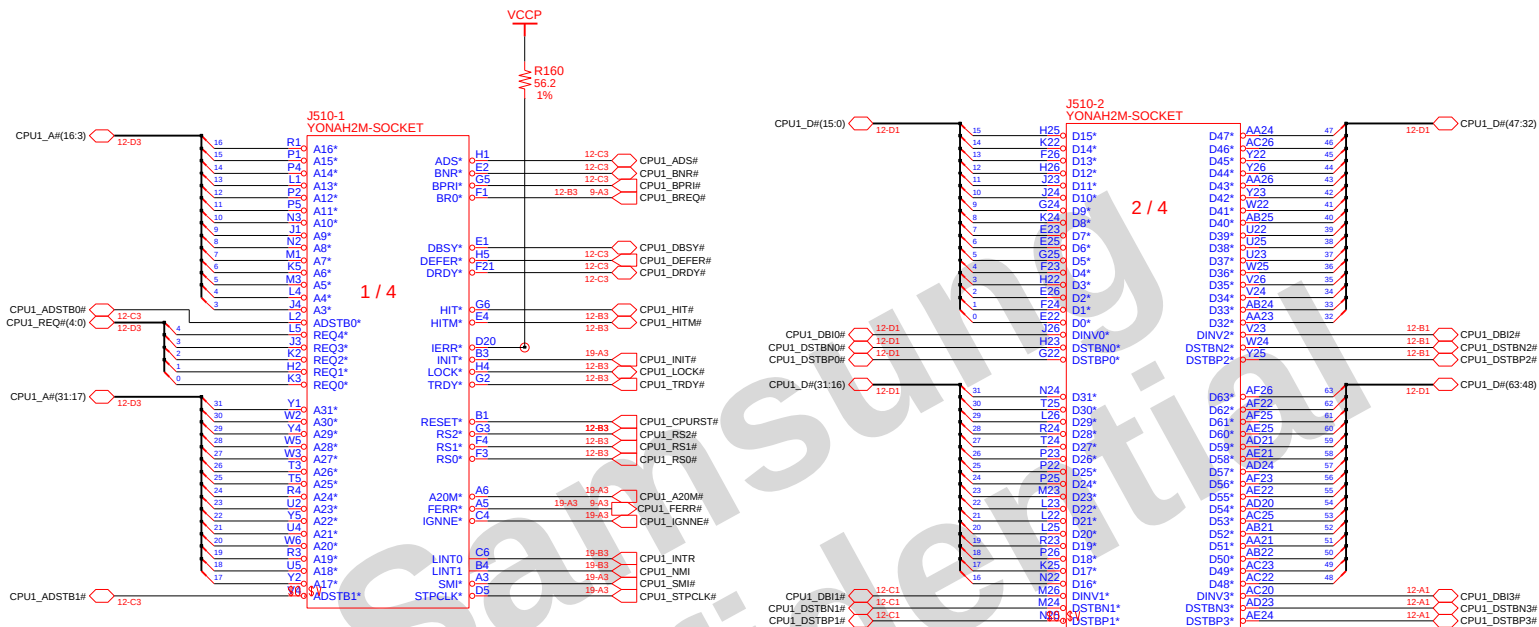
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	FSA BSEL0	FSB BSEL1	FSC BSEL2	HOST CLK
<i>CPU</i>	0	0	0	266 MHz
	0	0	1	333 MHz
	0	1	0	200 MHz
	0	1	1	400 MHz
	1	0	0	133 MHz
	1	0	1	100 MHz
	1	1	0	166 MHz
	1	1	1	RSVD

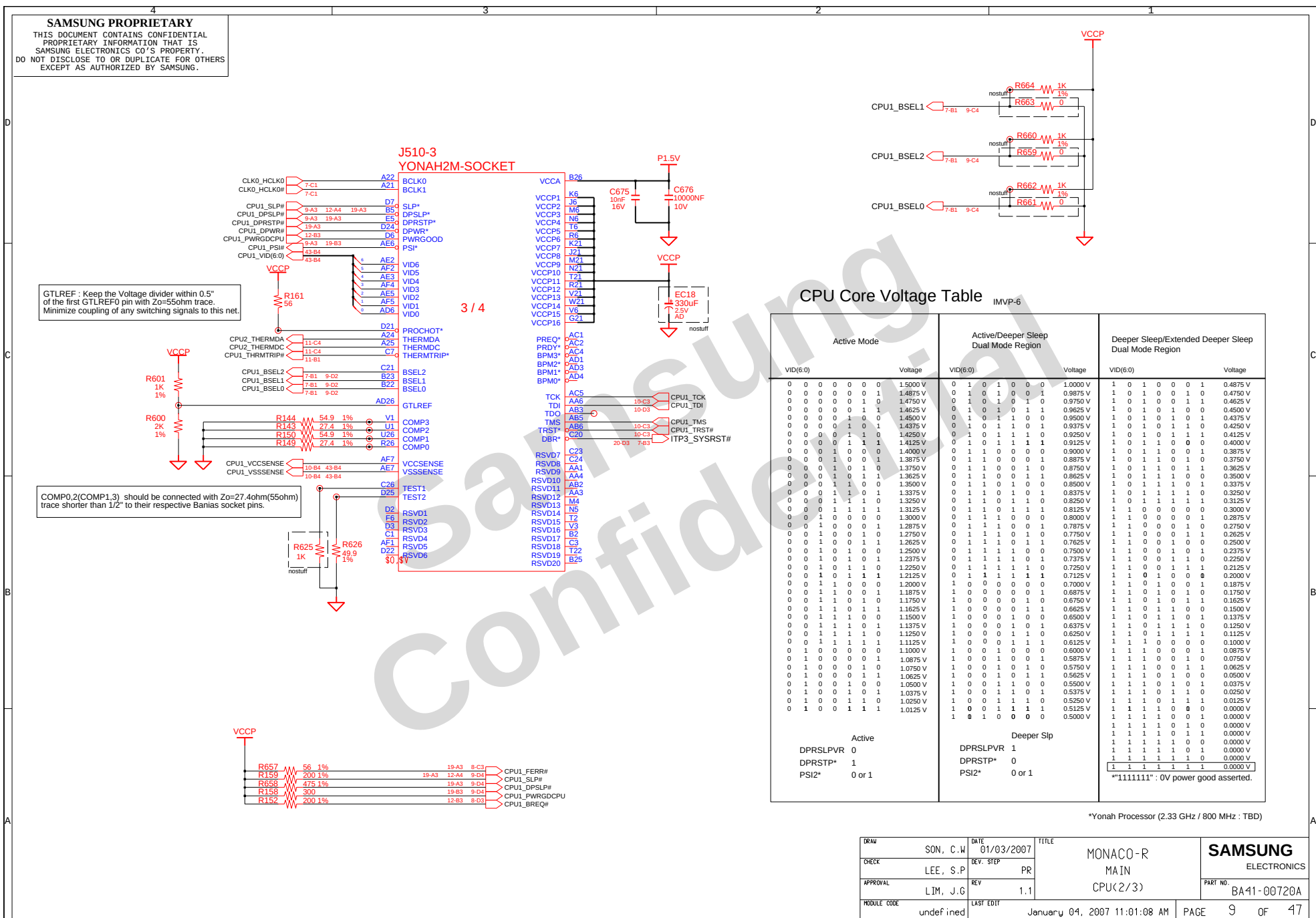


DATE	01/03/2007	MONACO-R MAIN CLOCK GENERATOR		SAMSUNG ELECTRONICS PART NO. BA41-00720A	
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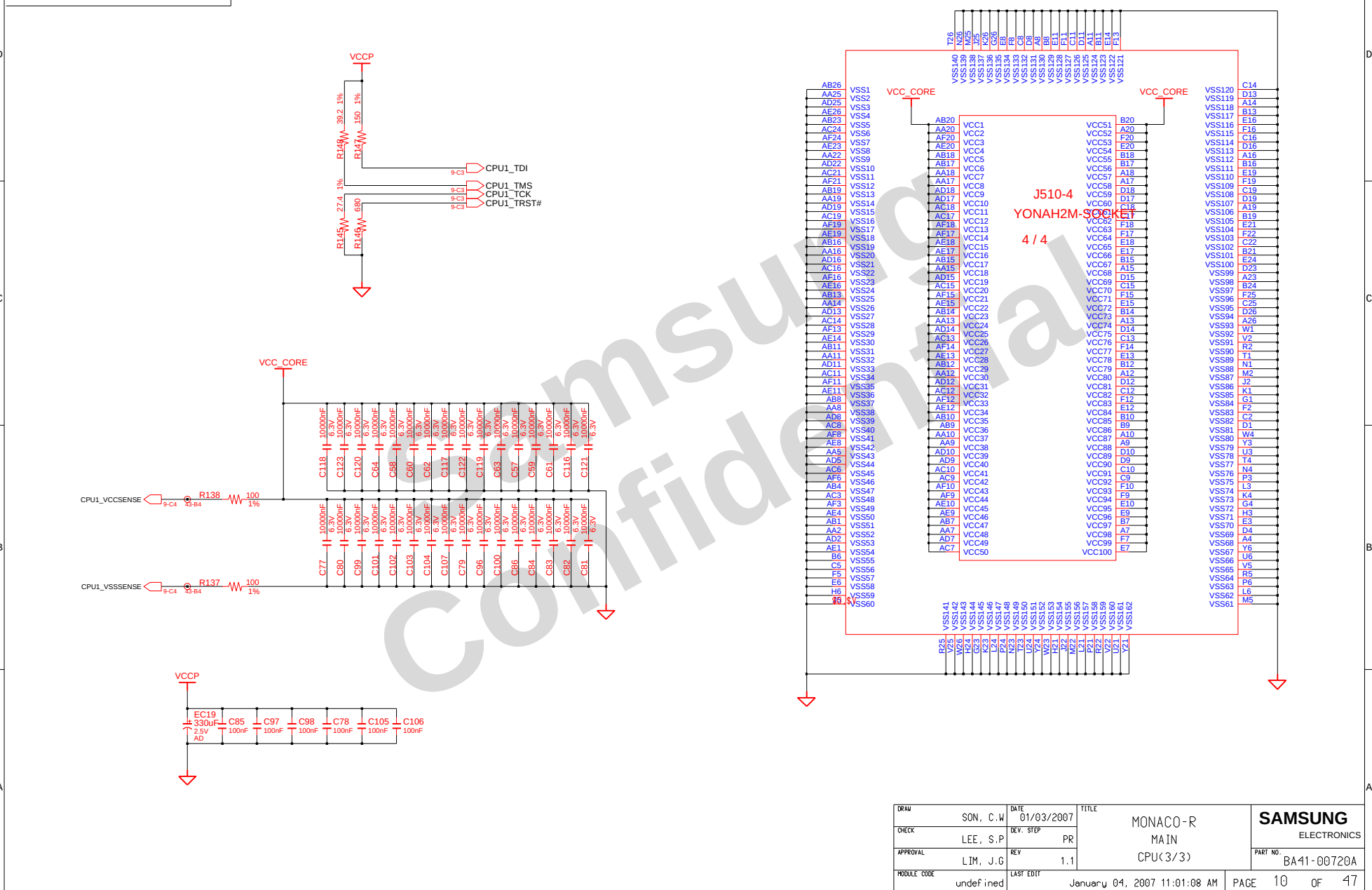
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CPU/MEMORY Thermal Sensor

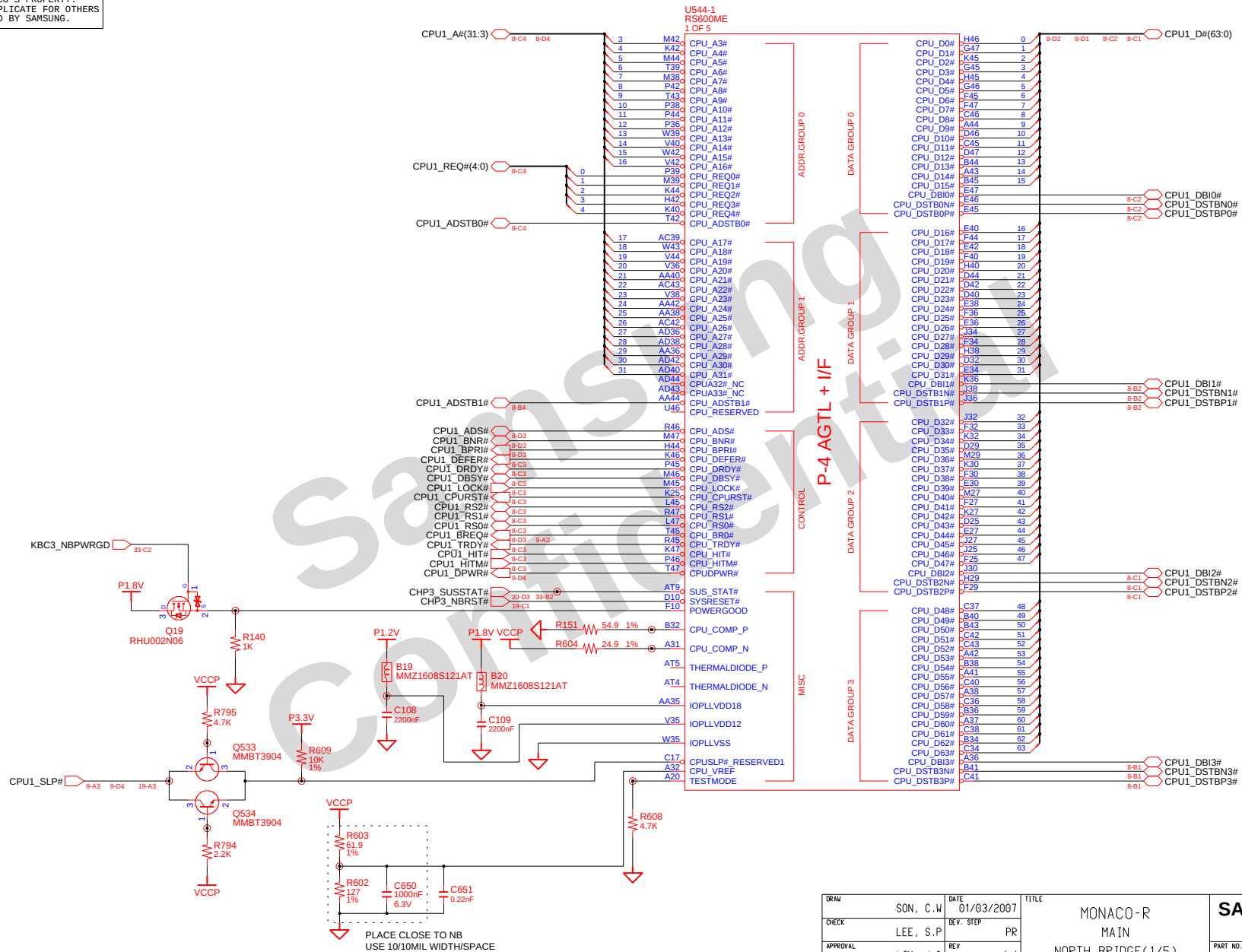
EXT

FAN CONTROL

FAN&RHE PEM

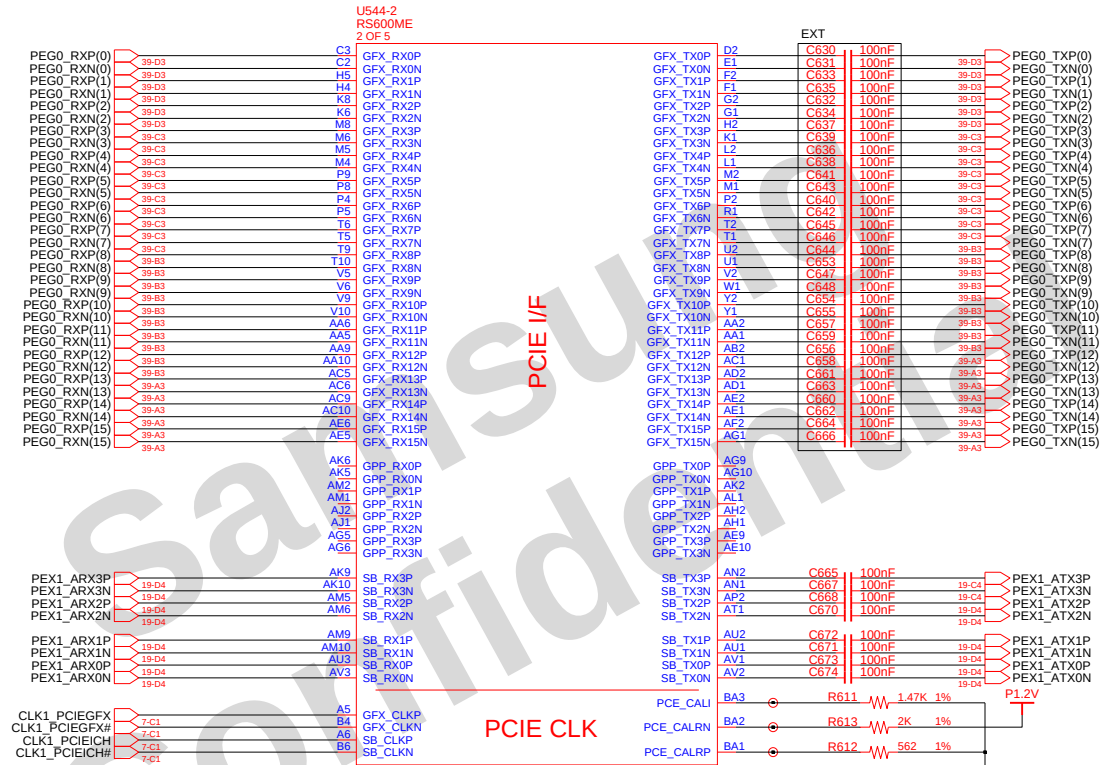
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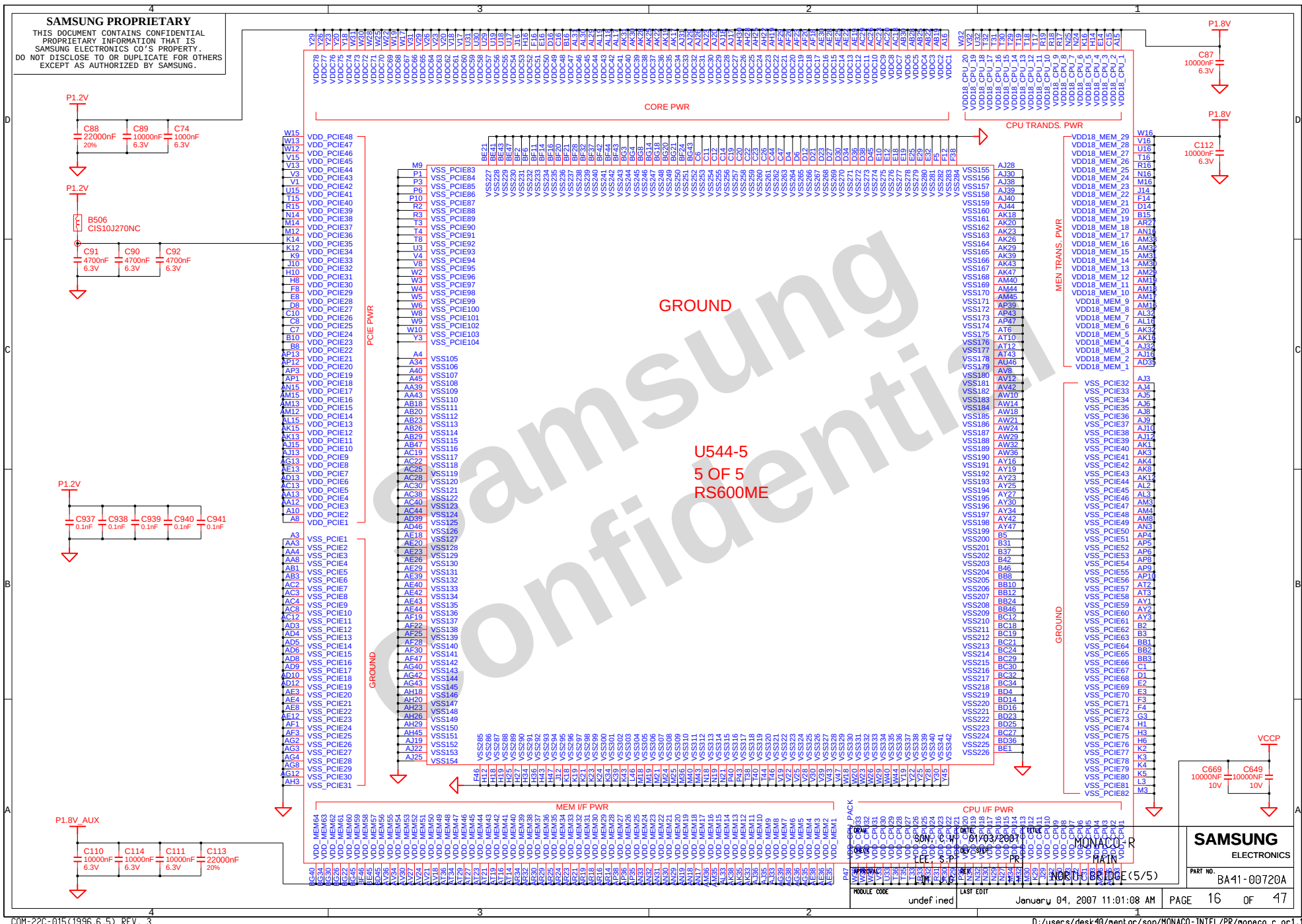
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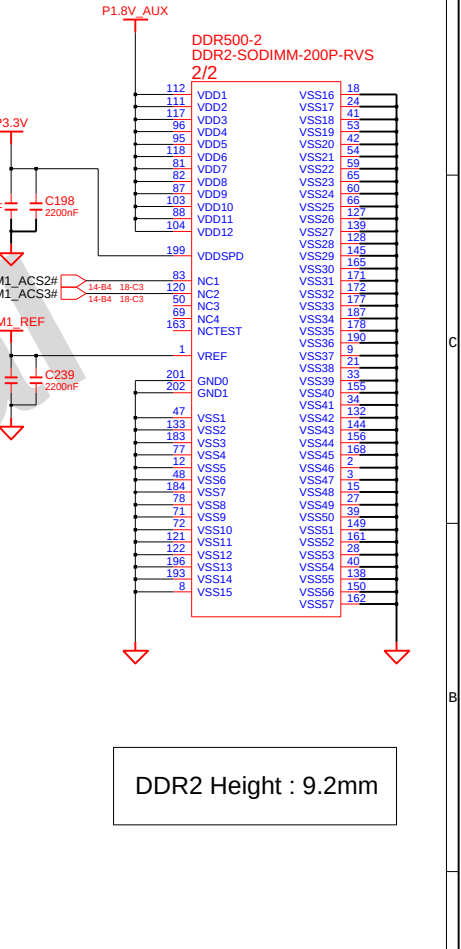
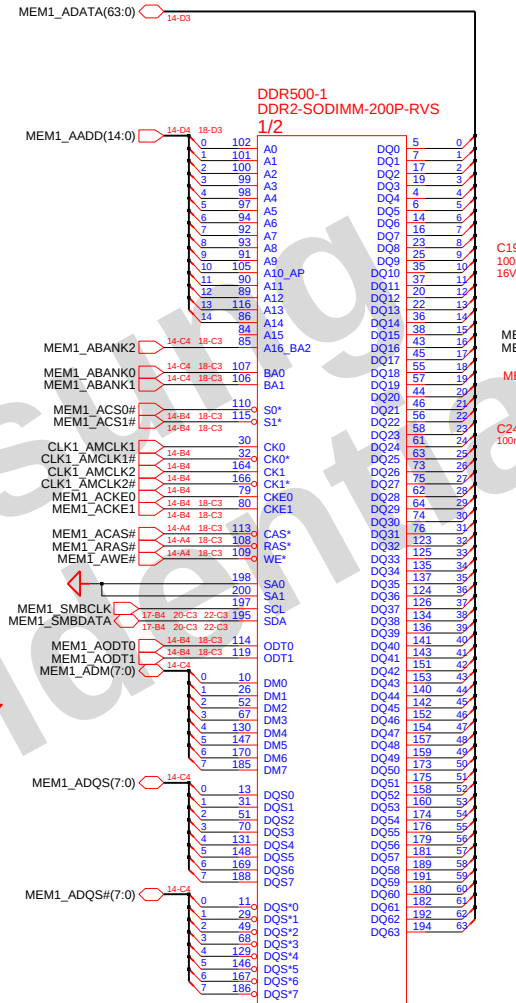
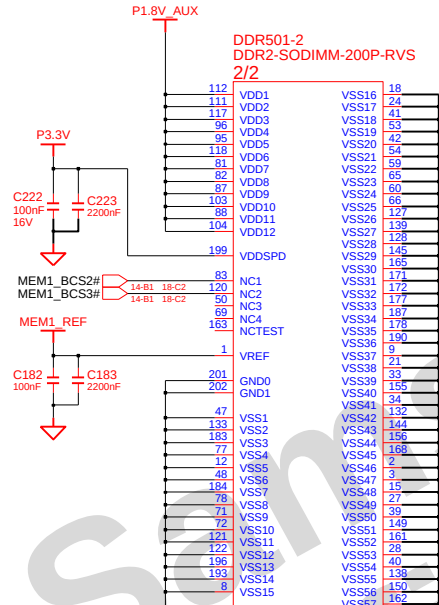
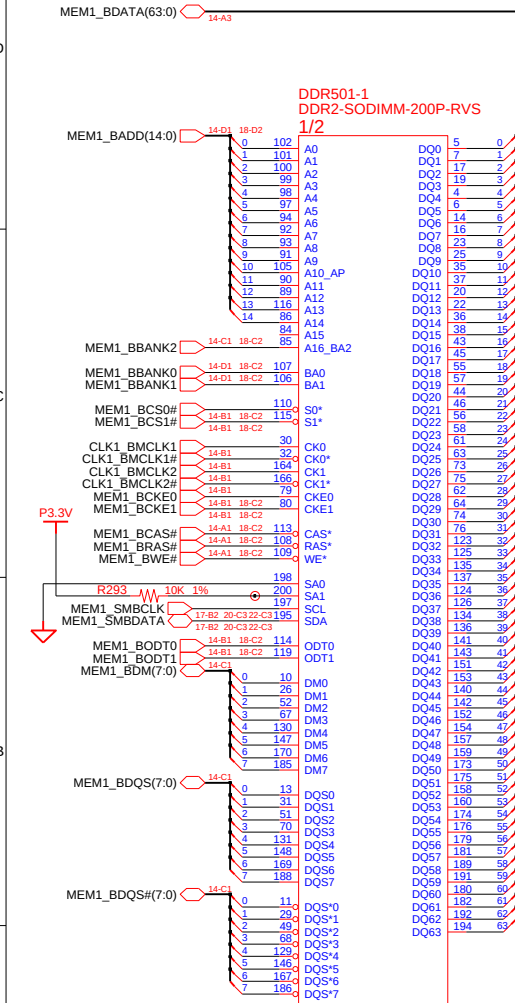
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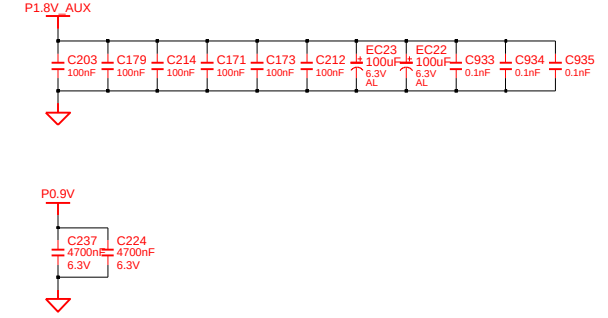
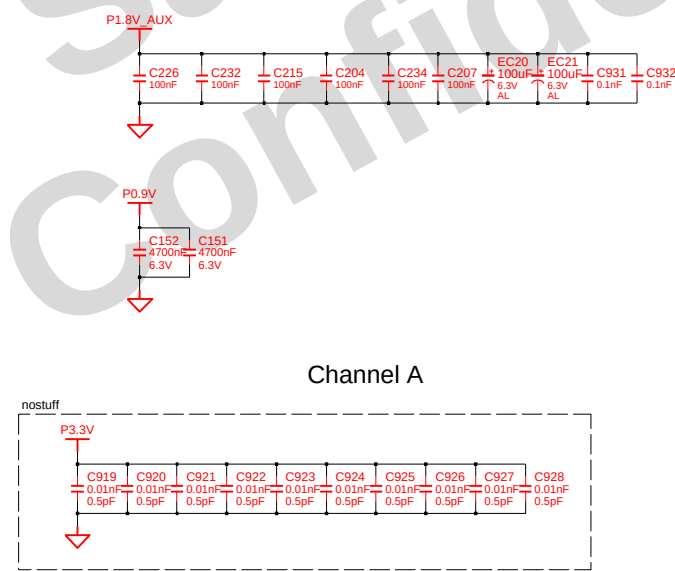
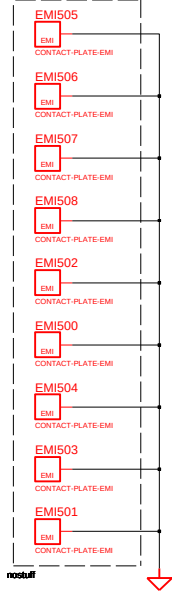
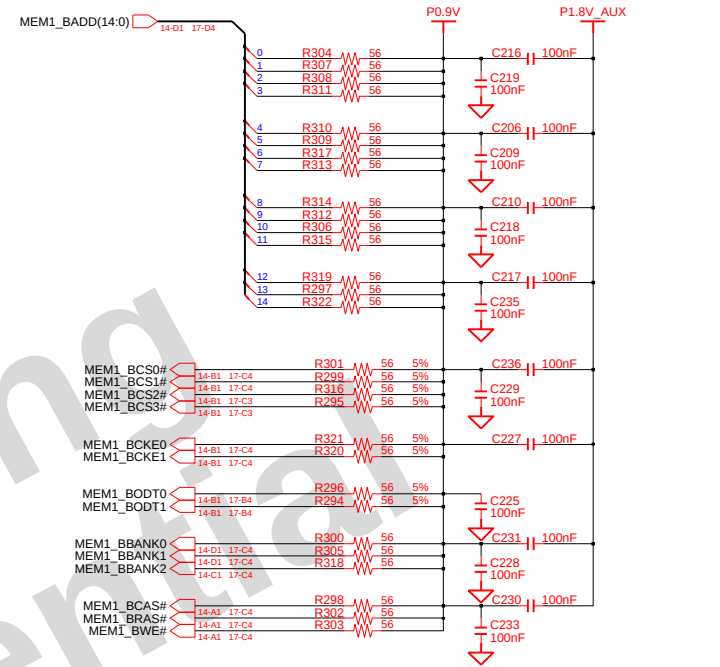
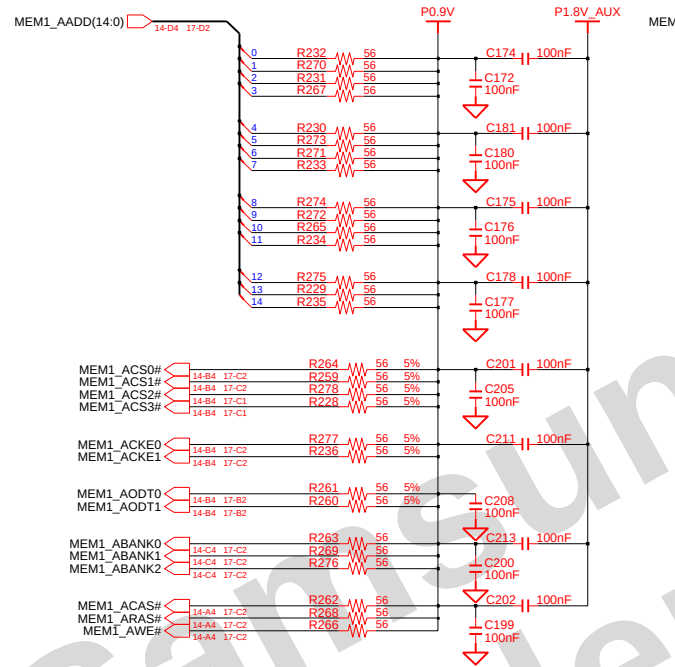


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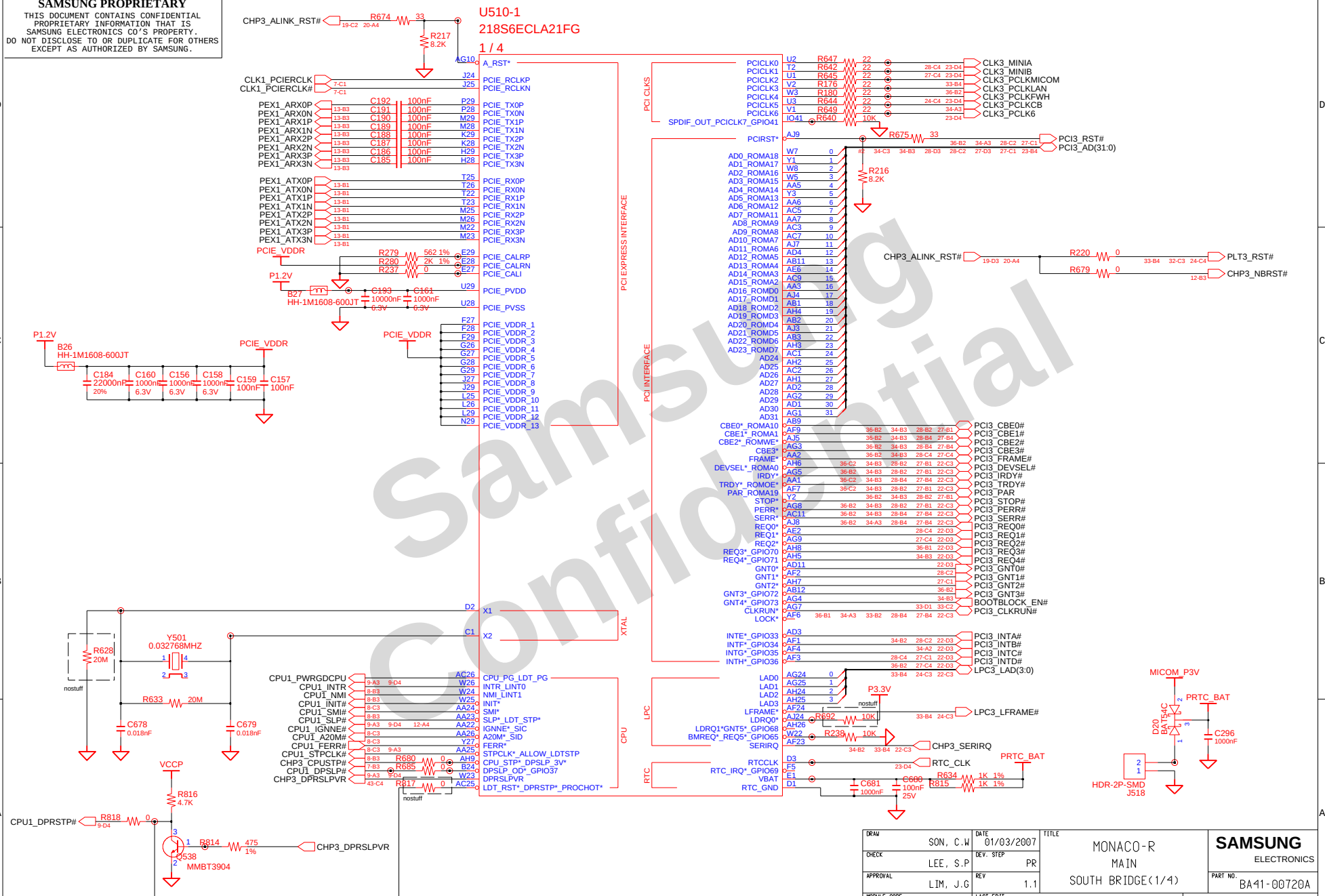
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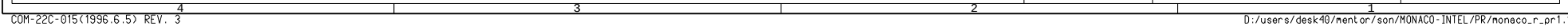


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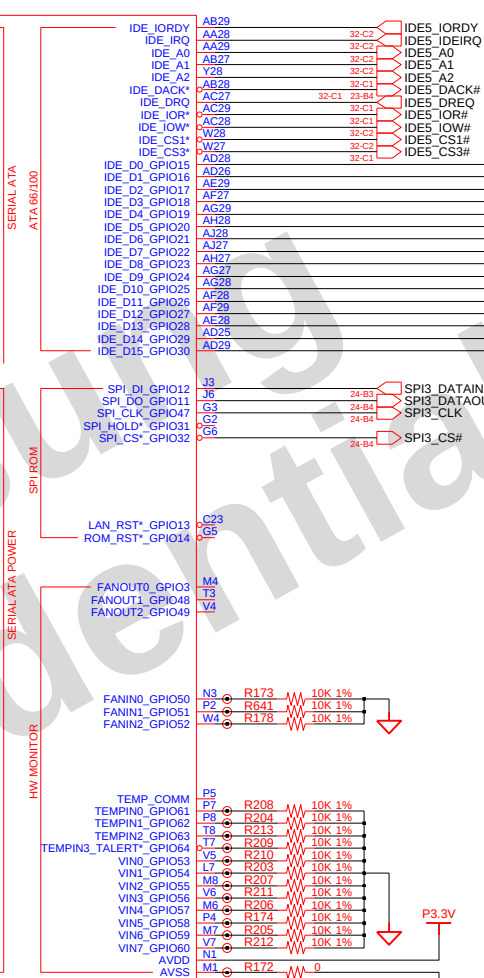
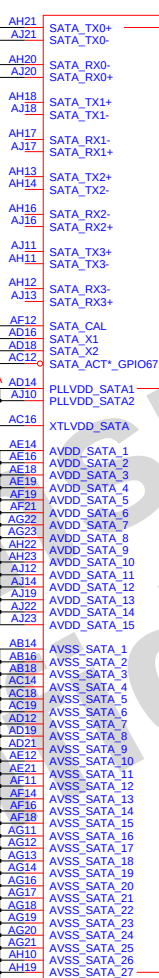
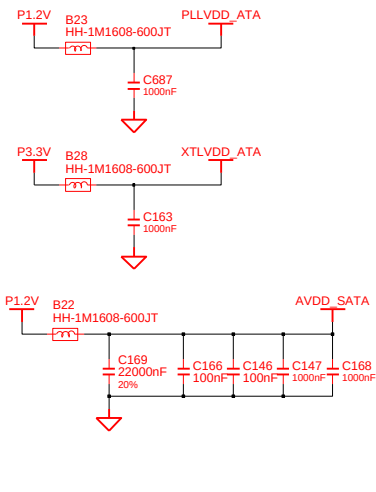
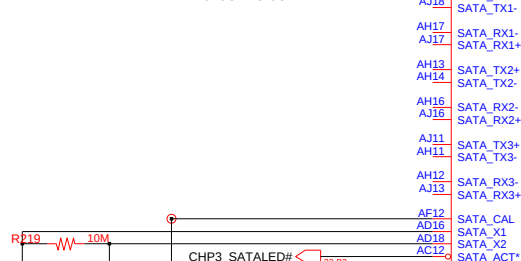
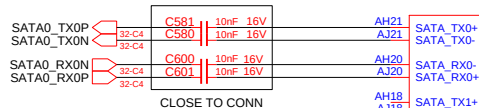


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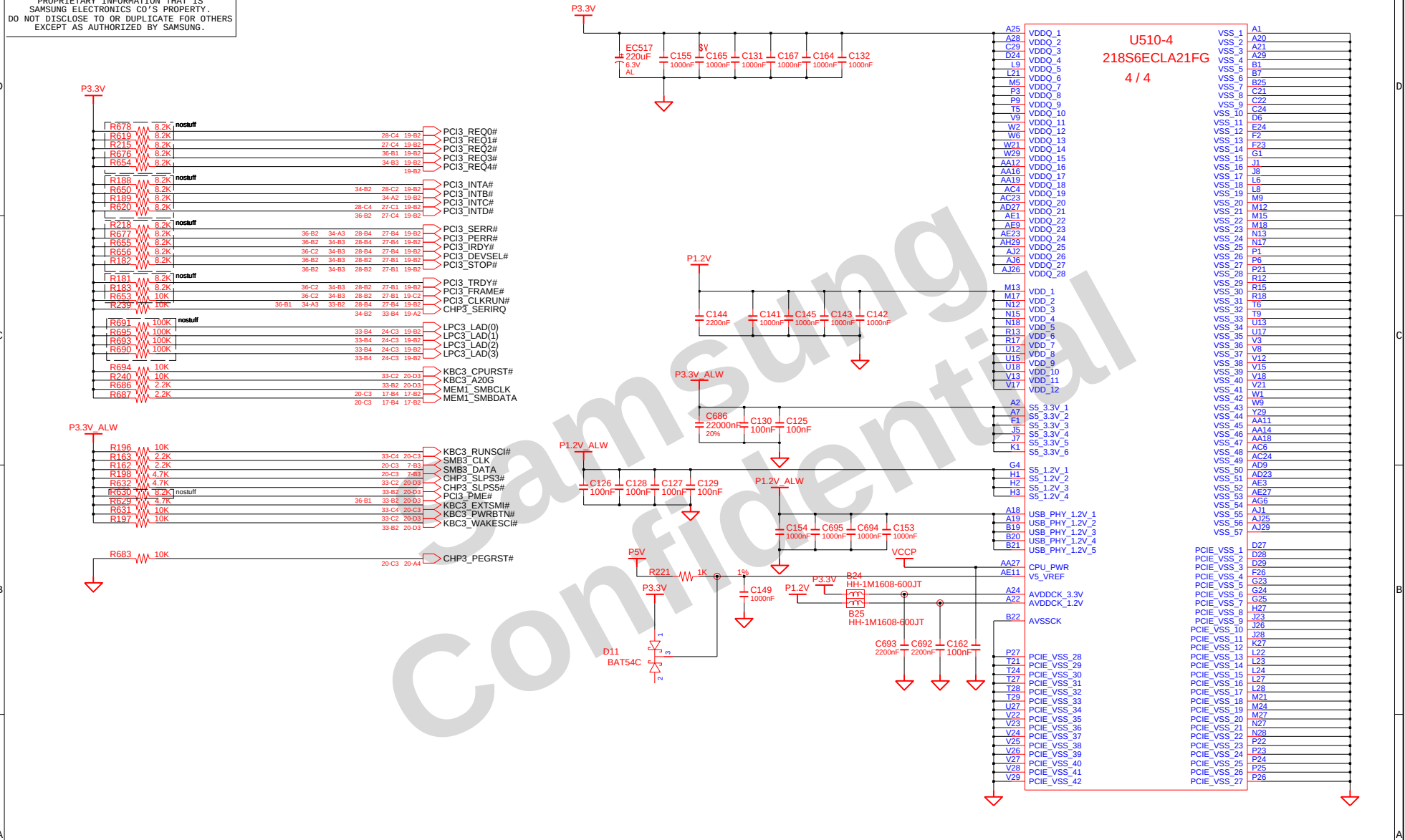
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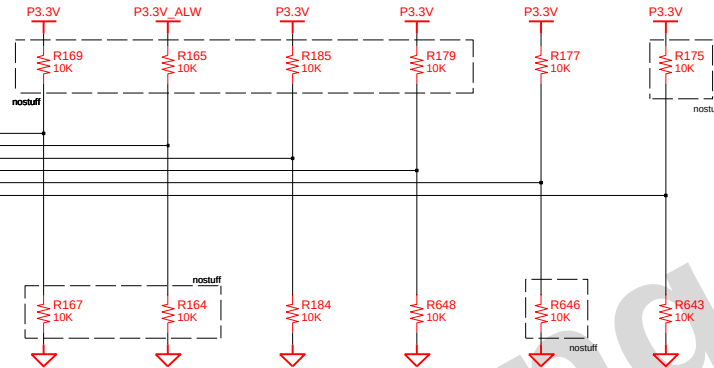


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REQUIRED SYSTE STRAPS

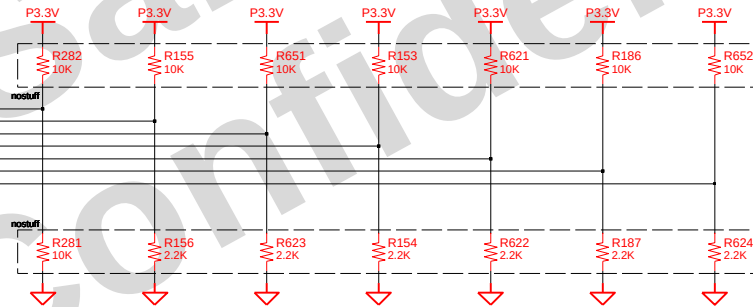
AC_SDOUT 20-B3
RTC_CLK 19-A2
CLK3_PCLKFWH 19-D2 24-C4
CLK3_PCLK6 19-D2
CLK3_MINIA 19-D2 28-C4
CLK3_MINIB 19-D2 27-C4



	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF = K8	ROM TYPE: H,H = PCI ROM H,H = SPI ROM L,H = LPC ROM L,L = FWH ROM	DEFAULT
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXT.RTC	USE EXT. 48MHz DEFAULT	CPU IF = P4		

DEBUS STRAPS

IDE5_DACK# 21-D2 32-C1
PCI3_AD(28) 19-D1 27-D3 28-D3 34-C3 36-C4
PCI3_AD(27) 19-D1 27-D3 28-D3 34-C3 36-C4
PCI3_AD(26) 19-D1 27-D3 28-D3 34-C3 36-C4
PCI3_AD(25) 19-D1 27-D3 28-D3 34-C3 36-C4
PCI3_AD(24) 19-D1 27-D3 28-D3 34-B3 34-C3 36-C4
PCI3_AD(23) 19-D1 27-D3 28-D3 34-C3 36-B1 36-C4



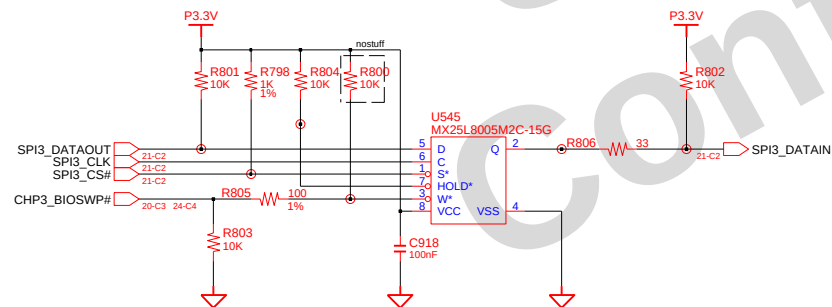
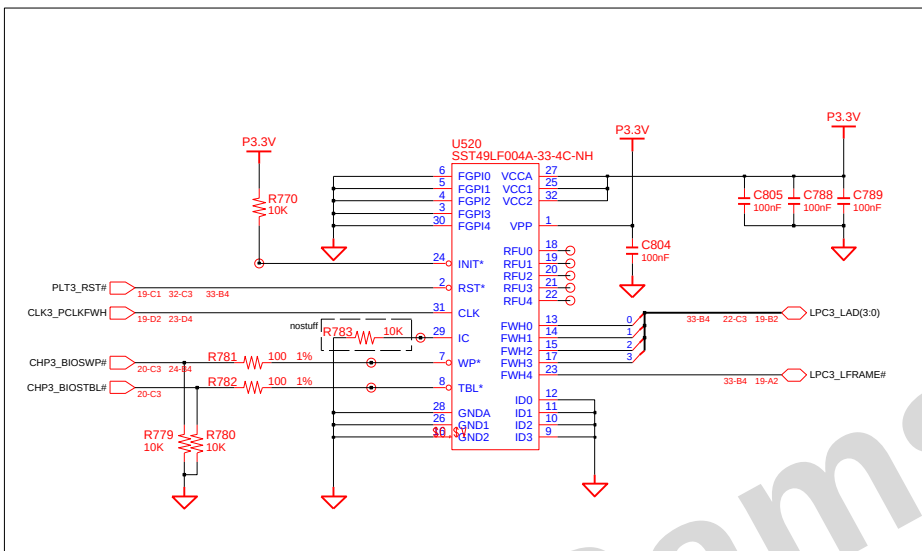
	IDE5_DACK*	PCI3_AD(28)	PCI3_AD(27)	PCI3_AD(26)	PCI3_AD(25)	PCI3_AD(24)	PCI3_AD(23)
STRAP HIGH	USE LONG RESET DEFAULT	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOTFAIL TIMER DISABLED DEFAULT
STRAP LOW	USE SHORT RESET	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	BYPASS EEPROM PCIE STRAPS	BOOTFAIL TIMER ENABLED

DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R MAIN STRAPS OPTION	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	PR			PART NO. BA41-00720A
APPROVAL	LIM, J.G	REV	1.1			
MODULE CODE	undefined	LAST EDIT	January 04, 2007 11:01:08 AM	PAGE	23	OF 47

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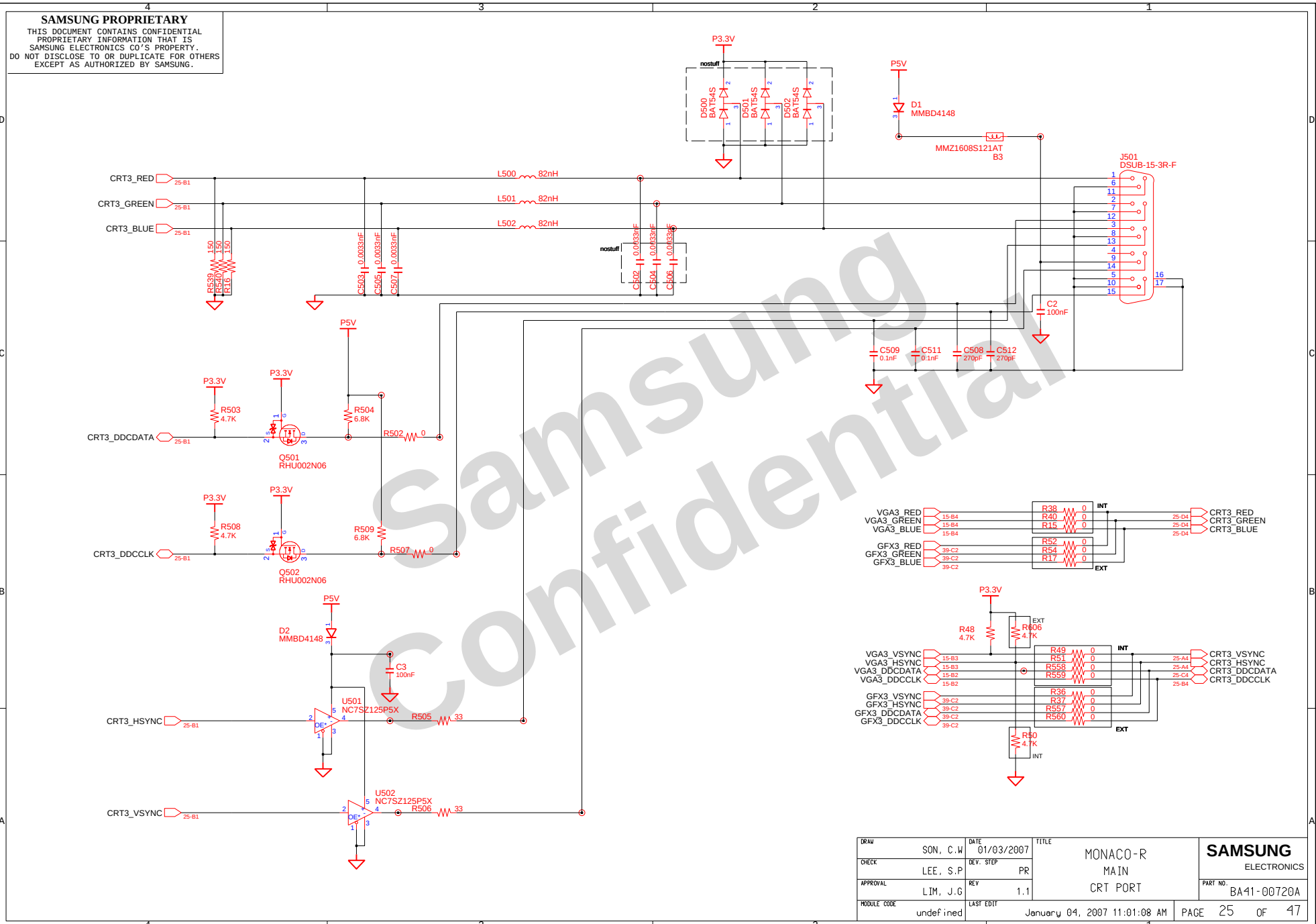
nostuff



- | | |
|---|--|
| 02 VERIFY REAL MODE | 66 CONFIGURE ADVANCE CACHE REGISTERS |
| 03 DISABLE NMI | 6A DISPLAY EXTERNAL CACHE SIZE |
| 04 GET CPU TYPE | 6C DISPLAY SHADOW MESSAGE |
| 06 INITIALIZE SYSTEM H/W | 6E DISPLAY NON-DISPOSABLE SEGMENT |
| 08 INITIALIZE CHIPSET REGISTERS | 70 DISPLAY ERROR MESSAGE |
| 09 SET IN POST FLAG | 72 CHECK FOR CONFIGURATION ERROR |
| 0A INIT CPU REGISTERS | 74 TEST REAL-TIME CLOCK |
| 0B CPU CACHE ON | 76 CHECK FOR KEYBOARD EERROR |
| 0C INITIALIZE CACHE TO POST | 7C SETUP HARDWARE INTERRUPT VECTOR |
| 0E INITIALIZE I/O VALUE | 7E TEST COPROCESSOR IF PRESENT |
| 0F ENABLE THE L-BUS IDE | 80 DISABLE ON-BOARD I/O PORT |
| 10 INITIALIZE POWER MANAGER | 82 DETECT AND INSTALL EXT. RS232C |
| 11 LOAD ALTERNATE REGISTERS | 84 DETECT AND INSTALL EXT. PARALLEL |
| 13 PCI BUS MASTER RESET WITH INITIAL POST VALUE | 86 RE-INITIALIZE ON-BOARD I/O PORT |
| 14 INITIALIZE KEYBOARD CONTROLLER | 88 INITIALIZE BIOS DATA ROM |
| 16 CHECK CHECKSUM | 8A INITIALIZE EXTENDED BIOS DATA AREA |
| 18 INITIALIZE 8254 TIMER | 8C INITIALIZE FDD CONTROLLER |
| 1A INITIALIZE 8237 DMA CONTROLLER | 9A SHADOW OPTION ROMS |
| 1C RESET INTERRUPT CONTROLLER | 9C SETUP POWER MANAGEMENT |
| 20 TEST DRAM REFRESH | 9E ENABLE H/W INTERRUPT |
| 22 TEST 8742 KEYBOARD CONTROLLER | A0 SET TIME OF DAY |
| 24 SET ES SEGMENT REGISTERS TO 4GB | A4 INITIALIZE TYPOMATIC RATE |
| 26 ENABLE A20 | A8 ERASE F2 PROMPT |
| 28 AUTO SIZING DRAM | AA SCAN FOR F2 KEY STROKE |
| 32 COMPUTE THE CPU SPEED | AC ENTER SETUP |
| 34 TEST CMOS RAM | AE CLEAR IN POST FLAG |
| 38 SHADOW SYSTEM BIOS ROM | B0 CHECK FOR ERRORS |
| 3A AUTO SIZING CACHE | B2 POST DONE-PREPARE TO BOOT O/S |
| 3C CONFIGURE ADVANCED CHIPSET REGISTERS | B4 ONE BEEP |
| 3D LOAD ALTER REG. WITH CMOS VALUE | B6 CHECK PASSWORD (OPTION) |
| 42 INITIALIZE INTERRUPT VECTOR | B7 ACPI INIT |
| 44 INITIALIZE BIOS INTERRUPT | BA DMI INIT |
| 46 CHECK ROM COPYRIGHT NOTICE | BE CLEAR SCREEN |
| 47 INITIALIZE I20 SUPPORT IF INSTALLED | C0 TRY BOOT WITH INT19 |
| 48 CHECK VIDEO CONFIGURE AGAINST CMOS | D0 INTERRUPT HANDLER ERROR |
| 49 INITIALIZE PCI BUS AND DEVICE | D2 UNKNOWN INTERRUPT ERROR |
| 4A INITIALIZE ALL VIDEO BIOS ROM | D4 PENDING INTERRUPT ERROR |
| 4C SHADOW VIDEO BIOS ROM | D6 SHUTDOWN 5 |
| 50 DISPLAY CPU TYPE AND SPEED | D8 SHUTDOWN ERROR |
| 52 TEST KEYBOARD | DA EXTENDED BLOCK MOVE |
| 54 SET KEYCLICK IF ENABLED | DC SHUTDOWN 10 |
| 56 ENABLE KEYBOARD | 89 ENABLE NMI |
| 58 TEST FOR UNEXPECTED INTERRUPTS | 90 INITIALIZE HDD CONTROLLER |
| 5A DISPLAY "PRESS SETUP" | 91 INITIALIZE LOCAL BUS HDD CONTROLLER |
| 5C TEST RAM BETWEEN 512K AND 640K | 92 JUMP TO USER PATCH 2 |
| 60 TEST EXTENDED MEMORY | 94 DISABLE A20 ADDRESS LINE |
| 62 TEST EXTENDED MEMORY ADDRESS LINE | 96 CLEAR HUGE ES SEGMENT REG. |
| 64 JUMP TO USER PATCH 1 | 98 SEARCH FOR OPTION ROMS |

DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R	SAMSUNG
CHECK	LEE, S.P	DEV. STEP	PR	MAIN		ELECTRONICS
APPROVAL	LIM, J.G	REV	1.1	FHW		PART NO. BA41-00720A
MODULE CODE	undefined	LAST EDIT	January 04, 2007 11:01:08 AM	PAGE	24	OF 47

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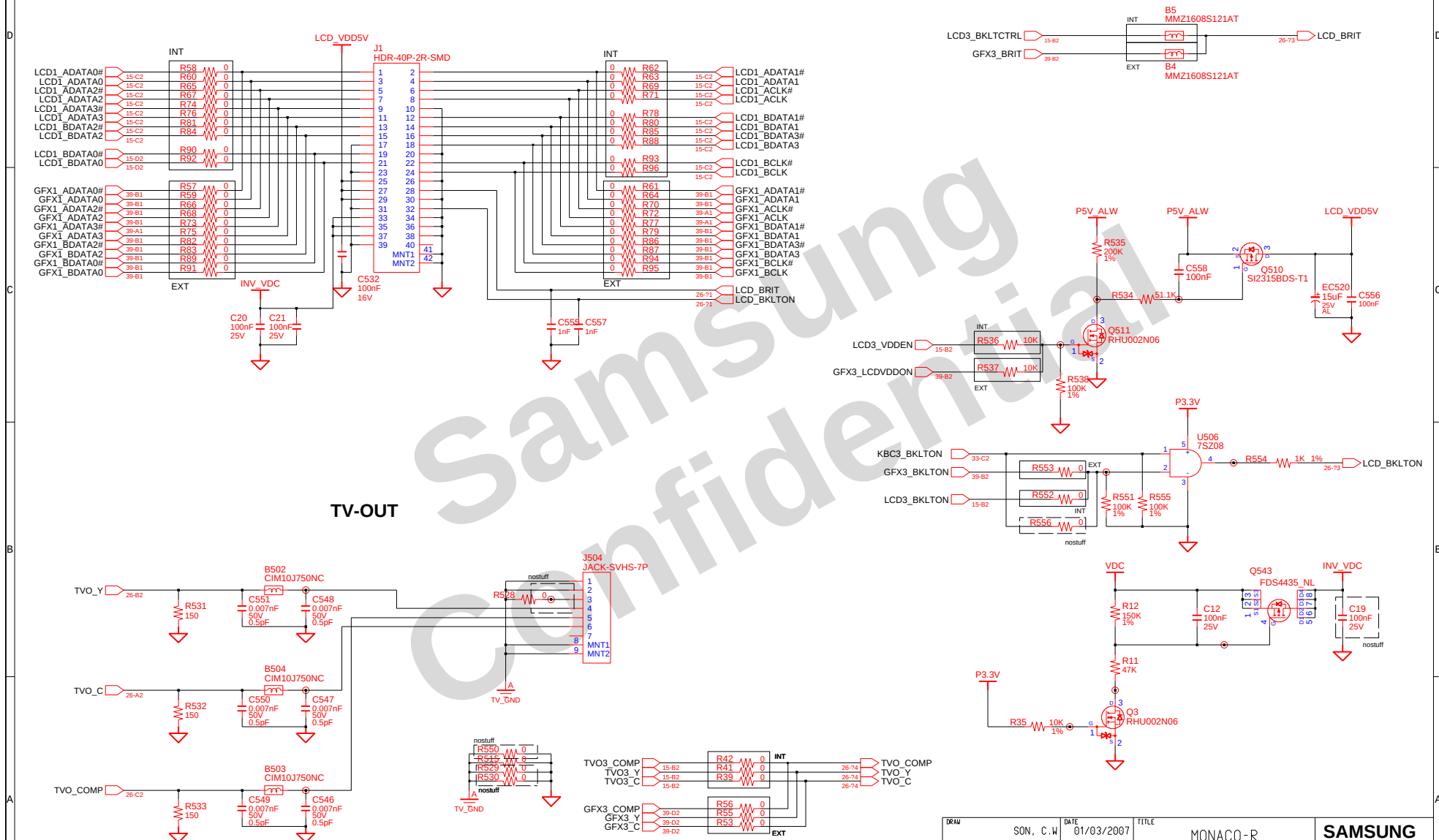


DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R MAIN CRT PORT	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	PR			PART NO. BA41-00720A
APPROVAL	LIM, J.G	REV	1.1			
MODULE CODE	undefined	LAST EDIT	January 04, 2007 11:01:08 AM	PAGE	25	OF 47

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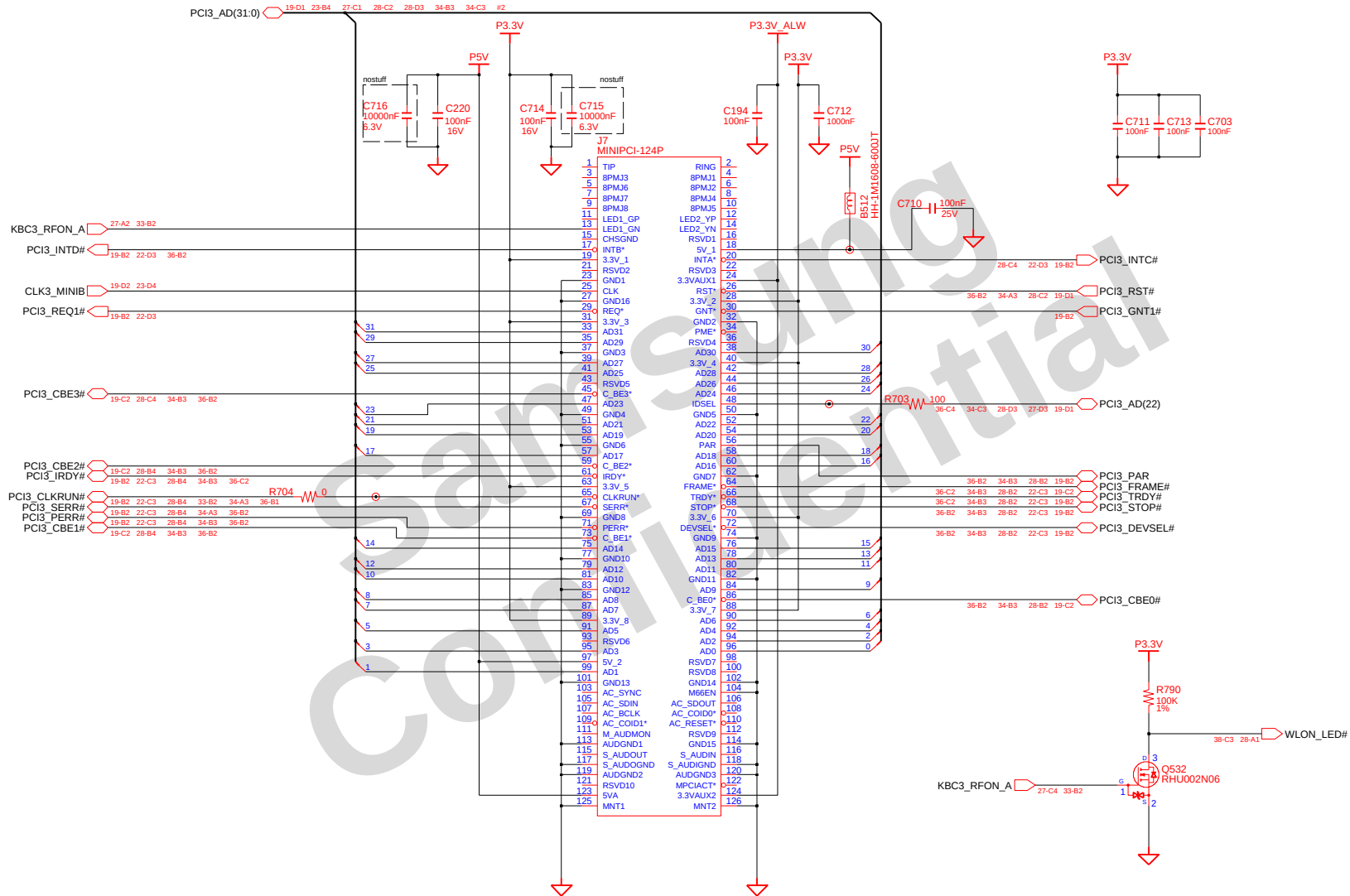
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LCD CONNECTOR



DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R MAIN LCD / TV-OUT	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	PR			PART NO. BA41-00720A
APPROVAL	LIM, J.G	REV	1.1			
MODULE CODE	undefined	LAST EDIT	January 04, 2007 11:01:08 AM	PAGE	26	OF 47

FOR WIRELESS LAN

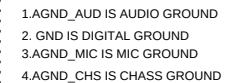


DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R MAIN MINI PCI A	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	PR			PART NO. BA41-00720A
APPROVAL	LIM, J.G	REV	1.1			
MODULE CODE	undefined	LAST EDIT	January 04, 2007 11:01:08 AM	PAGE	27	OF 47

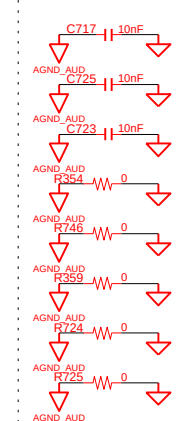
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DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R MAIN MINI PCI B	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.1			
MODULE CODE		LAST EDIT		January 04, 2007 11:01:08 AM		PAGE 28 OF 47

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ALL TYPE IS 1608



DRAM	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R MAIN AUDIO CODEC	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.1			
MODULE CODE	undefined	LAST EDIT	January 04, 2007 11:01:08 AM			
				PART NO.	BA41-00720A	

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JACK-PHONE-6P-PINK

5
4
3
6
2
1
G1
G2

AGND_AUD

AUDIO CHSS GND

Connect to Mount-hole.

B514 MMZ1608S121AT
B513 MMZ1608S121AT

C720 0.1nF
C719 0.1nF

29-B1 JCK_SENS_MIC#
29-D2 MIC1_R
29-D2 MIC1_L

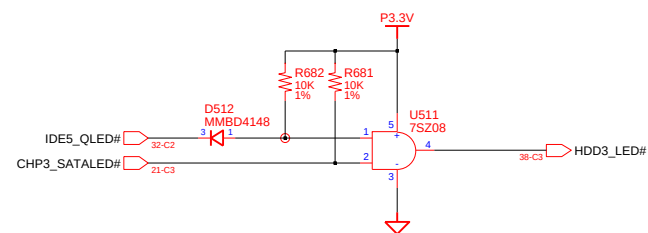
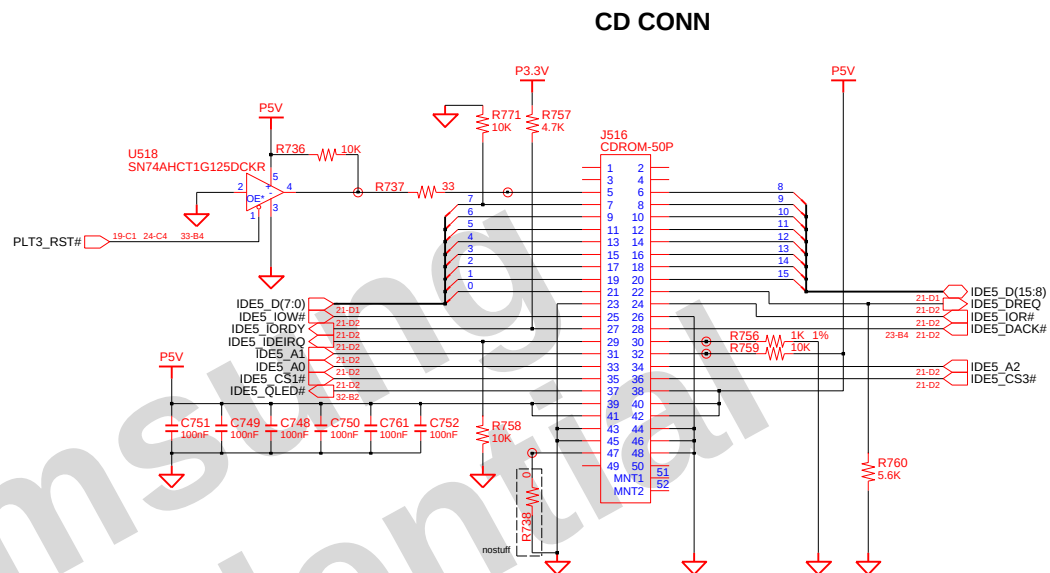
The schematic diagram illustrates the audio output stage of the 3722-002416 module. Key components and connections include:

- Input Stage:** A 6P-LIME jack (J515) provides input signals (R, L, G1, G2) to the 3722-002416 IC. The ground is connected to AGND_AUD.
- IC and Biasing:** The 3722-002416 IC is biased using a 0.1nF capacitor (C734) and a 1nF capacitor (C930). A 10K resistor (R739) is connected to the PSV supply.
- Comparison Stage:** Two MMZ1608S121AT comparators (B515, B516) are used to compare the input signals with a reference voltage.
- Output Stage:** The comparators drive two MMBT3904 transistors (Q522, Q523) through 1K resistors (R327, R328). The transistors are connected to a 3.3V supply (P3.3V) and a 7S208 component (Q27).
- Output Pins:** The circuit outputs signals to JCK_SENS# and JCK_SENS#P pins, and HP_OUT_R and HP_OUT_L pins.

DRAM	SON, C.W.	DATE	01/03/2007	TITLE	MONACO-R MAIN AUDIO / MDC CONN	SAMSUNG ELECTRONICS
CHECK	LEE, S.P.	DEV. STEP	PR			
APPROVAL	LIM, J.G.	REV	1.1			
MODULE CODE	undefined	LAST EDIT	January 04, 2007 11:01:08 AM			
				PAGE	31	OF 47

A

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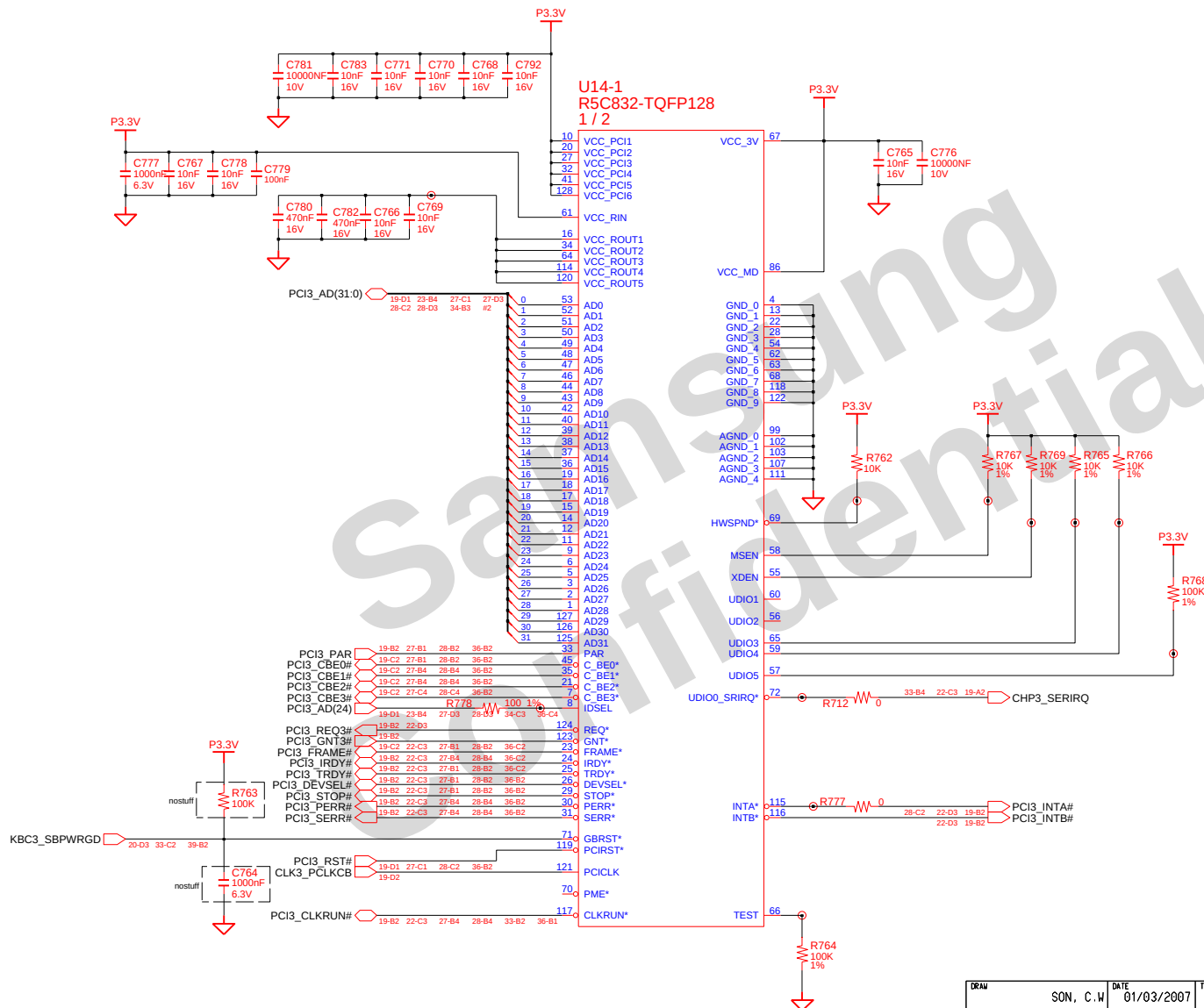
Condition: P90=P91=P92=High(MICOM_P3V)
MD0=MD1=Low(0V)
Serial Port: P84 & P85

DRAM	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R MAIN MICOM	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.1			
MODULE CODE	undefined	LAST EDIT	January 04, 2007 11:01:08 AM			
				PART NO.	BA41-00720A	

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OPTION



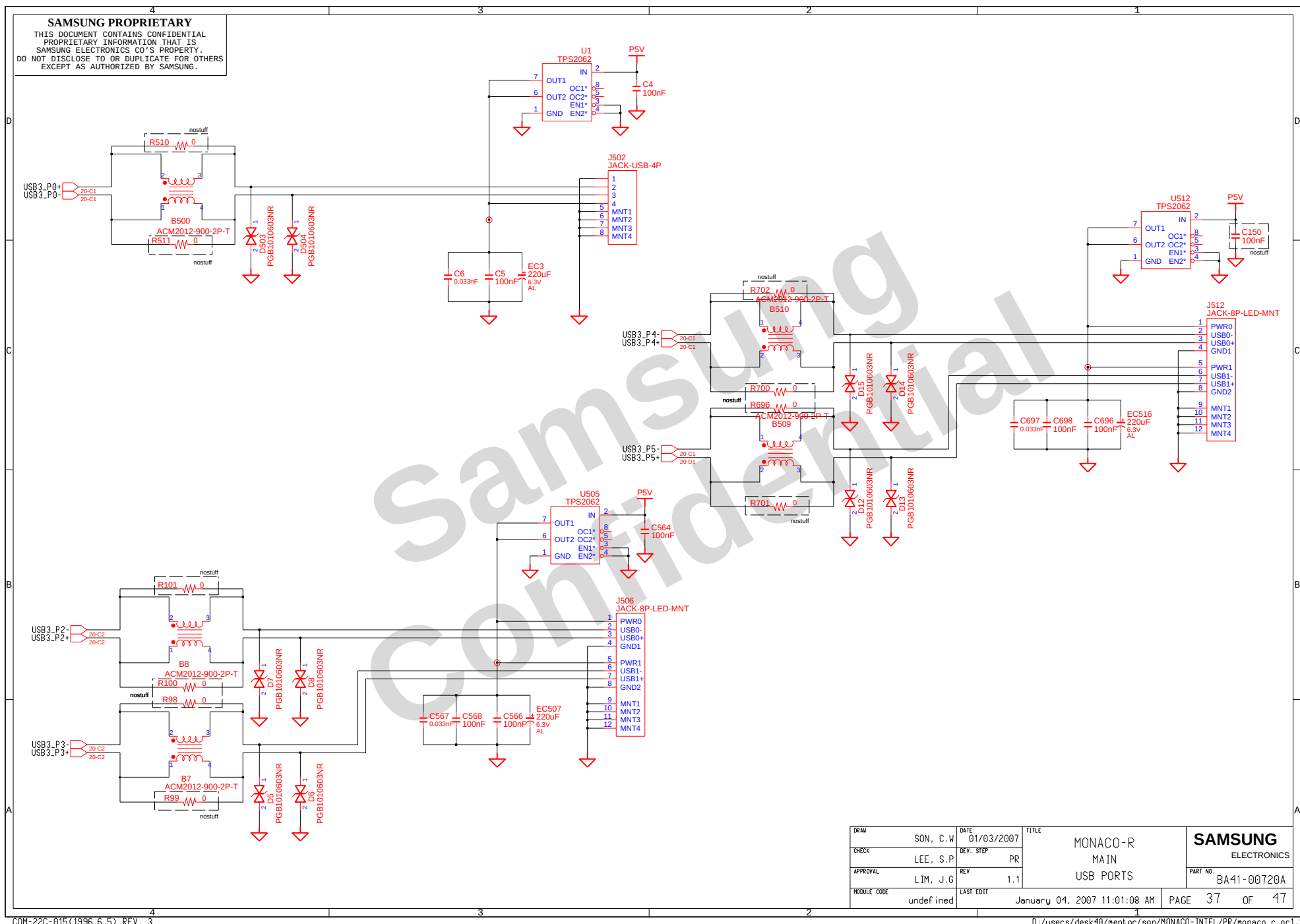
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CHECK	LEE, S.P	DEV. STEP	PR	MAIN		ELECTRONICS
APPROVAL	LIM, J.G	REV	1.1	5-IN-1 CONTROLLER(1/2)	PART NO.	BA41-00720A
MODULE CODE	undefined	LAST EDIT	January 04, 2007 11:01:08 AM	PAGE	34	OF 47



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DRAM	SON, C. W.	DATE	01/03/2007	TITLE	MONACO-R MAIN LAN CONTROLLER	SAMSUNG ELECTRONICS PART NO. BA41-00720A
CHECK	LEE, S. P.	DEV. STEP	PR			
APPROVAL	LIM, J. G.	REV	1.1			
MODULE CODE	undef ined	LAST EDIT				

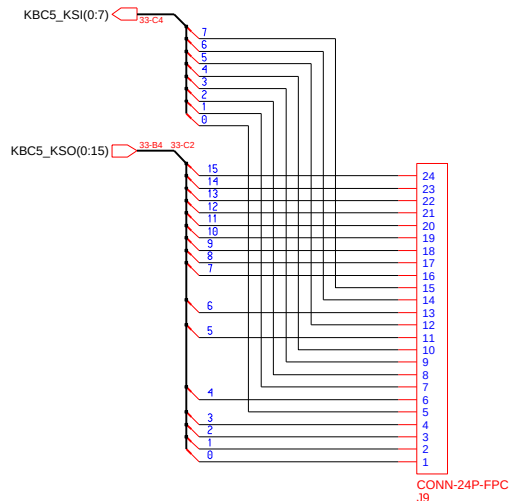
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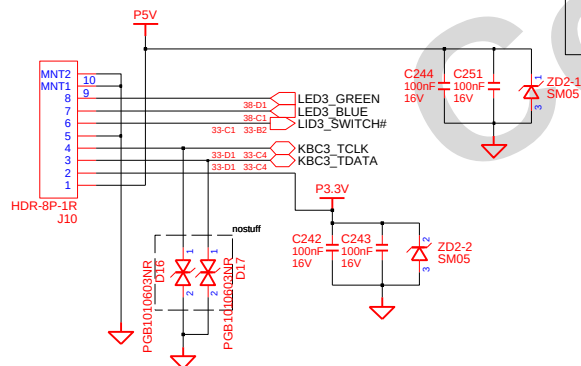
DRAM	SON, C. W.	DATE	01/03/2007	TITLE	MONACO-R MAIN USB PORTS	SAMSUNG ELECTRONICS PART NO. BA41-00720A
CHECK	LEE, S. P.	DEV. STEP	PR			
APPROVAL	LIM, J. G.	REV	1.1			
MODULE CODE	undefined	LAST EDIT				

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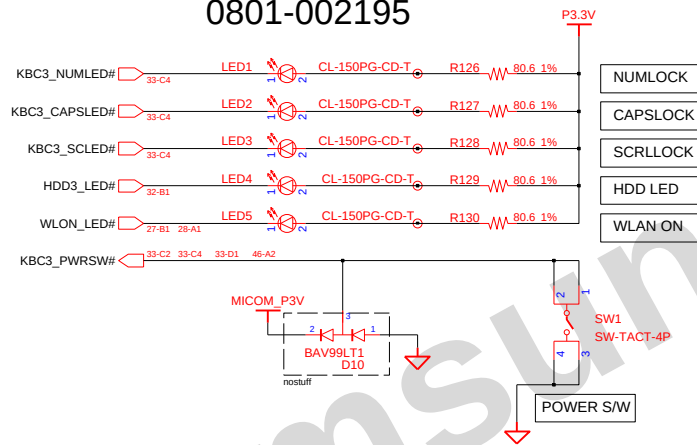
KEYBOARD



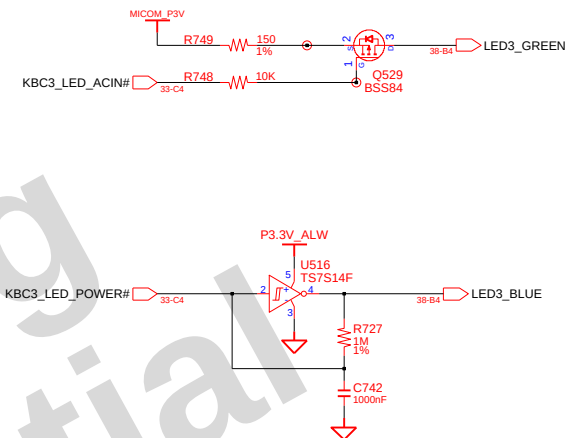
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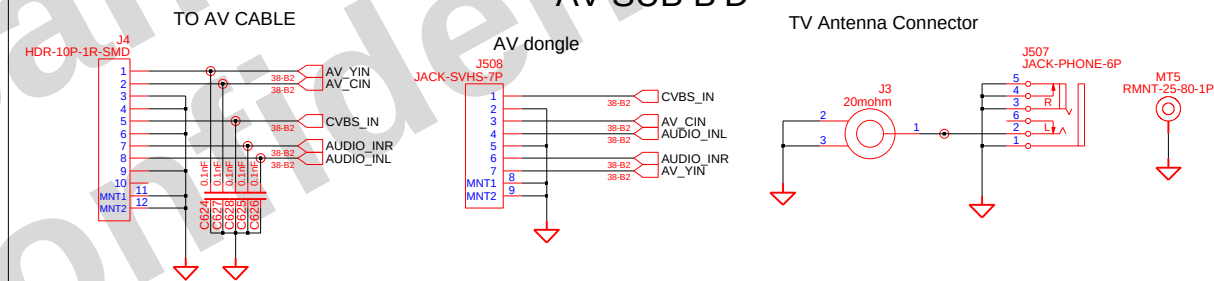
LED 0801-002195



ADAPTERIN/CHARGING LED

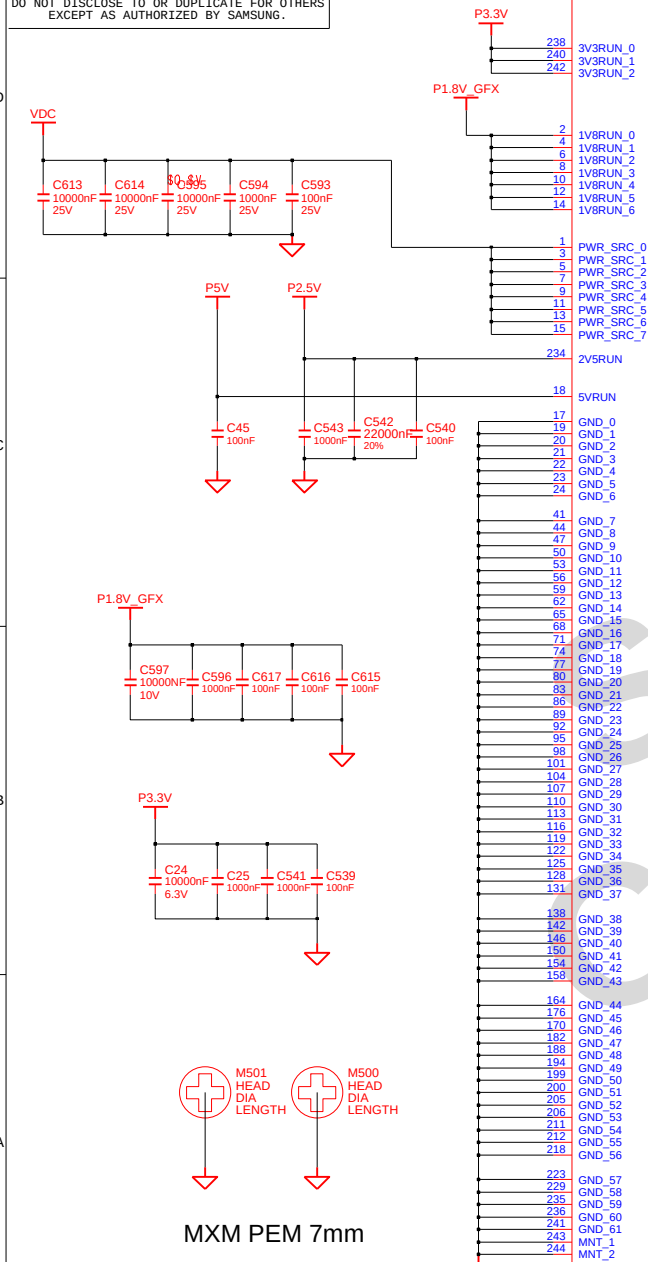


AV SUB B'D



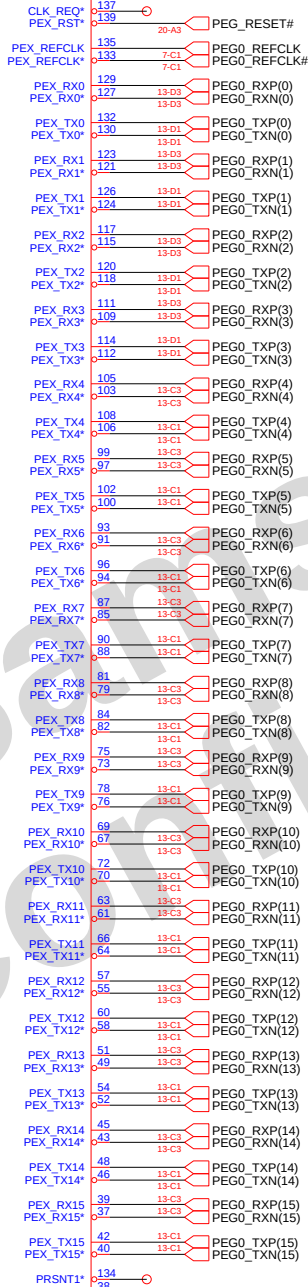
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CHECK	LEE, S.P	DEV. STEP	PR	MAIN		
APPROVAL	LIM, J.G	REV	1.1	KBD/TPAD/LED/SW		
MODULE CODE	undefined	LAST EDIT	January 04, 2007 11:01:08 AM	PAGE	38 OF 47	

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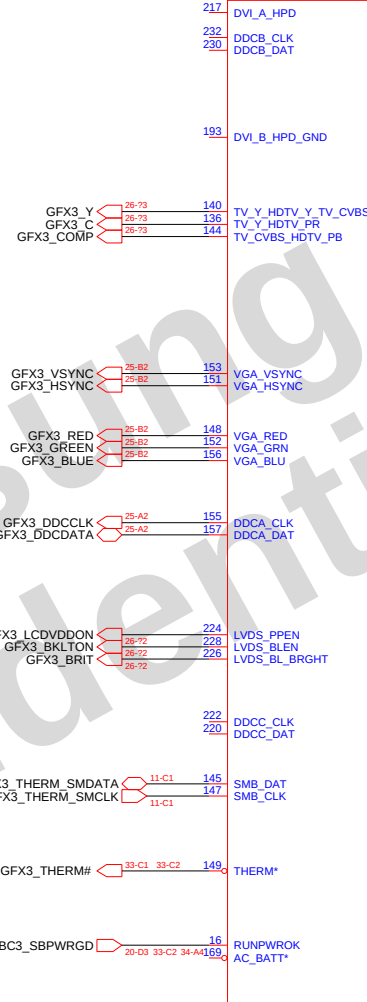


J505-1
SOCKET-242P-2R-SMD

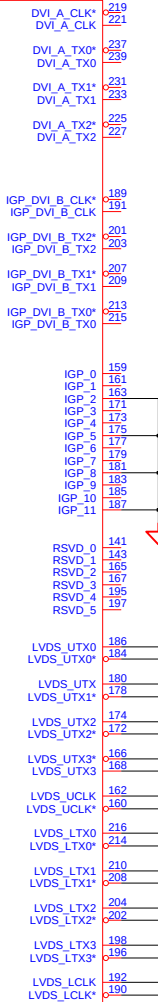
1/2



J505-2
SOCKET-242P-2R-SMD
2/2



EXT GFX ONLY

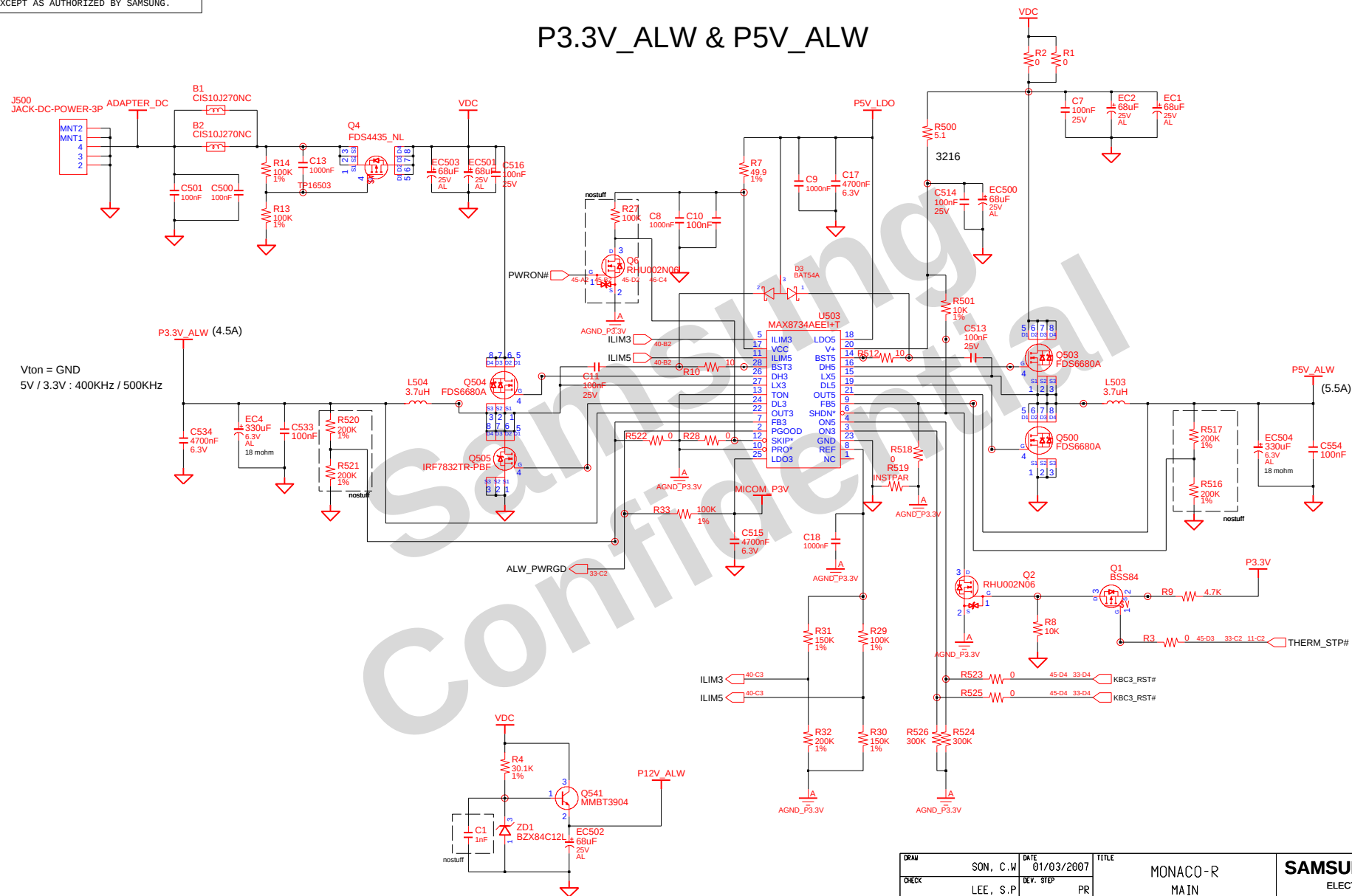


DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R	SAMSUNG
CHECK	LEE, S.P	DEV. STEP	PR		MAIN	ELECTRONICS
APPROVAL	LIM, J.G	REV	1.1		MXM CONN	PART NO. BA41-00720A
MODULE CODE	undefined	LAST EDIT	January 04, 2007 11:01:08 AM	PAGE	39	OF 47

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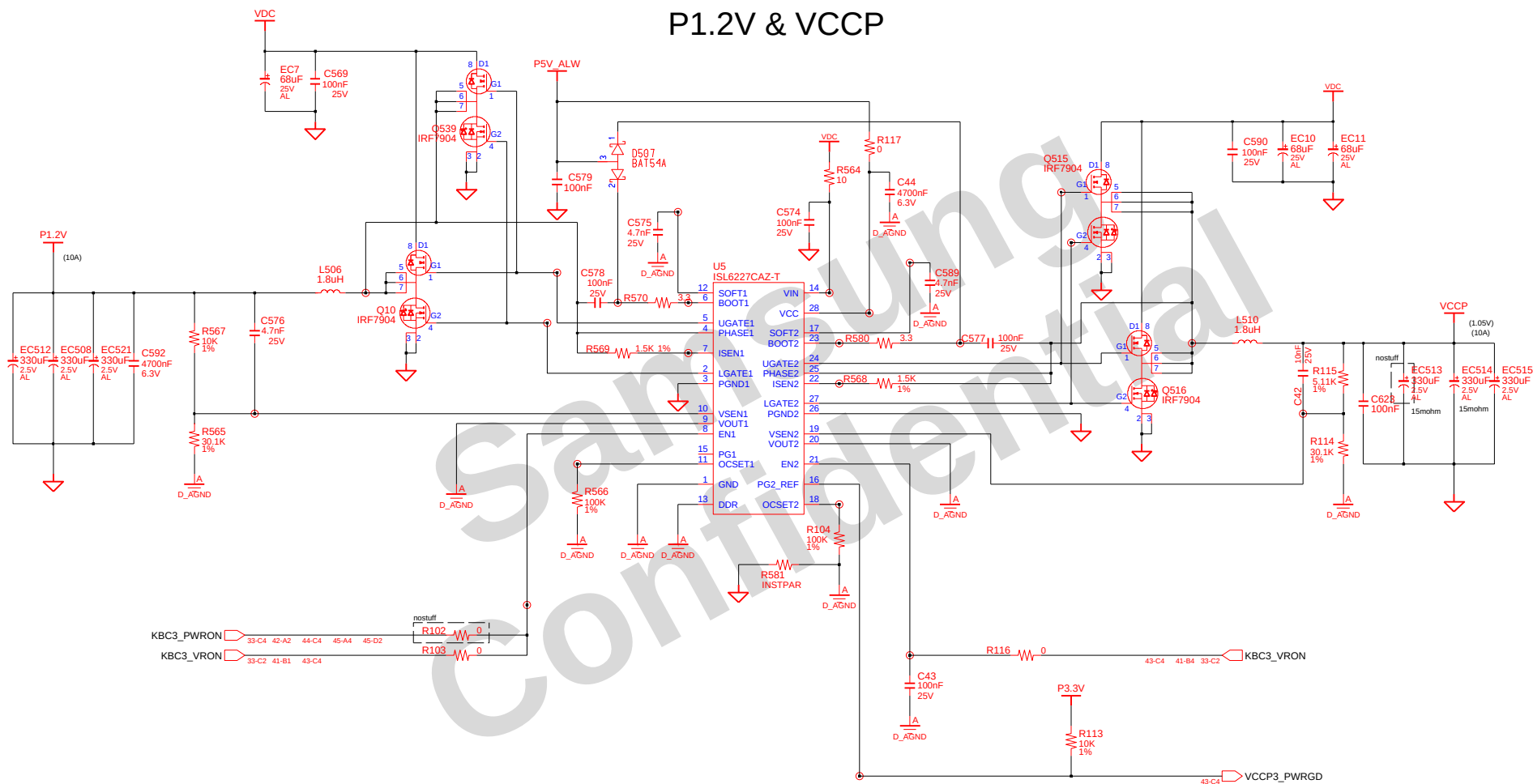
P3.3V_ALW & P5V_ALW



DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R	SAMSUNG
CHECK	LEE, S.P	DEV. STEP	PR	MAIN		ELECTRONICS
APPROVAL	LIM, J.G	REV	1.1	3.3V_ALW/5V_ALW POWER	PART NO.	BA41-00720A
MODULE CODE	undefined	LAST EDIT	January 04, 2007 11:01:08 AM	PAGE	40	OF 47

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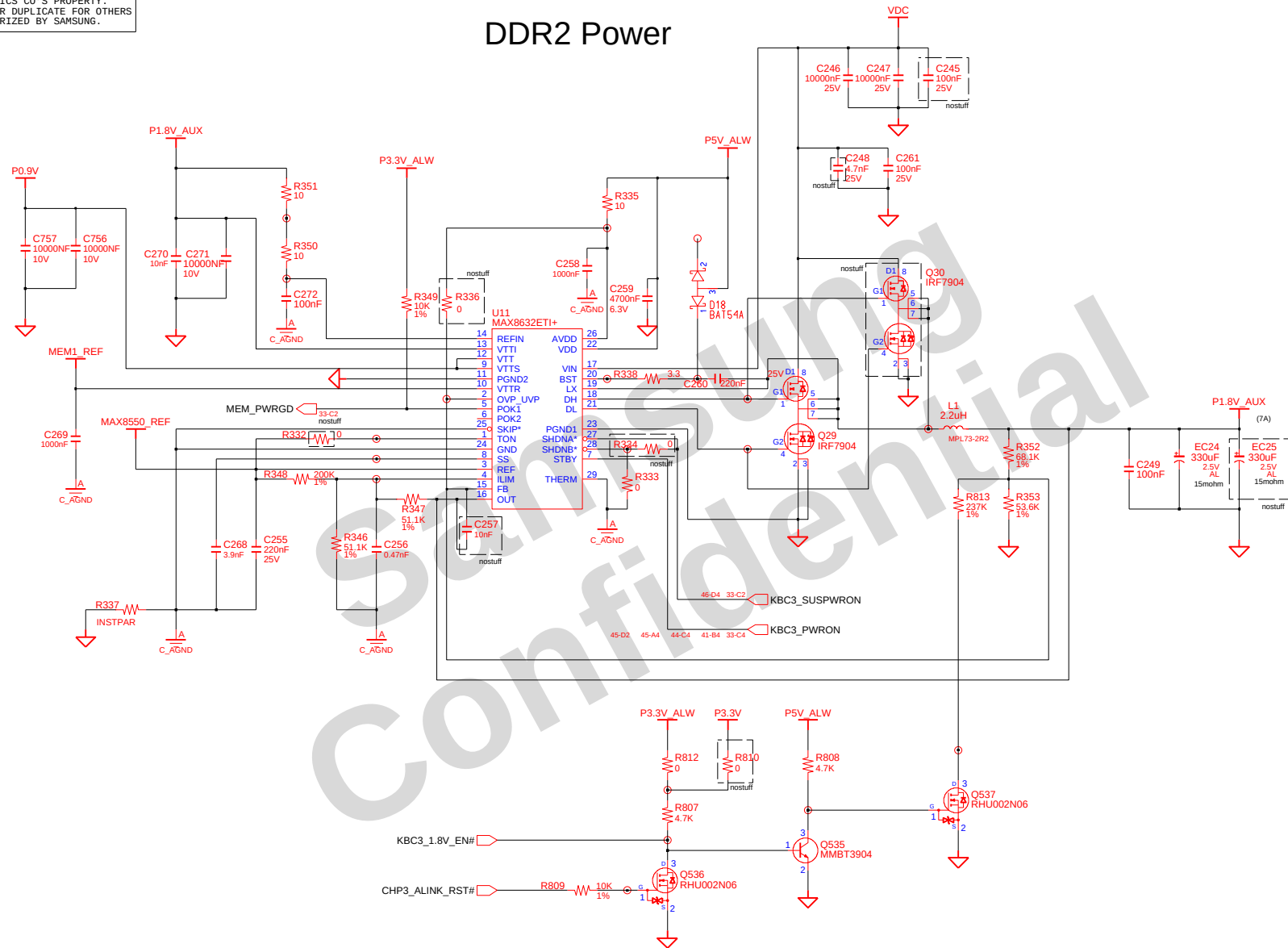
P1.2V & VCCP



DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R MAIN 1.2V/VCCP POWER	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	PR			PART NO. BA41-00720A
APPROVAL	LIM, J.G	REV	1.1			
MODULE CODE	undefined	LAST EDIT	January 04, 2007 11:01:08 AM	PAGE	41	OF 47

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DDR2 Power



DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R MAIN DDR2 POWER	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	PR			PART NO. BA41-00720A
APPROVAL	LIM, J.G	REV	1.1			
MODULE CODE	undefined	LAST EDIT	January 04, 2007 11:01:08 AM	PAGE	42	OF 47

CPU VRM [SEMTECH]

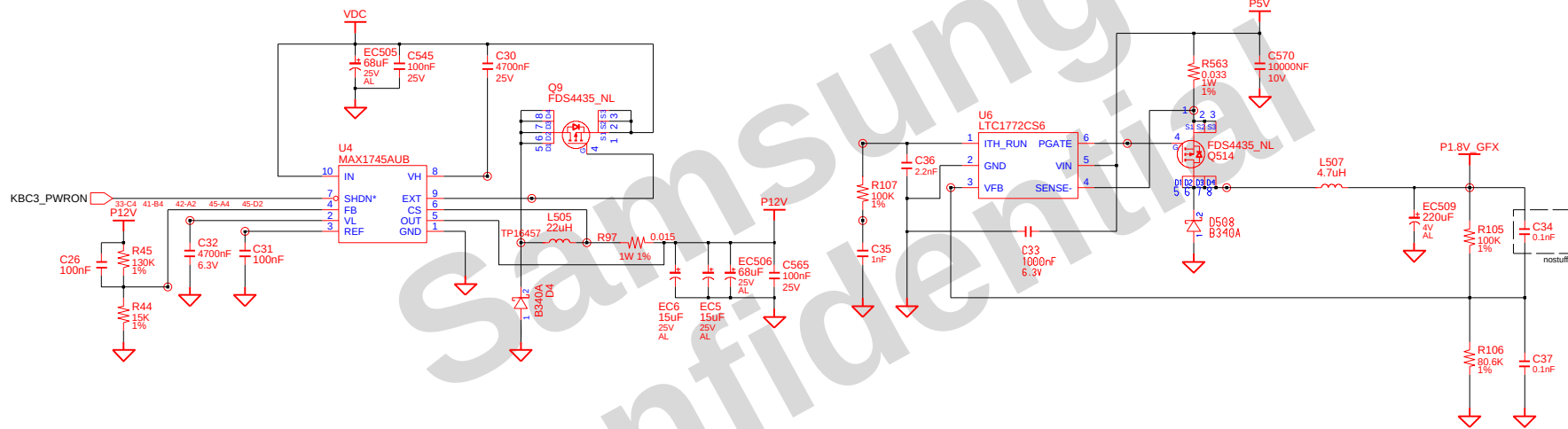
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P12V POWER

P1.8V POWER FOR MXM CARD

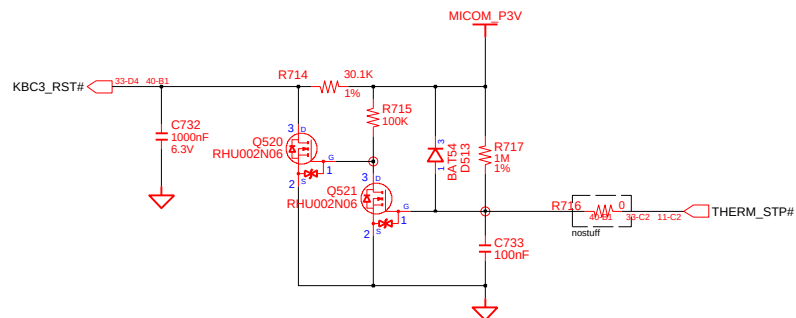


DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R MAIN P12V / MXM 1.8V POWER	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	PR			PART NO. BA41-00720A
APPROVAL	LIM, J.G	REV	1.1			
MODULE CODE	undefined	LAST EDIT	January 04, 2007 11:01:08 AM	PAGE	44	OF 47

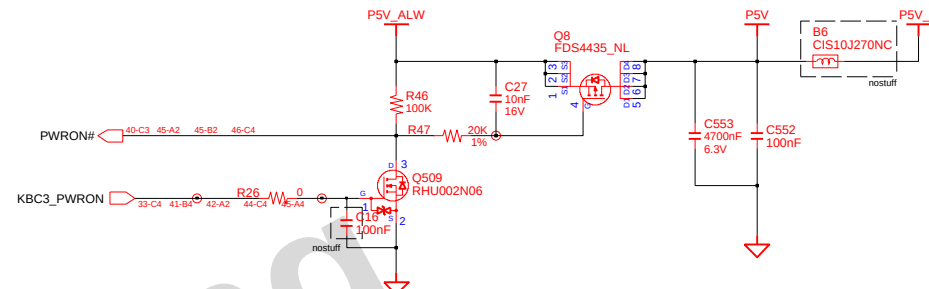
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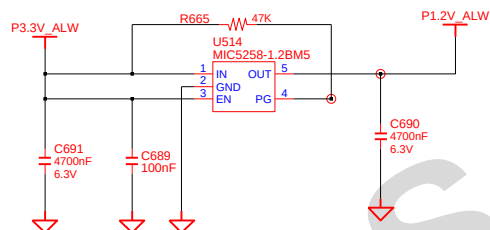
MICOM RESET



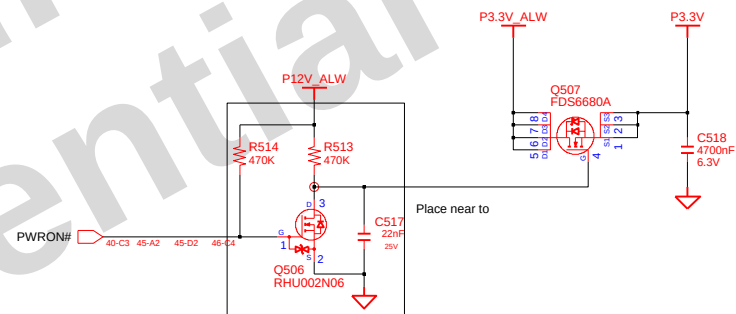
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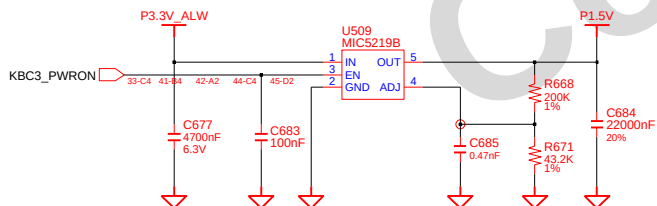
P1.2V_ALW



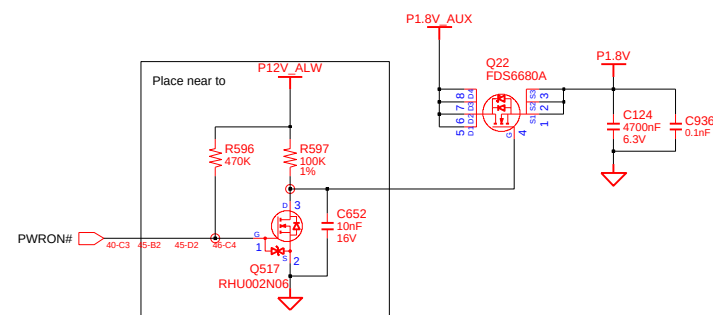
Switched Power On (P3.3V)



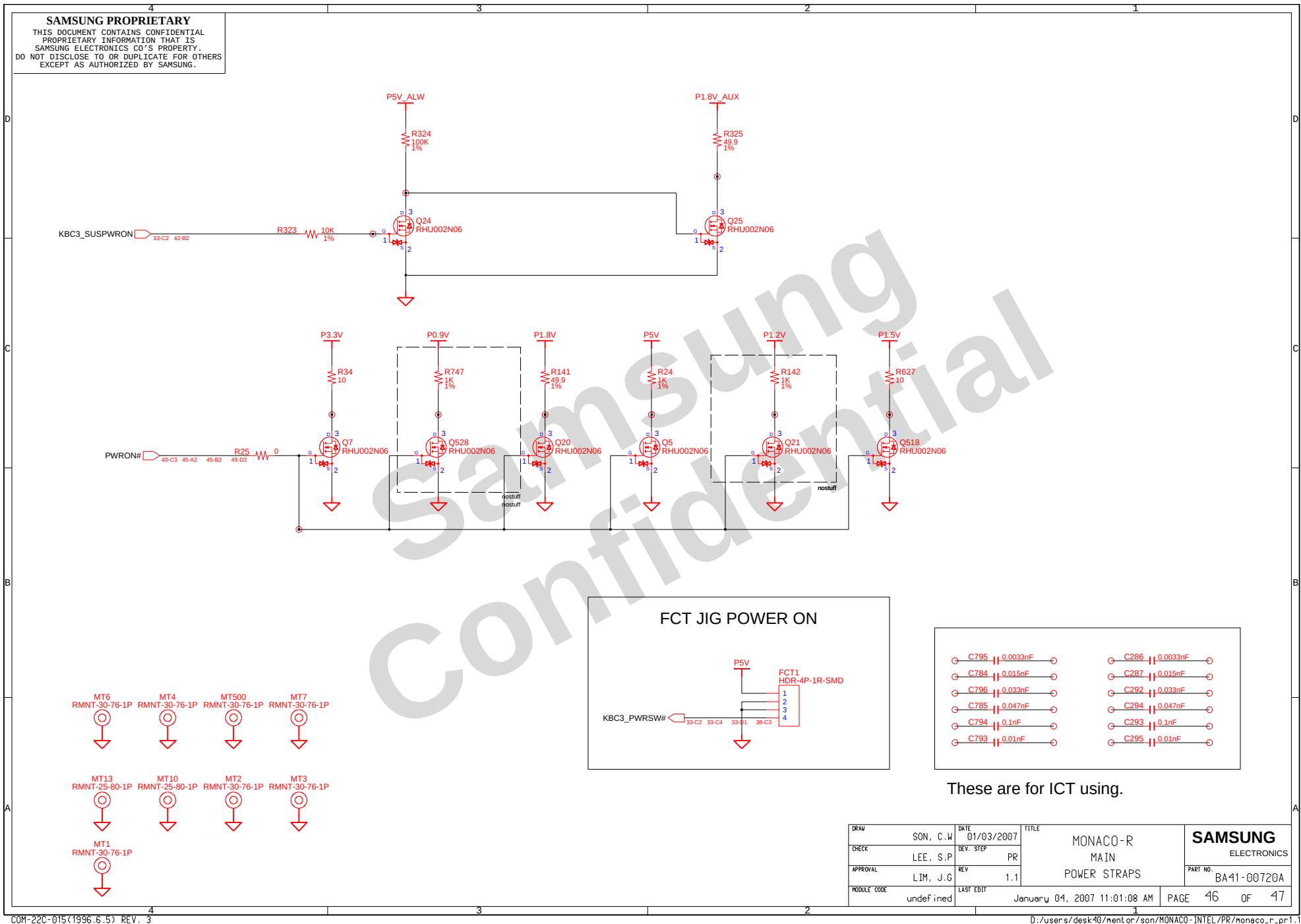
P1.5V POWER



Switched Power On (P1.8V)



DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R MAIN SWITCHED POWER	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	PR			PART NO. BA41-00720A
APPROVAL	LIM, J.G	REV	1.1			
MODULE CODE	undefined	LAST EDIT	January 04, 2007 11:01:08 AM	PAGE	45	OF 47



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TP16759OILIM5
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TP16761OTV0_Y
TP16762OCFX3_Y
TP16763OCFX3_Y
TP16764CMIC1_L
TP16765CMIC1_R
TP16766OTV03_C
TP16767OTV03_Y
TP16768OIDE5_A0
TP16769OIDE5_A1
TP16770OIDE5_A2
TP16774OPC_BEP
TP16755OAC_SDOU
TP16756OCRT3_RED
TP16747OCFX3_RED
TP16748CHP_OUT_L
TP16749CHP_OUT_R
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TP16751OPC13_PAR
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TP16753OTV0_COMP
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DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R MAIN TEST POINTS	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	PR			PART NO. BA41-00720A
APPROVAL	LIM, J.G	REV	1.1			
MODULE CODE		LAST EDIT				
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