Compal Confidential

G470/G570 DIS+UMA+Muxless M/B Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH
ATI Robson/PX3.0,PX4.0

2010-07-22

LA-6758P

REV:0.1

Security Classification	Compal Secret Data		
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Title	Cover Page	
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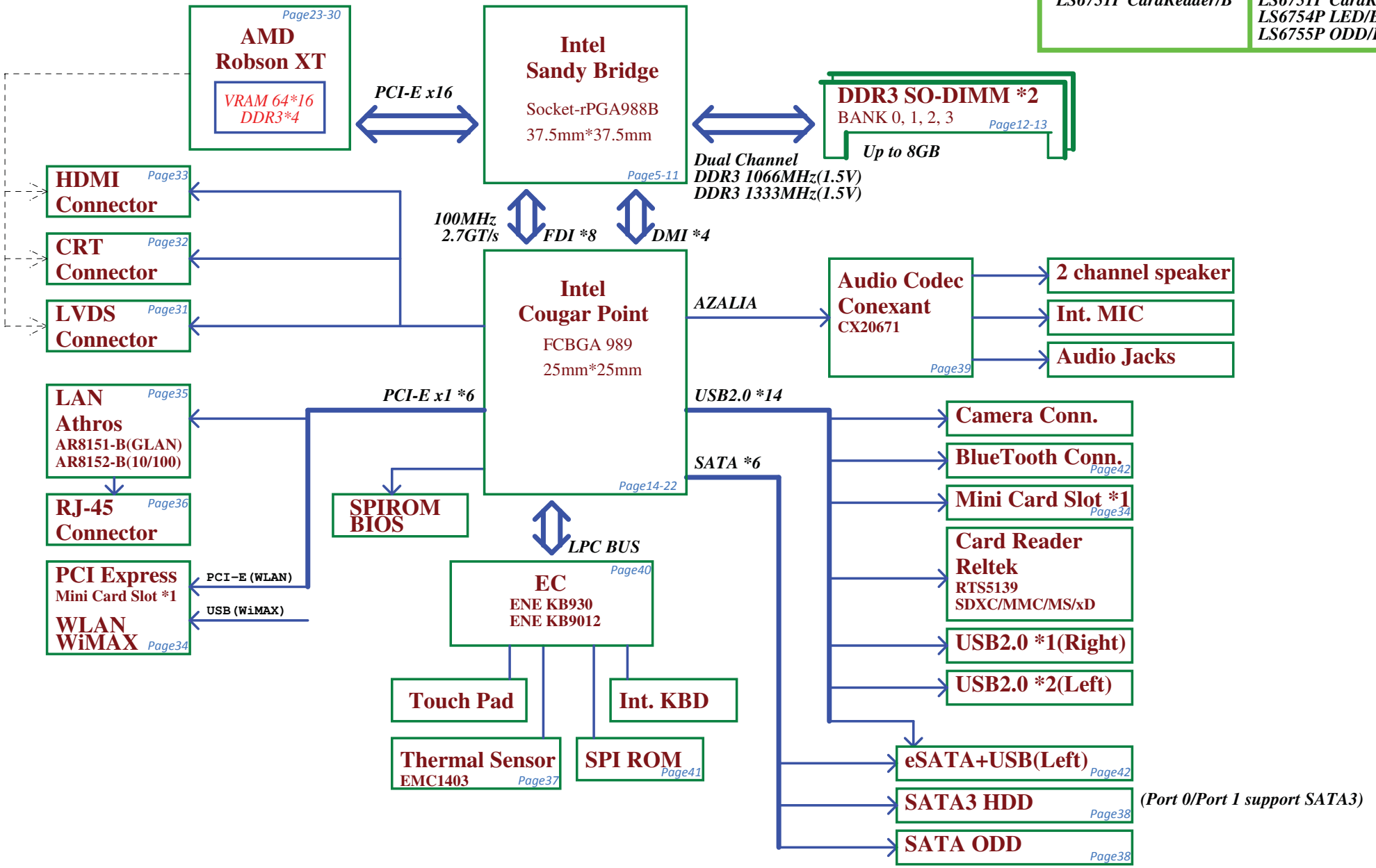
Compal confidential
File Name : G470/G570

For 14"(Page 4x)	For 15"(Page 4x+1)
LS6753P PWR/B	LS6753P PWR/B
LS6751P CardReader/B	LS6751P CardReader/B
	LS6754P LED/B
	LS6755P ODD/B



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Title	Block Diagram		
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Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +0.75VS +1.05VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	
0	0	0 V	0 V	0 V	EVT
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	DVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	PVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	MP
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	
7	NC	2.500 V	3.300 V	3.300 V	

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403-2	1001_101xb
Thermal Sensor EMC1402-1	100_1100 b

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B (Right Side)
		1	USB Port (Left Side)
	UHCI1	2	USB Port (Left Side)
		3	USB Port (Left Side)
	UHCI2	4	
		5	Camera
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Mini Card(WLAN)
		9	
	UHCI5	10	
		11	Card Reader
	UHCI6	12	
		13	Blue Tooth

BOM Structure Table

BTO Item	BOM Structure
UMA only	PX@
Muxless	PX@+VGA@
Discrete Only	DIS@+VGA@
PX3.0 only, not for BACO	PX3@
BACO	BACO@
COMMON HDMI	HDMI@
UMA HDMI	UMA_HDMI@
Discrete HDMI	VGA_HDMI@
eSATA	ESATA@
Blue Tooth	BT@
Connector	ME@
45 LEVEL	45@
10/100 LAN	8152@
GIGA LAN	GIGA@
Cameara	CMOS@
Unpop	@

SMBUS Control Table

	SOURCE	VGA	BATT	KE930	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB930 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB930 +3VALW	X	X	X	X	X	X	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	X	V +3VS	X	X	V +3VS	X

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Power-Up/Down Sequence

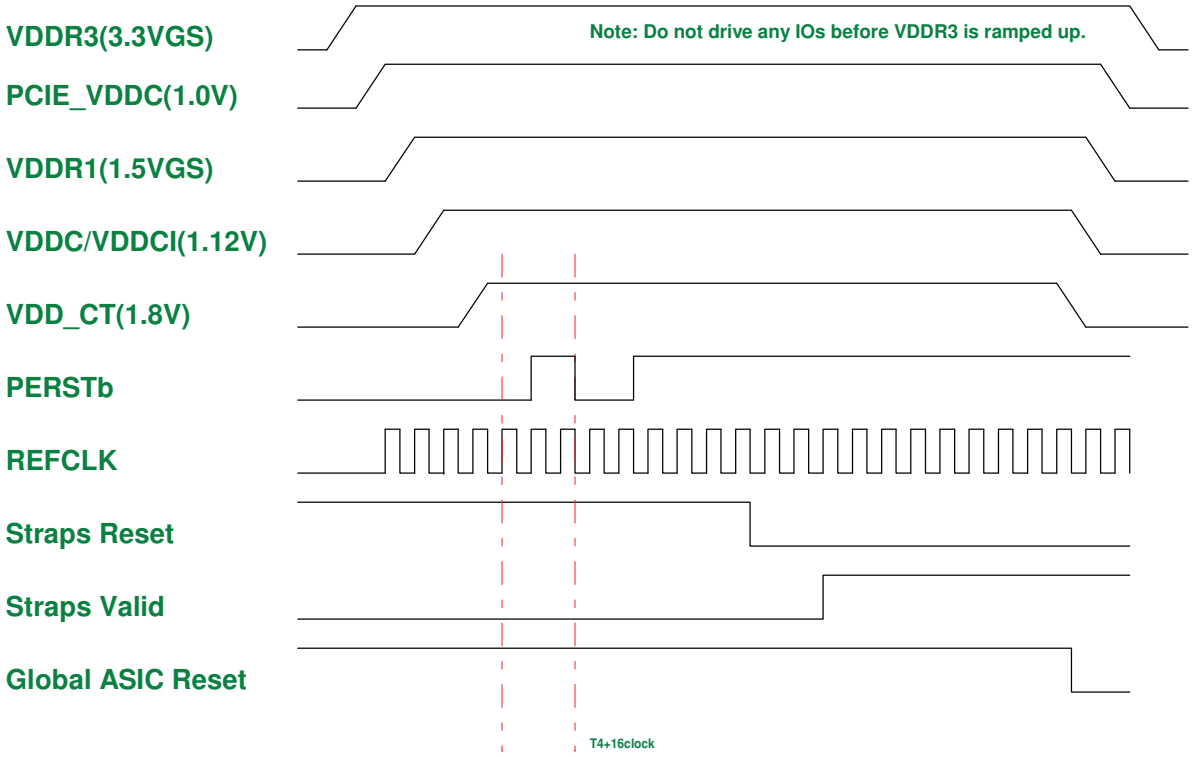
1. All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.

2. VDDR3 should ramp-up before or simultaneously with VDDC.

3. For LVDS, DPx_VDD10 should ramp-up before DPx_VDD18 and the PCIe Reference clock should begin before DPx_VDD18. For power-down, DPx_VDD18 should ramp-down before DPx_VDD10.

4. The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD_CT have ramped up.

5.VDDC and VDD_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD_CT starts to ramp-up (or vice versa).)



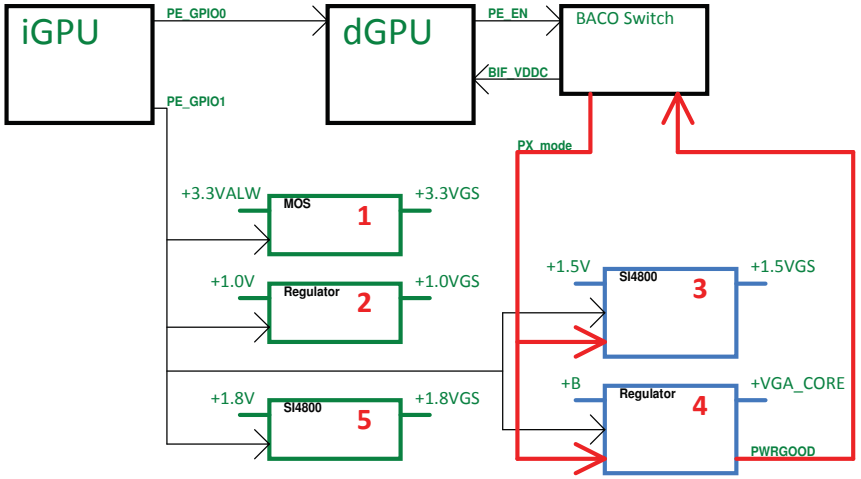
Without BACO option :

PE_GPIO0 : Low -> Reset dGPU ; High ->Normal operation
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON

BACO option :

PE_GPIO0 : High ->Normal operation (dGPU is not reseton BACO mode)
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	575mA
PCIE_VDDC	1.0V	OFF	ON	2A
VDDR3 , and A2VDD	3.3V	OFF	ON	190mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	OFF	ON Same as PCIE_VDDC	70mA
VDDR1	1.5V	OFF	OFF	2.8A
VDDC/VDDCI	1.12V	OFF	OFF	12.9A



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Title: dGPU Block Diagram

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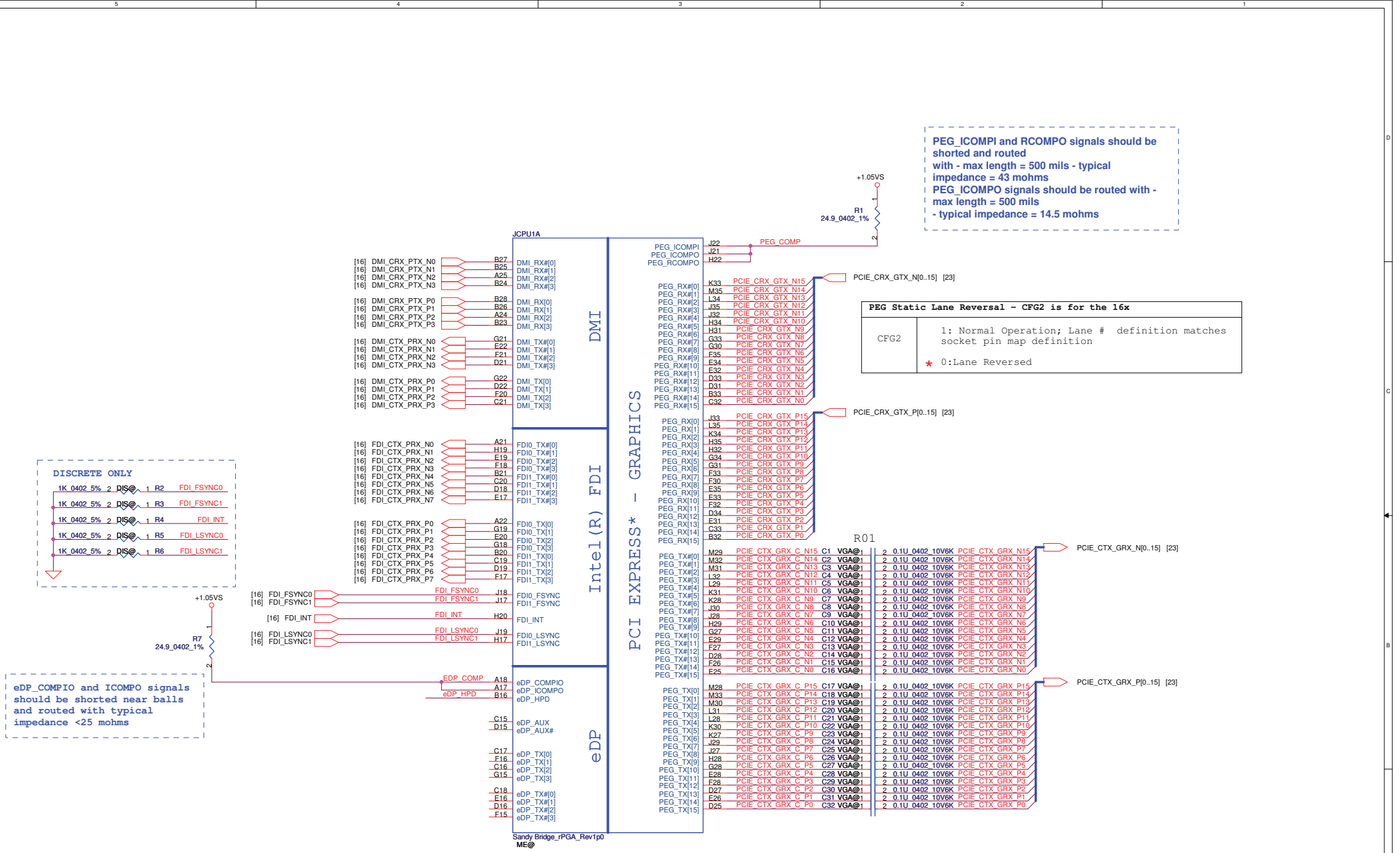

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Title: PROCESSOR(1/7) DMI,FDI,PEG

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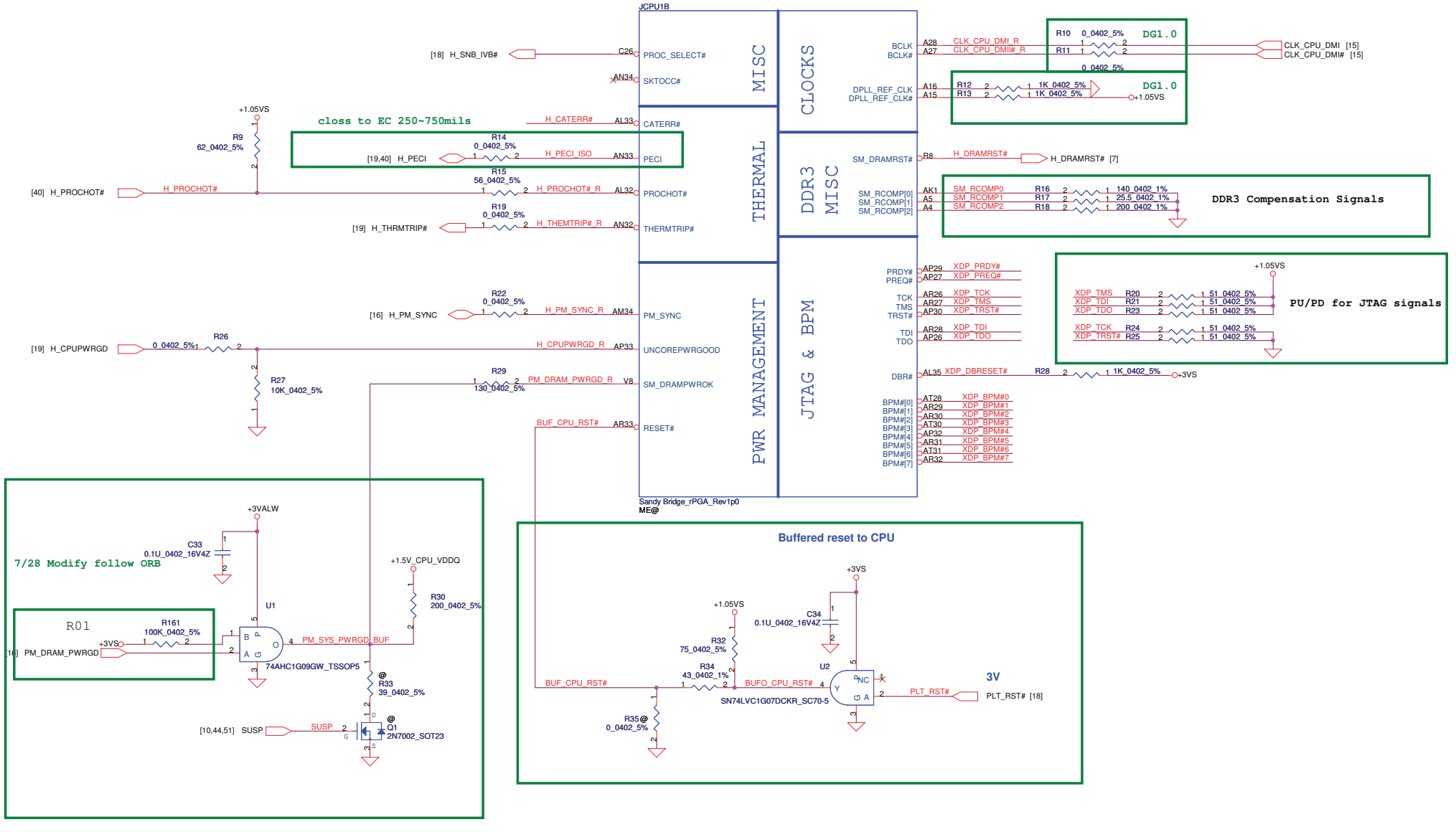

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Compal Electronics, Inc.			
Title: PROCESSOR(2/7) PM,XDP,CLK			
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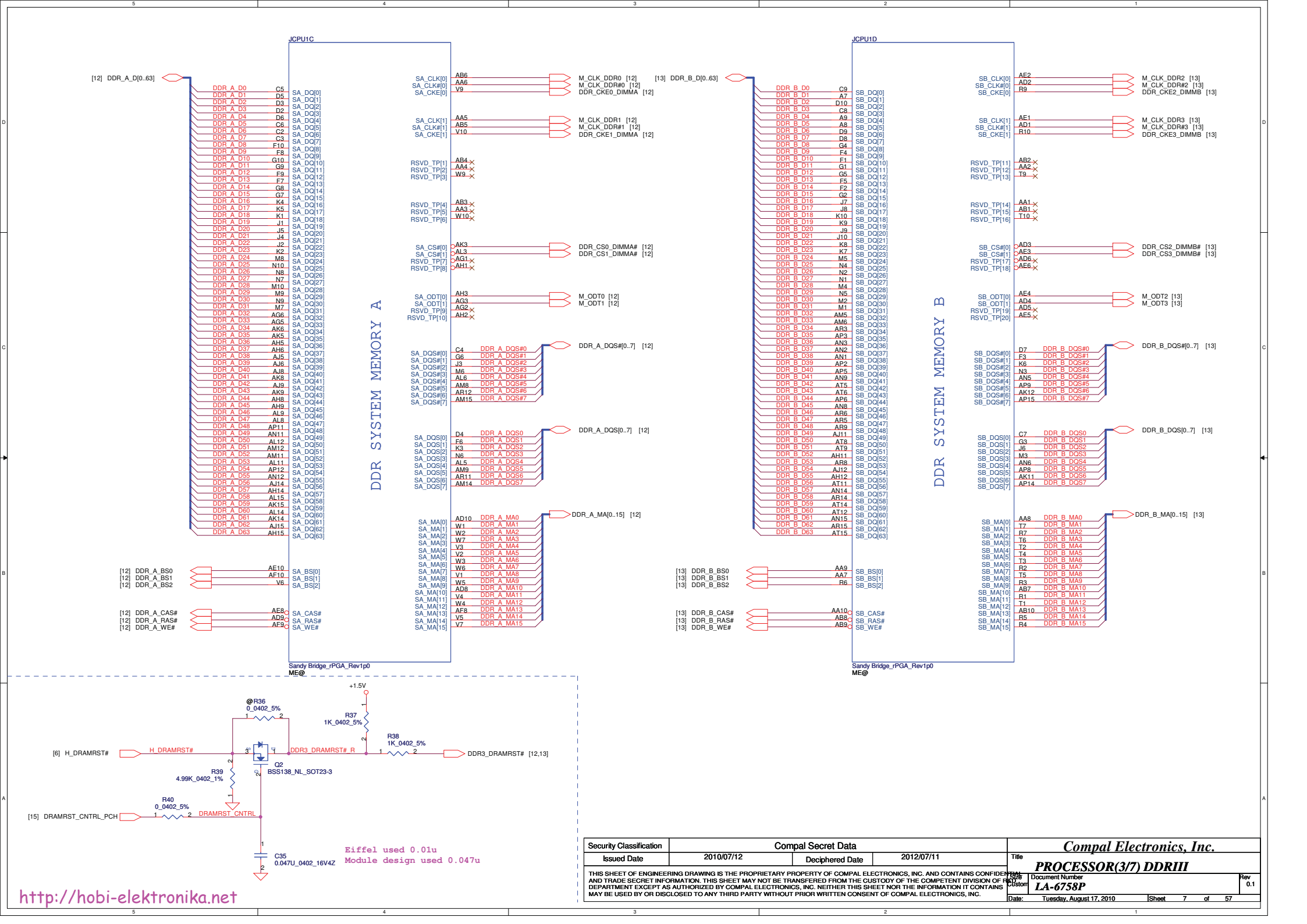

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Title: **PROCESSOR(3/7) DDRIII**

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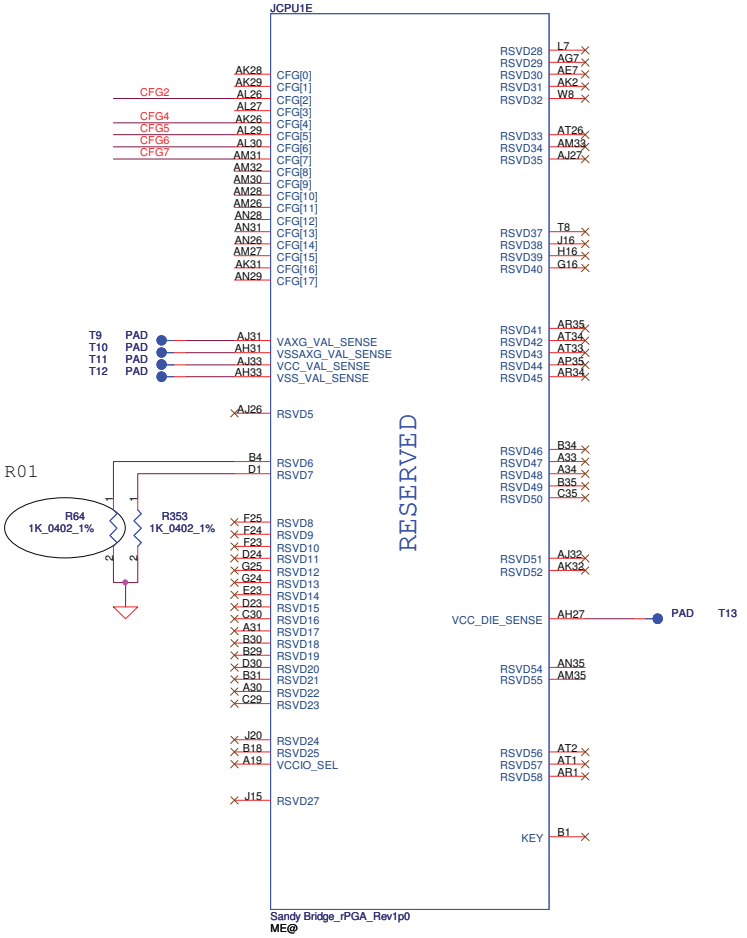
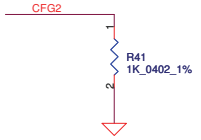
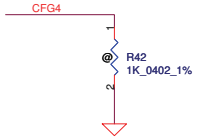
CFG Straps for Processor

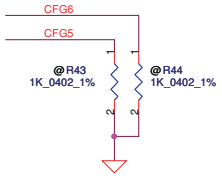




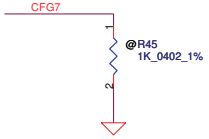
PEG Static Lane Reversal – CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 – Device 1 functions 1 and 2 disabled 10: x8, x8 – Device 1 function 1 enabled ; function 2 disabled 01: Reserved – (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 – Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Title: PROCESSOR(4/7) RSVD,CFG

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POWER

JCPU1F

QC=94A
DC=53A

CORE SUPPLY

+CPU_CORE
(6/16 change 10uF_0603_6.3V)*5
C36 10U_0805_6.3V6M
C37 10U_0805_6.3V6M
C38 10U_0805_6.3V6M
C39 10U_0805_6.3V6M
C40 10U_0805_6.3V6M
C48 10U_0603_6.3V6M
C49 10U_0603_6.3V6M
C50 10U_0603_6.3V6M
C51 10U_0603_6.3V6M
C52 10U_0603_6.3V6M
C53 @ 10U_0603_6.3V6M

+CPU_CORE
(22uF_0805_6.3V)*16
C66 22U_0805_6.3V6M
C67 22U_0805_6.3V6M
C68 22U_0805_6.3V6M
C70 22U_0805_6.3V6M
C71 22U_0805_6.3V6M
C74 22U_0805_6.3V6M
C75 22U_0805_6.3V6M
C76 22U_0805_6.3V6M
C77 22U_0805_6.3V6M
C78 22U_0805_6.3V6M
C79 22U_0805_6.3V6M
C80 22U_0805_6.3V6M
C81 22U_0805_6.3V6M
C82 22U_0805_6.3V6M
C83 22U_0805_6.3V6M
C84 22U_0805_6.3V6M
C85 @ 22U_0805_6.3V6M
C86 @ 22U_0805_6.3V6M
C87 @ 22U_0805_6.3V6M

+CPU_CORE
(330uF)*4
C88 330U_X_2VM_R8M
C89 330U_X_2VM_R8M
C90 330U_X_2VM_R8M
C91 330U_X_2VM_R8M

AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26
AF35 AF34 AF33 AF32 AF31 AF30 AF29 AF28 AF27 AF26
AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26
AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26
AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26
Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26
V35 V34 V33 V32 V31 V30 V29 V28 V27 V26
U35 U34 U33 U32 U31 U30 U29 U28 U27 U26
R35 R34 R33 R32 R31 R30 R29 R28 R27 R26
P35 P34 P33 P32 P31 P30 P29 P28 P27 P26

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

PEG AND DDR

Cap quantity follow HR_PDDG_Rev07
22uF*7 NO-STUFF
18A
OSCAN(22uF_0805_6.3V)*13
+1.05VS
C41 C42 C43 C44 C54 C45 C46 C55 C56 C47 22U_0805_6.3V6M
C57 C58 C59 @ C60 @ C61 @ C62 @ C63 @ C64 @ C65 @ 22U_0805_6.3V6M
C69 220U_6.3V_M
C72 220U_6.3V_M
C73 @ 330U_D2_2.5VY_R9M
OSCAN
(220uF_6.3V_4.2L_ESR17m)*2=(SF000002Y00)

VCCIO1 VCCIO2 VCCIO3 VCCIO4 VCCIO5 VCCIO6 VCCIO7 VCCIO8 VCCIO9 VCCIO10 VCCIO11 VCCIO12 VCCIO13 VCCIO14 VCCIO15 VCCIO16 VCCIO17 VCCIO18 VCCIO19 VCCIO20 VCCIO21 VCCIO22 VCCIO23 VCCIO24 VCCIO25 VCCIO26 VCCIO27 VCCIO28 VCCIO29 VCCIO30 VCCIO31 VCCIO32 VCCIO33 VCCIO34 VCCIO35 VCCIO36 VCCIO37 VCCIO38 VCCIO39 VCCIO40
AH13 AH10 AG10 AC10 Y10 U10 P10 L10 J14 J13 J12 J11 H14 H12 H11 G14 G13 G12 F14 F13 F12 F11 E14 E12 E11 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11 J23

SVID

+1.05VS
R46 75_0402_5%
VR_SVID_CLK series-resistors close to VR

VIDALERT# AJ29 H_CPU_SVIDALRT# R47 43_0402_5%
VIDSCLK AJ30 H_CPU_SVIDCLK R48 0_0402_5%
VIDSOUT AJ28 H_CPU_SVIDDAT R49 0_0402_5%
VR_SVID_ALRT# [53]
VR_SVID_CLK [53]
VR_SVID_DAT [53]
R50 130_0402_5% +1.05VS

VCC_SENCE 100ohm +-1% pull-up to VCC near processor

SENSE LINES

+CPU_CORE
R51 100_0402_1%
VCC_SENSE AJ35 VCCSENSE_R R52 0_0402_5%
VSS_SENSE AJ34 VSSSENSE_R R53 0_0402_5%
VCCSENSE [53]
VSSSENSE [53]
VCCIO_SENSE [51]
VCCIO_SENSE B10
VSSIO_SENSE A10 VSSIO_SENSE
R74 @ 0_0402_5%
R01
R54 100_0402_1%
8/6 Modify, need follow diffential routing

VSS_SENCE 100ohm +-1% pull-down to GND near processor

Sandy Bridge_rPGA_Rev1p0
ME@

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Title: PROCESSOR(5/7) PWR,BYPASS

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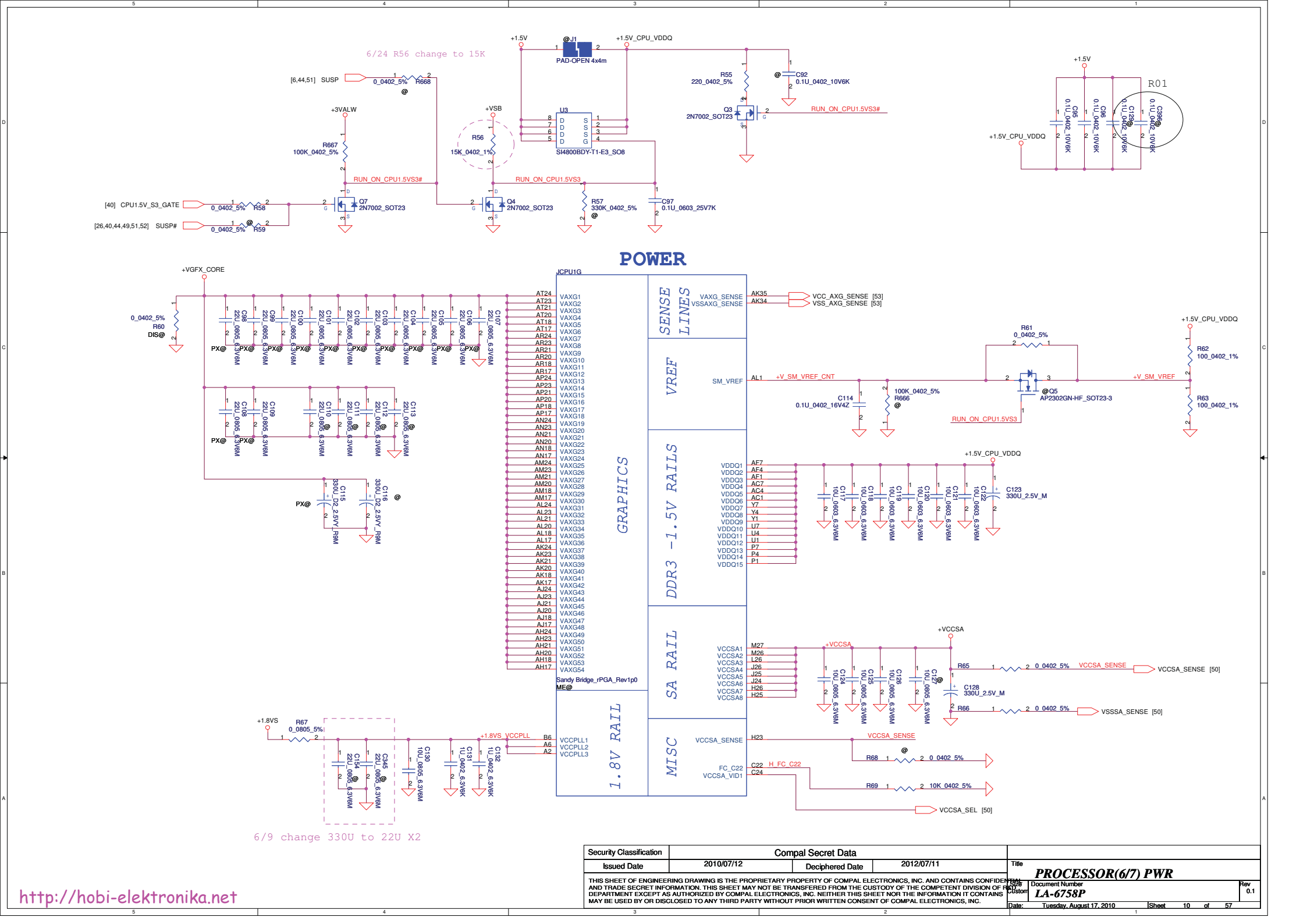

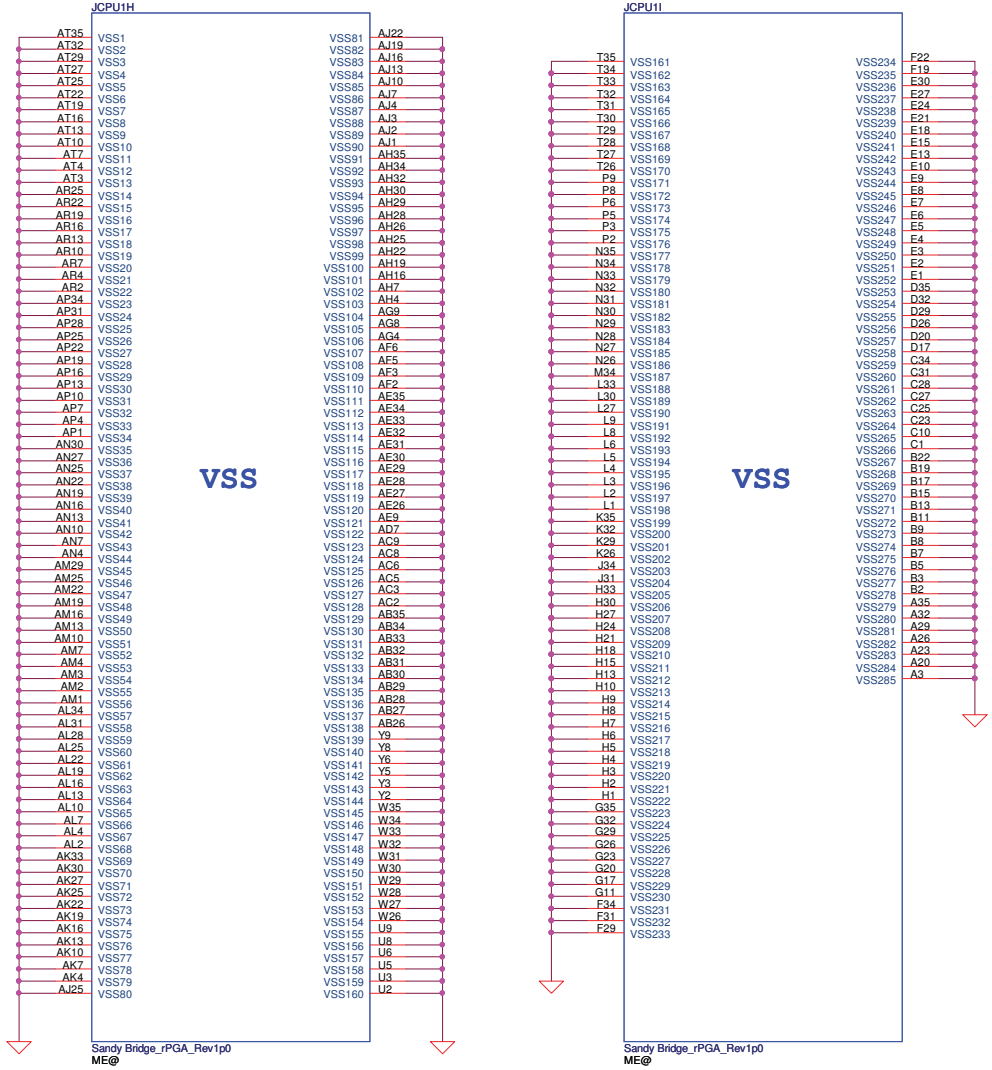

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Title: PROCESSOR(7/7) VSS

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DDR3 SO-DIMM A

JDIMM1

FOX_AS0A626-U4SN-7F

ME@

DDR_A_D[0..63]
DDR_A_DQS[0..7]
DDR_A_DQS#[0..7]
DDR_A_MA[0..15]

R70 1K_0402_1%
R71 1K_0402_1%
+VREF_DQ_DIMMA

C133 0.1U_0402_10V6K
C134 2.2U_0603_6.3V4Z

DDR3_DRAMRST# [7,13]

DDR_CKE0_DIMMA [7]
DDR_CKE1_DIMMA [7]
DDR_A_BS2 [7]
M_CLK_DDR0 [7]
M_CLK_DDR#0 [7]
DDR_A_BS0 [7]
DDR_A_WE# [7]
DDR_A_CAS# [7]
DDR_CS1_DIMMA# [7]

M_CLK_DDR1 [7]
M_CLK_DDR#1 [7]
DDR_A_BS1 [7]
DDR_A_RAS# [7]
DDR_CS0_DIMMA# [7]
M_ODT0 [7]
M_ODT1 [7]

R72 1K_0402_1%
R73 1K_0402_1%
+VREF_CA

C135 0.1U_0402_10V6K
C136 2.2U_0603_6.3V4Z

R81 10K_0402_5%
R83 10K_0402_5%
+3VS

C155 2.2U_0603_6.3V4Z
C156 0.1U_0402_10V6K

SMB_DATA_S3 [13,15,34]
SMB_CLK_S3 [13,15,34]
+0.75VS

0.65A@0.75V

VDDQ(1.5V) =
3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
6*0603 10uf (PER CONNECTOR)

VTT(0.75V) =
3*0805 10uf 4*0402 1uf

VREF =
1*0402 0.1uf 1*0402 2.2uf

VDDSPD (3.3V)=
1*0402 0.1uf 1*0402 2.2uf

Layout Note:
Place near DIMM

OSCAN (220uF_6.3V_4.2L_ESR17m)*1=(SF000002Y00)
(10uF_0603_6.3V)*8
(0.1uF_402_10V)*4

C137 @ 10U_0603_6.3V6M
C138 @ 10U_0603_6.3V6M
C139 10U_0603_6.3V6M
C140 10U_0603_6.3V6M
C141 10U_0603_6.3V6M
C142 10U_0603_6.3V6M
C143 10U_0603_6.3V6M
C144 10U_0603_6.3V6M
C145 0.1U_0402_10V6K
C146 0.1U_0402_10V6K
C147 0.1U_0402_10V6K
C148 0.1U_0402_10V6K
C149 220U_6.3V_M

Layout Note:
Place near DIMM

C150 C151 C152 C153 1U_0402_6.3V6K

7/28 Update connect GND directly

DDR_A_DM0
DDR_A_DM1
DDR_A_DM2
DDR_A_DM3
DDR_A_DM4
DDR_A_DM5
DDR_A_DM6
DDR_A_DM7

Layout Note:
Place near DIMM

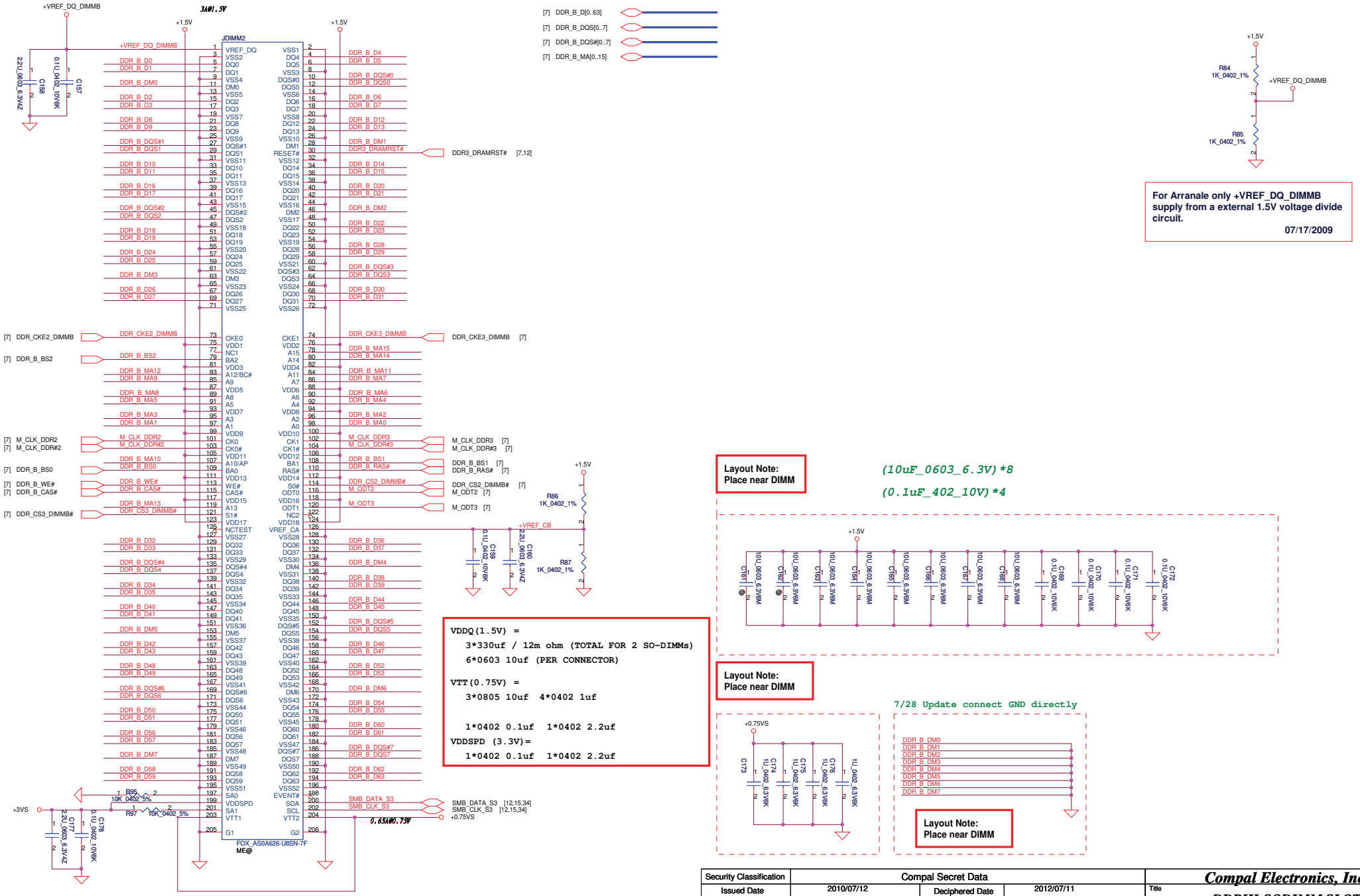
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT1

Size: Custom | Document Number: LA-6758P | Rev: 0.1

Date: Tuesday, August 17, 2010 | Sheet 12 of 57



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **DDRIII-SODIMM SLOT2**

Size	Document Number	Rev
	LA-6758P	0.1

Date: Tuesday, August 17, 2010 Sheet 13 of 57

W=20mils +RTCVCC R99 1K_0402_5% C179 1U_0603_10V4Z
W=20mils +RTCBATT CLRP1 SHORT PADS

PCH_RTCX1 R663 0_0402_5% PCH_RTCX1_OUT [40]
PCH_RTCX2 R670 0_0402_5% PCH_RTCX2_OUT [40]
R98 10M_0402_5%
6/24 Update R663,R670 must be close Y1
C180 18P_0402_50V8J
Y1 32.768KHZ_12.5PF_9H03200413
C181 18P_0402_50V8J
CMOS

+RTCVCC
R101 1M_0402_5% SM_INTRUDER#
R102 330K_0402_5% PCH_INTVRMEN
INTVRMEN
* H : Integrated VRM enable
L : Integrated VRM disable
(INTVRMEN should always be pull high.)

+3VS R105 1K_0402_5% HDA_SPKR
* HIGH= Enable (No Reboot)
LOW= Disable (Default)

+3VALW R106 1K_0402_5% HDA_SDOUT
* Low = Disabled (Default)
High = Enabled [Flash Descriptor Security Overide]

+3VALW R108 1K_0402_5% HDA_SYNC
This signal has a weak internal pull-down
* On Die PLL VR Select is supplied by
1.5V when smapled high
1.8V when sampled low
Needs to be pulled High for Huron River platfrom

[39] HDA_BITCLK_AUDIO R112 33_0402_5% HDA_BIT_CLK
[39] HDA_SYNC_AUDIO R114 33_0402_5% HDA_SYNC_R
[39] HDA_RST_AUDIO# R116 33_0402_5% HDA_RST#
[39] HDA_SDOUT_AUDIO R118 33_0402_5% HDA_SDOUT

+3VALW R121 200_0402_5% PCH_JTAG_TDO
+3VALW R122 200_0402_5% PCH_JTAG_TMS
+3VALW R123 200_0402_5% PCH_JTAG_TDI
R125 100_0402_1%
R126 100_0402_1%
R128 100_0402_1%
DPDG1.1
6/30 update R121, R122, R123

+3VS Q10 BSS138_NL_SOT23-3 HDA_SYNC
@R325 0_0402_5%
6/17 follow module design

+RTCVCC C183 1U_0603_10V4Z R103 20K_0402_5% R100 20K_0402_5% C182 1U_0603_10V4Z
CLRP2 SHORT PADS CLRP3 SHORT PADS

U4A

PCH_RTCX1	A20	RTCX1	RTC	
PCH_RTCX2	C20	RTCX2		
PCH_RTCRST#	D20	RTCRST#		
PCH_SRTCRST#	G22	SRTCRST#		
SM_INTRUDER#	K22	INTRUDER#		
PCH_INTVRMEN	C17	INTVRMEN		
HDA_BIT_CLK	N34	HDA_BCLK	IHDA	
HDA_SYNC	L34	HDA_SYNC		
HDA_SPKR	T10	SPKR		
HDA_RST#	K34	HDA_RST#		
HDA_SDIN0	E34	HDA_SDIN0		
	G34	HDA_SDIN1		
	C34	HDA_SDIN2		
	A34	HDA_SDIN3		
ME_FLASH R109 0_0402_5% HDA_SDOUT	A36	HDA_SDO		
R107 1K_0402_1% PCH_GPIO33	C36	HDA_DOCK_EN# / GPIO33		
Kill_SW#	N32	HDA_DOCK_RST# / GPIO13		
PCH_JTAG_TCK	J3	JTAG_TCK	JTAG	
PCH_JTAG_TMS	H7	JTAG_TMS		
PCH_JTAG_TDI	K5	JTAG_TDI		
PCH_JTAG_TDO	H1	JTAG_TDO		
SPI_CLK_PCH_R	T3	SPI_CLK	SPI	
SPI_SB_CS0#	Y14	SPI_CS0#		
	T1	SPI_CS1#		
SPI_SI	V4	SPI_MOSI		
SPI_SO_R	U3	SPI_MISO		

R110 51_0402_5%

COUGARPOINT_FCBGA989

FWH0 / LAD0	C38	LPC_AD0	LPC	LPC_AD0 [34,40]
FWH1 / LAD1	A38	LPC_AD1		LPC_AD1 [34,40]
FWH2 / LAD2	B37	LPC_AD2		LPC_AD2 [34,40]
FWH3 / LAD3	C37	LPC_AD3		LPC_AD3 [34,40]
FWH4 / LFRAME#	D36	LPC_FRAME#		LPC_FRAME# [34,40]
LDRQ0#	E36			
LDRQ1# / GPIO23	K36			
SERIRQ	V5	SERIRQ		SERIRQ [40]
SATA0RXN	AM3	SATA_DTX_C_IRX_N0	SATA 6G	SATA_DTX_C_IRX_N0 [38]
SATA0RXP	AM1	SATA_DTX_C_IRX_P0		SATA_DTX_C_IRX_P0 [38]
SATA0TXN	AP7	SATA_ITX_C_DRX_N0 0.01U_0402_16V7K C184		SATA_ITX_DRX_N0 SATA_ITX_DRX_N0 [38]
SATA0TXP	AP5	SATA_ITX_C_DRX_P0 0.01U_0402_16V7K C185		SATA_ITX_DRX_P0 SATA_ITX_DRX_P0 [38]
SATA1RXN	AM10			
SATA1RXP	AM8			
SATA1TXN	AP11			
SATA1TXP	AP10			
SATA2RXN	AD7	SATA_DTX_C_IRX_N2		SATA_DTX_C_IRX_N2 [56]
SATA2RXP	AD5	SATA_DTX_C_IRX_P2		SATA_DTX_C_IRX_P2 [56]
SATA2TXN	AH5	SATA_ITX_C_DRX_N2 0.01U_0402_16V7K C186		SATA_ITX_DRX_N2_CONN SATA_ITX_DRX_N2_CONN [56]
SATA2TXP	AH4	SATA_ITX_C_DRX_P2 0.01U_0402_16V7K C187		SATA_ITX_DRX_P2_CONN SATA_ITX_DRX_P2_CONN [56]
SATA3RXN	AB8			
SATA3RXP	AB10			
SATA3TXN	AF3			
SATA3TXP	AF1			
SATA4RXN	Y7	SATA_DTX_C_IRX_N4		SATA_DTX_C_IRX_N4 [42]
SATA4RXP	Y5	SATA_DTX_C_IRX_P4		SATA_DTX_C_IRX_P4 [42]
SATA4TXN	AD3	SATA_ITX_C_DRX_N4 ESATA@ 0.01U_0402_16V7K C188		SATA_ITX_DRX_N4 SATA_ITX_DRX_N4 [42]
SATA4TXP	AD1	SATA_ITX_C_DRX_P4 ESATA@ 0.01U_0402_16V7K C189		SATA_ITX_DRX_P4 SATA_ITX_DRX_P4 [42]
SATA5RXN	Y3			
SATA5RXP	Y1			
SATA5TXN	AB3			
SATA5TXP	AB1			
SATAICOMPO	Y11	R111 37.4_0402_1% +1.05VS_VCC_SATA		
SATAICOMPI	Y10	SATA_COMP		
SATA3RCOMPO	AB12	R113 49.9_0402_1% +1.05VS_SATA3		
SATA3COMPI	AB13	SATA3_COMP		
SATA3RBIAS	AH1	RBIAS_SATA3 R115 750_0402_1%		
SATALED#	P3	R117 10K_0402_5% +3VS HDD_LED#		HDD_LED# [56]
SATA0GP / GPIO21	V14	PCH_GPIO21 R119 10K_0402_5% +3VS		
SATA1GP / GPIO19	P1	PCH_GPIO19		

EC and Mini card debug port
+3VS R104 10K_0402_5% SERIRQ
HDD
ODD
ESATA R01
7/28 change from port 5 to port 4

4MB SPI ROM FOR ME & Non-share ROM.

+3VS R127 3.3K_0402_5% SPI_WP#
R129 3.3K_0402_5% SPI_HOLD#
SPI_CLK_PCH R124 33_0402_5% @ C190 22P_0402_50V8J @
+3VS C191 0.1U_0402_16V4Z
R130 0_0402_5% SPI_SO_R
SPI_SB_CS0# SPI_SO_L SPI_WP# R131 33_0402_5%
U5 S IC FL 32M W25Q32BVSSIG SOIC 8P
CS# SO WP# GND VCC HOLD# SCLK SI
SPI_HOLD# 0_0402_5% R132 SPI_CLK_PCH SPI_SI_R R133 33_0402_5%
SPI_CLK_PCH_R SPI_SI

Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

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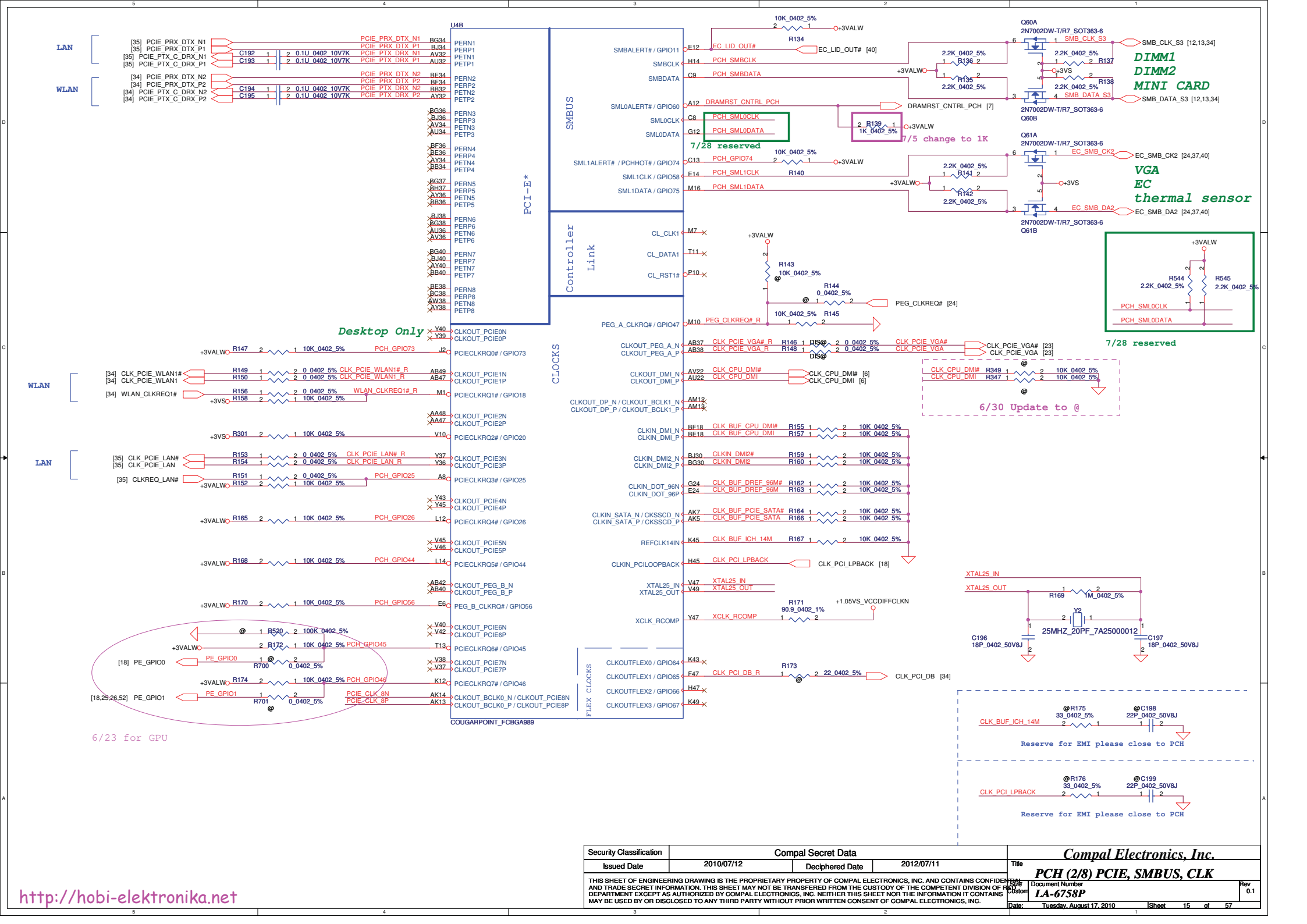
Compal Electronics, Inc.
Title: PCH (1/8) SATA,HDA,SPI, LPC, XDP
Size: Custom | Document Number: LA-6758P | Rev: 0.1
Date: Tuesday, August 17, 2010 | Sheet 14 of 57



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Issued Date	2010/07/12	Deciphered Date	2012/07/11

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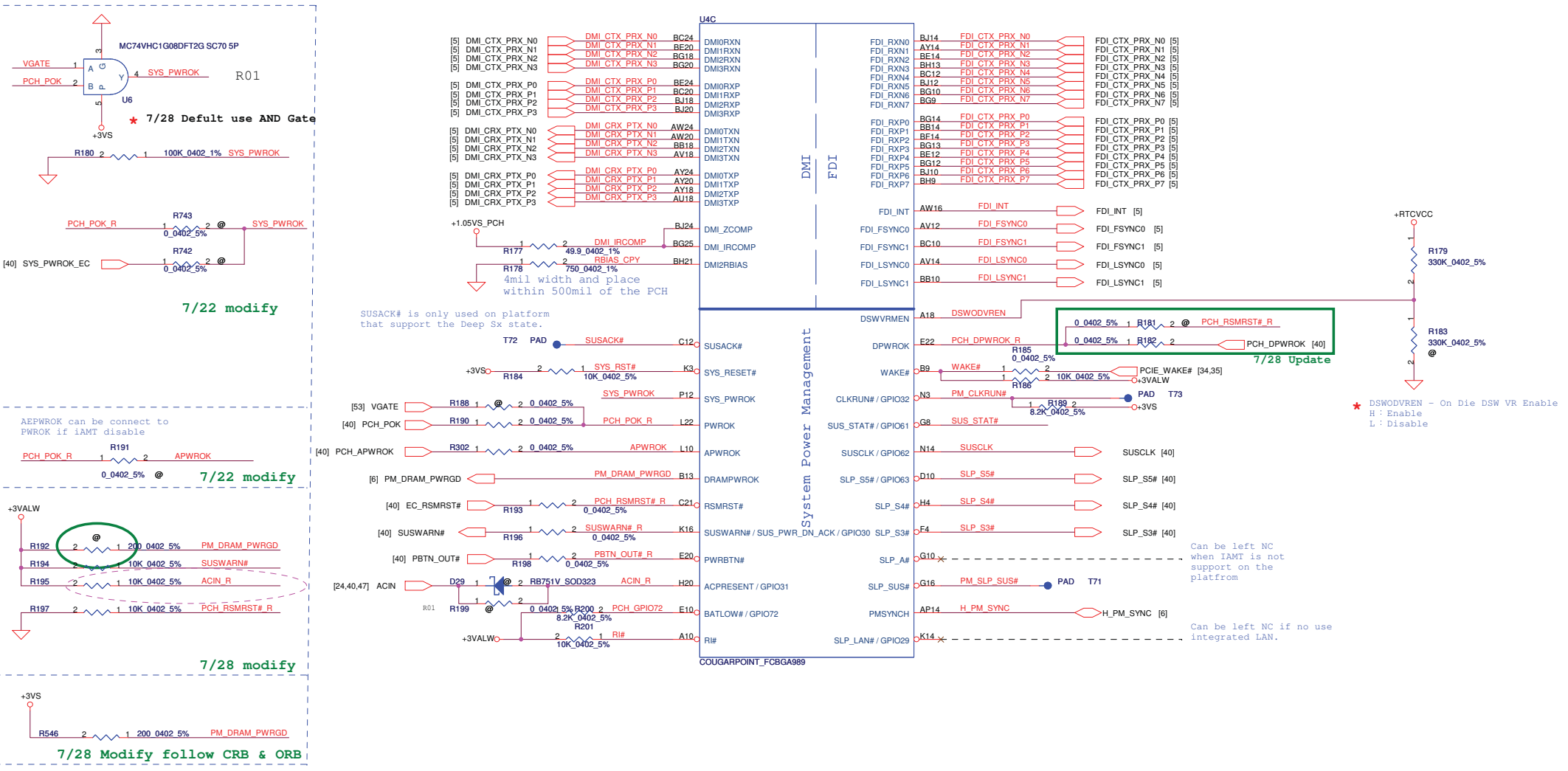
Compal Electronics, Inc.

Title: PCH (2/8) PCIE, SMBUS, CLK

Size	Document Number	Rev
Custom	LA-6758P	0.1

Date: Tuesday, August 17, 2010 Sheet 15 of 57



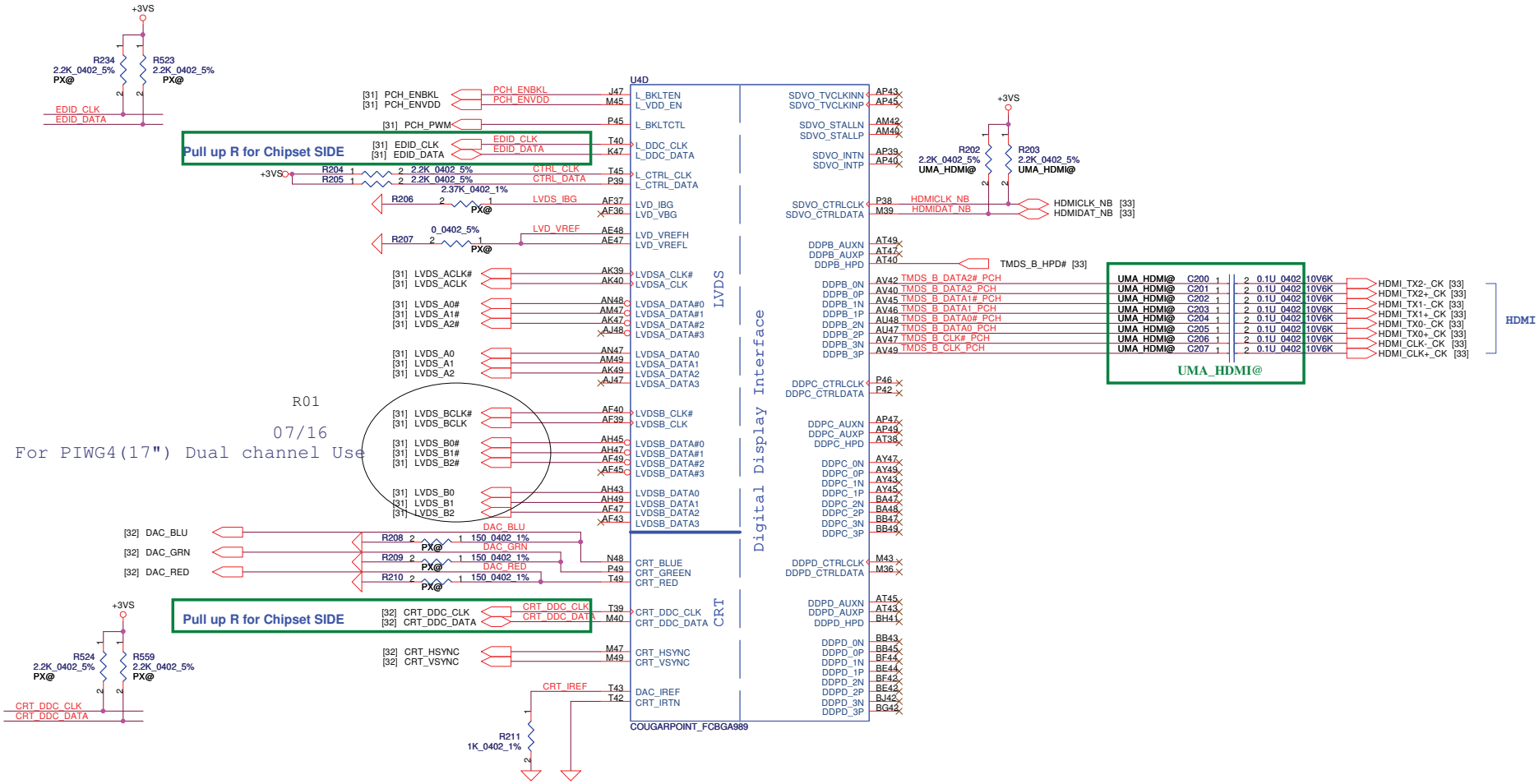
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (3/8) DMI,FDI,PM,

Size: Custom | Document Number: LA-6758P | Rev: 0.1

Date: Tuesday, August 17, 2010 | Sheet 16 of 57



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

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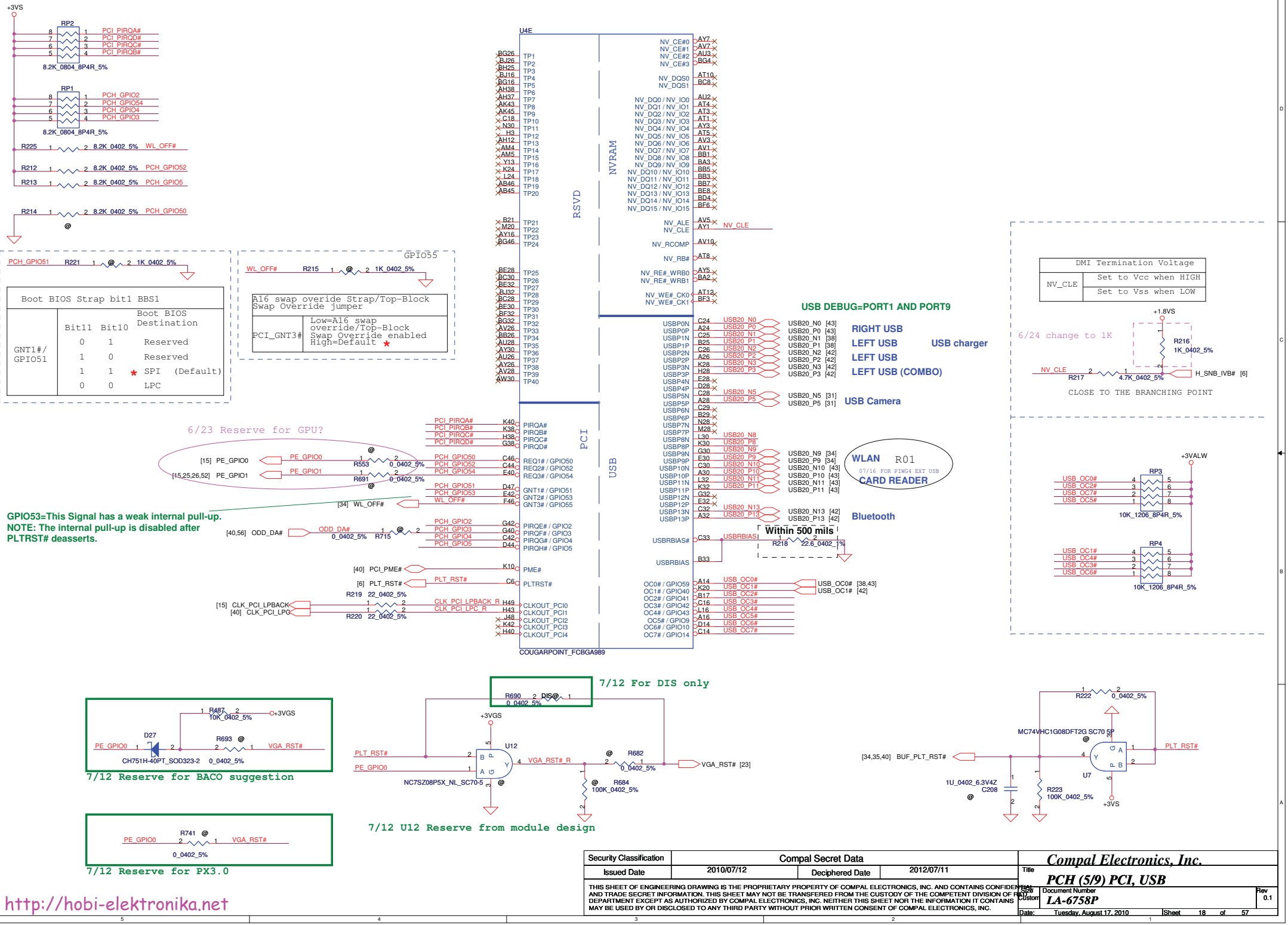
Compal Electronics, Inc.

Title: PCH (4/9) LVDS,CRT,DP,HDMI

Size: Custom | Document Number: LA-6758P | Rev: 0.1

Date: Tuesday, August 17, 2010 | Sheet 17 of 57



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

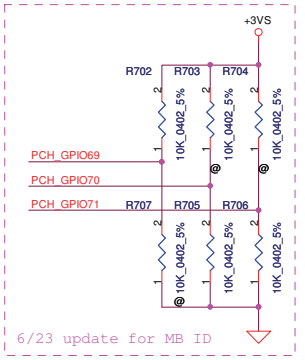
Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB

Size: Custom | Document Number: LA-6758P | Rev: 0.1

Date: Tuesday, August 17, 2010 | Sheet 18 of 57

PCH_GPIO69	PCH_GPIO70	PCH_GPIO71	Function
0	0	0	UMA
1	0	0	DIS *
0	1	0	PX3.0
1	1	0	PX4.0



ICC_EN#
Integrated Clock Chip Enable
H ; Disable
L ; Enable
R235 1 @ 2 1K_0402_5% EC_SMI#
Weak internal pull-high

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable
R240 1 @ 2 1K_0402_5% PCH_GPIO28

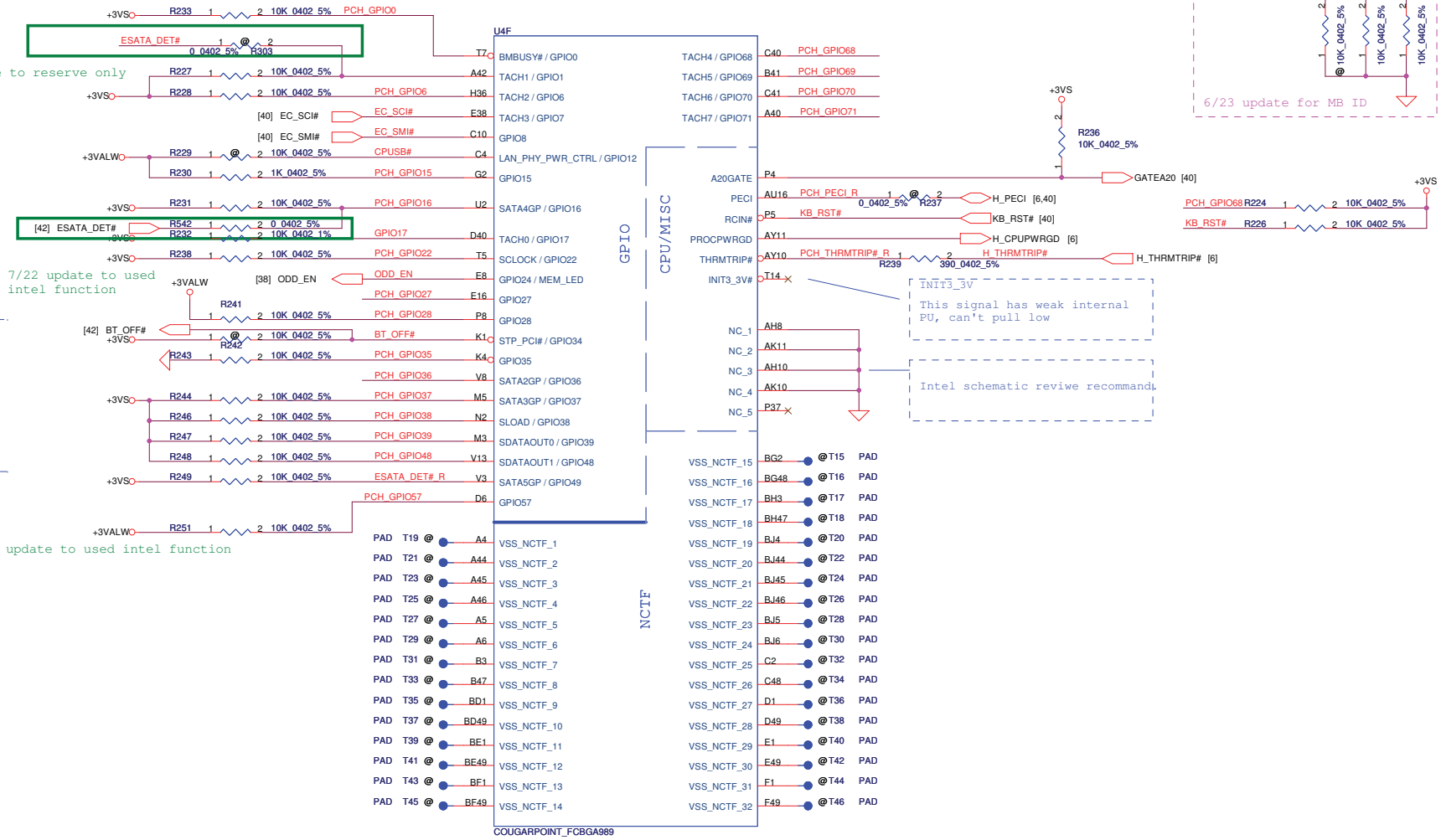
PCH_GPIO27 (Have internal Pull-High)
High: VCCVRM VR Enable
Low: VCCVRM VR Disable
R245 1 @ 2 10K_0402_5% PCH_GPIO27

+3VS R250 1 @ 2 10K_0402_5% PCH_GPIO36
1 R547 2 10K_0402_5%
R01

7/22 update to reserve only

7/22 update to used intel function

7/22 update to used intel function



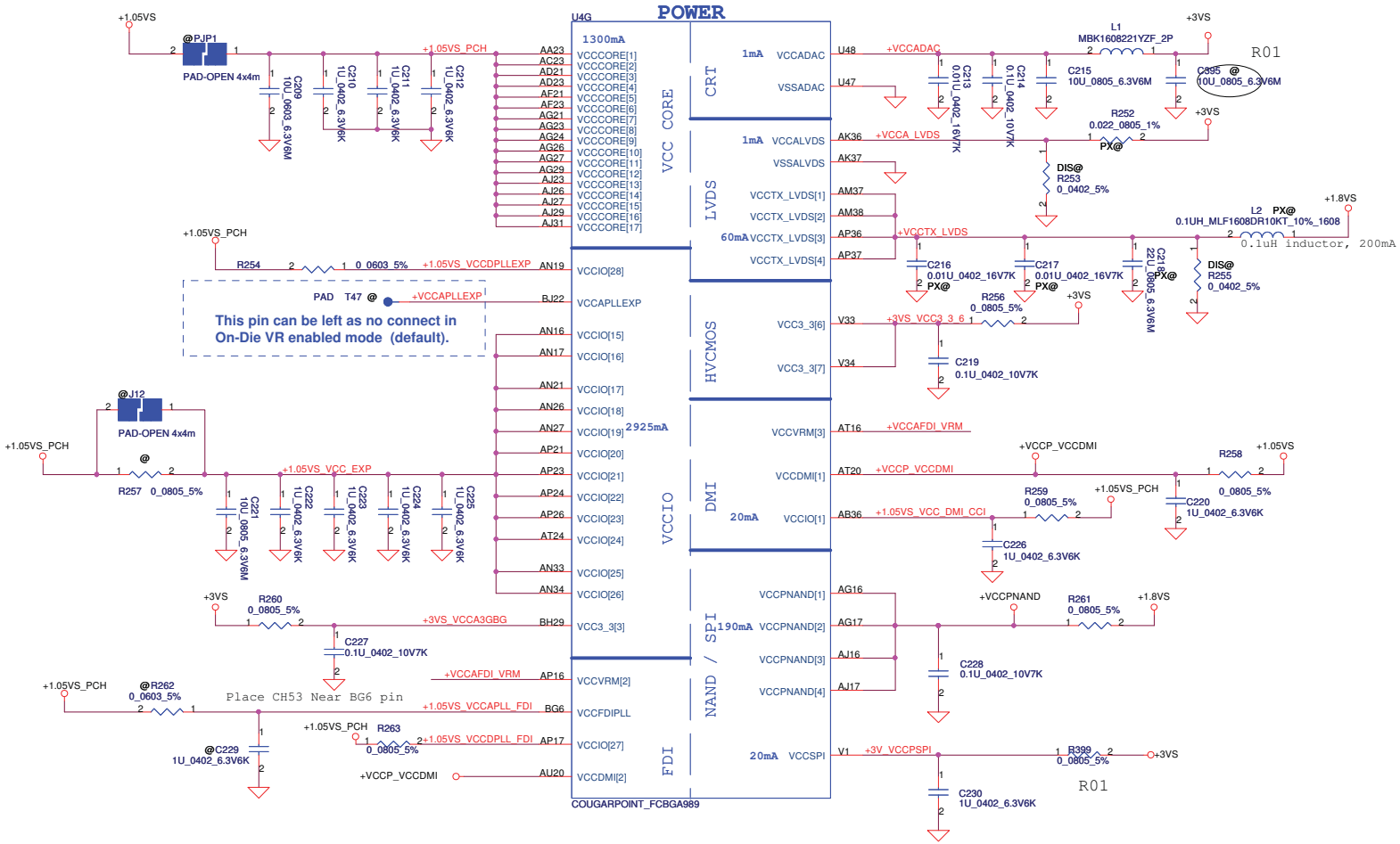
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

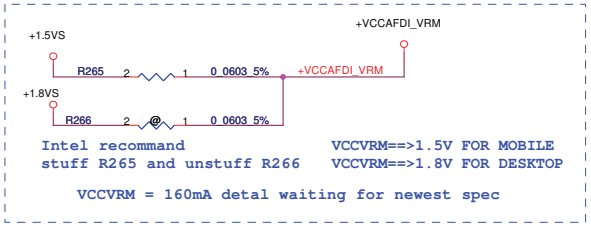
Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

Size: Custom | Document Number: LA-6758P | Rev: 0.1

Date: Tuesday, August 17, 2010 | Sheet 19 of 57





PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

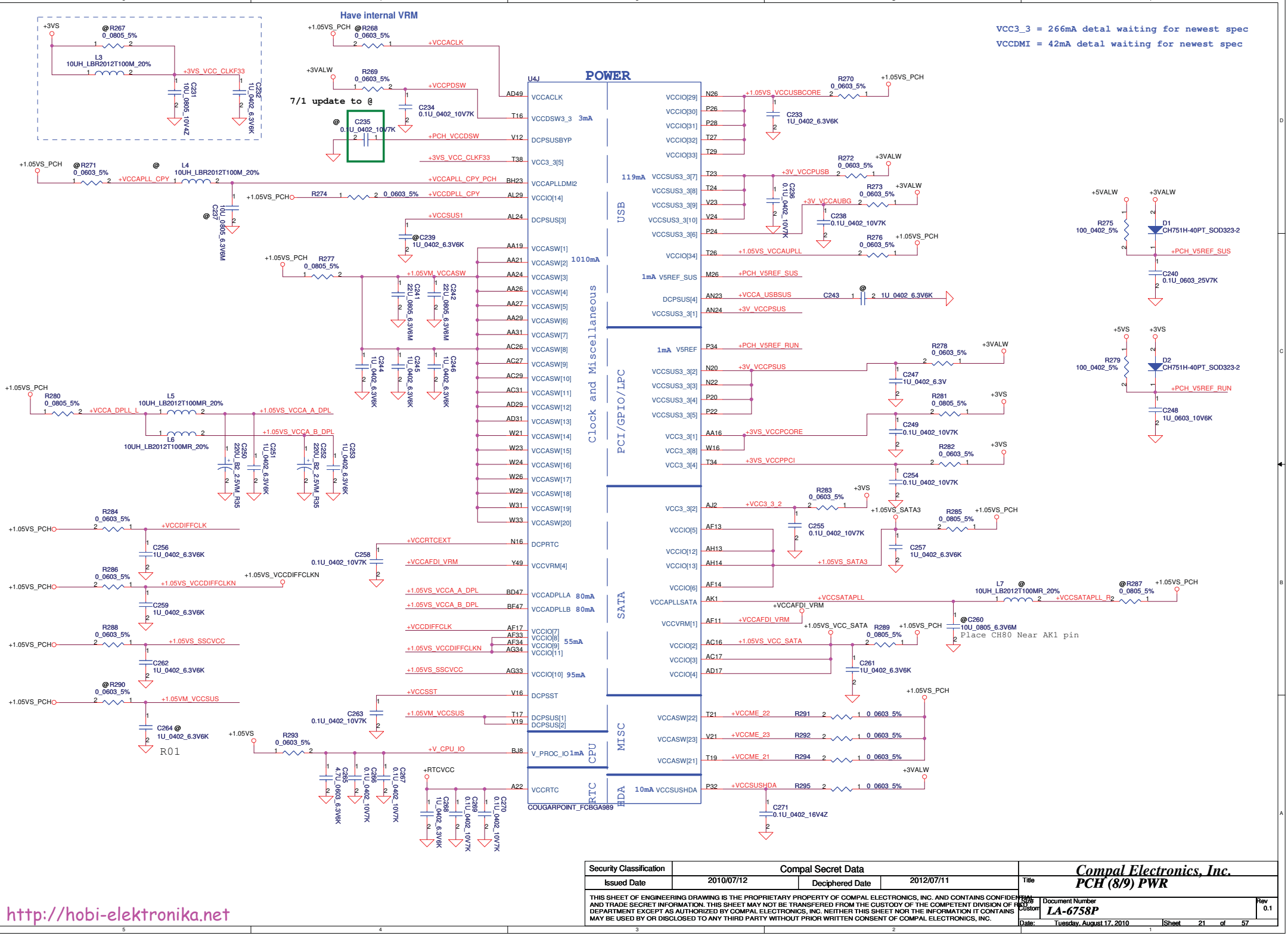
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (7/9) PWR

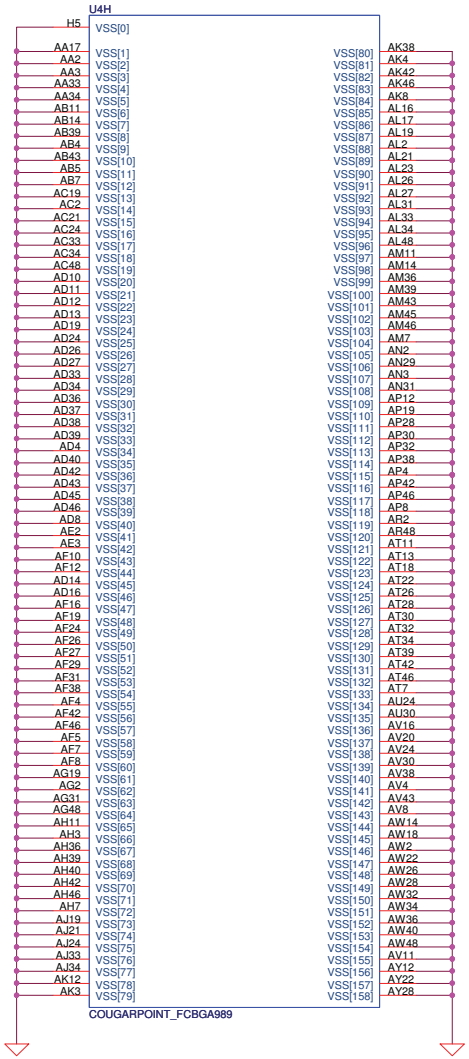
Size: Custom | Document Number: LA-6758P | Rev: 0.1

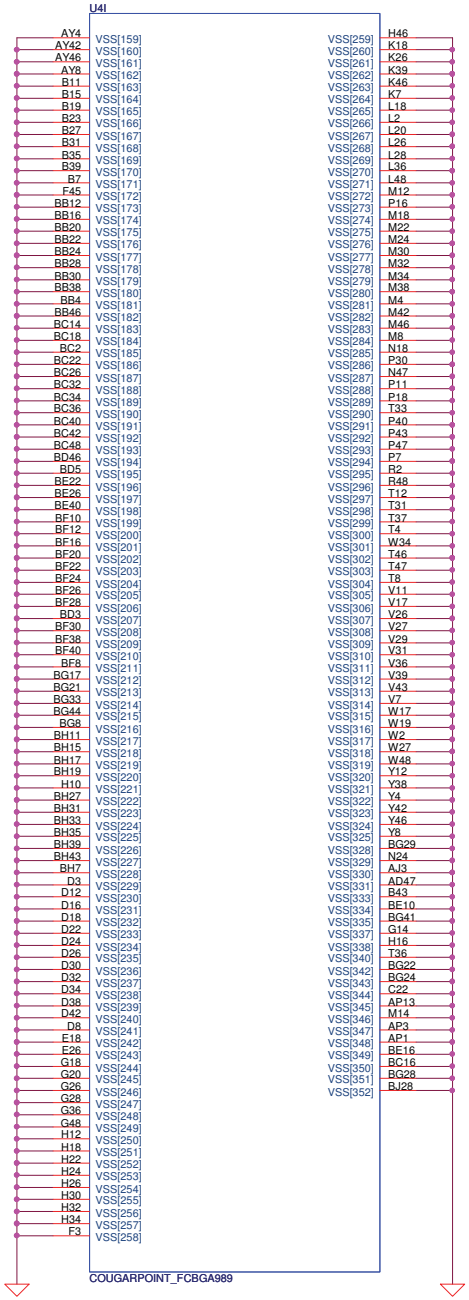
Date: Tuesday, August 17, 2010 | Sheet 20 of 57



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

Compal Electronics, Inc.			
Title: PCH (8/9) PWR			
Size: Custom	Document Number: LA-6758P		Rev: 0.1
Date: Tuesday, August 17, 2010	Sheet 21 of 57		





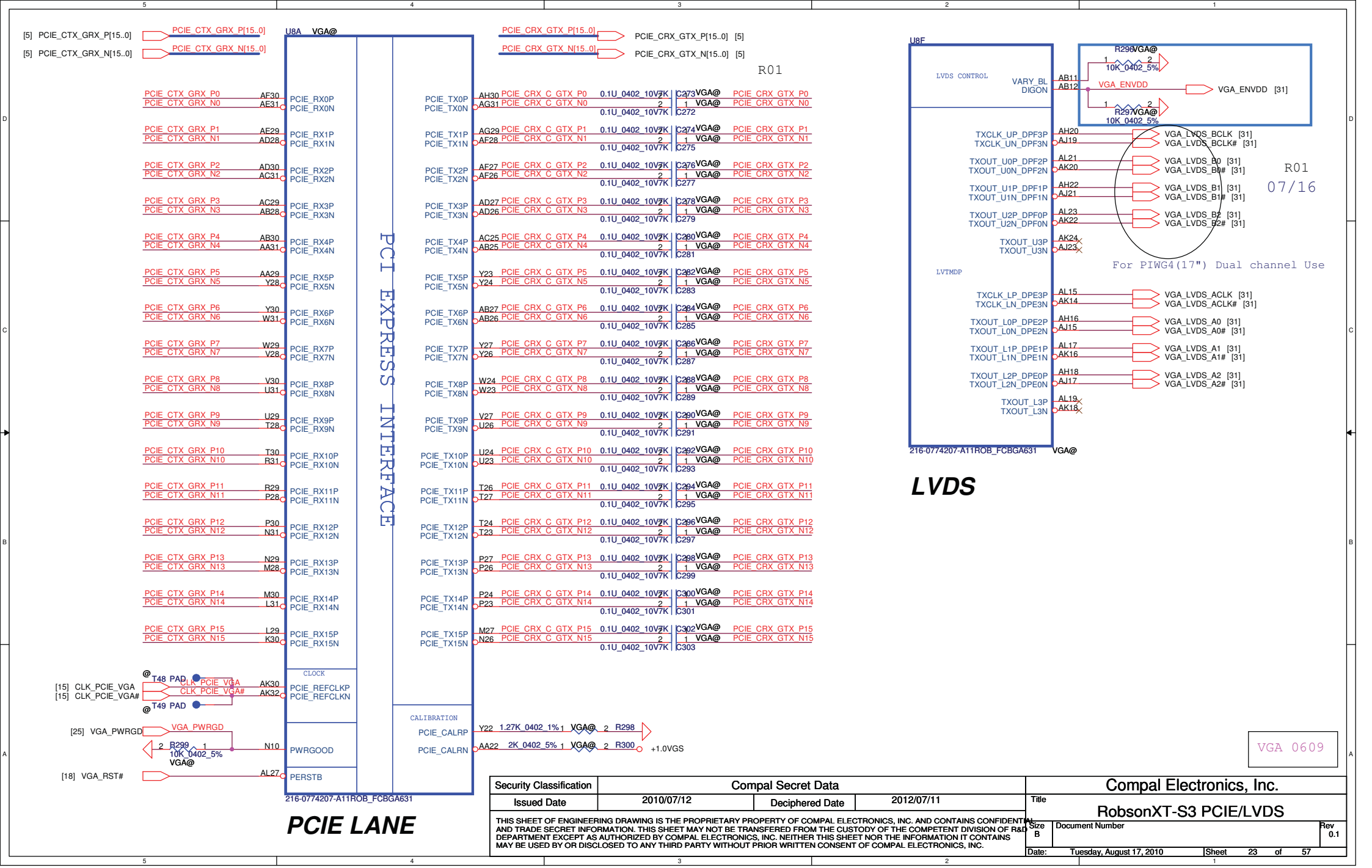
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (9/9) VSS

Size: Custom | Document Number: LA-6758P | Rev: 0.1

Date: Tuesday, August 17, 2010 | Sheet 22 of 57



TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Defailt setting for desktop)

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XXX
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD	H2SYNC		0
RSVD	GENERICC		0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

GPIO21	H2SYNC	GENERICC	GPIO2	GPIO8

STRAPS

VGA Thermal Sensor EMC1402-1

Closed to GPU

EMC1412-A (SA00003YA00)
Address 1111_100xb
S IC EMC1412-A-AC2L-TR MSOP 8P SENSOR

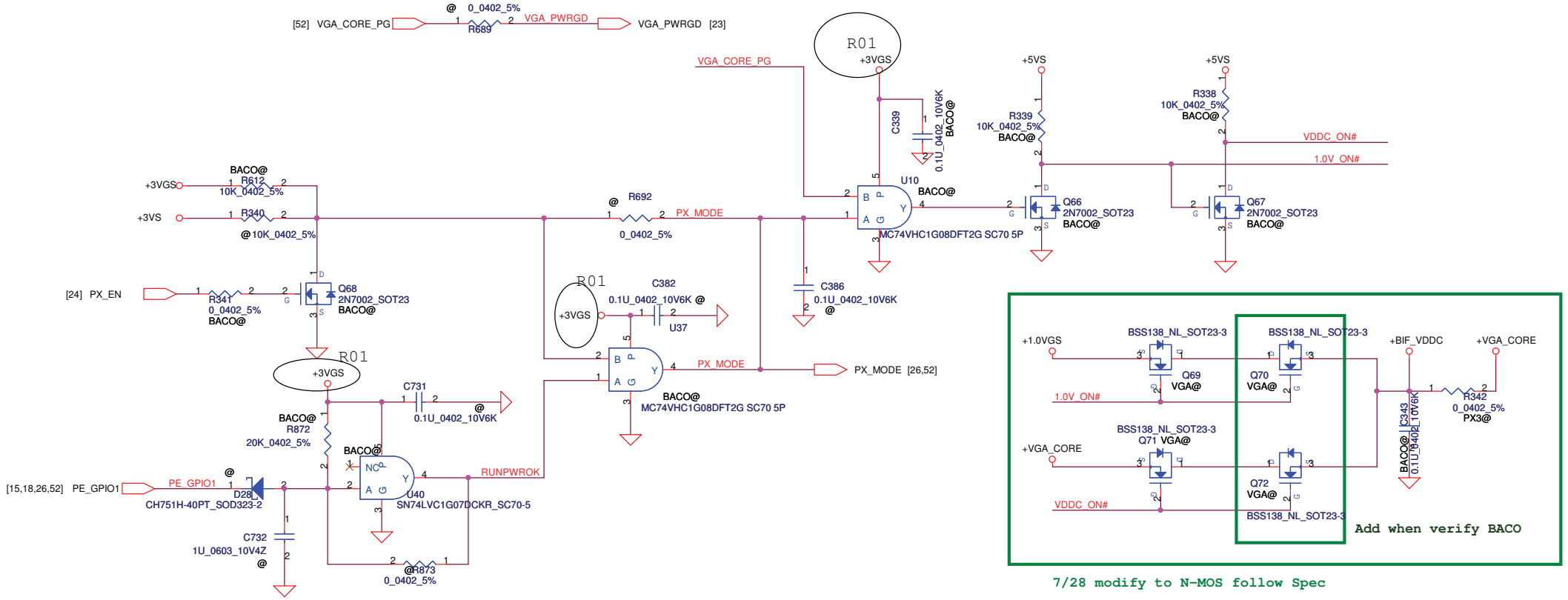
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: RobsonXT-S3 Main Generic/MSIC

Size	Document Number	Rev
C		0.1

Date: Tuesday, August 17, 2010 | Sheet 24 of 57



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

Compal Electronics, Inc.

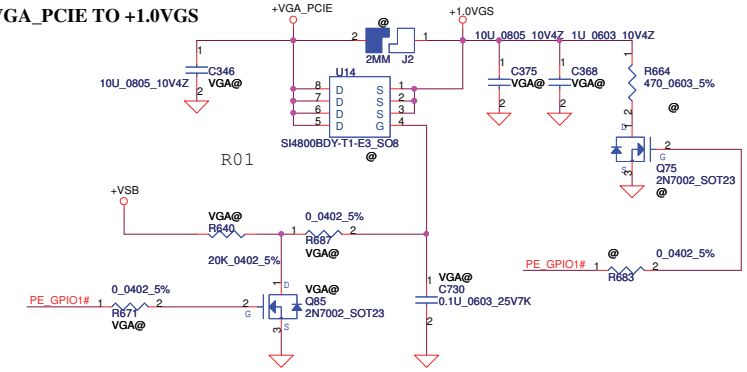
Title: PARK-S3 Main Generic/MSIC

Size	Document Number	Rev
B	LA-6758P	0.1

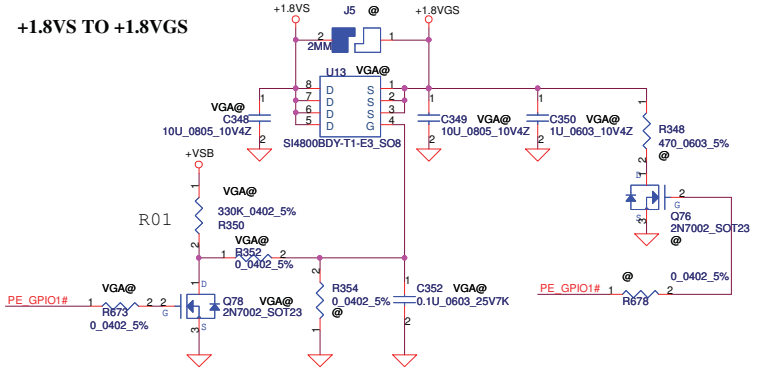
Date: Tuesday, August 17, 2010 Sheet 25 of 57

EVT Short J2 for DIS only

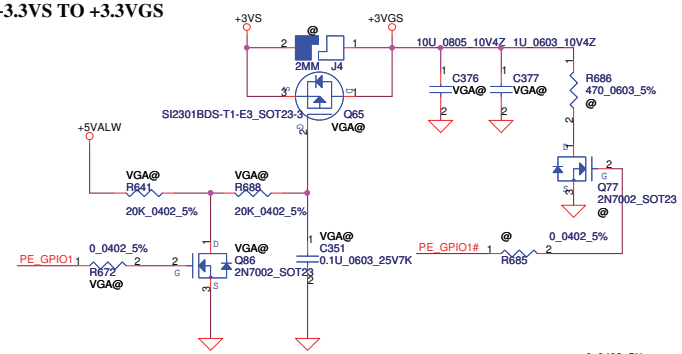
+VGA_PCIE TO +1.0VGS



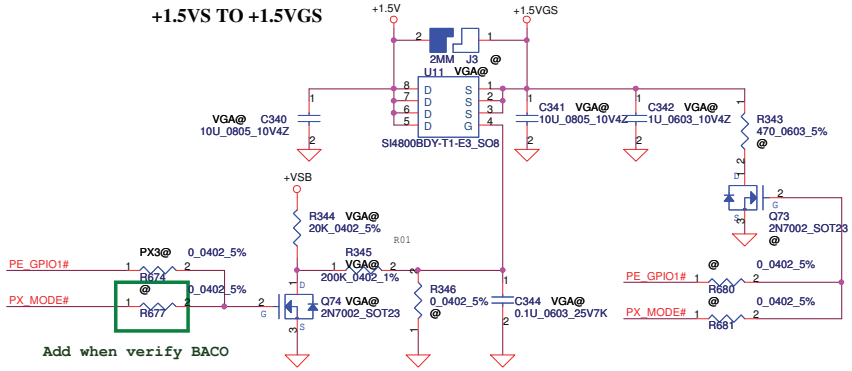
+1.8VS TO +1.8VGS



+3.3VS TO +3.3VGS

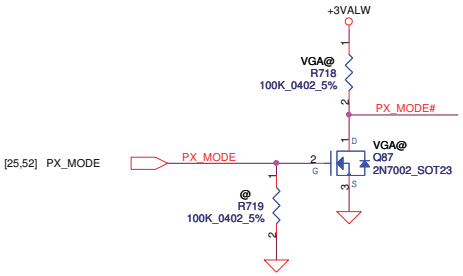


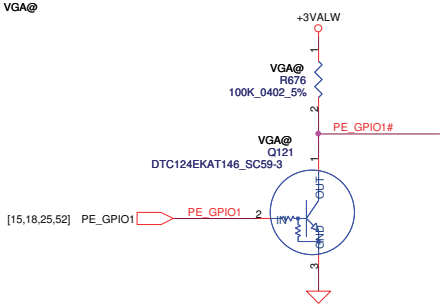
+1.5VS TO +1.5VGS



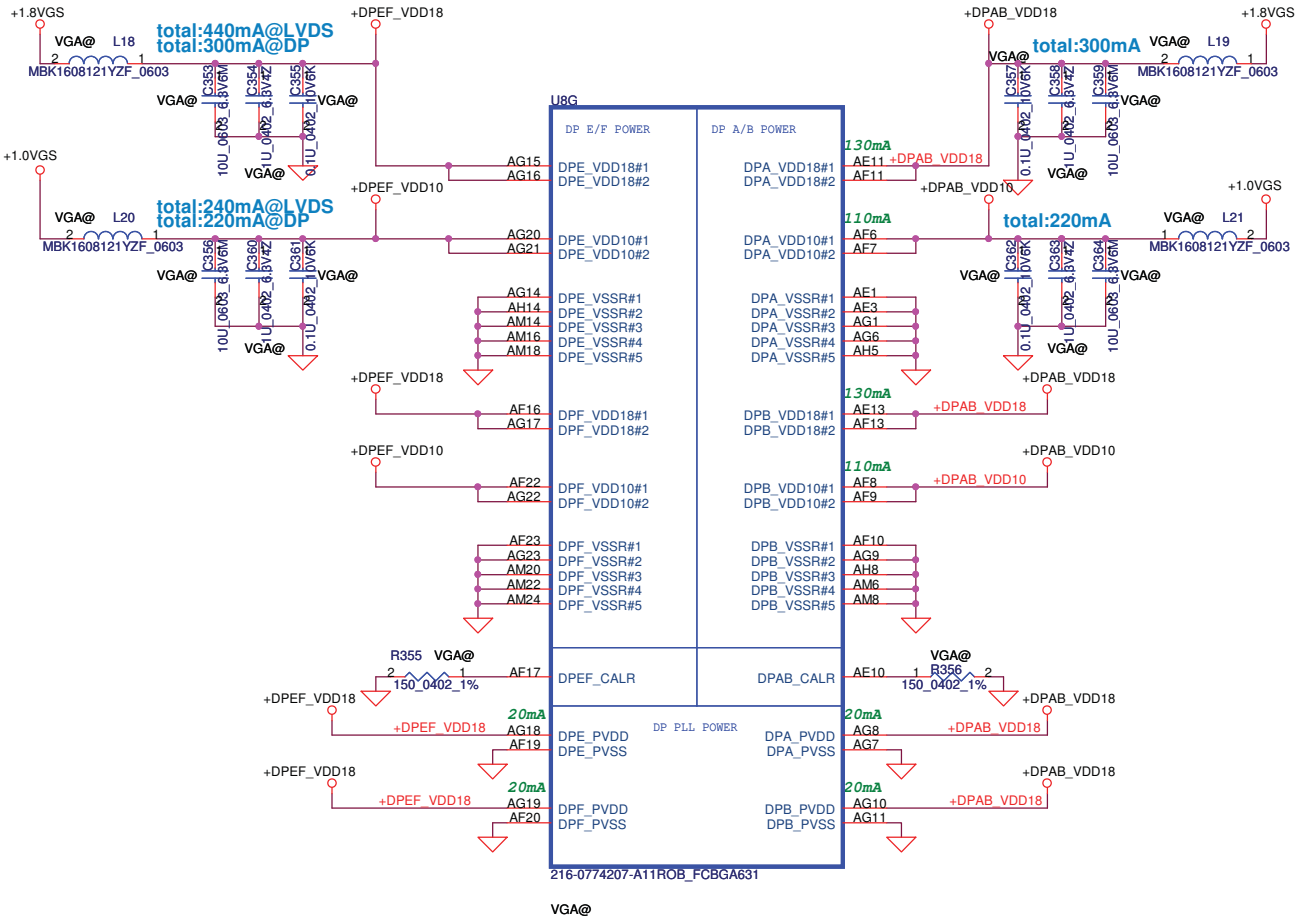
Add when verify BACO

[10,40,44,49,51,52] SUSP# — 0_0402_5% R744 VGA@ — PE_GPIO1





Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2010/07/12	Deciphered Date 2012/07/11	Title: PARK-S3 Main Generic/MSIC
Size: Custom	Document Number: LA-6758P		Rev: 0.1
Date: Tuesday, August 17, 2010	Sheet 26 of 57		



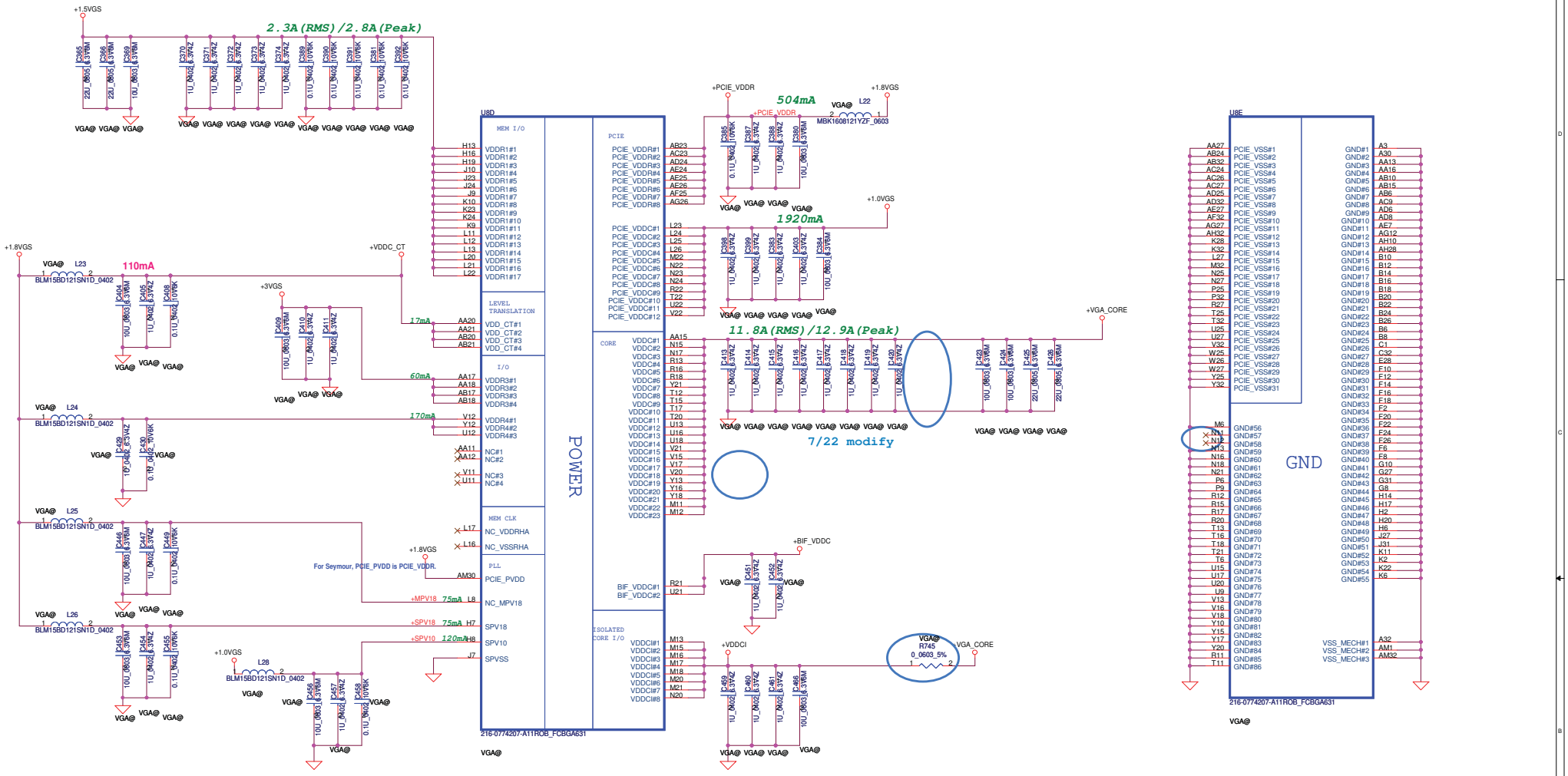
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: RobsonXT-S3 DP PWR

Size	Document Number	Rev
B		0.1

Date: Tuesday, August 17, 2010 Sheet 27 of 57



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: RobsonXT-S3 PWR/GND

Size	Document Number	Rev
C		0.1

Date: Tuesday, August 17, 2010 Sheet 28 of 57

[30] M_DA[63..0] — M_DA[63..0]
[30] M_MA[13..0] — M_MA[13..0]
[30] M_DQM[7..0] — M_DQM[7..0]
[30] M_DQS[7..0] — M_DQS[7..0]
[30] M_DQS#[7..0] — M_DQS#[7..0]

U8C

GDDR5/DDR3 | GDDR5/DDR3

MEMORY INTERFACE

M_DA0	K27	DQA0_0/DQA_0	MAA0_0/MAA_0	K17	M_MA0
M_DA1	J29	DQA0_1/DQA_1	MAA0_1/MAA_1	J20	M_MA1
M_DA2	H30	DQA0_2/DQA_2	MAA0_2/MAA_2	H23	M_MA2
M_DA3	H32	DQA0_3/DQA_3	MAA0_3/MAA_3	G23	M_MA3
M_DA4	G29	DQA0_4/DQA_4	MAA0_4/MAA_4	G24	M_MA4
M_DA5	F28	DQA0_5/DQA_5	MAA0_5/MAA_5	H24	M_MA5
M_DA6	F32	DQA0_6/DQA_6	MAA0_6/MAA0_6	J19	M_MA6
M_DA7	F30	DQA0_7/DQA_7	MAA0_7/MAA0_7	K19	M_MA7
M_DA8	C30	DQA0_8/DQA_8	MAA1_0/MAA_8	J14	M_MA8
M_DA9	F27	DQA0_9/DQA_9	MAA1_1/MAA_9	K14	M_MA9
M_DA10	A28	DQA0_10/DQA_10	MAA1_2/MAA_10	J11	M_MA10
M_DA11	C28	DQA0_11/DQA_11	MAA1_3/MAA_11	J13	M_MA11
M_DA12	E27	DQA0_12/DQA_12	MAA1_4/MAA_12	H11	M_MA12
M_DA13	G26	DQA0_13/DQA_13	MAA1_5/MAA_13/BA2	G11	M_BA2 → M_BA2 [30]
M_DA14	D26	DQA0_14/DQA_14	MAA1_6/MAA_14/BA0	J16	M_BA0 → M_BA0 [30]
M_DA15	F25	DQA0_15/DQA_15	MAA1_7/MAA_15/BA1	L15	M_BA1 → M_BA1 [30]
M_DA16	A25	DQA0_16/DQA_16			
M_DA17	C25	DQA0_17/DQA_17	WCKA0_0/DQMA_0	E32	M_DQM0
M_DA18	E25	DQA0_18/DQA_18	WCKA0B_0/DQMA_1	E30	M_DQM1
M_DA19	D24	DQA0_19/DQA_19	WCKA0_1/DQMA_2	A21	M_DQM2
M_DA20	E23	DQA0_20/DQA_20	WCKA0B_1/DQMA_3	C21	M_DQM3
M_DA21	F23	DQA0_21/DQA_21	WCKA1_0/DQMA_4	E13	M_DQM4
M_DA22	D22	DQA0_22/DQA_22	WCKA1B_0/DQMA_5	D12	M_DQM5
M_DA23	F21	DQA0_23/DQA_23	WCKA1_1/DQMA_6	E3	M_DQM6
M_DA24	E21	DQA0_24/DQA_24	WCKA1B_1/DQMA_7	F4	M_DQM7
M_DA25	D20	DQA0_25/DQA_25			
M_DA26	F19	DQA0_26/DQA_26	EDCA0_0/RDQSA_0	H28	M_DQS0
M_DA27	A19	DQA0_27/DQA_27	EDCA0_1/RDQSA_1	C27	M_DQS1
M_DA28	D18	DQA0_28/DQA_28	EDCA0_2/RDQSA_2	A23	M_DQS2
M_DA29	F17	DQA0_29/DQA_29	EDCA0_3/RDQSA_3	E19	M_DQS3
M_DA30	A17	DQA0_30/DQA_30	EDCA1_0/RDQSA_4	E15	M_DQS4
M_DA31	C17	DQA0_31/DQA_31	EDCA1_1/RDQSA_5	D10	M_DQS5
M_DA32	E17	DQA1_0/DQA_32	EDCA1_2/RDQSA_6	D6	M_DQS6
M_DA33	D16	DQA1_1/DQA_33	EDCA1_3/RDQSA_7	G5	M_DQS7
M_DA34	F15	DQA1_2/DQA_34			
M_DA35	A15	DQA1_3/DQA_35	DDBIA0_0/WDQSA_0	H27	M_DQS#0
M_DA36	D14	DQA1_4/DQA_36	DDBIA0_1/WDQSA_1	A27	M_DQS#1
M_DA37	F13	DQA1_5/DQA_37	DDBIA0_2/WDQSA_2	C23	M_DQS#2
M_DA38	A13	DQA1_6/DQA_38	DDBIA0_3/WDQSA_3	C19	M_DQS#3
M_DA39	C13	DQA1_7/DQA_39	DDBIA1_0/WDQSA_4	C15	M_DQS#4
M_DA40	E11	DQA1_8/DQA_40	DDBIA1_1/WDQSA_5	E9	M_DQS#5
M_DA41	A11	DQA1_9/DQA_41	DDBIA1_2/WDQSA_6	C5	M_DQS#6
M_DA42	C11	DQA1_10/DQA_42	DDBIA1_3/WDQSA_7	H4	M_DQS#7
M_DA43	F11	DQA1_11/DQA_43			
M_DA44	A9	DQA1_12/DQA_44	ADBIA0/ODTA0	L18	VRAM_ODT0 → VRAM_ODT0 [30]
M_DA45	C9	DQA1_13/DQA_45	ADBIA1/ODTA1	K16	VRAM_ODT1 → VRAM_ODT1 [30]
M_DA46	F9	DQA1_14/DQA_46			
M_DA47	D8	DQA1_15/DQA_47	CLKA0	H26	M_CLK0 → M_CLK0 [30]
M_DA48	E7	DQA1_16/DQA_48	CLKA0B	H25	M_CLK#0 → M_CLK#0 [30]
M_DA49	A7	DQA1_17/DQA_49			
M_DA50	C7	DQA1_18/DQA_50	CLKA1	G9	M_CLK1 → M_CLK1 [30]
M_DA51	F7	DQA1_19/DQA_51	CLKA1B	H9	M_CLK#1 → M_CLK#1 [30]
M_DA52	A5	DQA1_20/DQA_52			
M_DA53	E5	DQA1_21/DQA_53	RASA0B	G22	M_RAS#0 → M_RAS#0 [30]
M_DA54	C3	DQA1_22/DQA_54	RASA1B	G17	M_RAS#1 → M_RAS#1 [30]
M_DA55	E1	DQA1_23/DQA_55			
M_DA56	G7	DQA1_24/DQA_56	CASA0B	G19	M_CAS#0 → M_CAS#0 [30]
M_DA57	G6	DQA1_25/DQA_57	CASA1B	G16	M_CAS#1 → M_CAS#1 [30]
M_DA58	G1	DQA1_26/DQA_58			
M_DA59	G3	DQA1_27/DQA_59	CSA0B_0	H22	M_CS#0 → M_CS#0 [30]
M_DA60	J6	DQA1_28/DQA_60	CSA0B_1	J22	
M_DA61	J1	DQA1_29/DQA_61			
M_DA62	J3	DQA1_30/DQA_62	CSA1B_0	G13	M_CS#1 → M_CS#1 [30]
M_DA63	J5	DQA1_31/DQA_63	CSA1B_1	K13	
MVREFDA	K26	MVREFDA	CKEA0	K20	M_CKE0 → M_CKE0 [30]
MVREFSA	J26	MVREFSA	CKEA1	J17	M_CKE1 → M_CKE1 [30]
	J25	MEM_CALRN0	WEA0B	G25	M_WE#0 → M_WE#0 [30]
	K25	MEM_CALRP0	WEA1B	H10	M_WE#1 → M_WE#1 [30]
			GDDR5 MAA1_8	G14	
			MAA0_8	G20	M_MA13
DRAM_RST	L10	DRAM_RST			
	K8	CLKTESTA			
	L7	CLKTESTB			

216-0774207-A11ROB_FCBGA631 VGA@

+1.8VGS

R357	X76@	10K_0402_5%	VRAM_ID0	VRAM_ID0 [24]
R358	X76@	10K_0402_5%		
R359	X76@	10K_0402_5%	VRAM_ID1	VRAM_ID1 [24]
R360	X76@	10K_0402_5%		
R361	X76@	10K_0402_5%	VRAM_ID2	VRAM_ID2 [24]
R362	X76@	10K_0402_5%		

Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
Hynix 512MB PN:SA000032460	R357	R360	R362
Samsung 512MB PN:SA000035700	R358	R359	R362
Hynix 1GB PN:SA00003VS20	R357	R360	R361
Samsung 1GB PN:SA00003MQ20	R358	R359	R361

+1.5VGS
VGA@ R363 40.2_0402_1% — MVREFDA — VGA@ R364 100_0402_1%
C467 VGA@ 0.1U_0402_16V4Z

+1.5VGS
VGA@ R365 40.2_0402_1% — MVREFSA — VGA@ R367 100_0402_1%
C468 VGA@ 0.1U_0402_16V4Z

PARK SCL has different recommand

[30] DRAM_RST# — VGA@ R366 49.9_0402_1% — VGA@ R369 10_0402_1% — DRAM_RST
VGA@C469 120P_0402_50V8J
R371 VGA@ 4.99K_0402_1%

+1.5VGS
R368 VGA@ 243_0402_1%
R370 VGA@ 243_0402_1%

R372 @51.1_0402_1% C470 @0.1U_0402_16V4Z
R373 @51.1_0402_1% C471 @0.1U_0402_16V4Z

Route 50ohms single-ended/100ohm diff and keep short

debug only, for clock observation,if not need, DNI.

Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: RobsonXT-S3 MEM Interface

Size: B | Document Number | Rev: 0.1

Date: Tuesday, August 17, 2010 | Sheet 29 of 57

[29] M_DA[63..0] → M_DA[63..0]
[29] M_MA[13..0] → M_MA[13..0]
[29] M_DQM[7..0] → M_DQM[7..0]
[29] M_DQS[7..0] → M_DQS[7..0]
[29] M_DQS#[7..0] → M_DQS#[7..0]

H1G / S1G
Hynix H1G@ X7624938L01 / Samsung S1G@ X7624938L02
0706 update
update X76 PN
H512 / S512
Hynix H512@ X7624938L03 / Samsung S512@ X7624938L04

U19 / U20 / U18 / U21
64MX16 H5TQT63BFR-12C FBGA
X76@
100-BALL SDRAM DDR3

ref 139-02 recommand
add off page
Park SCL recommand pu 60.4 ohm to 1.5VGS
0619 update

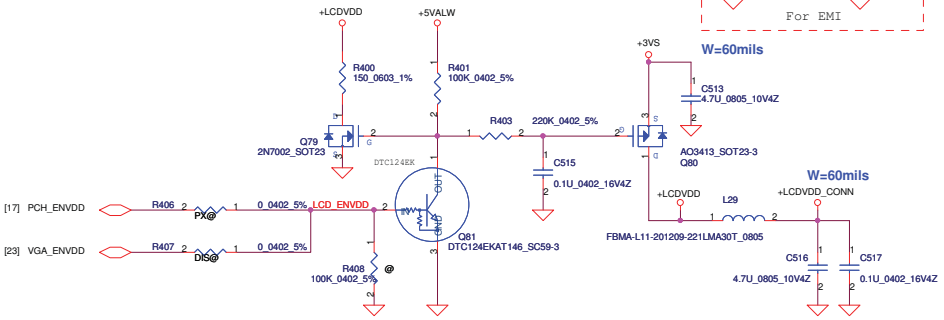
VRAM P/N :
Hynix : SA000041S10 (S IC D3 64MX16 H5TQ1G63BFR-11C FBGA C38!)
Samsung : SA000041T10 (S IC D3 64MX16 K4W1G1646E-HC11 FBGA C38!)
update VRAM PN 0619 update

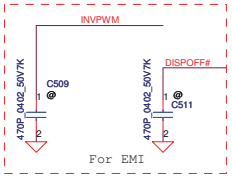
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

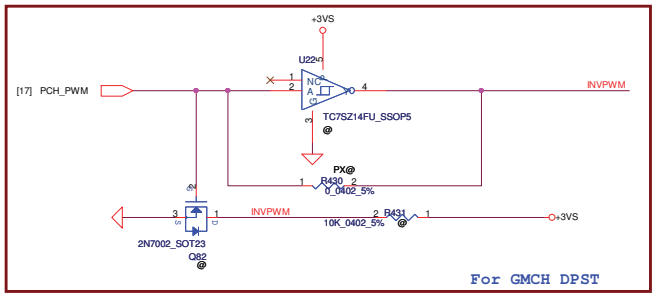
Compal Electronics, Inc.
Title: RobsonXT-S3 VRAM
Size: C | Document Number | Rev: 0.1
Date: Tuesday, August 17, 2010 | Sheet 30 of 57

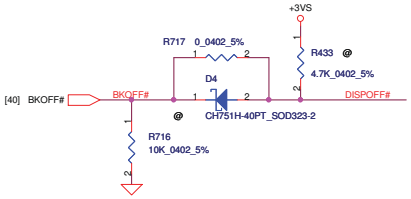
VGA LCD/PANEL BD. Conn.

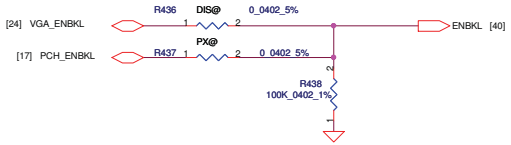
LCD POWER CIRCUIT

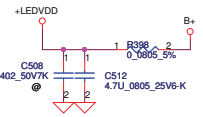




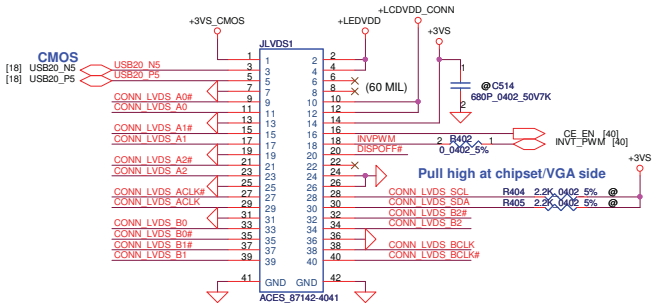


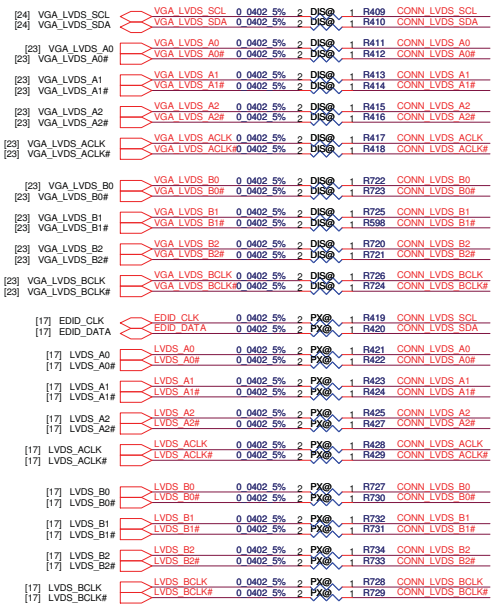




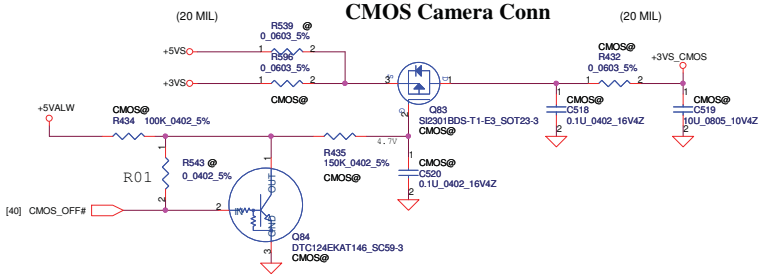


R01





CMOS Camera Conn



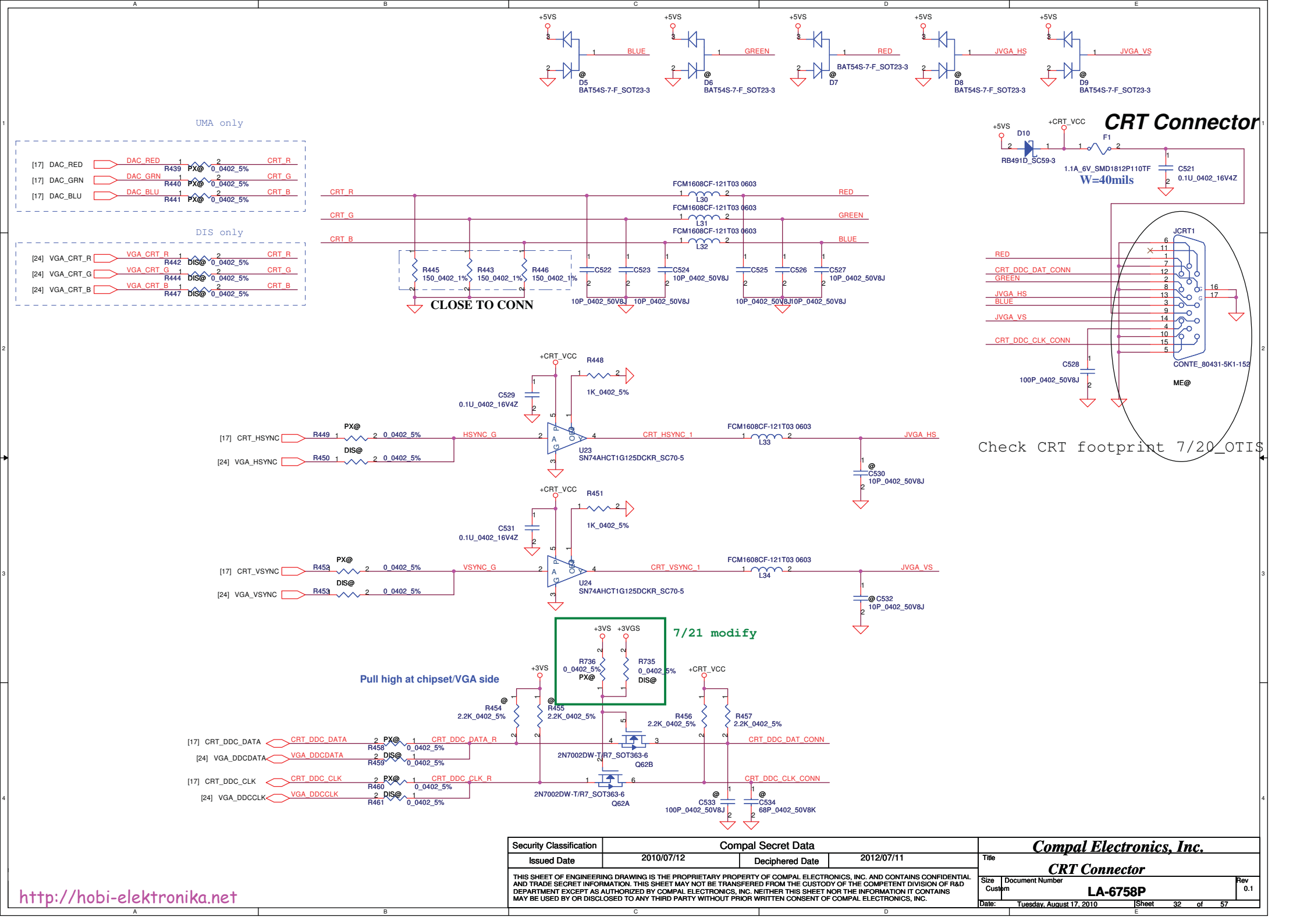
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: LVDS/CAMERA

Size	Document Number	Rev
Custom	LA-6758P	0.1

Date: Tuesday, August 17, 2010 | Sheet 31 of 57



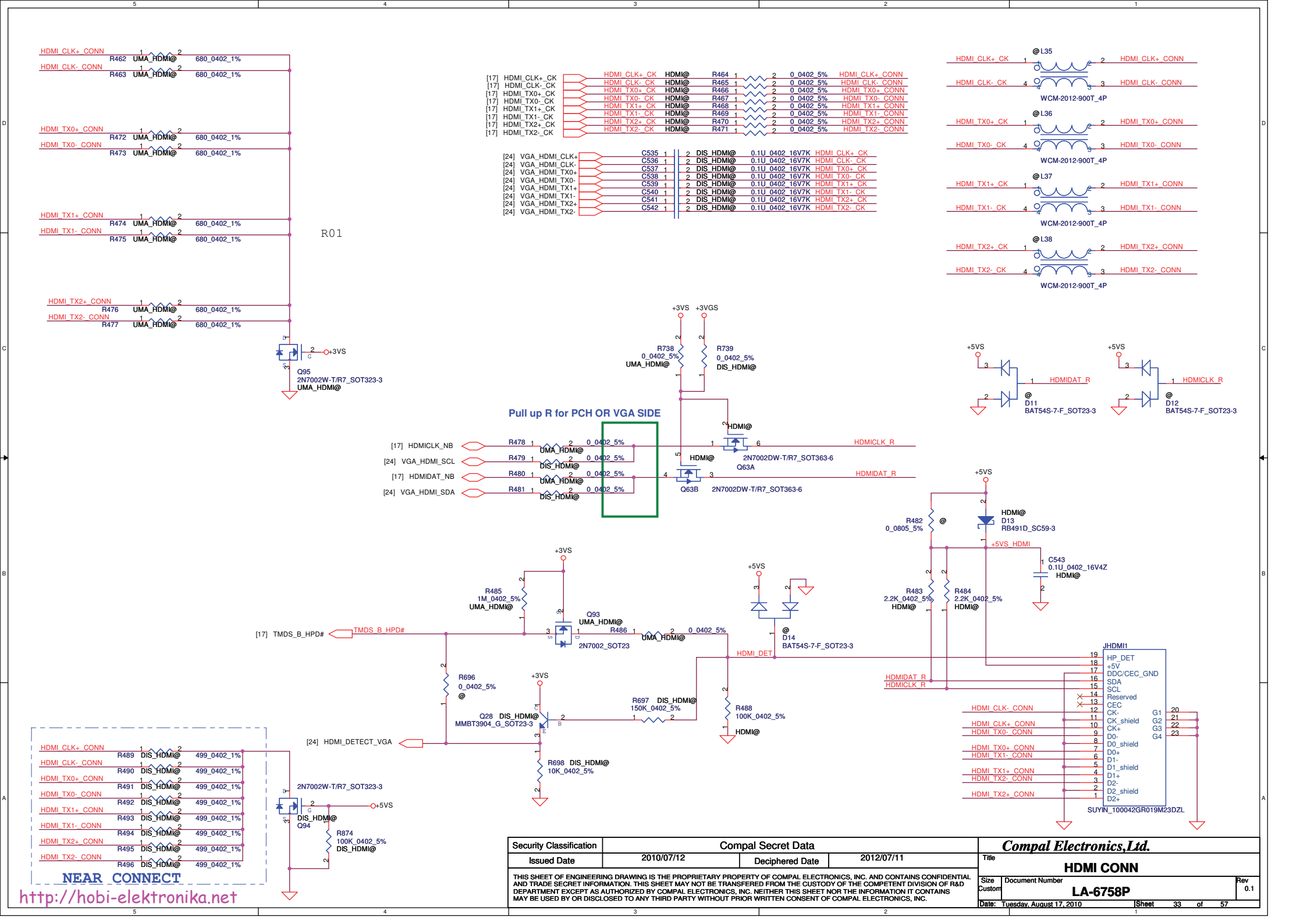
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: CRT Connector

Size	Document Number	Rev
Custom	LA-6758P	0.1

Date: Tuesday, August 17, 2010 Sheet 32 of 57



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

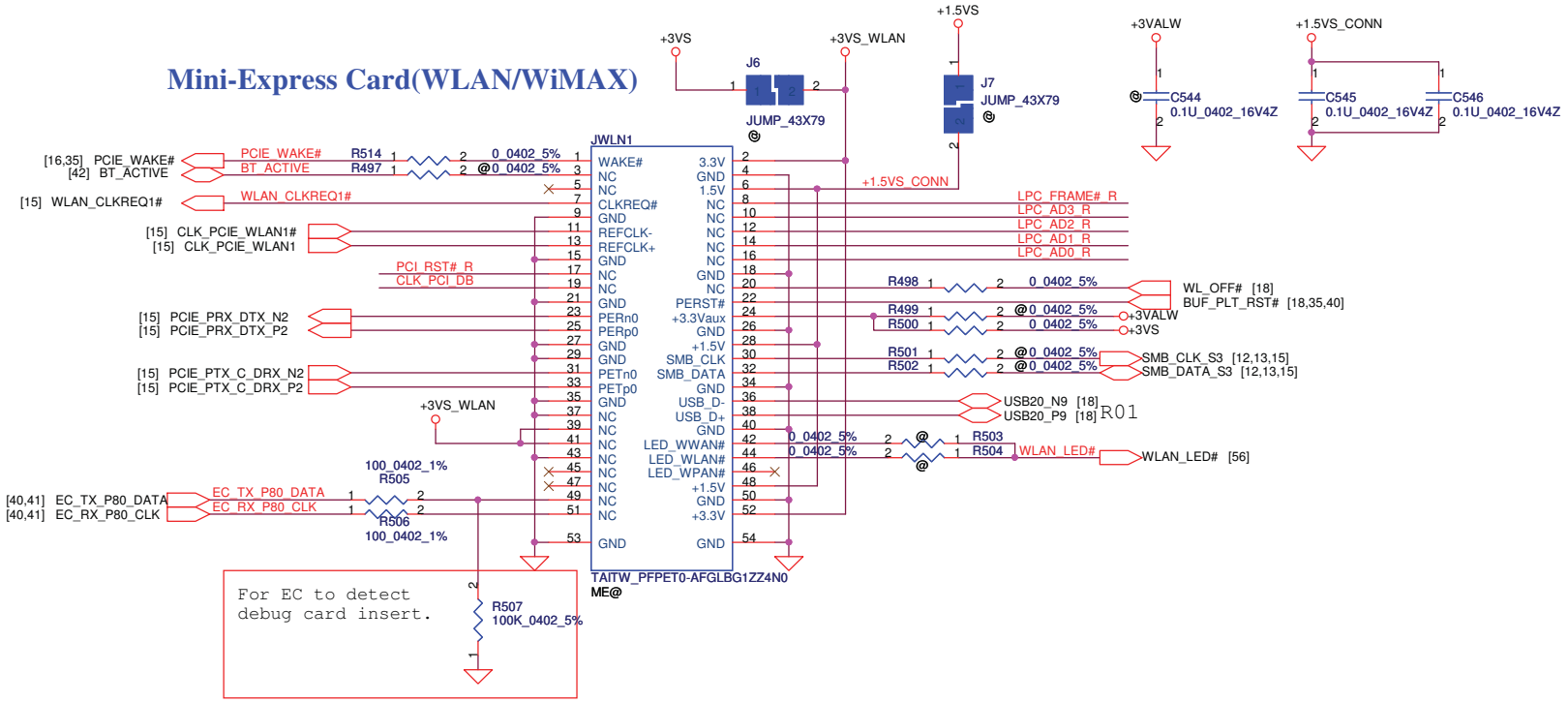
Compal Electronics, Ltd.

Title: HDMI CONN

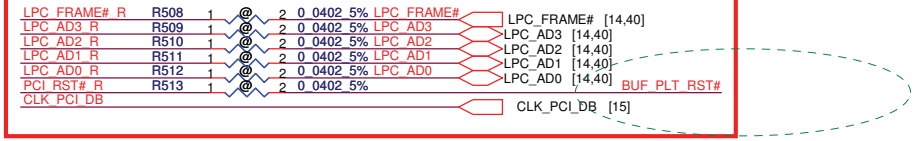
Size	Document Number	Rev
Custom	LA-6758P	0.1

Date: Tuesday, August 17, 2010 Sheet 33 of 57

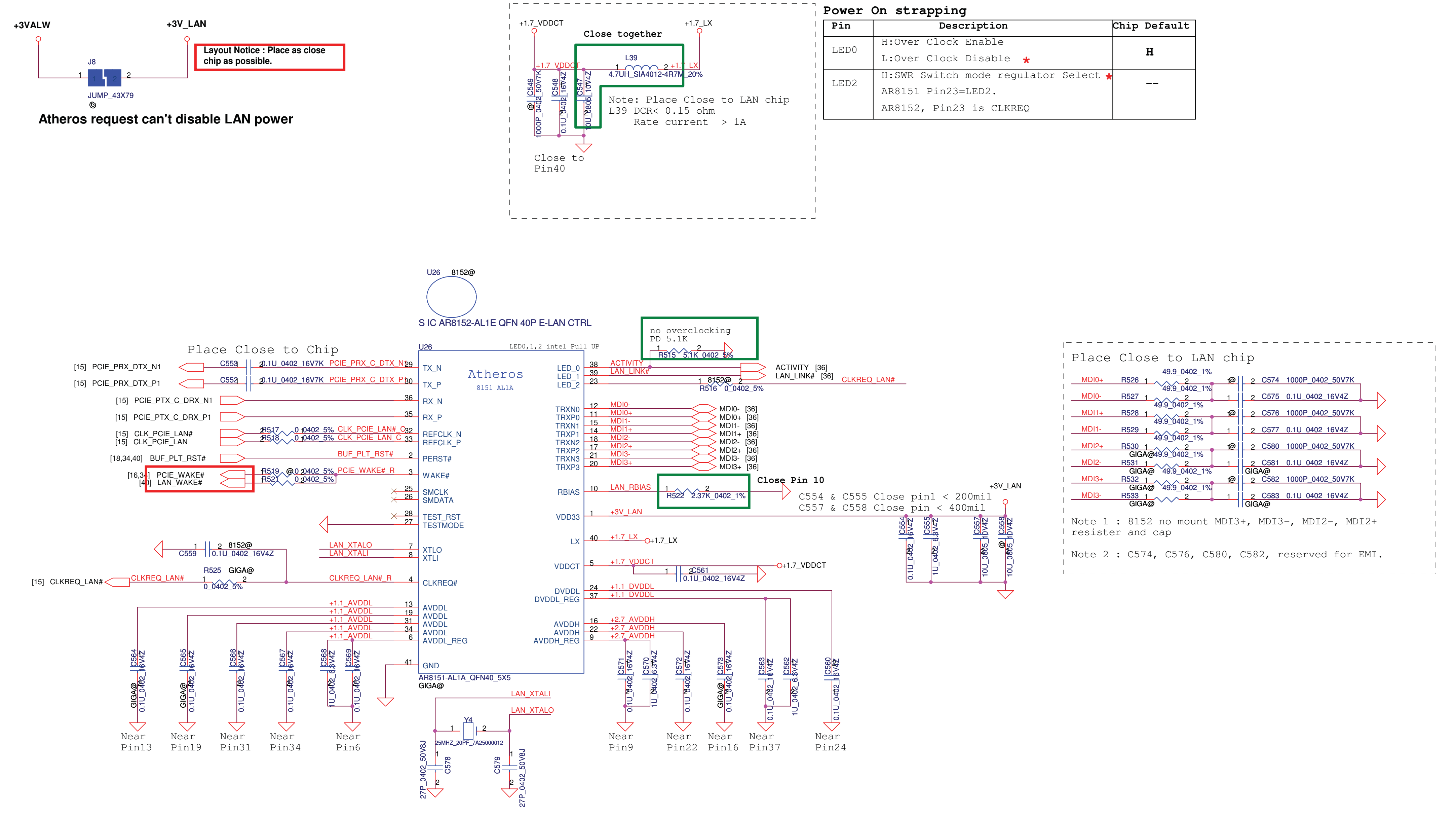
Mini-Express Card for WLAN/WiMAX(Half)



Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2010/07/12	Deciphered Date	2012/07/11
Title	Mini-Card/NEW Card/SIM		
Size	Document Number		Rev
	LA-6758P		0.1
Date: Tuesday, August 17, 2010	Sheet 34 of 57		



Power On strapping

Pin	Description	Chip Default
LED0	H:Over Clock Enable L:Over Clock Disable *	H
LED2	H:SWR Switch mode regulator Select * AR8151 Pin23=LED2. AR8152, Pin23 is CLKREQ	--

		Configure				Configure
	Pin4	R525	C559		Pin23	R516
AR8152	VDDCT_REG		*		CLKREQn	*
AR8151	CLKREQn	*			LED[2]	

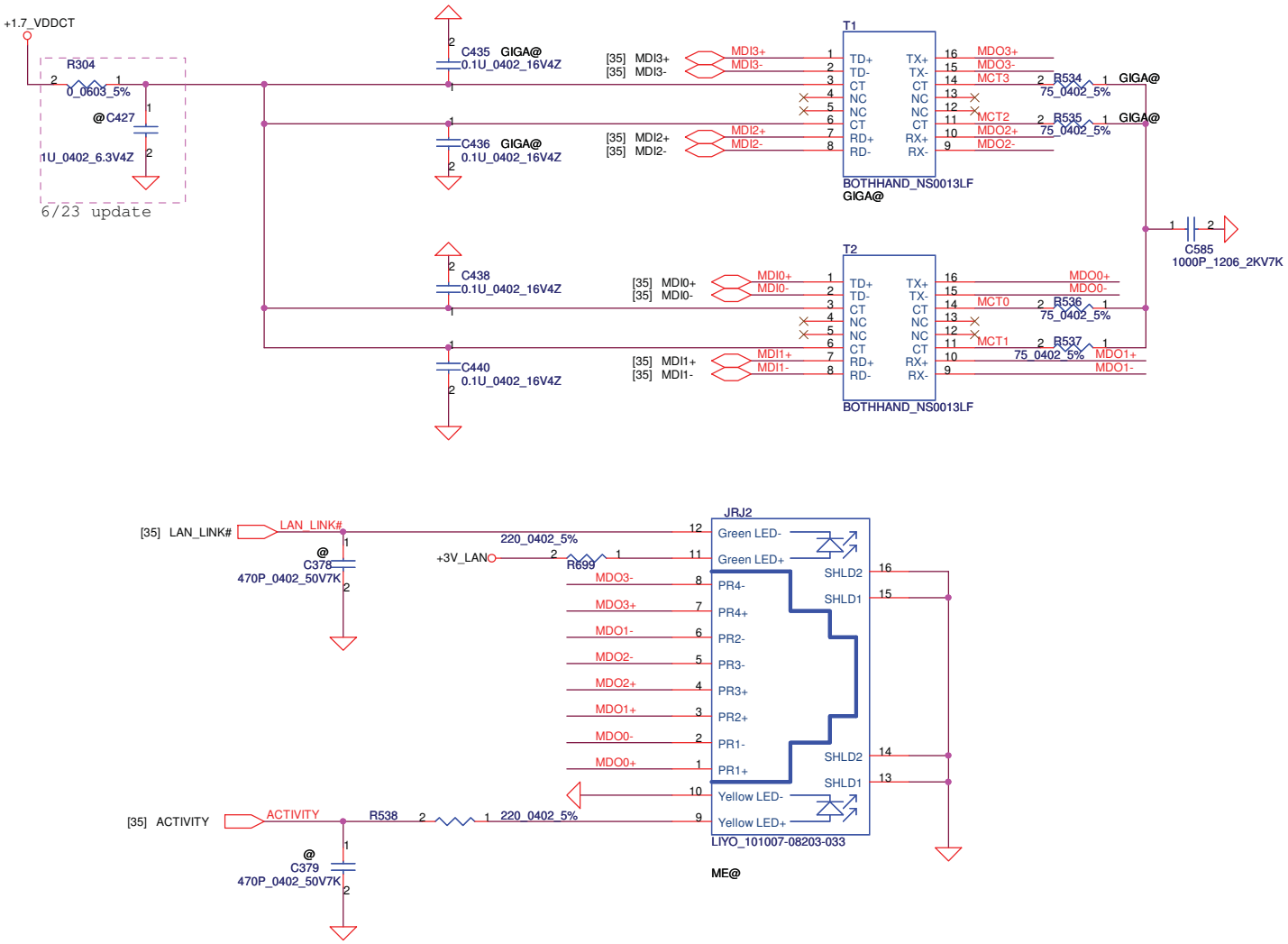
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: LAN-AR8151/8152

Size: Custom | Document Number: LA-6758P | Rev: 0.1

Date: Tuesday, August 17, 2010 |



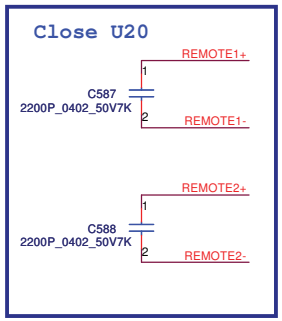
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

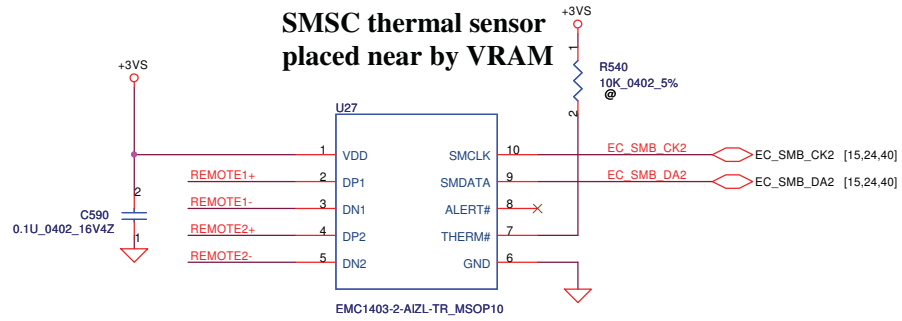
Compal Electronics, Inc.

Title: **LAN_Transformer**

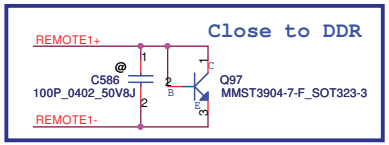
Size	Document Number	Rev
B	LA-6758P	0.1

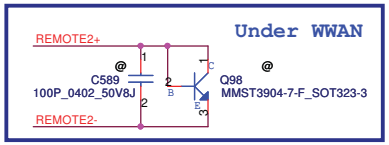
Date: Tuesday, August 17, 2010 Sheet 36 of 57





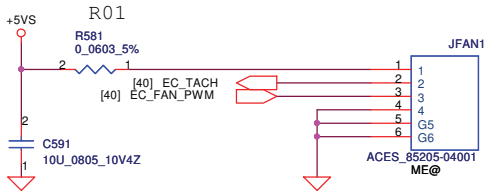
Address 1001_101xb





REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

FAN1 Conn



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

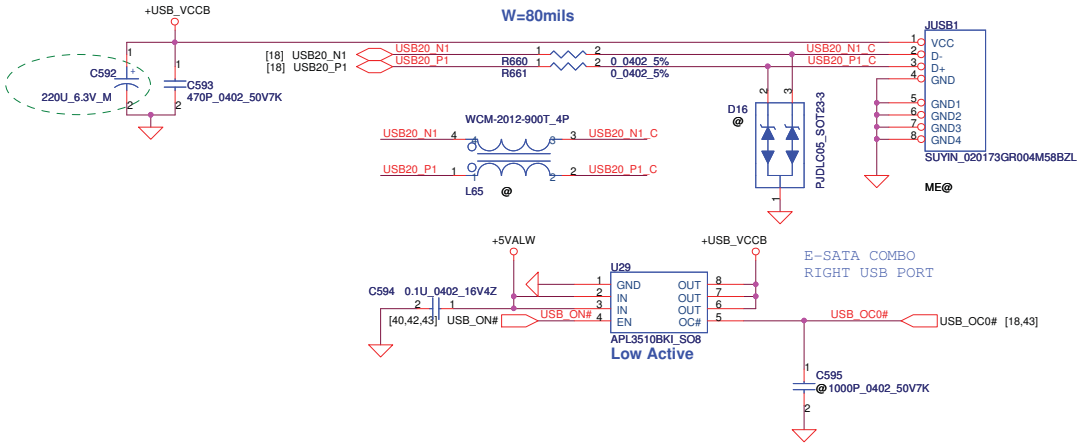
Compal Electronics,Ltd.

Title: **EMC1403_Thermal sensor/FAN**

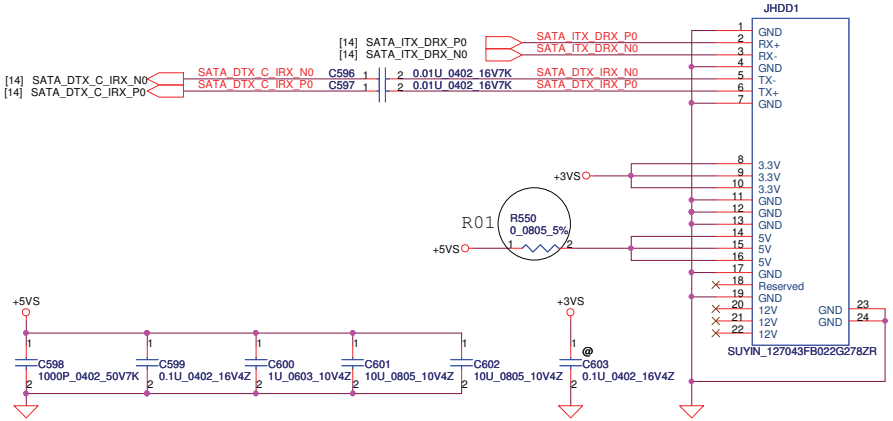
Size	Document Number	Rev
Custom	LA-6758P	0.1

Date: Tuesday, August 17, 2010 Sheet 37 of 57

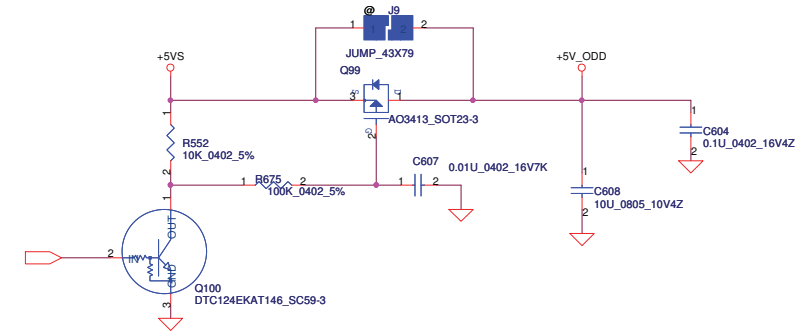
Left USB Conn.



SATA HDD Conn.



ODD Power Control



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

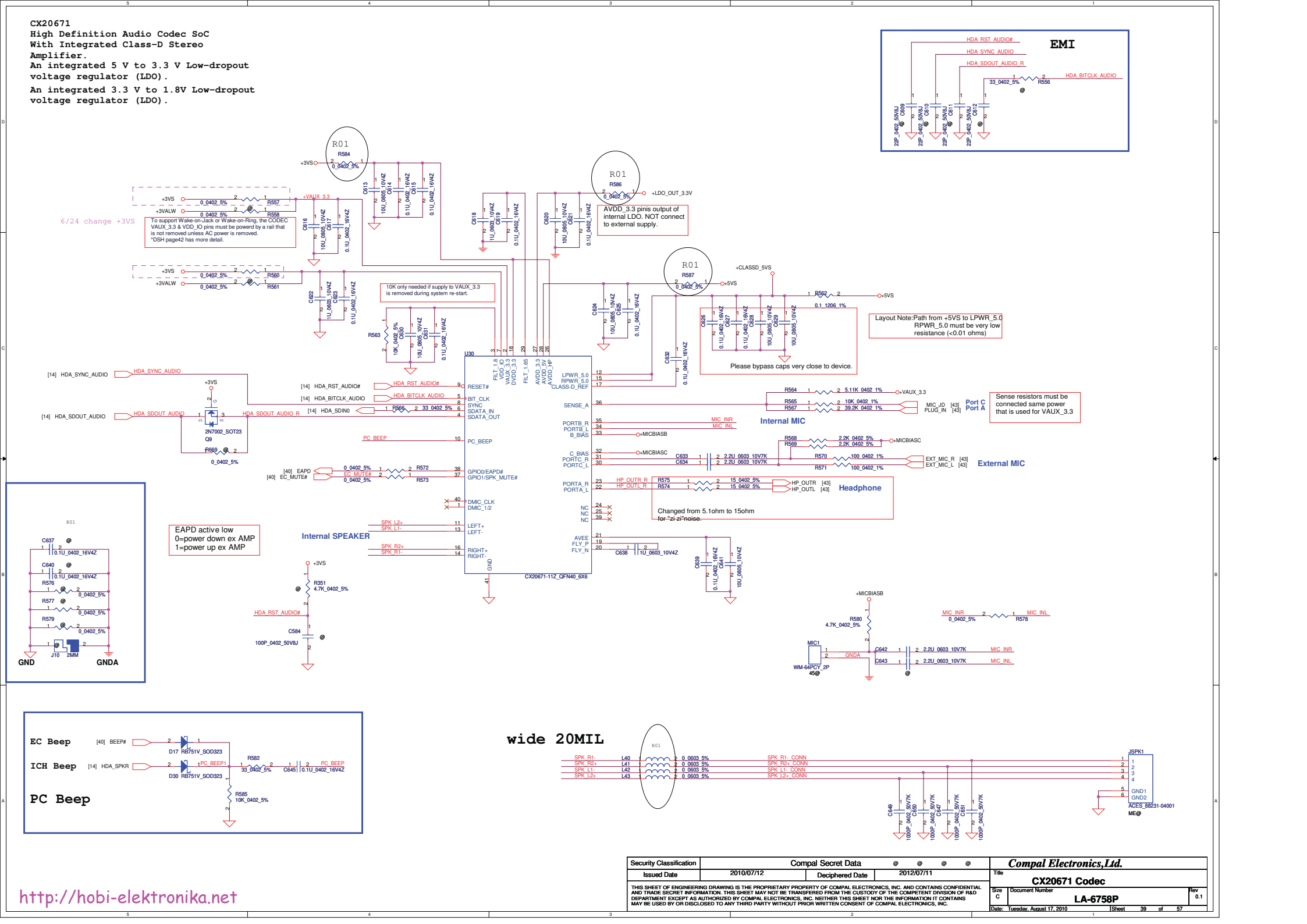
Compal Electronics, Inc.

Title: HDD/ODD Connector

Size: B | Document Number: LA-6758P | Rev: 0.1

Date: Tuesday, August 17, 2010 | Sheet 38 of 57

CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

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Compal Electronics,Ltd.

Title: CX20671 Codec

Size: C | Document Number: LA-6758P | Rev: 0.1

Date: Tuesday, August 17, 2010 | Sheet 39 of 57

Vcc	3.3V +/- 5%
R694	100K +/- 5%

Board ID	R695	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	
0	0	0 V	0 V	0 V	EVT
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	DVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	PVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	MP

ENE UPDATE 08/10/21

7/21 modify

7/23 Modify

7/23 Modify

6/19 Add BRDID

7/28 Modify

6/24 Update R708,R709 must be close Y5

6/15 add XTAL

http://hobi-elektronika.net

Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

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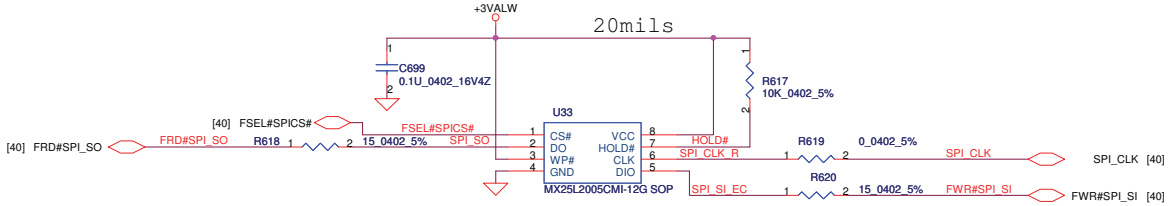
Compal Electronics, Inc.

Title: BIOS & EC I/O Port

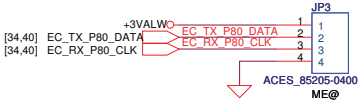
Size: Custom | Document Number: LA-6758P | Rev: 0.1

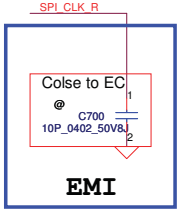
Date: Tuesday, August 17, 2010 | Sheet 40 of 57

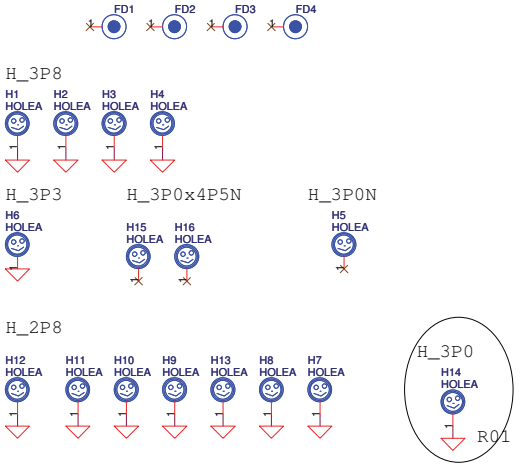
FOR EC 256KB SPI ROM
(150mil PACKAGE)



EC DEBUG PORT

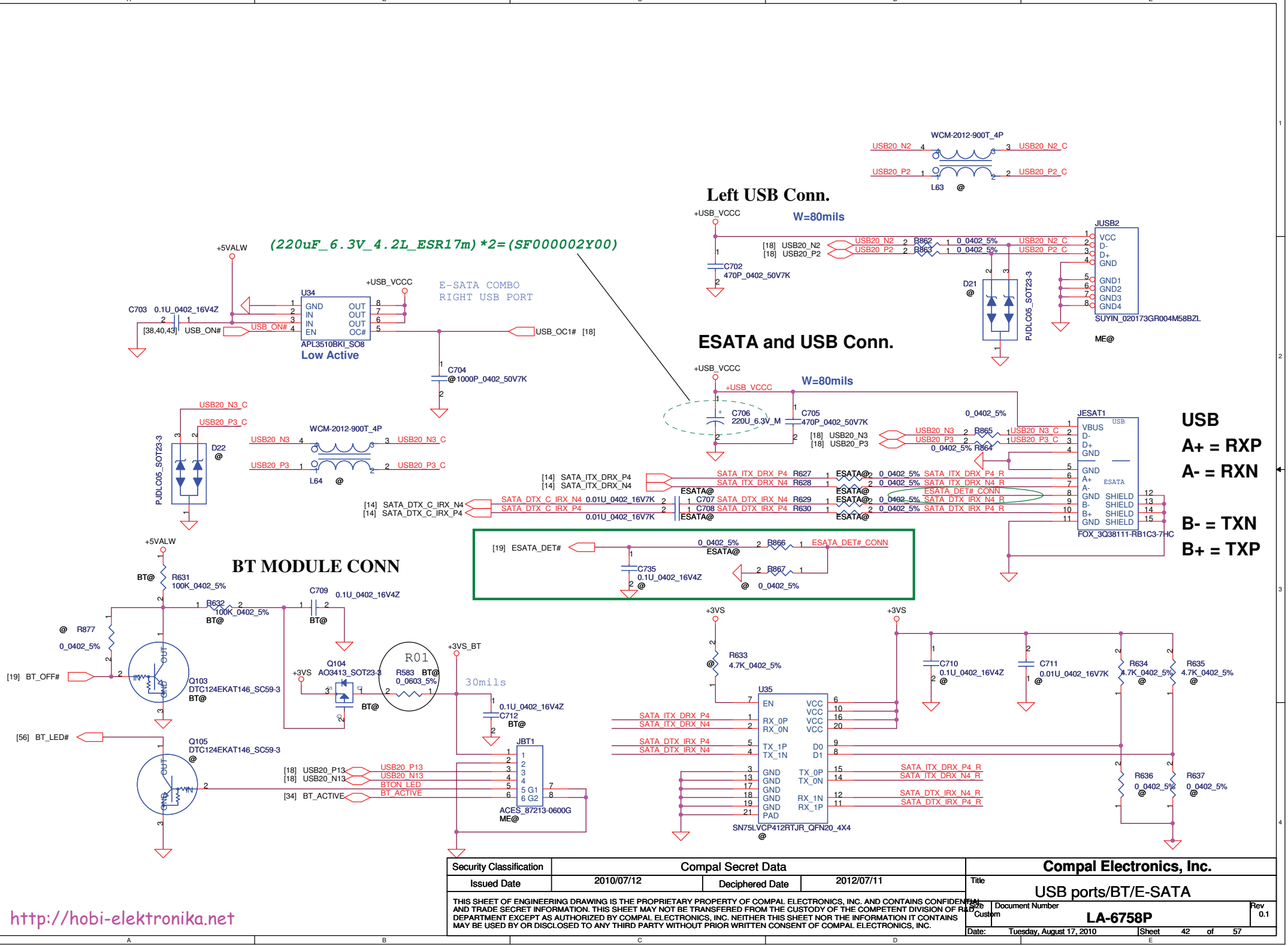






Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

Compal Electronics, Inc.			
Title: LED/EC SPI ROM			
Size: B	Document Number: LA-6758P		Rev: 0.1
Date: Tuesday, August 17, 2010	Sheet 41 of 57		



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

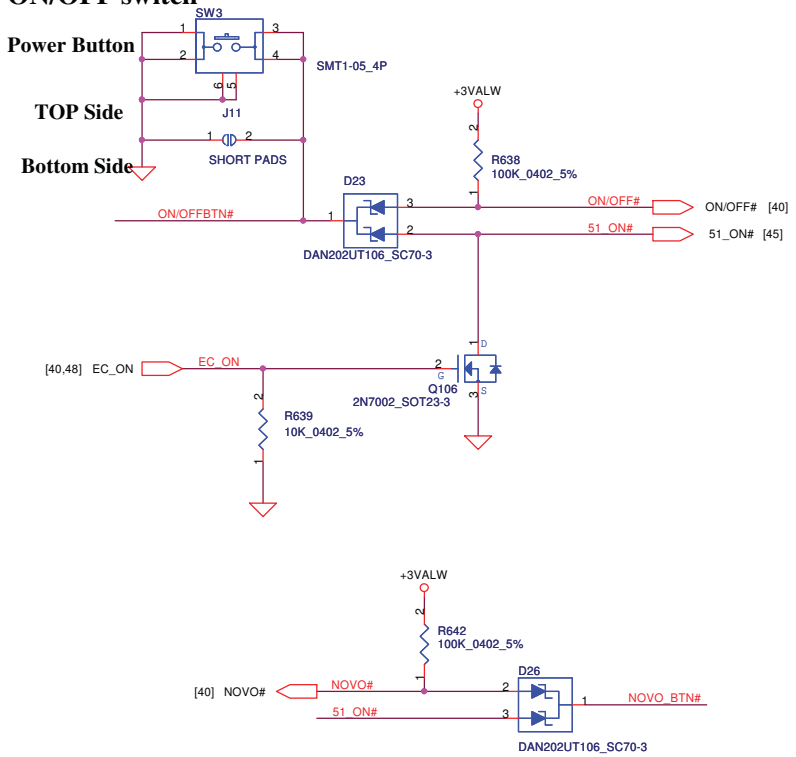
Compal Electronics, Inc.

Title: USB ports/BT/E-SATA

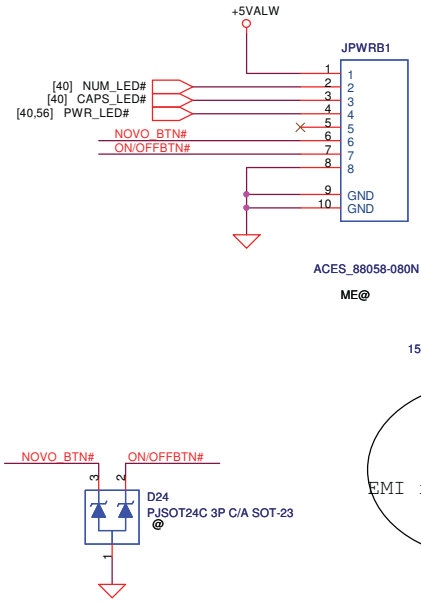
Size	Document Number	Rev
Custom	LA-6758P	0.1

Date: Tuesday, August 17, 2010 | Sheet 42 of 57

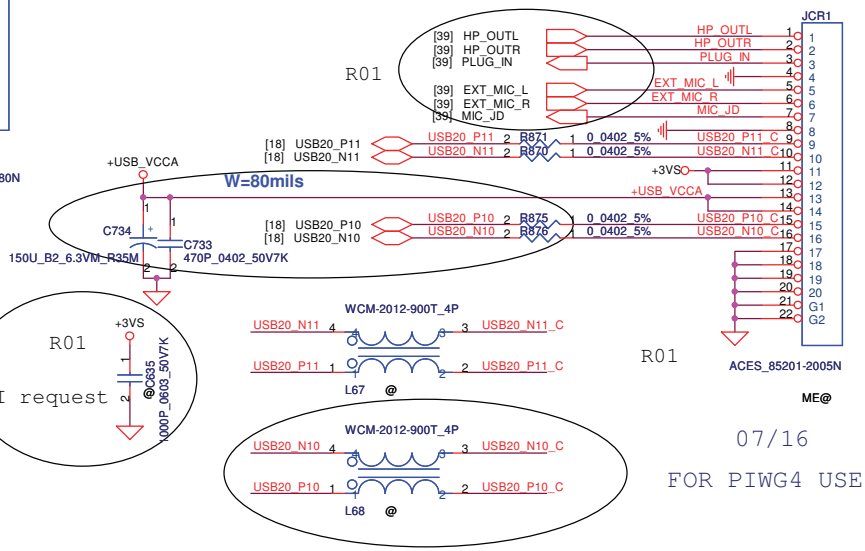
ON/OFF switch



Power Bottom Board Conn. 8pin



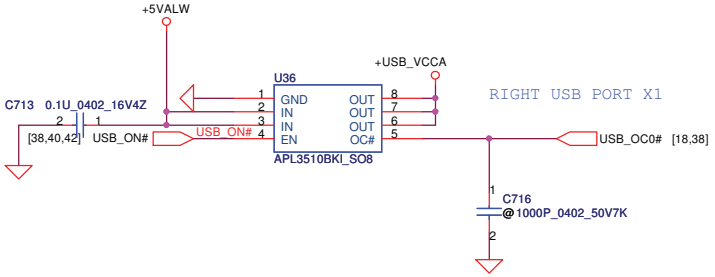
Card Reader/Audio Jack SB CONN



EMI REQUEST 1ST = SCA00000E00
2ST = SCA00000R00

07/16

FOR PIWG4 USE

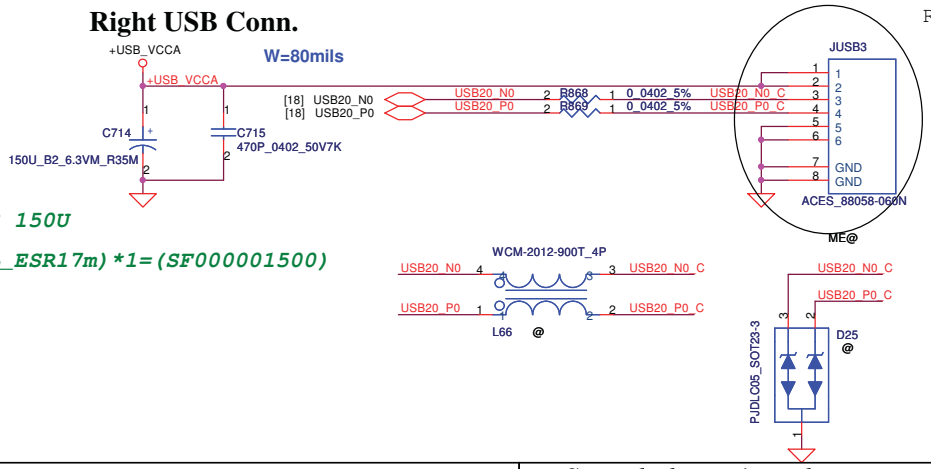


07/16

FOR PIWG4 USE

R01

Right USB Conn.



6/9 change to B2 150U

*(220uF_6.3V_5.8L_ESR17m)*1=(SF000001500)*

Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

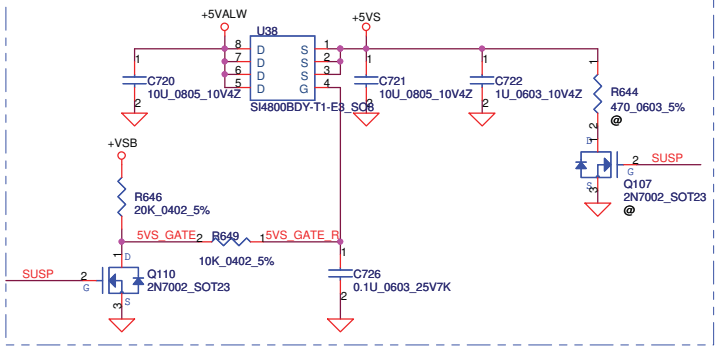
Compal Electronics,Ltd.

Title: **other IO connector**

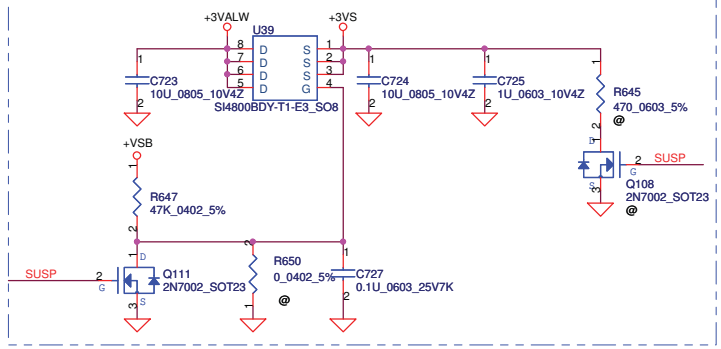
Size	Document Number	Rev
Custom	LA-6758P	0.1

Date: Tuesday, August 17, 2010 Sheet 43 of 57

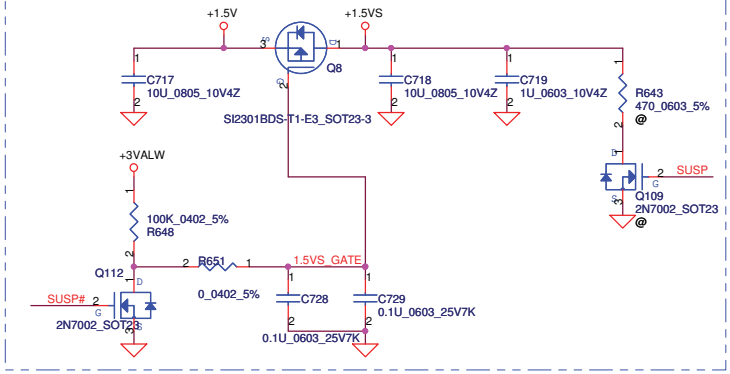
+5VALW TO +5VS



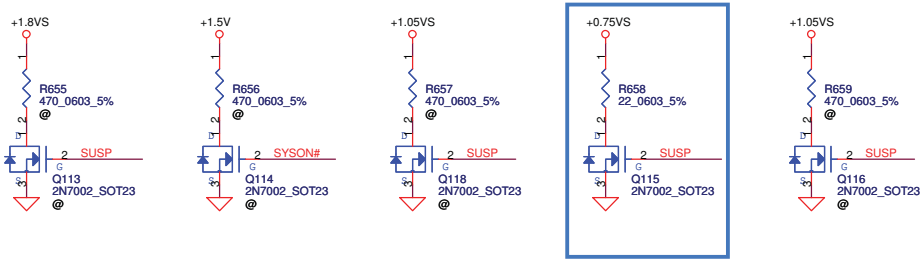
+3VALW TO +3VS



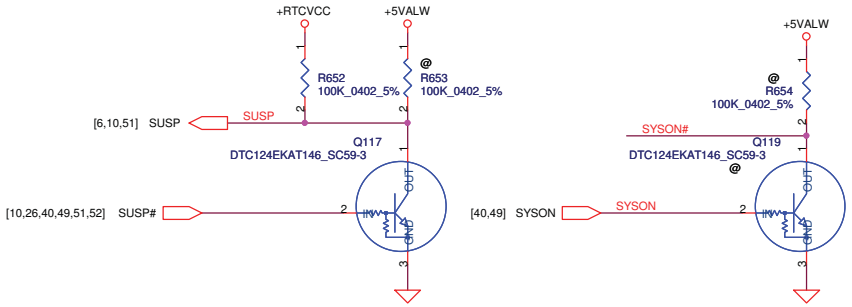
+1.5V to +1.5VS



6/13 change SI4800 to SI2301



For Intel S3 Power Reduction.



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

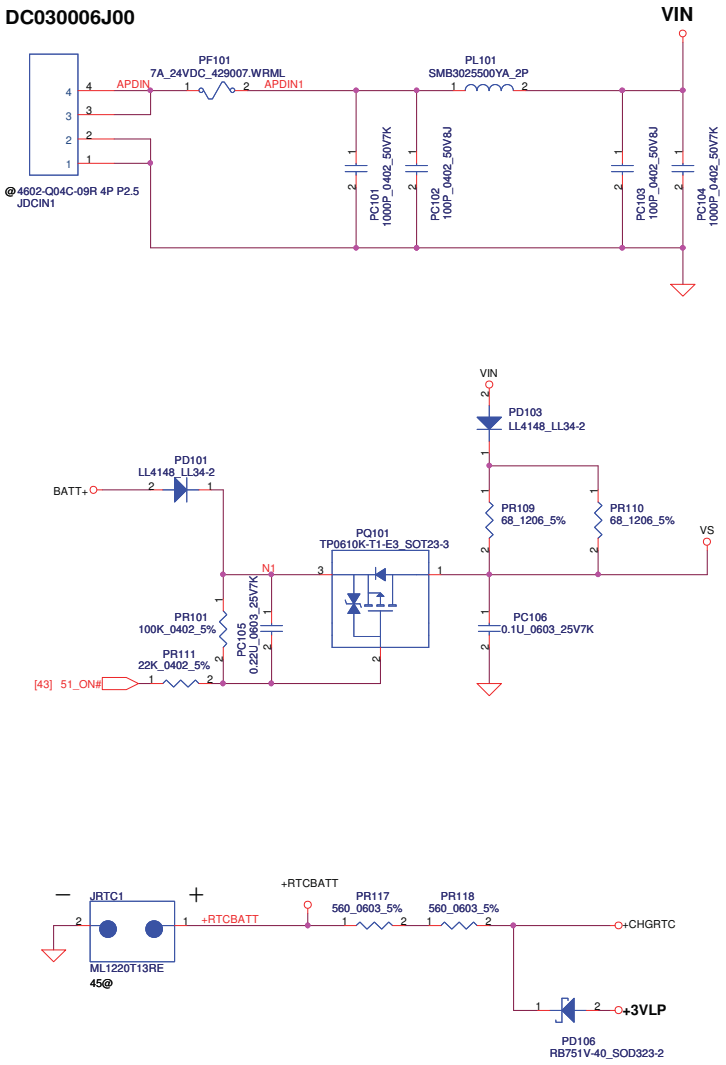
Compal Electronics, Inc.

Title: DC Interface

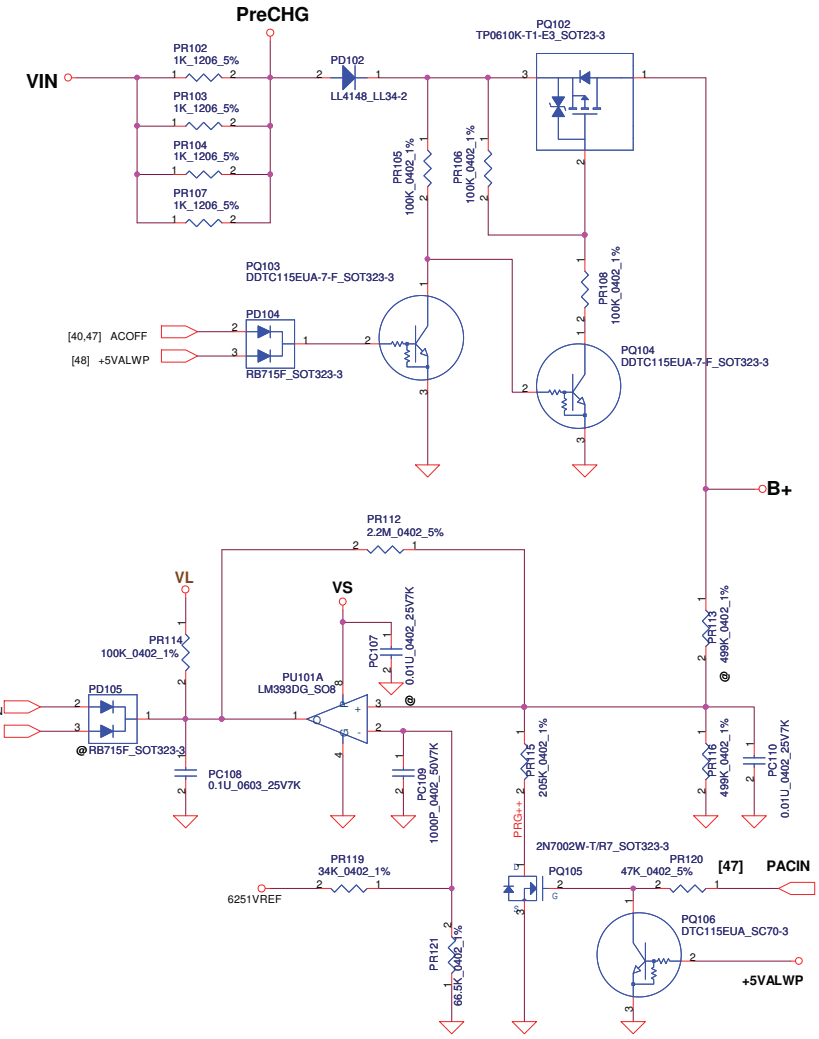
Size: Custom | Document Number: LA-6758P | Rev: 0.1

Date: Tuesday, August 17, 2010 | Sheet 44 of 57

DC030006J00



Precharge detector
15.97V/14.84V FOR
ADAPTOR



ACIN

Precharge detector	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

BATT ONLY

Precharge detector	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V

Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

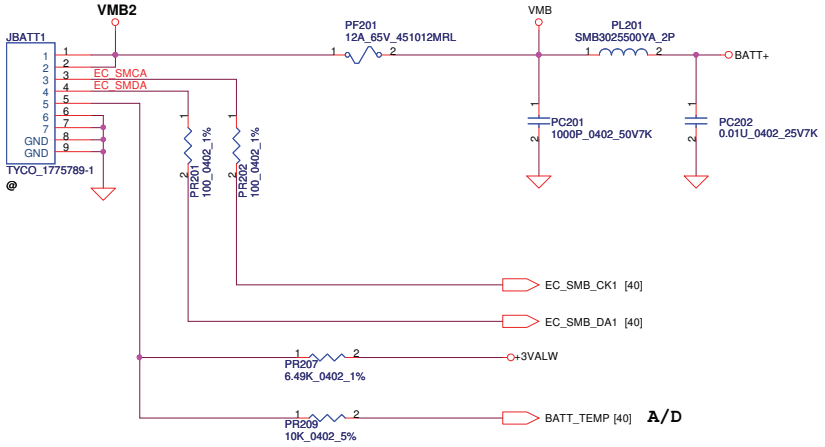
Compal Electronics, Inc.

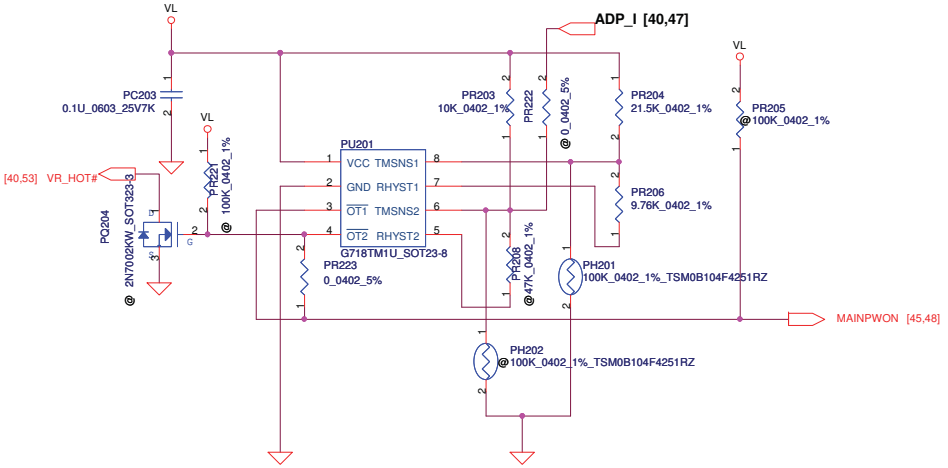
Title: PWR DCIN / Vin Detector /Pre-charge

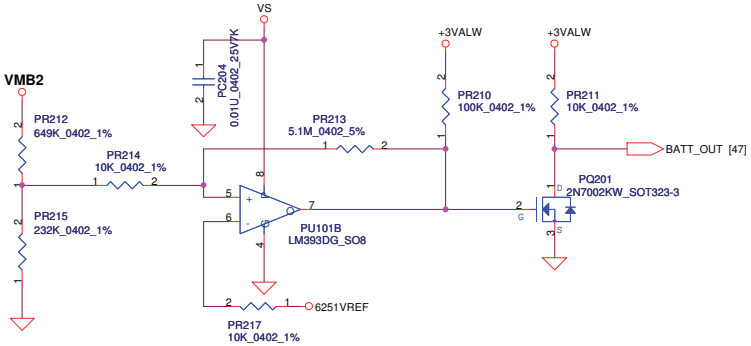
Size: Custom | Document Number: PIWG4 | Rev: 0.1

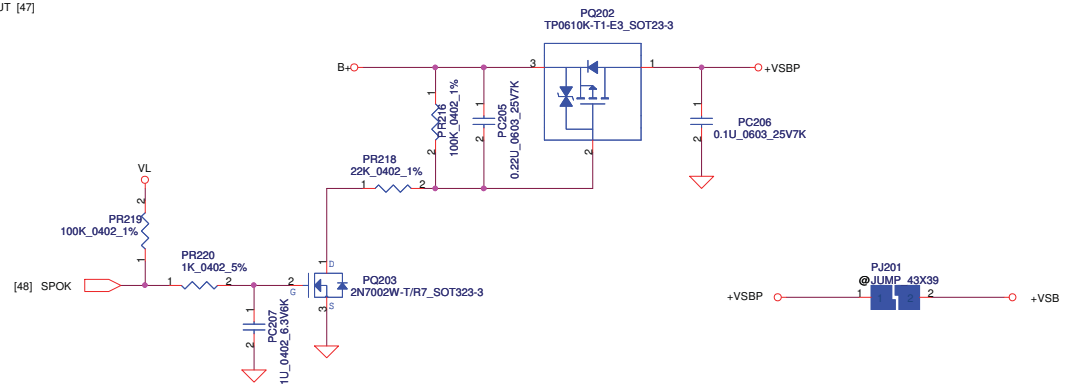
Date: Tuesday, August 17, 2010 | Sheet 45 of 57

PH201 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



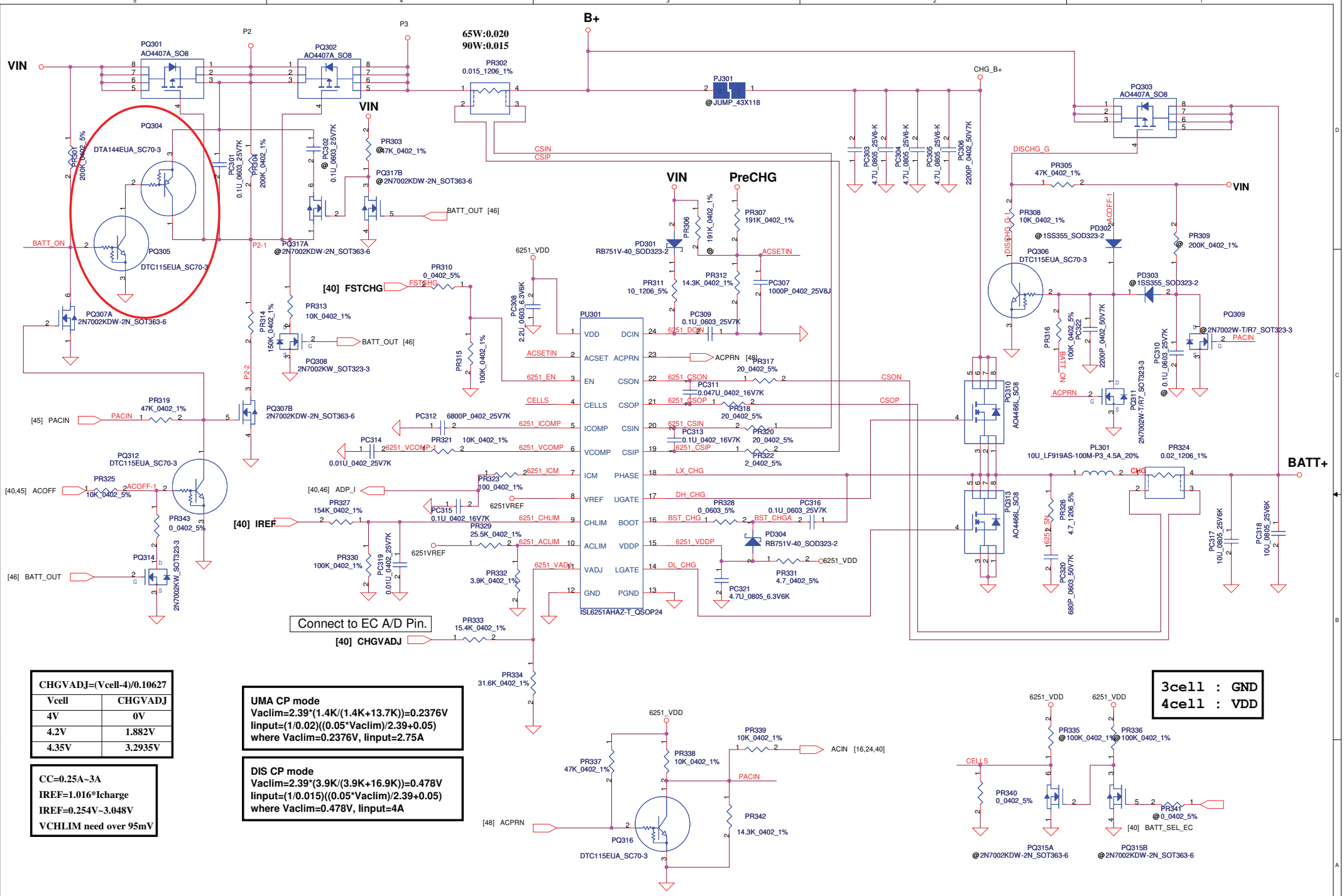






Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.			
Title: PWR-BATTERY CONN/OTP			
Size: Custom	Document Number: PIWG4		Rev: 0.1
Date: Tuesday, August 17, 2010	Sheet 46 of 57		



Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2011/01/13

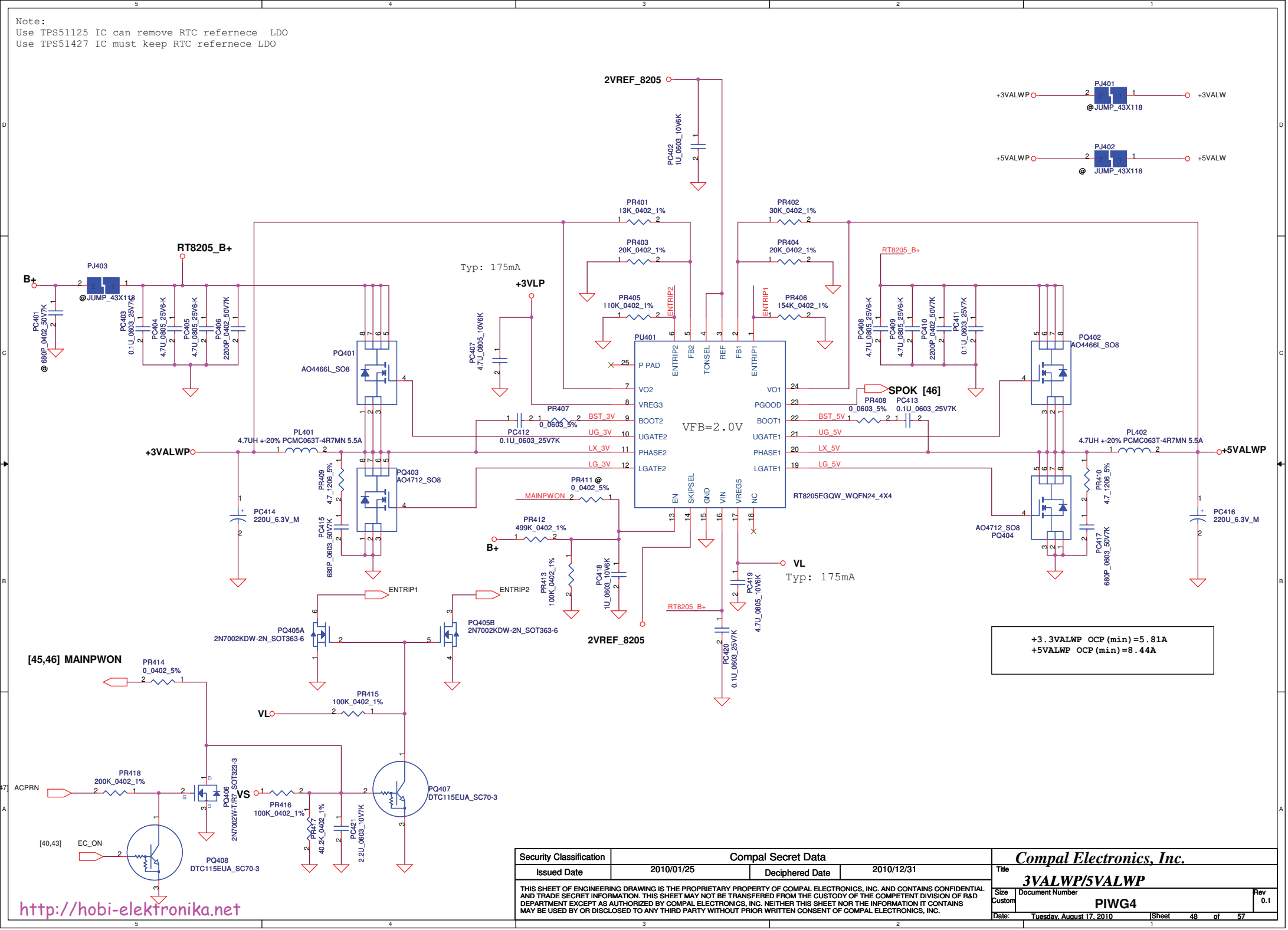
Compal Electronics, Inc.

Title: CHARGER

Size: | Document Number: PIWG4 | Rev: 0.1

Date: Tuesday, August 17, 2010 | Sheet 47 of 57

Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



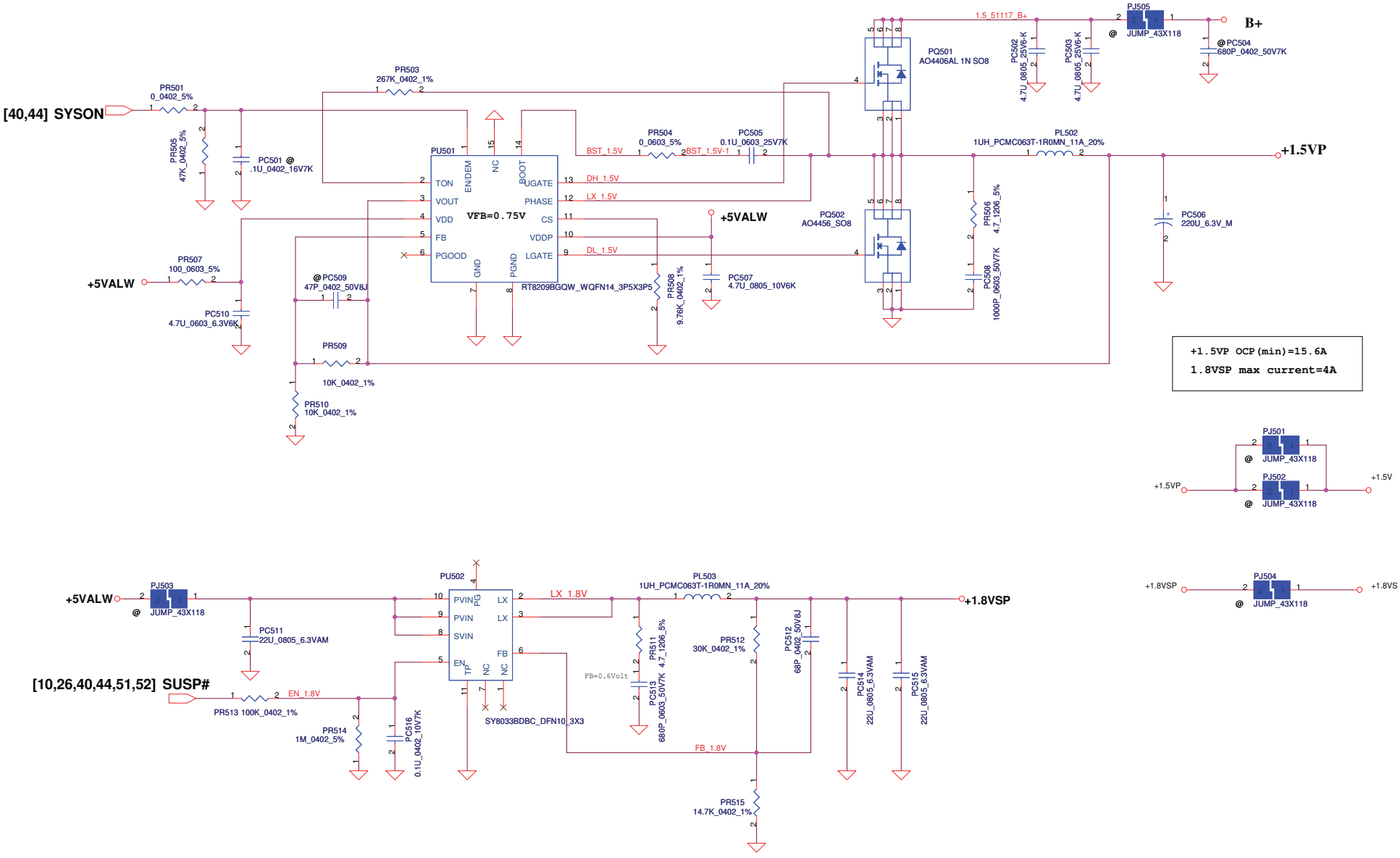
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size	Document Number	Rev
Custom	PIWG4	0.1

Date: Tuesday, August 17, 2010 Sheet 48 of 57



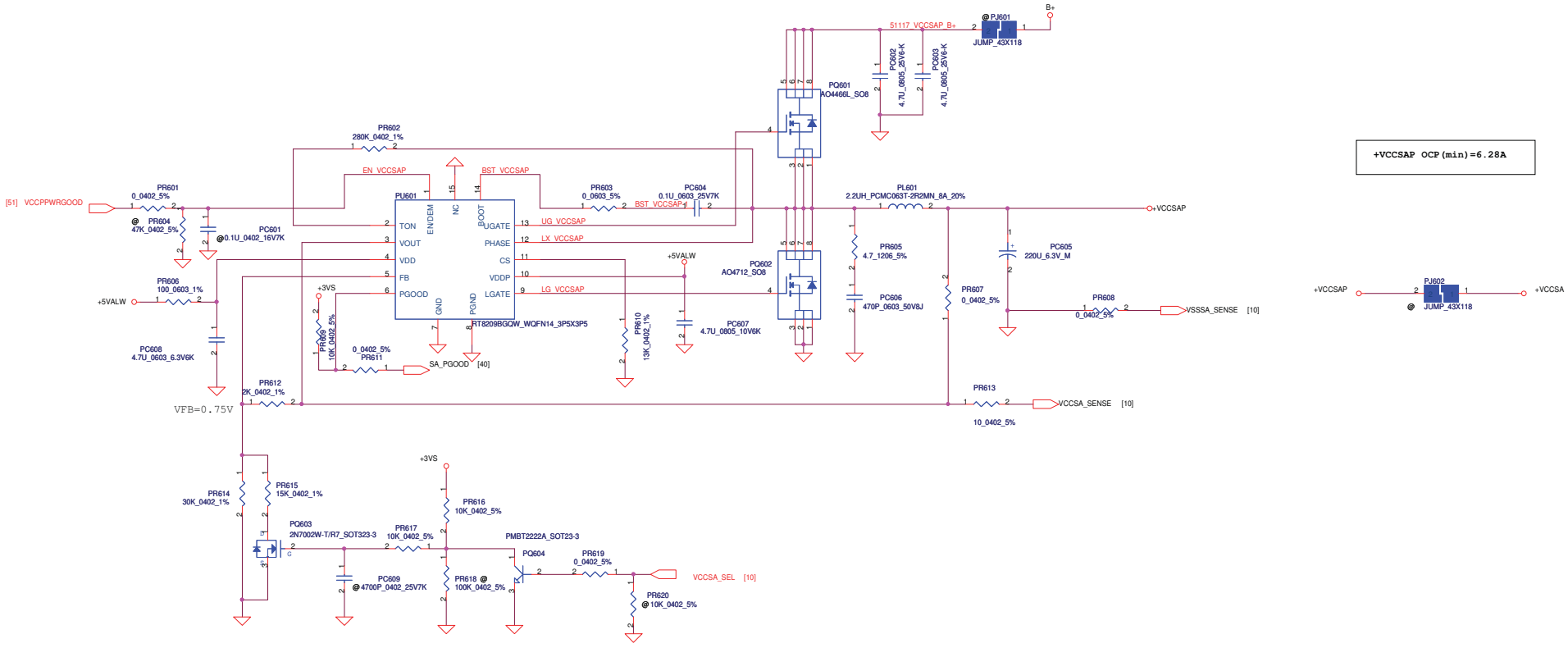
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: ***PWR-+1.5VP/+1.8VSP***

Size	Document Number	Rev
Custom	PIWG4	0.1

Date: Tuesday, August 17, 2010 | Sheet 49 of 57



VID[0]	VID[1]	VCCSA Vout	Require on 2011/ 2012 Required
0	0	0.9 V	Yes/Yes
0	1	0.8 V	Yes/Yes
1	1	0.75V	No/Yes
1	1	0.65V	No/Yes

Note:Use VCCSA_SEL to switch High & Low Level for VID[1]
(ie. VCCSA_SEL) due to the VID[0] is don't care for this setting.

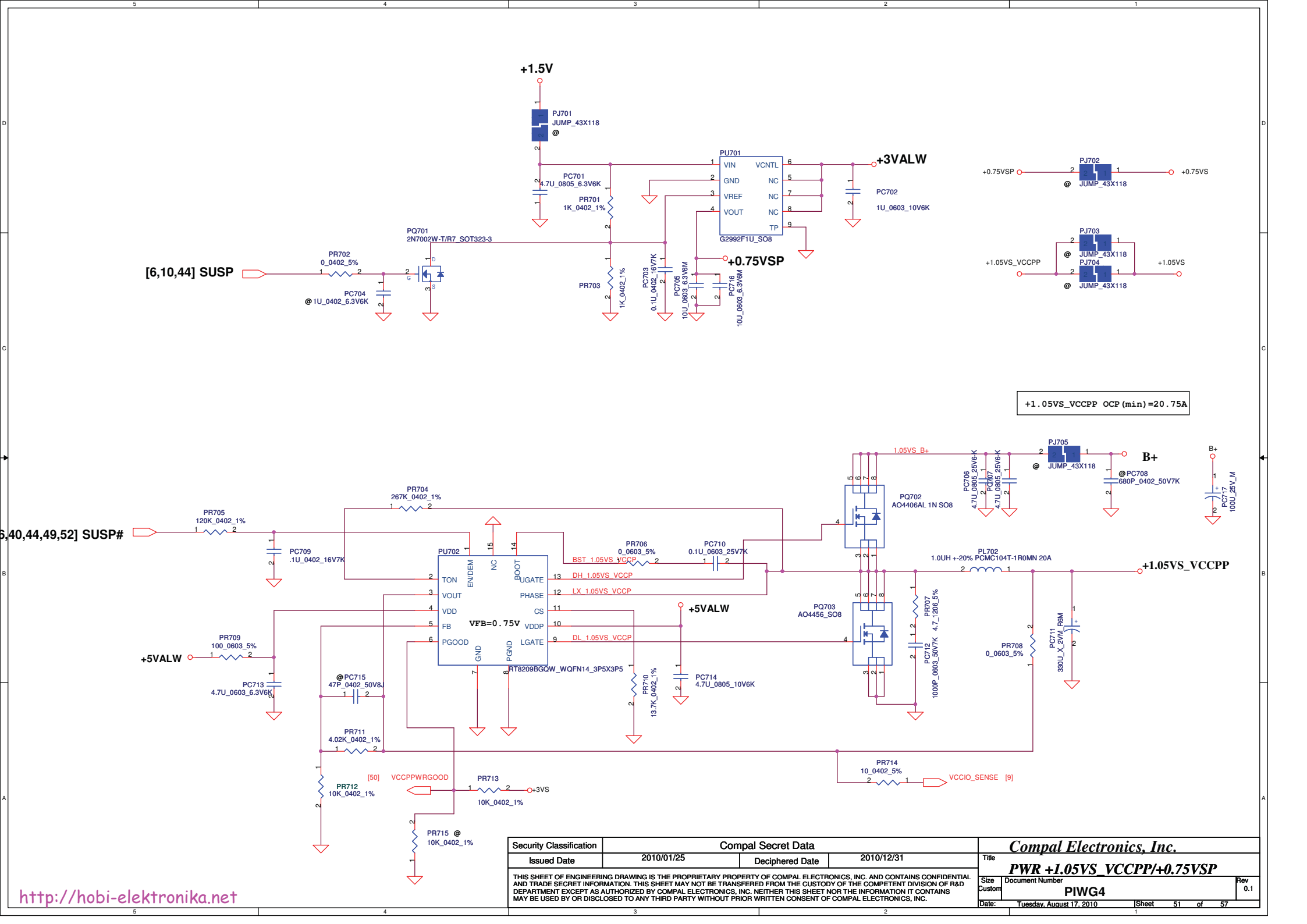
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PWR +VCCSAP

Size	Document Number	Rev
C	PIWG4	0.1

Date: Tuesday, August 17, 2010 Sheet 50 of 57



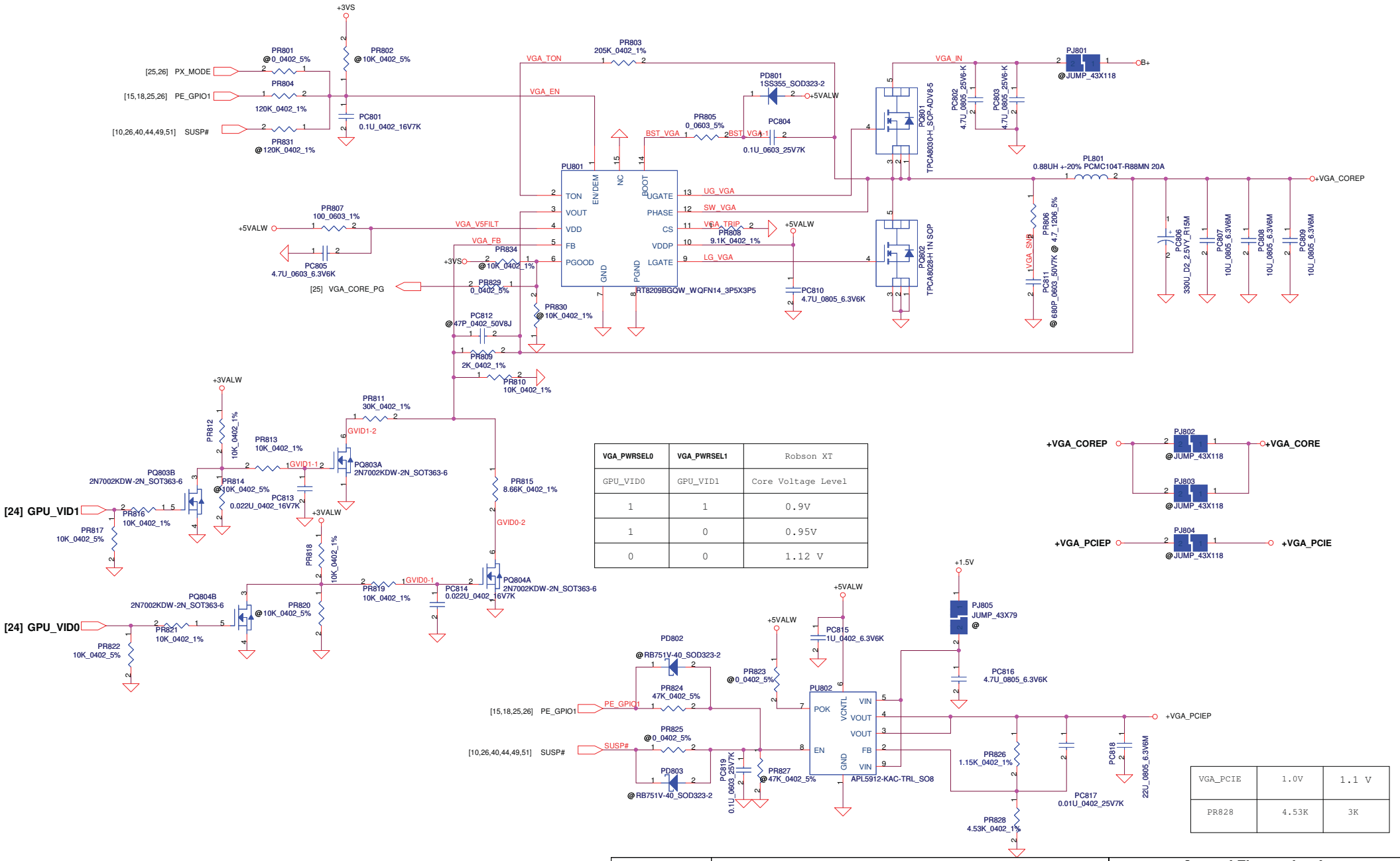
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PWR +1.05VS_VCCPP/+0.75VSP

Size	Document Number	Rev
Custom	PIWG4	0.1

Date: Tuesday, August 17, 2010 Sheet 51 of 57



VGA_PWRSEL0	VGA_PWRSEL1	Robson XT
GPU_VID0	GPU_VID1	Core Voltage Level
1	1	0.9V
1	0	0.95V
0	0	1.12 V

VGA_PCIE	1.0V	1.1 V
PR828	4.53K	3K

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2009/01/06	Deciphered Date	2010/01/06

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Title: VGA_CORE/PCIE

Size: | Document Number: PIWG4 | Rev: 0.1

Date: Tuesday, August 17, 2010 | Sheet 52 of 57

Alert# PU resister need close CPU,
so the PU resister in HW schematic.
but DAT and CLK need close PWM-IC,
so the PU resister in POWER schematic.

Parallel and tune length

change from 43P to 47P
for shortage problem
2010-03-15

*Iccmax in Turbo Mode for SV (35W) is 53A

+CPU_CORE

Icc-max=53A
Rdson=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1)10U_0805_4V *10
(2)22U_0805_6.3V *15
(3)470U_D2_2V *4(ESR=4.5m ohm)

*OCP setting value=71A

+VGFX_COREP

Ipeak=26A , Imax=18.2A , 1.2Ipeak=31.2A
Rdson=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1)22U_0805_6.3V *12
(2)470U_D2_2V *2(ESR=4.5m ohm)

*OCP setting value=37A

Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PWR +CPU_CORE/+VGFX_CORE

Size: Custom | Document Number: PIWG4 | Rev: 0.1

Date: Tuesday, August 17, 2010 | Sheet 53 of 57

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

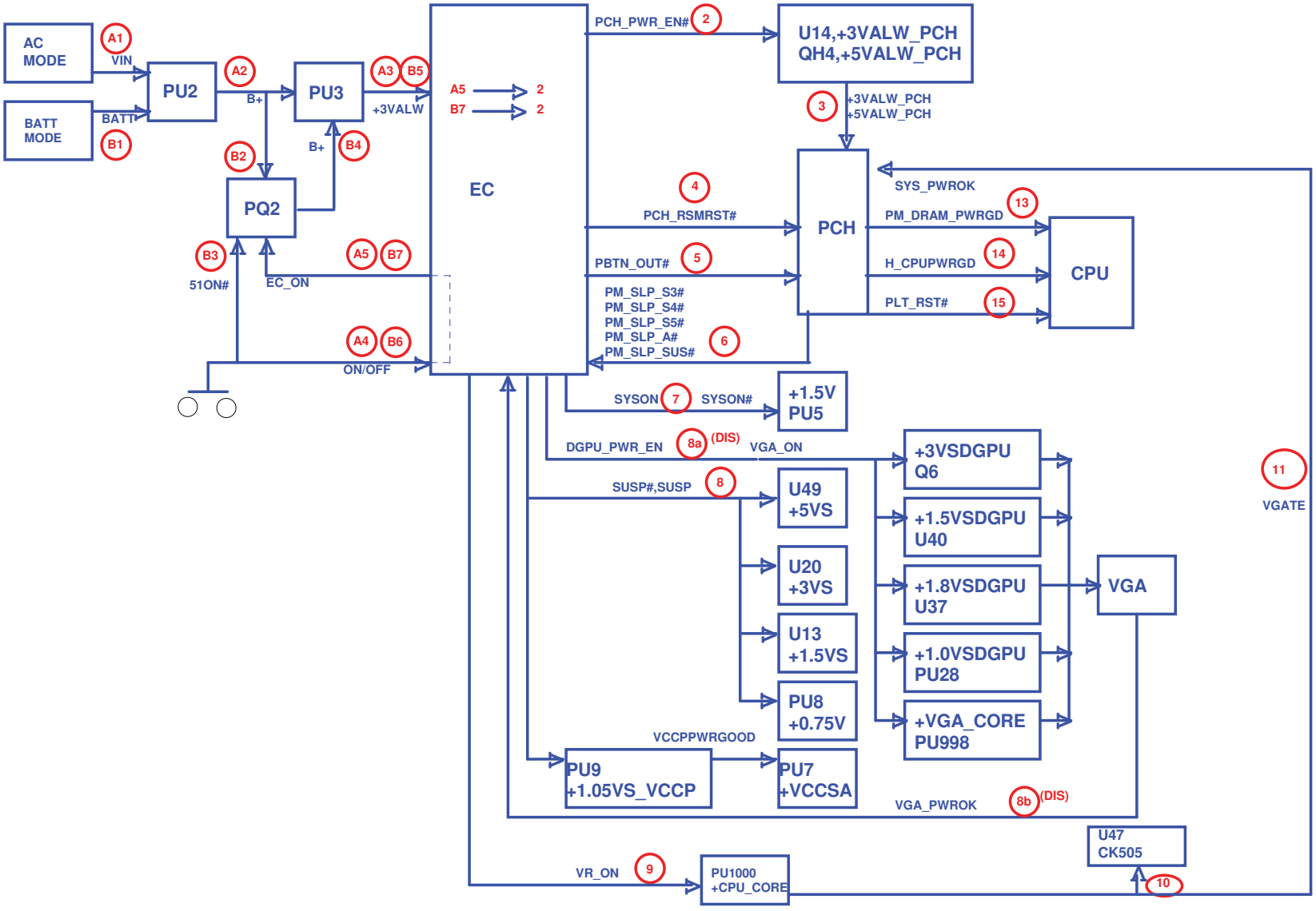
Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2009/01/06

Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number: PIWG4 | Rev: 0.1

Date: Tuesday, August 17, 2010 | Sheet 54 of 57



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

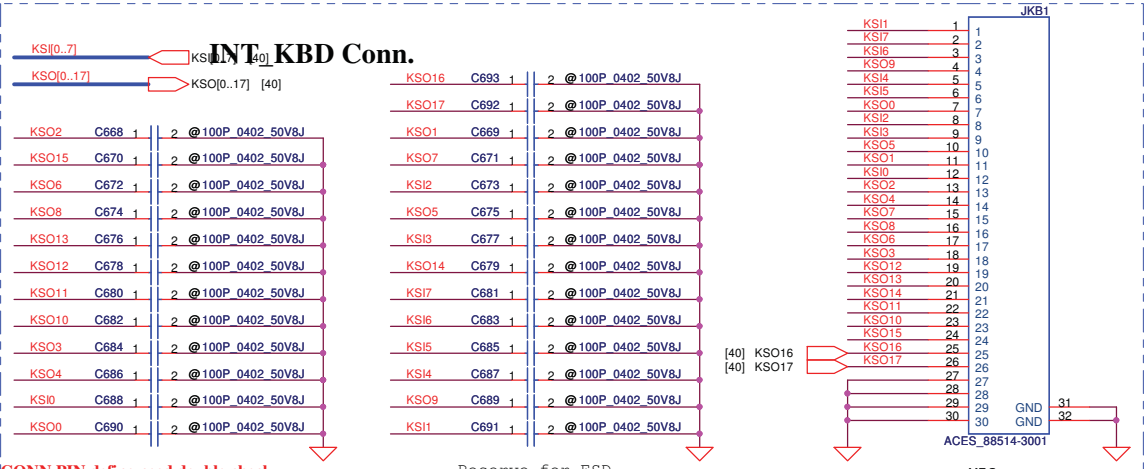
Compal Electronics, Inc.

Title: Power sequence

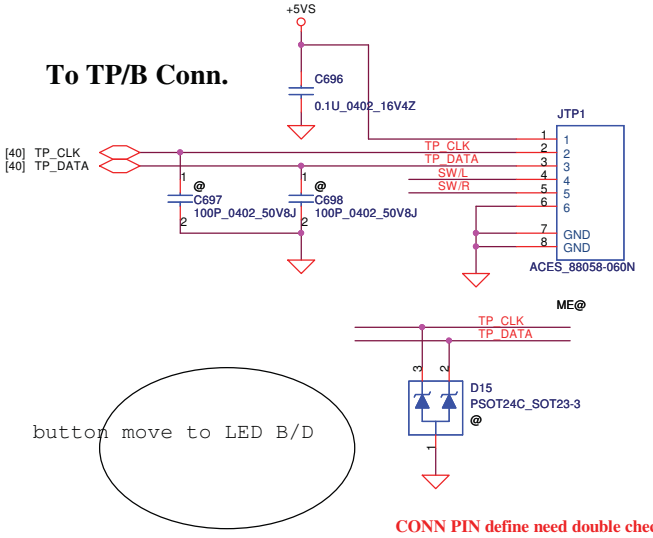
Size: Custom | Document Number: LA-6758P | Rev: 0.1

Date: Tuesday, August 17, 2010 | Sheet 55 of 57

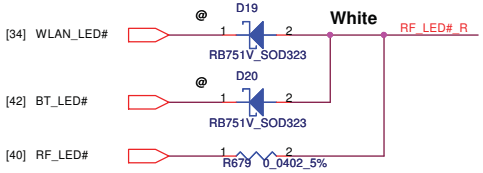
INT_KBD Conn.

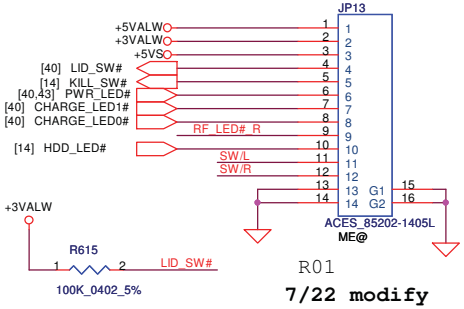


To TP/B Conn.



For 17" M/B to LED/B



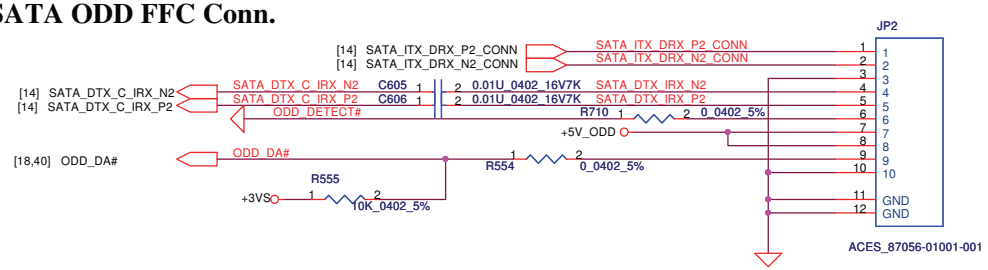


R01
7/22 modify

VRAM screw hole

Fan screw hole

SATA ODD FFC Conn.



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PHASE	PAGE	Modification list	PURPOSE
0.2	P31	Change CRT Symbol	For CRT footprint issue
0.2	P31	Del C510	For Non-used part
0.2	P39	change C610 pin 1 net name	change C610 pin 1 net name to correct
0.2	P35	U25 change to U26	For co-lay 10/100 and GIGA
0.2	P32	Add R735,R736	For DIS only SMBus pull high
0.2	P33	Add R738,R739	For DIS only SMBus pull high
0.2	P33	Change Q63 BOM structure to HDMI@	For DIS HDMI function
0.2	P40	Add R740, C93	For EC request
0.2	P18	Change R215 pin1 net name	Change R215 pin1 net name to correct
0.2	P18	Add R741	Add R741 for Reserved PE_GPIO0
0.2	P16	Add R742, R743	For PCH power sequence
0.2	P38	Del U28, R542~R551 , J12	Del USB charger circuit
0.2	P40	Add EC pin 97,98,103	Add EC pin 97 for SYS_PWROK_EC , pin 98 for CE_EN , pin 103 for BATT_SEL_EC
0.2	P24	Change R662 pin 2 net name	Change R662 pin 2 net name to correct
0.2	P28	Del C421,C422,C431,C432,C433, L27, Add R745, U8 pin N11,N12 change to NC	For AMD new document suggestion
0.2	P26	Add R744	Add R744 for control PE_GPIO1 from SUSP#
0.2	P39	Change J10 footprint and Add J13	Change J10 footprint by DFx request and Add J13 by vendor suggestion
0.2	P39	Change PC_Beep circuit	Change PC_Beep circuit
0.2	P6	Add R161, R182, R192 BOM structure hange to @	Follow ORB circuit
0.2	P58/59	Add R615 in 15" and 17" page	Pull high LID_SW# at M/B side
0.2	P31	Add Q83 pin 1 power net name +CMOS_PW	For power trace net
0.2	P56/57/58	Change JP21 to JKB1	Change connector to standard name
0.2	P56/57/58	Change JP4 to JTP1	Change connector to standard name
0.2	P43/60	Change JP6 to JPWRB1	Change connector to standard name
0.2	P34	Change JP1 to JWLN1	Change connector to standard name
0.2	P42	Change JP5 to JBT1	Change connector to standard name
0.2	P43/60	Change JP7 to JCR1	Change connector to standard name
0.2	P19	Add R542	For ESATA detect function
0.2	P42	Add R886, R887 , C735	For ESATA detect function
0.2	P31	Add R543	For reserve EC control directly
0.2	P39	Change J10 footprint, Del C635, C636	Change J10 for DFx and Del component for layout
0.2	P42	Add R877	For reserve EC control directly
0.2	P42	SW3 BOM structure change to @	For ME ASSY concern
0.2	P24	R324 BOM structure change, del @	For AMD update
0.2	P25	Change Q69,Q70,Q71,Q72 to BSS138, change Q66,Q67 pin 1 net name, D28 change to @	For Change BACO part follow AMD reference DATA ,D28 change to @ for leakage
0.2	P42	Change ESATA from port 5 to port 4	For intel risk
0.2	P15	Add R544,R545	For Pull high SMBus
0.2	P12/13	Del R74~R80,R82 R88~R94,R96	For DDR3 DM Bus to GND
0.2	P16	Add R182,R546	Add 186 for reserve sequence, Add R546 for follow CRB & ORB
0.2	P20	Del Add J12, R257 change to @	For voltage drop

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