KIWB3/B4

Schematics Document

Mobile Penryn uFCPGA with Intel Cantiga_GM/PM+ICH9-M core logic

REV:0.1

Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

Compal Electronics,Ltd.

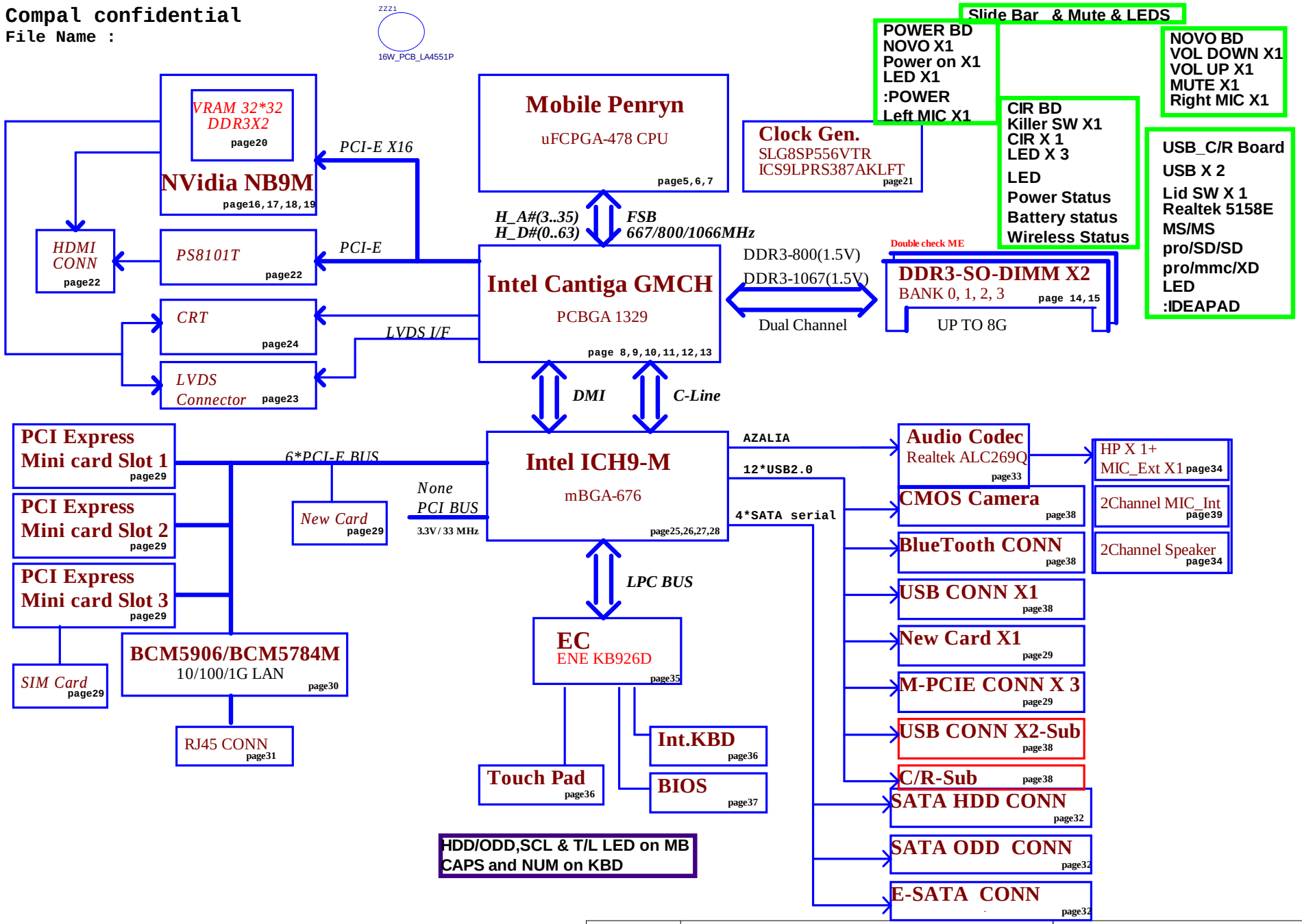
Title: **Cover Sheet**

Size: B | Document Number: **KIWB3/B4_LA4551P** | Rev: 0.1

Date: Friday, June 27, 2008 | Sheet 1 of 49

Compal confidential
File Name :

ZZZ1
16W_PCB_LA4551P



Security Classification	Compal Secret Data		
Issued Date	2008/03/24	Deciphered Date	2008/04/

Compal Electronics, Inc.

Title: *MB Block Diagram*

Size	Document Number	Rev
Custom	*KIWB3/B4_LA4551P*	0.1

Date: Friday, June 27, 2008 Sheet 2 of 49

DDR3 Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V +1.8V +0.75V	+5VS +3VS +1.5VS +1.1VS +VCCP +CPU_CORE +VGA_CORE +1.8VS
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

PM@ , GM@ , N9@ , N10@

SMBUS, SPI and I2C Control Table

	SOURCE	HDMI	LVDS	CRT	HDCP	SERIAL EEPROM	NEW CARD	CLK GEN	CAP sensor	Mini CARD1	Mini CARD2	BATT	THERMAL SENSOR (VGA)	THERMAL SENSOR (CPU)
EC_SMB_CK1 EC_SMB_DA1	KB926	X	X	X	X	V	X	X	X	X	X	V	X	X
EC_SMB_CK2 EC_SMB_DA2	KB926	X	X	X	X	X	X	X	V	X	X	X	V	V
ICH_SMBCLK ICH_SMBDAT	ICH9	X	X	X	X	X	V	V	X	V	V	X	X	X
LVDS_SCL LVDS_SDA	Cantiga	X	V	X	X	X	X	X	X	X	X	X	X	X
GMCH_CRT_CLK GMCH_CRT_DAT	Cantiga	X	X	V	X	X	X	X	X	X	X	X	X	X
HDMICLK_NB HDMIDAT_NB	Cantiga	V	X	X	X	X	X	X	X	X	X	X	X	X
VGA_DDCCLK VGA_DDCDATA	VGA	X	X	V	X	X	X	X	X	X	X	X	X	X
VGA_LVDS_SCL VGA_LVDS_DAT	VGA	X	V	X	X	X	X	X	X	X	X	X	X	X
VGA_HDMI_SCL VGA_HDMI_DAT	VGA	V	X	X	X	X	X	X	X	X	X	X	X	X
HDCP_SMB_CK1 HDCP_SMB_DA1	VGA	X	X	X	X	V	X	X	X	X	X	X	X	X
FSEL#SPICS#_SB FRD#SPI_SO_SB SPI_CLK_SB FWR#SPI_SI_SB	ICH9	X	X	X	X	V	X	X	X	X	X	X	X	X
FSEL#SPICS# FRD#SPI_SO SPI_CLK FWR#SPI_SI	KB926	X	X	X	X	V	X	X	X	X	X	X	X	X

Security Classification	Compal Secret Data		
Issued Date	2008/03/24	Deciphered Date	2008/04/

Compal Electronics, Inc.

Title: MB Notes List

Size: B | Document Number: KIWB3/B4_LA4551P | Rev: 0.1

Date: Friday, June 27, 2008 | Sheet 3 of 49

VGA and DDR2 Voltage Rails (NB9M-GS)

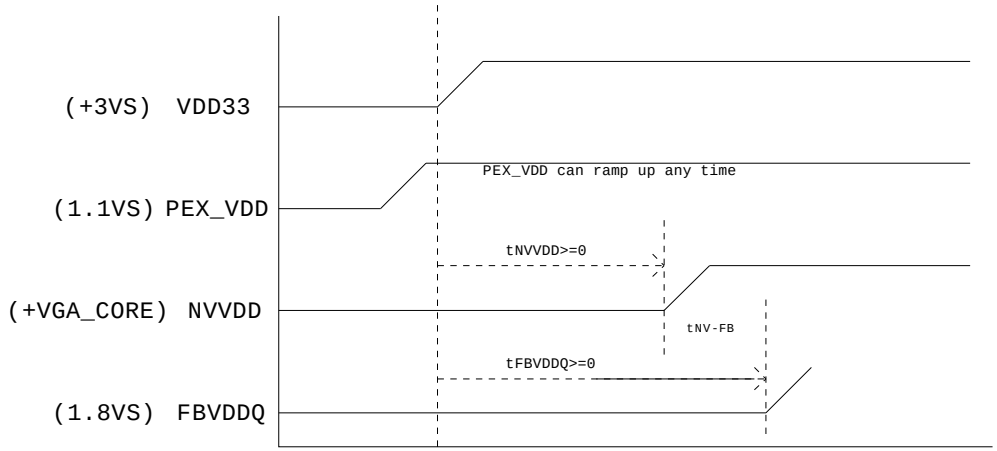
power plane / State			+1.8V	+3VS +VGA_CORE +1.1VS
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

EDP at Tj = 97C*

Power Supply Rail	(V)	NB9M-GS		NB9M-GE	
		GDDR3	DDR2	GDDR3	DDR2
NVVDD	Variable	11.22A	10.87A	9.2A	8.88A
FB_DLLAVDD	1.1	25mA			
FB_PLLAVDD	1.1	10mA			
IFPC_IOVDD	1.1	385mA			
IFPD_IOVDD	1.1	385mA			
IFPE_IOVDD	1.1	385mA			
IFPF_IOVDD	1.1	385mA			
PEX_IOVDD/Q	1.1	1550mA			
PEX_PLLVDD	1.1	165mA			
PLLVDD	1.1	55mA			
SP_PLLVDD	1.1	25mA			
VID_PLLVDD	1.1	50mA			
TOTAL	1.1	3.425A			
FBVDD/Q	1.8	2.24A	1.65A	2.17A	1.63A
IFPA_IOVDD	1.8	50mA			
IFPB_IOVDD	1.8	50mA			
IFPAB_PLLVDD	1.8	100mA			
IFPCD_PLLVDD	1.8	160mA			
IFPEF_PLLVDD	1.8	160mA			
TOTAL	1.8	2.76A	2.17A	2.69A	2.15A
DACA_VDD	3.3	110mA			
DACB_VDD	3.3	125mA			
DACC_VDD	3.3	110mA			
MIOA_VDDQ	3.3	10mA			
MIOB_VDDQ	3.3	10mA			
VDD33	3.3	80mA			
TOTAL	3.3	0.445A			

POWER SQUENCE

The ramp time for any rail must be more than 40us

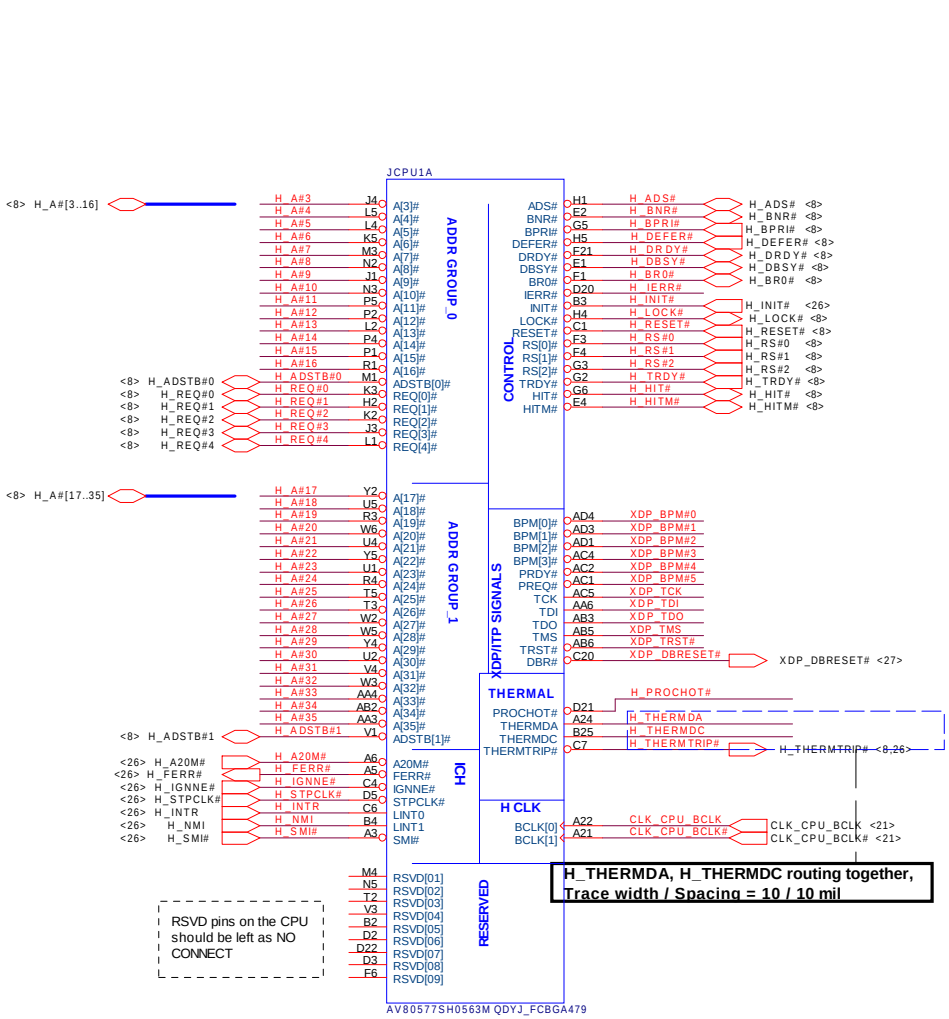


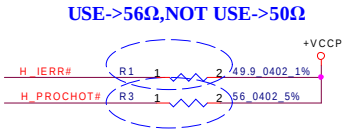
Compal Electronics, Inc.

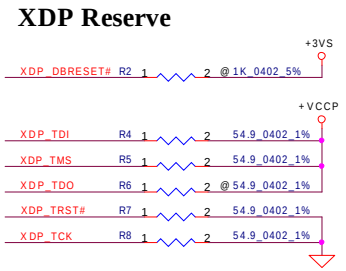
Title: VGA Notes List

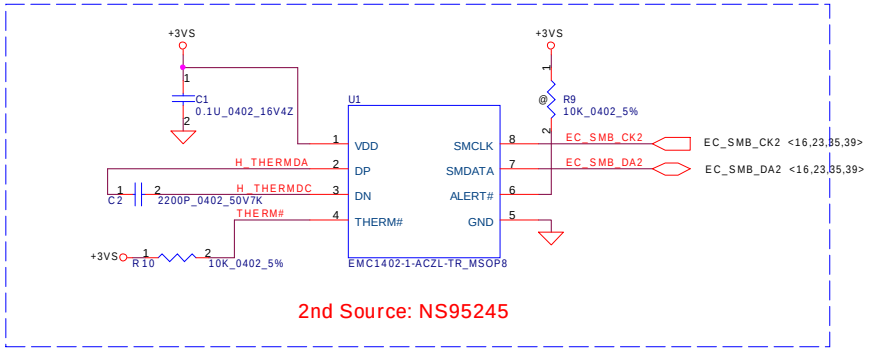
Size: B | Document Number: KIWB3/B4_LA4551P | Rev: 0.1

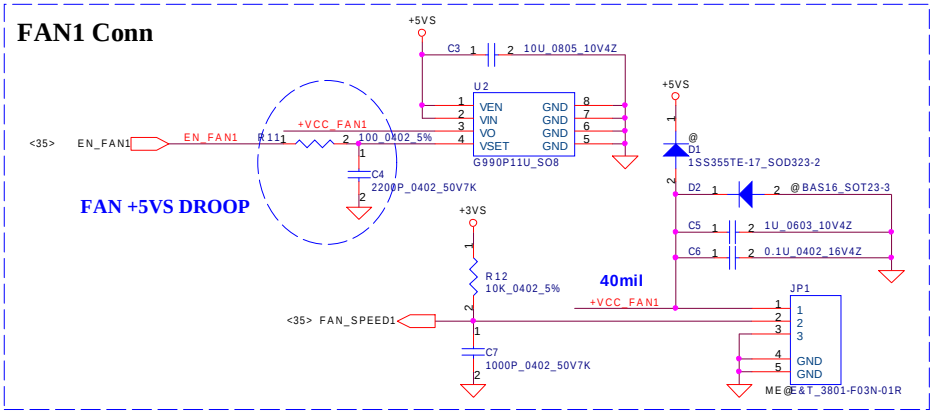
Date: Friday, June 27, 2008 | Sheet 4 of 49











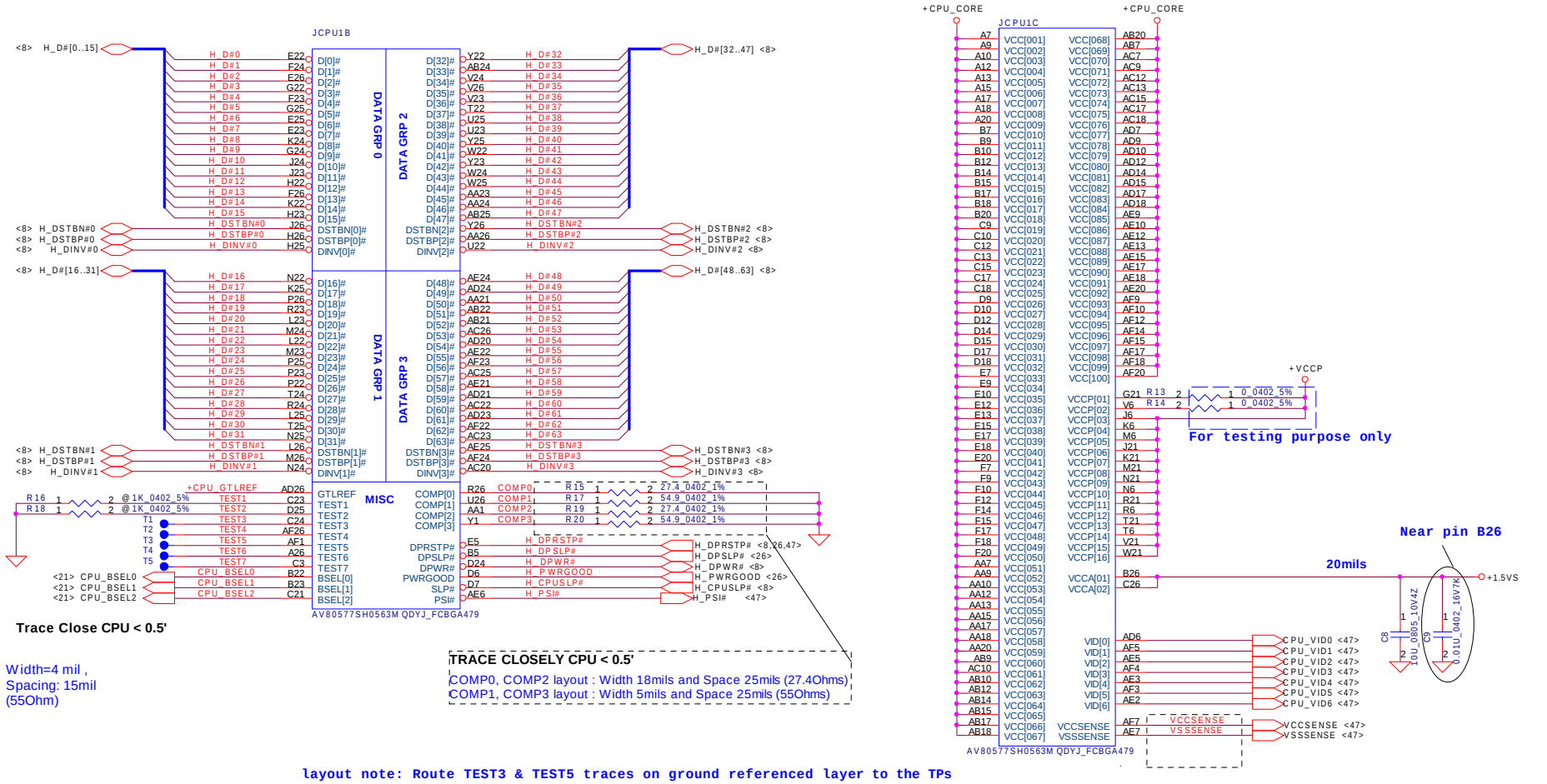
Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

Compal Electronics,Ltd.

Title: Penryn(1/3)

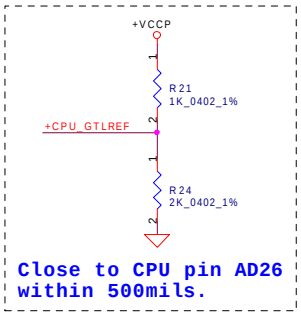
Size: Custom | Document Number: KIWB3/B4_LA4551P | Rev: 0.1

Date: Friday, June 27, 2008 | Sheet 5 of 49



layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

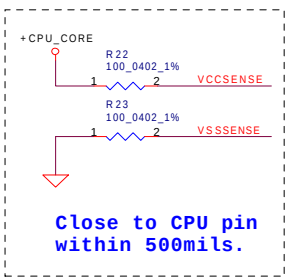
Layout note: Z0=55 ohm
0.5" max for GTLREF.



FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

Length match within 25 mils.
The trace width/space/other is 18/7/25.

Layout Note:
Route VCCSENSE and VSSSENSE traces at 27.4 Ohms with 50 mil spacing.
Place PU and PD within 1 inch of CPU.
Length matched to within 25 mils.



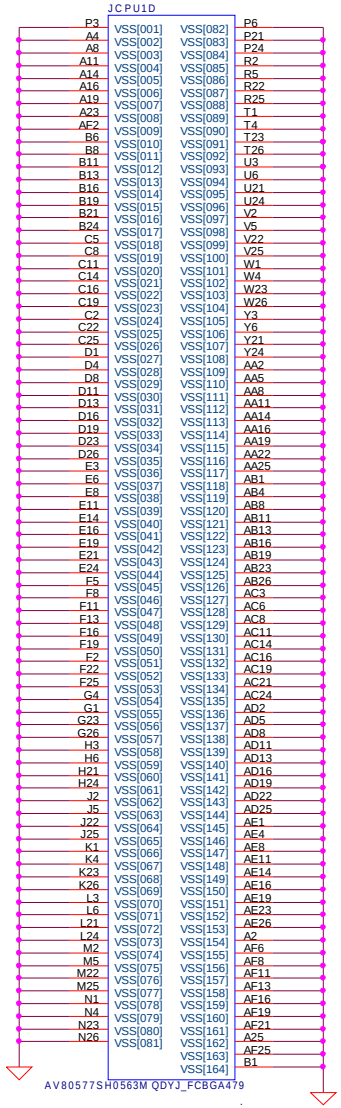
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

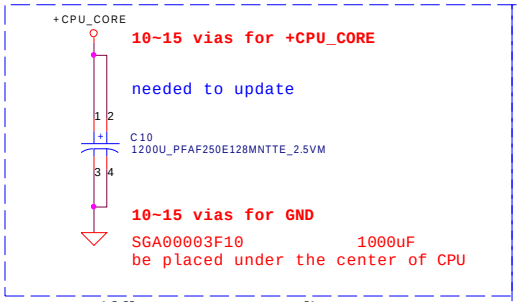
Compal Electronics, Inc.

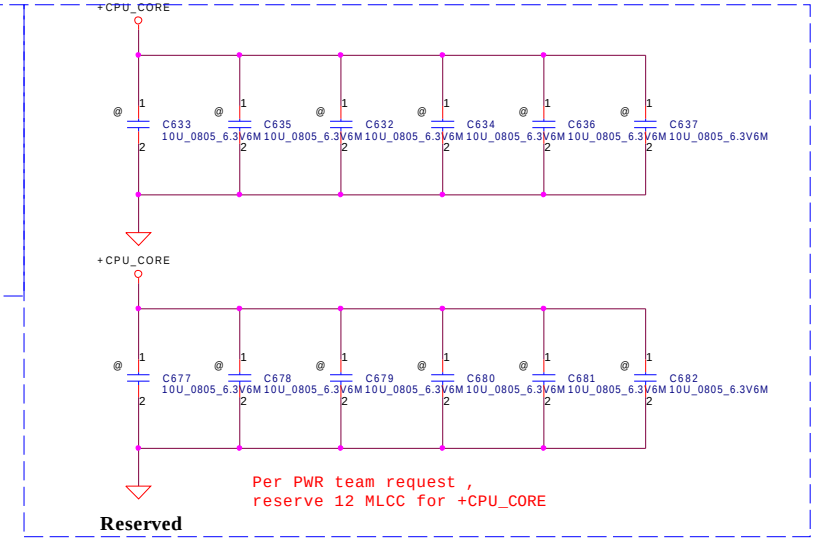
Title: **Penryn (2/3)**

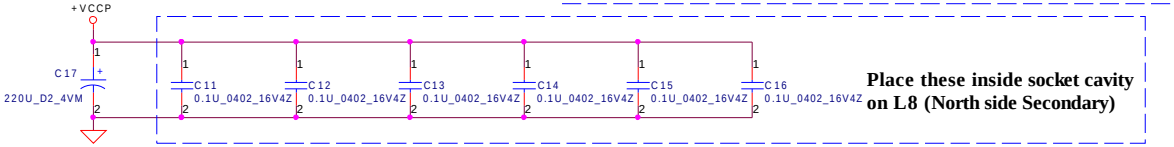
Size	Document Number	Rev
B	KIWB3/B4_LA4551P	0.1

Date: Friday, June 27, 2008 Sheet 6 of 49









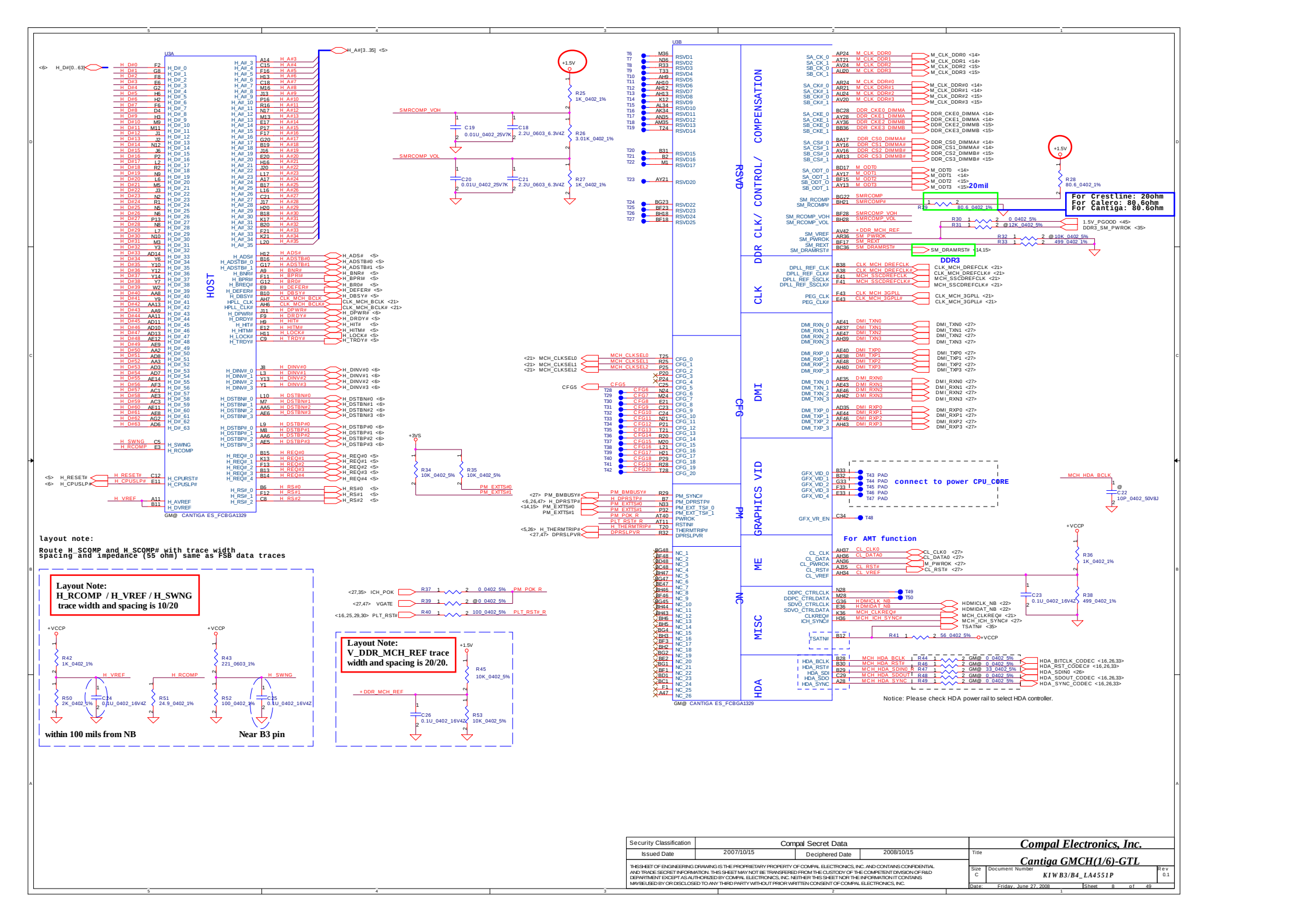
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **Penryn (3/3)**

Size	Document Number	Rev
B	KIWB3/B4_LA4551P	0.1

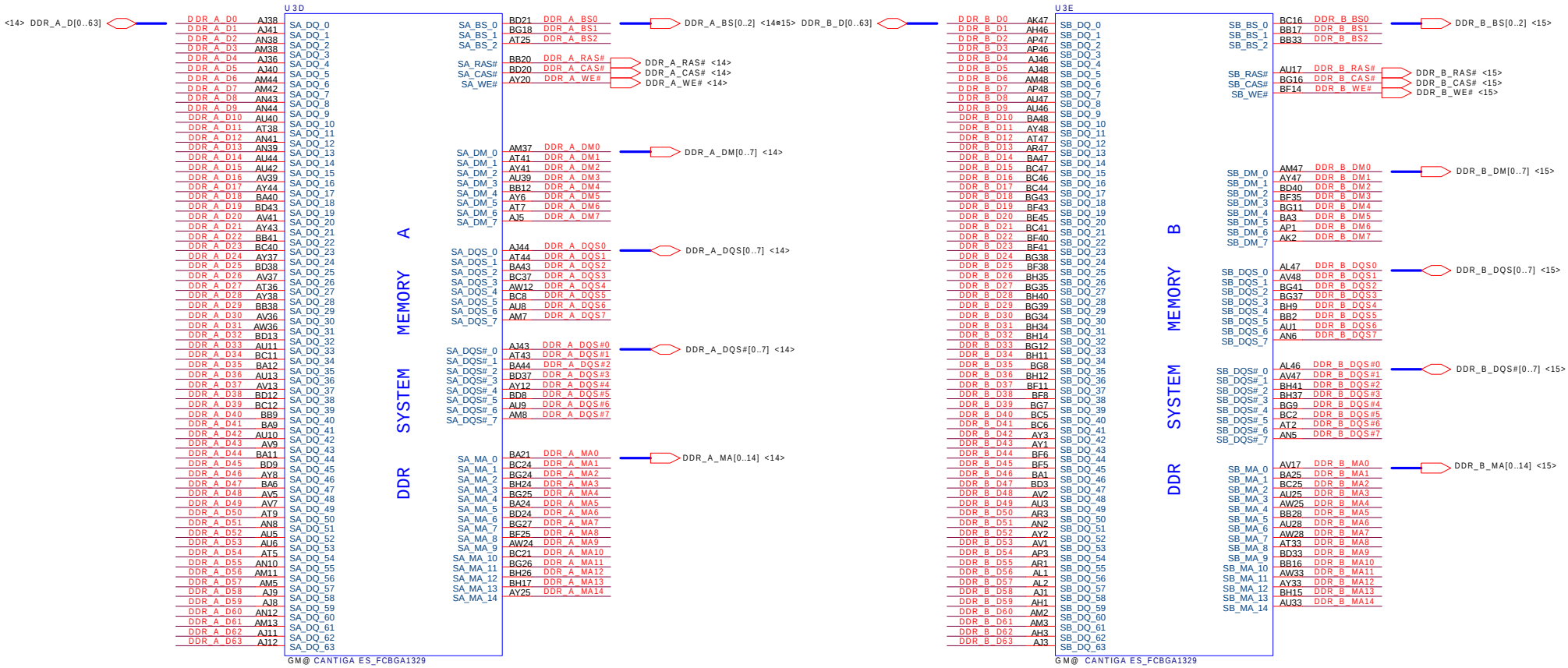
Date: Friday, June 27, 2008 Sheet 7 of 49



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.	
Title	Cantiga GMCH(1/6)-GTL
Size C	Document Number KIWB3/B4_LA4551P
Rev	0.1
Date: Friday, June 27, 2008	Sheet 8 of 49

MEMORY 7-GROUPS
1. Data Bus;
2. Data Strobe Differential Pairs;
3. Data Mask Bits;
4. Address Group;
5. Bank Select Group;
6. Command Group;
7. CLK Group;
*. Reset Group;



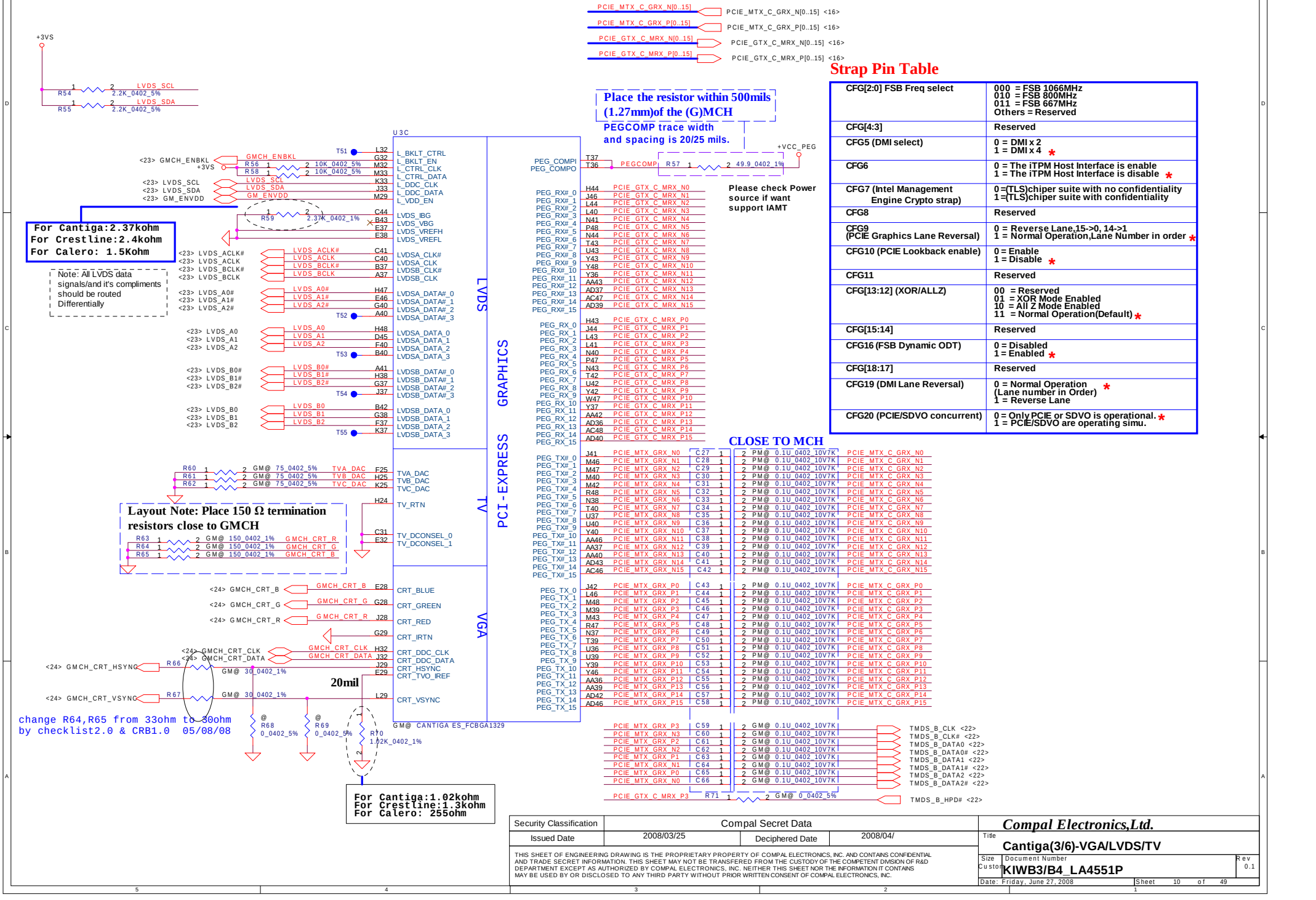
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

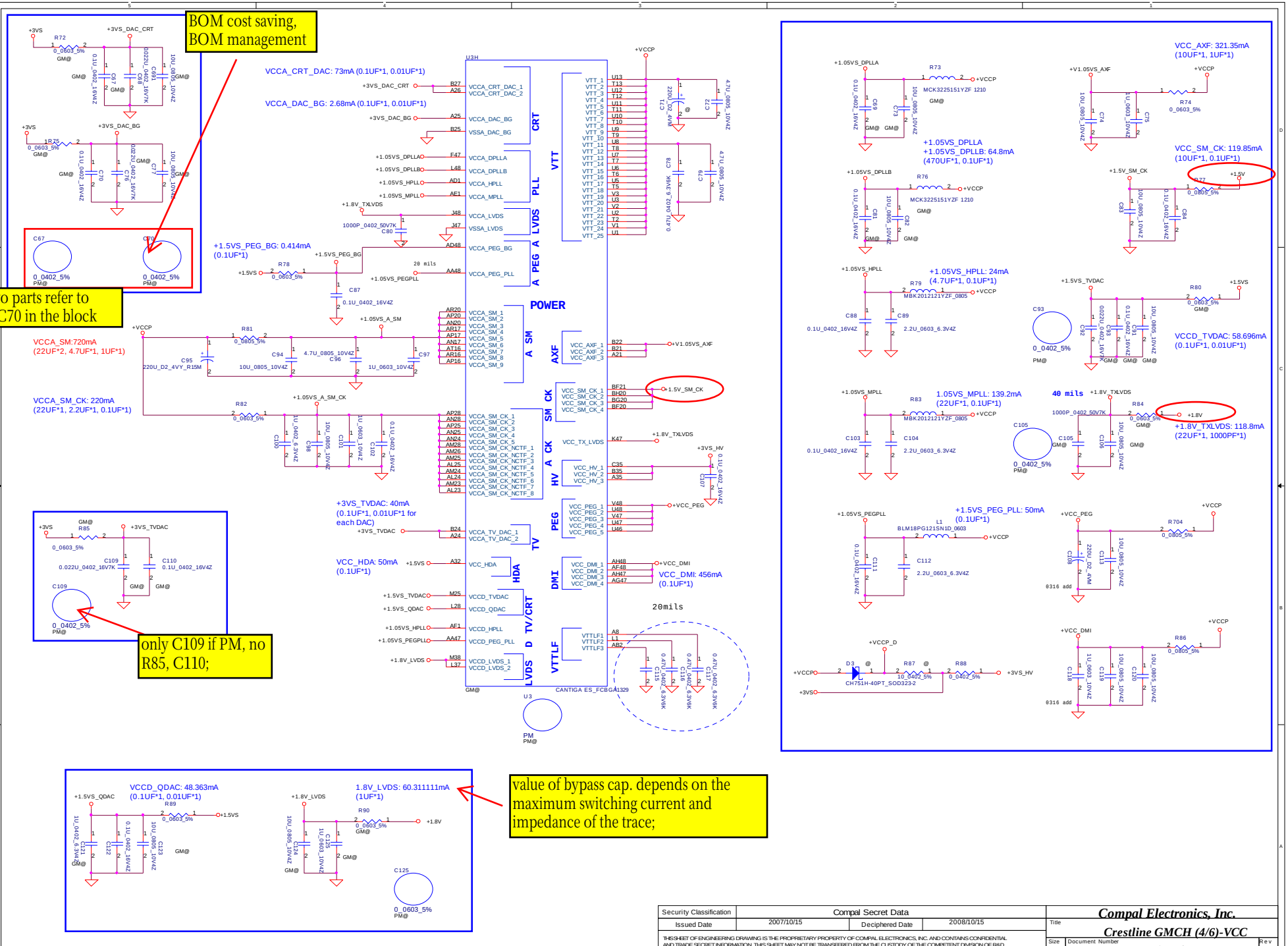
Compal Electronics, Inc.

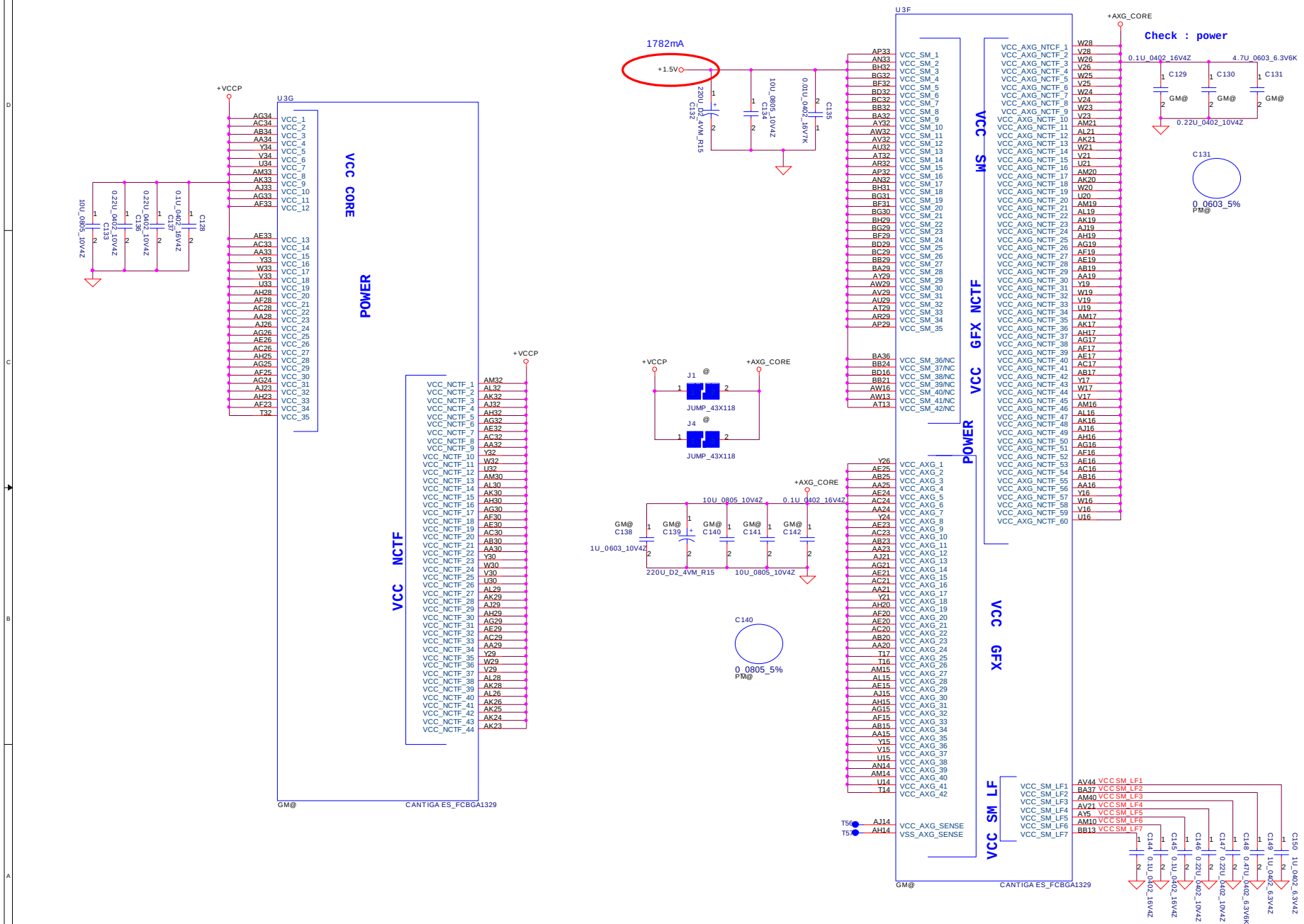
Title: **Cantiga GMCH (2/6)-DDRII**

Size	Document Number	Rev
B	KIWB3/B4_LA4551P	0.1

Date: Friday, June 27, 2008 | Sheet 9 of 49




BOM cost saving, BOM management
the two parts refer to C67, C70 in the block
only C109 if PM, no R85, C110;
value of bypass cap. depends on the maximum switching current and impedance of the trace;
VCCA_CRT_DAC: 73mA (0.1UF*1, 0.01UF*1)
VCCA_DAC_BG: 2.68mA (0.1UF*1, 0.01UF*1)
+1.5VS_PEG_BG: 0.414mA (0.1UF*1)
VCCA_SM:720mA (22UF*2, 4.7UF*1, 1UF*1)
VCCA_SM_CK: 220mA (22UF*1, 2.2UF*1, 0.1UF*1)
+3VS_TVDAC: 40mA (0.1UF*1, 0.01UF*1 for each DAC)
VCC_HDA: 50mA (0.1UF*1)
VCC_DMI: 456mA (0.1UF*1)
VCCD_QDAC: 48.363mA (0.1UF*1, 0.01UF*1)
1.8V_LVDS: 60.311111mA (1UF*1)
+1.05VS_DPLLA +1.05VS_DPLLB: 64.8mA (470UF*1, 0.1UF*1)
+1.05VS_HPLL: 24mA (4.7UF*1, 0.1UF*1)
1.05VS_MPLL: 139.2mA (22UF*1, 0.1UF*1)
+1.5VS_PEG_PLL: 50mA (0.1UF*1)
VCC_AXF: 321.35mA (10UF*1, 1UF*1)
VCC_SM_CK: 119.85mA (10UF*1, 0.1UF*1)
VCCD_TVDAC: 58.696mA (0.1UF*1, 0.01UF*1)
+1.8V_TXLVDS: 118.8mA (22UF*1, 1000PF*1)
CRT
VTT
PLL
LVDS
A PEG
POWER
A SM
AXF
SM CK
A CK
HV
PEG
TV
HDA
DMI
D TV/CRT
D VTTLF
LVDS
CANTIGA ES_FCBGA1329
20mils
40 mils
0316 add
PM
Security Classification
Compal Secret Data
Issued Date
2007/10/15
Deciphered Date
2008/10/15
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.
Compal Electronics, Inc.
Title
Crestline GMCH (4/6)-VCC
Size
Custom
Document Number
KIWB3/B4_LA4551P
Rev
0.1
Date:
Friday, June 27, 2008
Sheet
11
of
49



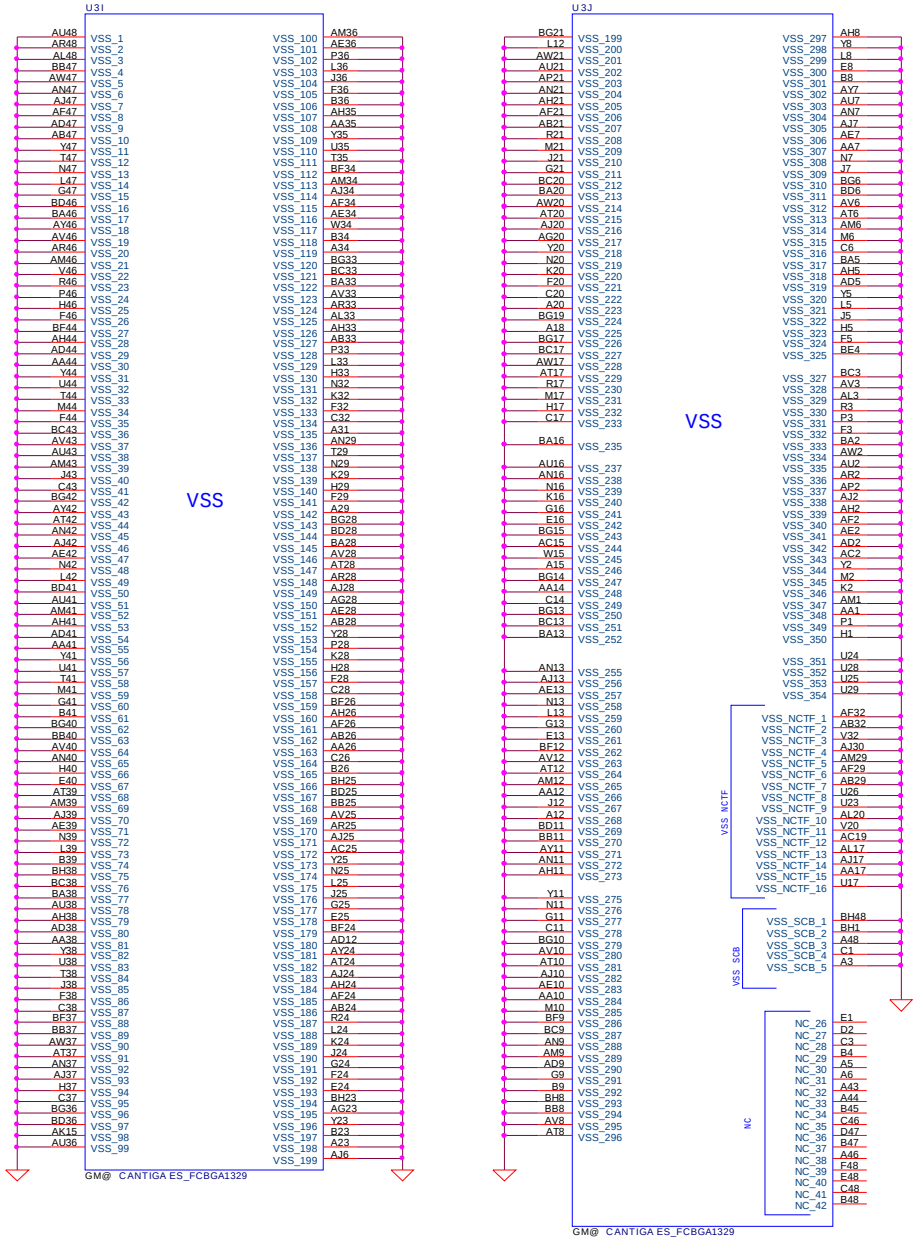
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **Crestline GMCH (5/6)-VCC**

Size	Document Number	Rev
Custom	KIWB3/B4_LA4551P	0.1

Date: Friday, June 27, 2008 | Sheet 12 of 49



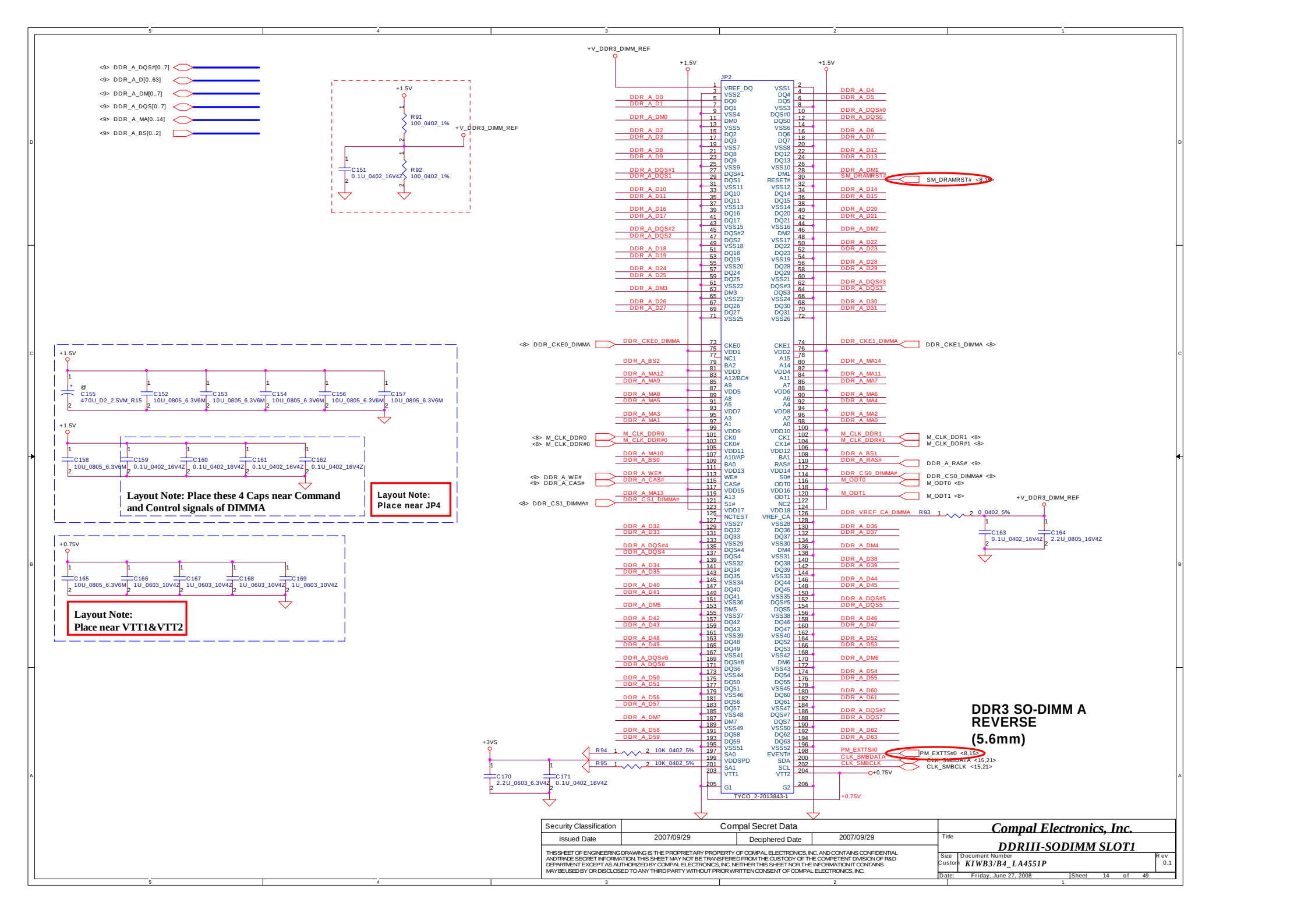
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **Cantiga GMCH (6/6)-GND**

Size	Document Number	Rev
Custom	KIWB3/B4_LA4551P	0.1

Date: Friday, June 27, 2008 | Sheet 13 of 49



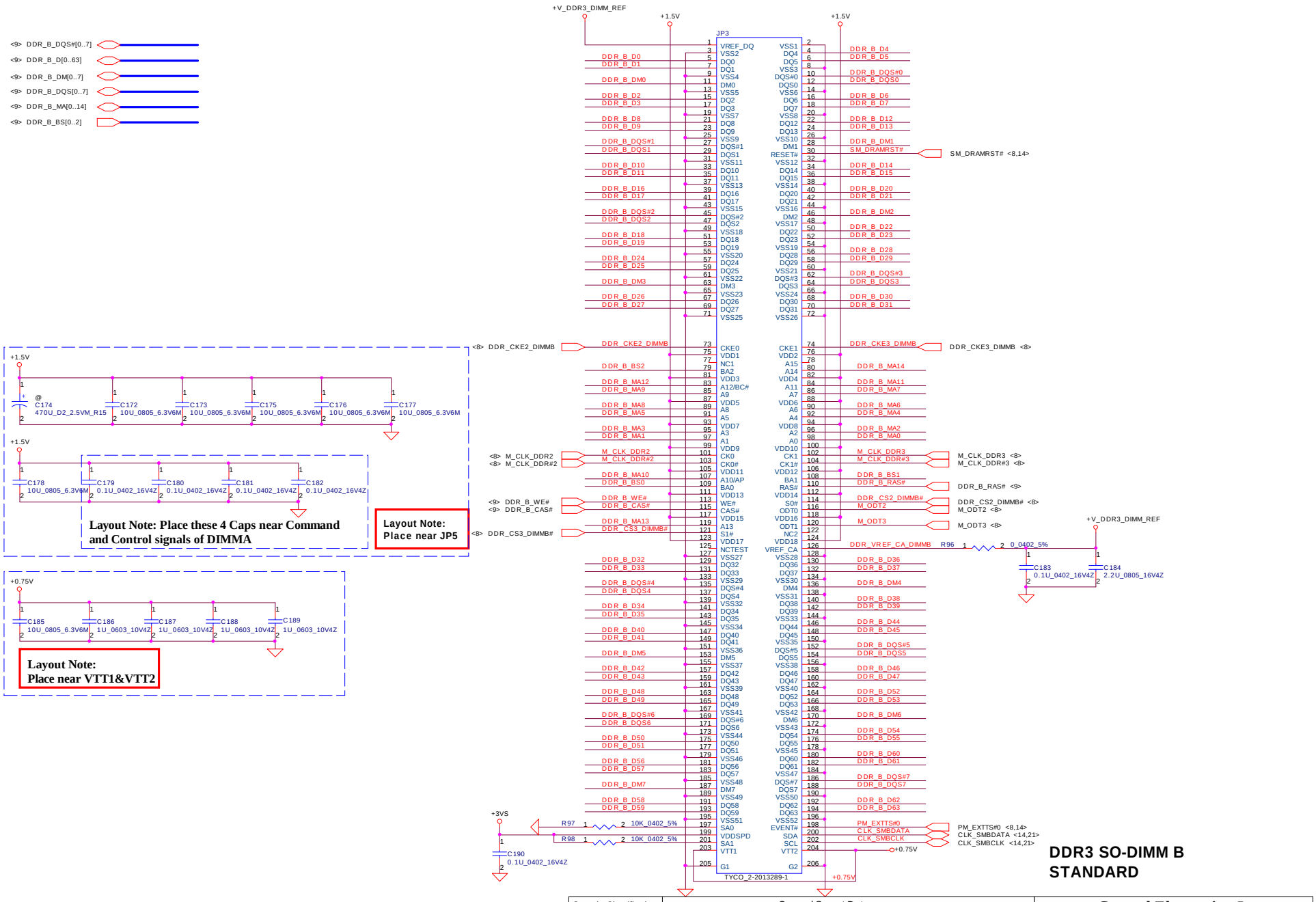
Security Classification	Compal Secret Data		
Issued Date	2007/09/29	Deciphered Date	2007/09/29

Compal Electronics, Inc.

Title: **DDRIII-SODIMM SLOT1**

Size	Document Number	Rev
Custom	KIWB3/B4_LA4551P	0.1

Date: Friday, June 27, 2008 Sheet 14 of 49



Security Classification	Compal Secret Data		
Issued Date	2007/09/29	Deciphered Date	2007/09/29

Compal Electronics, Inc.			
Title	DDRIII-SODIMM SLOT2		
Size	Document Number		Rev
	KIWB3/B4_LA4551P		0.1
Date:	Friday, June 27, 2008	Sheet	15 of 49

GPU_VID1	GPU_VID0	VGA_CORE	P-State
0	0	0.9V	10,12
1	1	1.17V	0
0	1	1.09V	8

U5A

Part 1 of 5

NB9M-GS_BGA533

PM@

For N10M

For N10M

so change the port for HDMI I2C

For N10M

CRT OUT

EMI

If External Spread Spectrum not stuff than stuff resistor

External Spread Spectrum

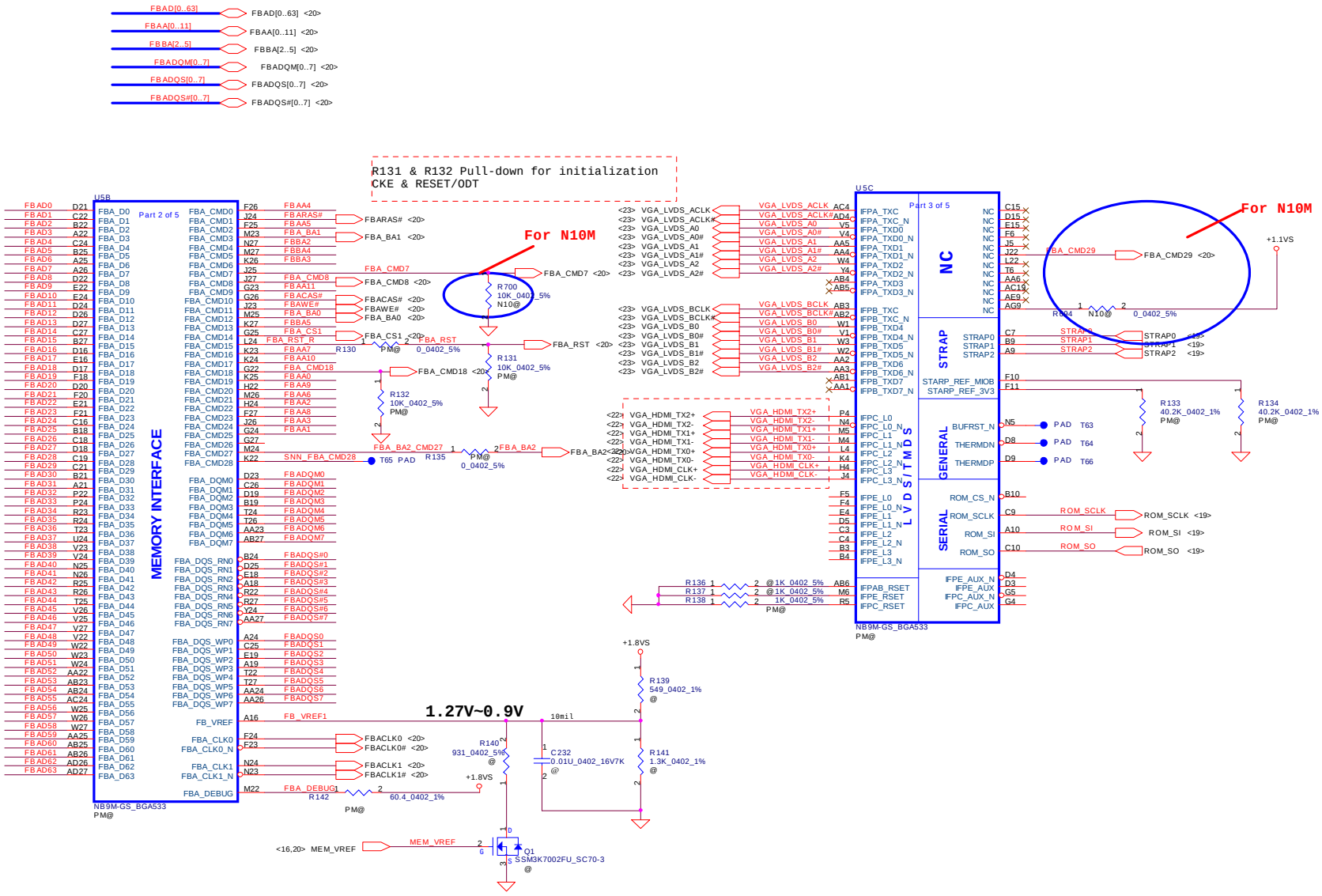
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: NB9M-GS PCIE,LVDS,GPIO,CLK

Size	Document Number	Rev
B	KIWB3/B4_LA-4551P	0.1

Date: Friday, June 27, 2008 Sheet 16 of 49



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: NB9M-GS Memory

Size	Document Number	Rev
B	KIWB3/B4_LA-4551P	0.1

Date: Friday, June 27, 2008 Sheet 17 of 49

FOR N10M , 1.1VS will changed to 1.05VS

+VGA_CORE

11.57A NEAR BALL

0.1U_0402_16V4Z 0.1U_0402_16V4Z 0.1U_0402_16V4Z

220U_D2_4VM 330U_D2_4VM

C240 C241 C242 C243 C244 C245

@PM@ PM@ PM@ PM@ PM@ PM@

0.1U_0402_16V4Z 0.1U_0402_16V4Z 0.1U_0402_16V4Z

0.47U_0402_6.3V6K 0.47U_0402_6.3V6K

C252 C253 C254 C255 C256 C257

PM@ PM@ PM@ PM@ PM@ PM@

0.47U_0402_6.3V6K

0.47U_0402_6.3V6K 0.47U_0402_6.3V6K 0.47U_0402_6.3V6K

4.7U 6.3V K X5R 0603

C263 C264 PM@ PM@

NEAR BGA

4.7U 6.3V K X5R 0603

+3VS

NEAR BGA 110mA

C273 PM@

1U_0603_10V4Z

NEAR BALL

0.1U_0402_16V4Z

C274 C275 PM@ PM@

0.1U_0402_16V4Z

U5D

Part 4 of 5

POWER

VDD: J9 J10 J12 J13 L9 M9 M11 M17 N9 N11 N12 N13 N14 N15 N16 N17 N19 P11 P12 P13 P14 P15 P16 P17 R9 R11 R12 R13 R14 R15 R16 R17 T9 T11 T17 U9 U19 W9 W10 W12 W13 W18 W19

VDD33: A12 B12 C12 D12 E12 F12

FBVDDQ: A13 B13 C13 D13 D14 E13 F13 F14 F15 F16 F17 F19 F22 H23 H26 J15 J16 J18 J19 L19 L23 L26 M19 N22 U22 Y22

PEX_IOVDDQ: AG6 AF6 AE6 AD6 AC13 AC7 AB17 AB16 AB13 AB9 AB8 AB7 AG7 AF7 AE7 AD8 AD7 AC9

PEX_IOVDD: AF9 K6 L6 K5

PEX_PLLVDD

VID_PLLVDD

SP_PLLVDD

PLLVDD

IFPA_IOVDD V3

IFPB_IOVDD V2

IFPC_IOVDD J6

IFPE_IOVDD

IFPAB_PLLVDD AD5

IFPC_PLLVDD P6

IFPE_PLLVDD N6

FB_PLLAVDD R19

FB_DLLAVDD T19

FB_CAL_PD_VDDQ B15

DACA_VDD AG2

DACB_VDD D7

DACC_VDD W5

NB9M-GS_BGA533

PM@

PLACE NEAR BGA

+1.8VS

0.022U_0402_16V7K 0.1U_0402_16V4Z 4.7U 6.3V K X5R 0603

C233 C234 C235 C236 C237 @ C238

PM@ PM@ PM@ PM@ PM@

0.022U_0402_16V7K 0.1U_0402_16V4Z 4.7U 6.3V K X5R 0603

PLACE BELOW GPU FBAVDDQ=1.72A

+1.8VS

4700P_0402_25V7K 4700P_0402_25V7K 1U_0603_10V4Z

C246 C247 C248 C249 C250 C251

PM@

4700P_0402_25V7K 0.022U_0402_16V7K 0.1U_0402_16V4Z

+1.8VS

4700P_0402_25V7K 0.022U_0402_16V7K 1U_0603_10V4Z

C258 C259 C260 C261 C262

PM@

4700P_0402_25V7K 0.1U_0402_16V4Z

0.1U_0402_16V4Z 0.47U_0402_6.3V6K

C265 C266 C267 C268

PM@

0.1U_0402_16V4Z 0.47U_0402_6.3V6K

1U_0402_6.3V4Z

C269 PM@

NEAR BALL

PEX_IOVDDQ=1.6A
PEX_IOVDD=500mA
PEX_PLLVDD=100mA

+1.1VS

10U_0805_10V4Z

C270 C271 C272

PM@

4.7U 6.3V K X5R 0603 10U_0805_10V4Z

+PEX_PLLVDD +1.1VS_PLL

12~16mil

0.1U_0402_16V4Z 1U_0402_6.3V6K

MBK1608121YZF_0603 +1.1VS

C276 C277 C278 C279 C280

PM@

0.1U_0402_16V4Z 1U_0402_6.3V6K 1U_0402_6.3V6K

NEAR BALL

PLLVDD=65mA
SP_PLLVDD=25mA
VID_PLLVDD=50mA

IFPA/B_IOVDD: please add option to support both 1.8V(for G9X) and 3.3V(for GT21X)

+1.8VS L7 MBK1608121YZF_0603 N9@

+3VS L41 MBK1608121YZF_0603 N10@

4700P_0402_25V7K 470P_0402_50V7K

C281 C282 C283

PM@

4.7U 6.3V K X5R 0603

110mA NEAR BGA

NEAR BALL

12~16mil

+IFPA_IOVDD

+IFPB_IOVDD +IFPC_IOVDD

10K_0402_5% R143

+IFPAB_PLLVDD +IFPC_PLLVDD

10K_0402_5% R146

+1.8VS L9 MBK1608121YZF_0603 N9@

+3VS L42 MBK1608121YZF_0603 N10@

4700P_0402_25V7K 470P_0402_50V7K

C287 C288 C289

PM@

4.7U 6.3V K X5R 0603

NEAR BGA

NEAR BALL

+FB_PLLAVDD

+FB_DLLAVDD

+DACA_VDD +DACB_VDD +DACC_VDD

R144 R145 10K_0402_5%

R147 44.2_0402_1%

+1.8VS

+1.1VS

+PEX_PLLVDD

0.1U_0402_16V4Z

C290 C291 C292

PM@

0.01U_0402_16V7K

10U_0805_10V4Z L10 MBK1608121YZF_0603

1U_0402_6.3V4Z C293

NEAR BALL

NEAR BGA

+1.1VS

+FB_PLLAVDD

0.1U_0402_16V4Z L8 MBK1608121YZF_0603

C284 C285 C286

PM@

0.01U_0402_16V7K 4.7U 6.3V K X5R 0603

+FB_DLLAVDD

0.1U_0402_16V4Z L11 MBK1608121YZF_0603

C294 C295 C296

PM@

0.01U_0402_16V7K 4.7U 6.3V K X5R 0603

IFPC_PLLVDD: please add option to support both 1.8V (for G9X) and 1.05V(for GT21X)

+1.8VS L12 MBK1608121YZF_0603 N9@

+1.1VS L43 MBK1608121YZF_0603 N10@

4700P_0402_25V7K +IFPC_PLLVDD

C297 C298

PM@

4.7U 6.3V K X5R 0603

+1.1VS L15 MBK1608121YZF_0603 PM@

4700P_0402_25V7K +IFPC_IOVDD

C304 C305 C306

PM@

4.7U 6.3V K X5R 0603 470P_0402_50V7K

NEAR BGA

NEAR BALL

260mA NEAR BGA

+1.8VS L13 MBK1608121YZF_0603 N9@

+1.1VS L44 MBK1608121YZF_0603 N10@

4700P_0402_25V7K +IFPAB_PLLVDD

C299 C300

PM@

4.7U 6.3V K X5R 0603

NEAR BALL

IFPAB_PLLVDD: please add option to support both 1.8V(for G9X) and 1.05V(for GT21X)

150mA

+DACA_VDD

4700P_0402_25V7K 4.7U 6.3V K X5R 0603

L14 MBK1608121YZF_0603 PM@ +3VS

C301 C302 C303

PM@

470P_0402_50V7K

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

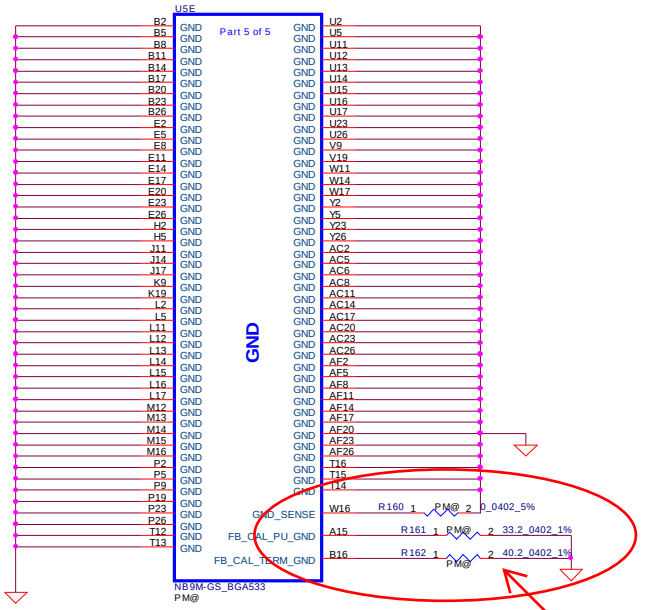
Compal Electronics, Inc.

Title: NB9M-GS Power

Size: Custom | Document Number: KIWB3/B4_LA-4551P | Rev: 0.1

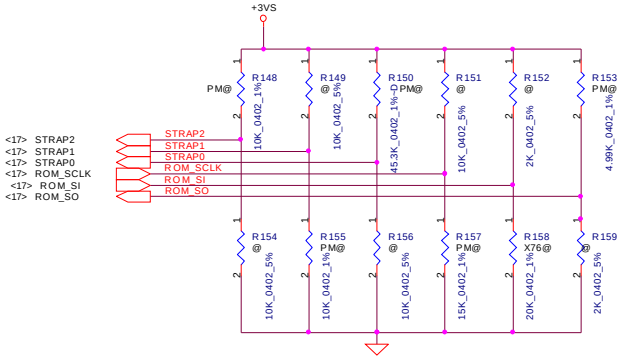
Date: Friday, June 27, 2008 | Sheet 18 of 49

A total of 8 signals are required for GB1 strapping this includes
2 reference signals
6 physical strapping pins
4 logical strapping bits
A total of 24 logical strapping bits are available



Memory/PKG	FBCAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
DDR2	30.1ohm	30.1ohm	NC
GDDR3	33.2ohm	44.2ohm	40.2ohm

To update for NV PUN-03304-001_V06 (2008/4/01)



GB1 Family GPU Strap Qptions

X76

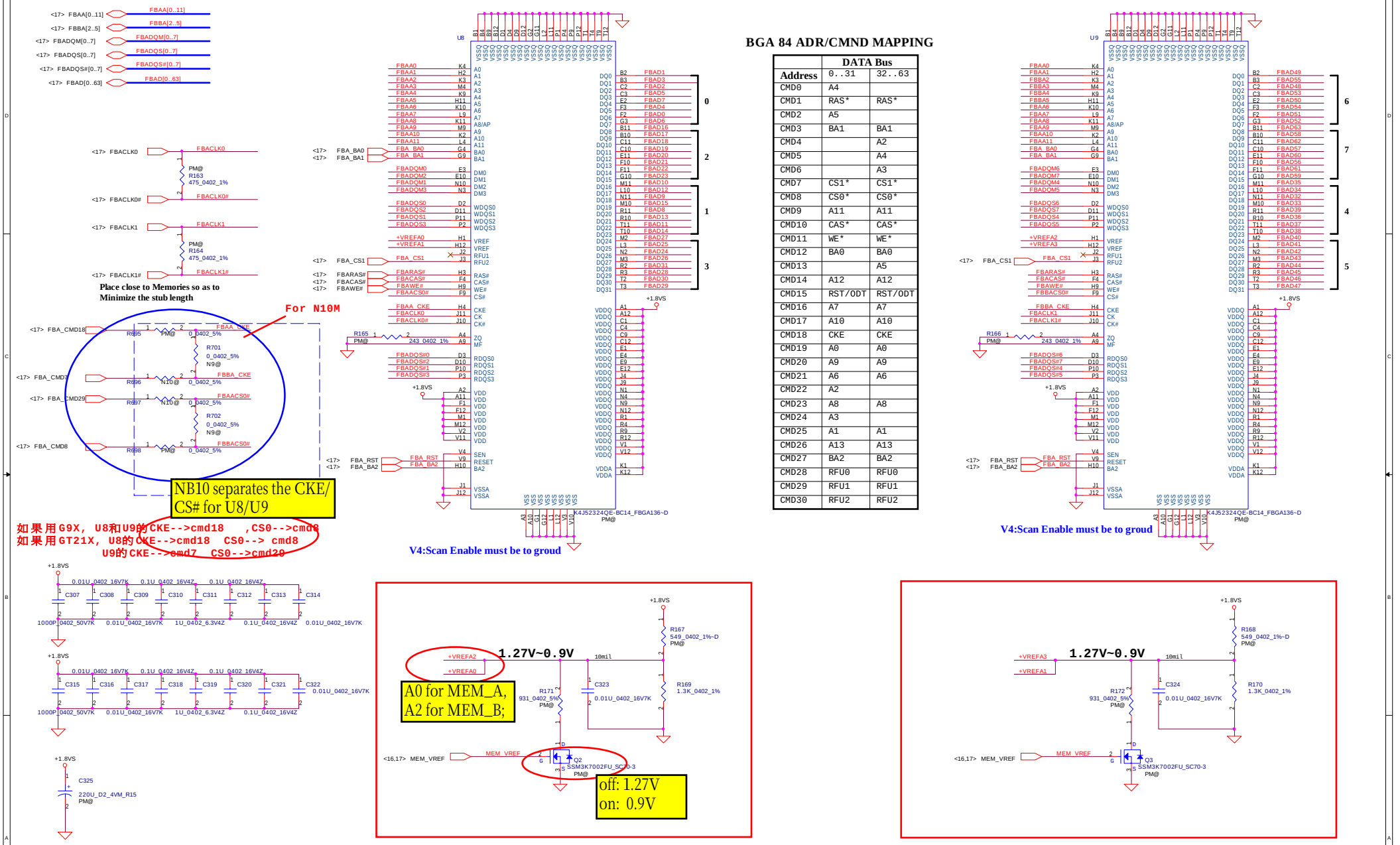
GPU	FB Memory (GDDR3)		ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
NB9M-GS (0x06E9)	Samsung	16Mx32	PU 5K	PD 15K	PD 20K	PU 10K	PD 10K	PU 45K
		32Mx32	PU 5K	PD 15K	PD 45K	PU 10K	PD 10K	PU 45K
	Hynix	16Mx32	PU 5K	PD 15K	PD 15K	PU 10K	PD 10K	PU 45K
		32Mx32	PU 5K	PD 15K	PD 35K	PU 10K	PD 10K	PU 45K
	Qimonda	16Mx32	PU 5K	PD 15K	PD 10K	PU 10K	PD 10K	PU 45K
		32Mx32	PU 5K	PD 15K	PD 30K	PU 10K	PD 10K	PU 45K

Compal Electronics, Inc.

Title: NB9M-GE GND & STRAP

Size	Document Number	Rev
B	KIWB3/B4_LA-4551P	0.1

Date: Friday, June 27, 2008 Sheet 19 of 49



BGA 84 ADR/CMND MAPPING

Address	DATA Bus 0..31	DATA Bus 32..63
CMD0	A4	
CMD1	RAS*	RAS*
CMD2	A5	
CMD3	BA1	BA1
CMD4		A2
CMD5		A4
CMD6		A3
CMD7	CS1*	CS1*
CMD8	CS0*	CS0*
CMD9	A11	A11
CMD10	CAS*	CAS*
CMD11	WE*	WE*
CMD12	BA0	BA0
CMD13		A5
CMD14	A12	A12
CMD15	RST/ODT	RST/ODT
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	CKE
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	
CMD23	A8	A8
CMD24	A3	
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28	RFU0	RFU0
CMD29	RFU1	RFU1
CMD30	RFU2	RFU2

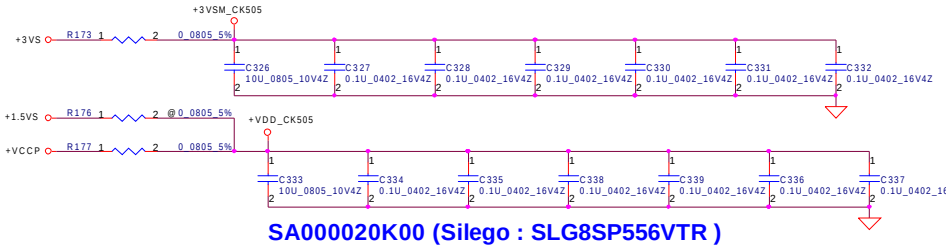
Compal Electronics, Inc.

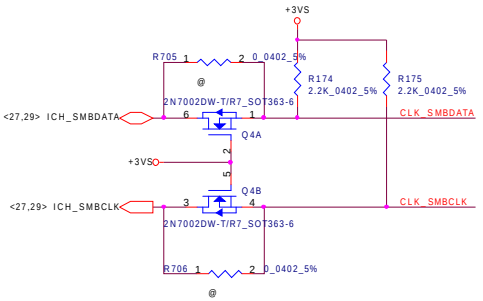
Title: VRAM DDRA

Size: Custom | Document Number: KIWB3/B4_LA-4551P | Rev: 0.1

Date: Friday, June 27, 2008 | Sheet 20 of 49

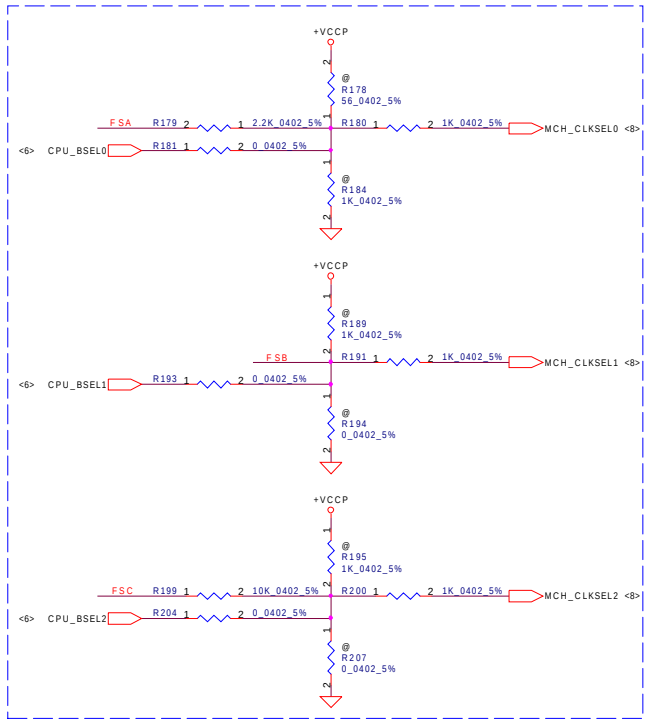
FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					

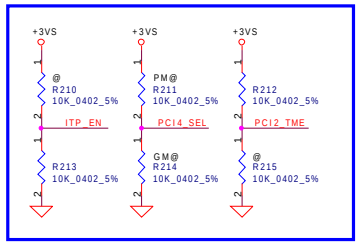


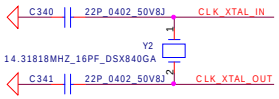


SA000020K00 (Silego : SLG8SP556VTR)

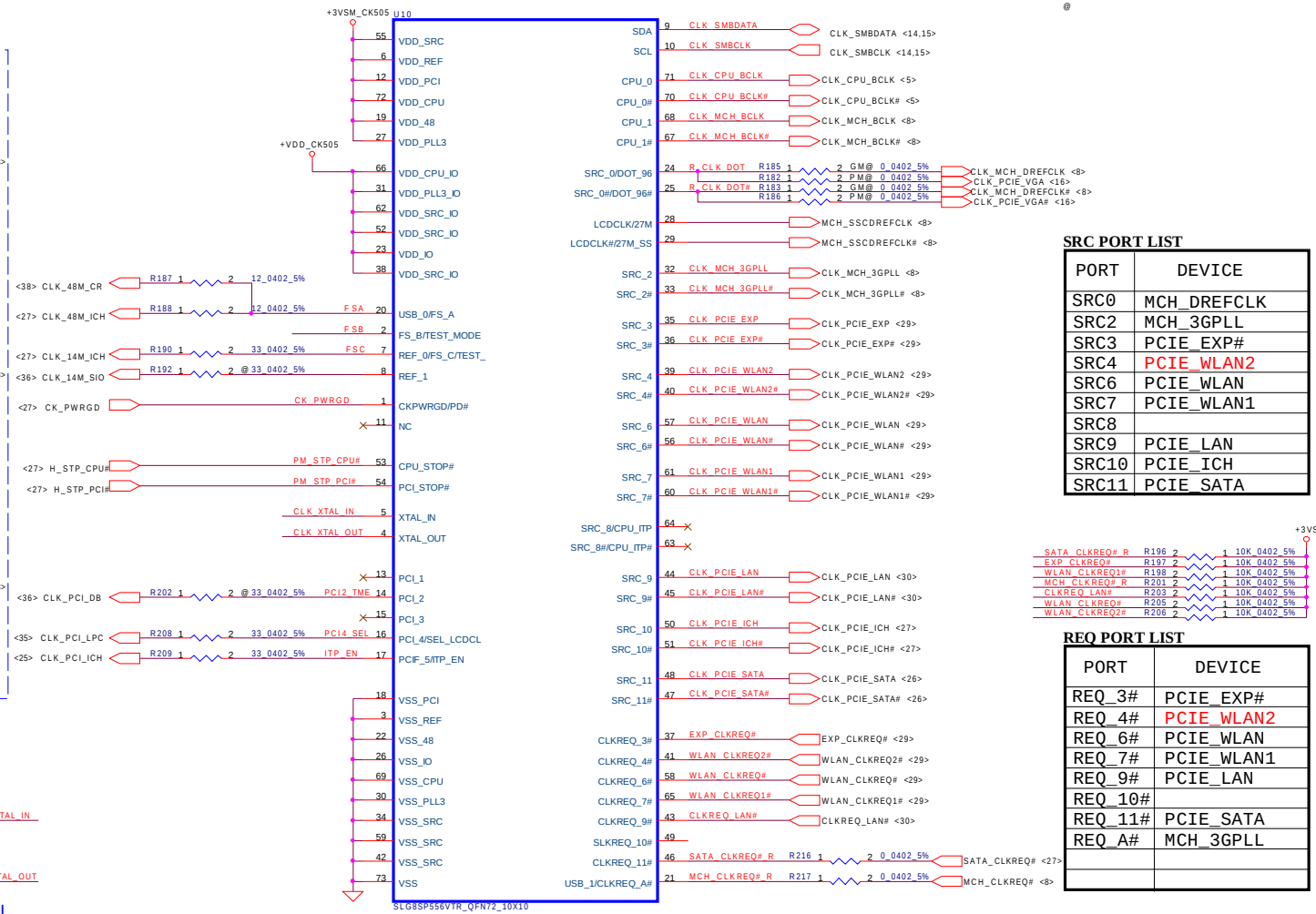
SA000020H00 (ICS : ICS9LPRS387AKLFT)







Routing the trace at least 10mil



SRC PORT LIST

PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	MCH_3GPLL
SRC3	PCIE_EXP#
SRC4	PCIE_WLAN2
SRC6	PCIE_WLAN
SRC7	PCIE_WLAN1
SRC8	
SRC9	PCIE_LAN
SRC10	PCIE_ICH
SRC11	PCIE_SATA

REQ PORT LIST

PORT	DEVICE
REQ_3#	PCIE_EXP#
REQ_4#	PCIE_WLAN2
REQ_6#	PCIE_WLAN
REQ_7#	PCIE_WLAN1
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	PCIE_SATA
REQ_A#	MCH_3GPLL

For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#

For PCI4_SEL, 0 = Pin24/25 : DOT96 / DOT96#
Pin28/29 : LCDCLK / LCDCLK#
1 = Pin24/25 : SRC_0 / SRC_0#
Pin28/29 : 27M/27M_SS

Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

Compal Electronics,Ltd.

Title: **Clock Generator CK505**

Size: Custom | Document Number: **KIWB3/B4_LA4551P** | Rev: 0.1

Date: Friday, June 27, 2008 | Sheet 21 of 49

P/N:SA00002D700 (8101T)
P/N:SA00001U920 (CH7318C)

U11

GM@ PS8101TQFN48G_QFN48_7X7

Reserved for CH7318C

1.2k for CH7318C

TMDS pull down (500ohm) resistors G9x only

NEAR CONNECTOR

place those component near JP4

for NV request 0515

9/14 Modify for UMA used

9/14 Reserve for VGA used;check pin name

JHDMI1

TYCO_1775040-6

ME@

Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

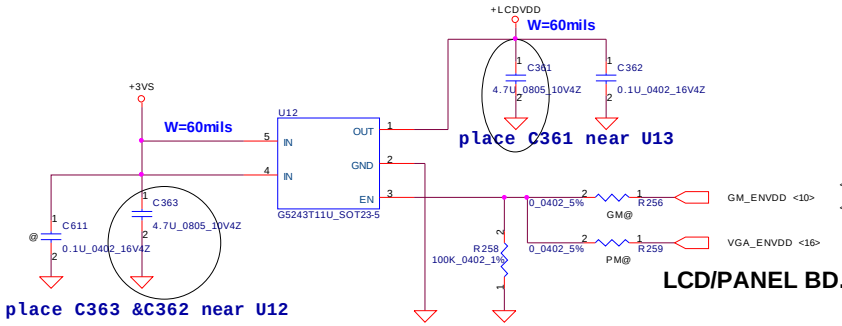
Compal Electronics,Ltd.

Title: Level Shiftter_PS8101T

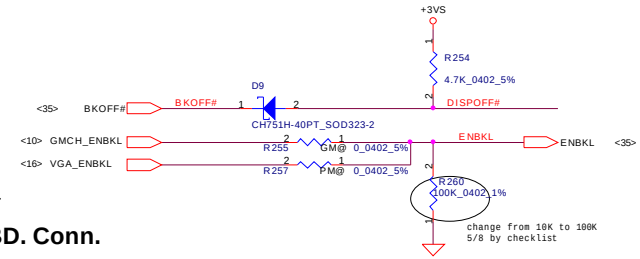
Size: Custom | Document Number: KIWB3/B4_LA4551P | Rev: 0.1

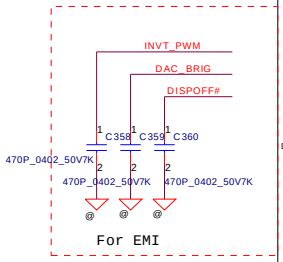
Date: Friday, June 27, 2008 | Sheet 22 of 49

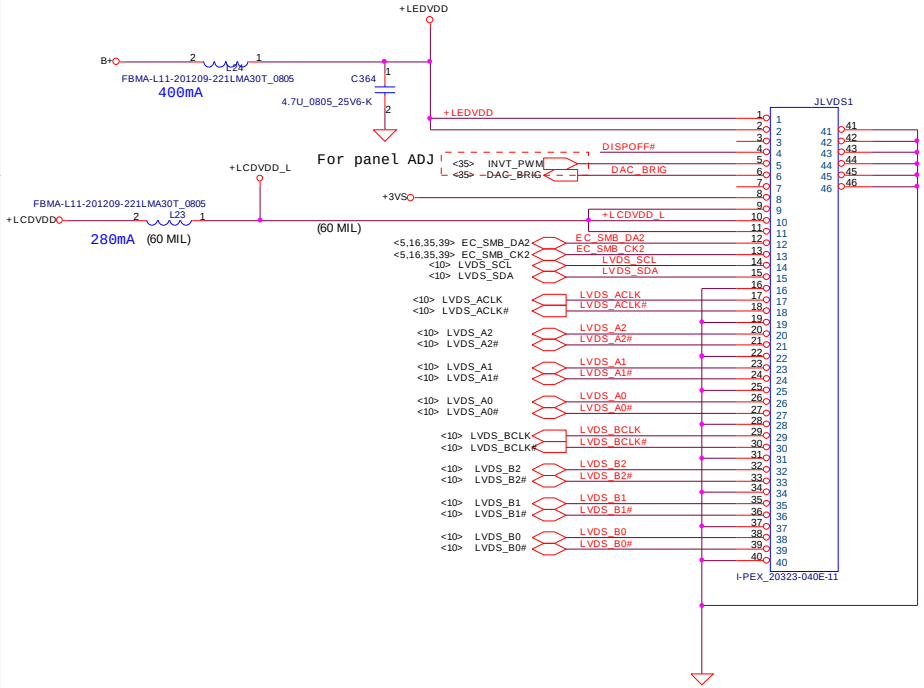
LCD POWER CIRCUIT



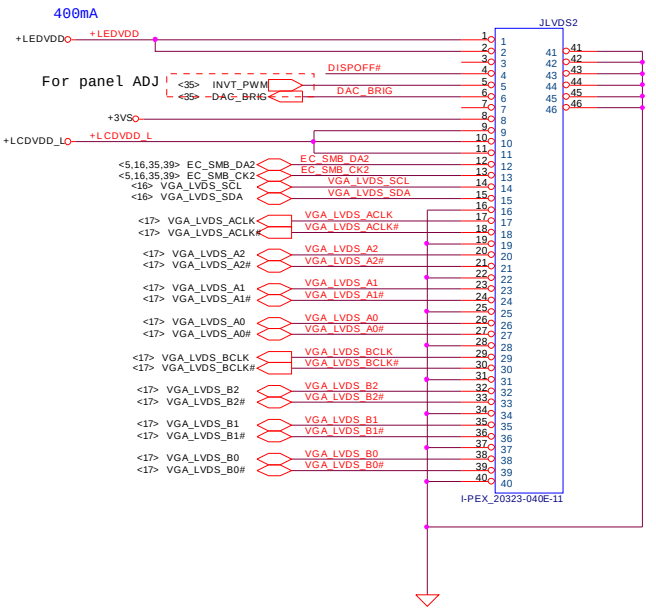
LCD/PANEL BD. Conn.







LCD/PANEL BD. Conn.



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

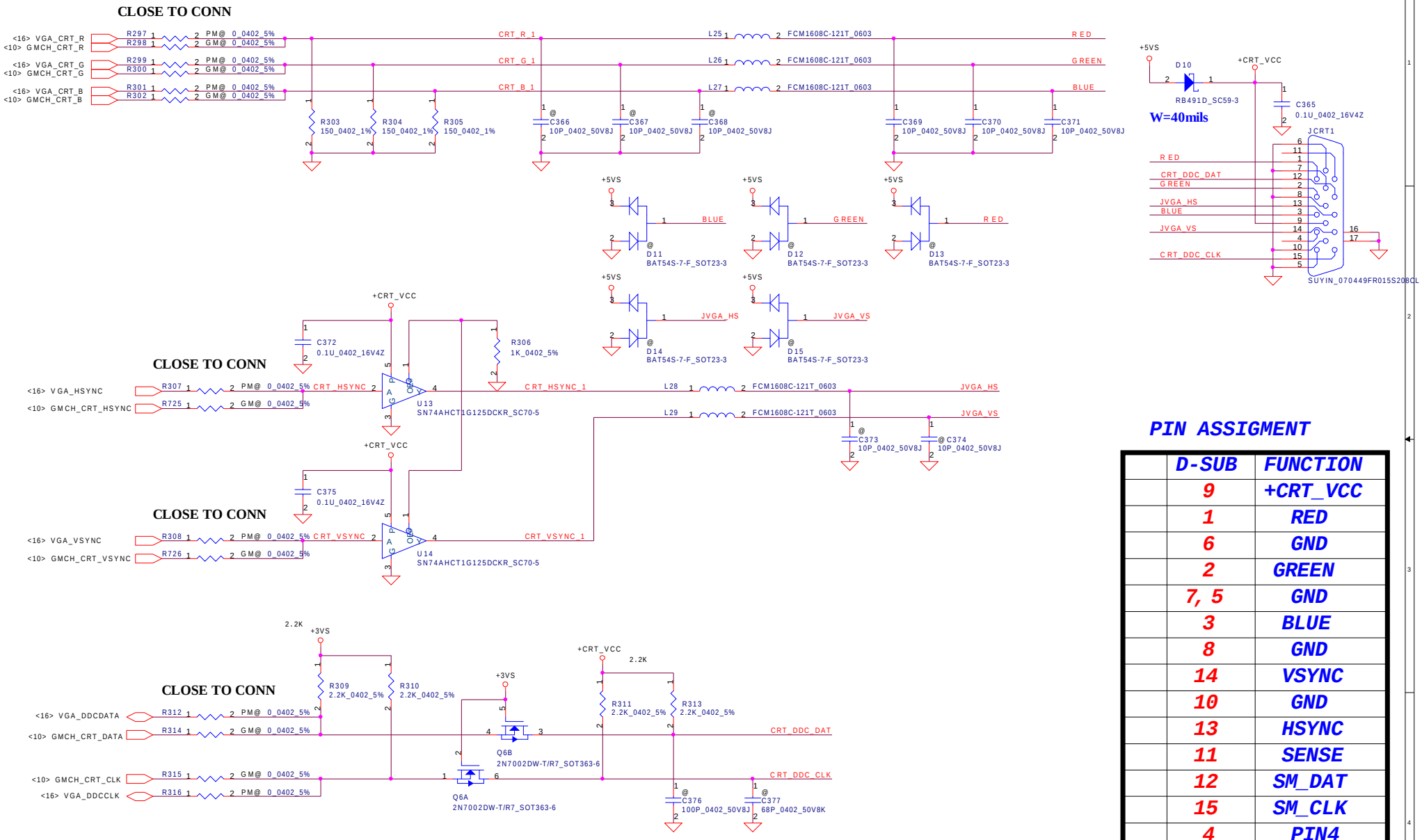
Compal Electronics, Inc.

Title: **LVDS & DVI Connector**

Size	Document Number	Rev
B	JITR1_LA-4141P	0.1

Date: Friday, June 27, 2008 Sheet 23 of 49

CRT Connector



PIN ASSIGMENT

	D-SUB	FUNCTION
	9	+CRT_VCC
	1	RED
	6	GND
	2	GREEN
	7, 5	GND
	3	BLUE
	8	GND
	14	VSYNC
	10	GND
	13	HSYNC
	11	SENSE
	12	SM_DAT
	15	SM_CLK
	4	PIN4

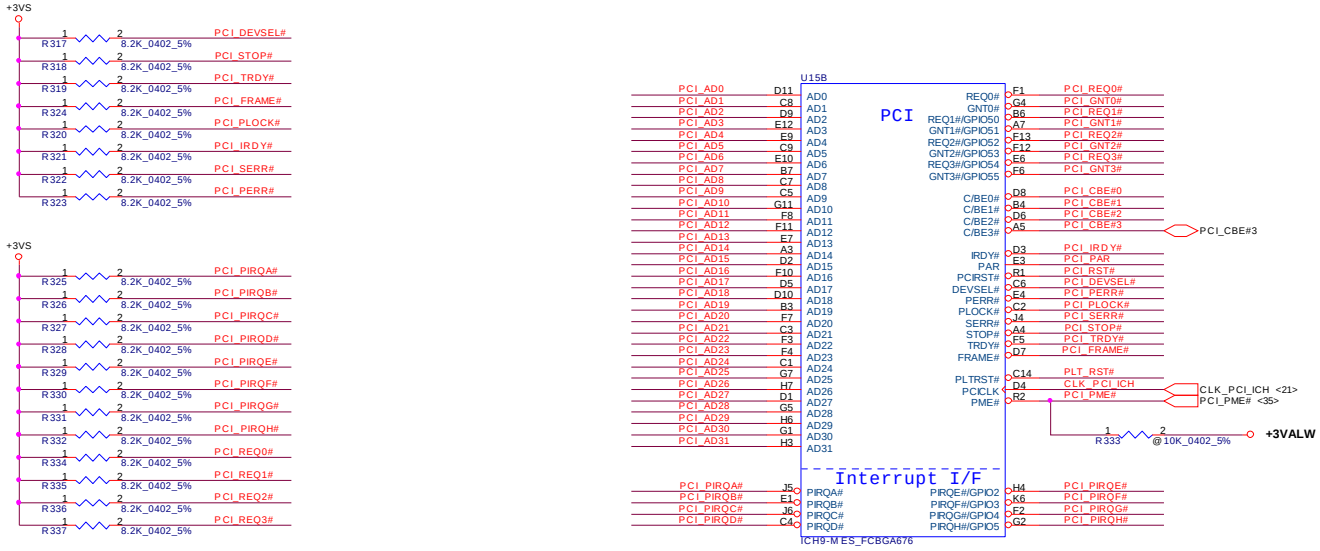
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: CRT & TV-OUT Connector

Size	Document Number	Rev
Custom	JITR1_LA-4141P	0.1

Date: Friday, June 27, 2008 Sheet 24 of 49



A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction
0	1	SPI
1	0	PCI
1	1	LPC*

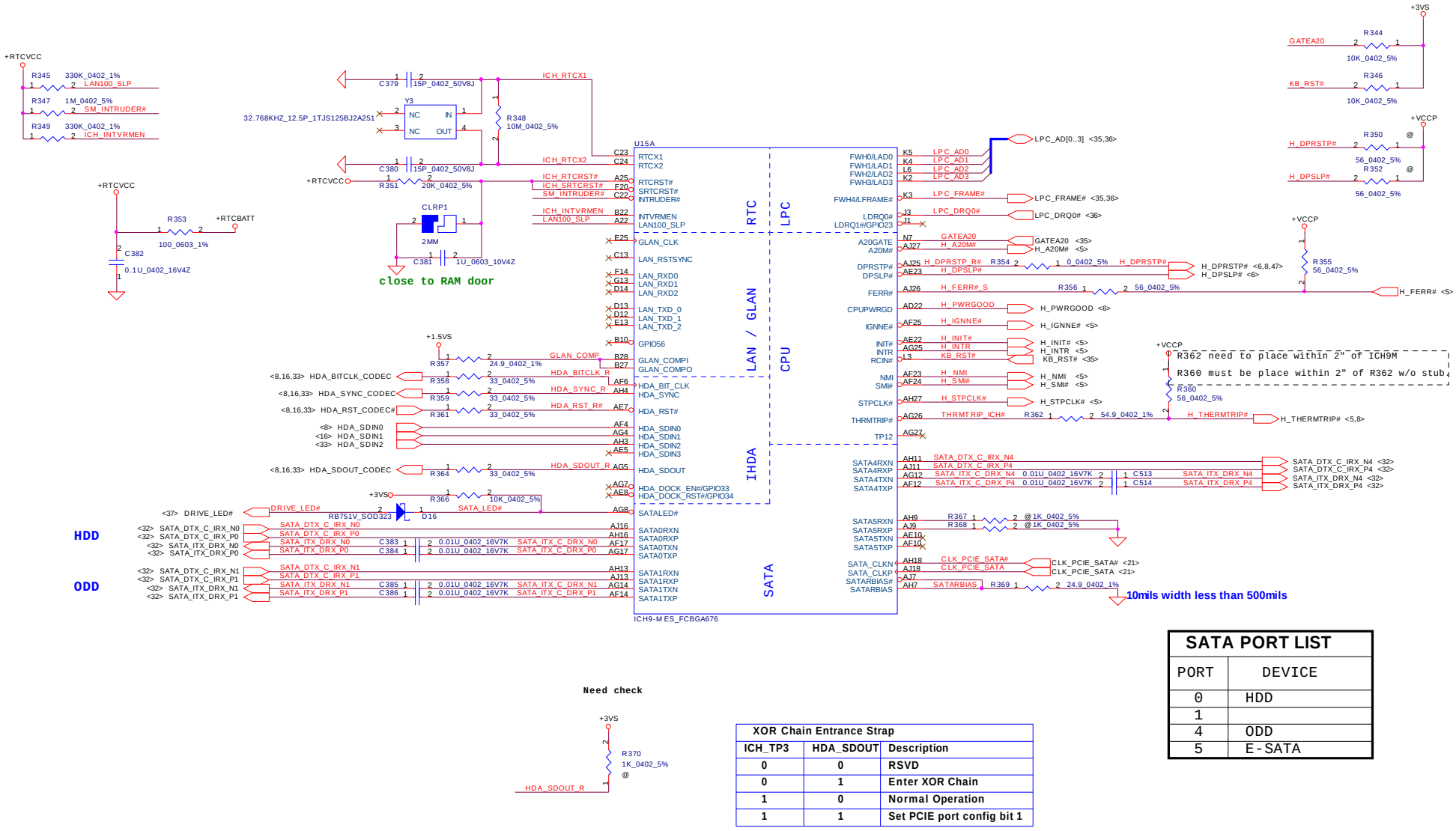
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: ICH9M(1/4)-PCI

Size	Document Number	Rev
	JITR1_LA-4141P	0.1

Date: Friday, June 27, 2008 Sheet 25 of 49



SATA PORT LIST	
PORT	DEVICE
0	HDD
1	
4	ODD
5	E-SATA

XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1

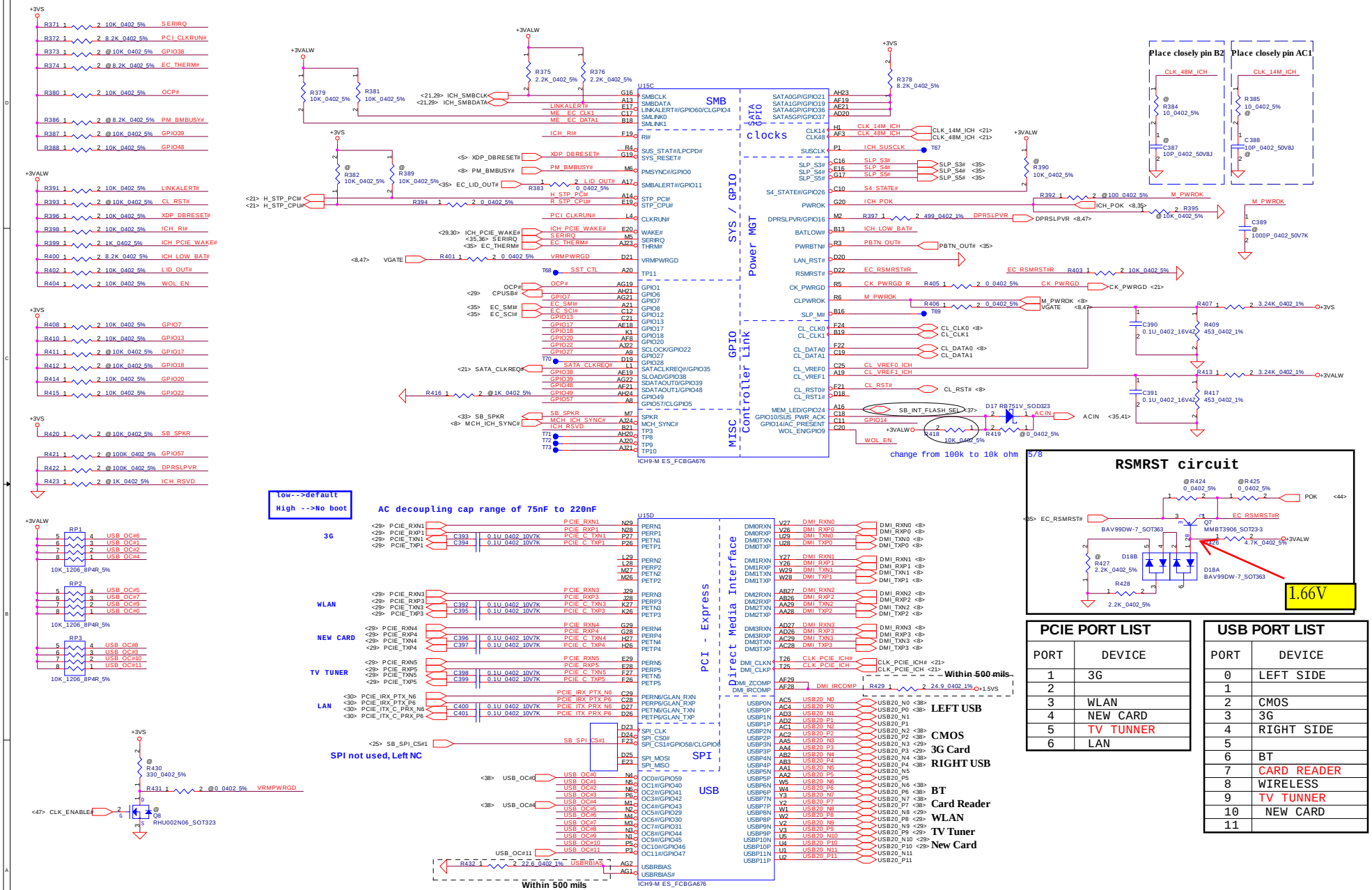
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: ICH9M(2/4)-LAN,IDELPC,RTC

Size	Document Number	Rev
Custom	JITR1_LA-4141P	0.1

Date: Friday, June 27, 2008 Sheet 26 of 49



PCIE PORT LIST	
PORT	DEVICE
1	3G
2	
3	WLAN
4	NEW CARD
5	TV TUNNER
6	LAN

USB PORT LIST	
PORT	DEVICE
0	LEFT SIDE
1	
2	CMOS
3	3G
4	RIGHT SIDE
5	
6	BT
7	CARD READER
8	WIRELESS
9	TV TUNNER
10	NEW CARD
11	

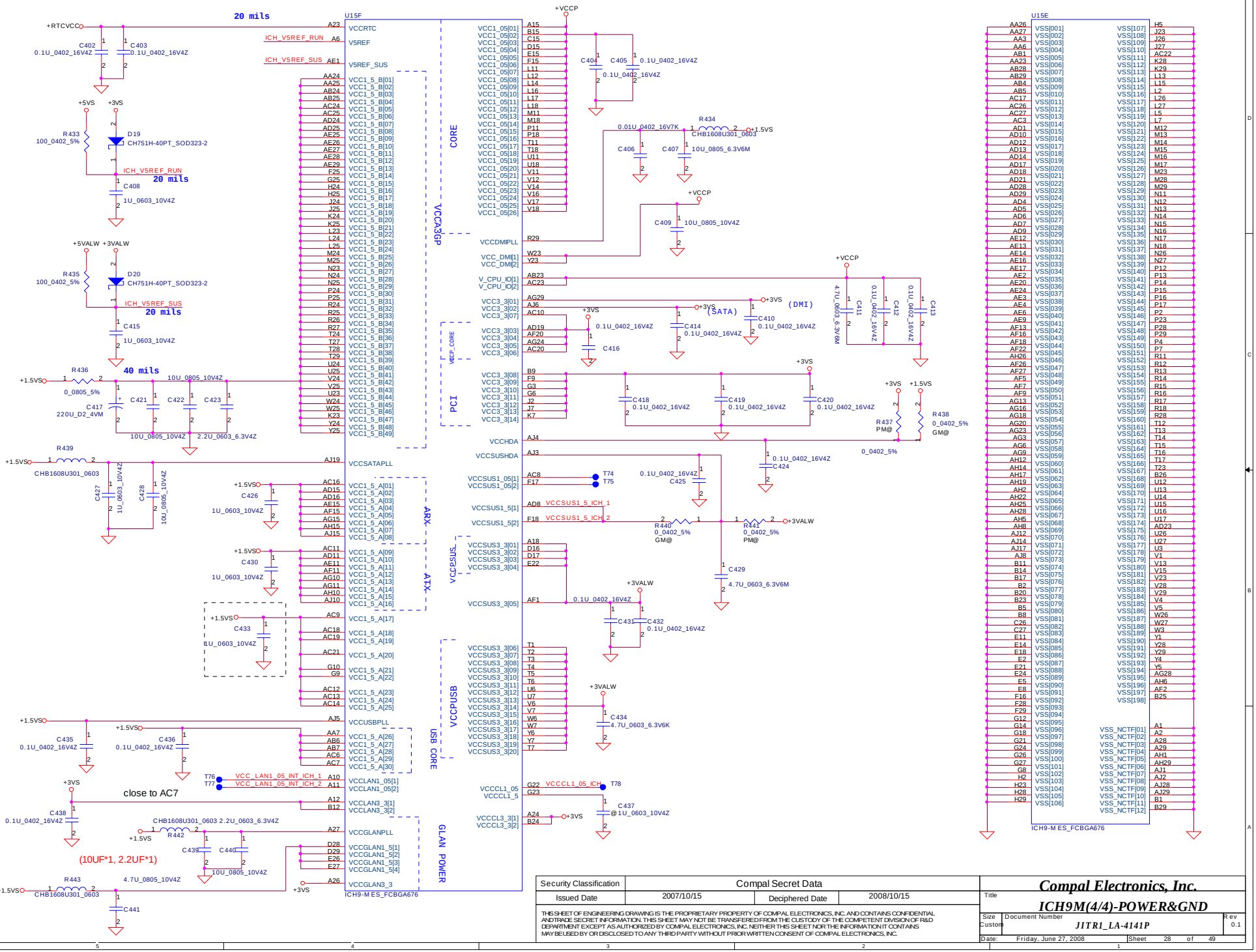
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **ICH9M(3/4)-USB,GPIO,PCIE**

Size	Document Number	Rev
C	JITR1_LA-4141P	0.1

Date: Friday, June 27, 2008 | Sheet 27 of 49



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

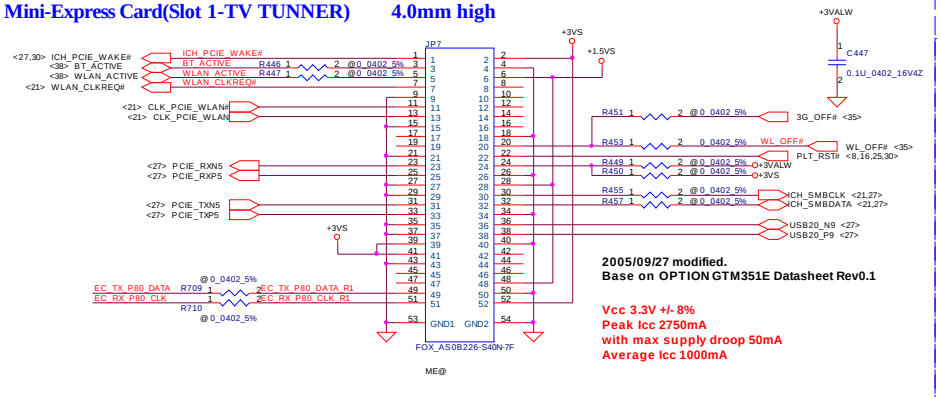
Title: ICH9M(4/4)-POWER&GND

Size	Document Number	Rev
Custom	JITR1_LA-4141P	0.1

Date: Friday, June 27, 2008 | Sheet 28 of 49

Mini-Express Card for 3G Or TV Tuner
Mini-Express Card for WLAN

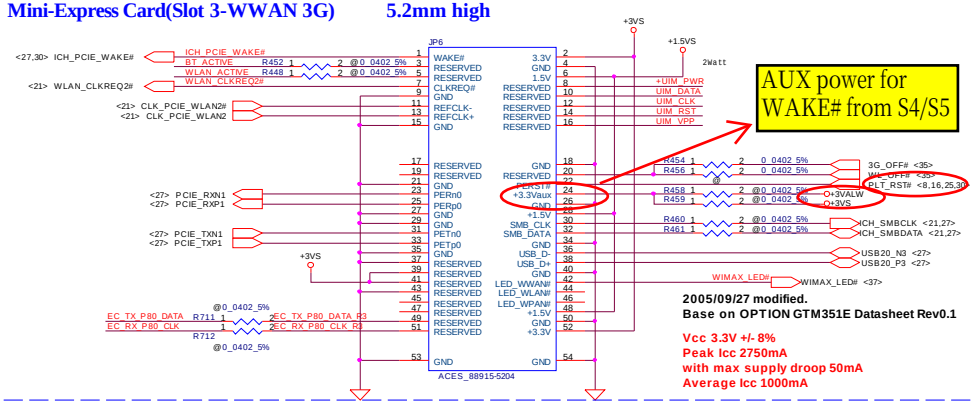
Mini-Express Card(Slot 1-TV TUNNER) 4.0mm high



2005/09/27 modified.
Base on OPTION GTM351E Datasheet Rev0.1

Vcc 3.3V +/- 8%
Peak Icc 2750mA
with max supply droop 50mA
Average Icc 1000mA

Mini-Express Card(Slot 3-WWAN 3G) 5.2mm high

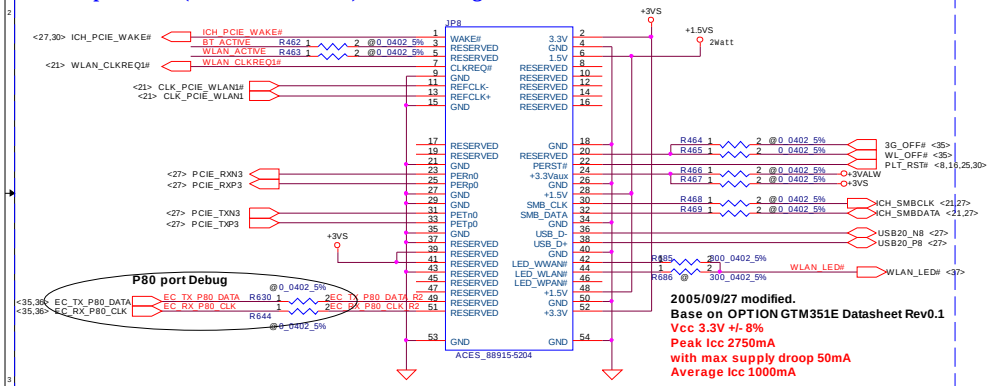


AUX power for WAKE# from S4/S5

2005/09/27 modified.
Base on OPTION GTM351E Datasheet Rev0.1

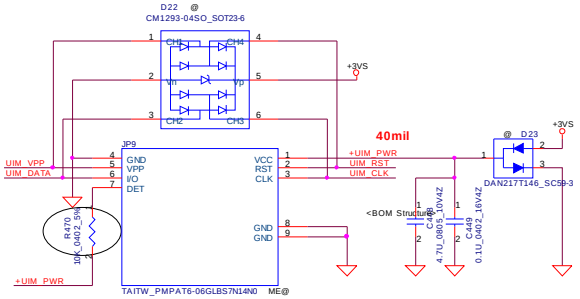
Vcc 3.3V +/- 8%
Peak Icc 2750mA
with max supply droop 50mA
Average Icc 1000mA

Mini-Express Card(Slot 2-WIRELESS) 5.2mm high

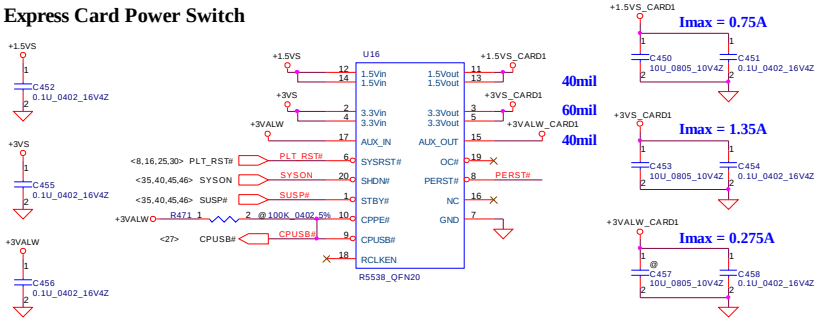


2005/09/27 modified.
Base on OPTION GTM351E Datasheet Rev0.1

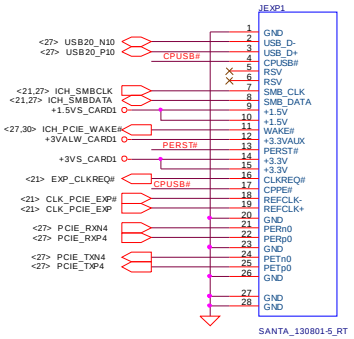
Vcc 3.3V +/- 8%
Peak Icc 2750mA
with max supply droop 50mA
Average Icc 1000mA



Express Card Power Switch



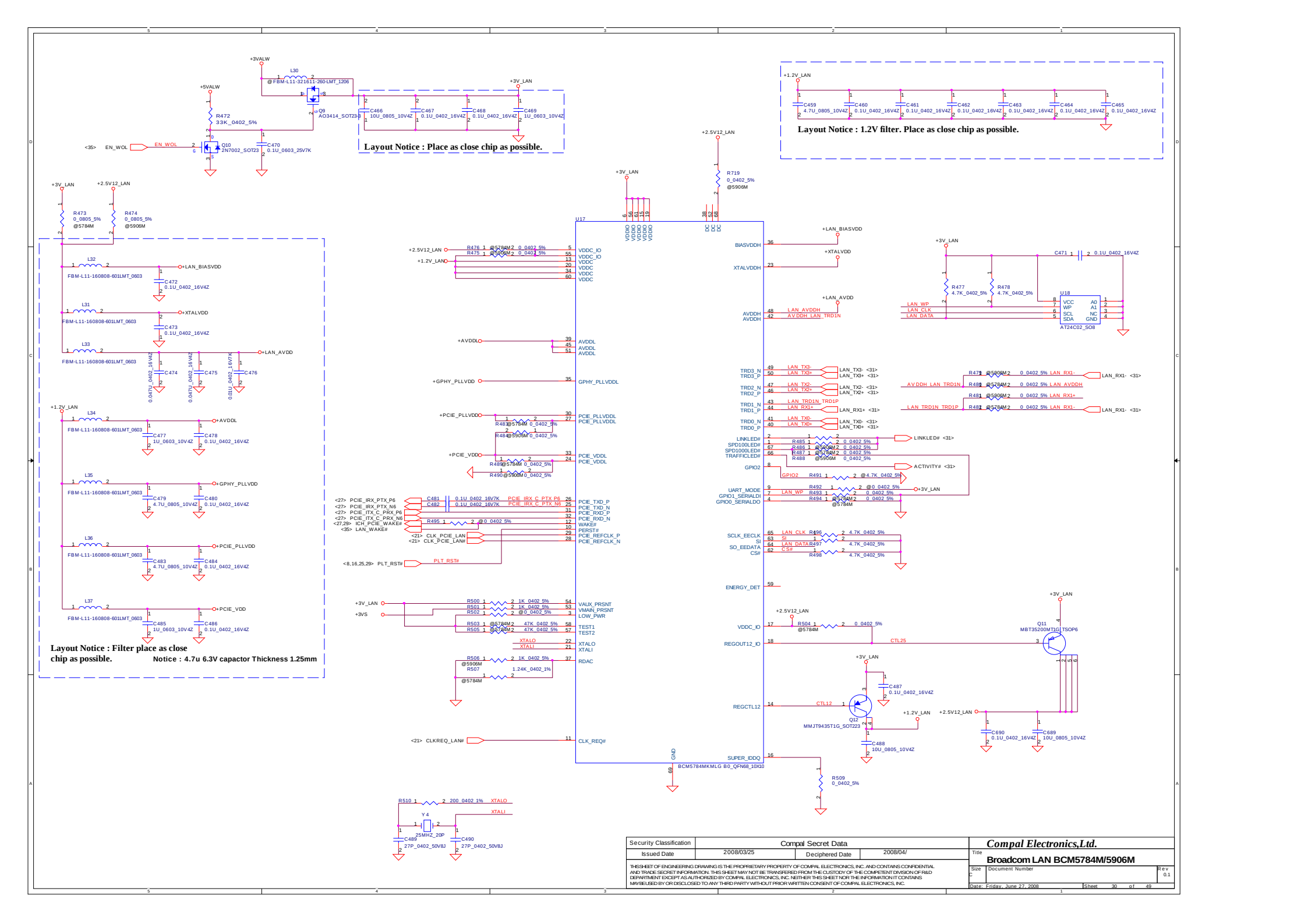
New Card 34mm Socket (Left/TOP)



(NEW)

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.	
Title	Mini-Card/3G/FeliCa/BT
Size	Document Number: JITR1_LA-4141P
Rev	0.1
Date: Friday, June 27, 2008	Sheet 29 of 49



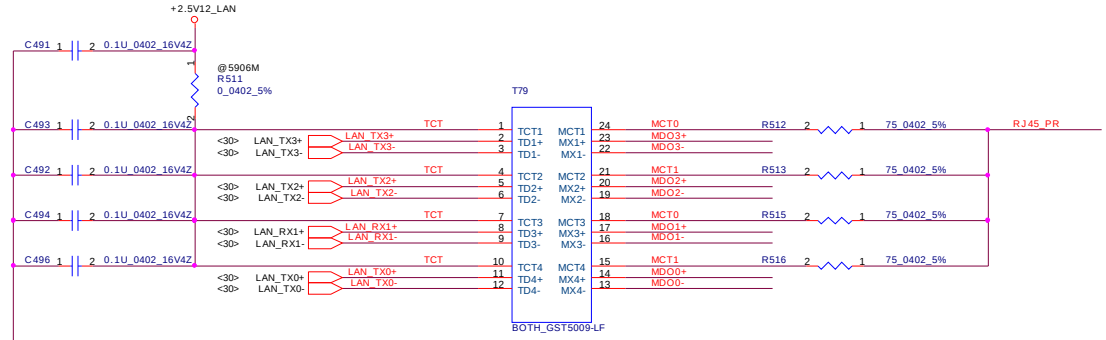
Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

Compal Electronics,Ltd.

Title: **Broadcom LAN BCM5784M/5906M**

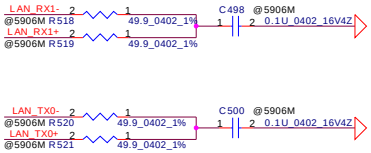
Size	Document Number	Rev
C		0.1

Date: Friday, June 27, 2008 Sheet 30 of 49

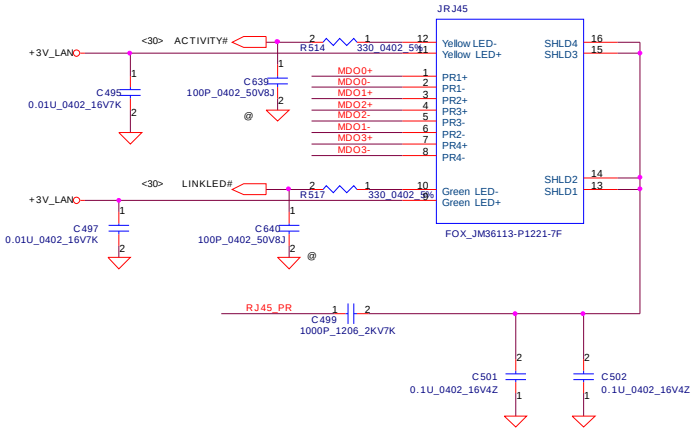


Change C468,C470,C473,C474,C475,C476 from 0.01uF to 0.1uF

near LAN controller



RJ45 CONN



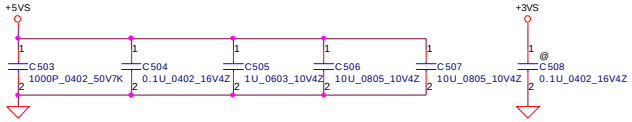
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

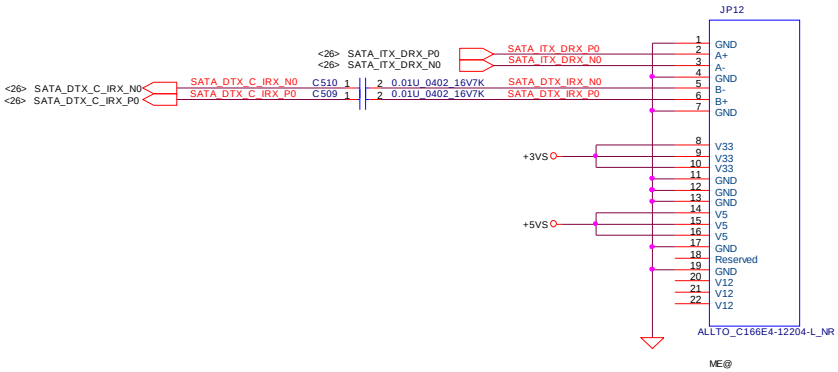
Title: **LAN CONTROLLER**

Size	Document Number	Rev
Custom	JITR1_LA-4141P	0.1

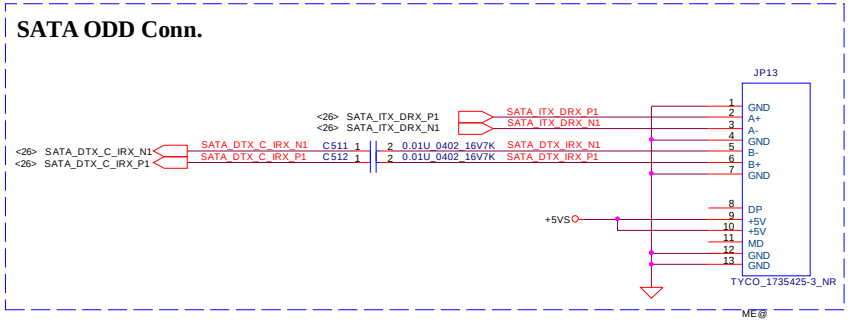
Date: Friday, June 27, 2008 Sheet 31 of 49



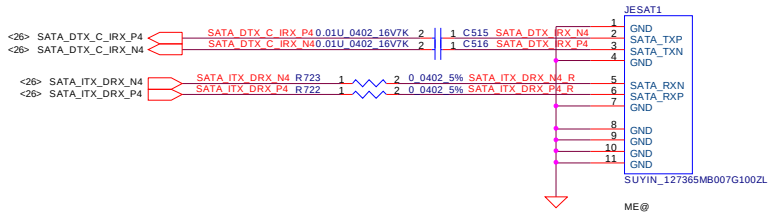
SATA HDD Conn.



SATA ODD Conn.



E-SATA Conn.
place R722&R723&C515&C516
near JESAT1

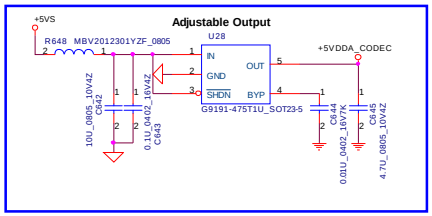


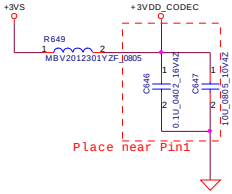
Compal Electronics, Inc.

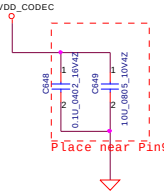
Title: **HDD & ODD Connector**

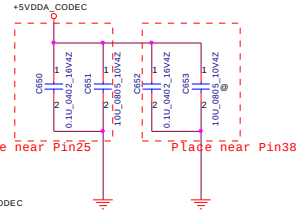
Size	Document Number	Rev
B	JITR1_LA-4141P	0.1

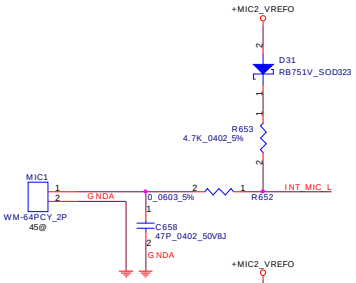
Date: Friday, June 27, 2008 | Sheet 32 of 49

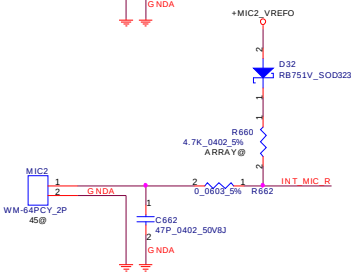




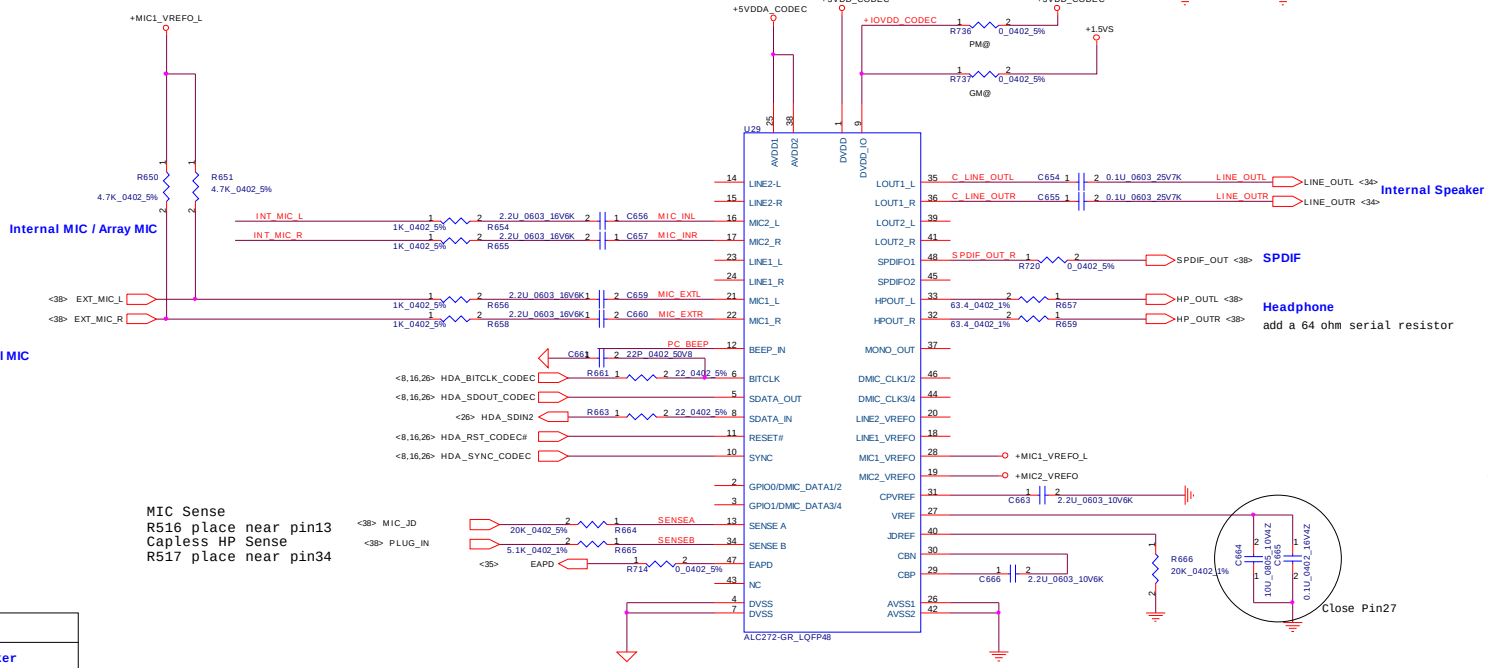




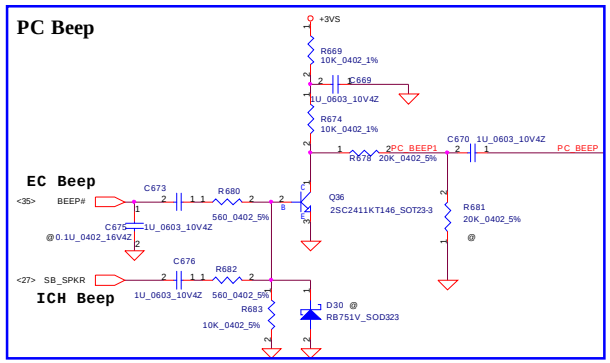


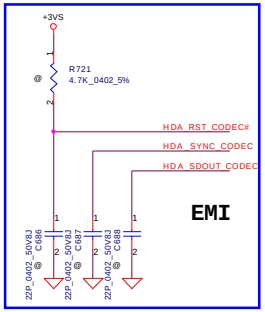


external MIC



Pin Assignment	Location	Function
LINE-OUT (Pin35/36)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
LINE1 (Pin23/24)	External	Line in
MIC1(Pin21/22)	External	Mic in
MONO-OUT(Pin37)	Internal	Internal Subwoofer
MIC2(Pin16/17)	Internal	Internal Mic





Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

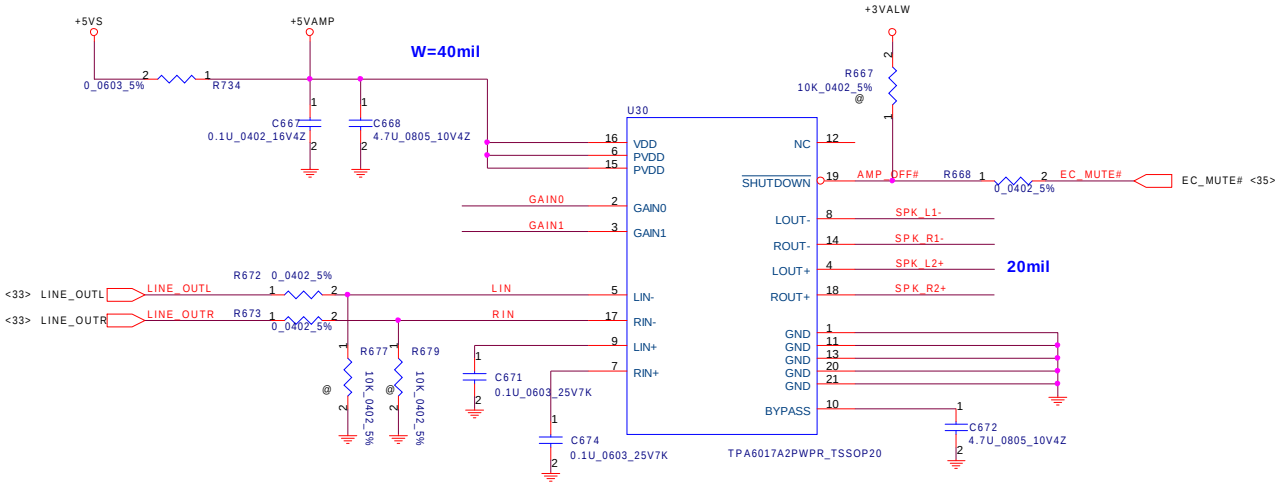
Compal Electronics,Ltd.

Title: HD Audio Codec_ALC272

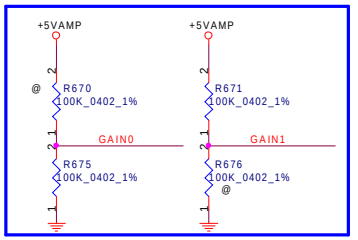
Size: C | Document Number: KIWB3/B4_LA4551P | Rev: 0.1

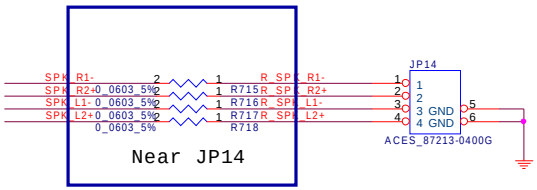
Date: Friday, June 27, 2008 | Sheet 33 of 49

Speaker Connector



GAIN0	GAIN1	
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB





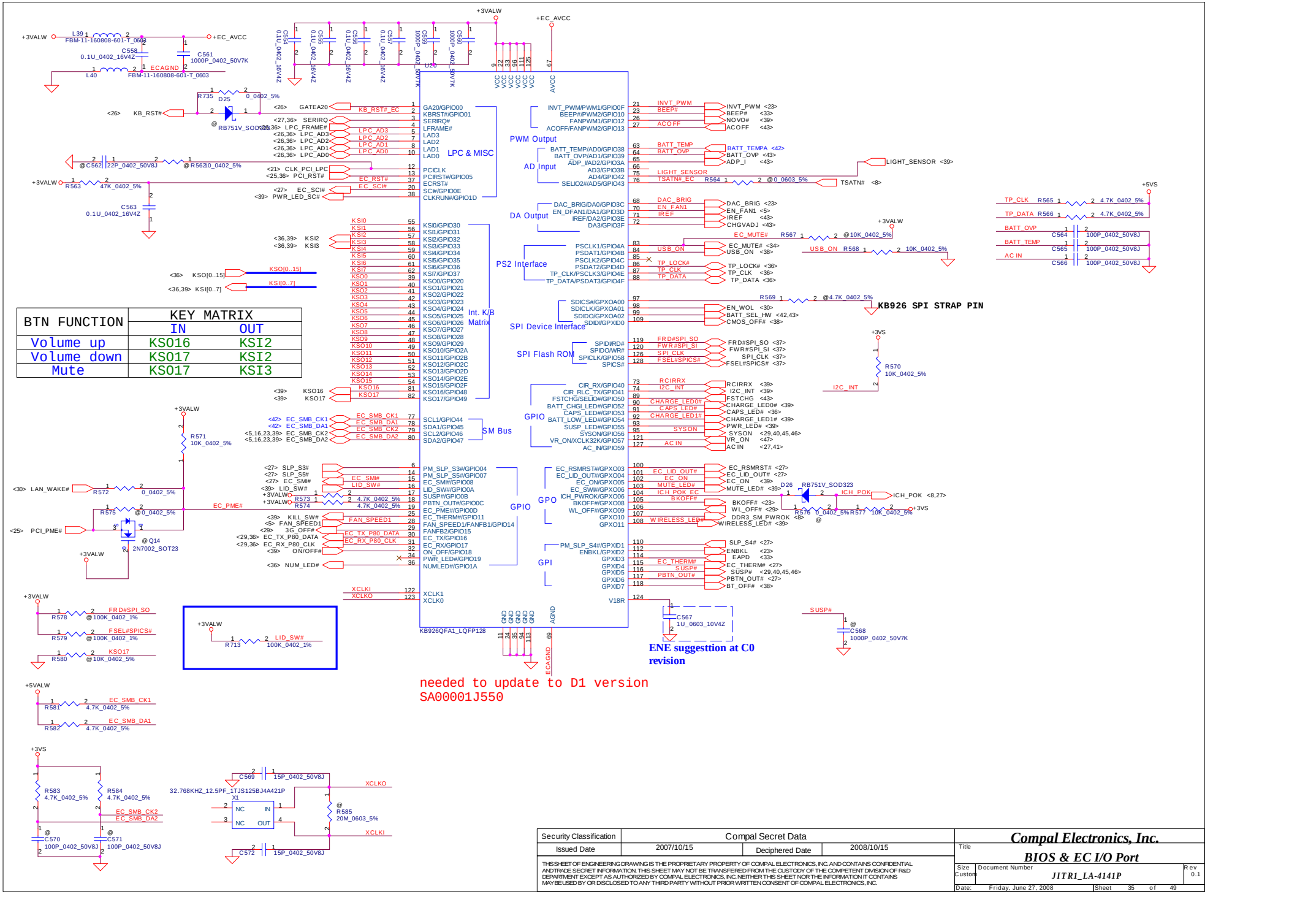
Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

Compal Electronics,Ltd.

Title: AMP,Audio speaker CONN

Size: Custom | Document Number: KIWB3/B4_LA4551P | Rev: 0.1

Date: Friday, June 27, 2008 | Sheet 34 of 49



BTN FUNCTION	KEY MATRIX	
	IN	OUT
Volume up	KSO16	KSI2
Volume down	KSO17	KSI2
Mute	KSO17	KSI3

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

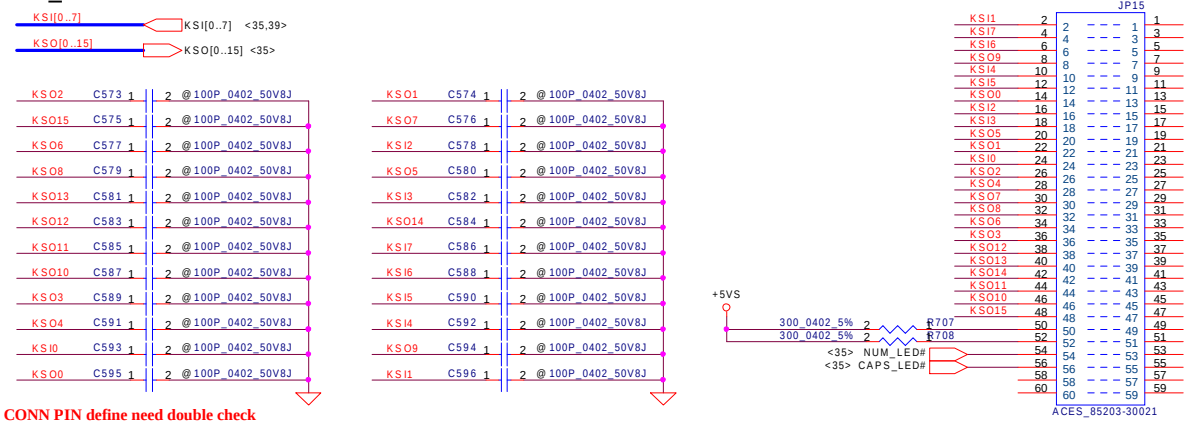
Title: **BIOS & EC I/O Port**

Size	Document Number	Rev
Custom	JITR1_LA-4141P	0.1

Date: Friday, June 27, 2008 Sheet 35 of 49

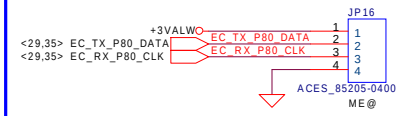
INT_KBD Conn.

Source:SP01000IE00
2nd source:SP01000IF00
30 pin

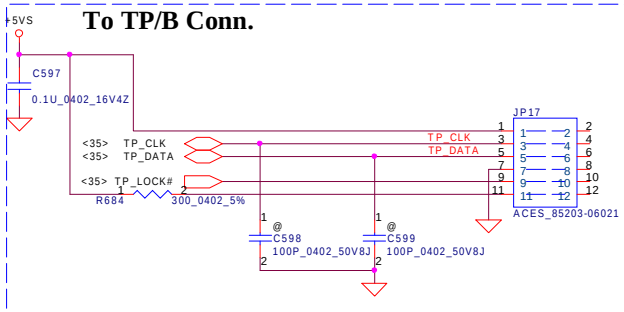


CONN PIN define need double check

EC DEBUG PORT

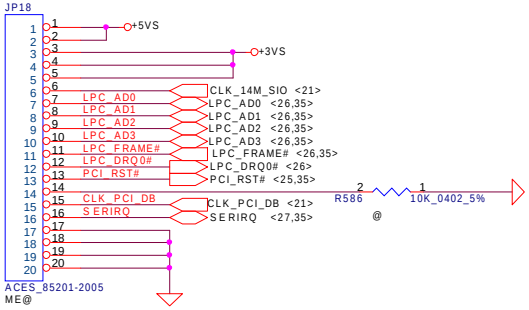


To TP/B Conn.



CONN PIN define need double check

FOR LPC SIO DEBUG PORT



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

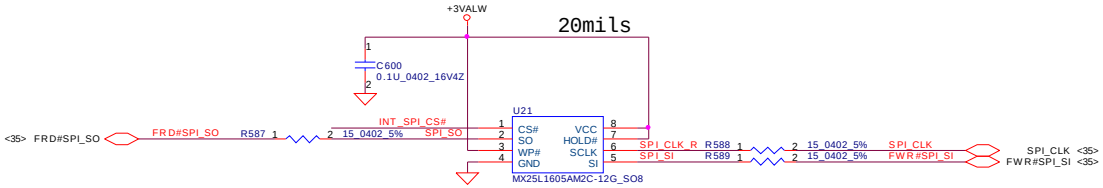
Compal Electronics, Inc.

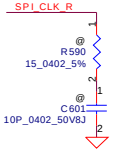
Title: **KB /SW /LPC Debug Conn.**

Size	Document Number	Rev
B	JITR1_LA-4141P	0.1

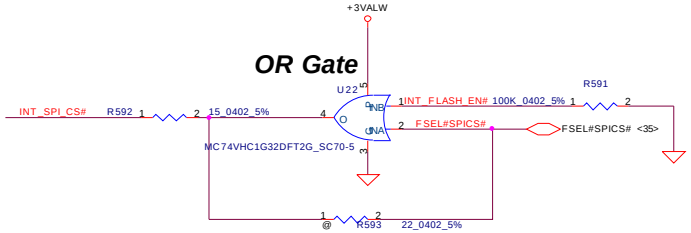
Date: Friday, June 27, 2008 Sheet 36 of 49

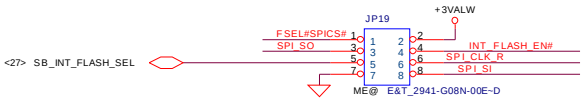
FOR EC 16M SPI ROM

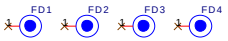


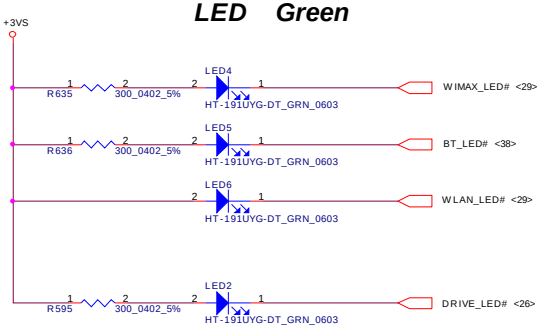


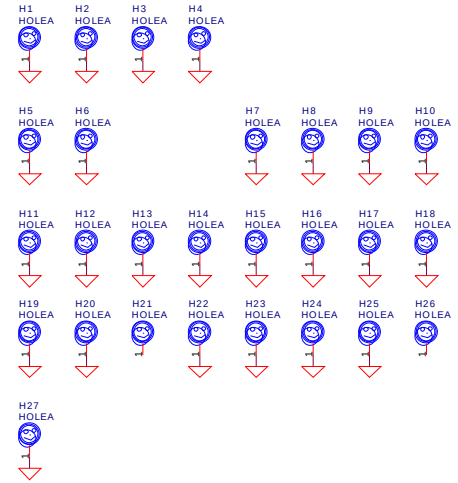
INPUT		OUTPUT
A	B	Y
L	L	L
H	L	H
L	H	H
H	H	H





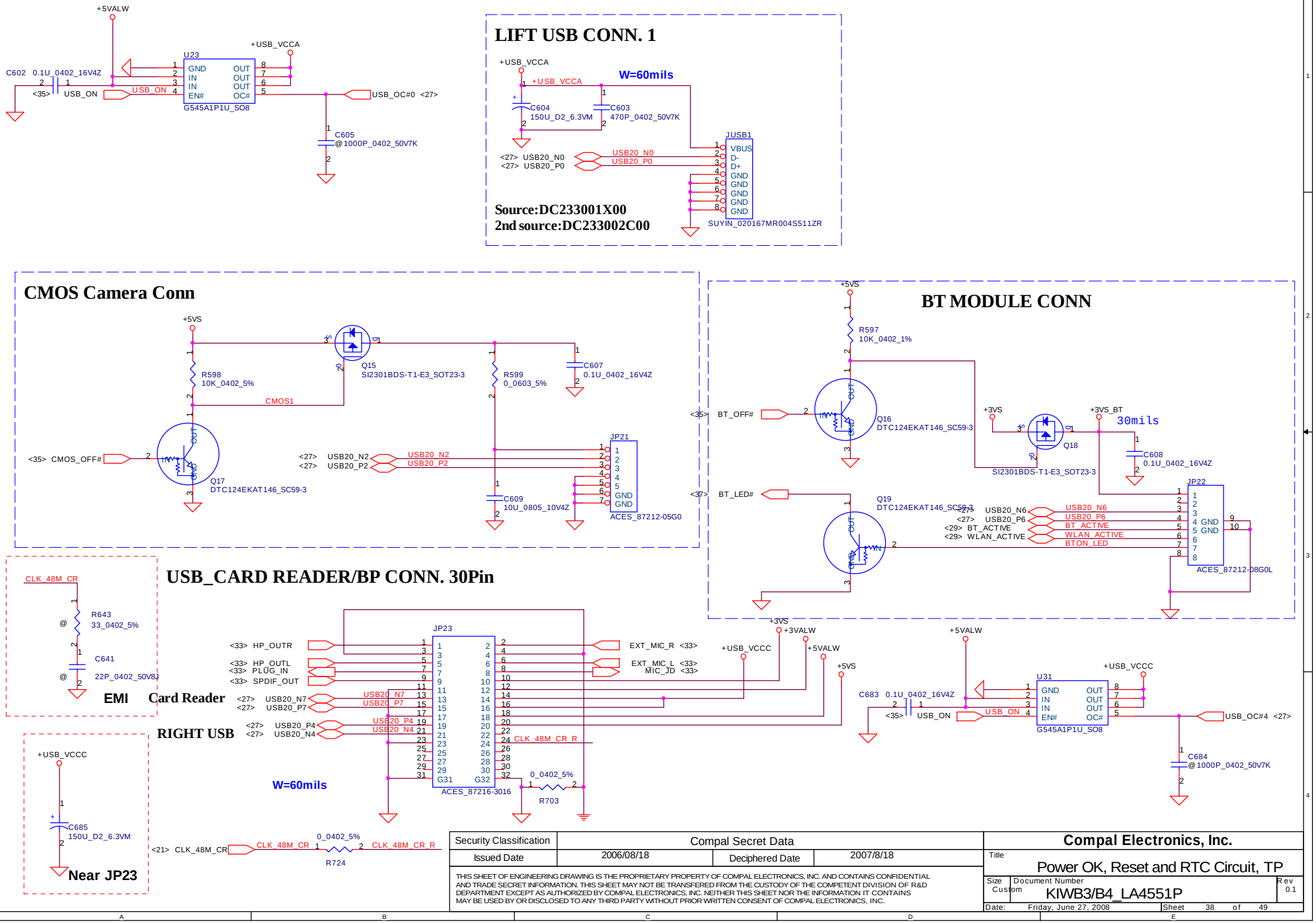






Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title	LED/EC SPI ROM		
Size B	Document Number JITR1_LA-4141P		Rev 0.1
Date: Friday, June 27, 2008	Sheet 37 of 49		



Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

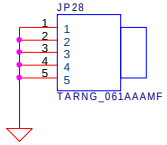
Compal Electronics, Inc.

Title: Power OK, Reset and RTC Circuit, TP

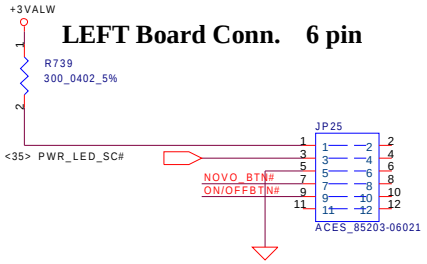
Size	Document Number	Rev
Custom	KIWB3/B4_LA4551P	0.1

Date: Friday, June 27, 2008 Sheet 38 of 49

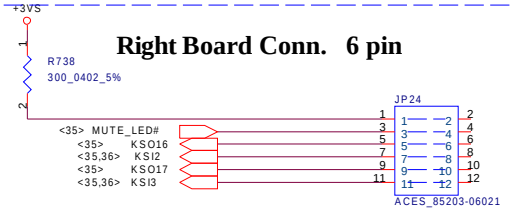
TV ANTENNA



LEFT Board Conn. 6 pin



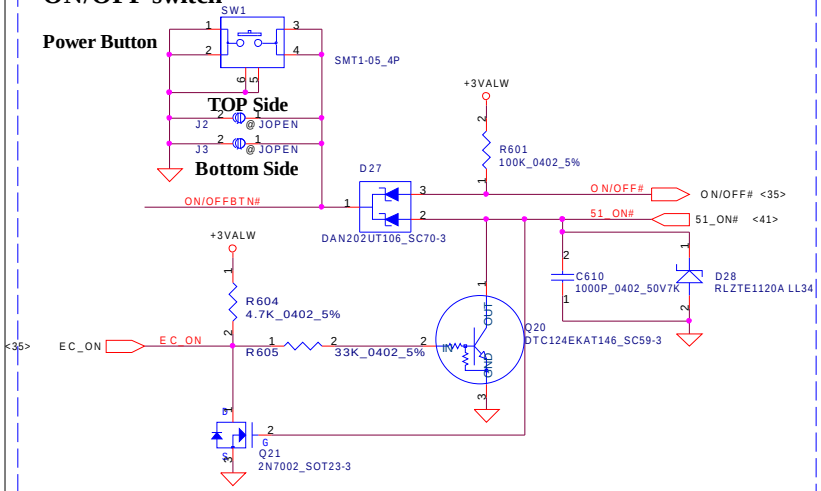
Right Board Conn. 6 pin

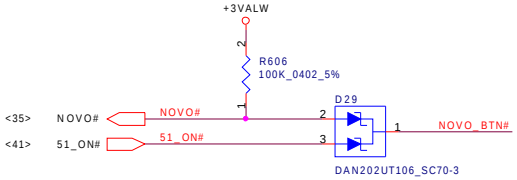


BTN FUNCTION	KEY MATRIX	
	IN	OUT
UP	KSO16	KSI2
DOWN	KSO17	KSI2
MUTE	KSO17	KSI3

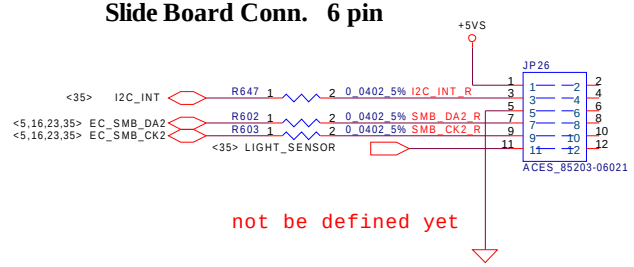
ON/OFF switch

Power Button



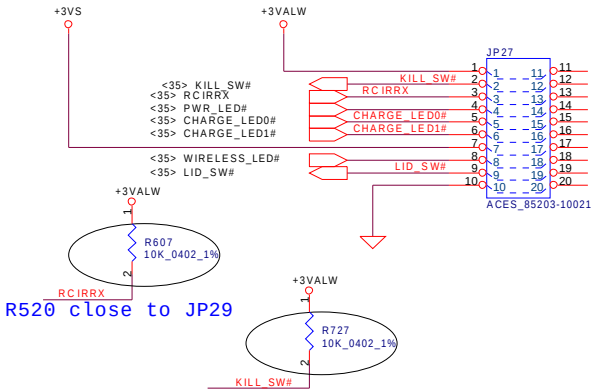


Slide Board Conn. 6 pin



not be defined yet

CIRl Board Conn. 14 pin



R520 close to JP29

Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

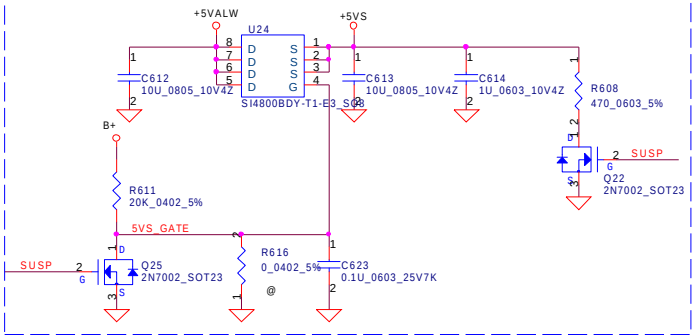
Compal Electronics,Ltd.

Title: **Audio Jack & SW connector**

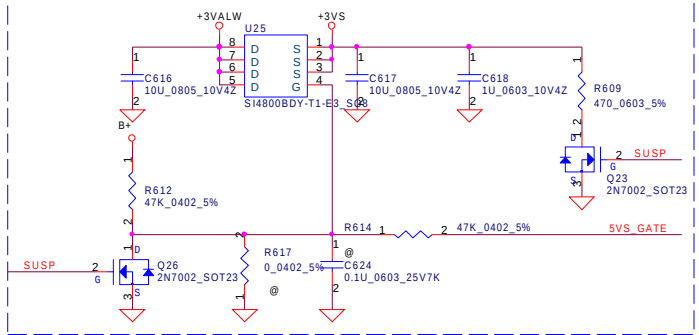
Size	Document Number	Rev
Custom	KIWB3/B4_LA4551P	0.1

Date: Friday, June 27, 2008 Sheet 39 of 49

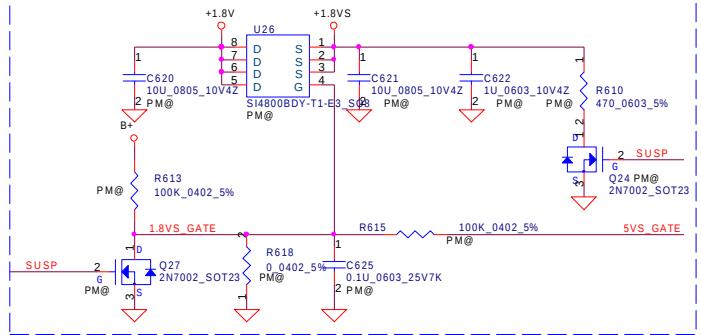
+5VALW TO +5VS



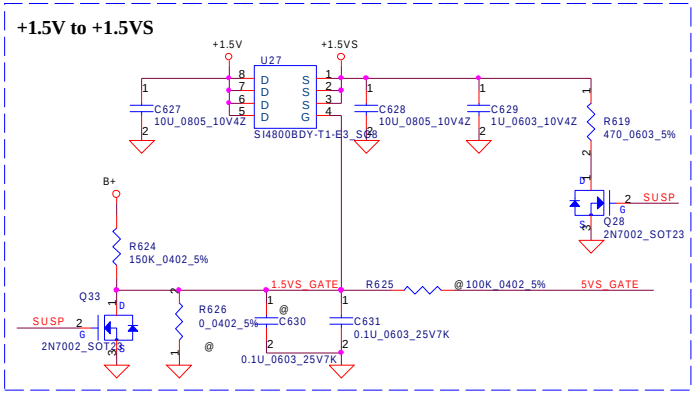
+3VALW TO +3VS

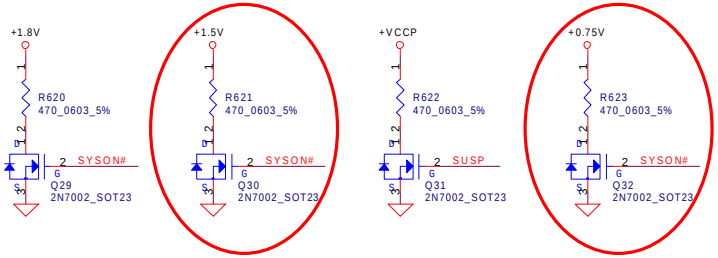


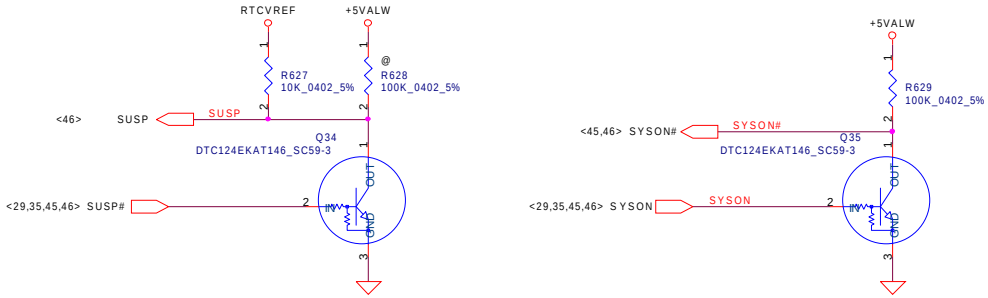
+1.8V to +1.8VS



+1.5V to +1.5VS







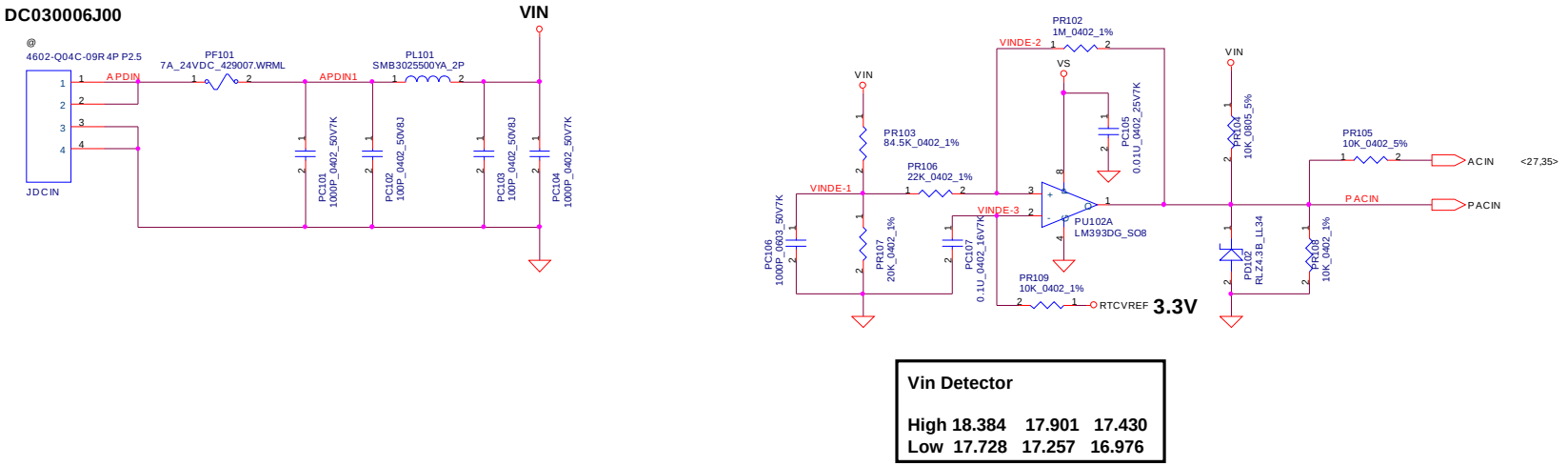
Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

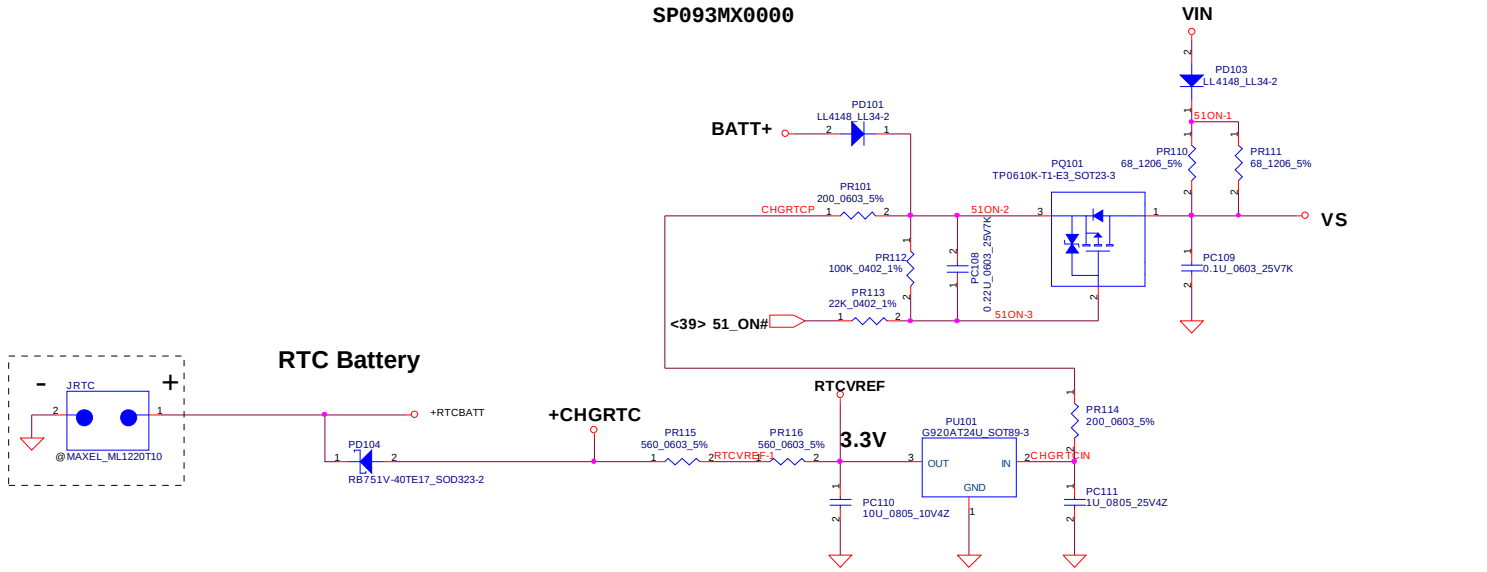
Title: DC Interface

Size	Document Number	Rev
Custom	KIWB3/B4_LA4551P	0.1

Date: Friday, June 27, 2008 Sheet 40 of 49



Vin Detector			
High	18.384	17.901	17.430
Low	17.728	17.257	16.976



Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

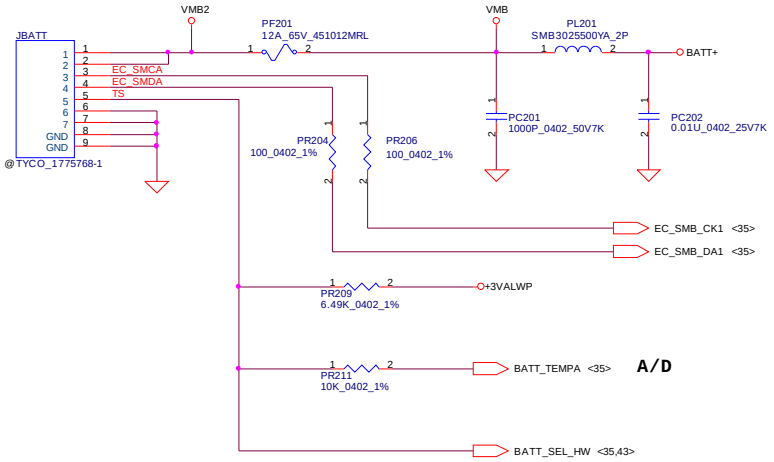
Compal Electronics, Inc.

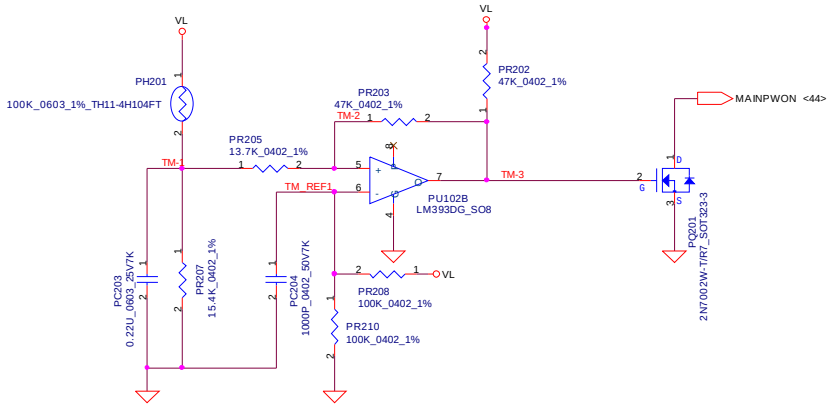
Title: DCIN & DETECTOR

Size	Document Number	Rev
Custom		0.1

Date: Friday, June 27, 2008 Sheet 41 of 49

PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C





Security Classification	Compal Secret Data		
Issued Date	2007/6/22	Deciphered Date	2008/6/22

Compal Electronics, Inc.

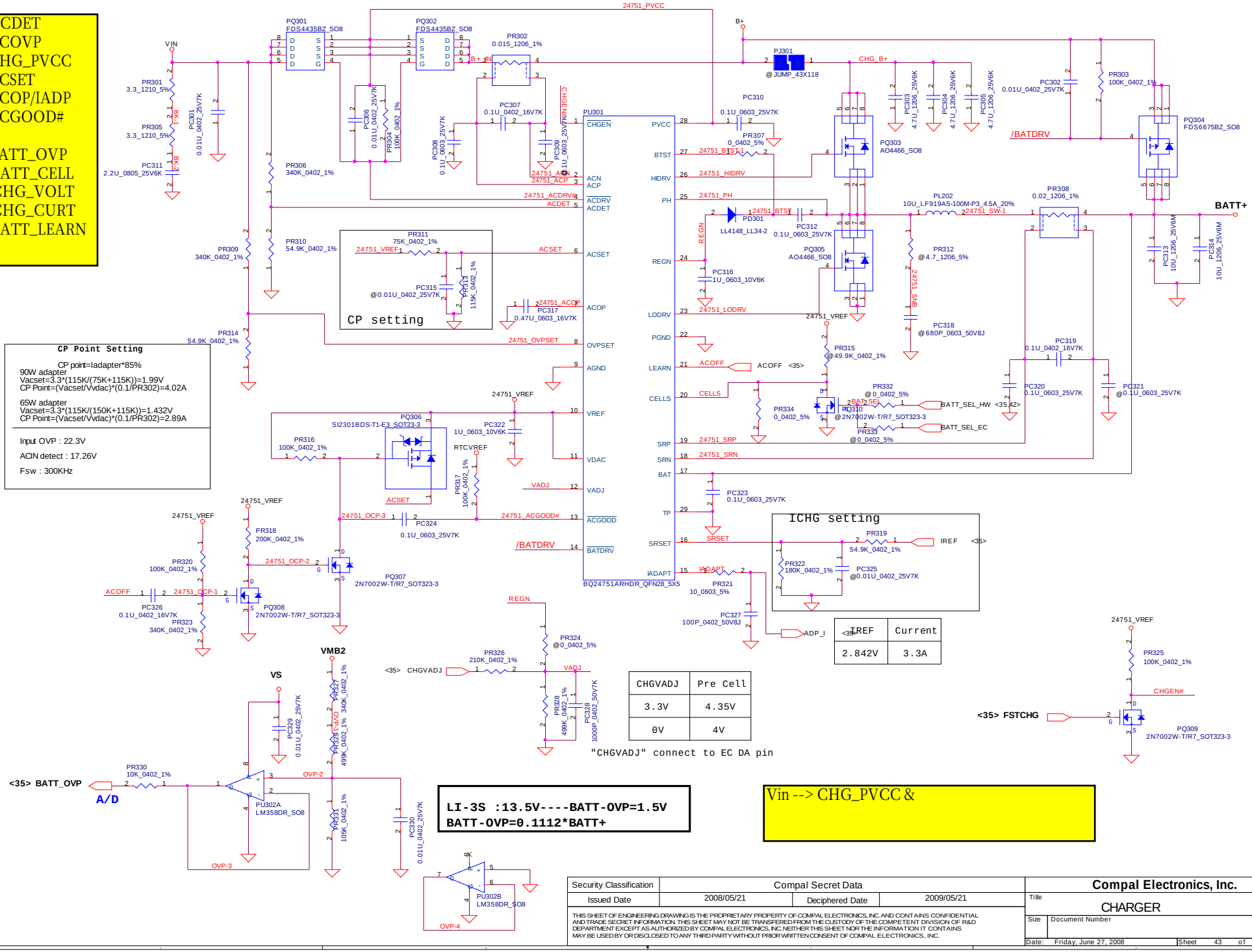
Title: BATTERY CONN / OTP

Size	Document Number	Rev
		0.1

Date: Friday, June 27, 2008 Sheet 42 of 49

1. ACDET
   ACOVP
   CHG_PVCC
   ACSET
   ACOP/IADP
   ACGOOD#

2. BATT_OVP
   BATT_CELL
   CHG_VOLT
   CHG_CURT
   BATT_LEARN



IREF	Current
2.842V	3.3A

CHGVADJ	Pre Cell
3.3V	4.35V
0V	4V

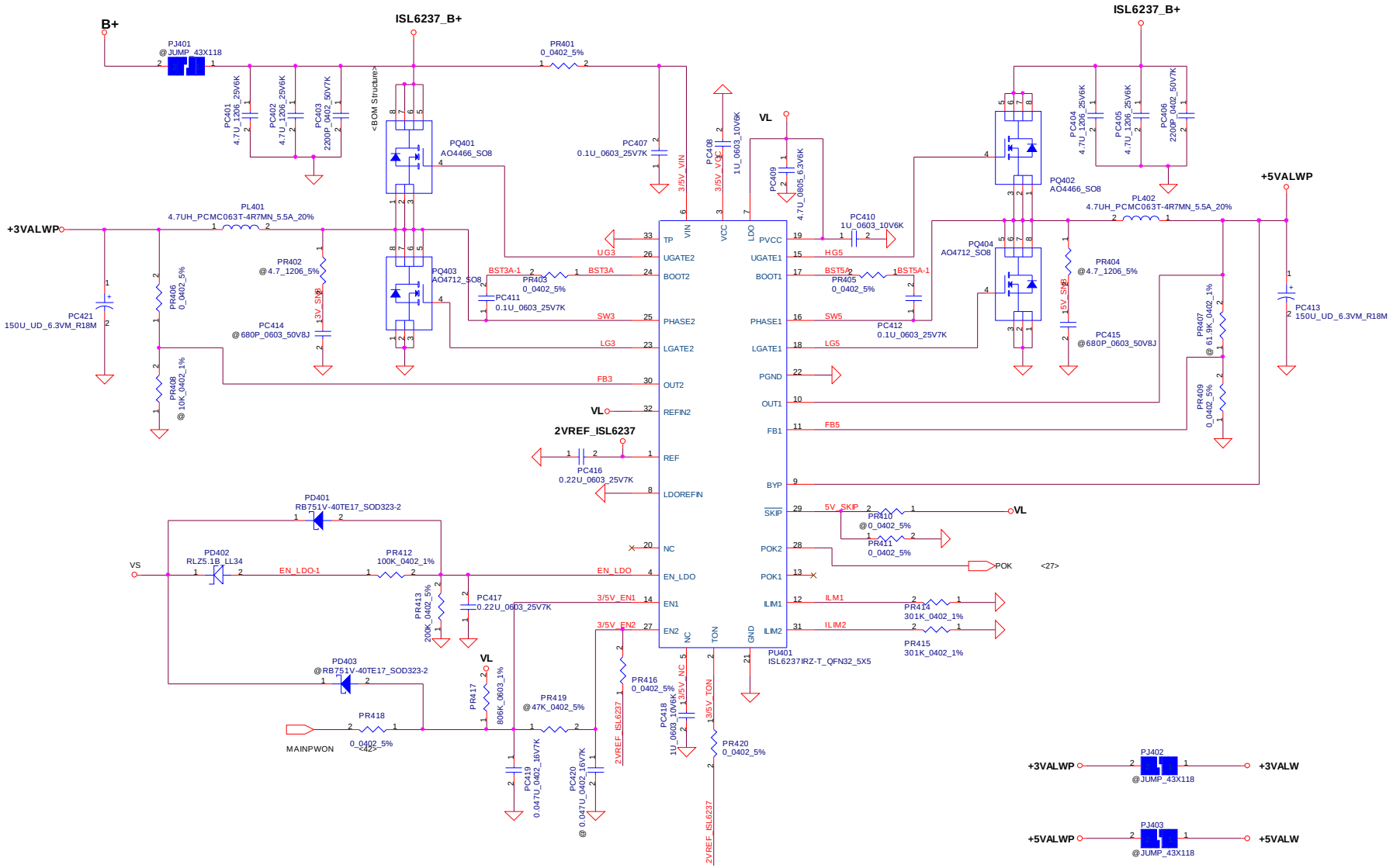
Security Classification	Compal Secret Data		
Issued Date	2008/05/21	Deciphered Date	2009/05/21

Compal Electronics, Inc.

Title: CHARGER

Size | Document Number | Rev 0.1

Date: Friday, June 27, 2008 | Sheet 43 of 49



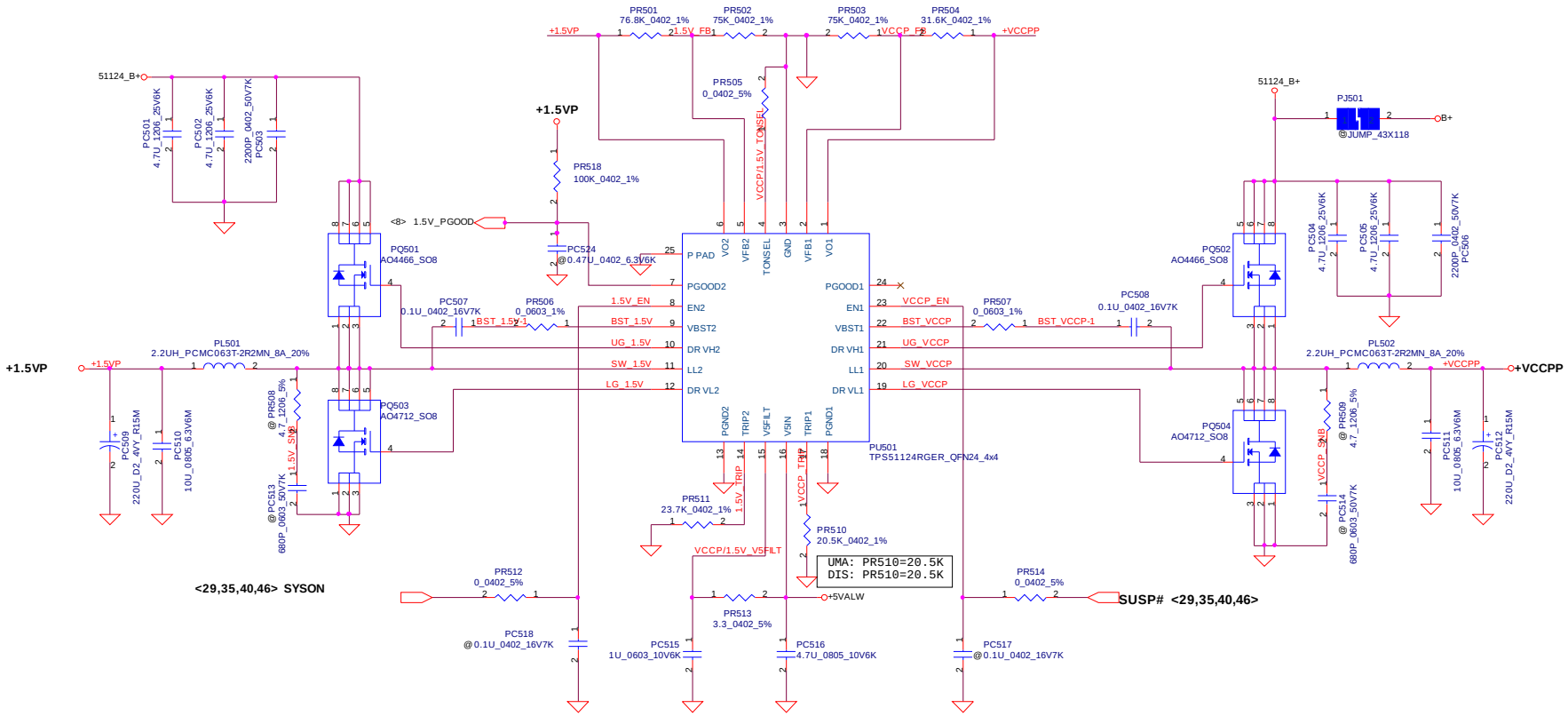
Security Classification	Compal Secret Data		
Issued Date	2007/06/22	Deciphered Date	2008/06/22

Compal Electronics, Inc.

Title: **3VALW/5VALW**

Size	Document Number	Rev
Custom		0.1

Date: Friday, June 27, 2008 | Sheet 44 of 49



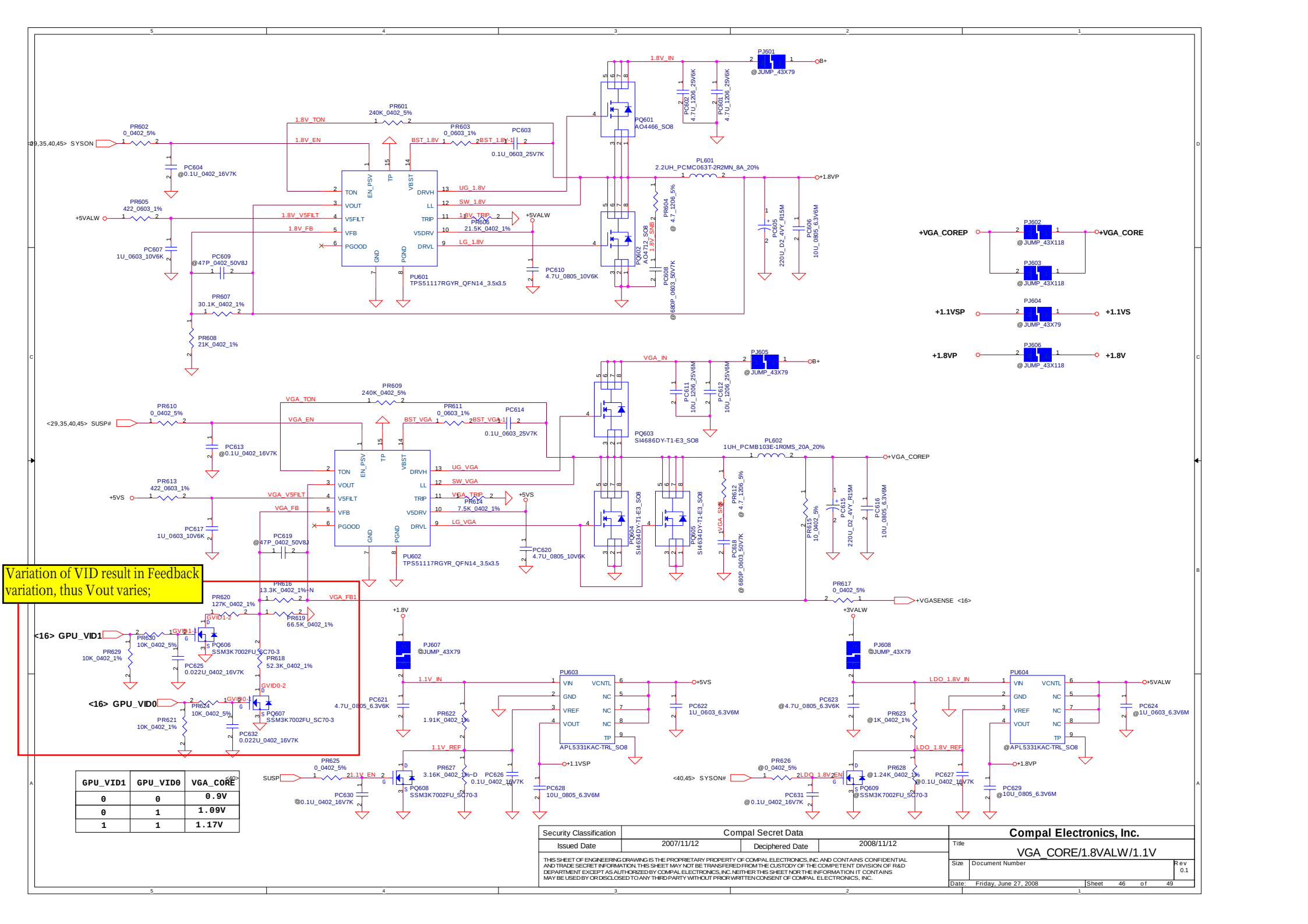
Security Classification	Compal Secret Data		
Issued Date	2007/11/12	Deciphered Date	2008/11/12

Compal Electronics, Inc.

Title: 1.8V / 0.9V

Size	Document Number	Rev
		0.1

Date: Friday, June 27, 2008 | Sheet 45 of 49



GPU_VID1	GPU_VID0	VGA_CORE
0	0	0.9V
0	1	1.09V
1	1	1.17V

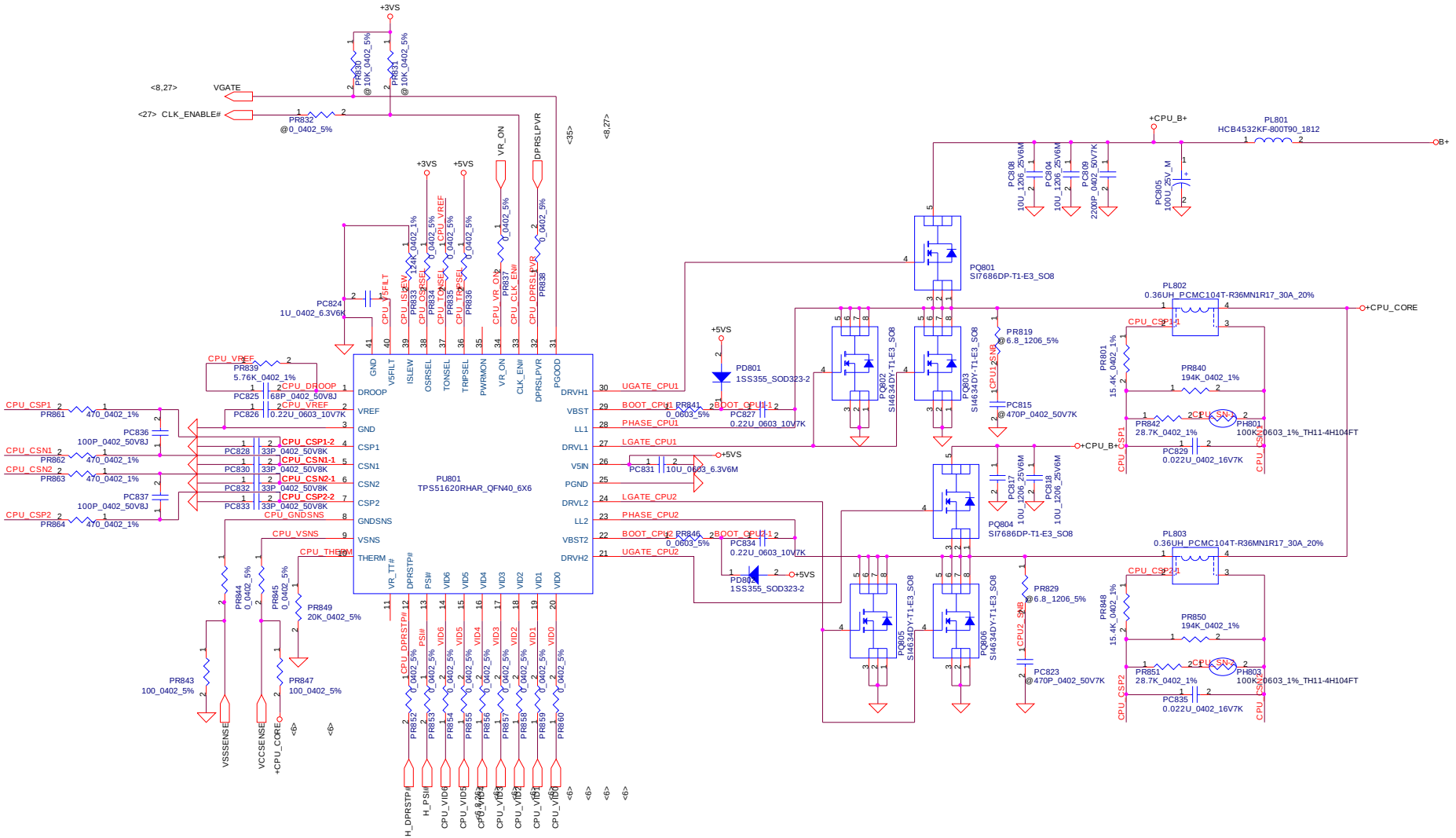
Security Classification	Compal Secret Data		
Issued Date	2007/11/12	Deciphered Date	2008/11/12

Compal Electronics, Inc.

Title: VGA_CORE/1.8VALW/1.1V

Size | Document Number | Rev 0.1

Date: Friday, June 27, 2008 | Sheet 46 of 49



Security Classification	Compal Secret Data		
Issued Date	2008/05/21	Deciphered Date	2009/05/21

Compal Electronics, Inc.

Title: +CPU_CORE

Size: Custom | Document Number | Rev: 0.1

Date: Friday, June 27, 2008 | Sheet 47 of 49

Version change list (P.I.R. List)

for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		**Schematic modify**	**0.1**	**41 43 46 47**	**Add PR334,PR861,PR862,PR863PR864 Canel PH802 Change PR841,PR846 to 0ohm Change PC831 to 10U Change PR840,PR850 to 194K Change PR801,PR848 to 15.4K Change PR842,PR851 to 28.7K Change PC106 to 1000P Change PC829,PC835 to 0.022U Change PR622 to 1.91K Change PR627 to 3.16K Change PR628 to 1.24K PU401 main source change to TPS51427**		EVT
2							
3							
4							
5							
6							
7							
8							
9							
10							
11							
12							
13							
14							
15							
16							
17							
18							
19							
20							
21							

Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number: <Doc> | Rev: 0.1

Date: Friday, June 27, 2008 | Sheet 48 of 49

NO DATE PAGE MODIFICATION LIST PURPOSE

Compal Electronics, Inc.

Title

HW PIR

Size	Document Number	Rev
B	KIWB3/B4_LA4551P	0.1

Date: Friday, June 27, 2008 Sheet 49 of 49