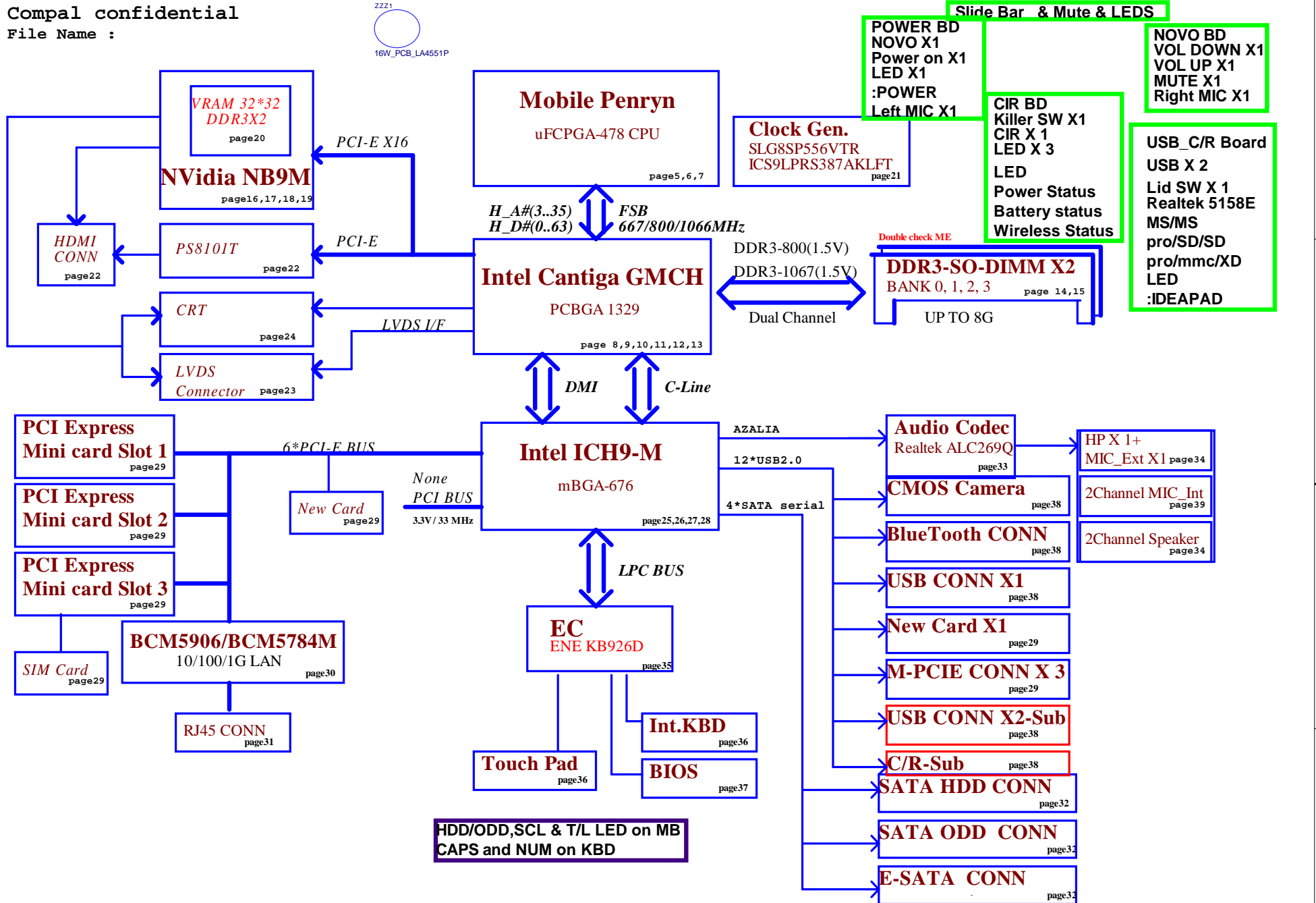


KIWB3/B4

Schematics Document

Mobile Penryn uFCPGA with Intel
Cantiga_GM/PM+ICH9-M core logic
REV:0.1

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HDD/ODD,SCL & T/L LED on MB
CAPS and NUM on KBD

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DDR3 Voltage Rails

power plane State	+B	+5VALW +3VALW	+1.5V +1.8V +0.75V	+5VS +3VS +1.5VS +1.1VS +VCCP +CPU_CORE +VGA_CORE +1.8VS
s0	o	o	o	o
s1	o	o	o	o
s3	o	o	o	x
s5 S4/AC	o	o	x	x
s5 S4/ Battery only	o	x	x	x
s5 S4/AC & Battery don't exist	x	x	x	x

PM@ , GM@ , N9@ , N10@

SMBUS, SPI and I2C Control Table

	SOURCE	HDMI	LVDS	CRT	HDCP	SERIAL EEPROM	NEW CARD	CLK GEN	CAP sensor	Mini CARD1	Mini CARD2	BATT	THERMAL SENSOR (VGA)	THERMAL SENSOR (CPU)
EC_SMB_CK1 EC_SMB_DA1	KB926	X	X	X	X	V	X	X	X	X	X	V	X	X
EC_SMB_CK2 EC_SMB_DA2	KB926	X	X	X	X	X	X	X	V	X	X	X	V	V
ICH_SMBCLK ICH_SMBDAT	ICH9	X	X	X	X	X	V	V	X	V	V	X	X	X
LVDS_SCL LVDS_SDA	Cantiga	X	V	X	X	X	X	X	X	X	X	X	X	X
GMCH_CRT_CLK GMCH_CRT_DAT	Cantiga	X	X	V	X	X	X	X	X	X	X	X	X	X
HDMI_CLK_NB HDMI_DAT_NB	Cantiga	V	X	X	X	X	X	X	X	X	X	X	X	X
VGA_DDCCLK VGA_DDCDATA	VGA	X	X	V	X	X	X	X	X	X	X	X	X	X
VGA_LVDS_SCL VGA_LVDS_DAT	VGA	X	V	X	X	X	X	X	X	X	X	X	X	X
VGA_HDMI_SCL VGA_HDMI_DAT	VGA	V	X	X	X	X	X	X	X	X	X	X	X	X
HDCP_SMB_CK1 HDCP_SMB_DA1	VGA	X	X	X	X	V	X	X	X	X	X	X	X	X
FSEL#SPIC#_SB FRD#SPI_SO_SB SPI_CLK_SB FWR#SPI_SI_SB	ICH9	X	X	X	X	V	X	X	X	X	X	X	X	X
FSEL#SPIC#_SO SPI_CLK FWR#SPI_SI	KB926	X	X	X	X	V	X	X	X	X	X	X	X	X

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VGA and DDR2 Voltage Rails (NB9M-GS)

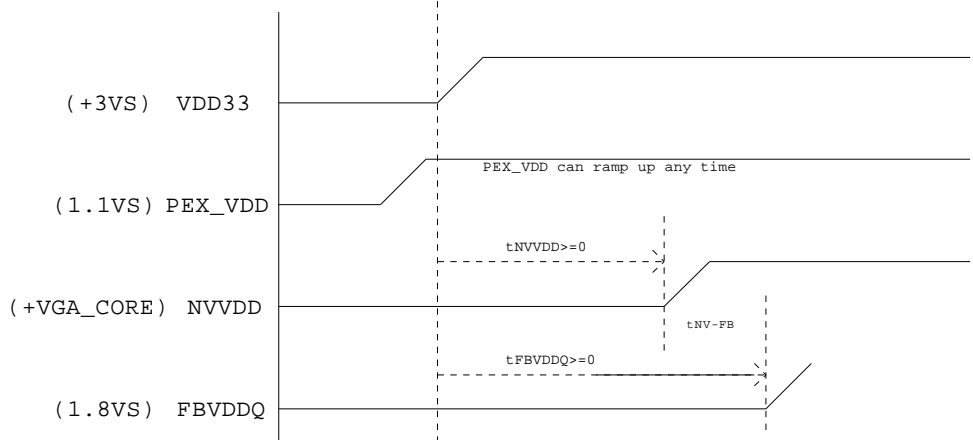
power plane			+1.8V	+3VS +VGA_CORE +1.1VS
State				
S0	○	○	○	○
S1	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

EDP at Tj = 97C*

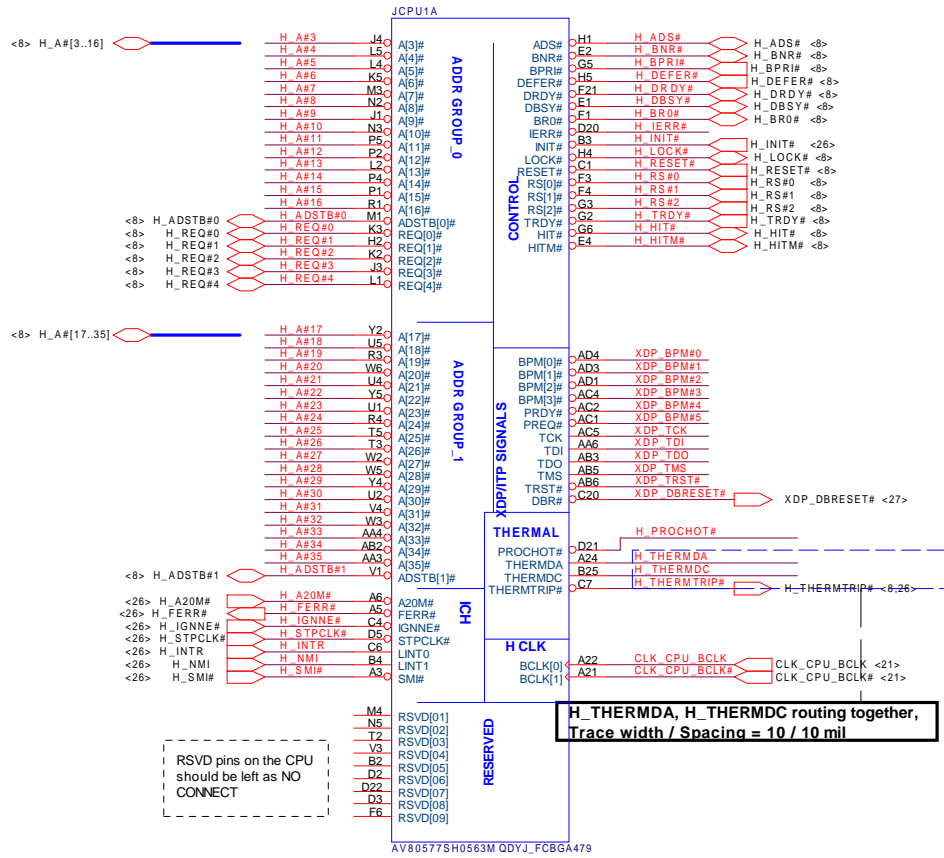
Power Supply Rail	(V)	NB9M-GS		NB9M-GE	
		GDDR3	DDR2	GDDR3	DDR2
NVVD	Variable	11.22A	10.87A	9.2A	8.88A
FB_DLLAVDD	1.1	25mA			
FB_PLLAVDD	1.1	10mA			
IFPC_IOVDD	1.1	385mA			
IFPD_IOVDD	1.1	385mA			
IFPE_IOVDD	1.1	385mA			
IFPF_IOVDD	1.1	385mA			
PEX_IOVDD/Q	1.1	1550mA			
PEX_PLLVDD	1.1	165mA			
PLLVD	1.1	55mA			
SP_PLLVDD	1.1	25mA			
VID_PLLVDD	1.1	50mA			
TOTAL	1.1	3.425A			
FBVDD/Q	1.8	2.24A	1.65A	2.17A	1.63A
IFPA_IOVDD	1.8	50mA			
IFPB_IOVDD	1.8	50mA			
IFPAB_PLLVDD	1.8	100mA			
IFPCD_PLLVDD	1.8	160mA			
IFPEF_PLLVDD	1.8	160mA			
TOTAL	1.8	2.76A	2.17A	2.69A	2.15A
DACA_VDD	3.3	110mA			
DACB_VDD	3.3	125mA			
DACC_VDD	3.3	110mA			
MIOA_VDDQ	3.3	10mA			
MIOB_VDDQ	3.3	10mA			
VDD33	3.3	80mA			
TOTAL	3.3	0.445A			

POWER SQUENCE

The ramp time for any rail must be more than 40us

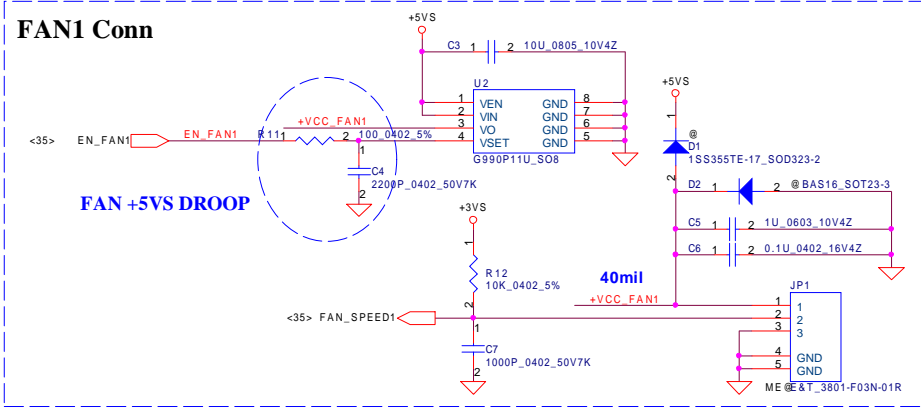
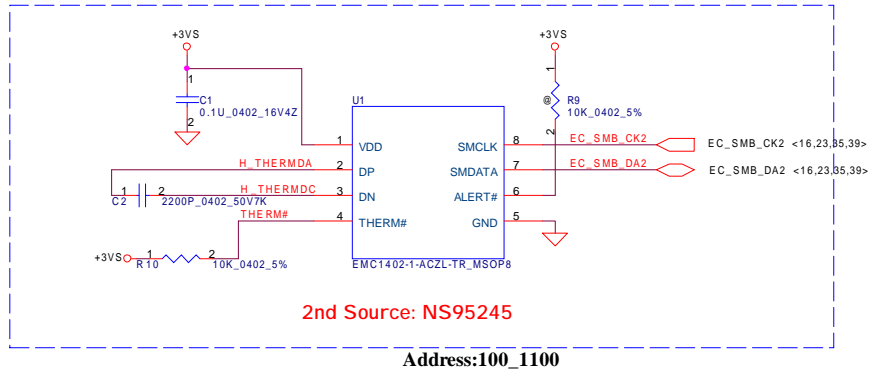
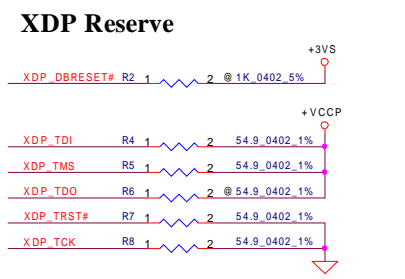
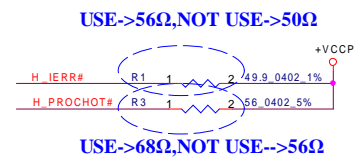


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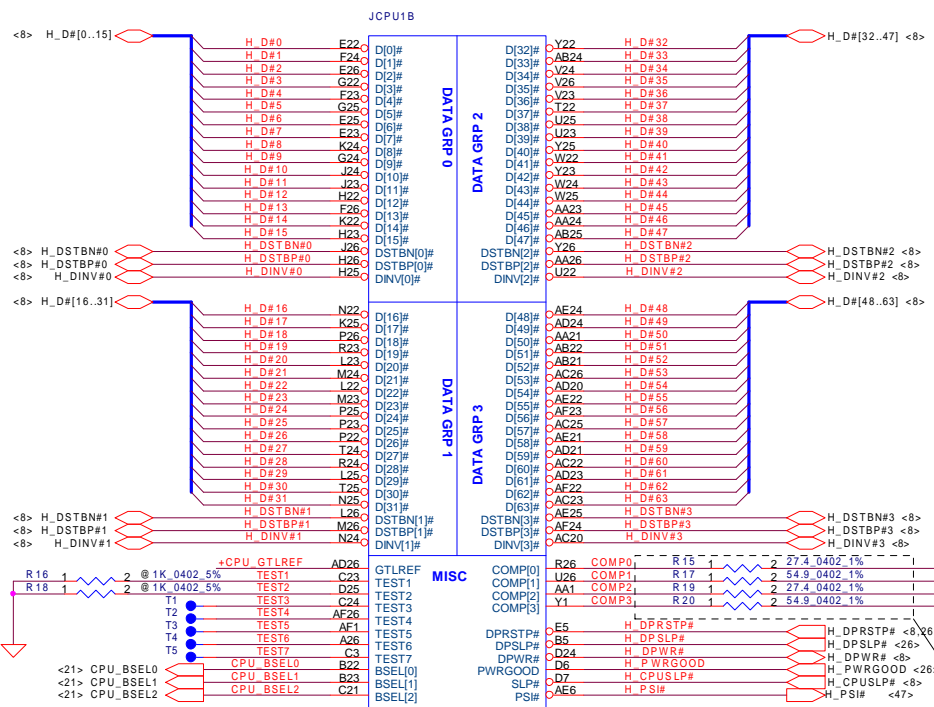


RSVD pins on the CPU should be left as NO CONNECT

H_THERMDA, H_THERMDC routing together, Trace width / Spacing = 10 / 10 mil



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Trace Close CPU < 0.5'

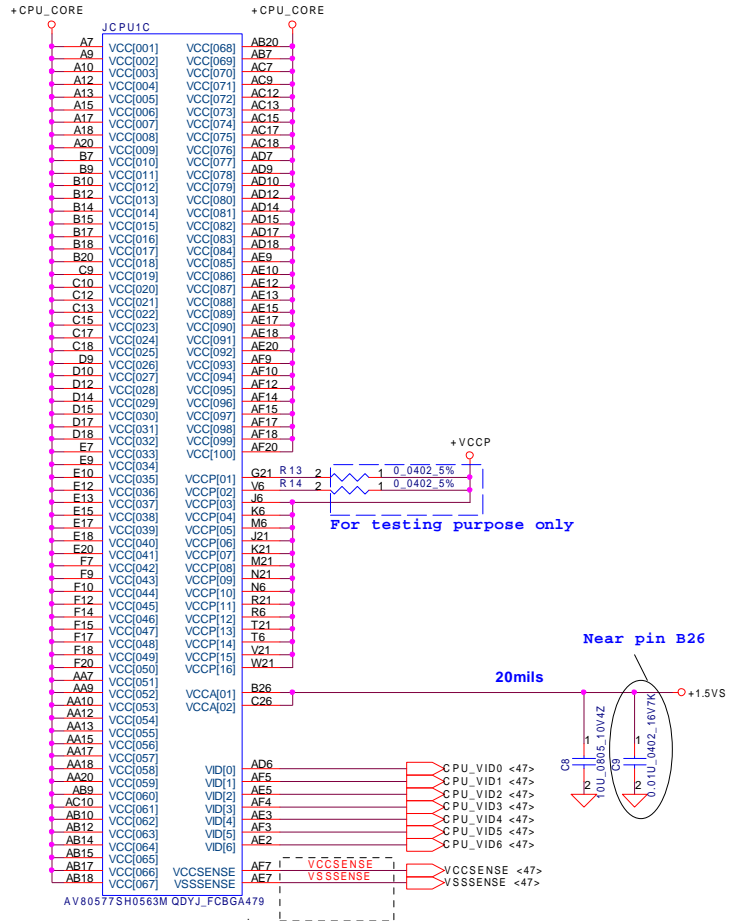
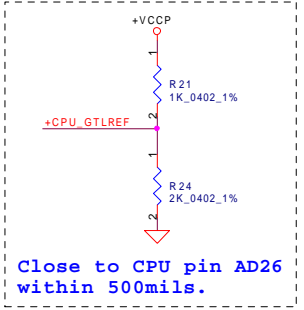
Width=4 mil,
Spacing: 15mil
(550hm)

TRACE CLOSELY CPU < 0.5'

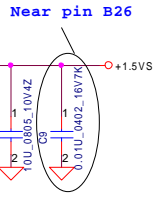
COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4Ohms)
COMP1, COMP3 layout : Width 5mils and Space 25mils (550hms)

layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

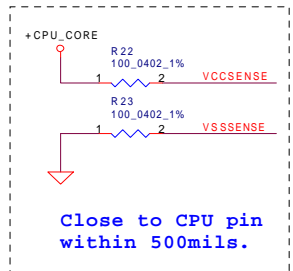


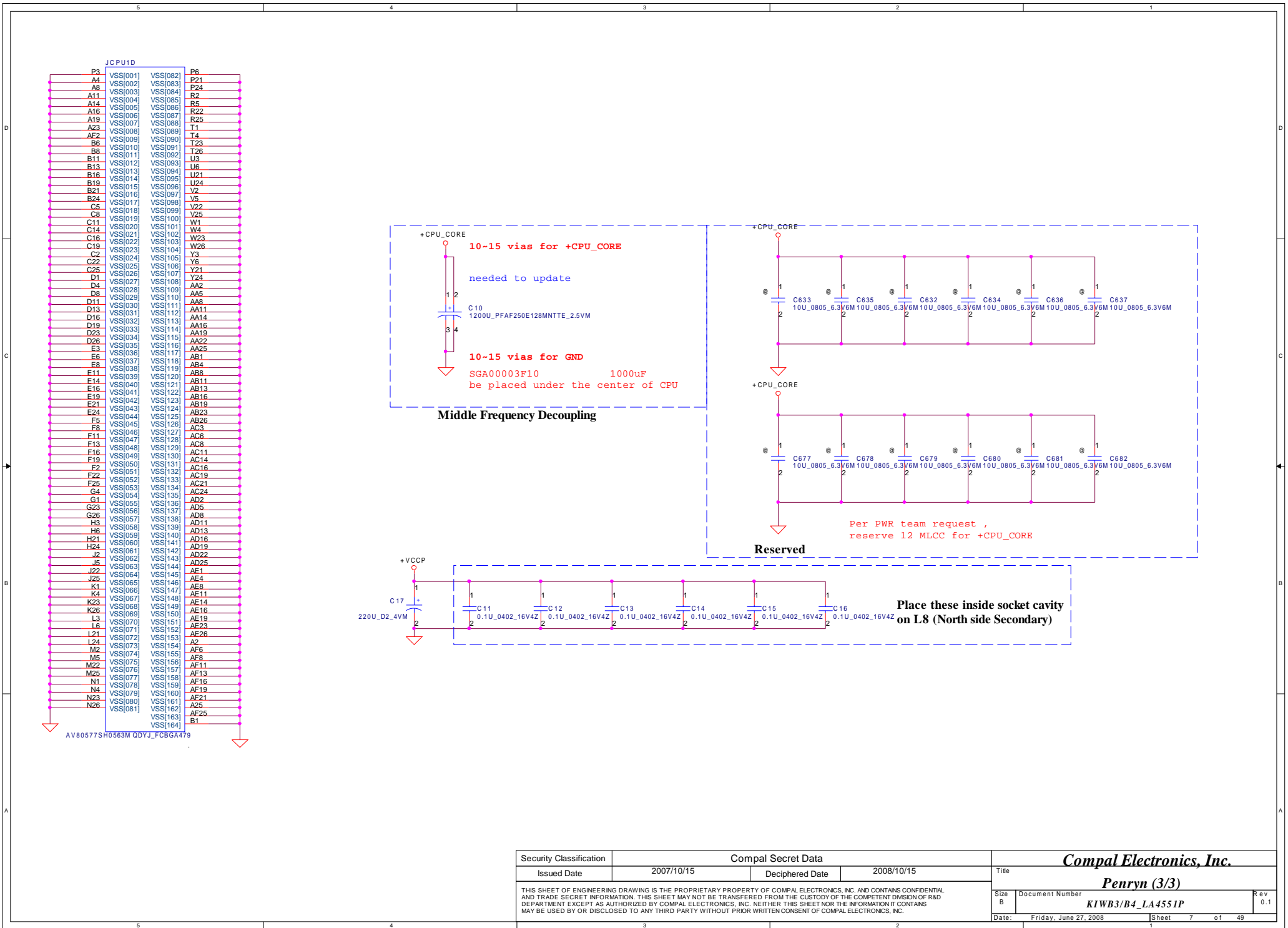
For testing purpose only



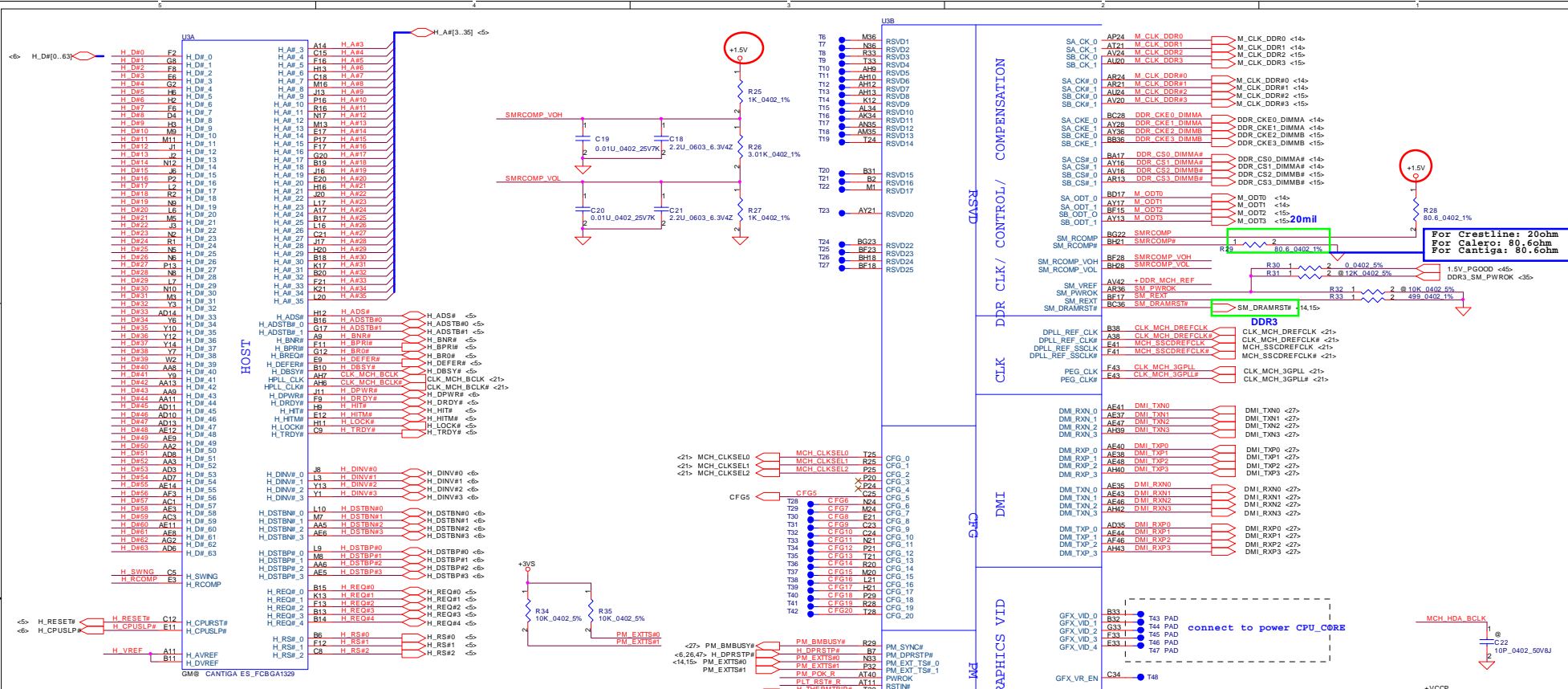
Length match within 25 mils.
The trace width/space/other is
18/7/25.

Layout Note:
Route VCCSENSE and VSSSENSE traces at
27.4 Ohms with 50 mil spacing.
Place PU and PD within 1 inch of CPU.
Length matched to within 25 mils.

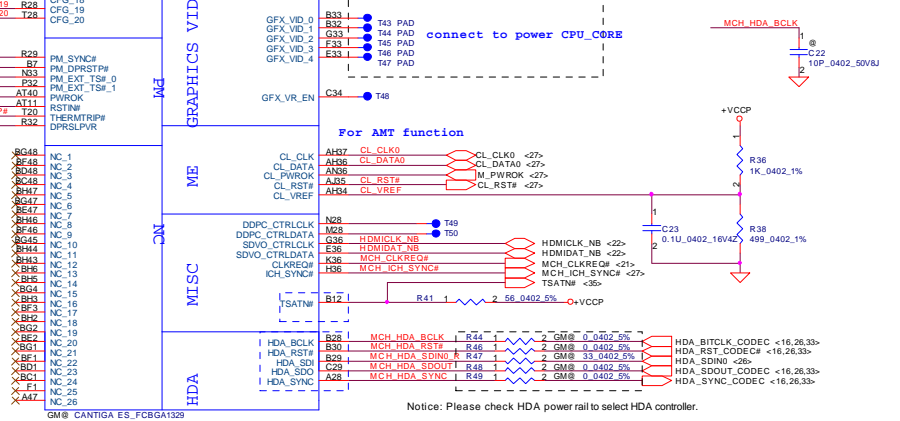
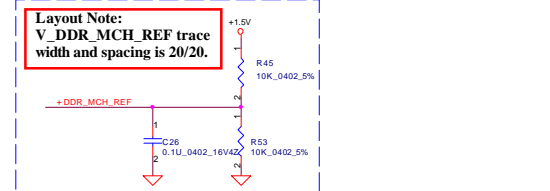
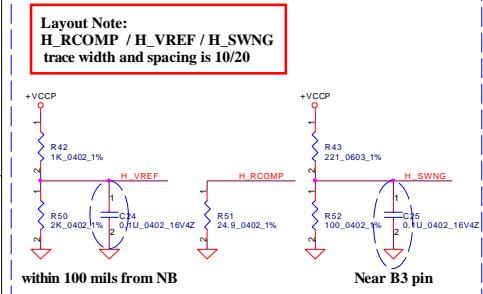




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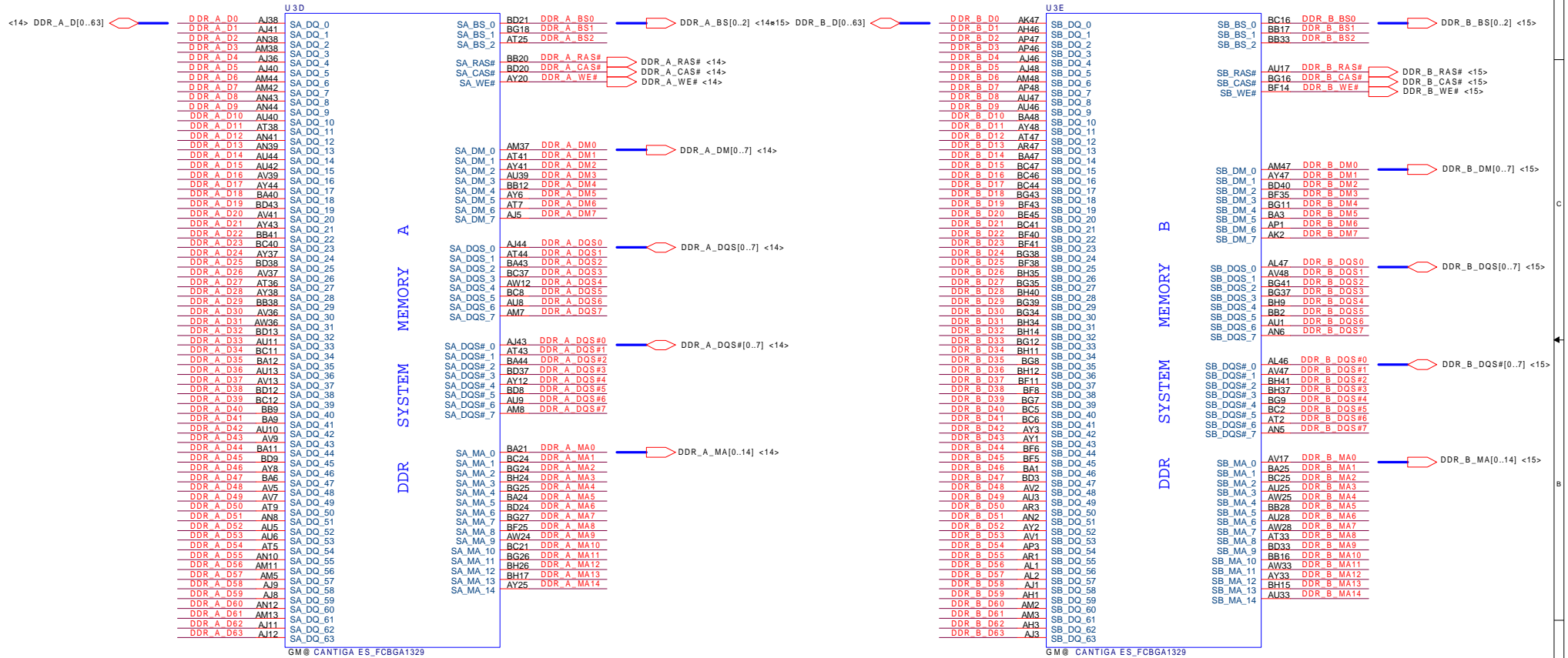
layout note:
Route H_SCOMP and H_SCOMP# with trace width spacing and impedance (55 ohm) same as FSB data traces



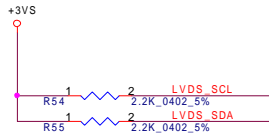
Notice: Please check HDA power rail to select HDA controller.

MEMORY 7-GROUPS

1. Data Bus;
 2. Data Strobe Differential Pairs;
 3. Data Mask Bits;
 4. Address Group;
 5. Bank Select Group;
 6. Command Group;
 7. CLK Group;
- *. Reset Group;

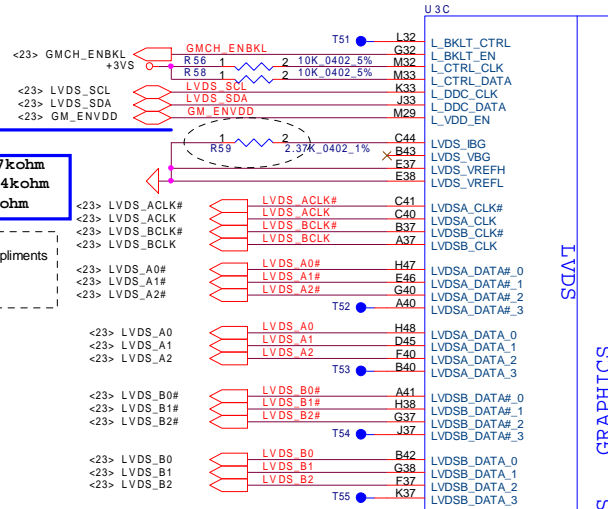


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Size	B	Document Number	KTWB3/B4_LA4551P	Rev	0.1
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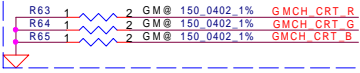


For Cantiga: 2.37kohm
For Crestline: 2.4kohm
For Calero: 1.5kohm

Note: All LVDS data signals and its compliments should be routed Differentially



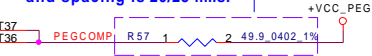
Layout Note: Place 150 Ω termination resistors close to GMCH



change R64, R65 from 33ohm to 30ohm by checklist.2.0 & CRB1.0 05/08/08

For Cantiga: 1.02kohm
For Crestline: 1.3kohm
For Calero: 255ohm

Place the resistor within 500mils (1.27mm) of the (G)MCH
PEGCOMP trace width and spacing is 20/25 mils.



Please check Power source if want support IAMT

Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane, 15->0, 14->1 1 = Normal Operation, Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) 1 = Reverse Lane *
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.

GRAPHICS

PCI-EXPRESS

TV

VGA

PEG_TX#_0	J41	PCIE MTX GRX N0	C27	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX N0
PEG_TX#_1	M46	PCIE MTX GRX N1	C28	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX N1
PEG_TX#_2	M47	PCIE MTX GRX N2	C29	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX N2
PEG_TX#_3	M40	PCIE MTX GRX N3	C30	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX N3
PEG_TX#_4	M42	PCIE MTX GRX N4	C31	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX N4
PEG_TX#_5	R48	PCIE MTX GRX N5	C32	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX N5
PEG_TX#_6	N38	PCIE MTX GRX N6	C33	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX N6
PEG_TX#_7	T47	PCIE MTX GRX N7	C34	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX N7
PEG_TX#_8	U37	PCIE MTX GRX N8	C35	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX N8
PEG_TX#_9	U40	PCIE MTX GRX N9	C36	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX N9
PEG_TX#_10	Y40	PCIE MTX GRX N10	C37	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX N10
PEG_TX#_11	AA46	PCIE MTX GRX N11	C38	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX N11
PEG_TX#_12	AA40	PCIE MTX GRX N12	C39	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX N12
PEG_TX#_13	AD43	PCIE MTX GRX N14	C41	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX N14
PEG_TX#_14	AC46	PCIE MTX GRX N15	C42	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX N15
PEG_TX#_15							
PEG_TX_0	J42	PCIE MTX GRX P0	C43	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX P0
PEG_TX_1	L46	PCIE MTX GRX P1	C44	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX P1
PEG_TX_2	M48	PCIE MTX GRX P2	C45	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX P2
PEG_TX_3	M39	PCIE MTX GRX P3	C46	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX P3
PEG_TX_4	M43	PCIE MTX GRX P4	C47	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX P4
PEG_TX_5	R47	PCIE MTX GRX P5	C48	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX P5
PEG_TX_6	N37	PCIE MTX GRX P6	C49	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX P6
PEG_TX_7	T39	PCIE MTX GRX P7	C50	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX P7
PEG_TX_8	U36	PCIE MTX GRX P8	C51	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX P8
PEG_TX_9	U39	PCIE MTX GRX P9	C52	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX P9
PEG_TX_10	Y39	PCIE MTX GRX P10	C53	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX P10
PEG_TX_11	Y46	PCIE MTX GRX P11	C54	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX P11
PEG_TX_12	AA36	PCIE MTX GRX P12	C55	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX P12
PEG_TX_13	AD39	PCIE MTX GRX P13	C56	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX P13
PEG_TX_14	AD42	PCIE MTX GRX P14	C57	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX P14
PEG_TX_15	AD46	PCIE MTX GRX P15	C58	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX P15
		PCIE MTX GRX P3	C59	1	2	GM@ 0.1U 0402 10V7K	
		PCIE MTX GRX N3	C60	1	2	GM@ 0.1U 0402 10V7K	TMDS_B_CLK <22>
		PCIE MTX GRX P2	C61	1	2	GM@ 0.1U 0402 10V7K	TMDS_B_CLK# <22>
		PCIE MTX GRX N2	C62	1	2	GM@ 0.1U 0402 10V7K	TMDS_B_DATA0 <22>
		PCIE MTX GRX P1	C63	1	2	GM@ 0.1U 0402 10V7K	TMDS_B_DATA1 <22>
		PCIE MTX GRX N1	C64	1	2	GM@ 0.1U 0402 10V7K	TMDS_B_DATA1# <22>
		PCIE MTX GRX P0	C65	1	2	GM@ 0.1U 0402 10V7K	TMDS_B_DATA2 <22>
		PCIE MTX GRX N0	C66	1	2	GM@ 0.1U 0402 10V7K	TMDS_B_DATA2# <22>
		PCIE GTX C MRX P3	R71	1	2	GM@ 0.0402 5%	TMDS_B_HPD# <22>

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		2008/04/

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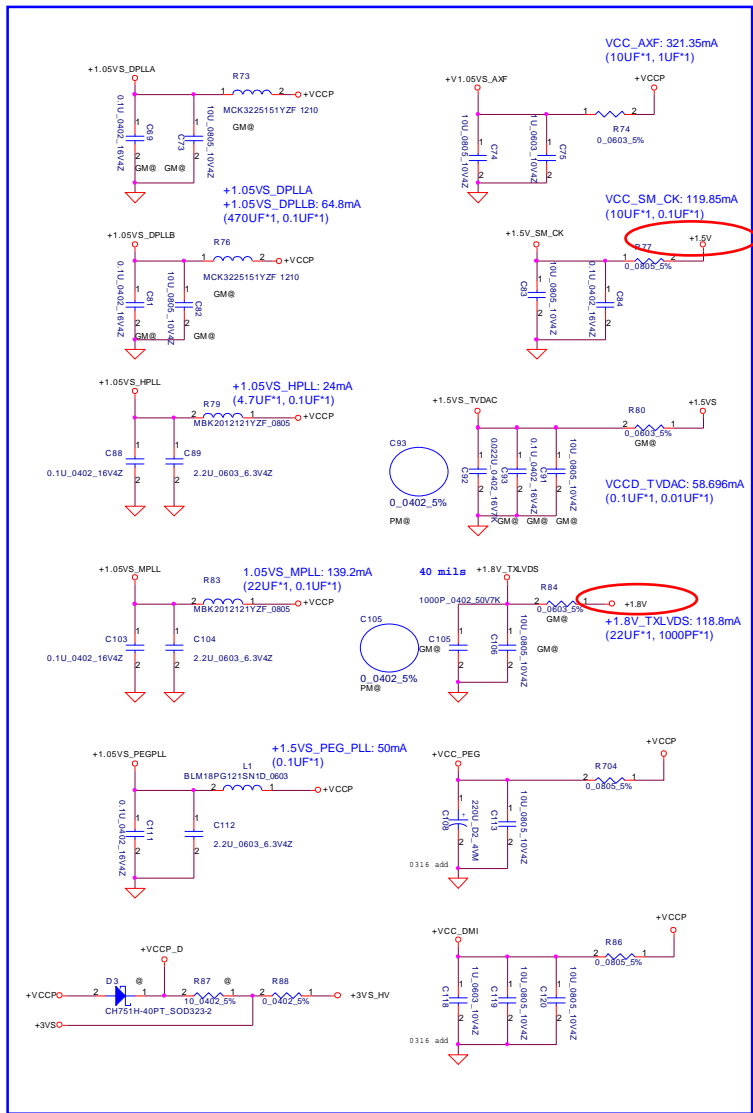
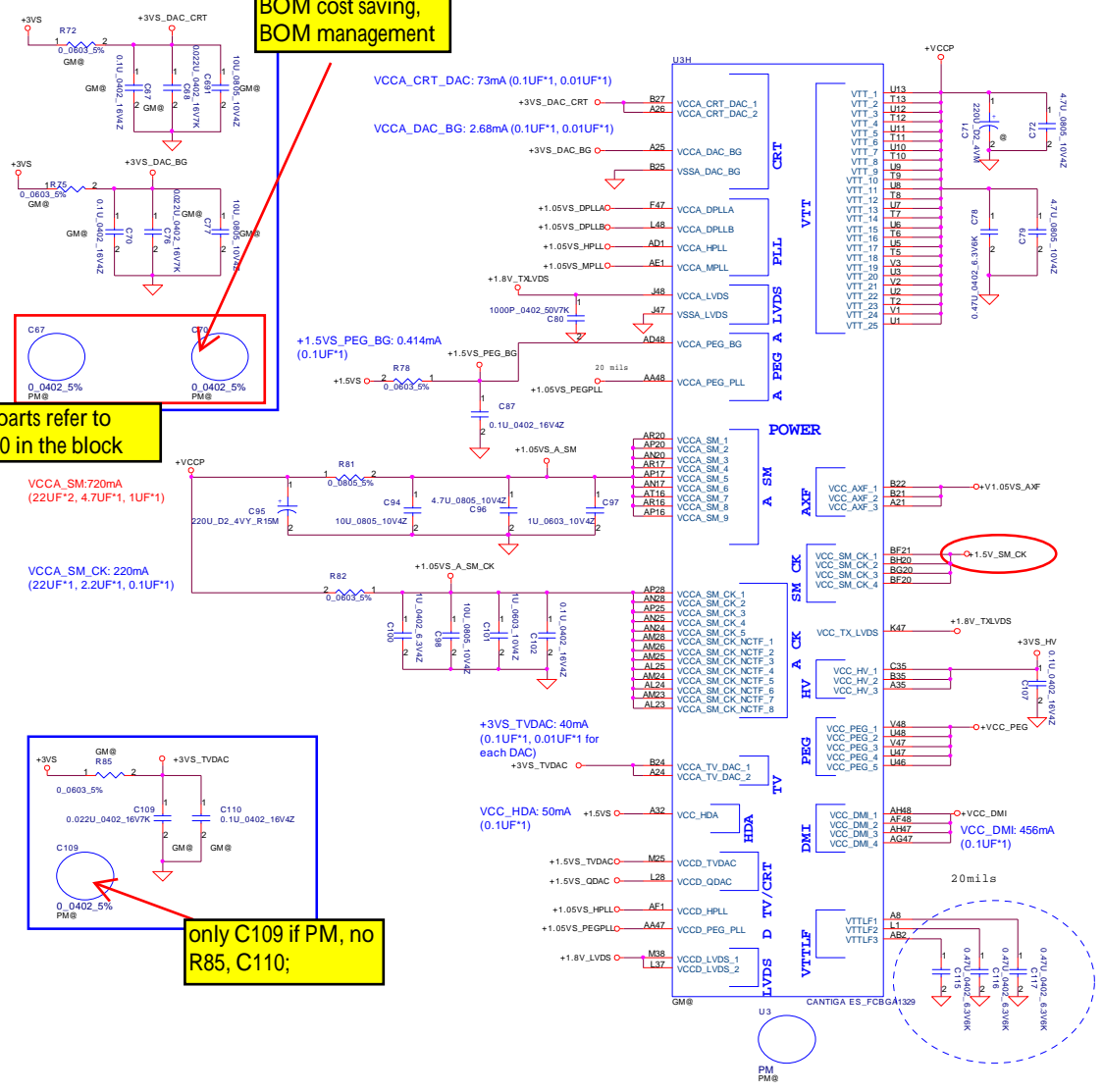
Compal Electronics, Ltd.	
Title Cantiga(3/6)-VGA/LVDS/TV	
Size	Document Number
Customer	KIWB3/B4_LA4551P
Date:	Friday, June 27, 2008
Sheet	10 of 49

**BOM cost saving,
BOM management**

**the two parts refer to
C67, C70 in the block**

**only C109 if PM, no
R85, C110;**

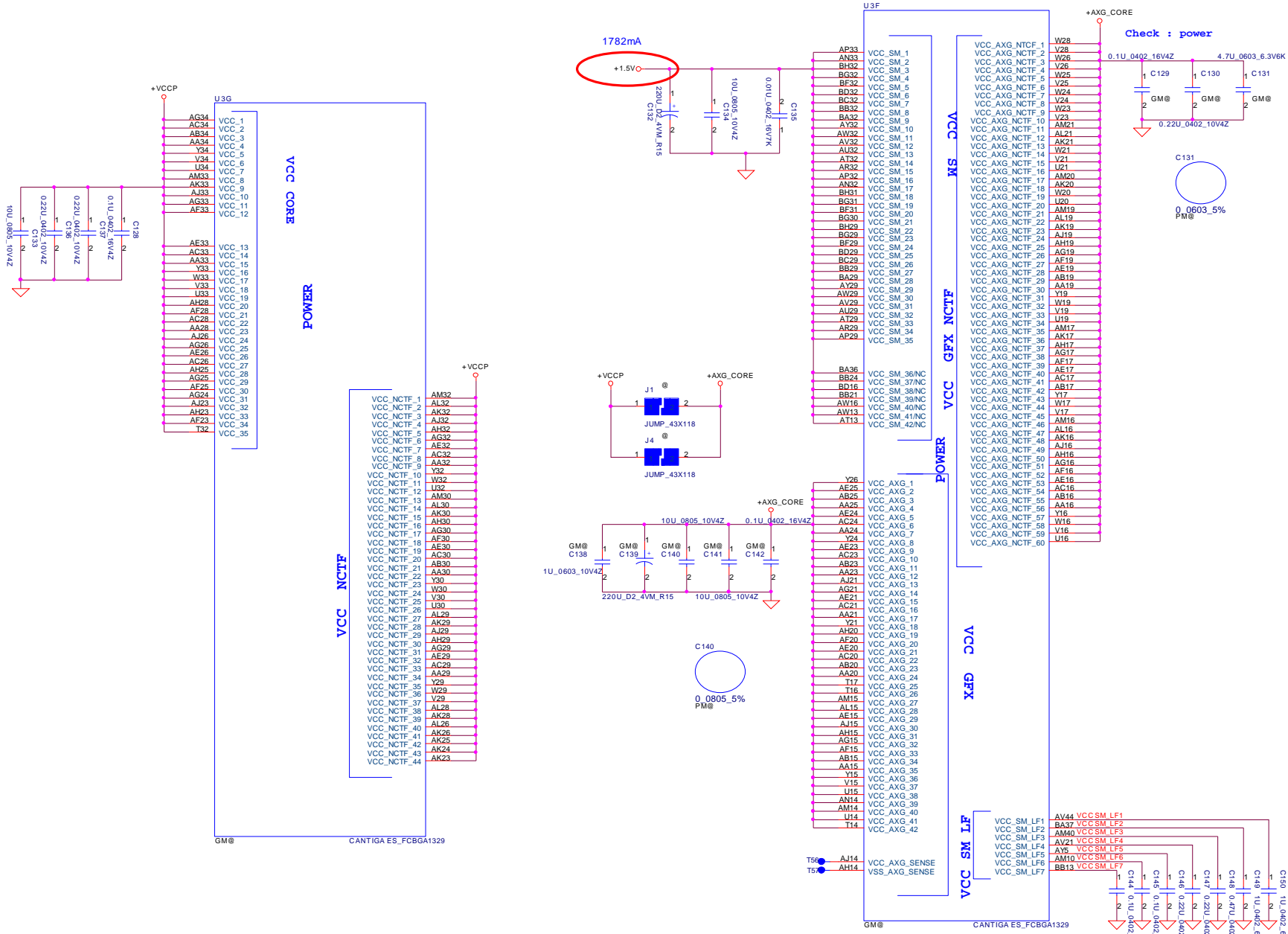
**value of bypass cap. depends on the
maximum switching current and
impedance of the trace;**



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Date	Friday, June 27, 2008	Sheet	11	of 49

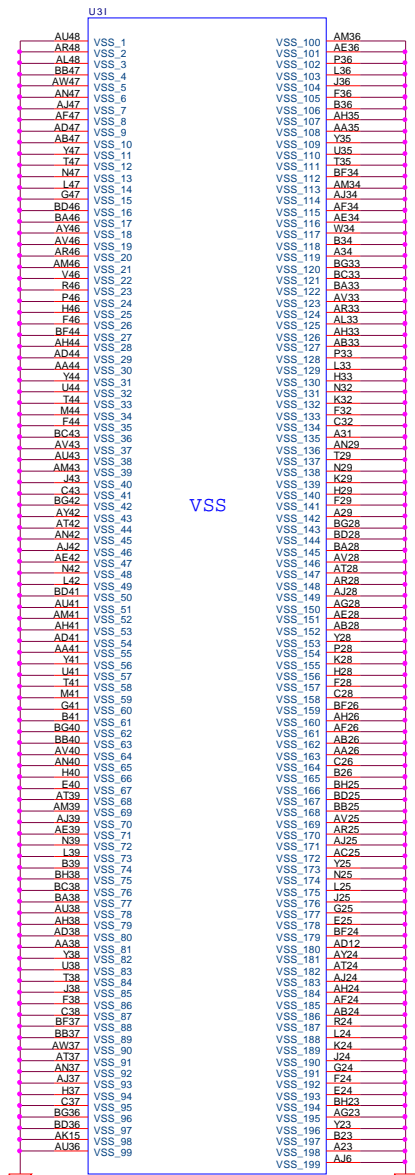
Compal Electronics, Inc.
Crestline GMCH (4/6)-VCC

Size: Document Number
Custom: **KIWB3/B4_LA4551P**

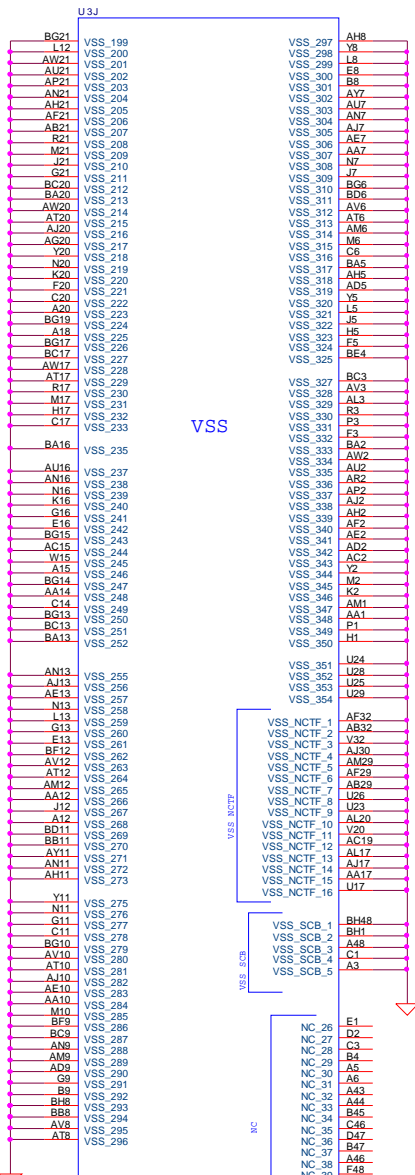


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Title	
Size	Document Number
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Date:	Friday, June 27, 2008
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GM® CANTIGA ES_FCBGA1329



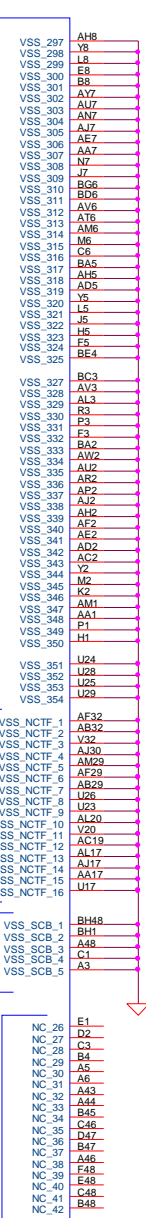
GM® CANTIGA ES_FCBGA1329

VSS

VSS NCTF

VSS SCB

NC



NC 26

NC 27

NC 28

NC 29

NC 30

NC 31

NC 32

NC 33

NC 34

NC 35

NC 36

NC 37

NC 38

NC 39

NC 40

NC 41

NC 42

E1

D2

C3

B4

A5

A6

A43

A44

B45

C46

D47

E48

F49

G50

H51

I52

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			Rev	0.1
Date:	Friday, June 27, 2008	Sheet	13	of 49

Compal Electronics, Inc.

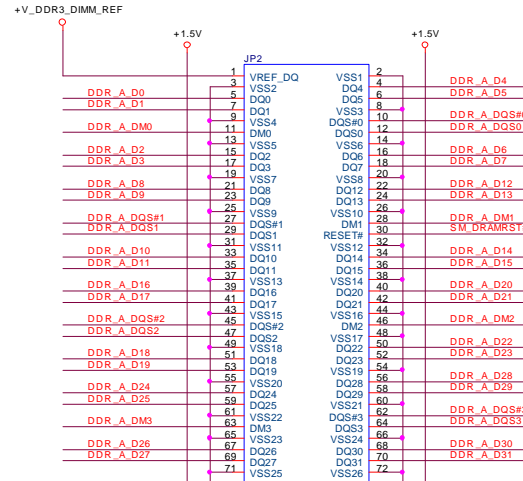
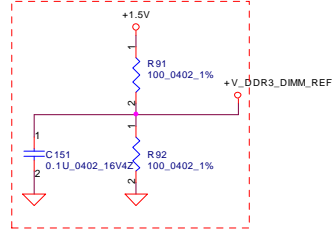
Cantiga GMCH (6/6)-GND

KIWB3/B4_LA4551P

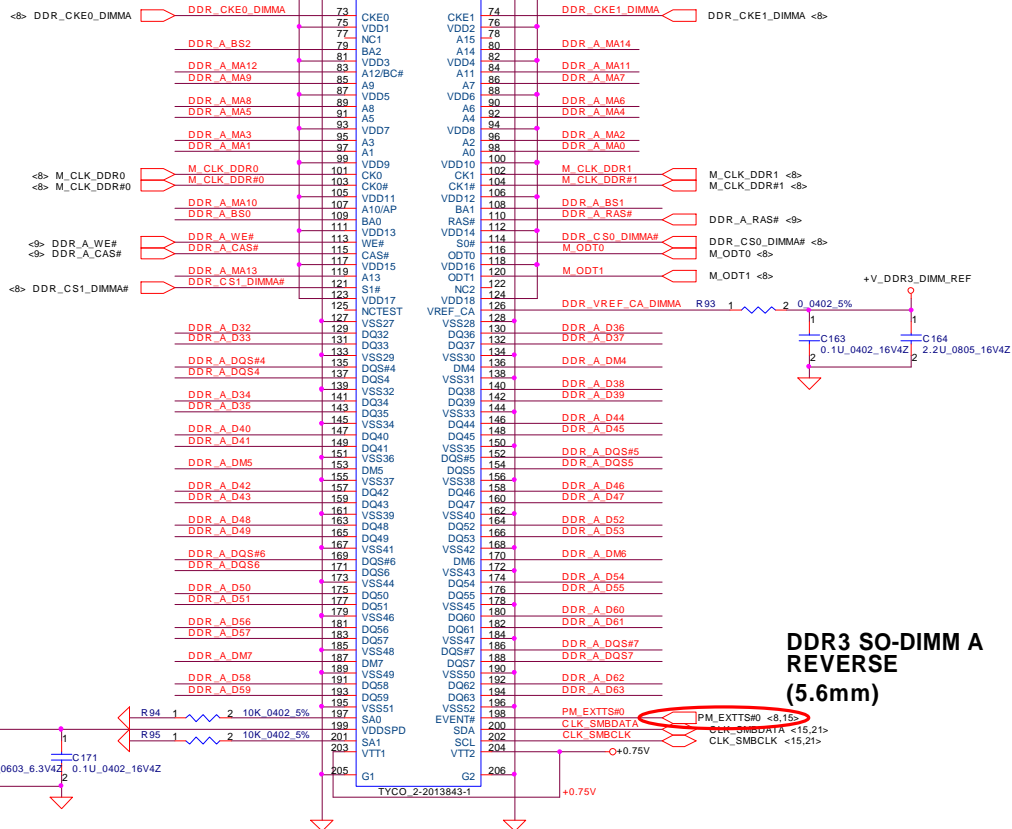
Friday, June 27, 2008

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- <9> DDR_A_DQS#0[0..7]
- <9> DDR_A_D0[0..63]
- <9> DDR_A_DM0[0..7]
- <9> DDR_A_DQS[0..7]
- <9> DDR_A_MA[0..14]
- <9> DDR_A_BS[0..2]



SM_DRAMRST# <8,1>

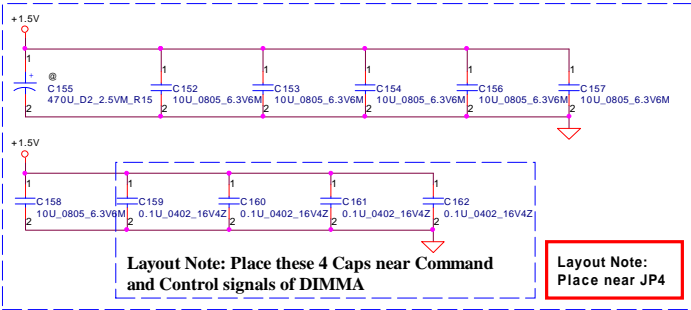


DDR3 SO-DIMM A
REVERSE
(5.6mm)

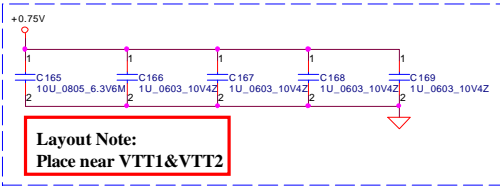
PM_EXTTS#0 <8,15>

CLK_SMBDATA <15,21>

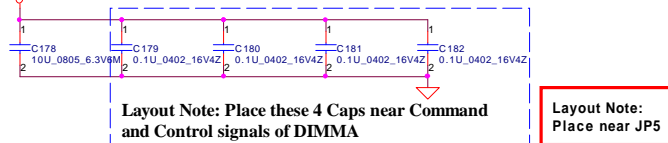
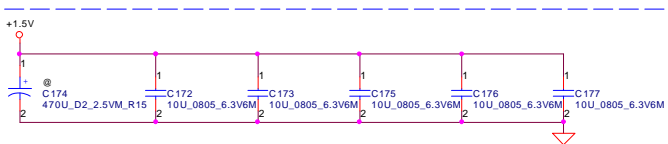
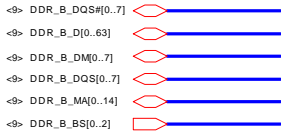
CLK_SMBCLK <15,21>



Layout Note:
Place near JP4

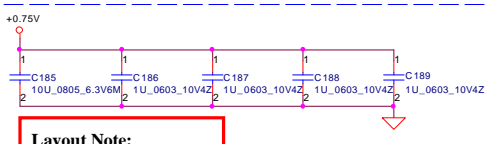


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Size	Document Number	Rev			
Custom	KIWB3/B4_LA4551P	0.1			
Date	Friday, June 27, 2008	Sheet	14	of	49

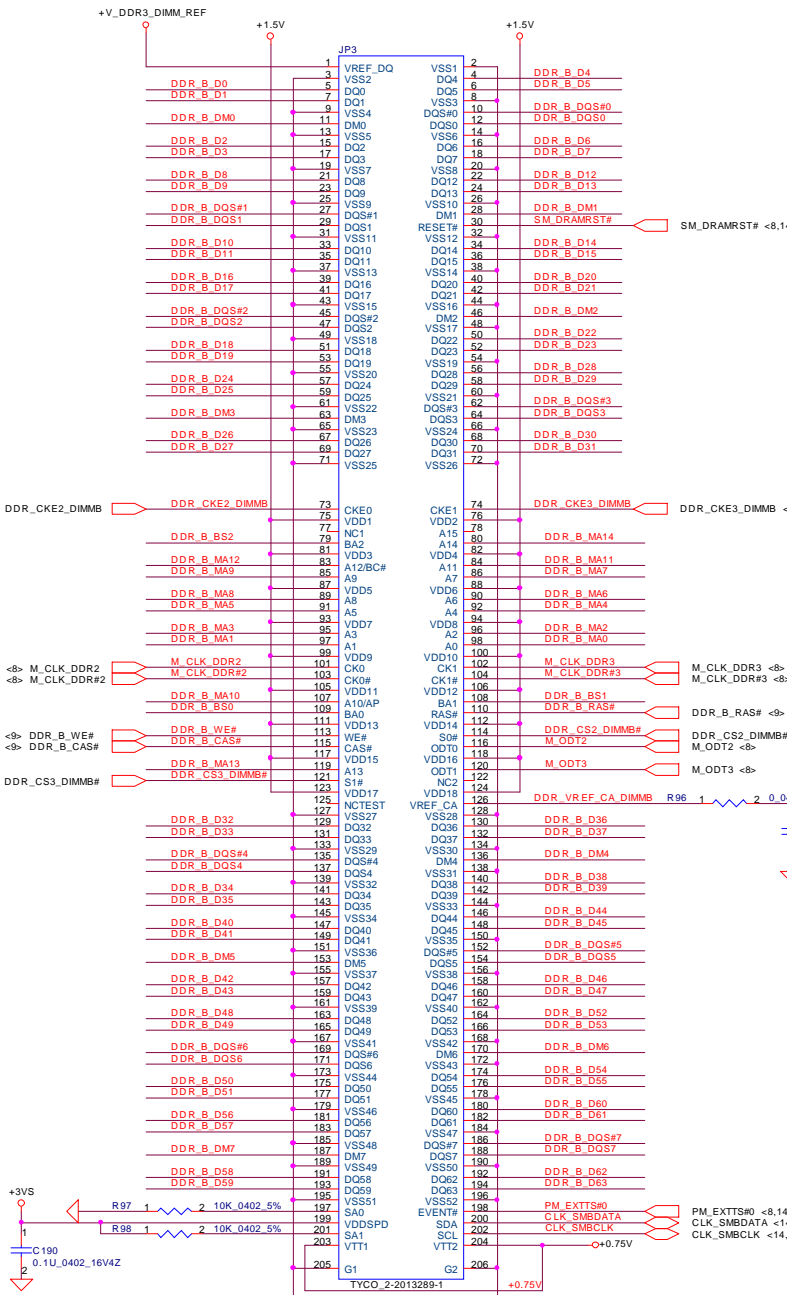


Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

Layout Note: Place near JP5

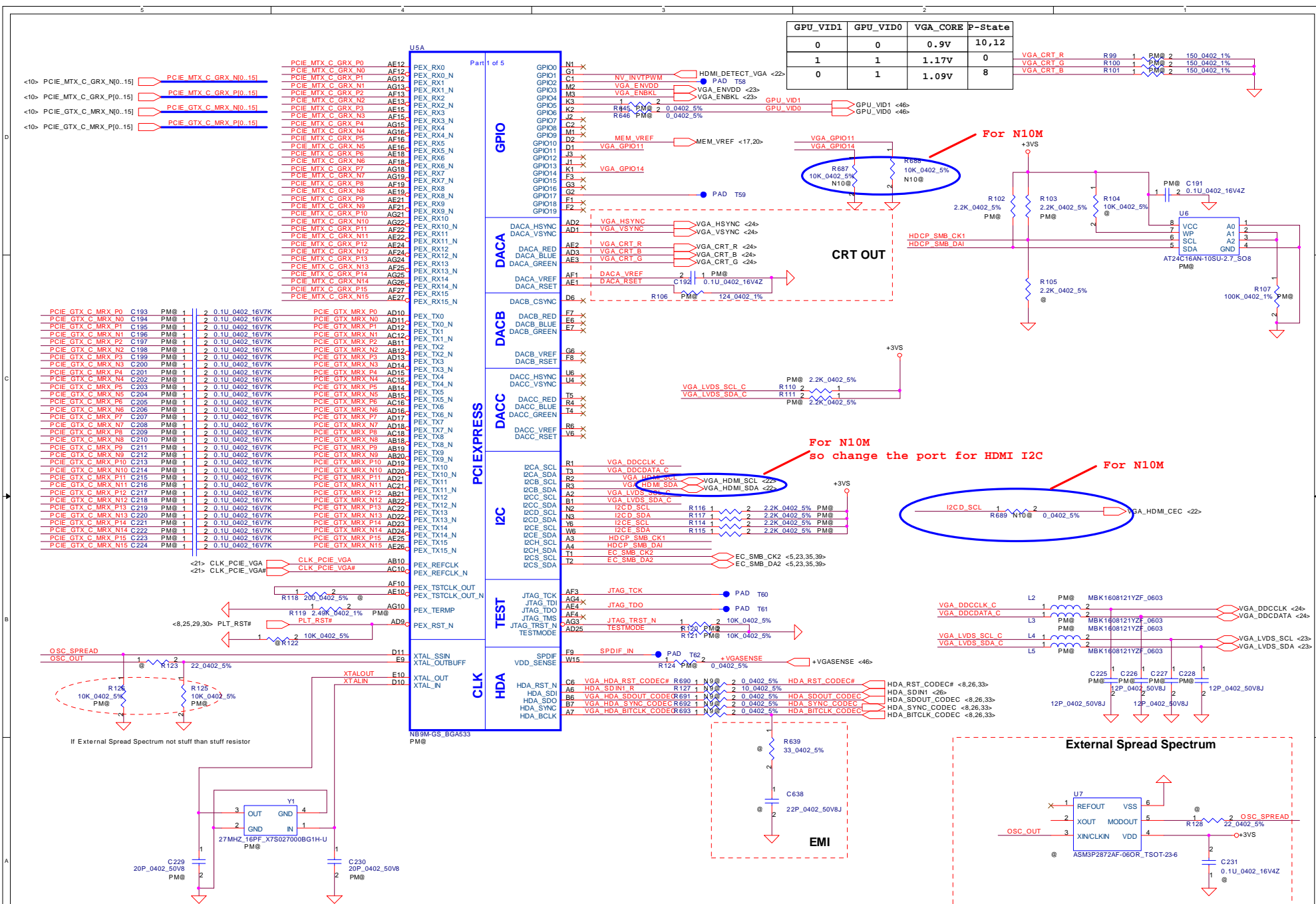


Layout Note: Place near VTT1&VTT2



DDR3 SO-DIMM B STANDARD

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				Date:	Friday, June 27, 2008
				Sheet	15 of 49



GPU_VID1	GPU_VID0	VGA_CORE	P-State
0	0	0.9v	10,12
1	1	1.17v	0
0	1	1.09v	8

USA

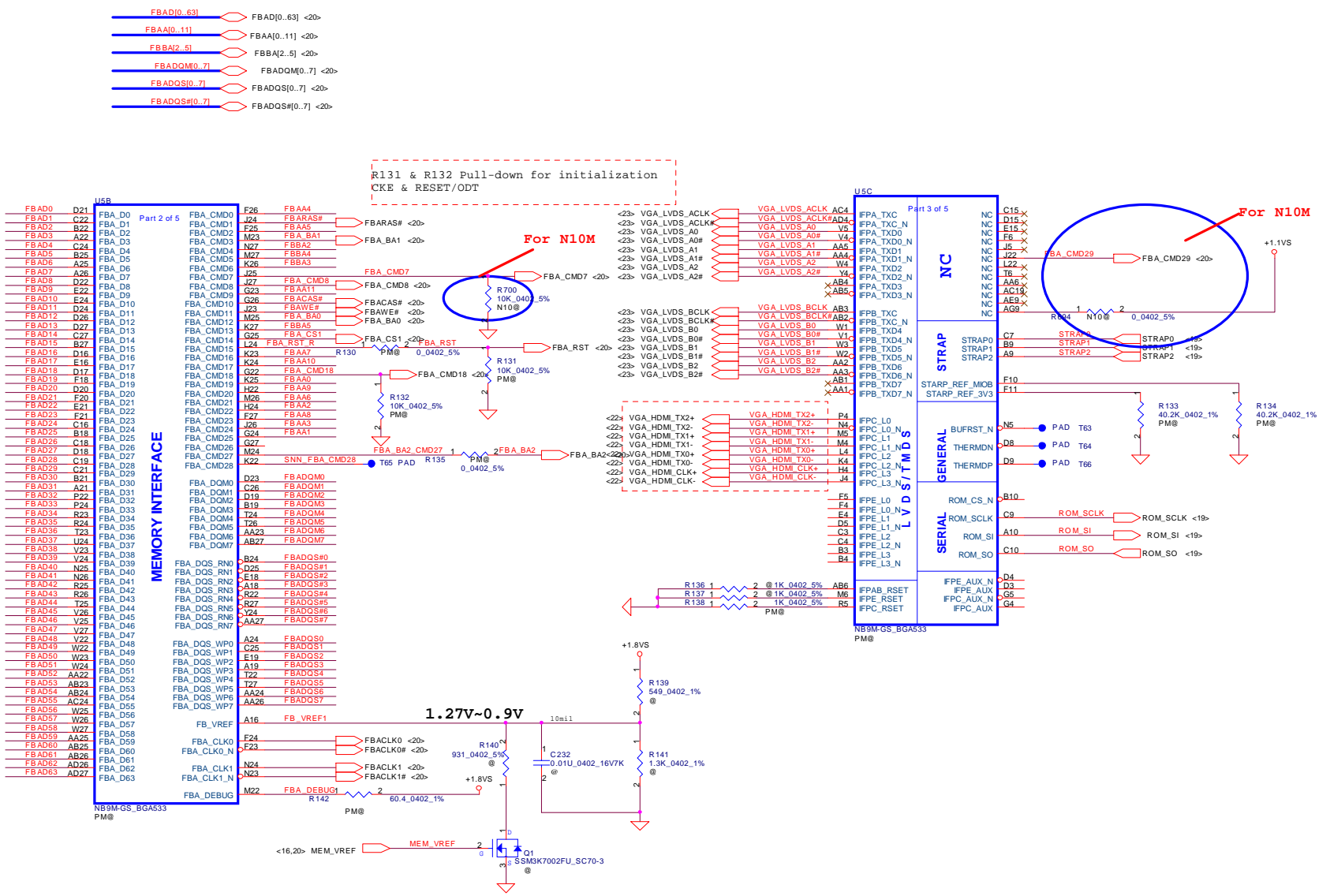
Part 1 of 5

Pin	Signal	Value
AE12	PCIE_MTX_C_GRX_P0	AE12
AF12	PCIE_MTX_C_GRX_N0	AF12
AG12	PCIE_MTX_C_GRX_P1	AG12
AG13	PCIE_MTX_C_GRX_N1	AG13
AF13	PCIE_MTX_C_GRX_P2	AF13
AE13	PCIE_MTX_C_GRX_N2	AE13
AE15	PCIE_MTX_C_GRX_P3	AE15
AF15	PCIE_MTX_C_GRX_N3	AF15
AG15	PCIE_MTX_C_GRX_P4	AG15
AG16	PCIE_MTX_C_GRX_N4	AG16
AF16	PCIE_MTX_C_GRX_P5	AF16
AE16	PCIE_MTX_C_GRX_N5	AE16
AE18	PCIE_MTX_C_GRX_P6	AE18
AF18	PCIE_MTX_C_GRX_N6	AF18
AG18	PCIE_MTX_C_GRX_P7	AG18
AG19	PCIE_MTX_C_GRX_N7	AG19
AE19	PCIE_MTX_C_GRX_P8	AE19
AF19	PCIE_MTX_C_GRX_N8	AF19
AE21	PCIE_MTX_C_GRX_P9	AE21
AF21	PCIE_MTX_C_GRX_N9	AF21
AG21	PCIE_MTX_C_GRX_P10	AG21
AG22	PCIE_MTX_C_GRX_N10	AG22
AF22	PCIE_MTX_C_GRX_P11	AF22
AG24	PCIE_MTX_C_GRX_N11	AG24
AF24	PCIE_MTX_C_GRX_P12	AF24
AG24	PCIE_MTX_C_GRX_N12	AG24
AF25	PCIE_MTX_C_GRX_P13	AF25
AG25	PCIE_MTX_C_GRX_N13	AG25
AG26	PCIE_MTX_C_GRX_P14	AG26
AG26	PCIE_MTX_C_GRX_N14	AG26
AE27	PCIE_MTX_C_GRX_P15	AE27
AE27	PCIE_MTX_C_GRX_N15	AE27

Pin	Signal	Value	Pin	Signal	Value
C193	PCIE_GTX_C_MRX_P0	2 0.1U 0402_16V7K	AD10	PCIE_GTX_MRX_P0	AD10
C194	PCIE_GTX_C_MRX_N0	2 0.1U 0402_16V7K	AD11	PCIE_GTX_MRX_N0	AD11
C195	PCIE_GTX_C_MRX_P1	2 0.1U 0402_16V7K	AD12	PCIE_GTX_MRX_P1	AD12
C196	PCIE_GTX_C_MRX_N1	2 0.1U 0402_16V7K	AD12	PCIE_GTX_MRX_N1	AD12
C197	PCIE_GTX_C_MRX_P2	2 0.1U 0402_16V7K	AG12	PCIE_GTX_MRX_P2	AG12
C198	PCIE_GTX_C_MRX_N2	2 0.1U 0402_16V7K	AG13	PCIE_GTX_MRX_N2	AG13
C199	PCIE_GTX_C_MRX_P3	2 0.1U 0402_16V7K	AD13	PCIE_GTX_MRX_P3	AD13
C200	PCIE_GTX_C_MRX_N3	2 0.1U 0402_16V7K	AD14	PCIE_GTX_MRX_N3	AD14
C201	PCIE_GTX_C_MRX_P4	2 0.1U 0402_16V7K	AD15	PCIE_GTX_MRX_P4	AD15
C202	PCIE_GTX_C_MRX_N4	2 0.1U 0402_16V7K	AC15	PCIE_GTX_MRX_N4	AC15
C203	PCIE_GTX_C_MRX_P5	2 0.1U 0402_16V7K	AD14	PCIE_GTX_MRX_P5	AD14
C204	PCIE_GTX_C_MRX_N5	2 0.1U 0402_16V7K	AD15	PCIE_GTX_MRX_N5	AD15
C205	PCIE_GTX_C_MRX_P6	2 0.1U 0402_16V7K	AC16	PCIE_GTX_MRX_P6	AC16
C206	PCIE_GTX_C_MRX_N6	2 0.1U 0402_16V7K	AD16	PCIE_GTX_MRX_N6	AD16
C207	PCIE_GTX_C_MRX_P7	2 0.1U 0402_16V7K	AD17	PCIE_GTX_MRX_P7	AD17
C208	PCIE_GTX_C_MRX_N7	2 0.1U 0402_16V7K	AD18	PCIE_GTX_MRX_N7	AD18
C209	PCIE_GTX_C_MRX_P8	2 0.1U 0402_16V7K	AC18	PCIE_GTX_MRX_P8	AC18
C210	PCIE_GTX_C_MRX_N8	2 0.1U 0402_16V7K	AD18	PCIE_GTX_MRX_N8	AD18
C211	PCIE_GTX_C_MRX_P9	2 0.1U 0402_16V7K	AD19	PCIE_GTX_MRX_P9	AD19
C212	PCIE_GTX_C_MRX_N9	2 0.1U 0402_16V7K	AD19	PCIE_GTX_MRX_N9	AD19
C213	PCIE_GTX_C_MRX_P10	2 0.1U 0402_16V7K	AD20	PCIE_GTX_MRX_P10	AD20
C214	PCIE_GTX_C_MRX_N10	2 0.1U 0402_16V7K	AD20	PCIE_GTX_MRX_N10	AD20
C215	PCIE_GTX_C_MRX_P11	2 0.1U 0402_16V7K	AD21	PCIE_GTX_MRX_P11	AD21
C216	PCIE_GTX_C_MRX_N11	2 0.1U 0402_16V7K	AC21	PCIE_GTX_MRX_N11	AC21
C217	PCIE_GTX_C_MRX_P12	2 0.1U 0402_16V7K	AD21	PCIE_GTX_MRX_P12	AD21
C218	PCIE_GTX_C_MRX_N12	2 0.1U 0402_16V7K	AD22	PCIE_GTX_MRX_N12	AD22
C219	PCIE_GTX_C_MRX_P13	2 0.1U 0402_16V7K	AC22	PCIE_GTX_MRX_P13	AC22
C220	PCIE_GTX_C_MRX_N13	2 0.1U 0402_16V7K	AD22	PCIE_GTX_MRX_N13	AD22
C221	PCIE_GTX_C_MRX_P14	2 0.1U 0402_16V7K	AD23	PCIE_GTX_MRX_P14	AD23
C222	PCIE_GTX_C_MRX_N14	2 0.1U 0402_16V7K	AD24	PCIE_GTX_MRX_N14	AD24
C223	PCIE_GTX_C_MRX_P15	2 0.1U 0402_16V7K	AE25	PCIE_GTX_MRX_P15	AE25
C224	PCIE_GTX_C_MRX_N15	2 0.1U 0402_16V7K	AE26	PCIE_GTX_MRX_N15	AE26

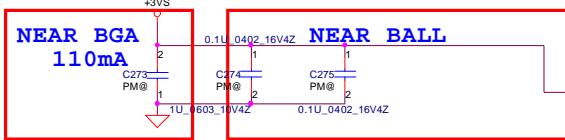
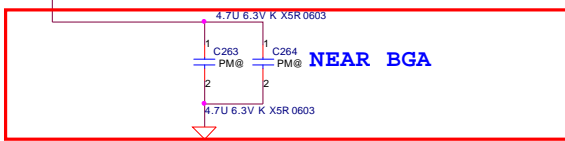
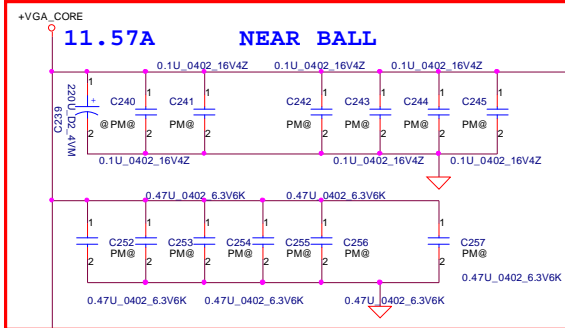
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Size	Document Number	Rev	
B	K1WB3/B4_LA-4551P	0.1	
Date:	Friday, June 27, 2008	Sheet	16 of 48

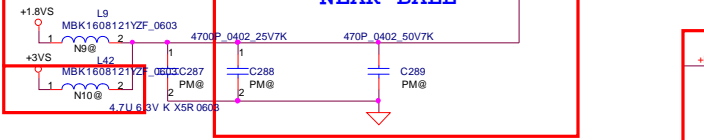
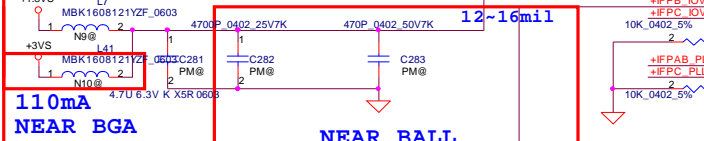


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Date: Friday, June 27, 2008				Sheet 17 of 48			

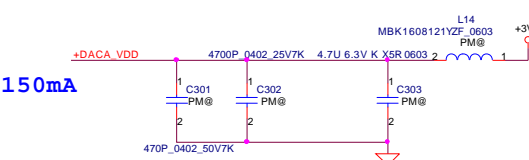
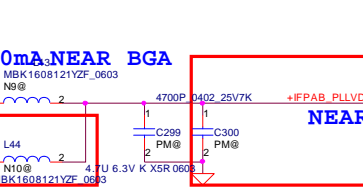
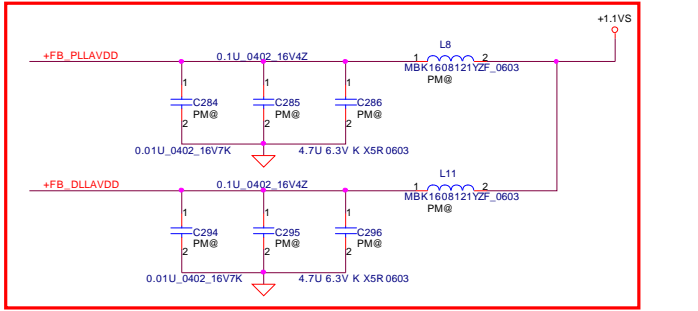
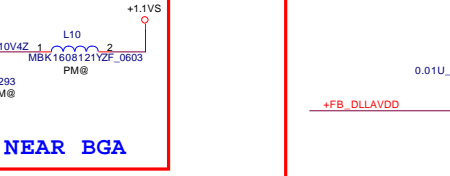
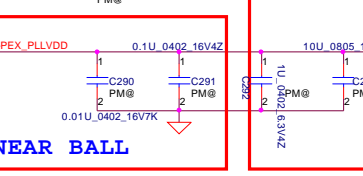
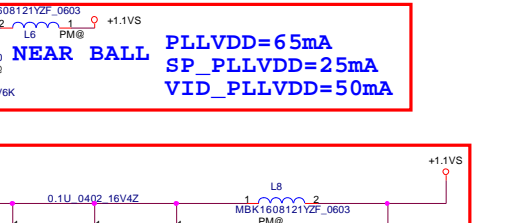
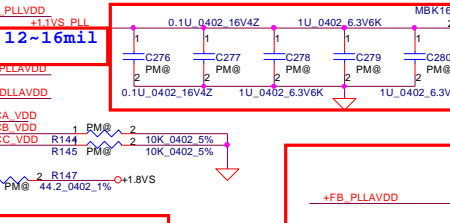
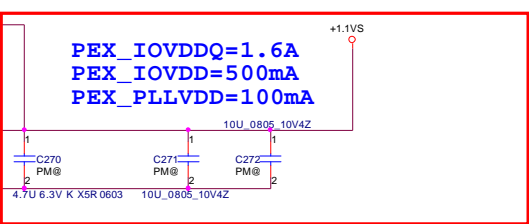
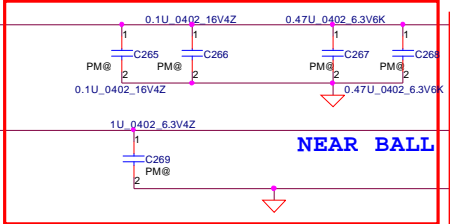
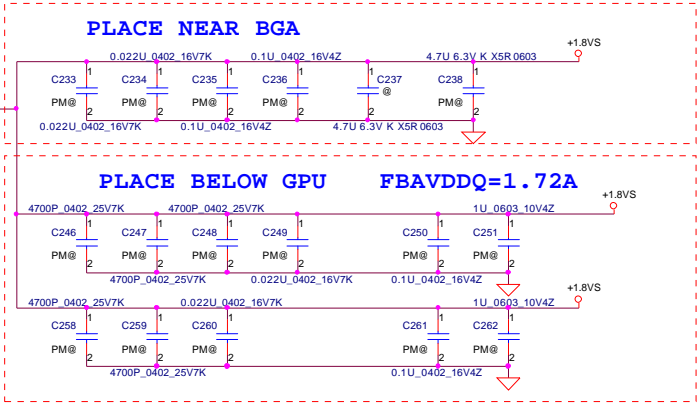
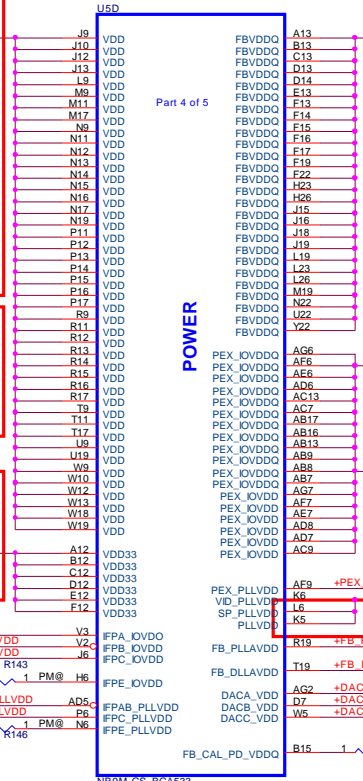
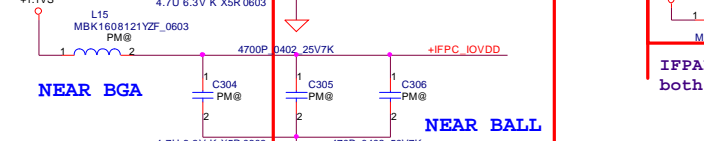
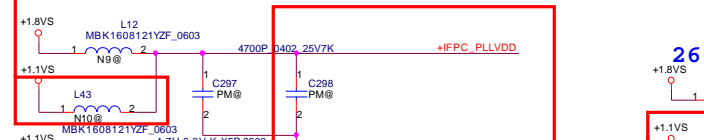
FOR N10M , 1.1VS will changed to 1.05VS



IFPA/B IOVDD: please add option to support both 1.8V(for G9X) and 3.3V(for GT21X)



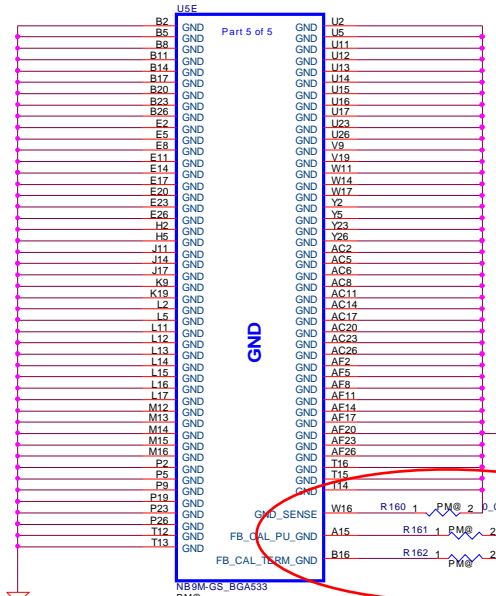
IFPC PLLVDD: please add option to support both 1.8V (for G9X) and 1.05V(for GT21X)



IFPAB PLLVDD: please add option to support both 1.8V(for G9X) and 1.05V(for GT21X)

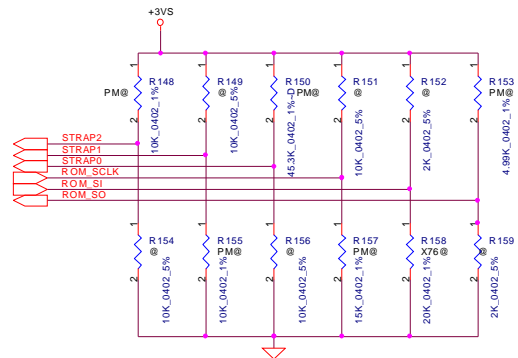
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Date:	Friday, June 27, 2008	Sheet	1 of 49	

A total of 8 signals are required for GBL strapping this includes
 2 reference signals
 6 physical strapping pins
 4 logical strapping bits
 A total of 24 logical strapping bits are available



Memory/PKG	FBCAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
DDR2	30.1ohm	30.1ohm	NC
GDDR3	33.2ohm	44.2ohm	40.2ohm

To update for NV PUN-03304-001_V06 (2008/4/01)



GBL Family GPU Strap Options

GPU	FB Memory (GDDR3)	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
NB9M-GS (0x06E9)	Samsung 16Mx32	PU 5K	PD 15K	PD 20K	PU 10K	PD 10K	PU 45K
	Samsung 32Mx32	PU 5K	PD 15K	PD 45K	PU 10K	PD 10K	PU 45K
Hynix	16Mx32	PU 5K	PD 15K	PD 15K	PU 10K	PD 10K	PU 45K
	32Mx32	PU 5K	PD 15K	PD 35K	PU 10K	PD 10K	PU 45K
Qimonda	16Mx32	PU 5K	PD 15K	PD 10K	PU 10K	PD 10K	PU 45K
	32Mx32	PU 5K	PD 15K	PD 30K	PU 10K	PD 10K	PU 45K

X76

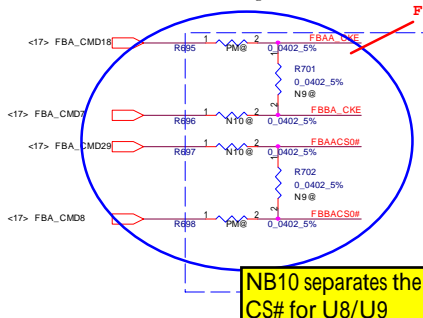
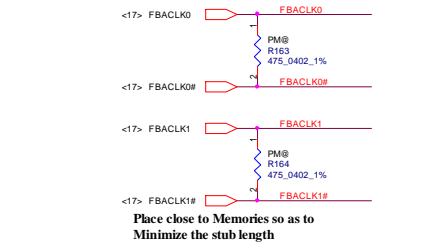
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Issued Date	2007/10/15	Deciphered Date 2008/10/15
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Compal Electronics, Inc.		
NB9M-GE GND & STRAP		
Size B	Document Number KIWB3/B4_LA-451P	Rev 0.1
Date: Friday, June 27, 2008	Sheet 19	of 48

<17> FBAA[0..11] FBAA[0..11]
 <17> FBBA[2..5] FBBA[2..5]
 <17> FBADQM[0..7] FBADQM[0..7]
 <17> FBADQS[0..7] FBADQS[0..7]
 <17> FBADQS[0..7] FBADQS[0..7]
 <17> FBAD[0..63] FBAD[0..63]

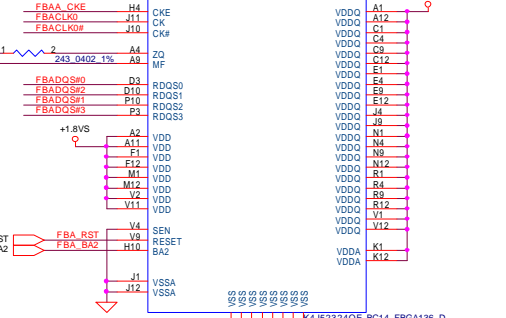
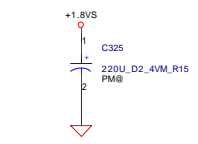
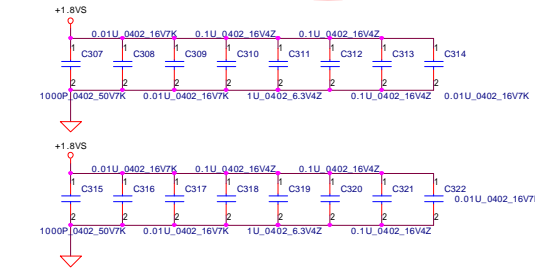
BGA 84 ADR/CMDN MAPPING

Address	0..31	32..63
CMD0	A4	
CMD1	RAS*	RAS*
CMD2	A5	
CMD3	BA1	BA1
CMD4	A2	
CMD5		A4
CMD6		A3
CMD7	CS1*	CS1*
CMD8	CS0*	CS0*
CMD9	A11	A11
CMD10	CAS*	CAS*
CMD11	WE*	WE*
CMD12	BA0	BA0
CMD13	A5	A5
CMD14	A12	A12
CMD15	RST/ODT	RST/ODT
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	CKE
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	
CMD23	A8	A8
CMD24	A3	
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28	RFU0	RFU0
CMD29	RFU1	RFU1
CMD30	RFU2	RFU2

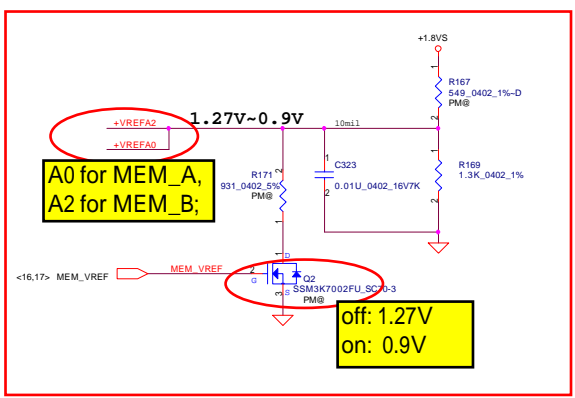


NB10 separates the CKE/CS# for U8/U9

如果用G9X, U8和U9的CKE-->cmd18, CS0-->cmd8
 如果用GT21X, U8的CKE-->cmd18 CS0--> cmd8
 U9的CKE-->cmd7 CS0-->cmd29

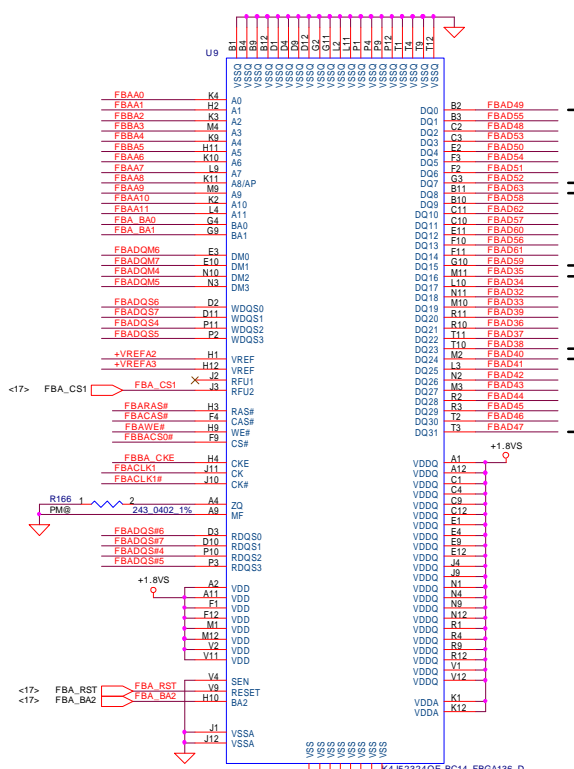


V4:Scan Enable must be to ground

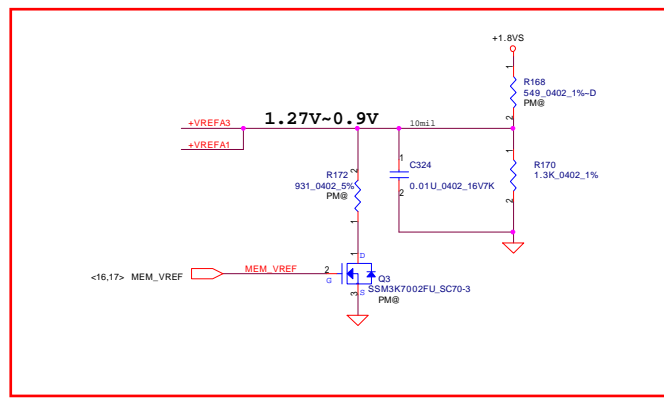


A0 for MEM_A,
A2 for MEM_B;

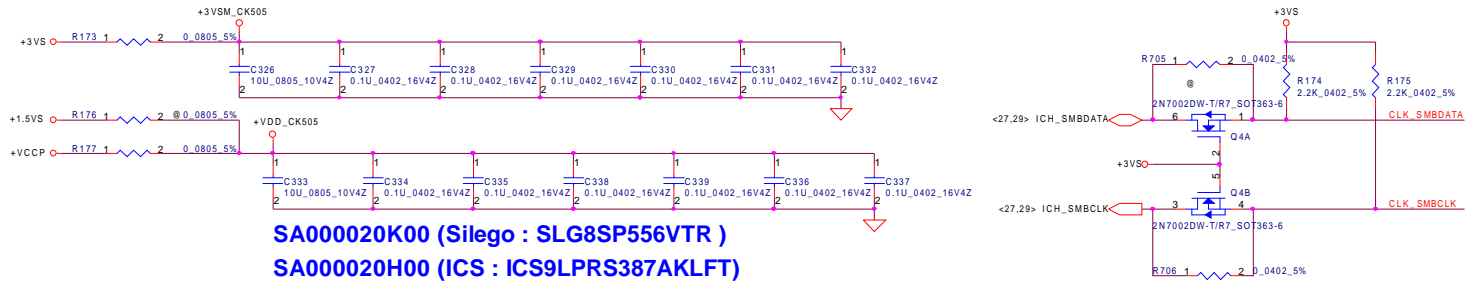
off: 1.27V
on: 0.9V



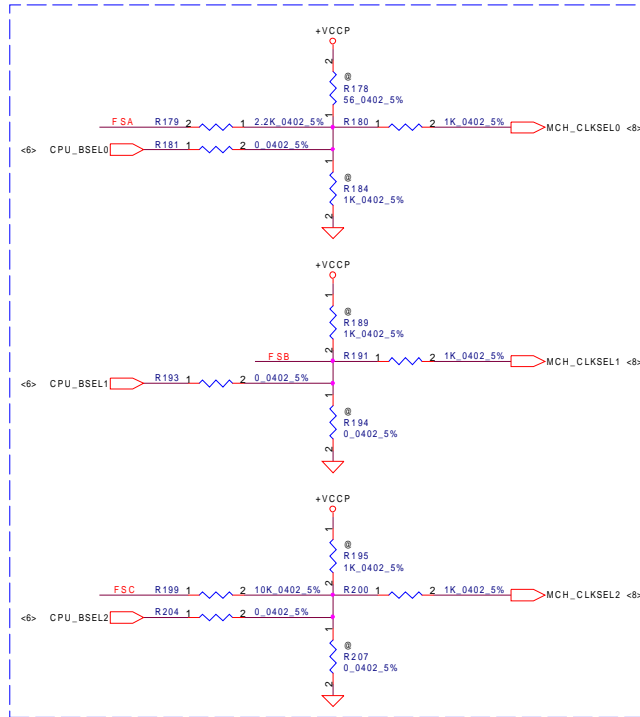
V4:Scan Enable must be to ground



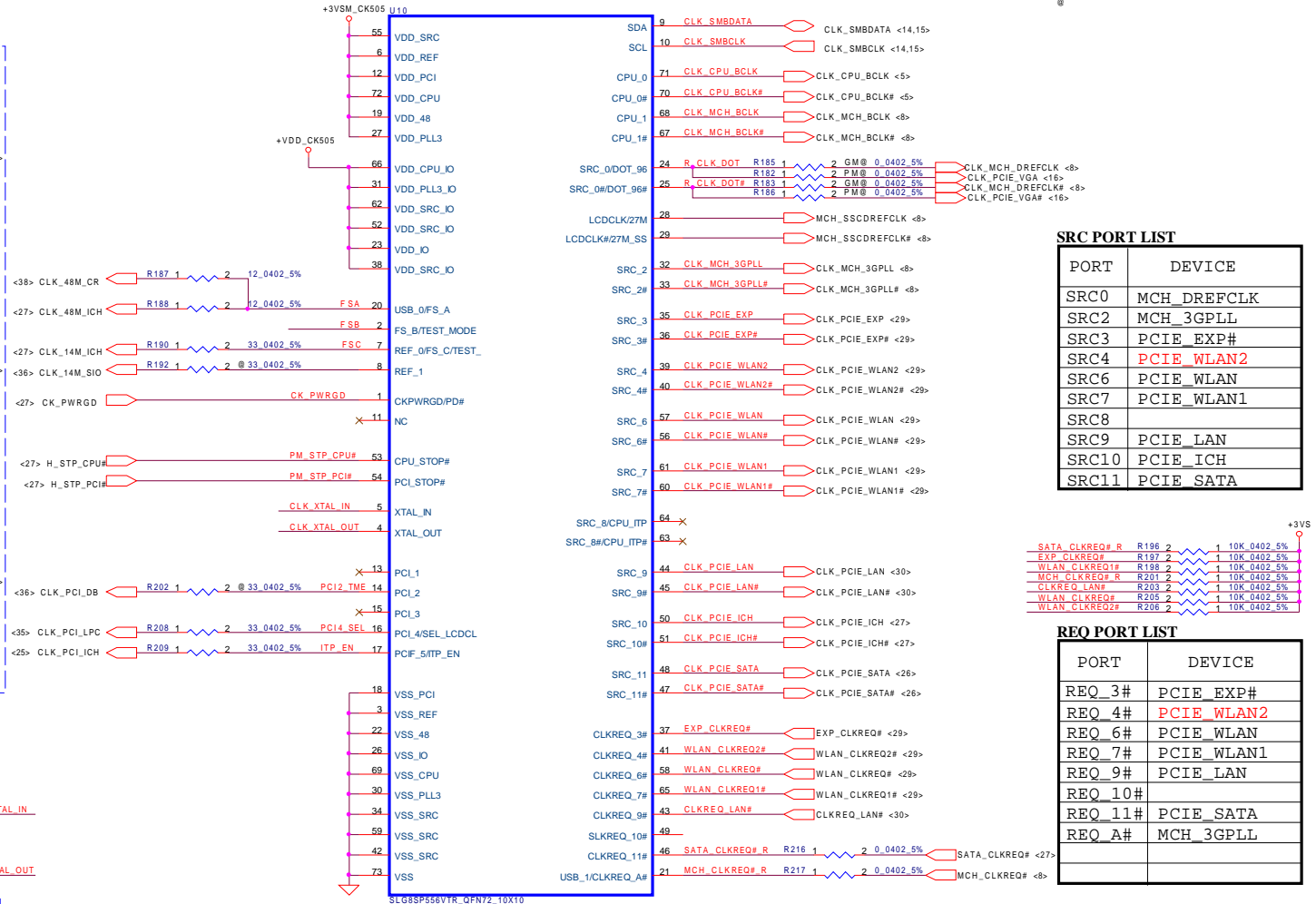
FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB	
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz	
0	0	0	266	100	33.3	14.318	96.0	48.0	
0	0	1	133	100	33.3	14.318	96.0	48.0	
0	1	0	200	100	33.3	14.318	96.0	48.0	
0	1	1	166	100	33.3	14.318	96.0	48.0	
1	0	0	333	100	33.3	14.318	96.0	48.0	
1	0	1	100	100	33.3	14.318	96.0	48.0	
1	1	0	400	100	33.3	14.318	96.0	48.0	
1	1	1	Reserved						



SA00020K00 (Silego : SLG8SP556VTR)
SA00020H00 (ICS : ICS9LPRS387AKLFT)



Routing the trace at least 10mil



SRC PORT LIST

PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	MCH_3GPLL
SRC3	PCIE_EXP#
SRC4	PCIE_WLAN2
SRC6	PCIE_WLAN
SRC7	PCIE_WLAN1
SRC8	PCIE_LAN
SRC9	PCIE_LAN
SRC10	PCIE_ICH
SRC11	PCIE_SATA

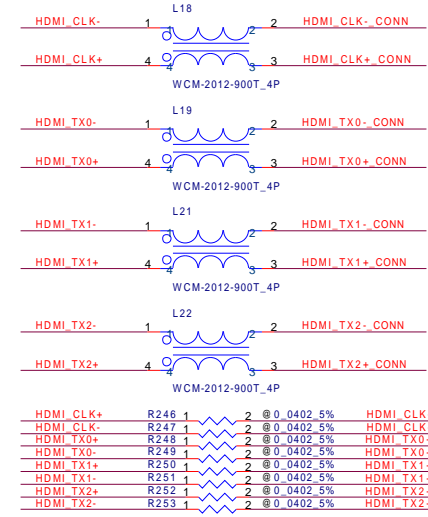
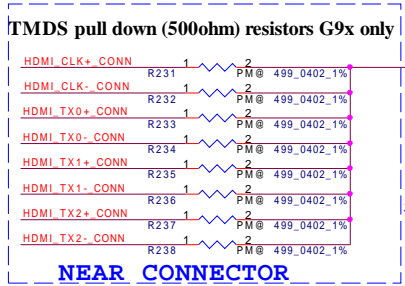
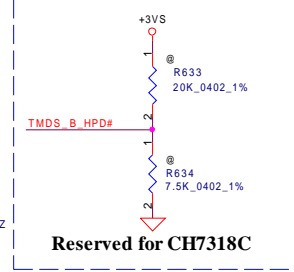
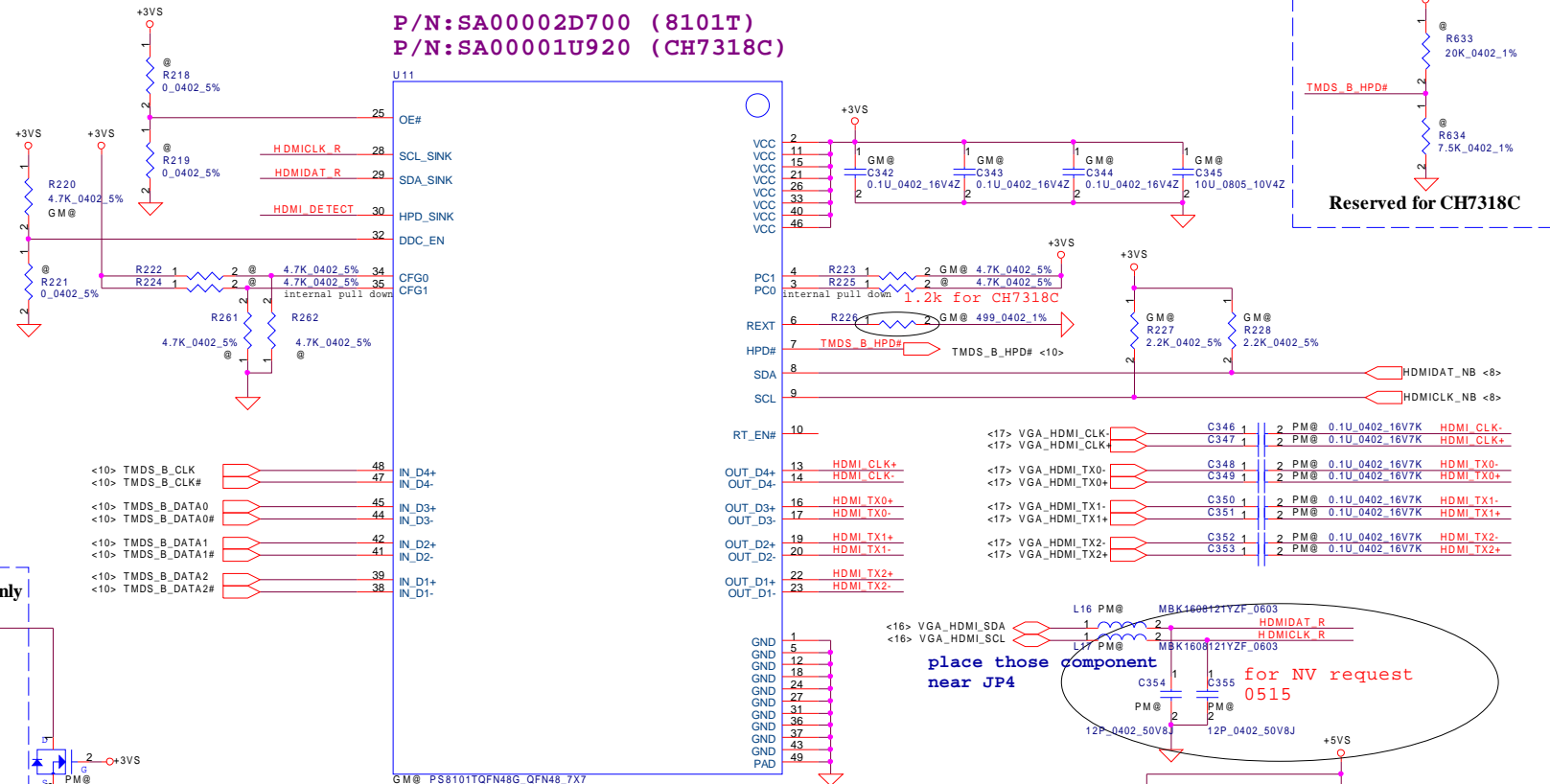
REQ PORT LIST

PORT	DEVICE
REQ_3#	PCIE_EXP#
REQ_4#	PCIE_WLAN2
REQ_6#	PCIE_WLAN
REQ_7#	PCIE_WLAN1
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	PCIE_SATA
REQ_A#	MCH_3GPLL

For ITP_EN, 0 = SRC8/SRC8#; 1 = ITP/ITP#
For PCI4_SEL, 0 = pin24/25 : DOT96 / DOT96#
Pin28/29 : LCDCLK / LCDCLK#
1 = Pin24/25 : SRC_0 / SRC_0#
Pin28/29 : 27M/27M_SS

Security Classification		Compal Secret Data		Compal Electronics Ltd.	
Issued Date	2008/03/25	Deciphered Date	2008/04/	Title	Clock Generator CK505
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Date:	Friday, June 27, 2008	1	Sheet	21	of 49
				Rev	0.1
				Part No.	KIWB3/B4_LA4551P

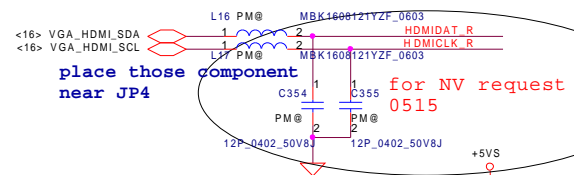
P/N:SA00002D700 (8101T)
P/N:SA00001U920 (CH7318C)



- <10> TMDS_B_CLK 48
- <10> TMDS_B_CLK# 47
- <10> TMDS_B_DATA0 45
- <10> TMDS_B_DATA0# 44
- <10> TMDS_B_DATA1 42
- <10> TMDS_B_DATA1# 41
- <10> TMDS_B_DATA2 39
- <10> TMDS_B_DATA2# 38

9/14 Modify for UMA used

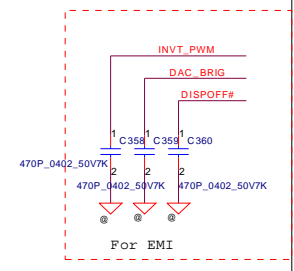
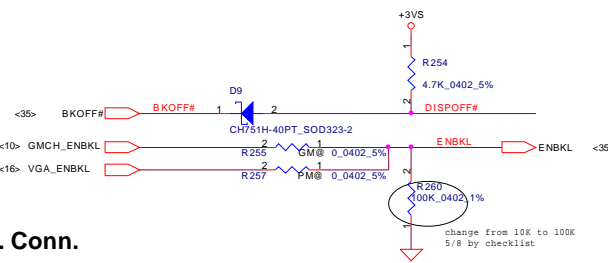
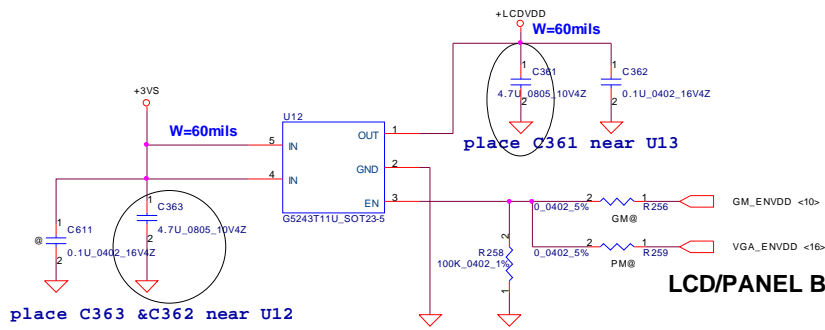
9/14 Reserve for VGA used;check pin name



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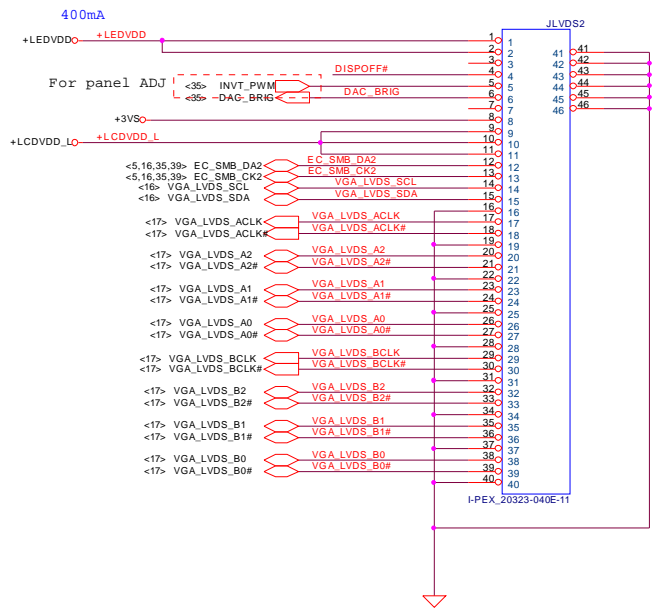
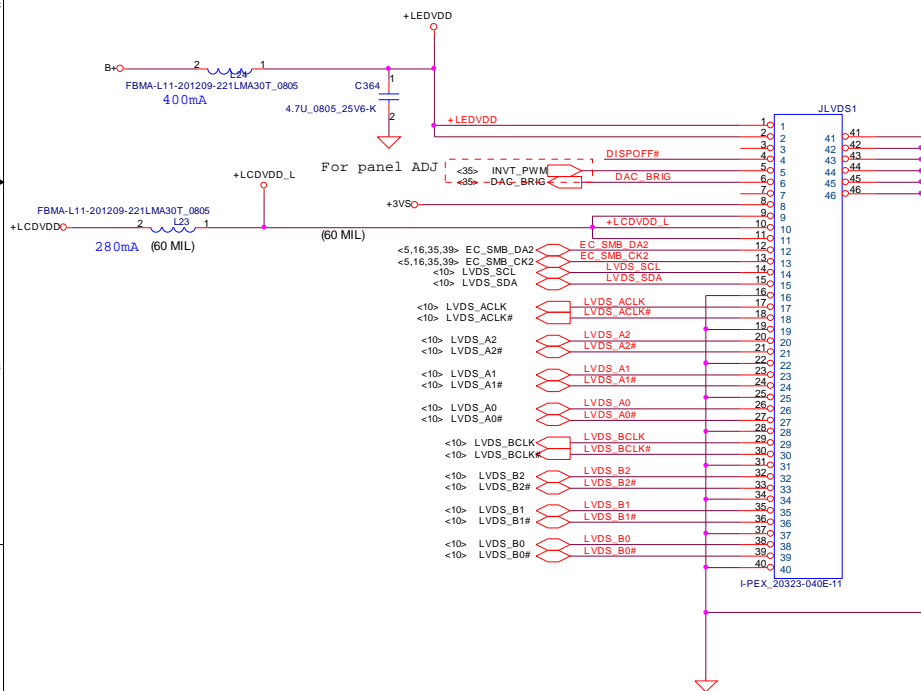
Compal Electronics, Ltd.	
Title	Level Shifter_PS8101T
Size	Document Number
Customer	KIWB3/B4_LA4551P
Date	Friday, June 27, 2008
Sheet	22 of 49
Rev	0.1

LCD POWER CIRCUIT



LCD/PANEL BD. Conn.

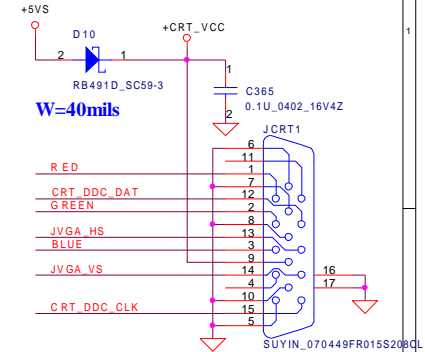
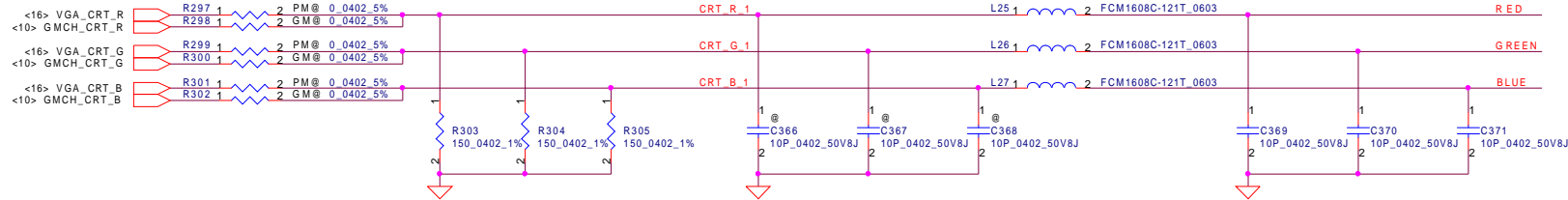
LCD/PANEL BD. Conn.



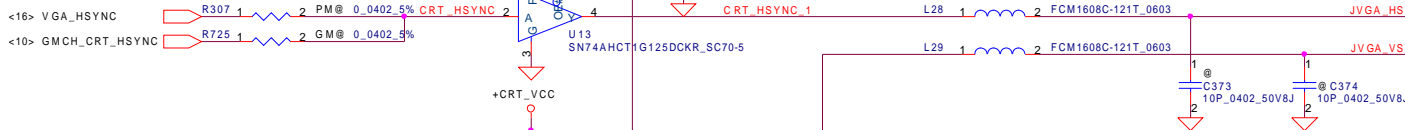
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2007/10/15		2008/10/15		Document Number	
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Date: Friday, June 27, 2008				Rev 0.1	
Sheet 23 of 48					

CRT Connector

CLOSE TO CONN



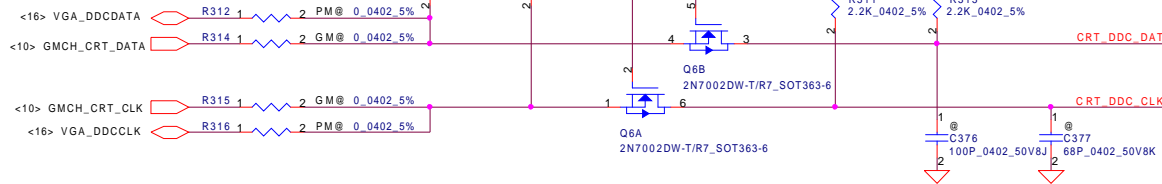
CLOSE TO CONN



CLOSE TO CONN



CLOSE TO CONN

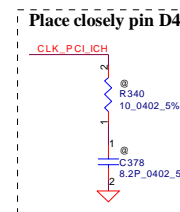
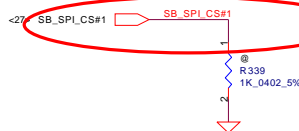
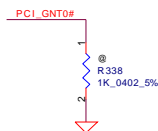
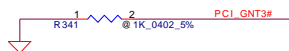
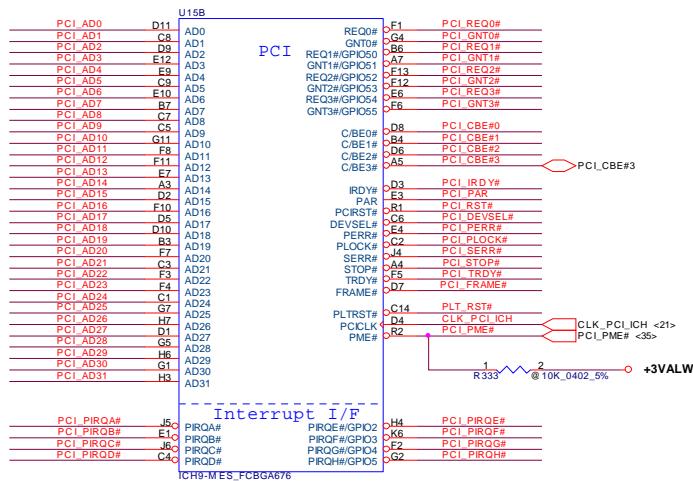
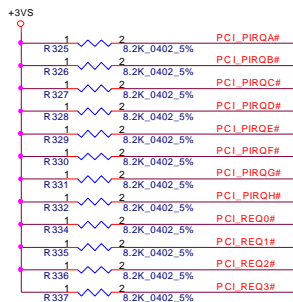
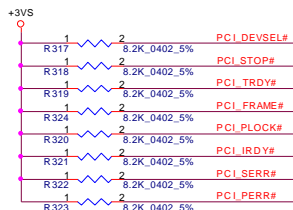


PIN ASSIGNMENT

D-SUB	FUNCTION
9	+CRT_VCC
1	RED
6	GND
2	GREEN
7, 5	GND
3	BLUE
8	GND
14	VSYNC
10	GND
13	HSYNC
11	SENSE
12	SM_DAT
15	SM_CLK
4	PIN4

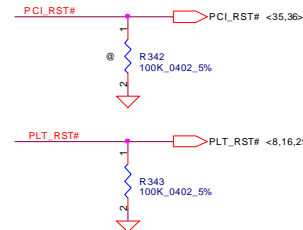
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Size		Custom	
Document Number		JITR1_LA-4141P	
Date:	Friday, June 27, 2008	Sheet	24 of 49
Rev	0.1		



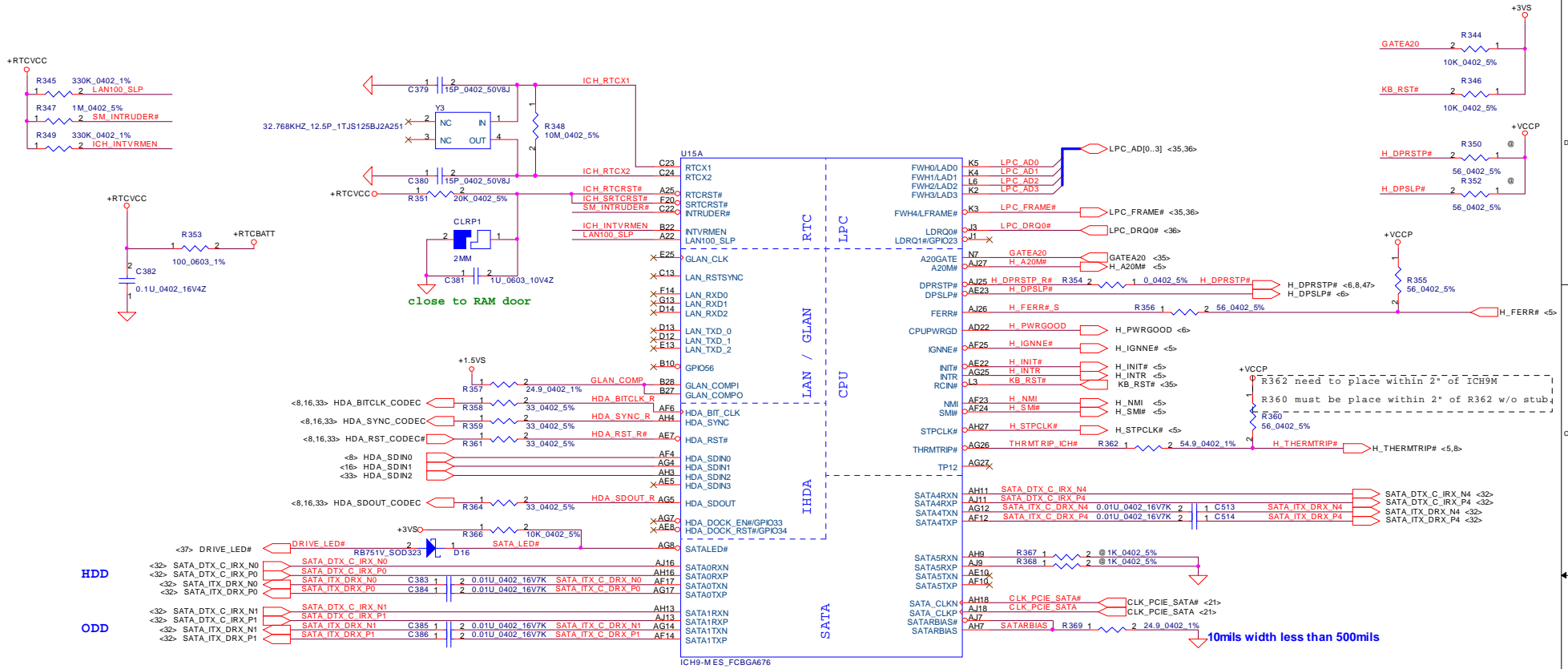
A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction
0	1	SPI
1	0	PCI
1	1	LPC*



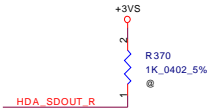
Security Classification	Compal Secret Data	
Issued Date	2007/10/15	Deciphered Date 2008/10/15
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Compal Electronics, Inc.		
Title ICH9M(U4)-PCI		
Size	Document Number	Rev
	JITRI_LA-4141P	0.1
Date:	Friday, June 27, 2008	Sheet 25 of 48

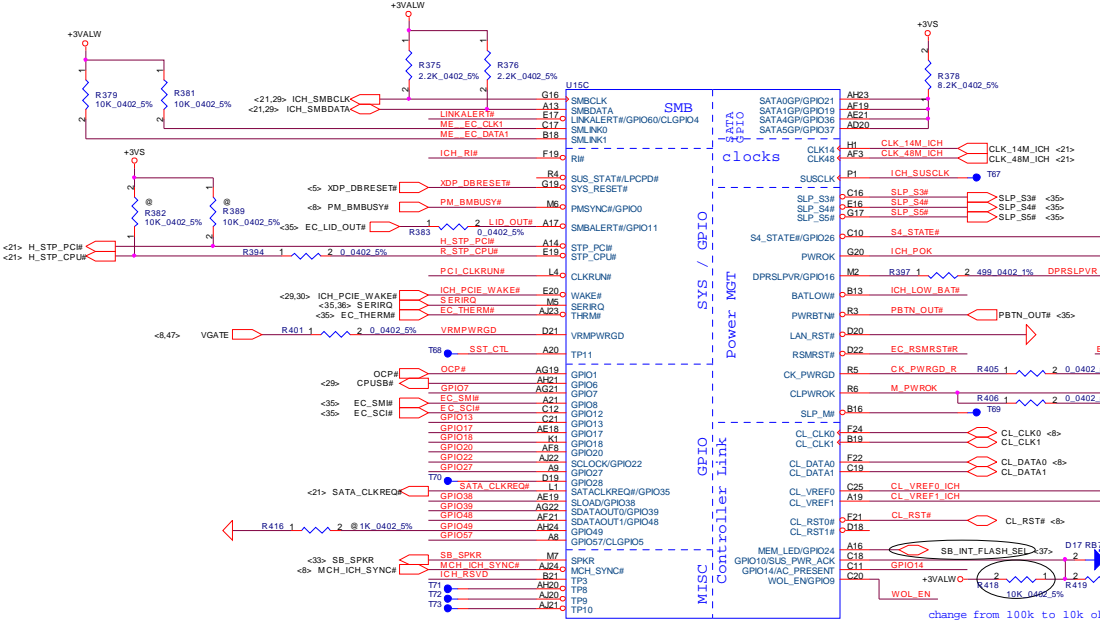
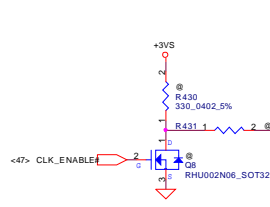
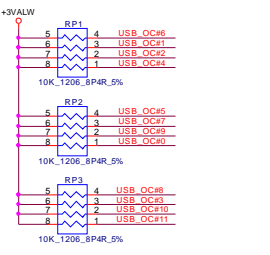
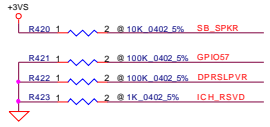
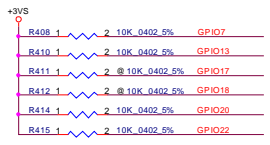
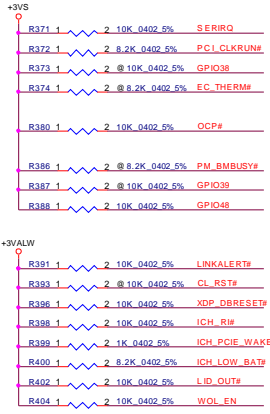


SATA PORT LIST	
PORT	DEVICE
0	HDD
1	
4	ODD
5	E-SATA

Need check

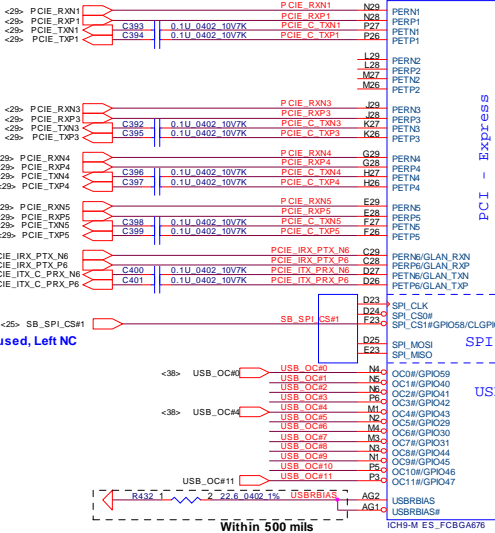


XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1



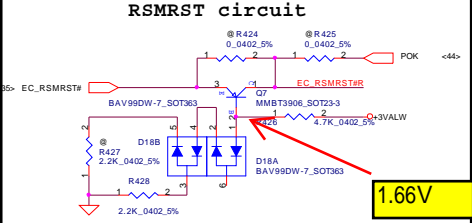
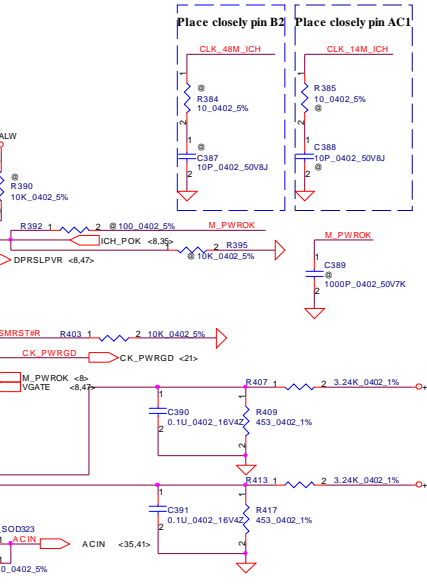
low-->default
High -->no boot

AC decoupling cap range of 75nF to 220nF



SPI not used, Left NC

Within 500 mils



PORT	DEVICE
1	3G
2	WLAN
3	NEW CARD
4	TV TUNER
5	LAN

PORT	DEVICE
0	LEFT SIDE
1	CMOS
2	3G Card
3	RIGHT USB
4	BT Card Reader
5	WLAN
6	TV Tuner
7	New Card
8	
9	
10	
11	

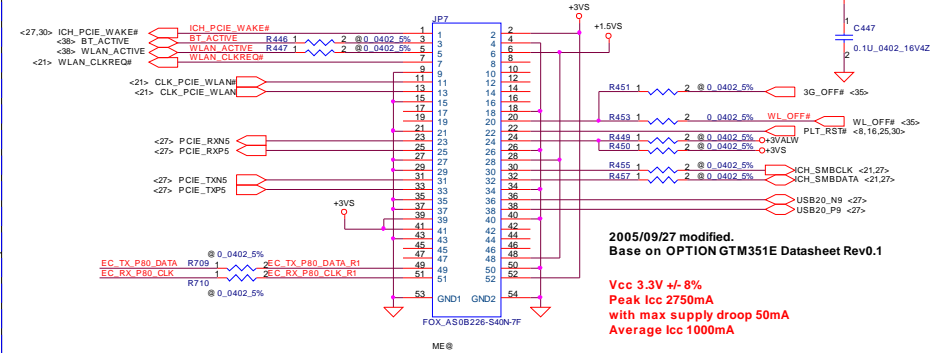
Security Classification	Compal Secret Data
Issued Date	2007/10/15
Deciphered Date	2008/10/15

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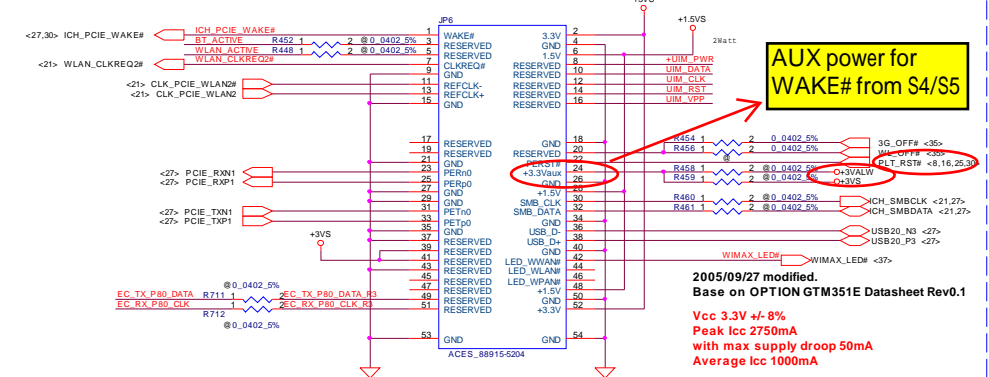
Compal Electronics, Inc.	
Title	
ICH9M(3/4)-USB,GPIO,PCIE	
Size	Document Number
JITRI_LA-4141P	Rev 0.1
Date: Friday, June 27, 2008	Sheet 27 of 49

Mini-Express Card for 3G Or TV Tuner Mini-Express Card for WLAN

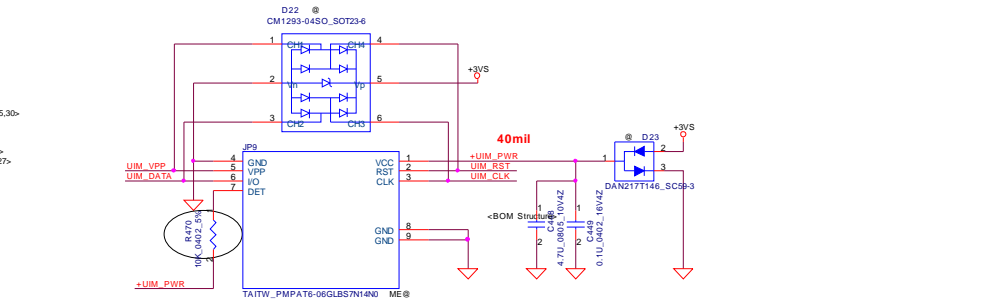
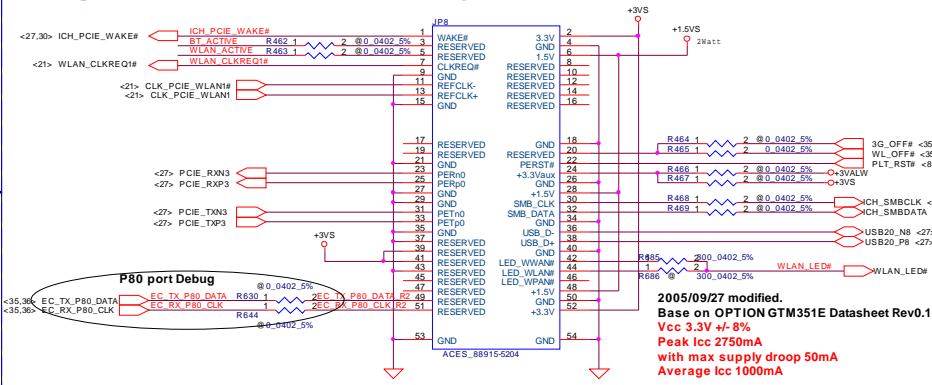
Mini-Express Card(Slot 1-TV TUNNER) 4.0mm high



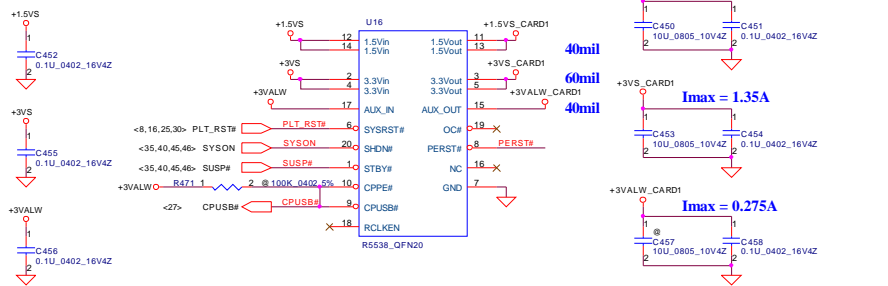
Mini-Express Card(Slot 3-WWAN 3G) 5.2mm high



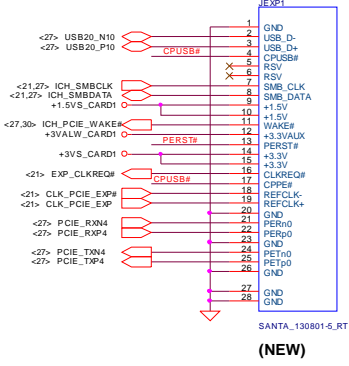
Mini-Express Card(Slot 2-WIRELESS) 5.2mm high



Express Card Power Switch

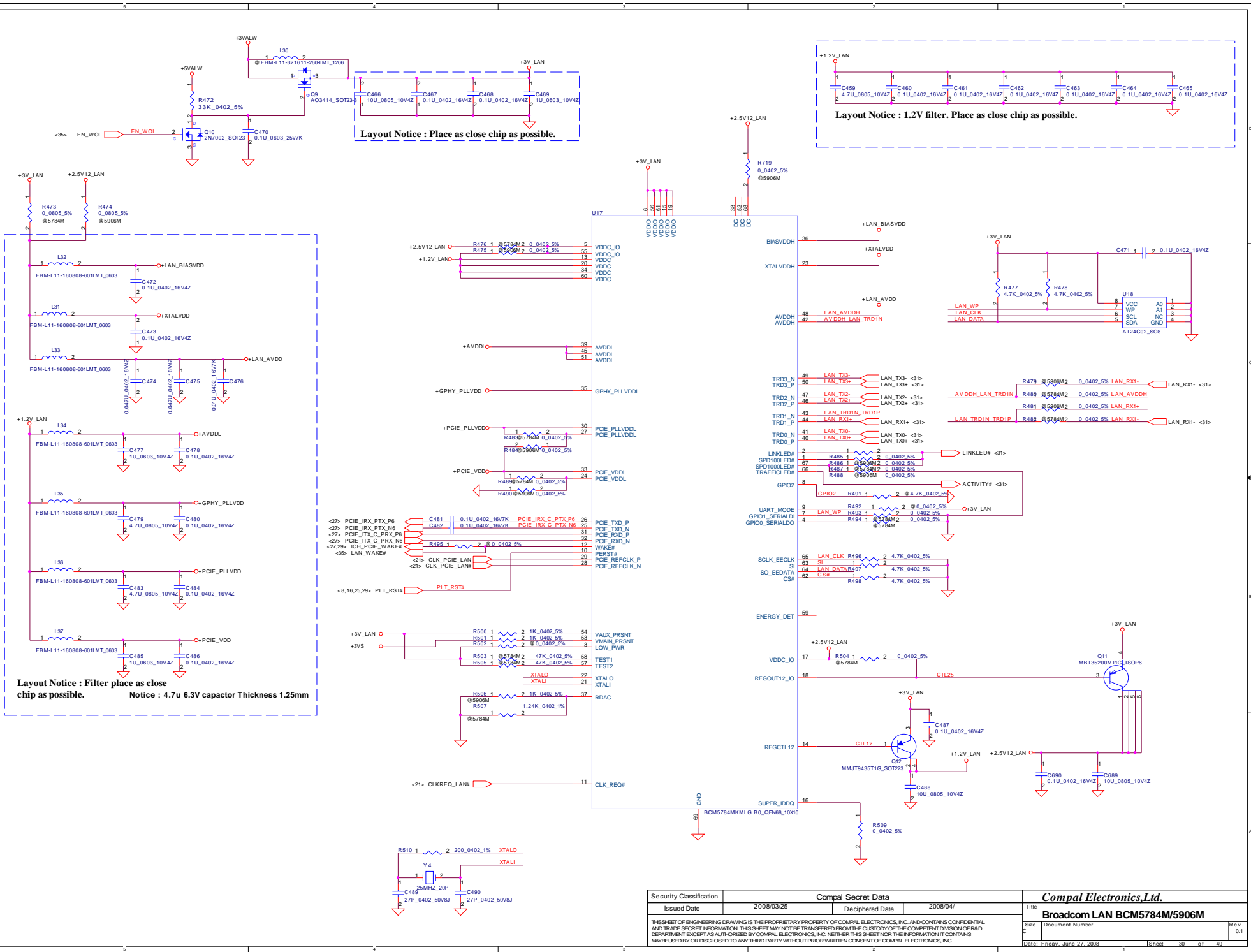


New Card 34mm Socket (Left/TOP)



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Compaq Electronics, Inc.	
Mini-Card/3G/FeliCa/BT	
Size	Document Number
	J1TR1_LA-414P
Date:	Friday, June 27, 2008
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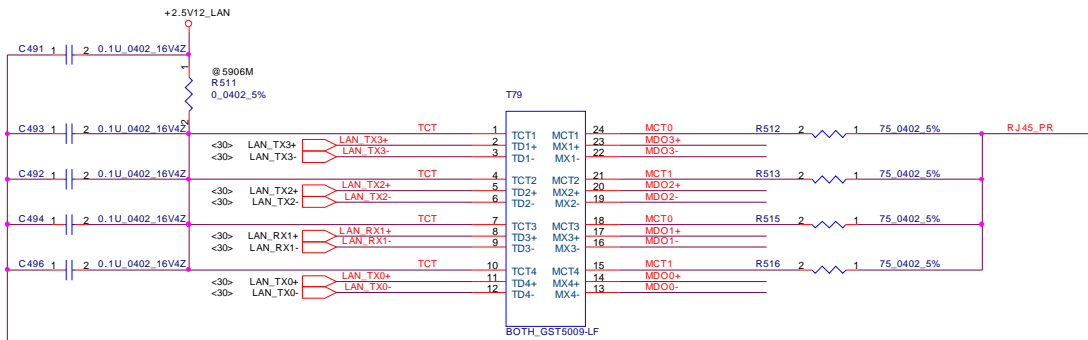


Layout Notice : Place as close chip as possible.

Layout Notice : 1.2V filter. Place as close chip as possible.

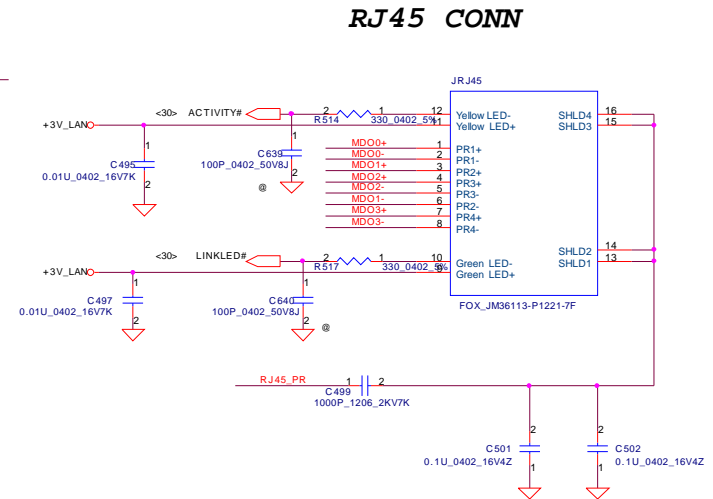
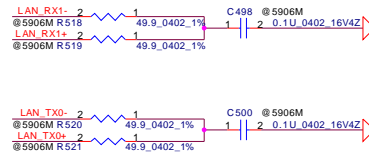
Layout Notice : Filter place as close chip as possible. Notice : 4.7u 6.3V capacitor Thickness 1.25mm

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Issued Date	2008/03/25	Deciphered Date	2008/04/	Title	Broadcom LAN BCM5784M/5906M
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Date:	Friday, June 27, 2008	Sheet	30 of 49	Rev	0.1

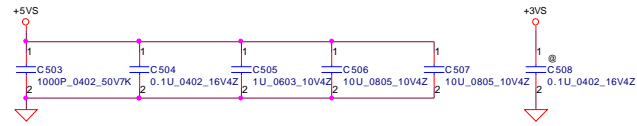


Change C468,C470,C473,C474,C475,C476 from 0.01uF to 0.1uF

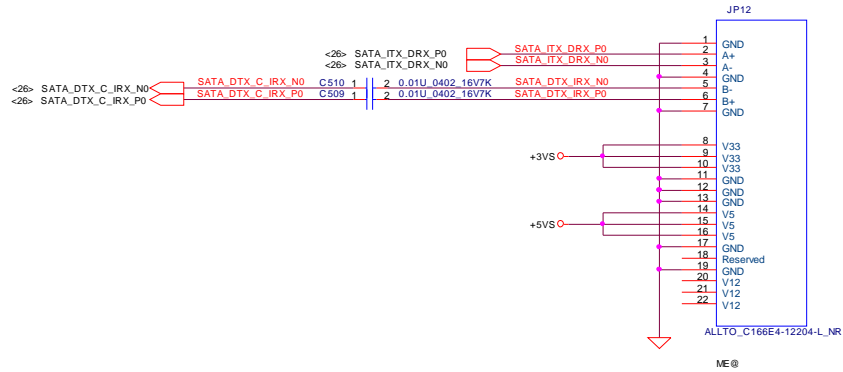
near LAN controller



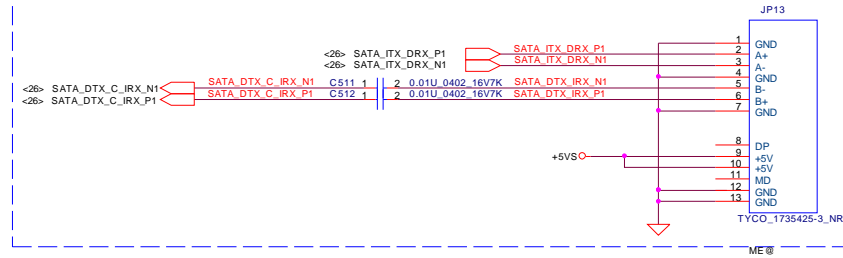
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title
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Size	Document Number	JITR1_LA-4141P		Rev
Custom				0.1
Date:	Friday, June 27, 2008	Sheet	31	of 48



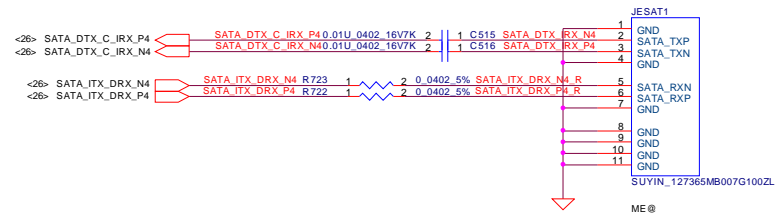
SATA HDD Conn.



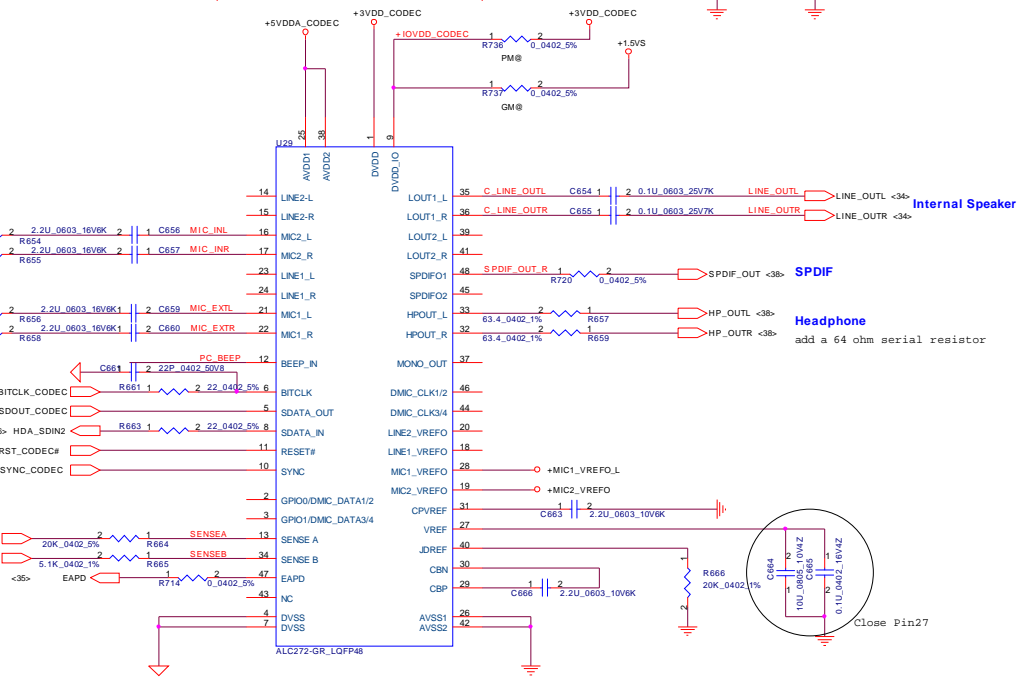
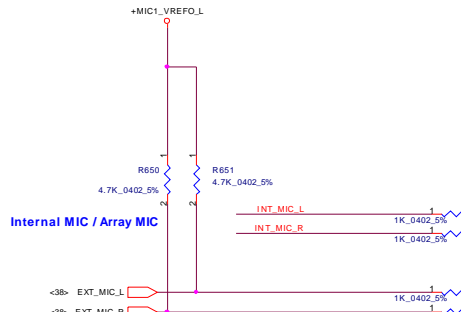
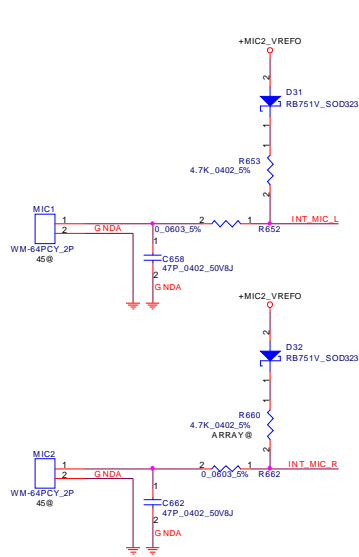
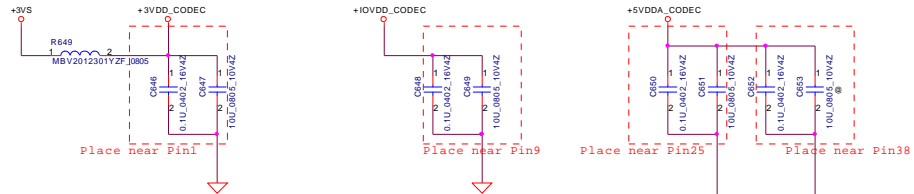
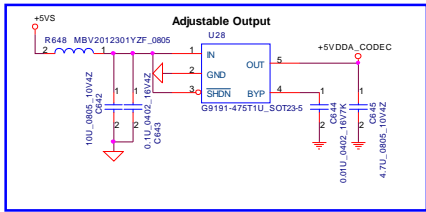
SATA ODD Conn.



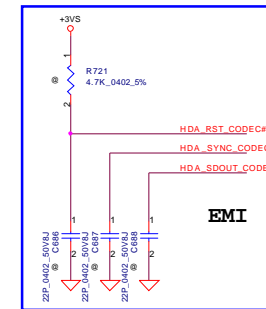
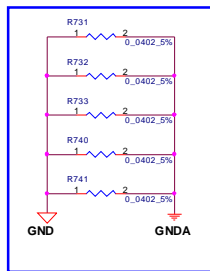
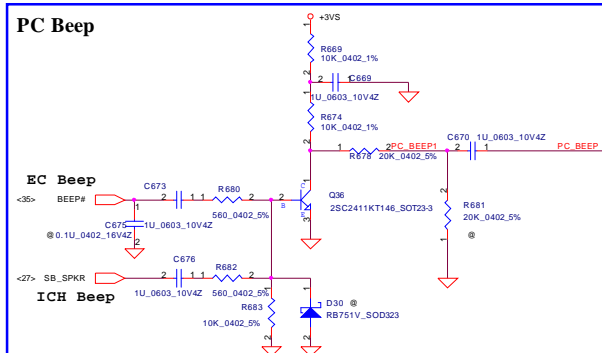
**E-SATA Conn.
place R722&R723&C515&C516
near JESAT1**



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Size	Document Number			Rev	
B	JITRI_LA-4141P			0.1	
Date:	Friday, June 27, 2008	Sheet	32	of	48



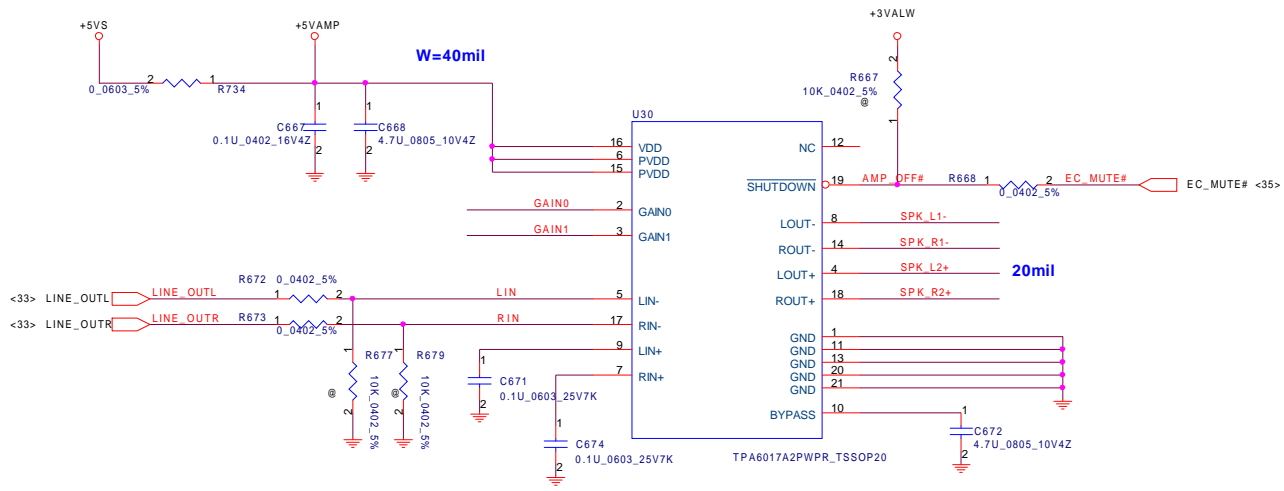
Pin Assignment	Location	Function
LINE-OUT (Pin35/36)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
LINE1 (Pin23/24)	External	Line in
MIC1 (Pin21/22)	External	Mic in
MONO-OUT (Pin37)	Internal	Internal Subwoofer
MIC2 (Pin16/17)	Internal	Internal Mic



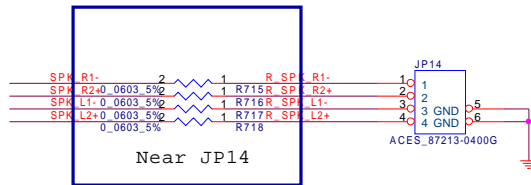
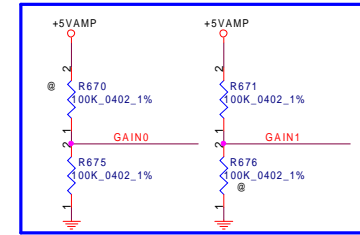
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Issued Date	2008/03/25	Deciphered Date 2008/04/
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Compaq Electronics Ltd.	
Title	HD Audio Codec ALC272
Size	Document Number
Date	Friday, June 27, 2008
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Rev	0.1
KWIB3/B4_LA4551P	

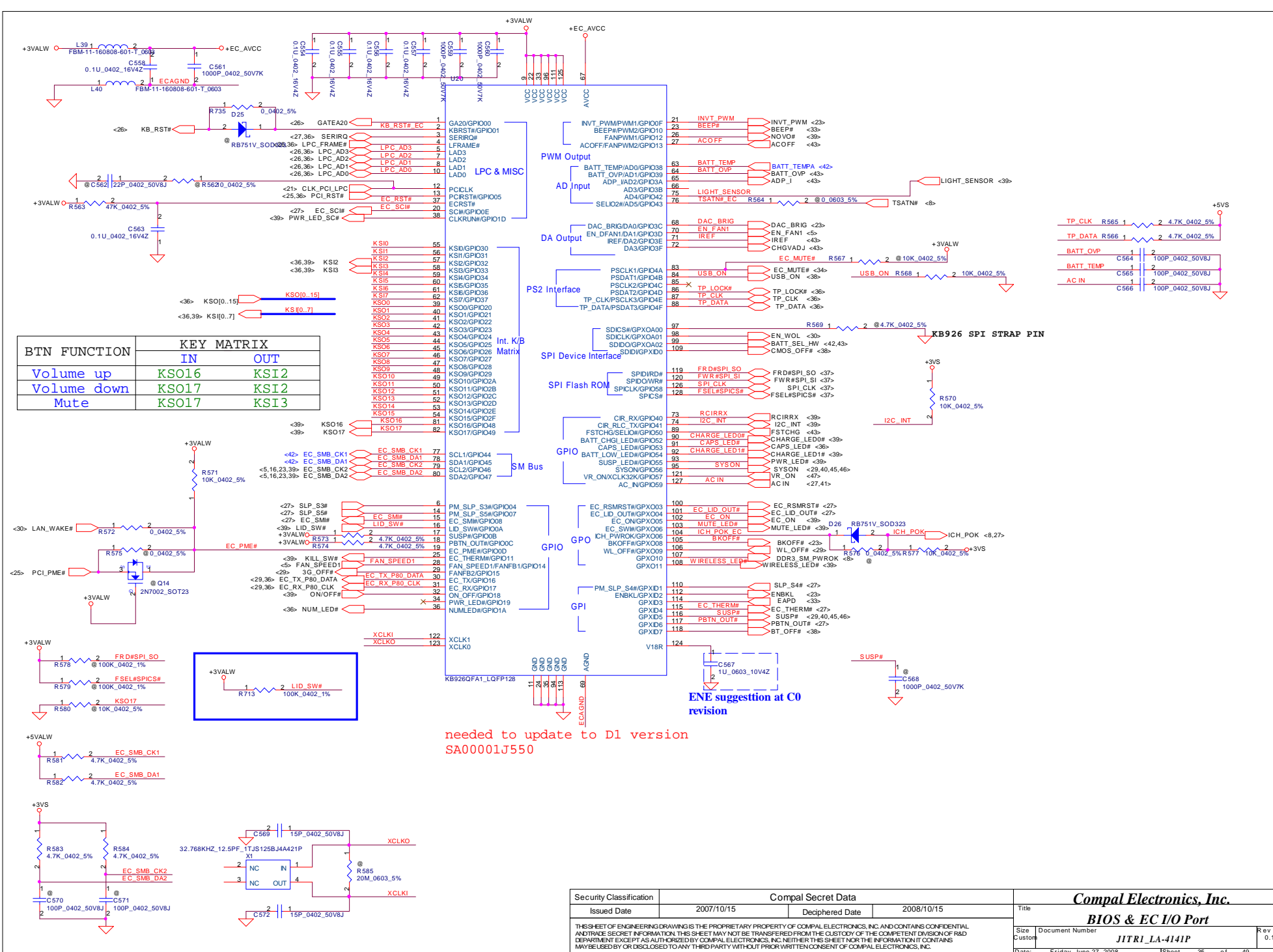
Speaker Connector



GAIN0	GAIN1	
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



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				Customer	KIWB3/B4_LA4551P
				Date	Friday, June 27, 2008
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				Rev	0.1

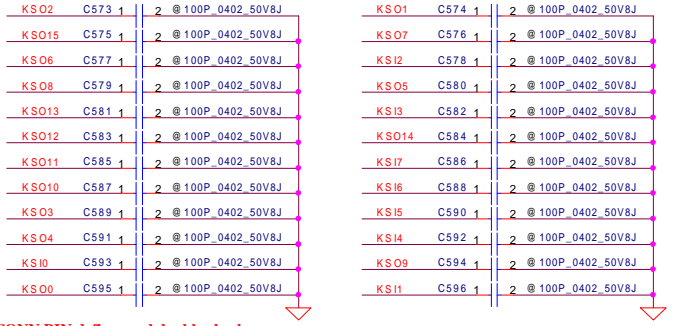
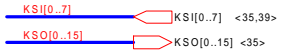


needed to update to D1 version SA00001J550

ENE suggestion at C0 revision

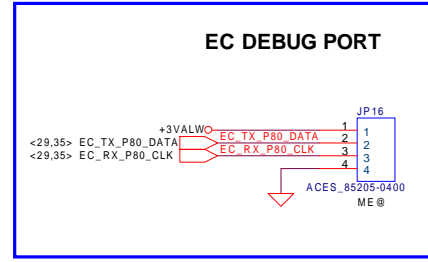
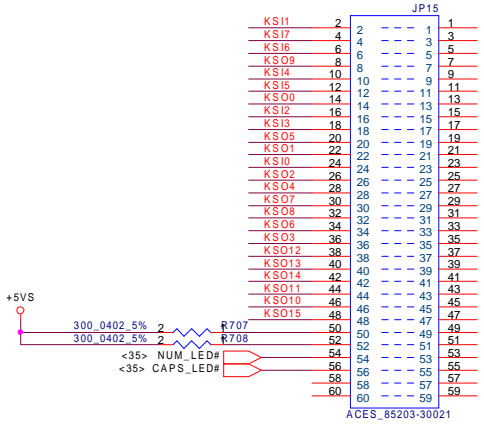
Security Classification	Compal Secret Data		Title
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Date:	Friday, June 27, 2008	Sheet	35 of 49

INT_KBD Conn.

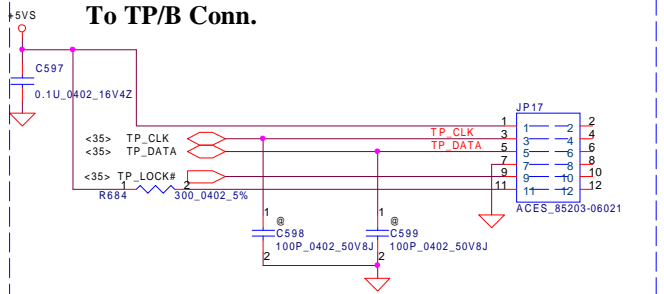


CONN PIN define need double check

Source:SP01000IE00
2nd source:SP01000IF00
30 pin

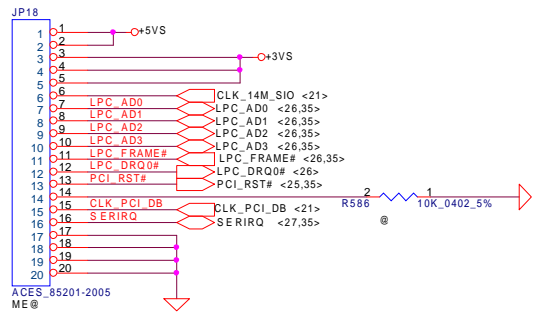


To TP/B Conn.



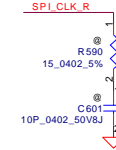
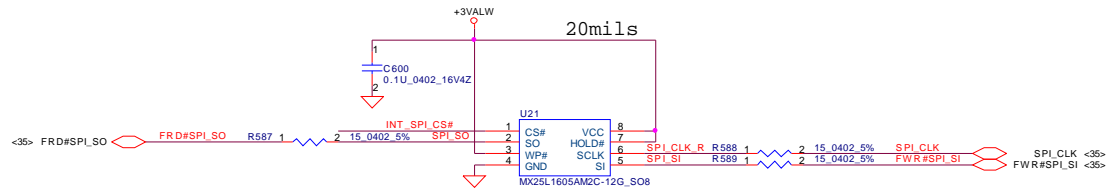
CONN PIN define need double check

FOR LPC SIO DEBUG PORT

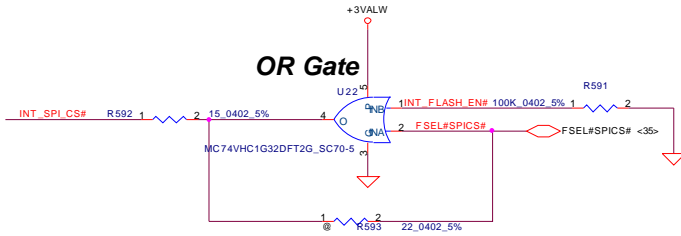


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Size	Document Number	JITRI_LA-4141P		Rev	0.1
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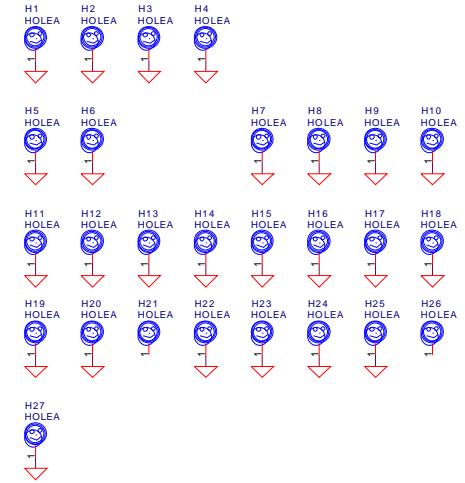
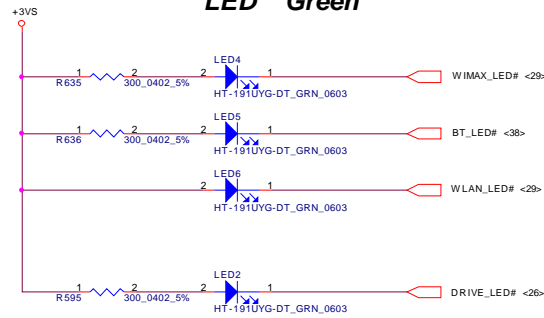
FOR EC 16M SPI ROM



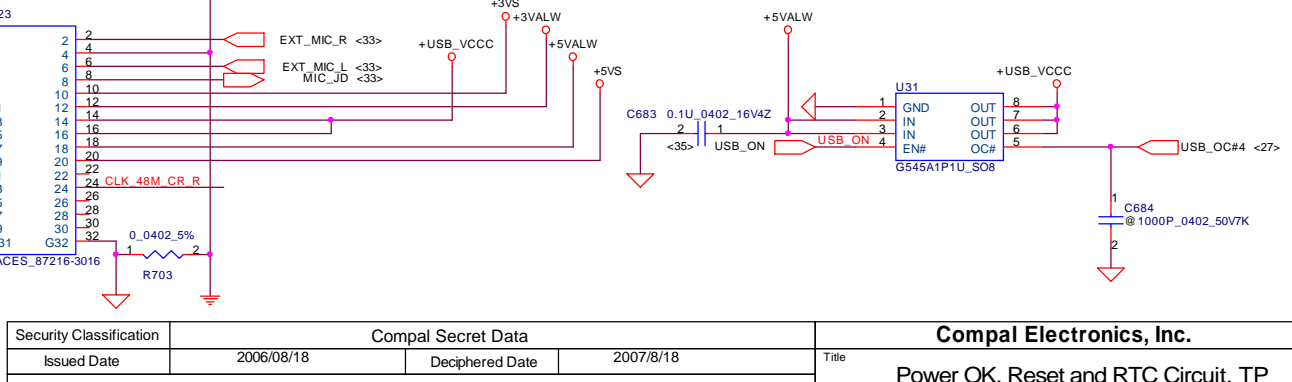
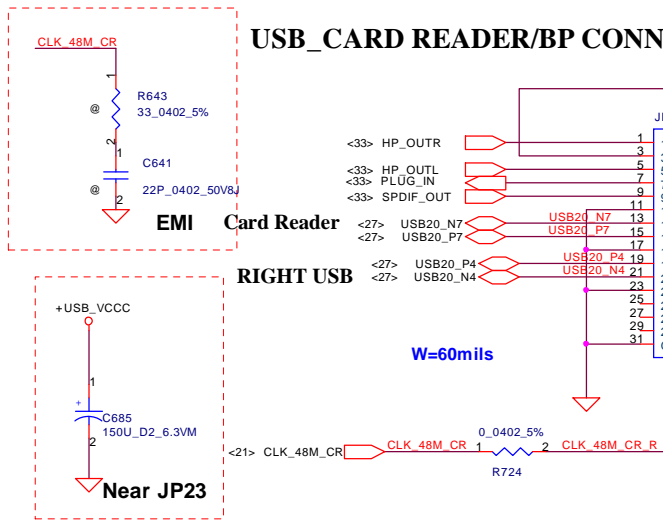
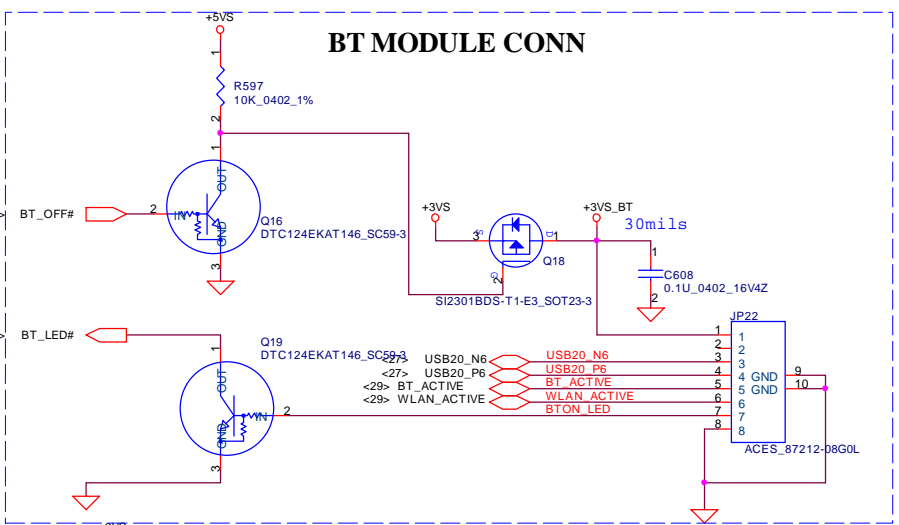
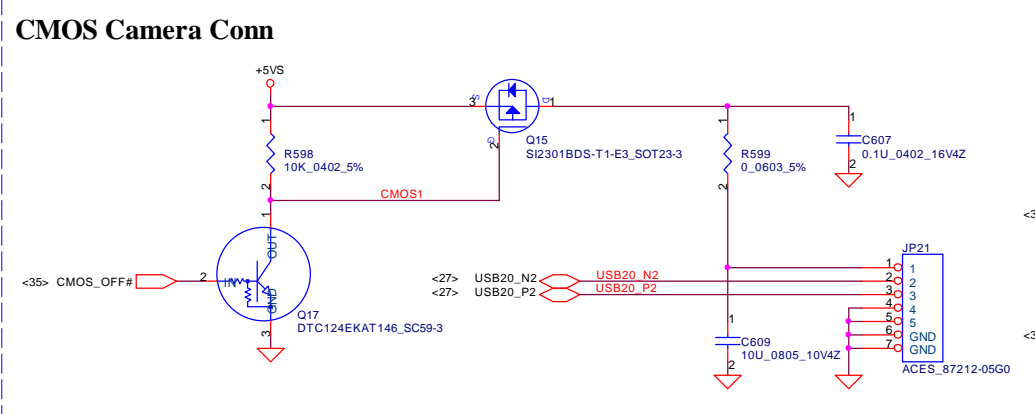
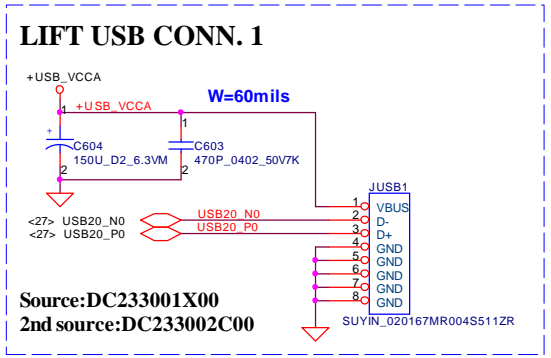
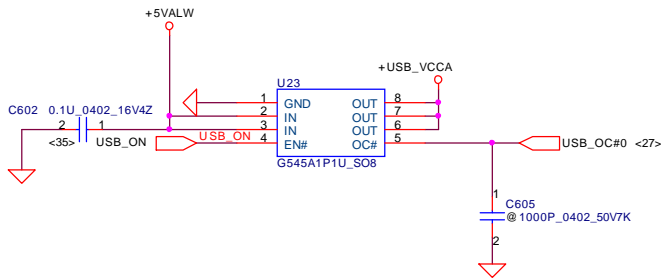
INPUT		OUTPUT
A	B	Y
L	L	L
H	L	H
L	H	H
H	H	H



LED Green

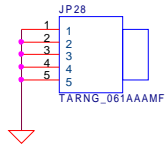


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				Size B	Document Number
				JITRI_LA-4141P	
				Date:	Friday, June 27, 2008
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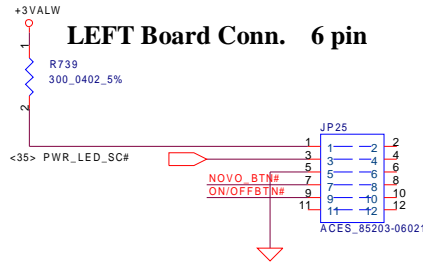


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Date:	Friday, June 27, 2008	Sheet	

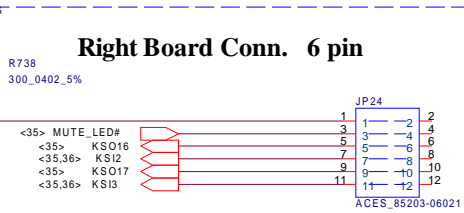
TV ANTENNA



LEFT Board Conn. 6 pin

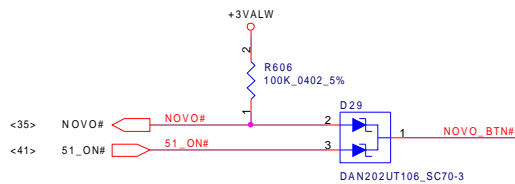
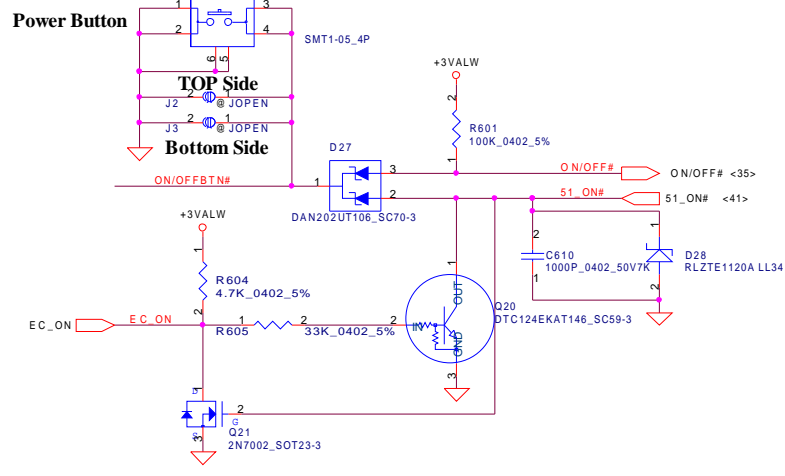


Right Board Conn. 6 pin

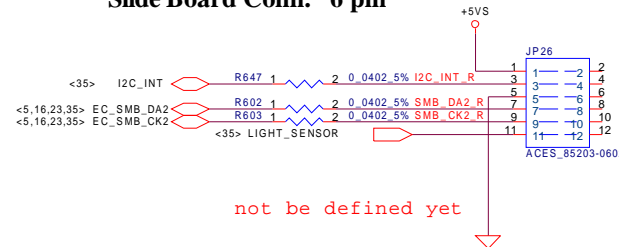


BTN FUNCTION	KEY MATRIX	
	IN	OUT
UP	KSO16	KSI2
DOWN	KSO17	KSI2
MUTE	KSO17	KSI3

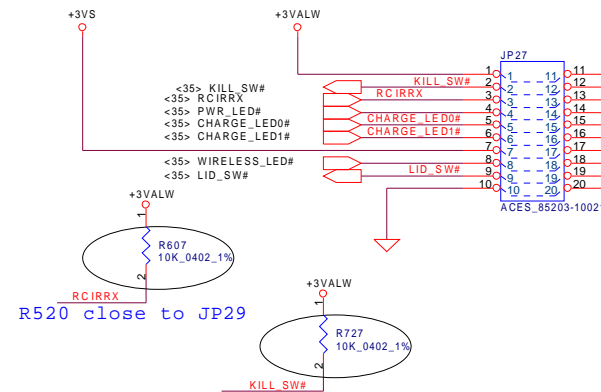
ON/OFF switch



Slide Board Conn. 6 pin

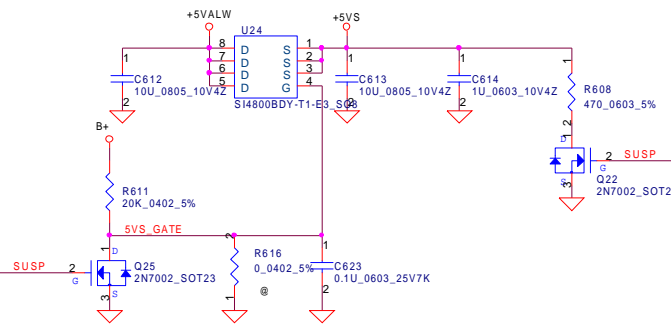


CIRI Board Conn. 14 pin

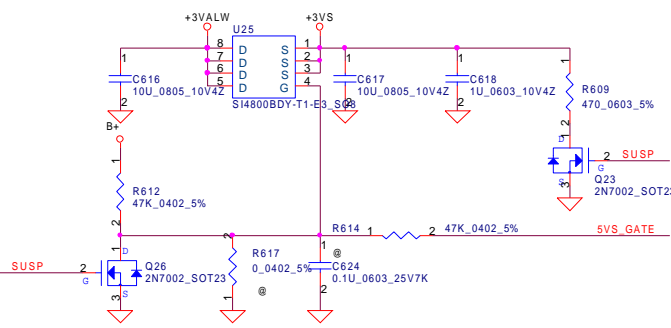


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Size	Document Number	Rev		
Custo	KIWB3/B4_LA4551P	0.1		
Date:	Friday, June 27, 2008	Sheet	39	of 49

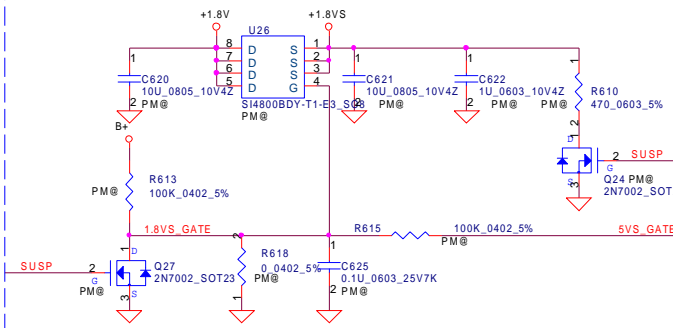
+5VALW TO +5VS



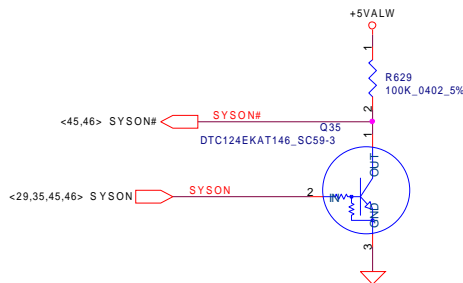
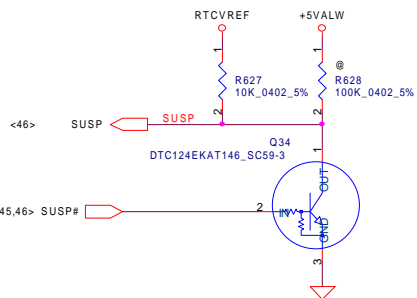
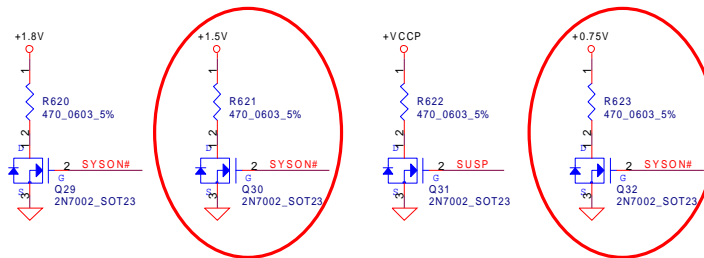
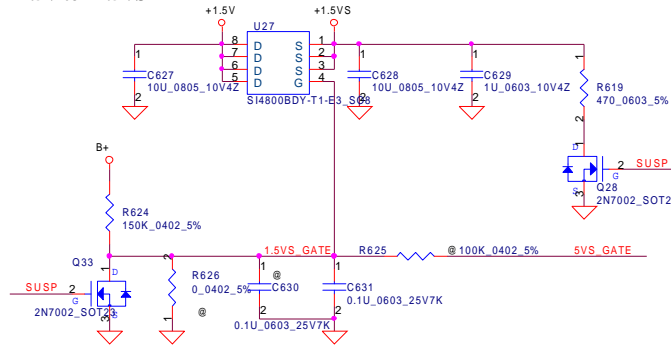
+3VALW TO +3VS



+1.8V to +1.8VS

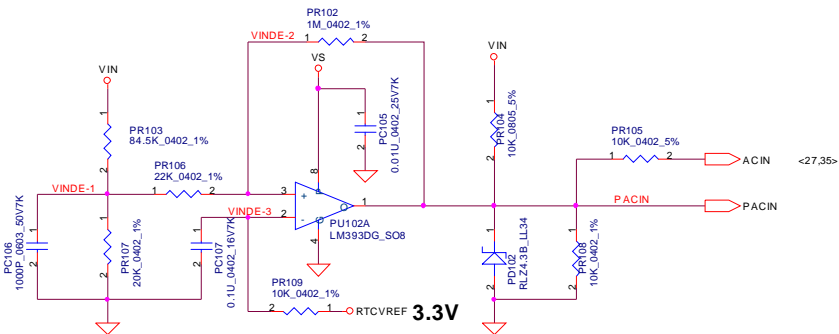
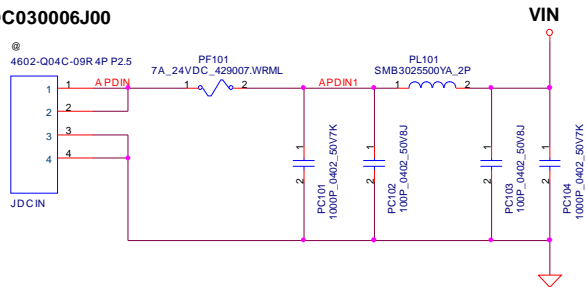


+1.5V to +1.5VS



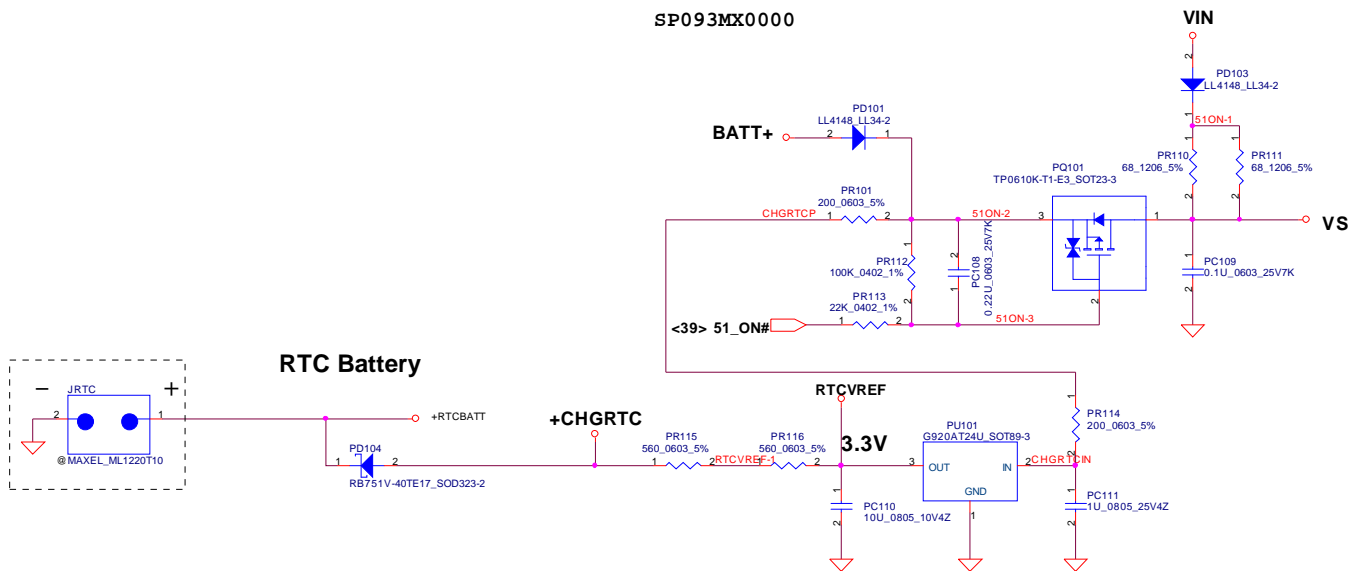
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DC030006J00

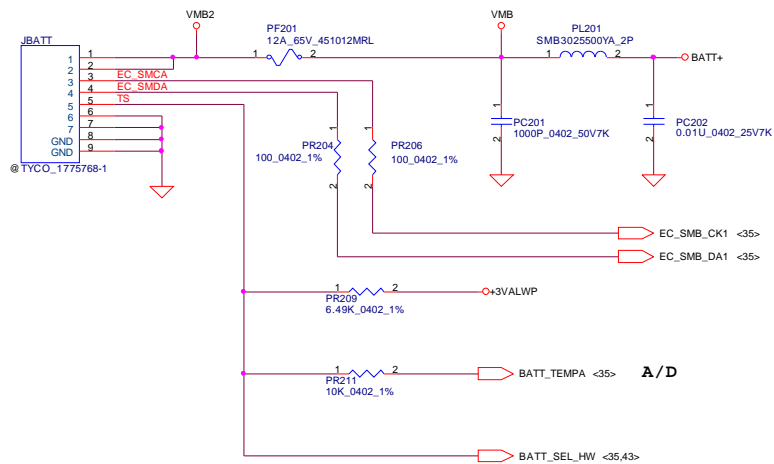


Vin Detector
High 18.384 17.901 17.430
Low 17.728 17.257 16.976

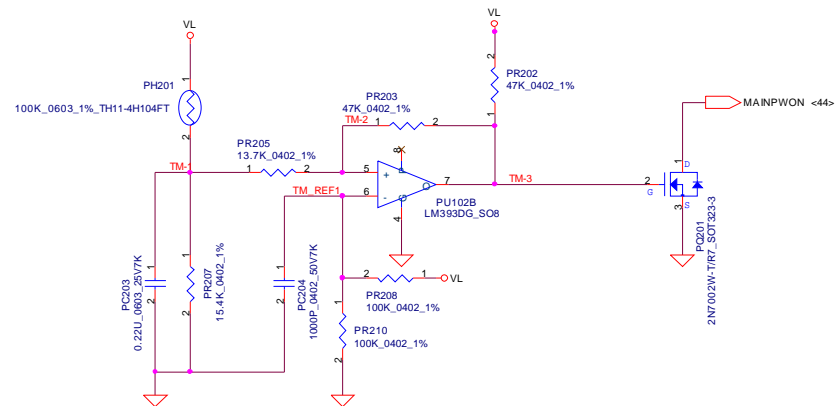
SP093MX0000



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PH1 under CPU bottom side :
 CPU thermal protection at 92 degree C
 Recovery at 56 degree C



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1. ACDET
 - ACOV
 - CHG_PVCC
 - ACSET
 - ACOP/IADP
 - ACGOOD#
2. BATT_OVP
 - BATT_CELL
 - CHG_VOLT
 - CHG_CURT
 - BATT_LEARN

CP Point Setting
 CP point=ladapter*85%
 $V_{acset}=3.3 \cdot (115K/(75K+115K))=1.99V$
 $CP \text{ Point}=(V_{acset}/V_{dca}) \cdot (0.1/PR302)=4.02A$

65W adapter
 $V_{acset}=3.3 \cdot (115K/(150K+115K))=1.432V$
 $CP \text{ Point}=(V_{acset}/V_{dca}) \cdot (0.1/PR302)=2.89A$

Input OVP : 22.3V
 ACIN detect : 17.26V
 Fsw : 300KHz

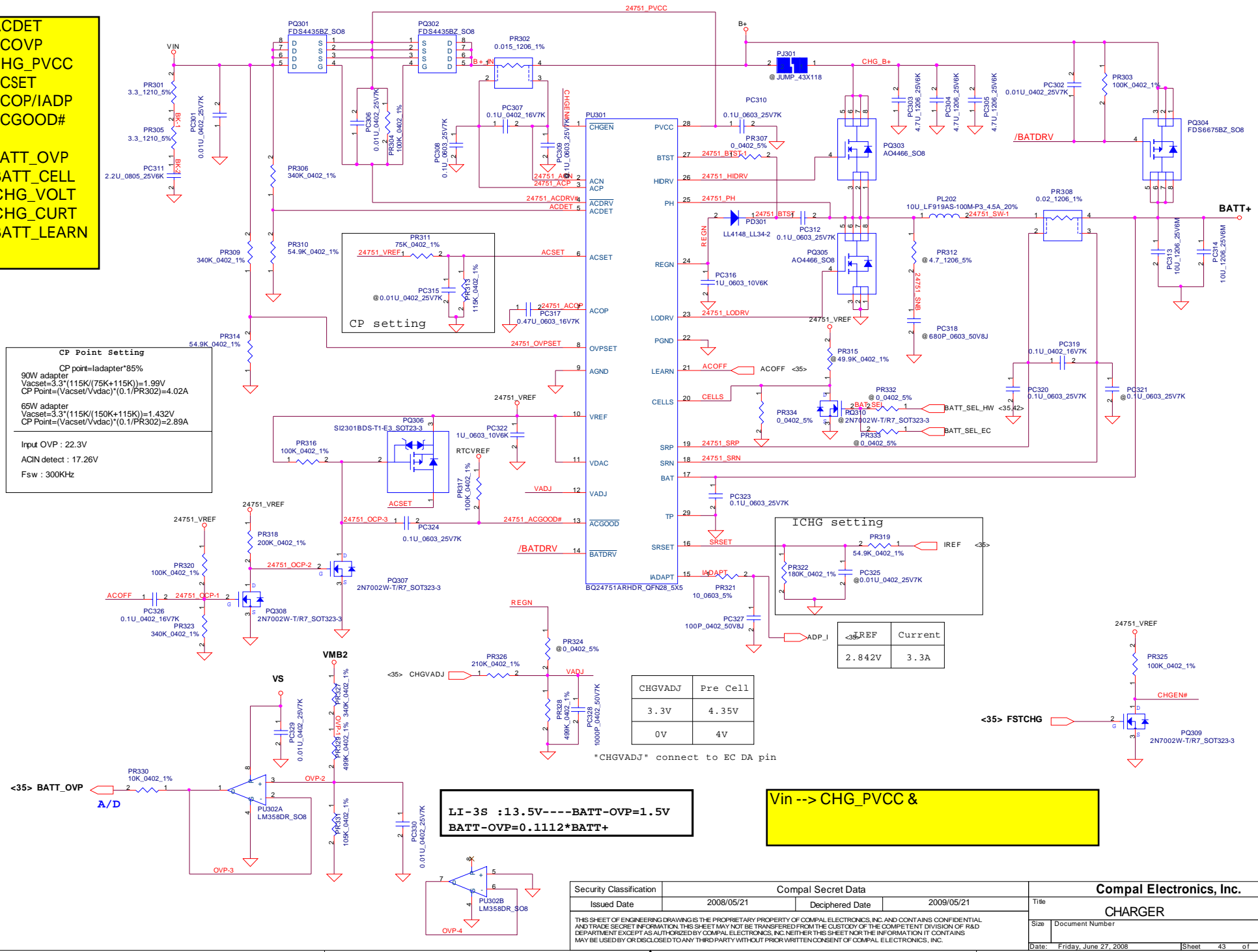
ICHG setting

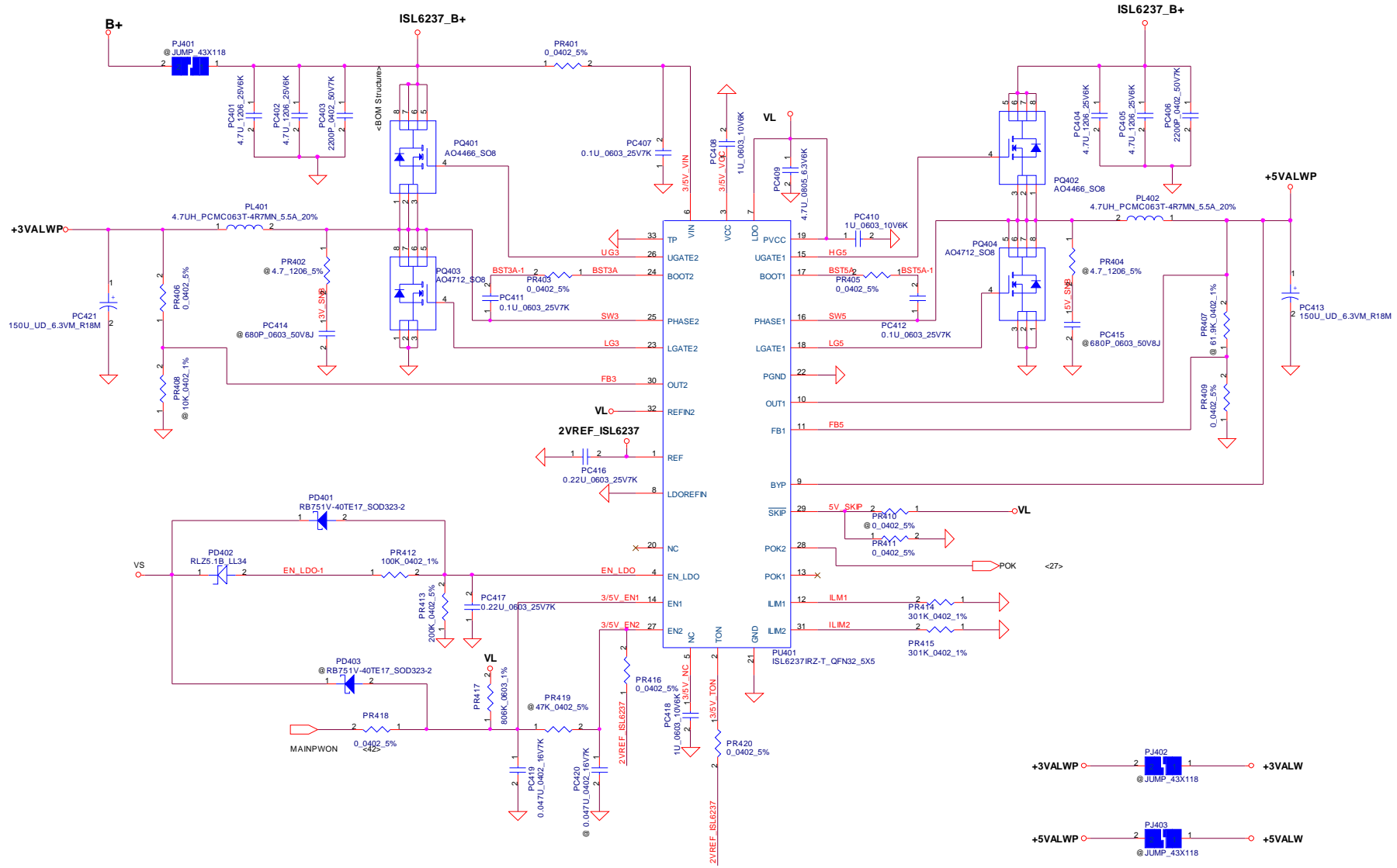
IREF	Current
2.842V	3.3A

CHGVADJ	Pre Cell
3.3V	4.35V
0V	4V

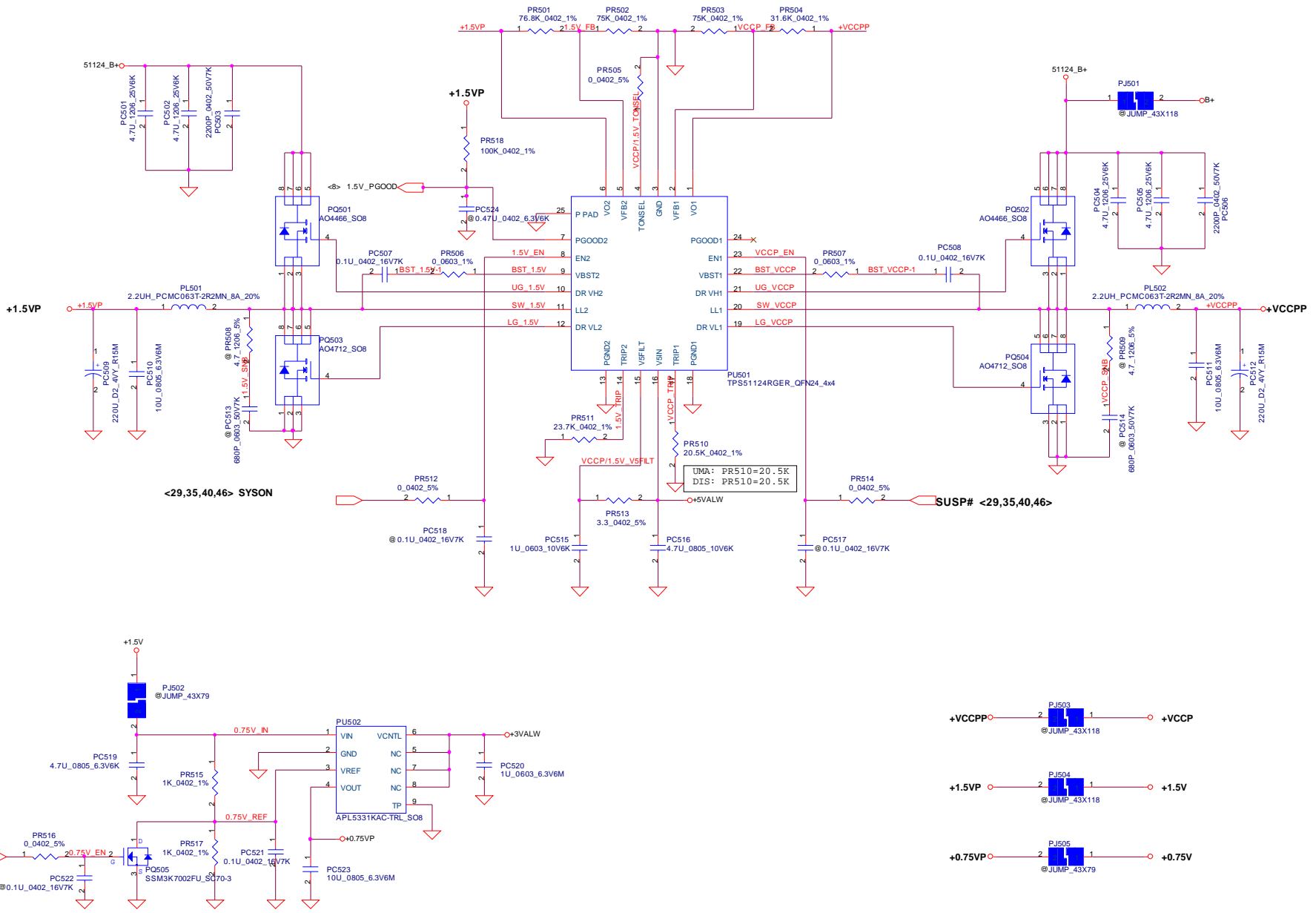
LI-3S : 13.5V --- BATT-OVP=1.5V
BATT-OVP=0.1112*BATT+

Vin --> CHG_PVCC &



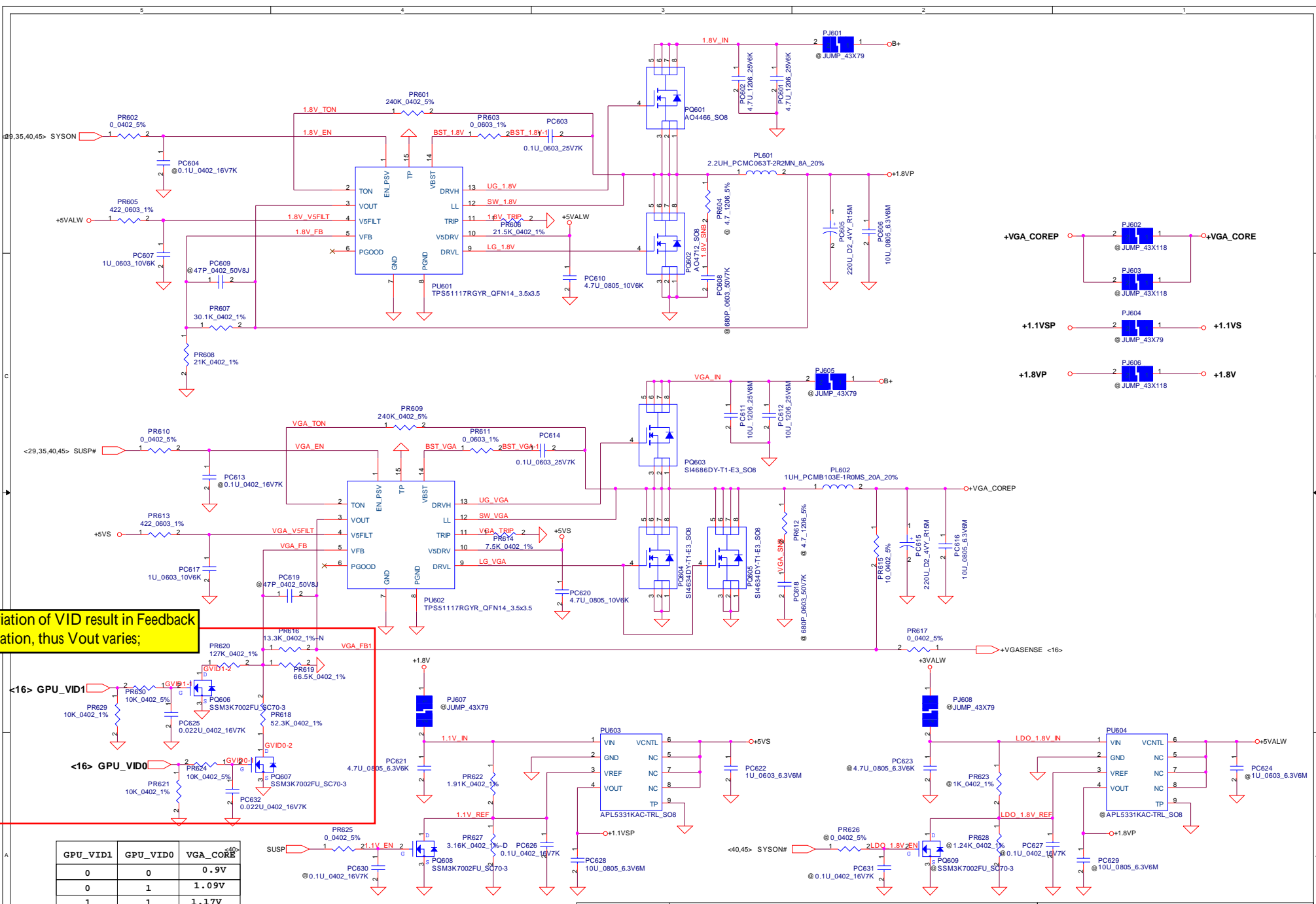


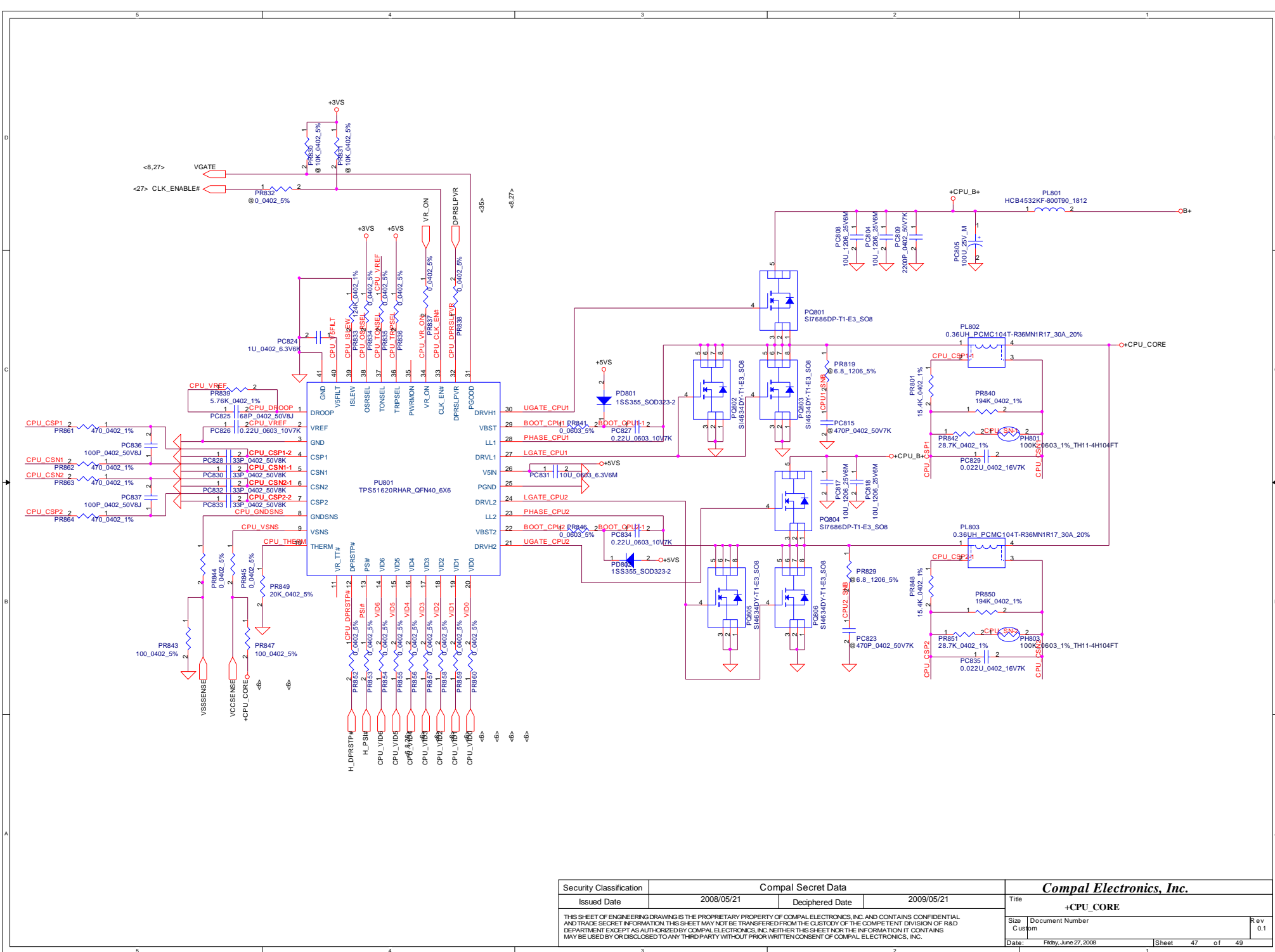
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		2008/11/12
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				+CPU_CORE
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Schematic modify	0.1	41 43 46 47	Add PR334,PR861,PR862,PR863PR864 Cancel PH802 Change PR841,PR846 to 0ohm Change PC831 to 10U Change PR840,PR850 to 194K Change PR801,PR848 to 15.4K Change PR842,PR851 to 28.7K Change PC106 to 1000P Change PC829,PC835 to 0.022U Change PR622 to 1.91K Change PR627 to 3.16K Change PR628 to 1.24K PU401 main source change to TPS51427		EVT
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NO DATE PAGE MODIFICATION LIST PURPOSE

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Title		
<i>HW PIR</i>		
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