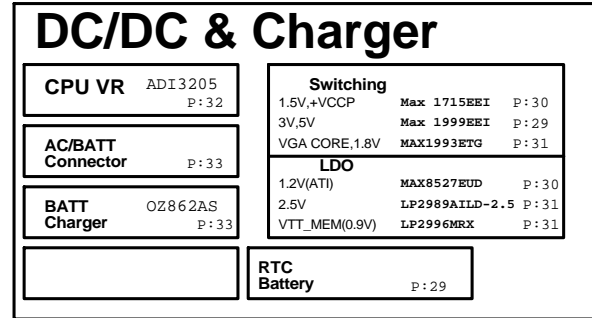


ARIES II BLOCK DIAGRAM

Dothan(Yonah)/Alviso




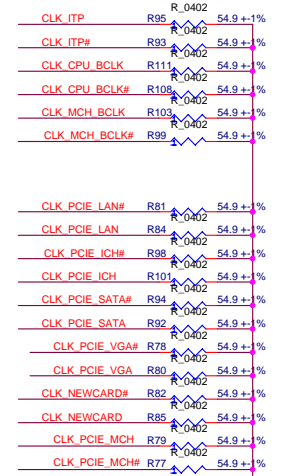
INDEX

Pg#	Description	DNI LIST
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10	DDR SO-DIMM	
11-13	ICH4-M	
14	Device Bay & Bridge BATT	
15	USB ports	
16	Cardbus Connector	
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20	RJ11&RJ45	
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35	CPU Power(max1987)	
36	Discharge	
37	Charger(max1772)&AC/BAT CONN	
38	EMI PADs& Screws	



Power & Ground

ADIN

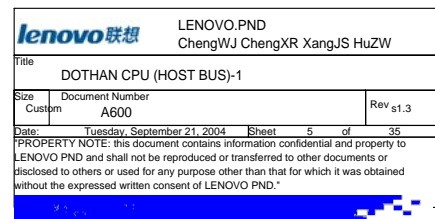
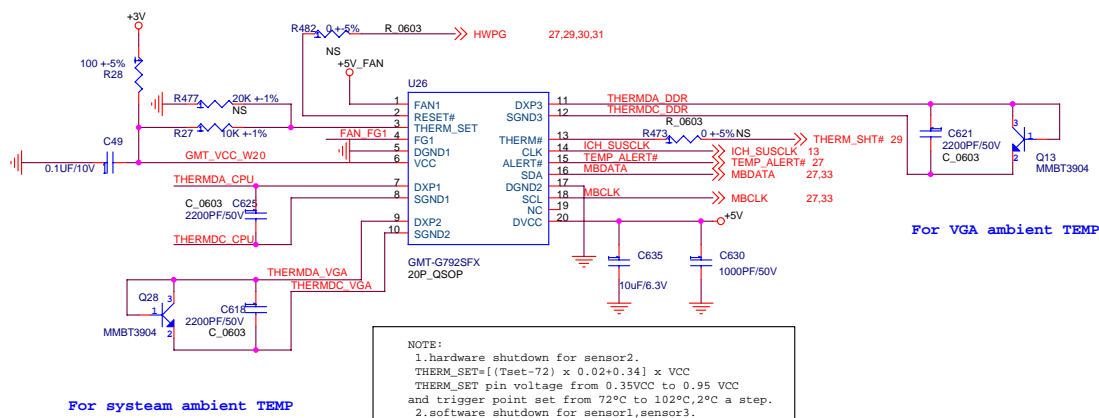
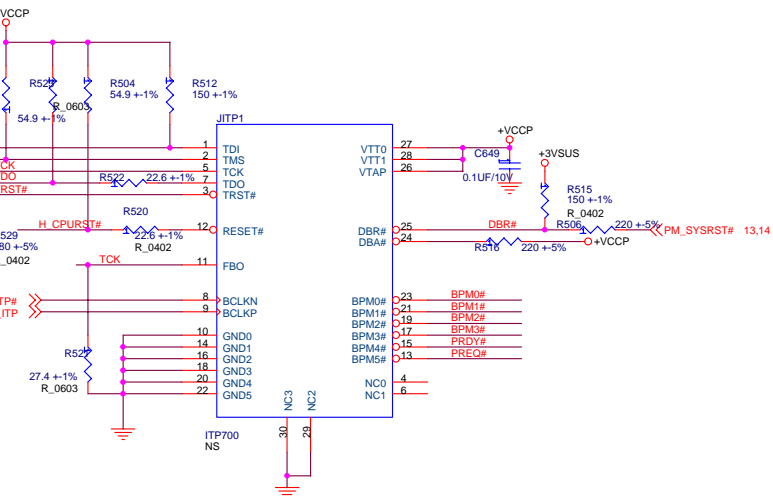
Label	Pg#	Description	Control Signal
 VA		AC ADAPTER (20V)	
 MBAT+		MAIN BATTERY + (10~17V)	
 VIN	23,29,30,31,32,33	MAIN POWER (10~20V)	
 VCCRTC	12,14,27,29	RTC & PCL POWER (3..3V)	
 +3VALW	23,26,27,29,33	EC 3V always power	
 +5VALW	28,29	5V always power	
 3VAUX	16,18,29	LAN power	3VAUXEN
 +1.5VSUS	14,30	ICH4-M 1.5V SUS power	SUSON
 VDIMM	7,9,10,11,28,31	DDRII RAM 1.8V power	SUSON
 +3VSUS	5,13,14,17,18,28,29,31	3V	SUSON
 +5VSUS	14,15,16,28,29,30	5V	SUSON
 +1.5V	6,7,10,13,14,16,21,28,30	AGP I/O power	MAINON
 +1.8V	6,20,21,28,31	+1.8V	MAINON
 VCORE_VGA	21,28,31	VGA Core power	MAINON
 VMEM_VGA	20,21	VGA 2.5V power	MAINON
 +3V	4,5,11,12,13,14,15,16,17,18,19,21,22,23,24,26,27,28,29,30,32	+3V	MAINON
 +5V	5,12,14,15,16,18,22,23,24,25,26,27,28,29,32	+5V	MAINON
 +5VA	24	AUDIO analog 5V power	MAINON
 +5V_FAN	5	FAN 5V power	VFAN
 BAYVCC	15	MediaBay 5V power	RBAYON#
 +12V		High Voltage to control MOS	MAINON
 VCORE_CPU	6,32	CPU power	VRON
 +VCCP	4,5,6,7,9,10,12,14,30	CPUI/O powers(1.05V)	MAINON
 +1.2V	21,30		VRON
 REF3V	33	EC analog 3V power	REFON
 GND	ALL PAGES	DIGITAL GROUND	
 AUDGND	16,24,25,34	AUDIO GND	

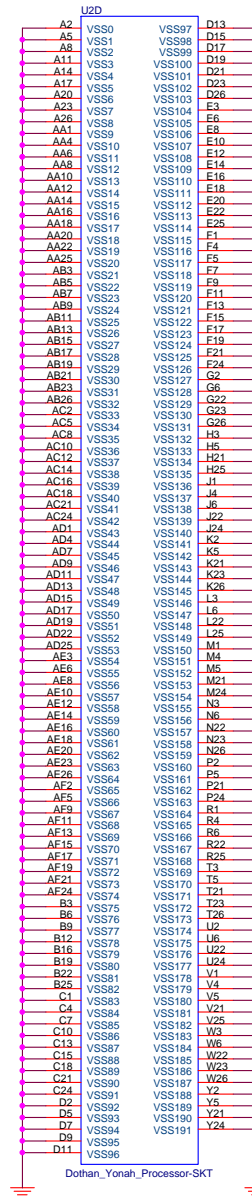
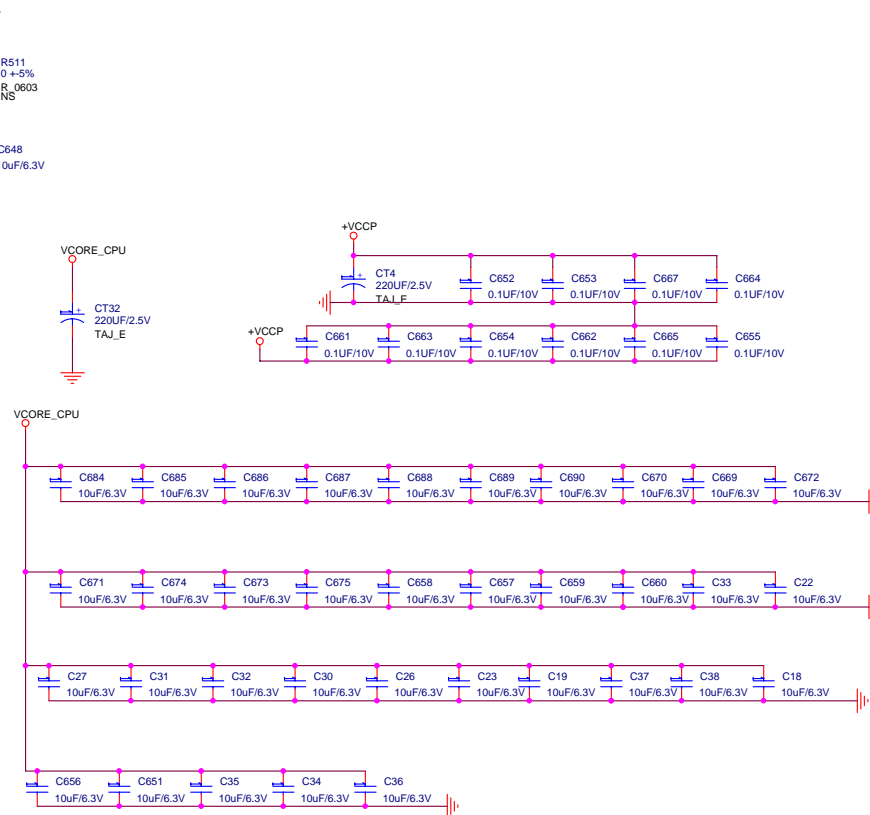
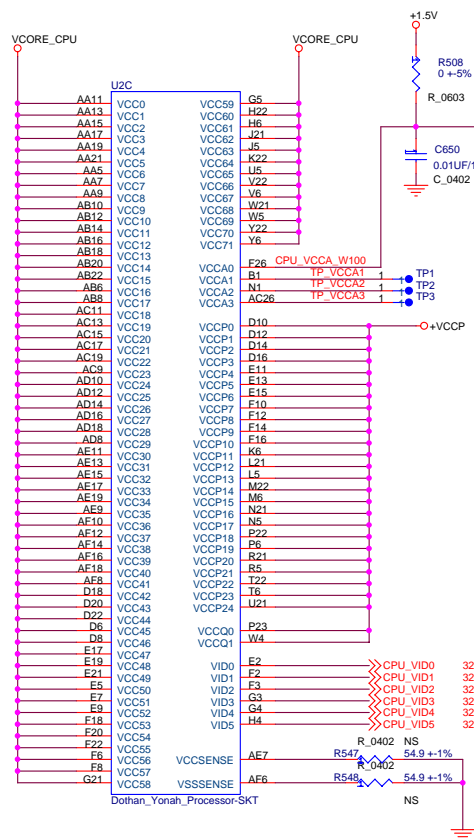


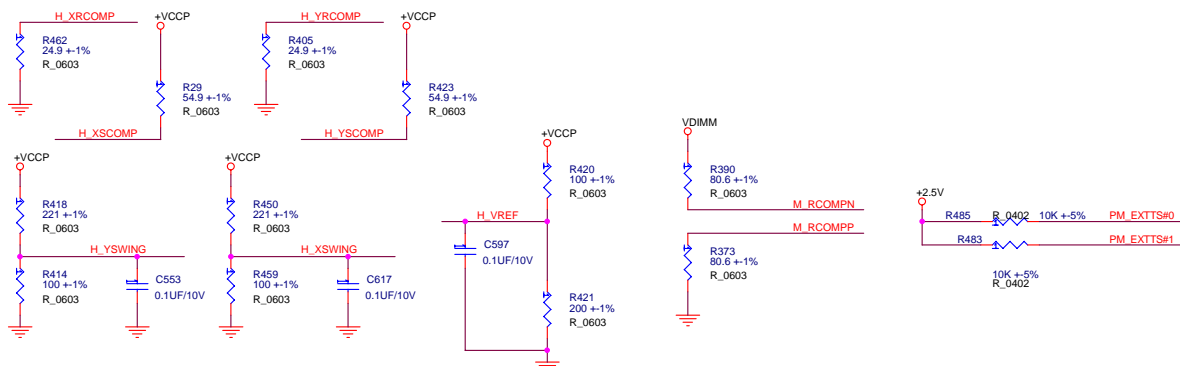
Place termination close to source IC

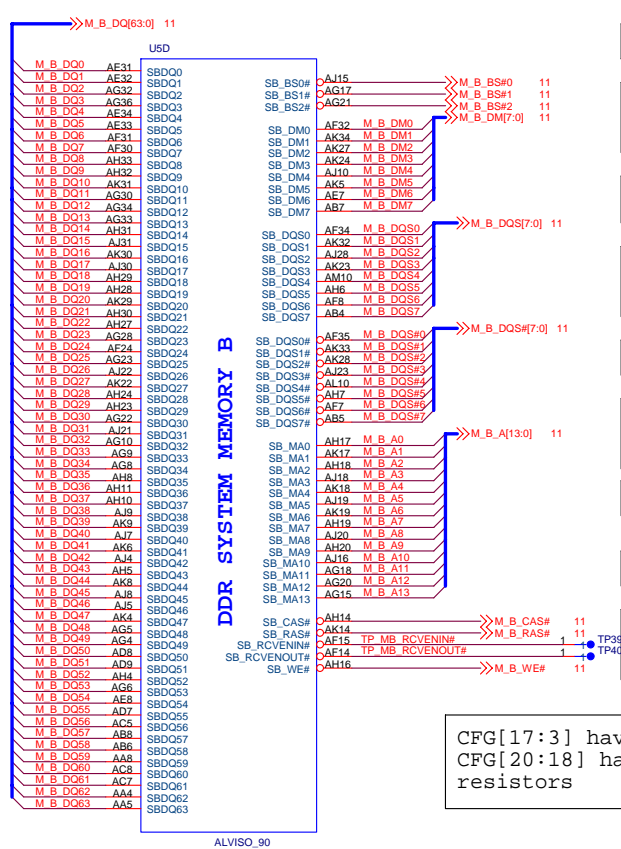
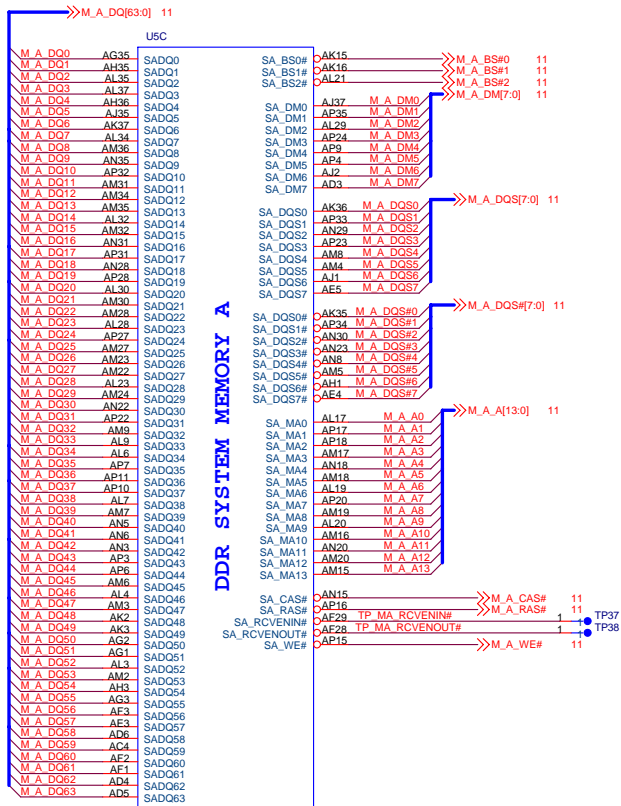
 		LENOVO.PND ChengWJ ChengXR XangJS HuZW	
Title			
CLOCK GENERATOR			
Size	Document Number		Rev. s1.1
Custom	A600		
Date:	Tuesday, September 21, 2004	Sheet	4 of 35

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CFG5	Low = DMix2	X
	High = DMix4	

CFG8 (LP PCIE)	Low = Normal Mode High = Low Power Mode	X
----------------------	--------------------------------------------------	---

CFG9 PCIe Graphics Lane	Low = Reverse Lane High = Normal operation	X
-------------------------------	--------------------------------------------------	---

CFG10 (Host PLL VCC Solution Select)	Low = Portability Option High = Mobility Option	X
-----------------------------------------------	----------------------------------------------------------	---

CFG11 (PSB 4x CLK Enable)	Low = HCLK 4x High = HCLK 8x	X
------------------------------	---------------------------------	---

CFG16 (FSB Dynamic ODT)	Low = Dynamic ODT Disabled High = Dynamic ODT Enabled	X
-------------------------------	----------------------------------------------------------------	---

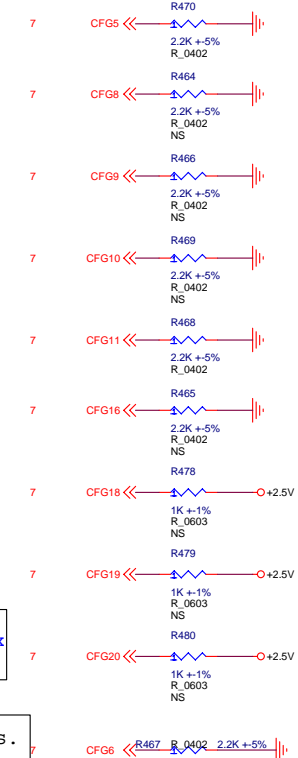
CFG18 (VCC Select)	Low = 1.05V High = 1.5V	X
-----------------------	----------------------------	---

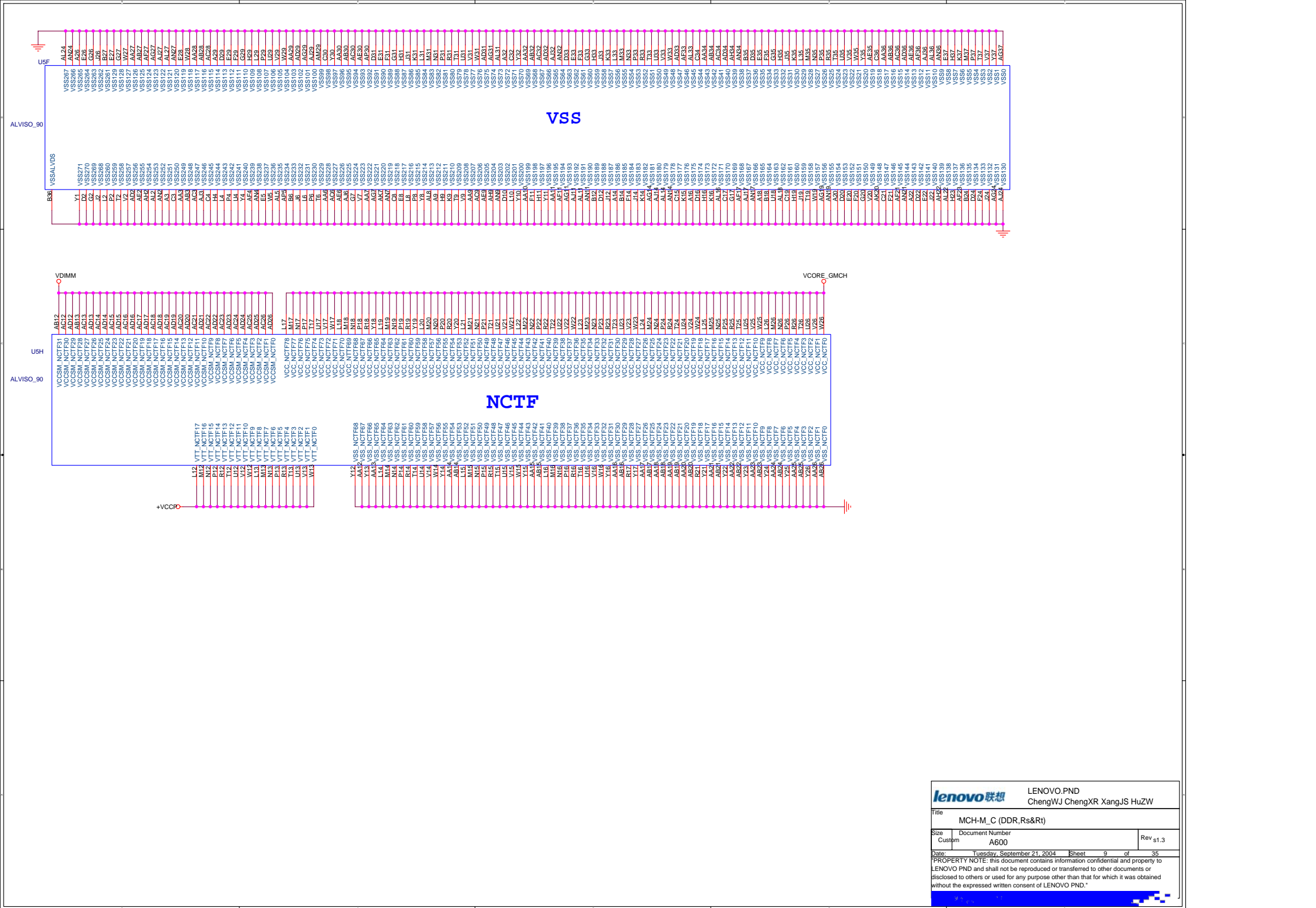
CFG19 (VTT Select)	Low = 1.05V High = 1.2V	X
-----------------------	----------------------------	---

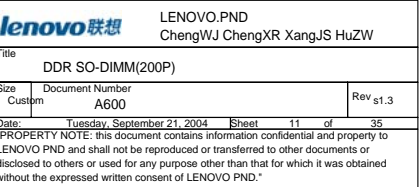
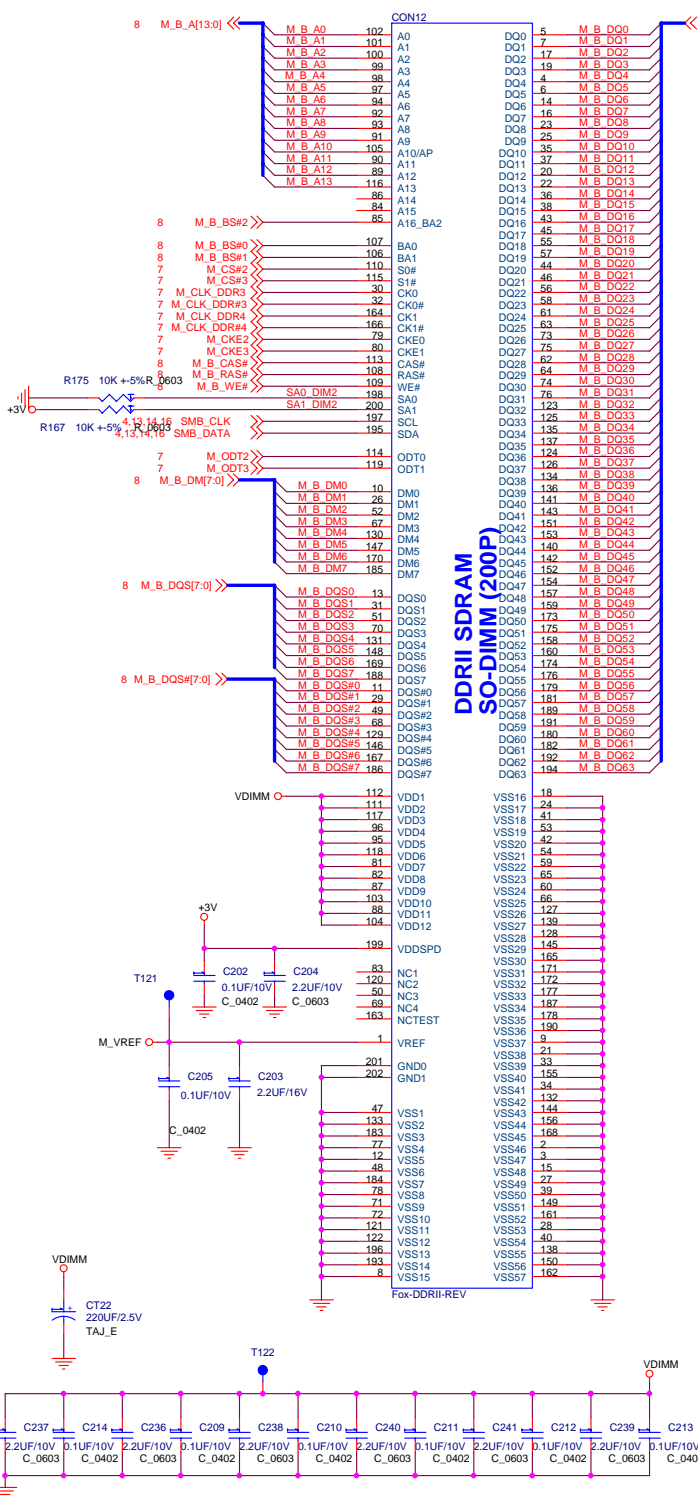
CFG20 (PCIe Backward Interoperability mode)	Low = Normal High = Backward Interoperability Enabled	X
---------------------------------------------------	----------------------------------------------------------------	---

CFG[17:3] have internal pullup resistors.
CFG[20:18] have internal pulldown
resistors

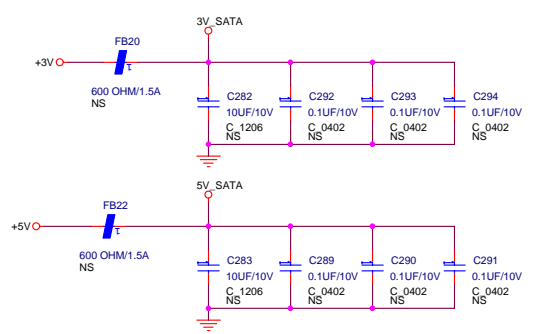
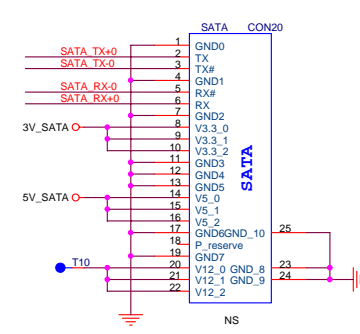
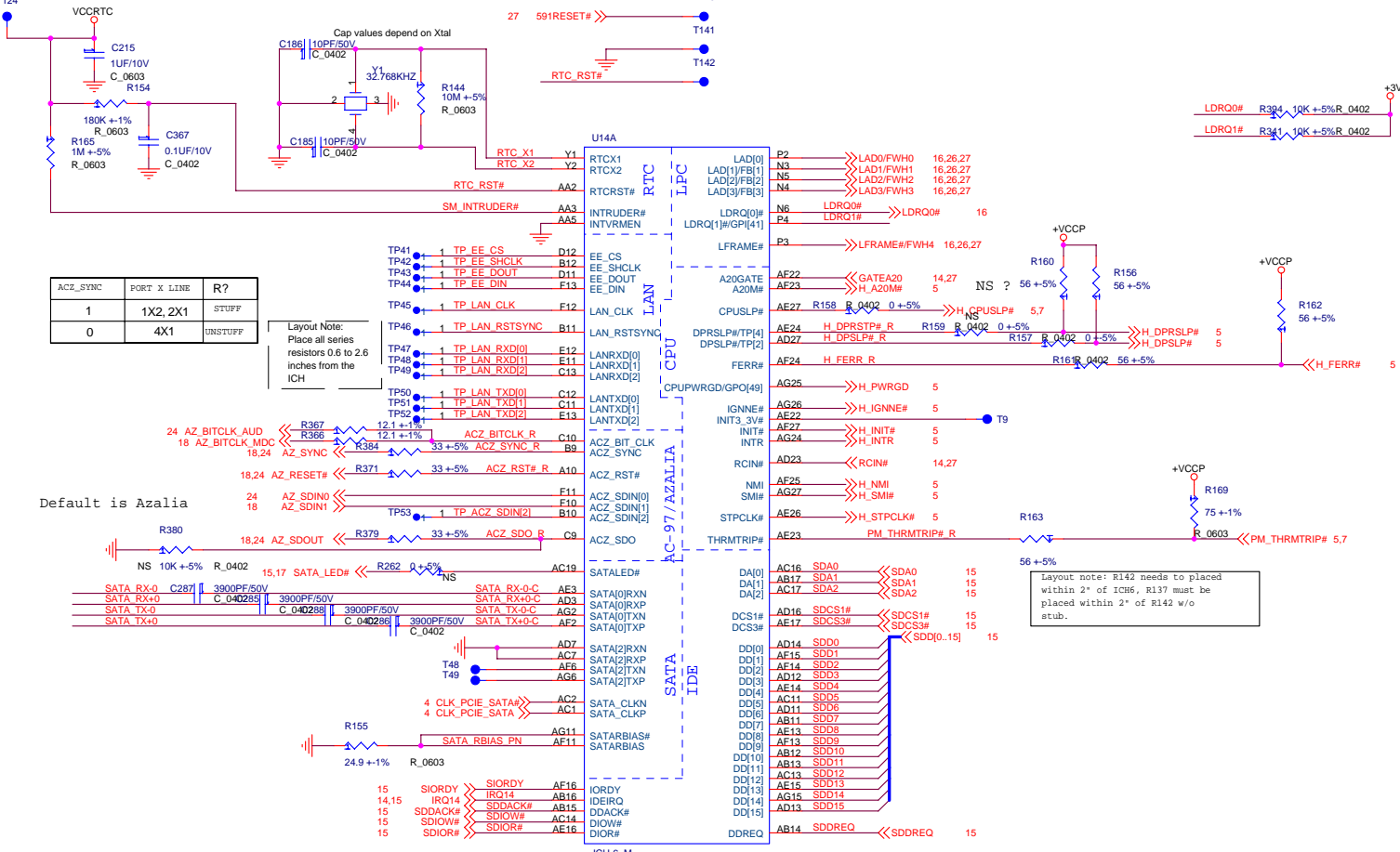
CFG6 (DDR Select)	Low = DDR-II High = DDR-I	
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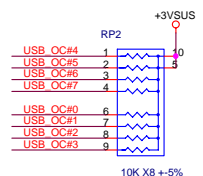




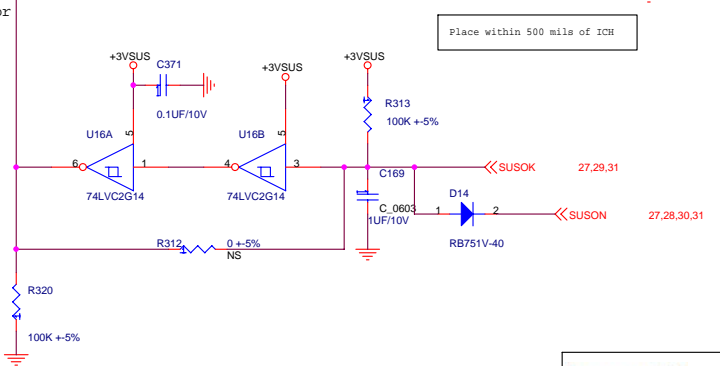


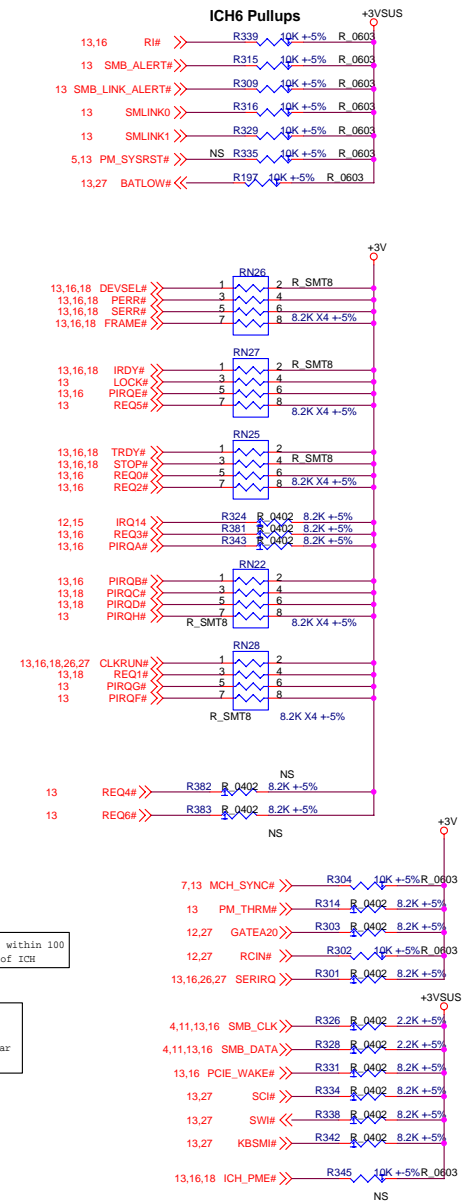
124 Consider VCCRTC sources

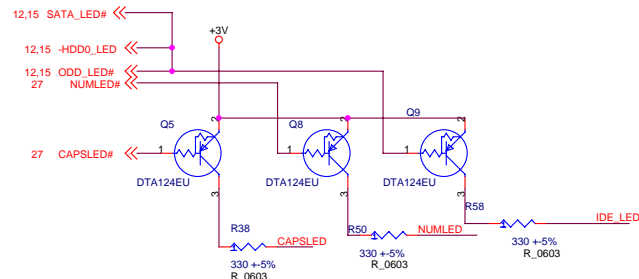




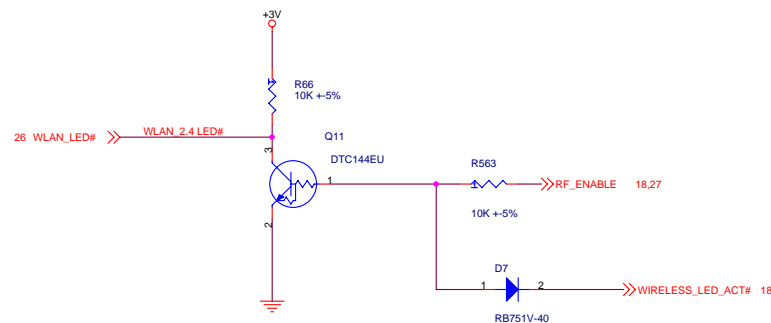
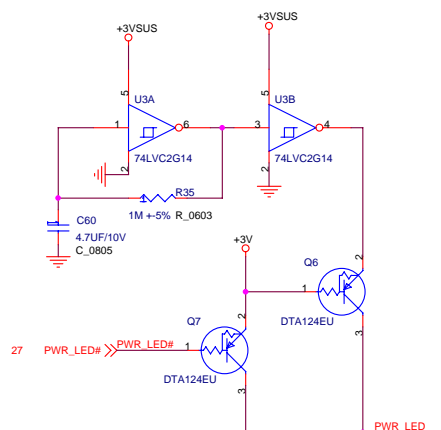
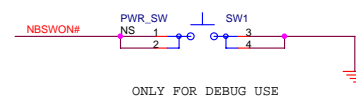
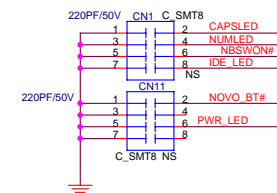
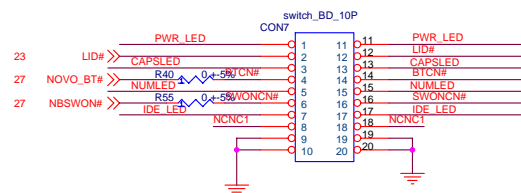
```
0 : SYS Port
1 : SYS Port
2 : SYS Port
3 : USB-KEY
4 : BlueTooth
5 : PC-CAM
7 : NewCard
```

[illegible]

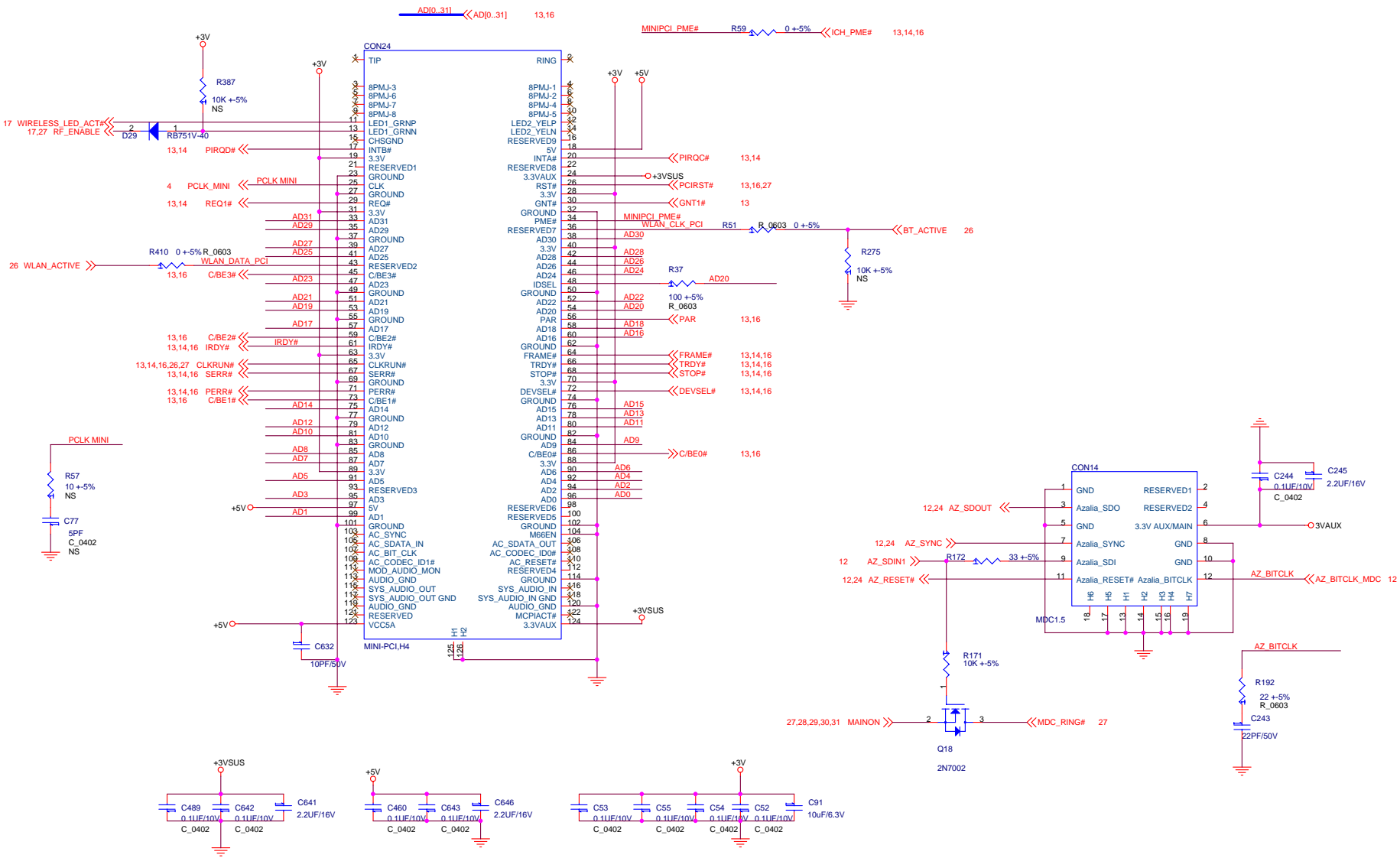




Switch Board



lenovo 联想		LENOVO.PND ChengWJ ChengXR XangJS HuZW	
Title BOARD CONN			
Size Custom	Document Number A600		Rev s1.3
Date:	Tuesday, September 21, 2004	Sheet 17 of 35	
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PEG_TXN0	C562	0.1UF/10V	C_0402	VPEG_TXN0
PEG_TXN1	C568	0.1UF/10V	C_0402	VPEG_TXN1
PEG_TXN2	C548	0.1UF/10V	C_0402	VPEG_TXN2
PEG_TXN3	C551	0.1UF/10V	C_0402	VPEG_TXN3
PEG_TXN4	C538	0.1UF/10V	C_0402	VPEG_TXN4
PEG_TXN5	C520	0.1UF/10V	C_0402	VPEG_TXN5
PEG_TXN6	C526	0.1UF/10V	C_0402	VPEG_TXN6
PEG_TXN7	C509	0.1UF/10V	C_0402	VPEG_TXN7
PEG_TXN8	C502	0.1UF/10V	C_0402	VPEG_TXN8
PEG_TXN9	C491	0.1UF/10V	C_0402	VPEG_TXN9
PEG_TXN10	C482	0.1UF/10V	C_0402	VPEG_TXN10
PEG_TXN11	C463	0.1UF/10V	C_0402	VPEG_TXN11
PEG_TXN12	C473	0.1UF/10V	C_0402	VPEG_TXN12
PEG_TXN13	C457	0.1UF/10V	C_0402	VPEG_TXN13
PEG_TXN14	C445	0.1UF/10V	C_0402	VPEG_TXN14
PEG_TXN15	C450	0.1UF/10V	C_0402	VPEG_TXN15

PEG_TXP0	C566	0.1UF/10V	C_0402	VPEG_TXP0
PEG_TXP1	C561	0.1UF/10V	C_0402	VPEG_TXP1
PEG_TXP2	C550	0.1UF/10V	C_0402	VPEG_TXP2
PEG_TXP3	C559	0.1UF/10V	C_0402	VPEG_TXP3
PEG_TXP4	C546	0.1UF/10V	C_0402	VPEG_TXP4
PEG_TXP5	C527	0.1UF/10V	C_0402	VPEG_TXP5
PEG_TXP6	C537	0.1UF/10V	C_0402	VPEG_TXP6
PEG_TXP7	C517	0.1UF/10V	C_0402	VPEG_TXP7
PEG_TXP8	C510	0.1UF/10V	C_0402	VPEG_TXP8
PEG_TXP9	C499	0.1UF/10V	C_0402	VPEG_TXP9
PEG_TXP10	C492	0.1UF/10V	C_0402	VPEG_TXP10
PEG_TXP11	C474	0.1UF/10V	C_0402	VPEG_TXP11
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PEG_TXP13	C462	0.1UF/10V	C_0402	VPEG_TXP13
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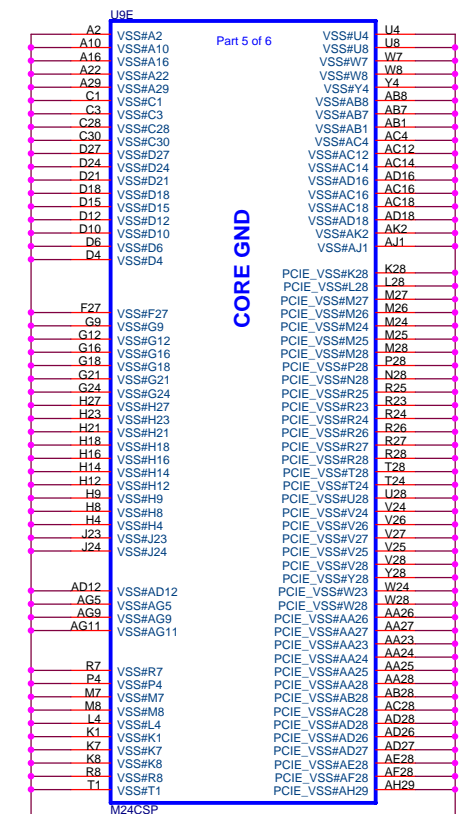
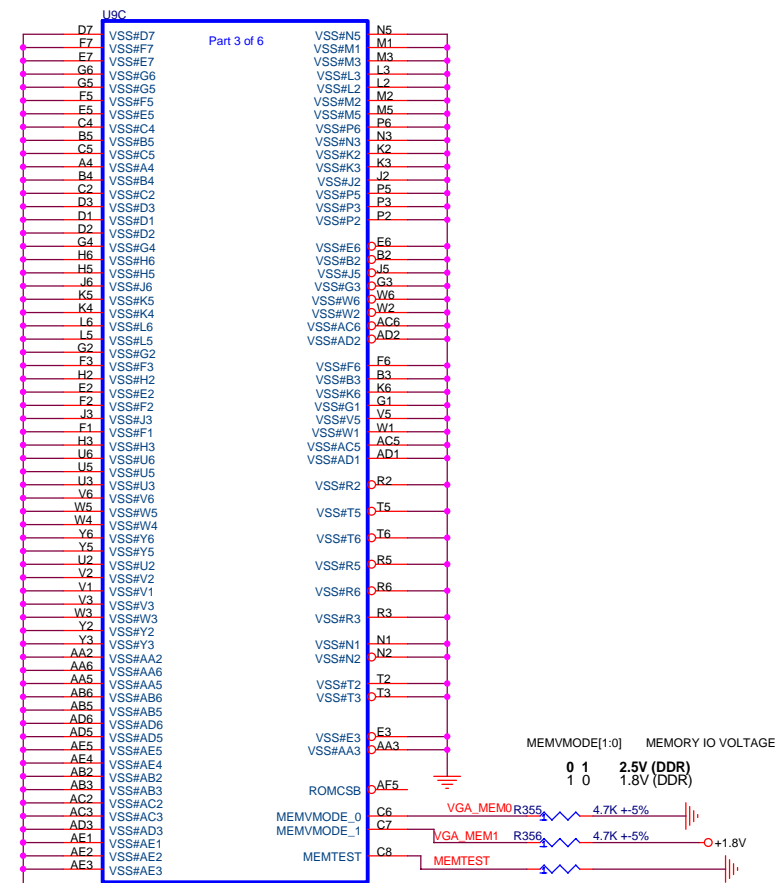
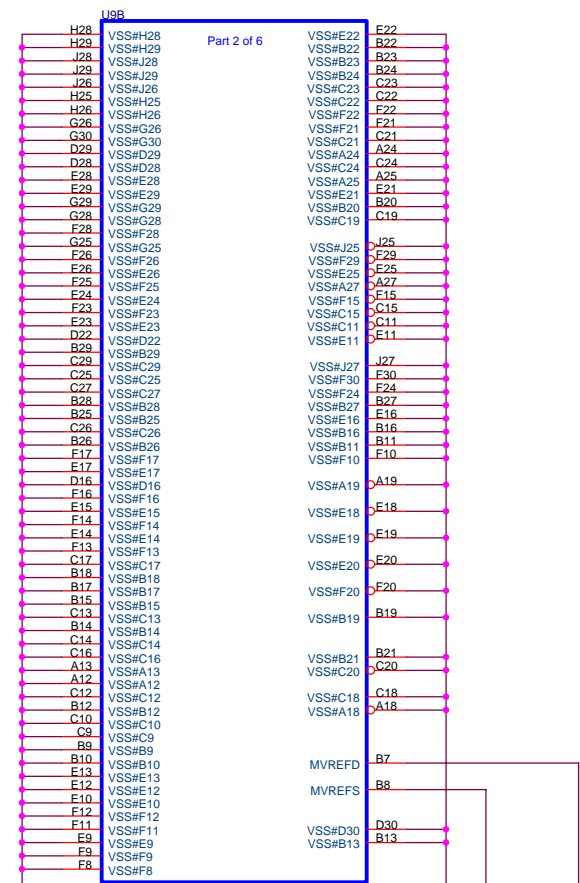
place these CAP close to M24

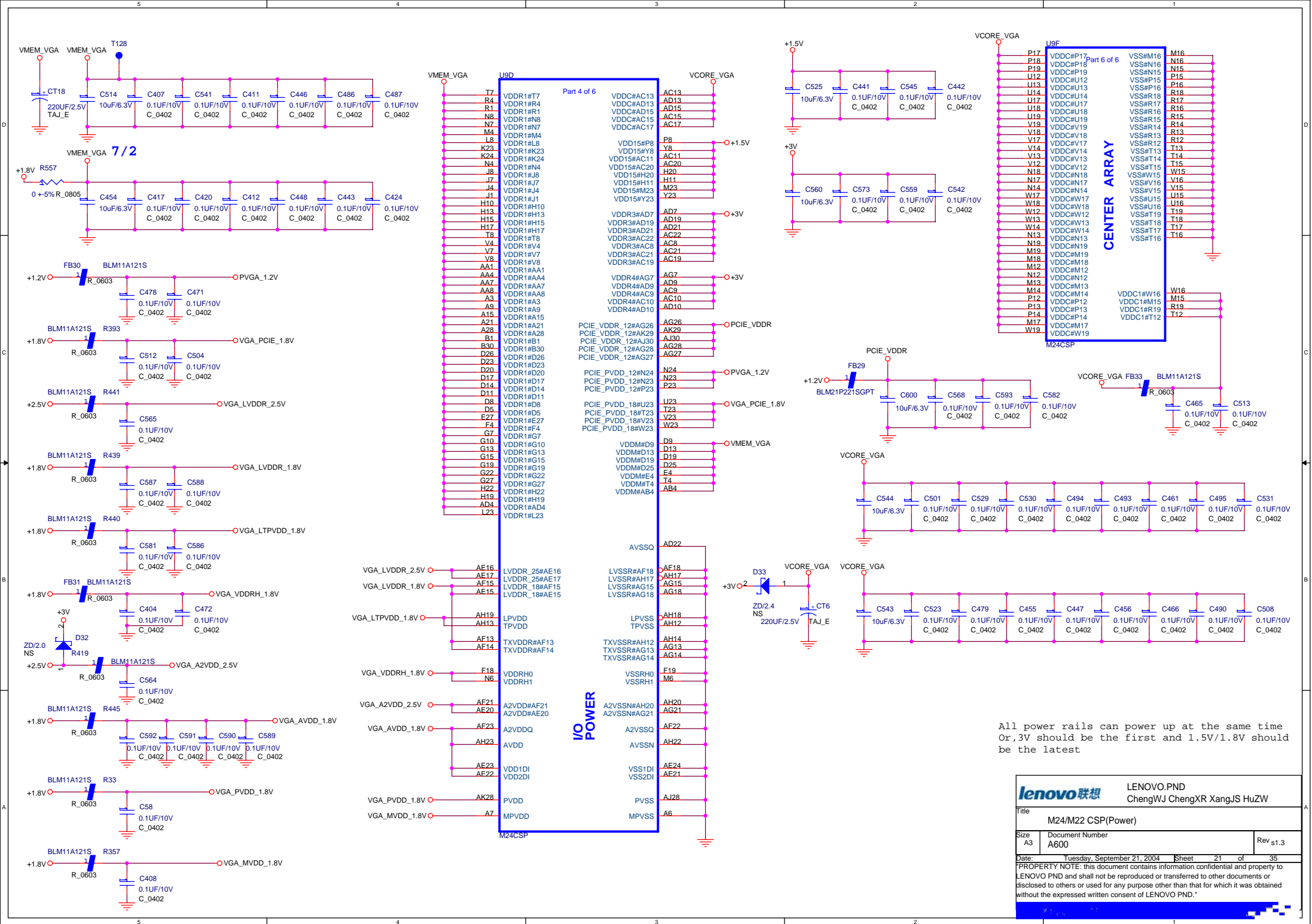
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VPEG_RXP2	AE29	PCIE_RX2P
VPEG_RXN2	AE30	PCIE_RX2N
VPEG_RXP3	AD30	PCIE_RX3P
VPEG_RXN3	AD29	PCIE_RX3N
VPEG_RXP4	AC29	PCIE_RX4P
VPEG_RXN4	AB29	PCIE_RX4N
VPEG_RXP5	AB30	PCIE_RX5P
VPEG_RXN5	AA30	PCIE_RX5N
VPEG_RXN6	AA29	PCIE_RX6P
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VPEG_RXP9	U29	PCIE_RX8N
VPEG_RXN9	T29	PCIE_RX9P
VPEG_RXP10	T30	PCIE_RX9N
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VPEG_RXP11	R29	PCIE_RX10N
VPEG_RXN11	P29	PCIE_RX11P
VPEG_RXP12	N29	PCIE_RX11N
VPEG_RXN12	M29	PCIE_RX12P
VPEG_RXP13	M30	PCIE_RX12N
VPEG_RXN13	M29	PCIE_RX13P
VPEG_RXP14	L29	PCIE_RX13N
VPEG_RXN14	K29	PCIE_RX14P
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VPEG_RXN15	J30	PCIE_RX15P
		PCIE_RX15N

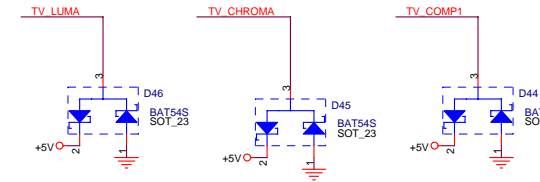
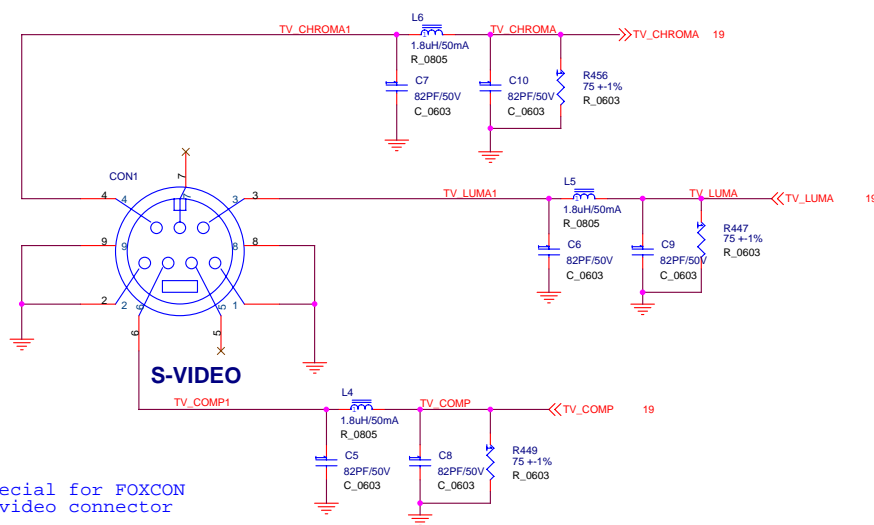
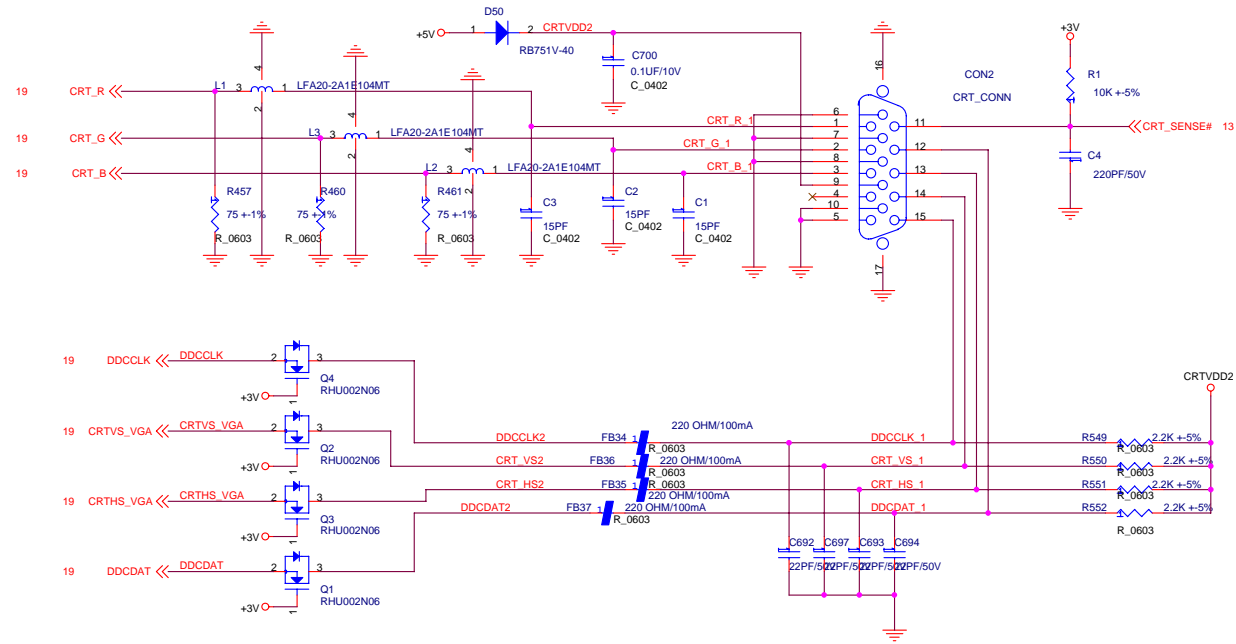
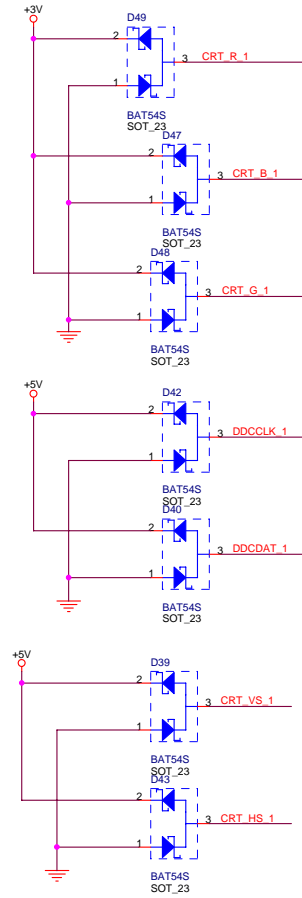
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VPEG_TXN2	AB27	PCIE_TX2N
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VPEG_TXN3	AB26	PCIE_TX3N
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VPEG_TXN4	W25	PCIE_TX4N
VPEG_TXP5	Y22	PCIE_TX5P
VPEG_TXN5	W27	PCIE_TX5N
VPEG_TXP6	Y26	PCIE_TX6P
VPEG_TXN6	W26	PCIE_TX6N
VPEG_TXP7	U25	PCIE_TX7P
VPEG_TXN7	T25	PCIE_TX7N
VPEG_TXP8	U27	PCIE_TX8P
VPEG_TXN8	T27	PCIE_TX8N
VPEG_TXP9	U26	PCIE_TX9P
VPEG_TXN9	T26	PCIE_TX9N
VPEG_TXP10	P25	PCIE_TX10P
VPEG_TXN10	N25	PCIE_TX10N
VPEG_TXP11	N27	PCIE_TX11P
VPEG_TXN11	M27	PCIE_TX11N
VPEG_TXP12	P26	PCIE_TX12P
VPEG_TXN12	N26	PCIE_TX12N
VPEG_TXP13	L25	PCIE_TX13P
VPEG_TXN13	K25	PCIE_TX13N
VPEG_TXP14	K27	PCIE_TX14P
VPEG_TXN14	J27	PCIE_TX14N
VPEG_TXP15	L26	PCIE_TX15P
VPEG_TXN15	K26	PCIE_TX15N

CLK_PCIE_VGA	AE27	PCIE_REFCLKP
CLK_PCIE_VGA#	AE27	PCIE_REFCLKN
CLK_PCIE_VGA#	AE27	PCIE_CALRP
CLK_PCIE_VGA#	AE27	PCIE_CALRN
CLK_PCIE_VGA#	AE27	PCIE_CALI
CLK_PCIE_VGA#	AE25	PCIE_TESTIN
CLK_PCIE_VGA#	AE25	PERSTb
CLK_PCIE_VGA#	AE25	PERSTb_MASK
CLK_PCIE_VGA#	AE25	R2SET
CLK_PCIE_VGA#	AE25	Y_G
CLK_PCIE_VGA#	AE25	C_R_PR
CLK_PCIE_VGA#	AE25	COMP_B_PB
CLK_PCIE_VGA#	AE25	H2SYNC
CLK_PCIE_VGA#	AE25	V2SYNC
CLK_PCIE_VGA#	AE25	SSIN
CLK_PCIE_VGA#	AE25	SSOUT
CLK_PCIE_VGA#	AE25	XTALIN
CLK_PCIE_VGA#	AE25	XTALOUT
CLK_PCIE_VGA#	AE25	TESTEN
CLK_PCIE_VGA#	AE25	TEST_YCLK
CLK_PCIE_VGA#	AE25	TEST_MCLK
CLK_PCIE_VGA#	AE25	PLLTEST
CLK_PCIE_VGA#	AE25	STEREOSYNC

Part 1 of 6	GPIO0	
	GPIO1	
	GPIO2	
	GPIO3	
	GPIO4	
	GPIO5	
	GPIO6	
	GPIO7	
	GPIO8	
	GPIO9	
GPIO10	GPIO11	
	GPIO12	
	GPIO13	
	GPIO14	
	GPIO15	
	GPIO16	
	GPIO17	
	GPIO18	
	GPIO19	
	GPIO20	
GPIO21	GPIO22	
	GPIO23	
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	GPIO31	
GPIO32	GPIO33	
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GPIO142	GPIO143	
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	GPIO148	
	GPIO149	
	GPIO150	
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	GPIO152	
GPIO153	GPIO154	
	GPIO155	
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	GPIO157	
	GPIO158	
	GPIO159	
	GPIO160	
	GPIO161	
	GPIO162	
	GPIO163	
GPIO164	GPIO165	
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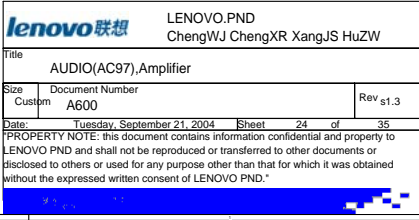


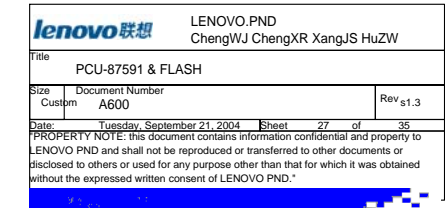


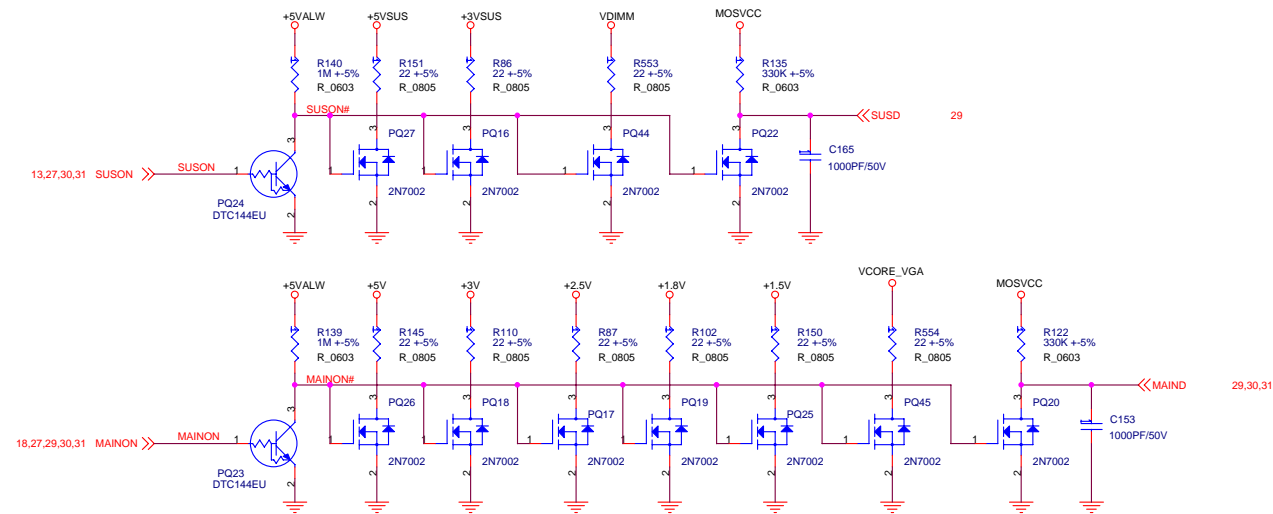
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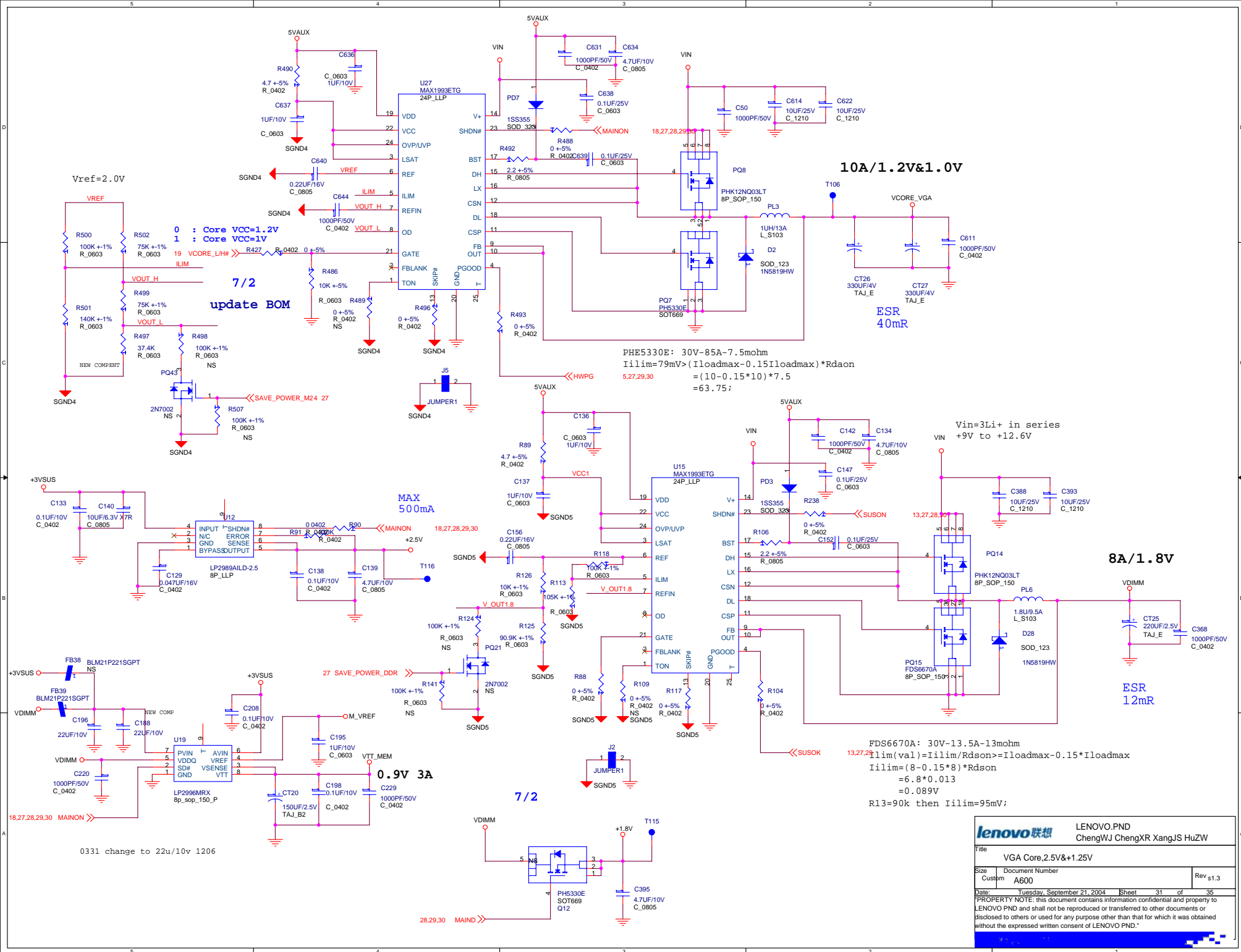
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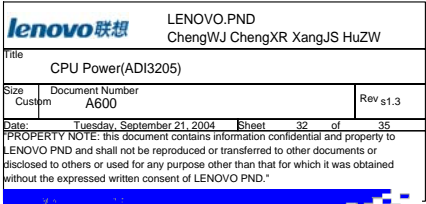
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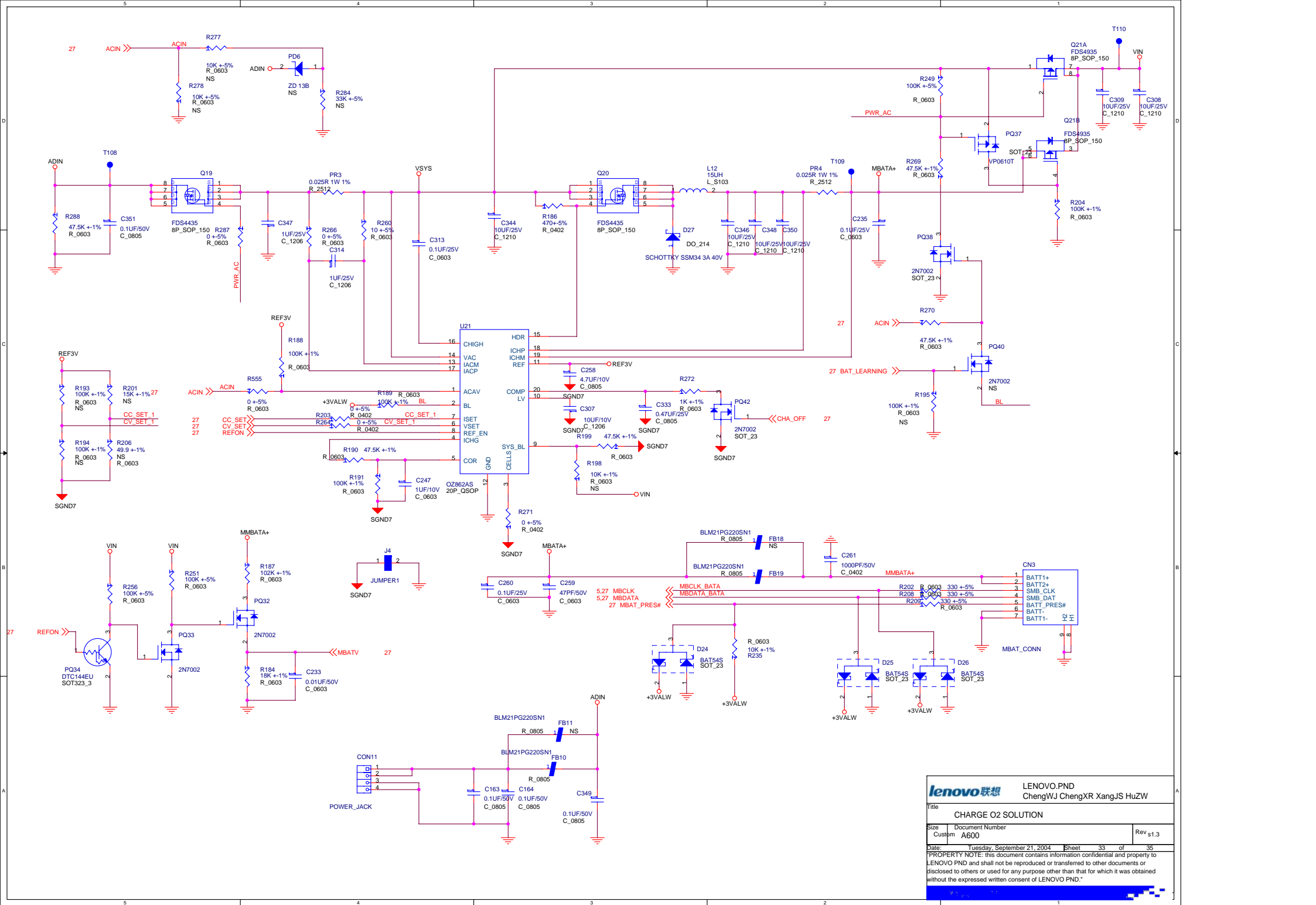


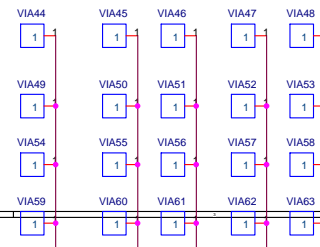
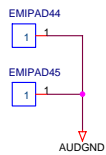
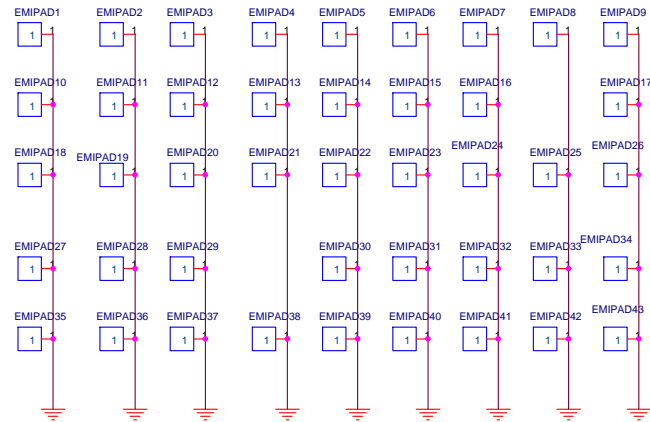
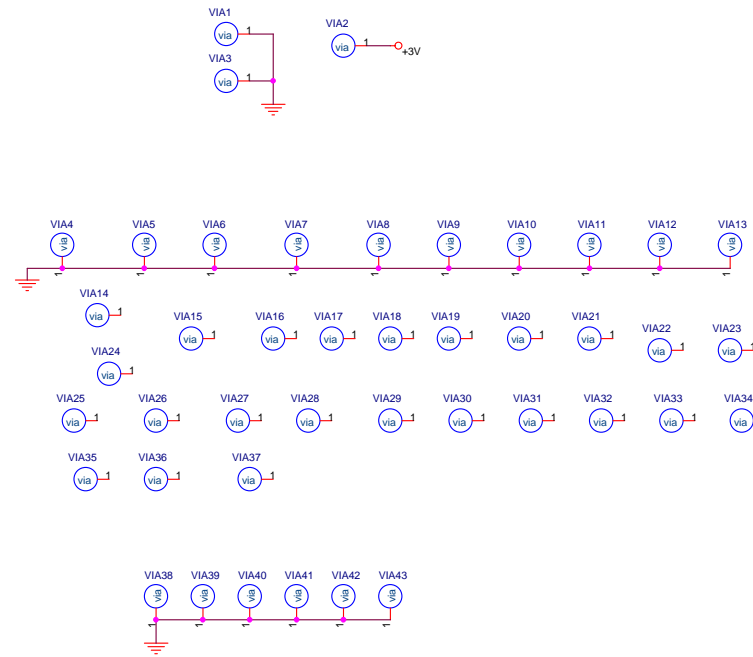
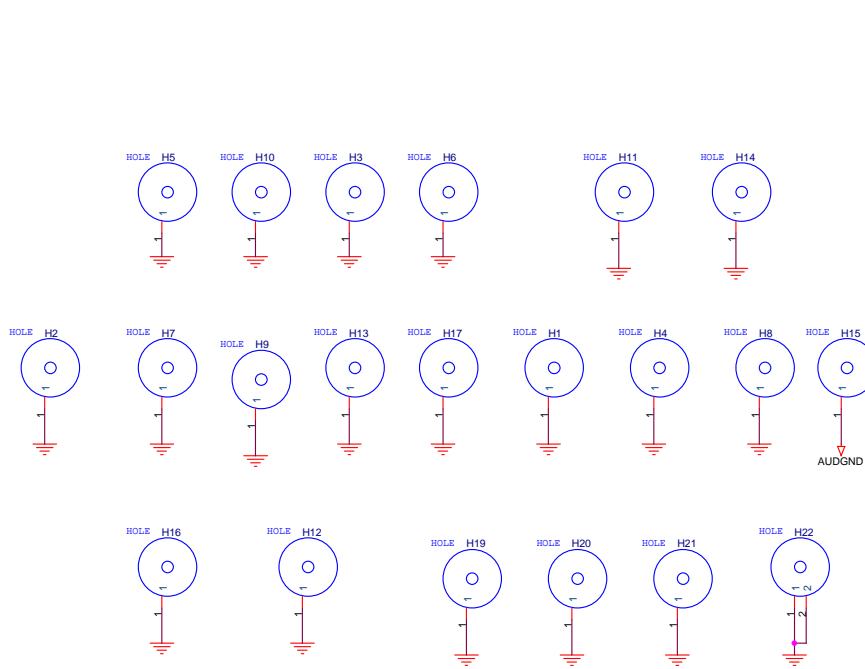












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