

Compal Confidential

Schematics Document

NIWE1

Arrandale

with Intel IBEX PEAK-M core logic

REV: 0.3

Security Classification	Compal Secret Data			<i>Compal Electronics, Ltd.</i>		
Issued Date	2008/03/25	Deciphered Date	2008/04/	Title	Cover Sheet	
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				Custom	LA-5751	0.3
Date: Thursday, October 29, 2009				Sheet	1	of 51

DDR3 Voltage Rails

power plane	+B	+5VALW +3VALW	+1.5V	+5VS
				+3VS
State				+1.5VS
				+VCCP
				+CPU_CORE
				+VGA_CORE
				+1.8VS
				+0.75VS
				+1.05VS
S0	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

SMBUS Control Table

	SOURCE	RAM M2	BATT	KE926	SODIMM	CLK CHIP	WLAN WWAN	N10x Thermal Sensor	N10x	Cap sensor board	NEW CARD	PCH
SMB_EC_CK1	KB926	X	V	X	X	X	X	X	X	X	X	X
SMB_EC_DA1	+3VALW		+3VALW									
SMB_EC_CK2	KB926	X	X	X	X	X	X	X	X	X	X	V
SMB_EC_DA2	+3VALW											+3VALW
SMBCLK	PCH	V	X	X	V	V	X	X	X	X	V	X
SMBDATA	+3VALW	+3VALW			+3VS	+3VS					+3VS	
SML0CLK	PCH	X	X	X	X	X	X	X	X	X	X	X
SML0DATA	+3VALW											
SML1CLK	PCH	X	X	V	X	X	X	V	X	V	X	X
SML1DATA	+3VALW			+3VALW				+3VS		+3VS		

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

@ FUNCTION

Structure	Description	NON-USE
45@	45 BOM	
BT@	Blue Tooth function	
3G@	3G function (WWAN)	
CAP@	CAP Sensor function	
CMOS@	CMOS CAMERA function	
ESATA@	E-SATA function	
HDMI@	HDMI function (UMA or DIS)	
UMA HDMI@	HDMI function (UMA only)	
X76@	X76 BOM	
100@	10/100 LAN function	
GIGA@	GIGA LAN function	
UMA@	UMA only (Arrandale)	
DIS@	DIS only (Arrandale)	

SKU

Arrandale (dGPU) DIS only	DIS@
Arrandale (iGPU) UMA only	UMA@

PORT	DEVICE
1	
2	WLAN
3	LAN
4	3G
5	NEW CARD
6	
7	
8	

PORT	DEVICE
0	RIGHT SIDE
1	LEFT SIDE
2	CMOS
3	LEFT SIDE
4	RIGHT SIDE
5	CARD READER
6	
7	
8	WIRELESS
9	
10	NEW CARD
11	BT
12	
13	3G

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				Size	Document Number	Rev
				LA-5751		
				Date: Thursday, October 29, 2009 Sheet 3 of 51		

VGA and DDR3 Voltage Rails (N11x GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	N/A	N/A	
GPIO1	IN	-	Hot plug detect for IFP link C
GPIO2	OUT	H	Panel Back-Light brightness(PWM capable)
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light On/Off (PWM)
GPIO5	OUT	-	GPU VID0
GPIO6	OUT	-	GPU VID1
GPIO7	OUT	N/A	
GPIO8	I/O	N/A	
GPIO9	OUT	N/A	
GPIO10	OUT	N/A	
GPIO11	I/O	-	Reserve 10K pull low.
GPIO12	IN	N/A	
GPIO13	OUT	N/A	
GPIO14	OUT	-	Reserve 10K pull low.
GPIO15	IN	N/A	
GPIO16	OUT	N/A	
GPIO17	IN	-	PAD
GPIO18	IN	N/A	
GPIO19	IN	N/A	

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

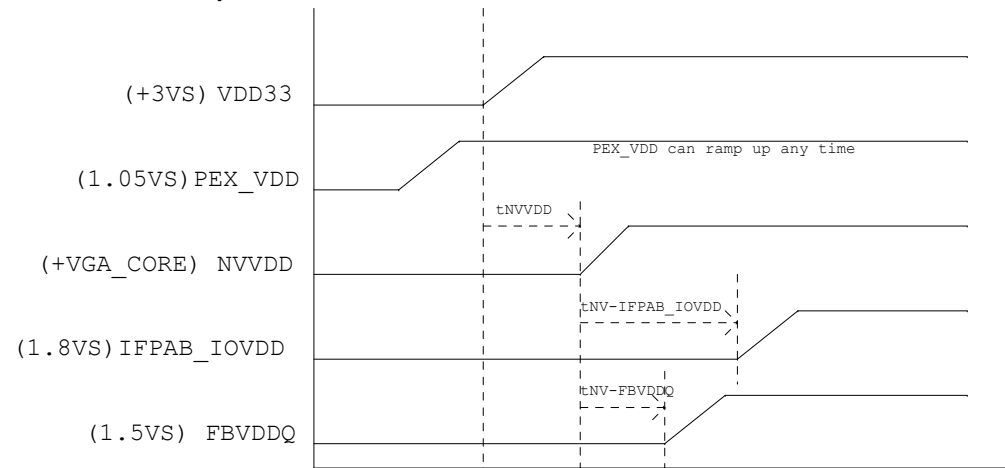
Products	GPU (4)	Mem (1,5)	NVCLK /MCLK	NVVDD		FBVDD (1.5V)		FBVDDQ (GPU+Mem) (1.5V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.8V)		I/O and PLLVDD (1.05V)		Other (3.3V)		
	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N11M-GE1 64bit 512MB DDR3	14.02	2.16	TBD	TBD	12.9	12.26	0.66	0.99	1.3	1.95	530	0.56	84	0.15	140	0.15	38	0.13

GPIO5 GPIO6

		Device ID	GPU_VID0	GPU_VID1	VGA_CORE	P-State
			0	0	0.8V	Deep P12
			0	1	0.85V	P8
			1	1	1.03V	P0

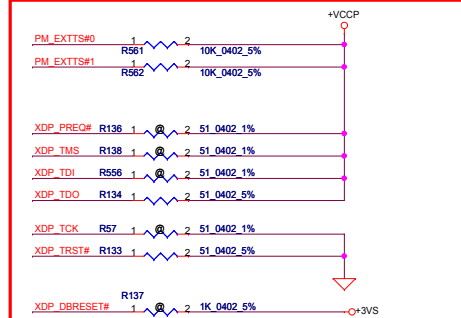
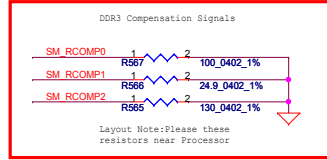
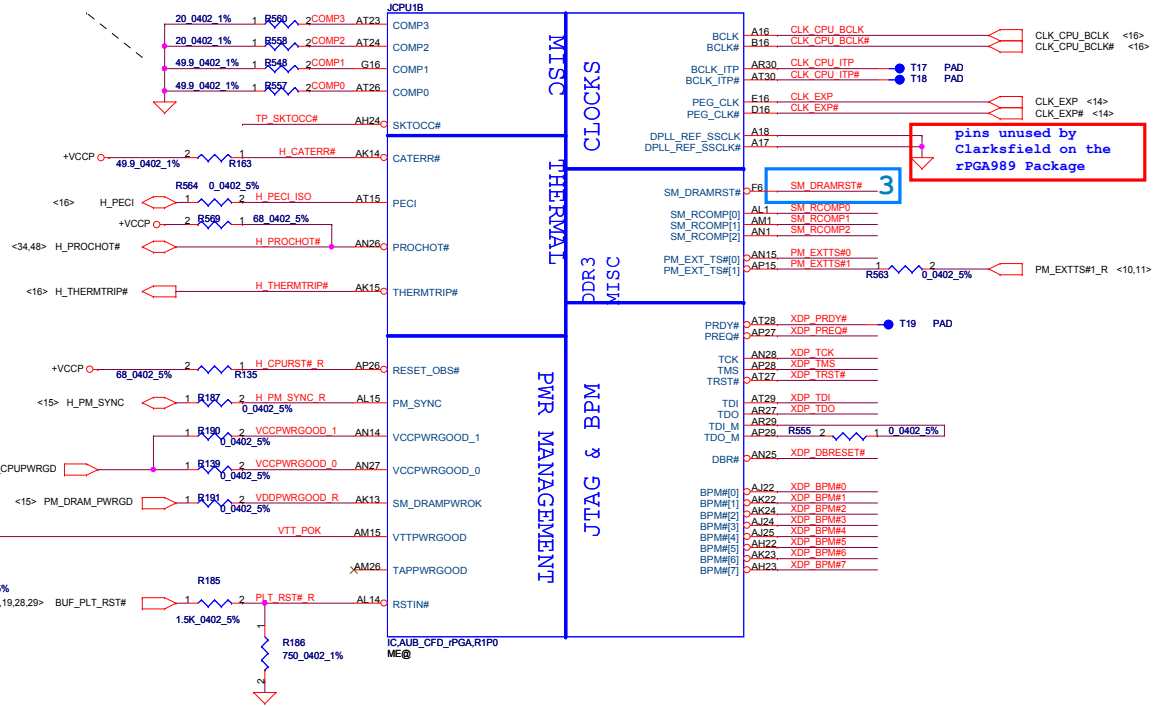
Power Sequence

The ramp time for any rail must be more than 40us

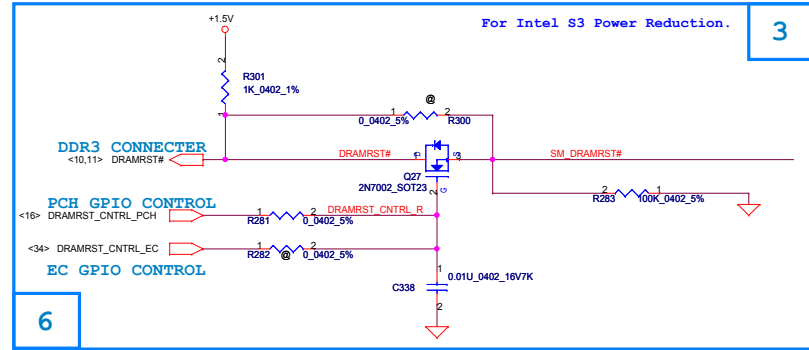
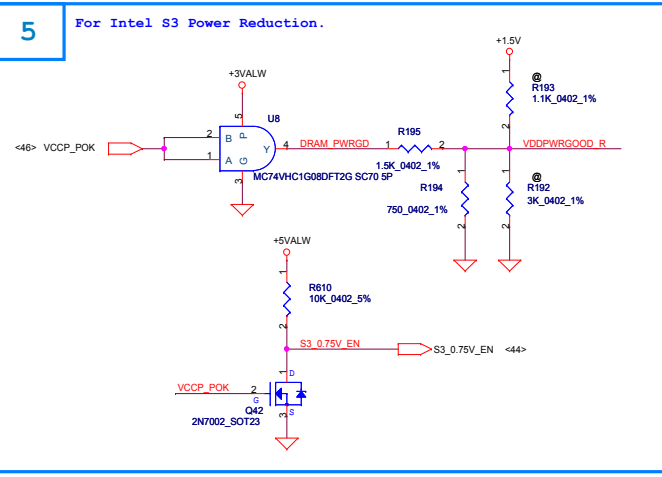
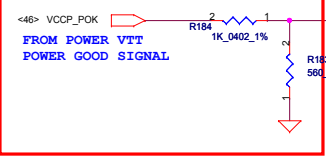


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				Size	Document Number	Rev
				LA-5751 0.3		
				Date: Thursday, October 29, 2009 Sheet 4 of 51		

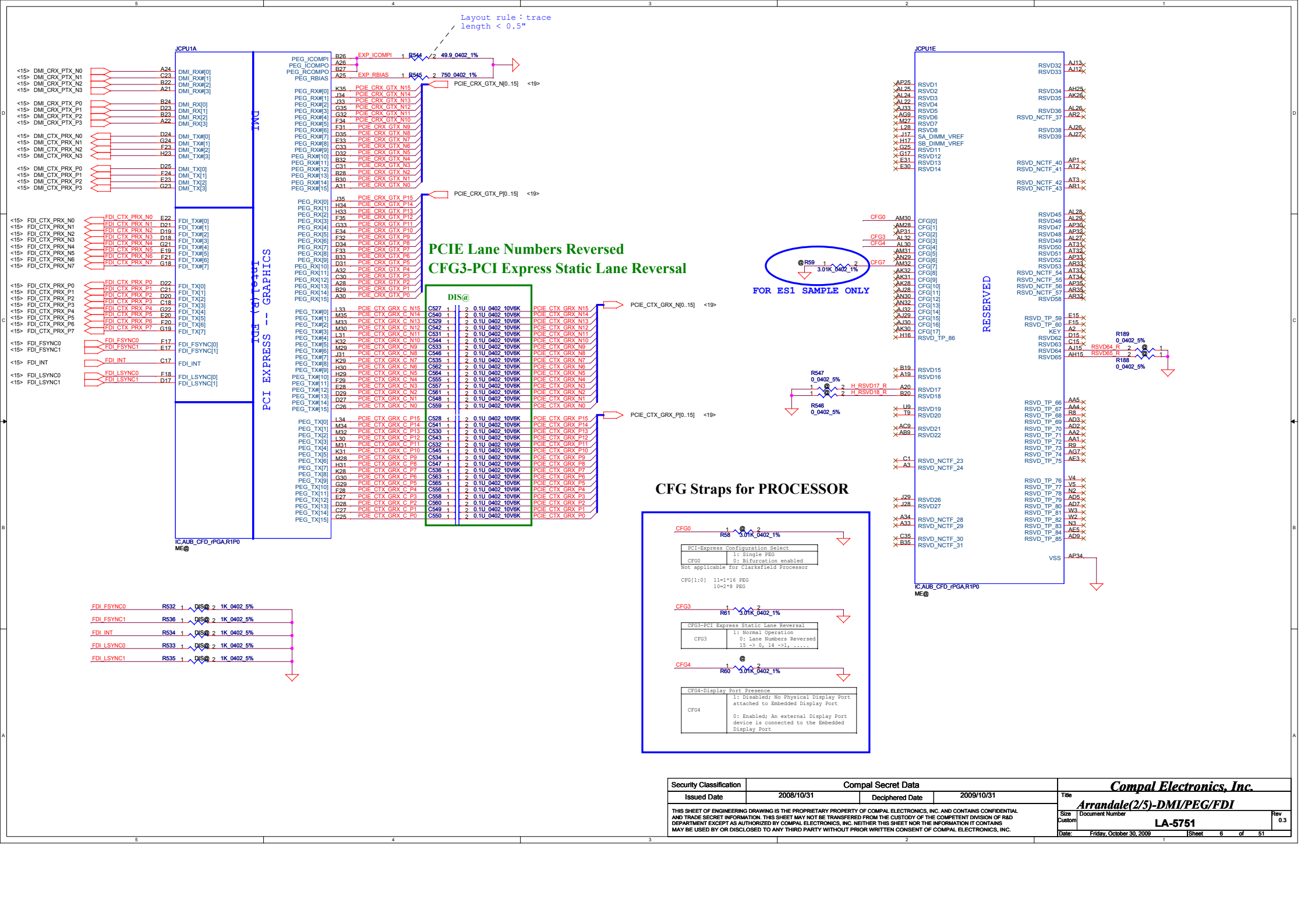
Layout rule: 10mil width trace
length < 0.5", spacing 20mil



**CHECK INTEL DOCUMENT #385422
Debug Port Design Guide Rev1.3**



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Custom	LA-5751	0.3	Date:	Friday, October 30, 2009	Sheet 5 of 51



Layout rule : trace length < 0.5"

**PCIE Lane Numbers Reversed
CFG3-PCI Express Static Lane Reversal**

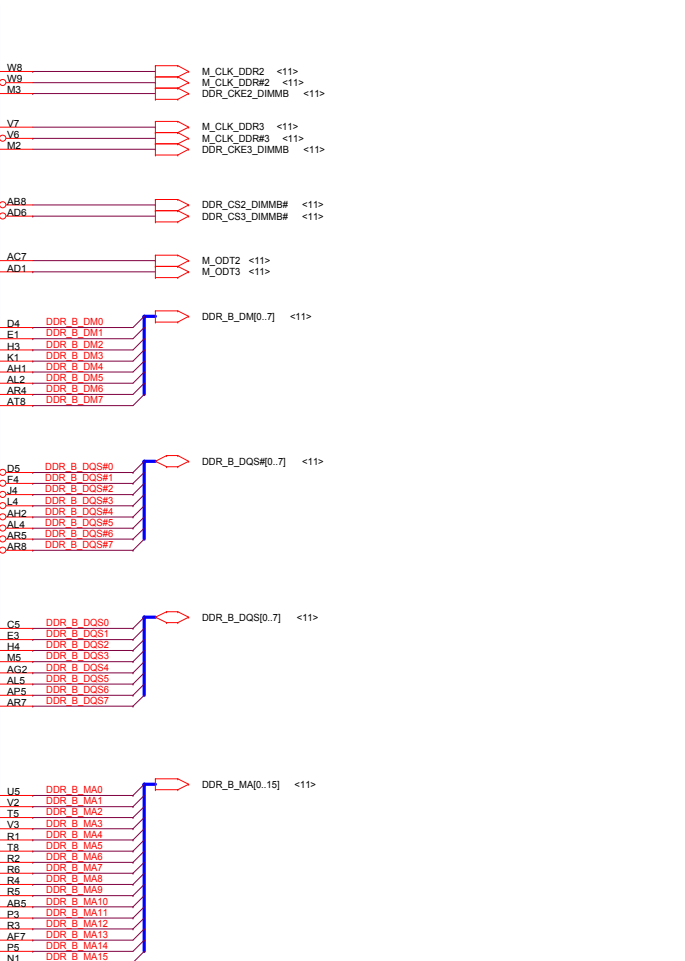
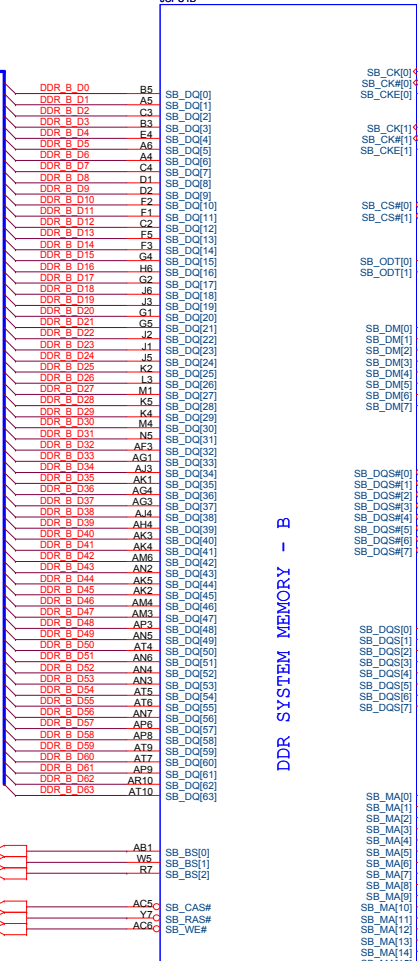
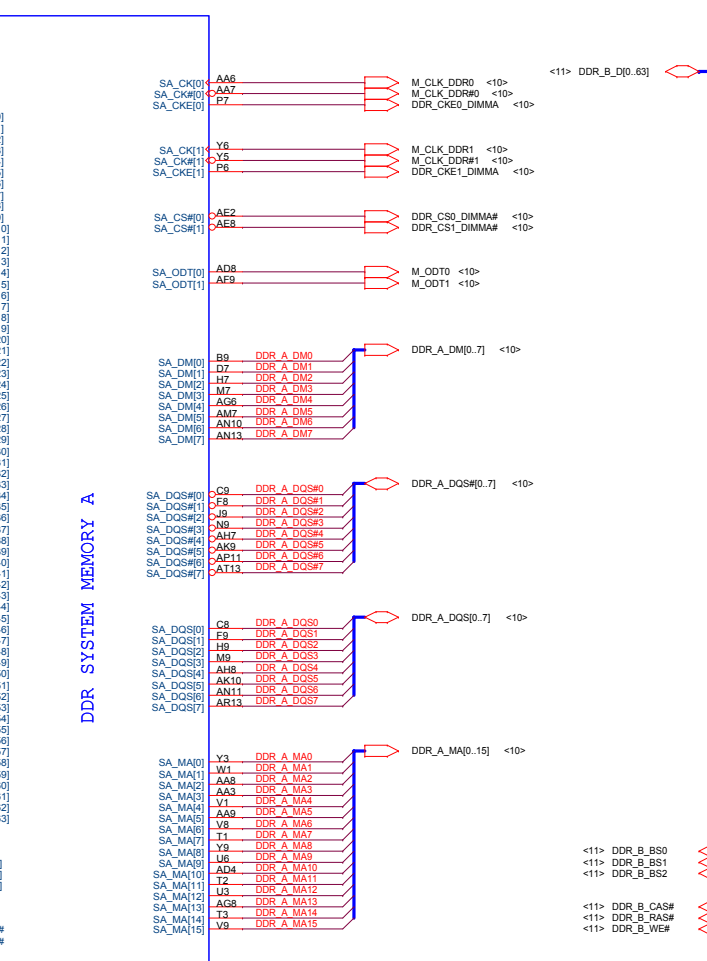
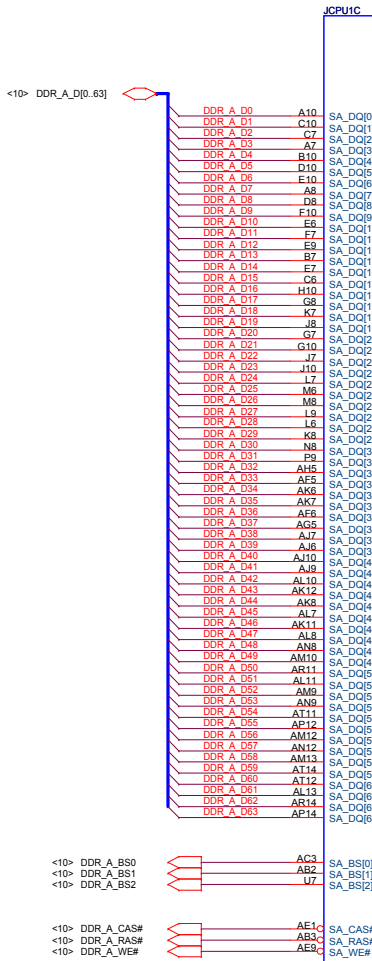
FOR ES1 SAMPLE ONLY

CFG Straps for PROCESSOR

CFG0	1	2	3.01K_0402_1%
PCI-Express Configuration Select CFG0 0: Bifurcation enabled Not applicable for Clarksfield Processor CFG[1:0] 11=1*16 PEG 10=2*8 PEG			
CFG3	1	2	3.01K_0402_1%
CFG3-PCI Express Static Lane Reversal CFG3 1: Normal Operation 0: Lane Numbers Reversed 15 -> 0, 14 -> 15,			
CFG4	1	2	3.01K_0402_1%
CFG4-Display Port Presence 1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port.			

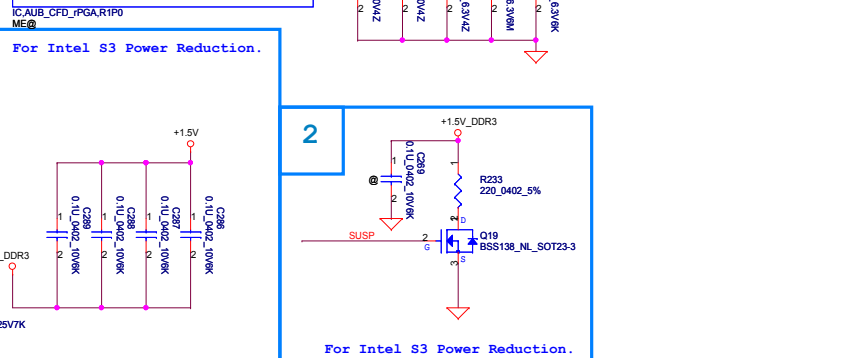
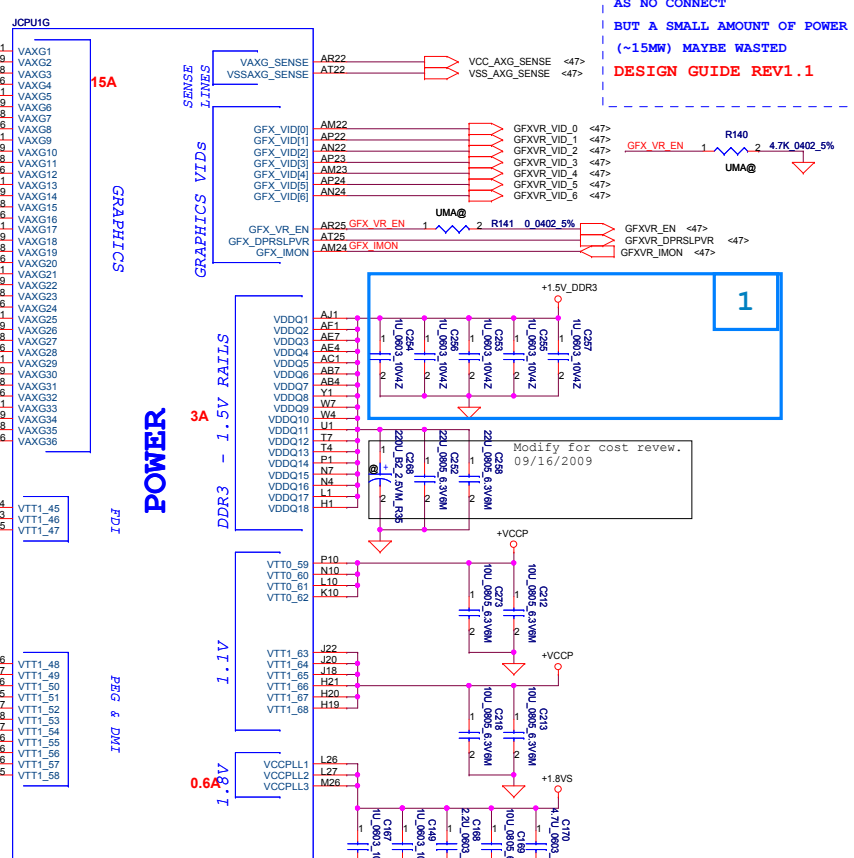
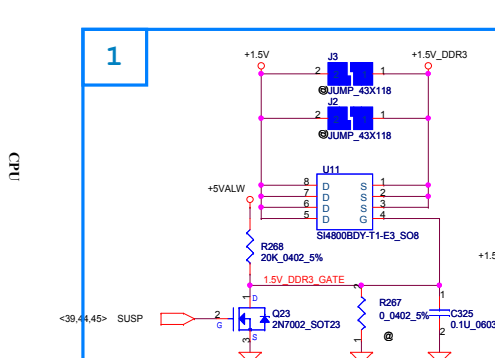
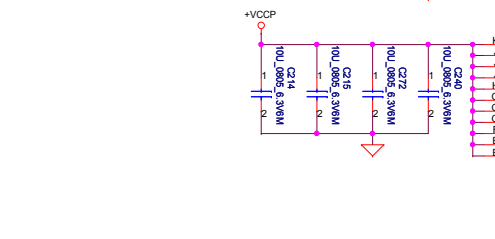
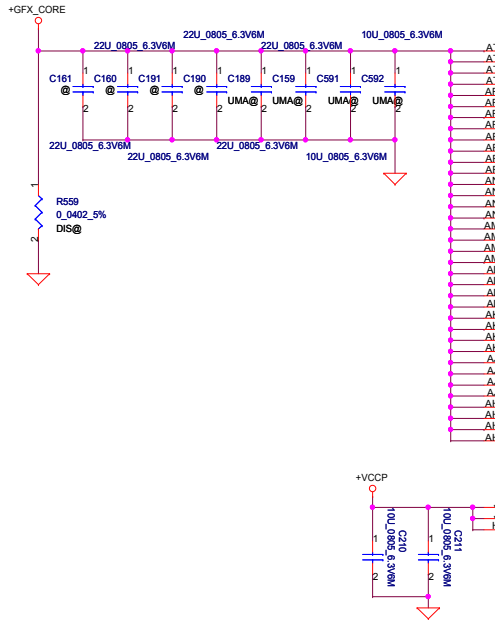
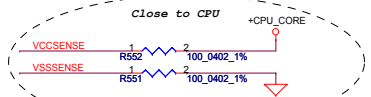
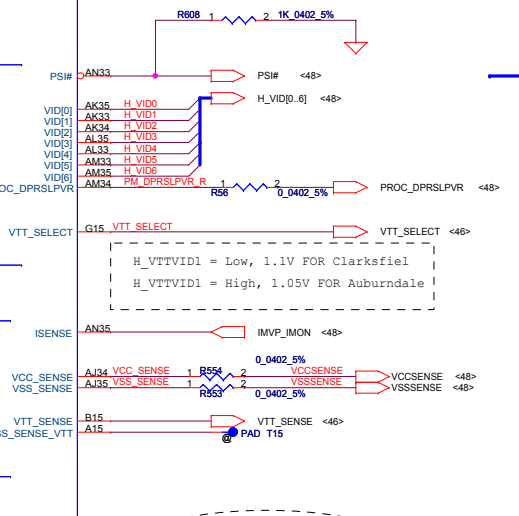
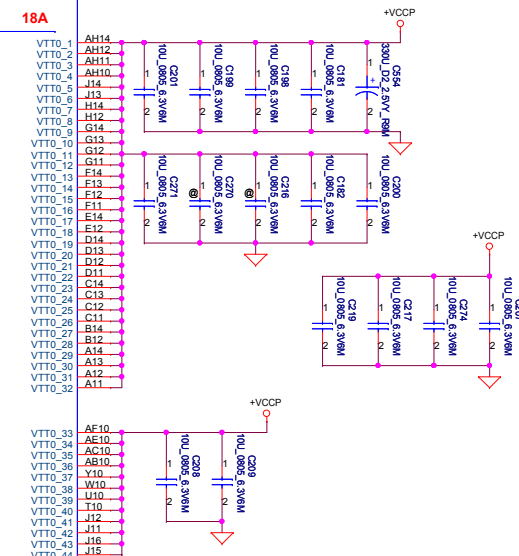
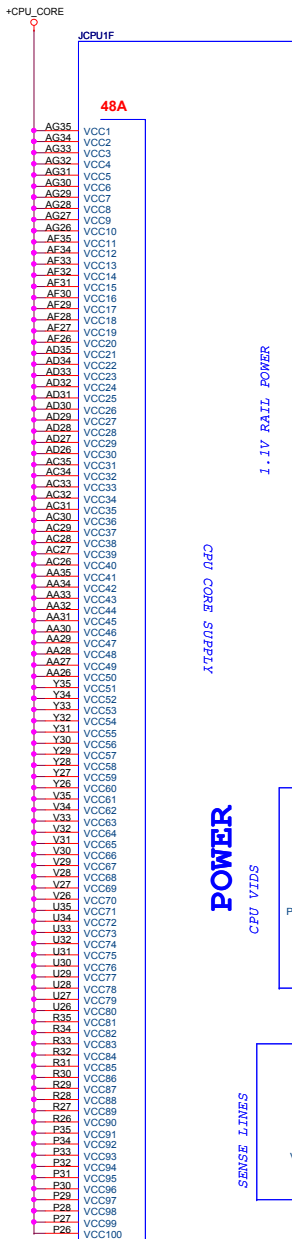
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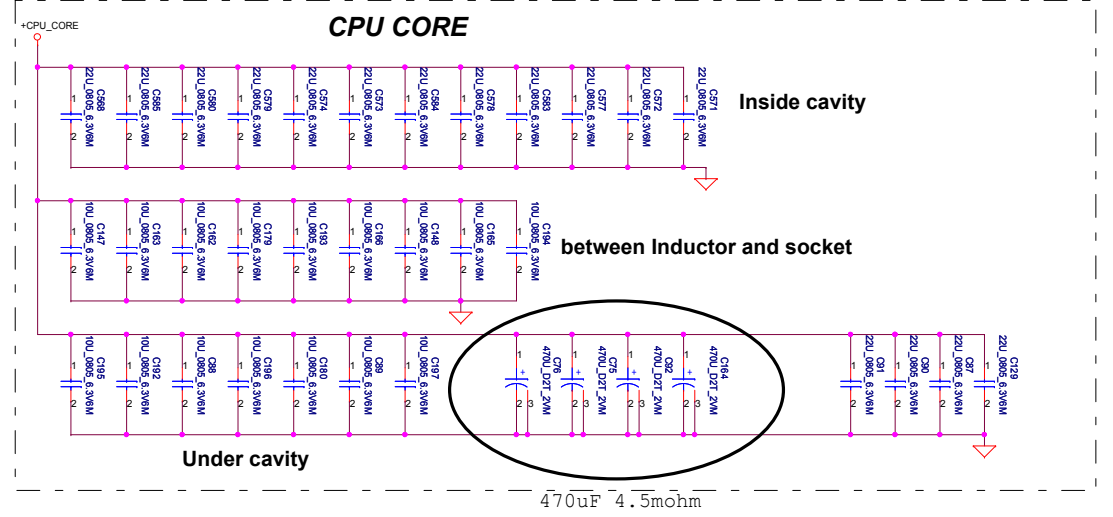
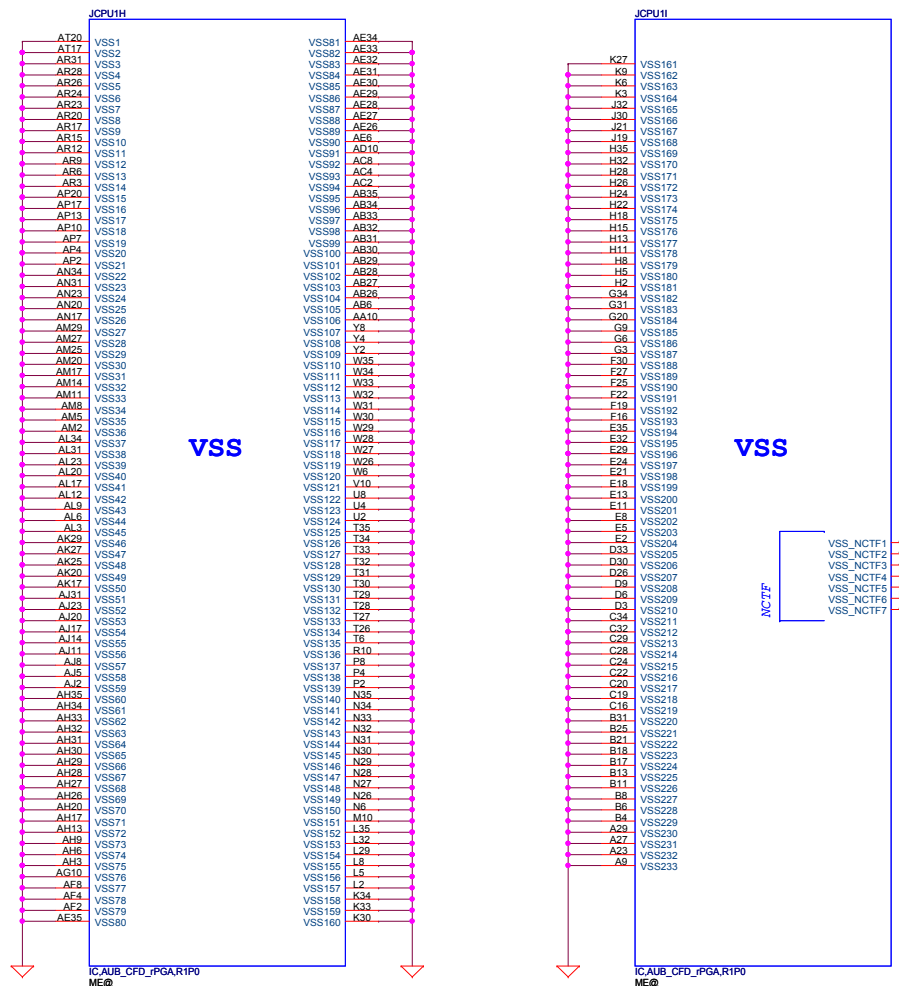
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Size			Arrandale(3/5)-DDR III	
Custom			Document Number	
Date			LA-5751	
Date			Friday, October 30, 2008	
Sheet			7 of 51	



AS NO CONNECT
BUT A SMALL AMOUNT OF POWER
(~15MW) MAYBE WASTED
DESIGN GUIDE REV1.1

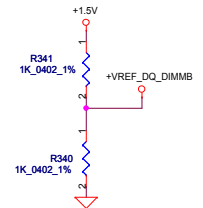
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Size	Document Number	Rev	LA-5751		
Customer	LA-5751	0.3	Date: Friday, October 30, 2009 Sheet 8 of 51		



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Size Custom	Document Number LA-5751	Date Thursday, October 29, 2009	Sheet 9	of 51

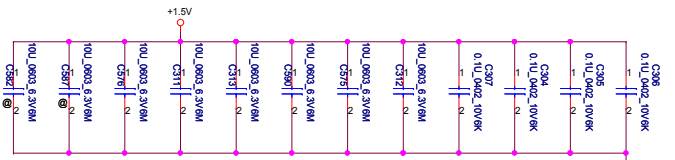


- <7> DDR_B_DQS#0..7
- <7> DDR_B_D[0..63]
- <7> DDR_B_DM[0..7]
- <7> DDR_B_DQS#0..7
- <7> DDR_B_MA[0..15]



For Arranale only +VREF_DQ_DIMMB supply from a external 1.5V voltage divide circuit.
07/17/2009

Layout Note:
Place near DIMM



Layout Note:
Place near DIMM



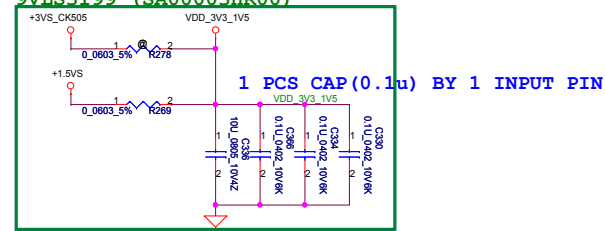
VDDQ (1.5V) =
3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMS)
6*0603 10uf (PER CONNECTOR)

VTT (0.75V) =
3*0805 10uf 4*0402 1uf

VDDSPD (3.3V) =
1*0402 0.1uf 1*0402 2.2uf

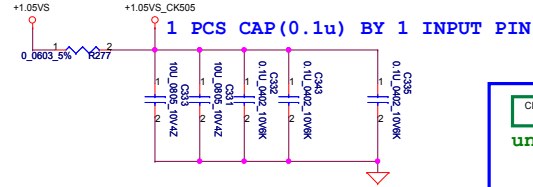
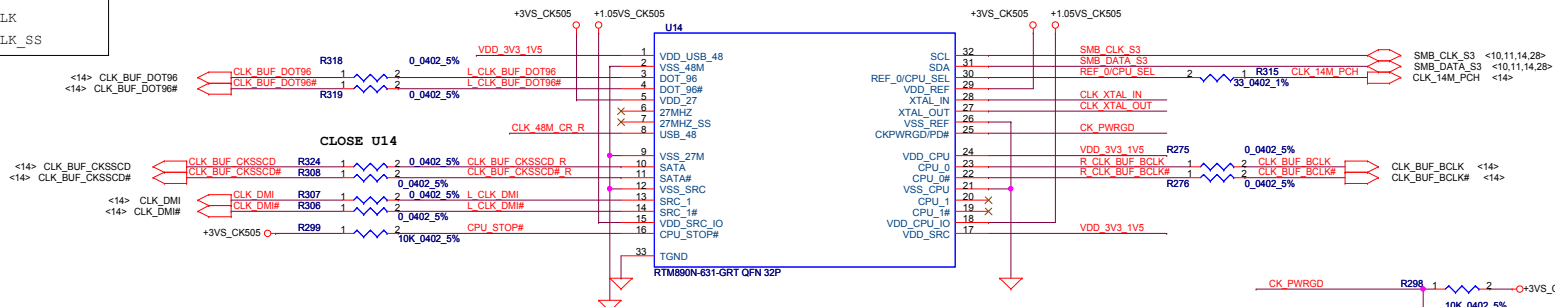
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				LA-5751
				Rev 0.3
Date: Friday, October 30, 2009				Sheet 11 of 51

Reserve for Low Power CLK GEN.
 RTM890N-631 (SA00003HQ00)
 SLG8LV597VTR
 9VLS3199 (SA00003HR00)

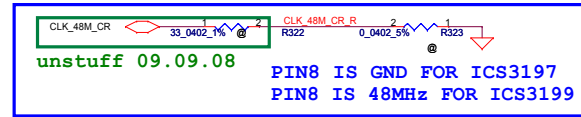


- CLK GEN TO PCH**
1. CLK_DMI
 2. CLK_BUF_BCLK
 3. CLK_BUF_CKSSCD
 4. CLK_BUF_DOT96
 5. CLK_14M_PCH

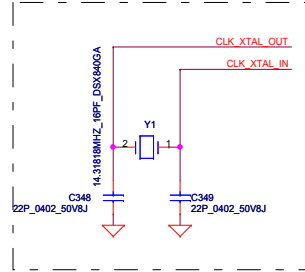
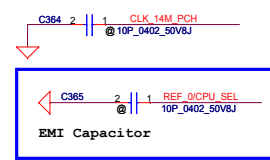
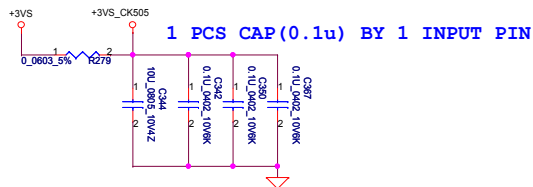
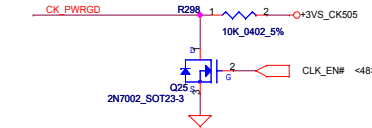
- CLK GEN TO VGA**
 Unused
1. 27M_CLK
 1. 27M_CLK_SS



S IC SLG8SP587VTR QFN 32P CLK GEN (SA00002XY00)
 S IC ICS9LRS3199AKLFT MLF 32P CLK GEN (SA000030P00)

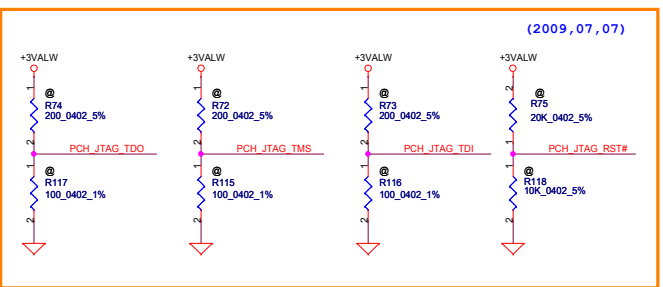
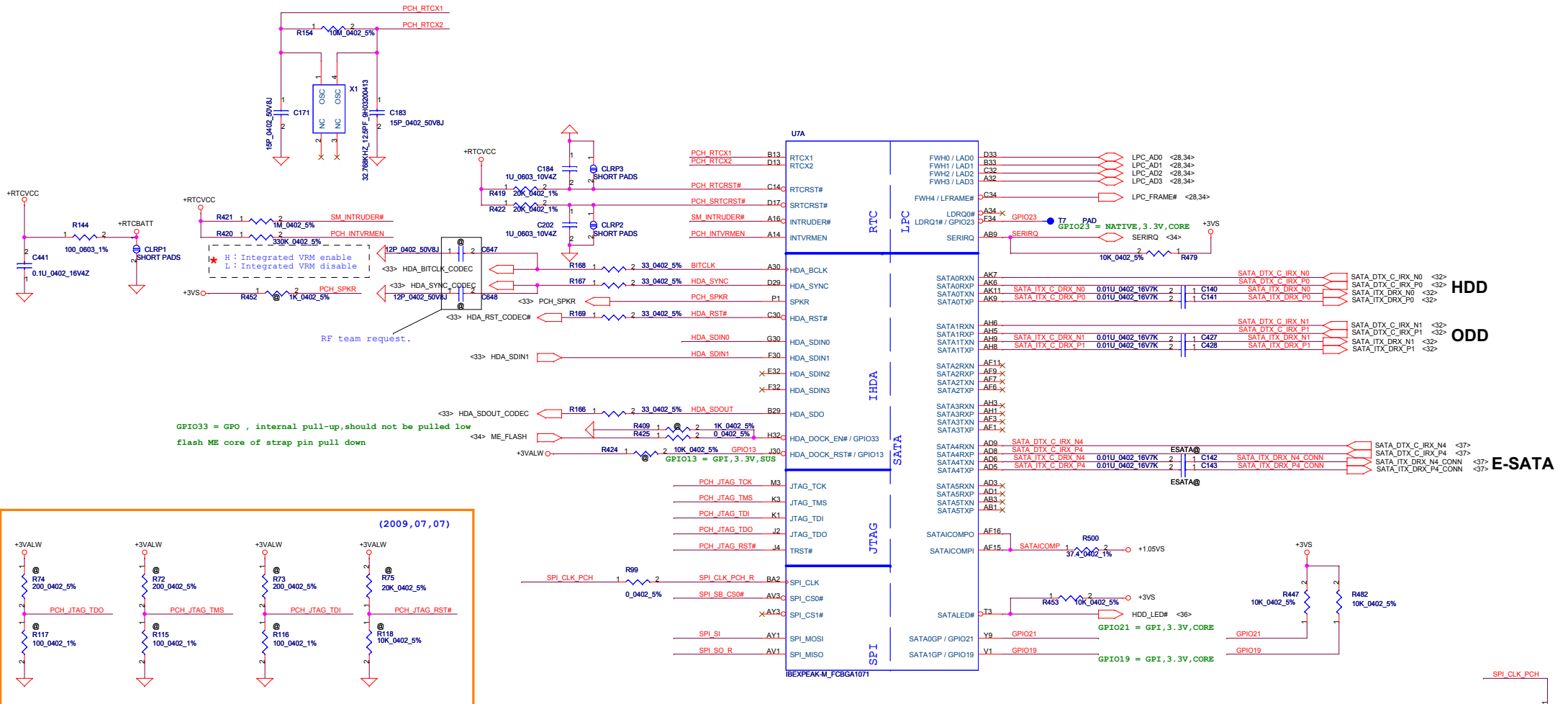


CLK_48M_CR 33_0402_1% 2
 CLK_48M_CR R R322 0_0402_5% 1
 unstuff 09.09.08
 PIN8 IS GND FOR ICS3197
 PIN8 IS 48MHz FOR ICS3199



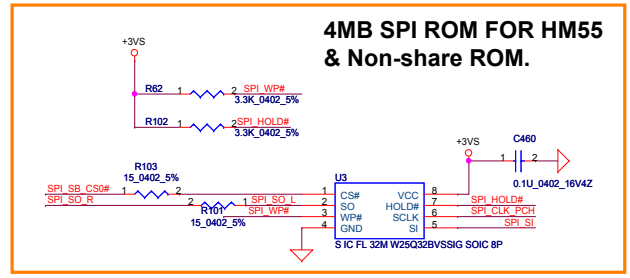
PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

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Date:	Friday, October 30, 2008	Sheet	12 of 51



PCH_JTAG_TCK R114 1 2 51 0402 5% (2009, 05, 04)
FOR INTEL DPGD REV1.6 (MAY 2009)

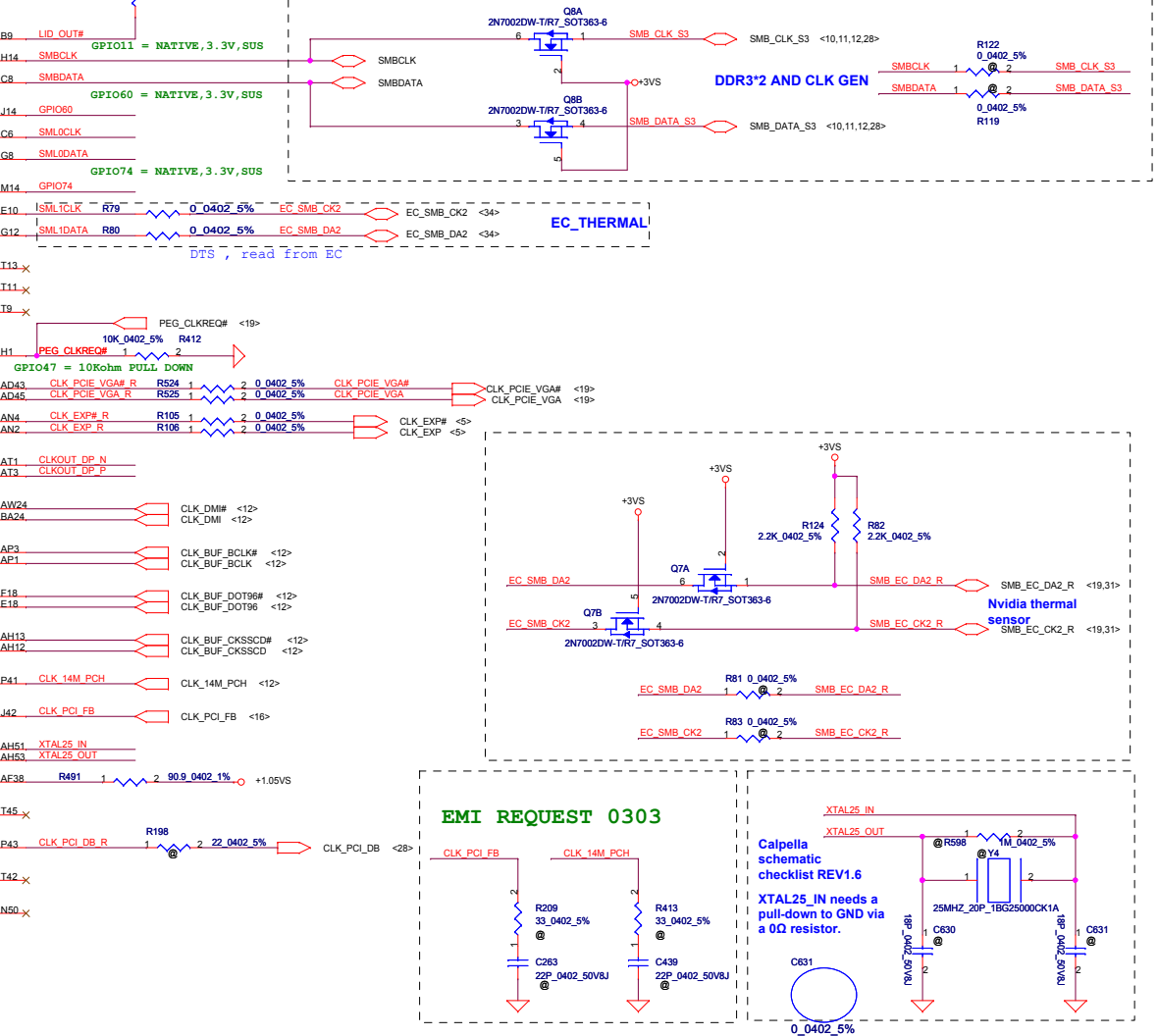
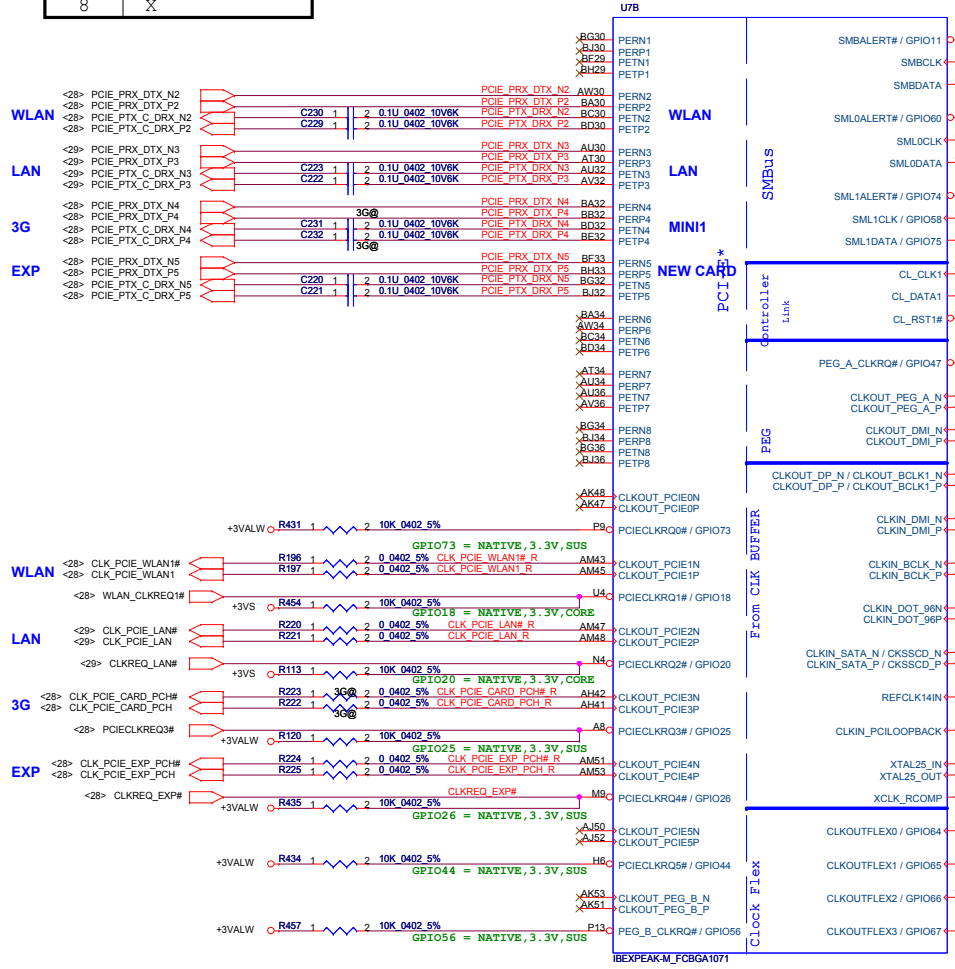
PCH Pin	RefDes	PCH JTAG Pre-Production		PCH JTAG Production
		ES1	ES2	MP
PCH_JTAG_TDO	R591	No Install	200ohm	No Install
	R590	No Install	100ohm	No Install
PCH_JTAG_TMS	R584	200ohm	200ohm	No Install
	R583	100ohm	100ohm	No Install
PCH_JTAG_TDI	R587	200ohm	200ohm	No Install
	R586	100ohm	100ohm	No Install
PCH_JTAG_TCK	R580	51ohm	51ohm	51ohm
	R595	20Kohm	20Kohm	No Install
PCH_JTAG_RST#	R594	10Kohm	10Kohm	No Install



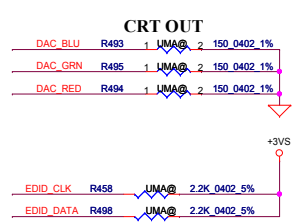
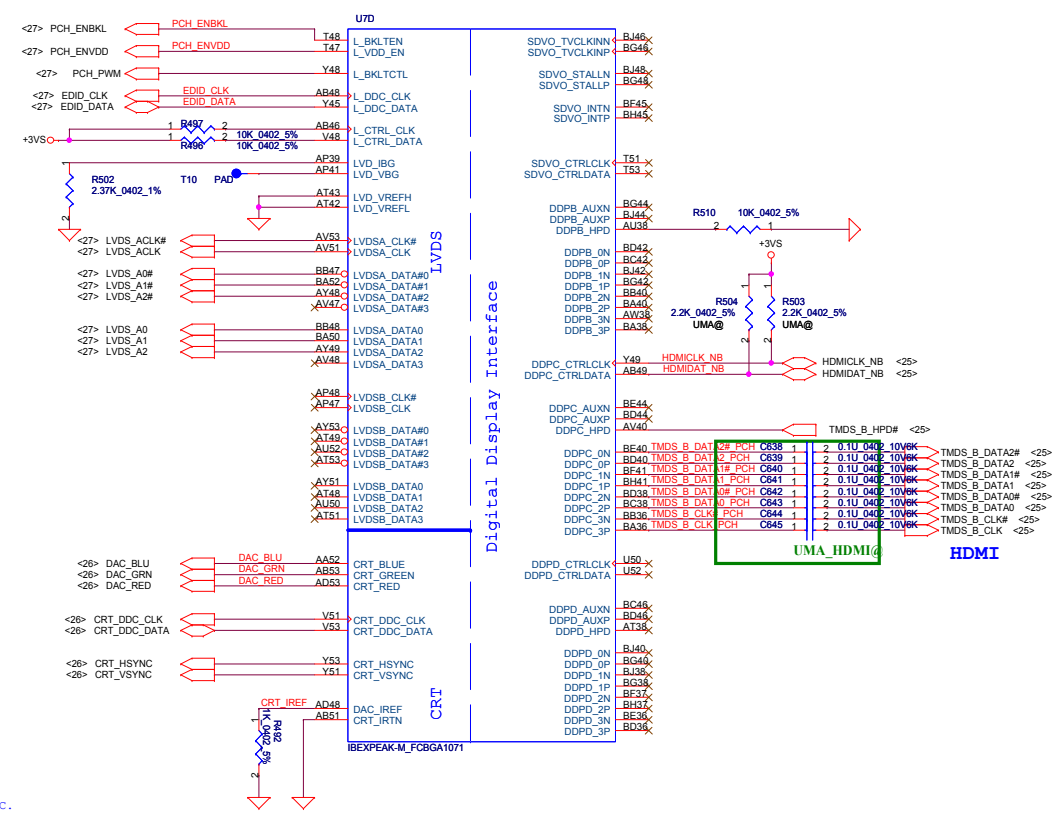
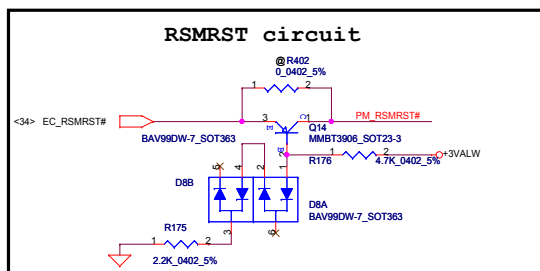
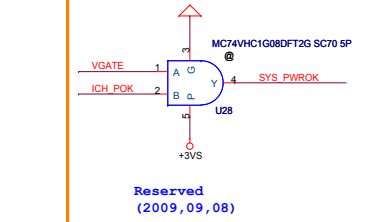
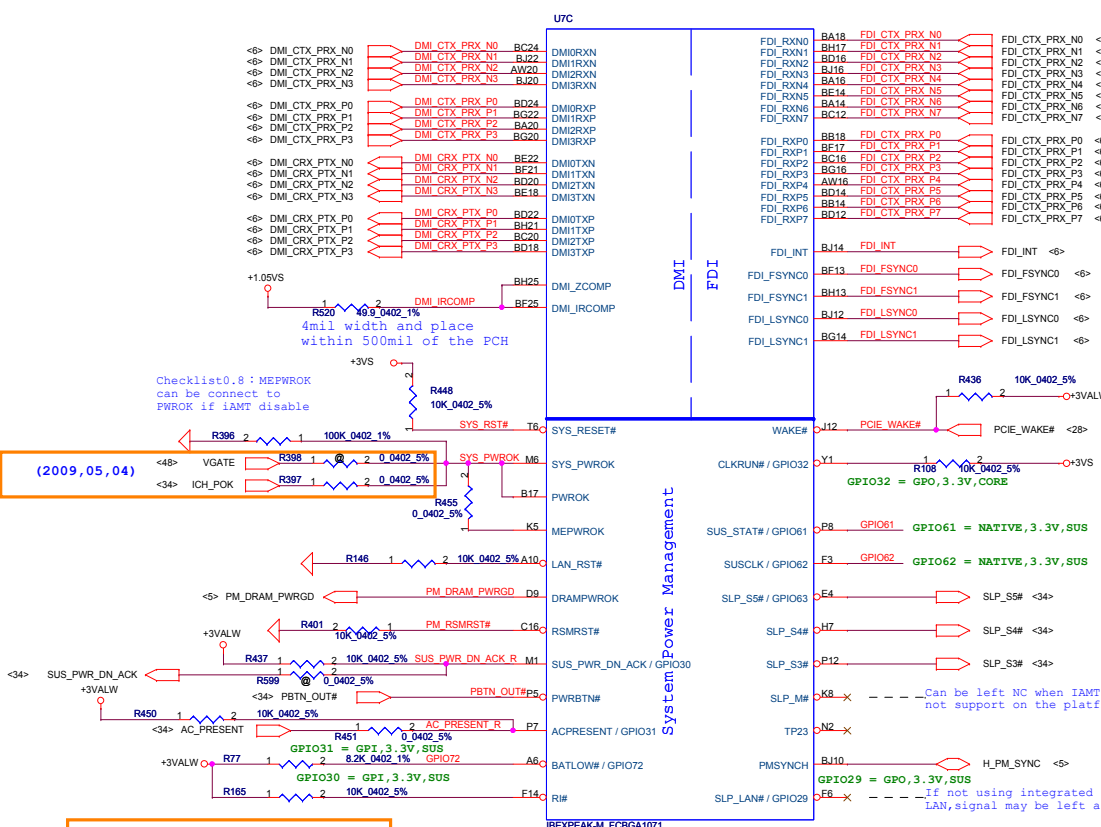
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Issued Date	2008/10/31	Deciphered Date	
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Site Custom	Document Number	Rev	
	LA-5751	0.3	
Date:	Friday, October 30, 2009	Sheet	13 of 51

HDD
ODD
E-SATA

PCIe PORT LIST	
PORT	DEVICE
1	X
2	WLAN
3	LAN
4	3G
5	NEW CARD
6	X
7	X
8	X

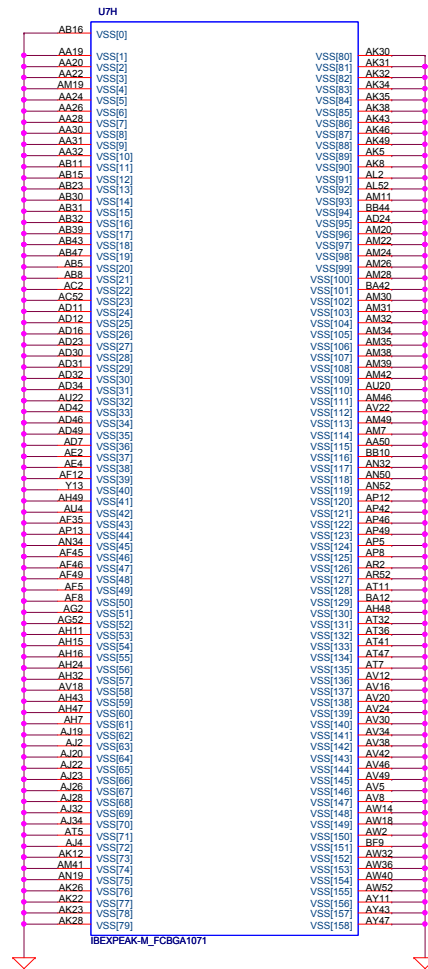
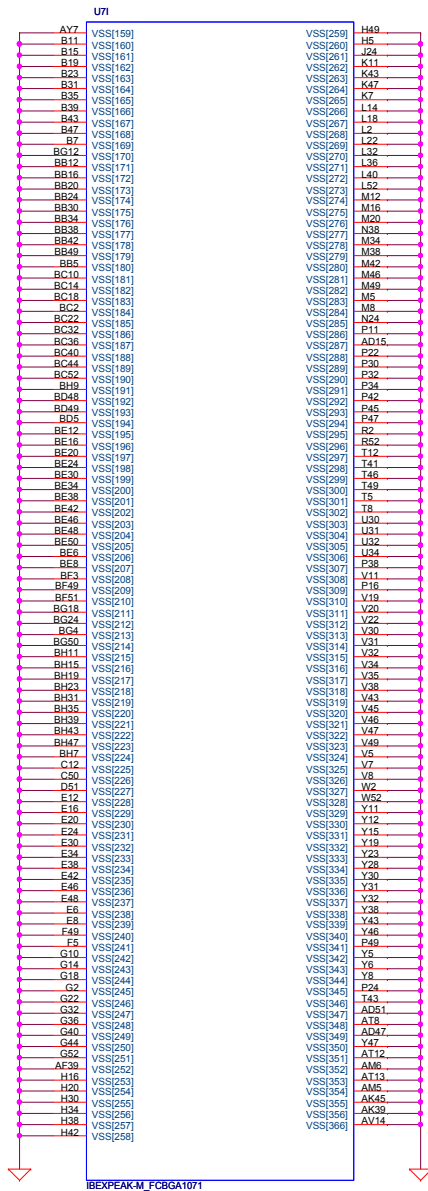


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			Customer	LA-5751	0.3
			Date	Friday, October 30, 2008	Sheet 14 of 51



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/10/31	Deciphered Date	2009/10/31	Title	
				IBEX-M(3/6)-DMI/GPIO/LVDS	
				Size	Document Number
				Customer	LA-5751
				Date	Friday, October 30, 2008
				Sheet	15 of 51

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Size	Customer	Date: Thursday, October 29, 2009		18 of 51
LA-5751				0.3

- <6> PCIE_CTX_GRX_N0..15] PCIE_CTX_GRX_N0..15]
- <6> PCIE_CTX_GRX_P0..15] PCIE_CTX_GRX_P0..15]
- <6> PCIE_CRX_GTX_N0..15] PCIE_CRX_GTX_N0..15]
- <6> PCIE_CRX_GTX_P0..15] PCIE_CRX_GTX_P0..15]

- PCIE_CTX_GRX_P0 AE12
- PCIE_CTX_GRX_N0 AE12
- PCIE_CTX_GRX_N1 AG12
- PCIE_CTX_GRX_P1 AE13
- PCIE_CTX_GRX_N1 AE13
- PCIE_CTX_GRX_P2 AE13
- PCIE_CTX_GRX_N2 AE13
- PCIE_CTX_GRX_P3 AE13
- PCIE_CTX_GRX_N3 AE13
- PCIE_CTX_GRX_P4 AG15
- PCIE_CTX_GRX_N4 AG16
- PCIE_CTX_GRX_P5 AF18
- PCIE_CTX_GRX_N5 AF18
- PCIE_CTX_GRX_P6 AE18
- PCIE_CTX_GRX_N6 AF18
- PCIE_CTX_GRX_P7 AG18
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- PCIE_CTX_GRX_P8 AF18
- PCIE_CTX_GRX_N8 AE19
- PCIE_CTX_GRX_P9 AE21
- PCIE_CTX_GRX_N9 AE21
- PCIE_CTX_GRX_P10 AG21
- PCIE_CTX_GRX_N10 AG22
- PCIE_CTX_GRX_P11 AF22
- PCIE_CTX_GRX_N11 AE22
- PCIE_CTX_GRX_P12 AE24
- PCIE_CTX_GRX_N12 AE24
- PCIE_CTX_GRX_P13 AG24
- PCIE_CTX_GRX_N13 AE24
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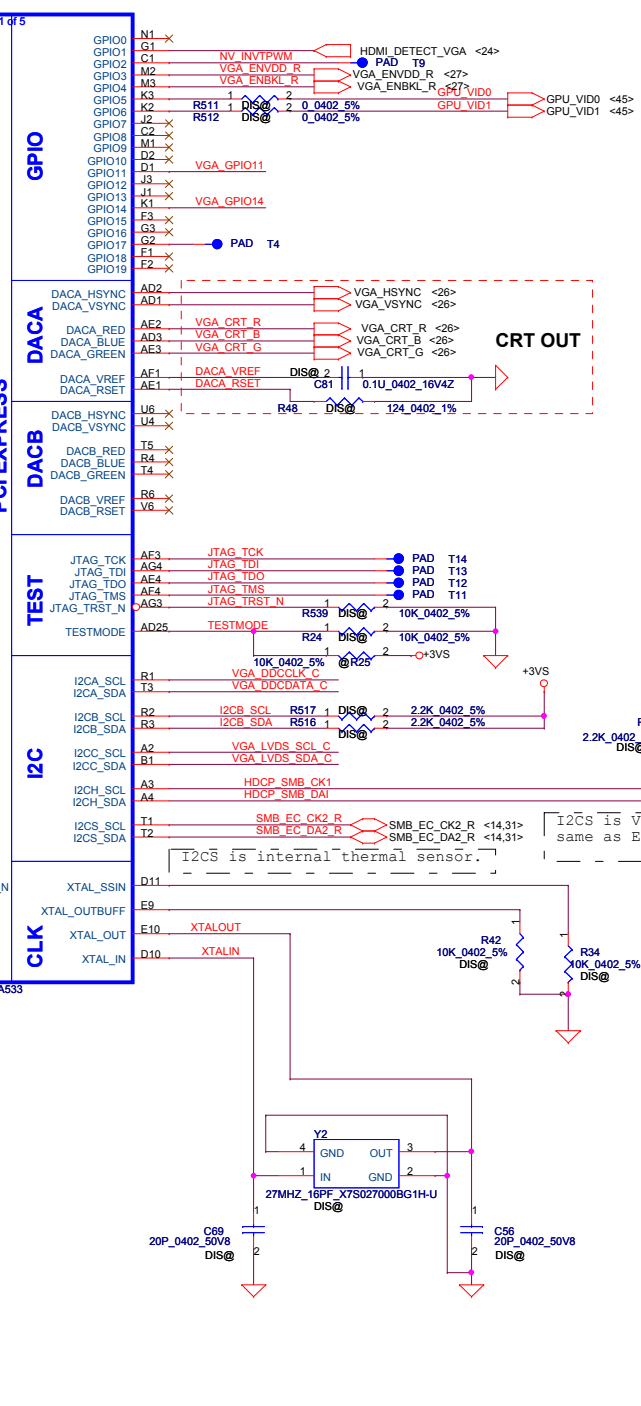
- PCIE_CRX_GTX_P0 C120 DIS@ 1 2 0.1U_0402_10V6K
- PCIE_CRX_GTX_N0 C119 DIS@ 1 2 0.1U_0402_10V6K
- PCIE_CRX_GTX_P1 C118 DIS@ 1 2 0.1U_0402_10V6K
- PCIE_CRX_GTX_N1 C117 DIS@ 1 2 0.1U_0402_10V6K
- PCIE_CRX_GTX_P2 C80 DIS@ 1 2 0.1U_0402_10V6K
- PCIE_CRX_GTX_N2 C79 DIS@ 1 2 0.1U_0402_10V6K
- PCIE_CRX_GTX_P3 C78 DIS@ 1 2 0.1U_0402_10V6K
- PCIE_CRX_GTX_N3 C77 DIS@ 1 2 0.1U_0402_10V6K
- PCIE_CRX_GTX_P4 C116 DIS@ 1 2 0.1U_0402_10V6K
- PCIE_CRX_GTX_N4 C115 DIS@ 1 2 0.1U_0402_10V6K
- PCIE_CRX_GTX_P5 C114 DIS@ 1 2 0.1U_0402_10V6K
- PCIE_CRX_GTX_N5 C113 DIS@ 1 2 0.1U_0402_10V6K
- PCIE_CRX_GTX_P6 C112 DIS@ 1 2 0.1U_0402_10V6K
- PCIE_CRX_GTX_N6 C111 DIS@ 1 2 0.1U_0402_10V6K
- PCIE_CRX_GTX_P7 C109 DIS@ 1 2 0.1U_0402_10V6K
- PCIE_CRX_GTX_N7 C108 DIS@ 1 2 0.1U_0402_10V6K
- PCIE_CRX_GTX_P8 C108 DIS@ 1 2 0.1U_0402_10V6K
- PCIE_CRX_GTX_N8 C107 DIS@ 1 2 0.1U_0402_10V6K
- PCIE_CRX_GTX_P9 C105 DIS@ 1 2 0.1U_0402_10V6K
- PCIE_CRX_GTX_N9 C106 DIS@ 1 2 0.1U_0402_10V6K
- PCIE_CRX_GTX_P10 C104 DIS@ 1 2 0.1U_0402_10V6K
- PCIE_CRX_GTX_N10 C103 DIS@ 1 2 0.1U_0402_10V6K
- PCIE_CRX_GTX_P11 C102 DIS@ 1 2 0.1U_0402_10V6K
- PCIE_CRX_GTX_N11 C101 DIS@ 1 2 0.1U_0402_10V6K
- PCIE_CRX_GTX_P12 C100 DIS@ 1 2 0.1U_0402_10V6K
- PCIE_CRX_GTX_N12 C99 DIS@ 1 2 0.1U_0402_10V6K
- PCIE_CRX_GTX_P13 C98 DIS@ 1 2 0.1U_0402_10V6K
- PCIE_CRX_GTX_N13 C97 DIS@ 1 2 0.1U_0402_10V6K
- PCIE_CRX_GTX_P14 C96 DIS@ 1 2 0.1U_0402_10V6K
- PCIE_CRX_GTX_N14 C95 DIS@ 1 2 0.1U_0402_10V6K
- PCIE_CRX_GTX_P15 C94 DIS@ 1 2 0.1U_0402_10V6K
- PCIE_CRX_GTX_N15 C93 DIS@ 1 2 0.1U_0402_10V6K

- <14> CLK_PCIE_VGA# CLK_PCIE_VGA#
- <14> CLK_PCIE_VGA# CLK_PCIE_VGA#
- PEX_RST_N
- PEX_CLKREQ_N
- PEX_TSTCLK_OUT
- PEX_TSTCLK_OUT_N
- PEX_TERM
- PEX_TEMP
- PEX_RST_N
- PEX_CLKREQ_N
- PEX_TSTCLK_OUT
- PEX_TSTCLK_OUT_N
- PEX_TERM
- PEX_TEMP



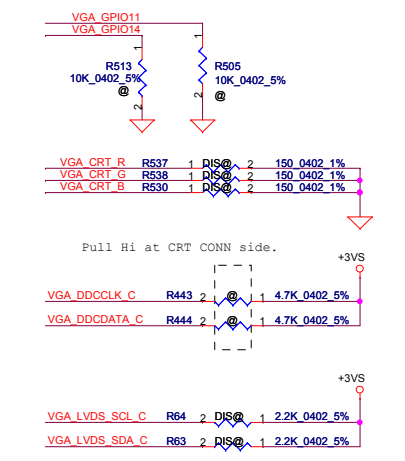
- PCIE_CRX_C_GTX_P0 AD10
- PCIE_CRX_C_GTX_N0 AD11
- PCIE_CRX_C_GTX_P1 AD12
- PCIE_CRX_C_GTX_N1 AC12
- PCIE_CRX_C_GTX_P2 AB11
- PCIE_CRX_C_GTX_N2 AB12
- PCIE_CRX_C_GTX_P3 AD13
- PCIE_CRX_C_GTX_N3 AC13
- PCIE_CRX_C_GTX_P4 AD15
- PCIE_CRX_C_GTX_N4 AC15
- PCIE_CRX_C_GTX_P5 AB14
- PCIE_CRX_C_GTX_N5 AB15
- PCIE_CRX_C_GTX_P6 AC16
- PCIE_CRX_C_GTX_N6 AD16
- PCIE_CRX_C_GTX_P7 AD17
- PCIE_CRX_C_GTX_N7 AD18
- PCIE_CRX_C_GTX_P8 AC18
- PCIE_CRX_C_GTX_N8 AB18
- PCIE_CRX_C_GTX_P9 AB19
- PCIE_CRX_C_GTX_N9 AB20
- PCIE_CRX_C_GTX_P10 AD19
- PCIE_CRX_C_GTX_N10 AD20
- PCIE_CRX_C_GTX_P11 AD21
- PCIE_CRX_C_GTX_N11 AC21
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- PCIE_CRX_C_GTX_N12 AB22
- PCIE_CRX_C_GTX_P13 AC22
- PCIE_CRX_C_GTX_N13 AD22
- PCIE_CRX_C_GTX_P14 AC23
- PCIE_CRX_C_GTX_N14 AD24
- PCIE_CRX_C_GTX_P15 AE25
- PCIE_CRX_C_GTX_N15 AE26

- CLK_PCIE_VGA#
- CLK_PCIE_VGA#
- PEX_REFCLK
- PEX_REFCLK_N
- PEX_TSTCLK_OUT
- PEX_TSTCLK_OUT_N
- PEX_TERM
- PEX_TEMP
- PEX_RST_N
- PEX_CLKREQ_N
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- PEX_TSTCLK_OUT_N
- PEX_TERM
- PEX_TEMP

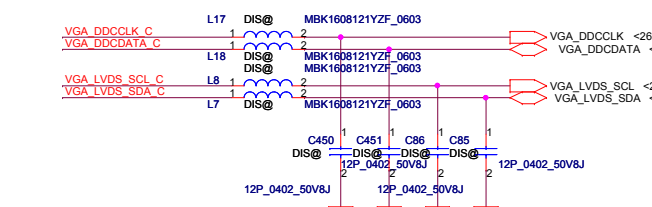


Device ID
0x0A7D

GPIO5	GPIO6	VGA_CORE	P-State
0	0	0.8V	Deep P12
0	1	0.85V	P8
1	1	1.03	P0



Removed external HDCP
07/17/2009

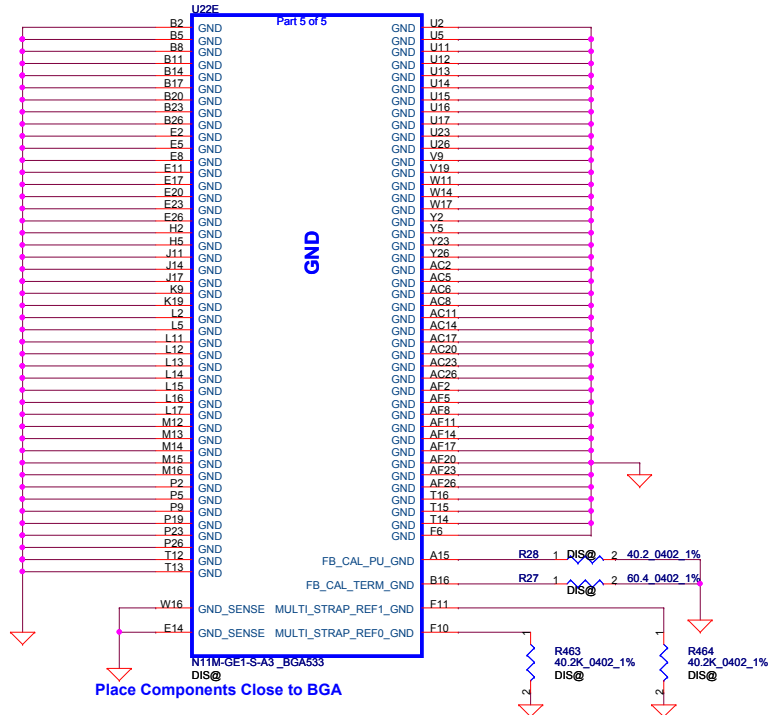


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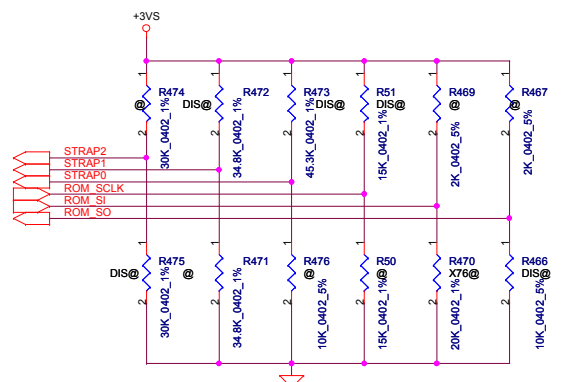
Compal Electronics, Inc.		
N11M-GE1 PCIE,GPIO,CLK		
Size B	Document Number	Rev 0.3
	LA-3751	
Date:	Friday, October 30, 2009	Sheet 19 of 51

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A total of 8 signals are required for GB1 strapping this includes
 2 reference signals
 6 physical strapping pins
 4 logical strapping bits
 A total of 24 logical strapping bits are available



<20> STRAP2
 <20> STRAP1
 <20> STRAP0
 <20> ROM_SCLK
 <20> ROM_SI
 <20> ROM_SO



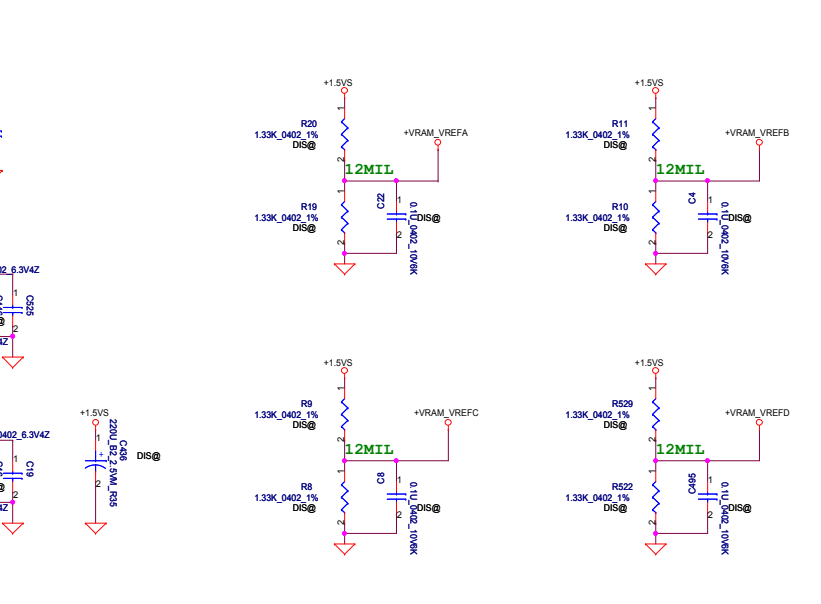
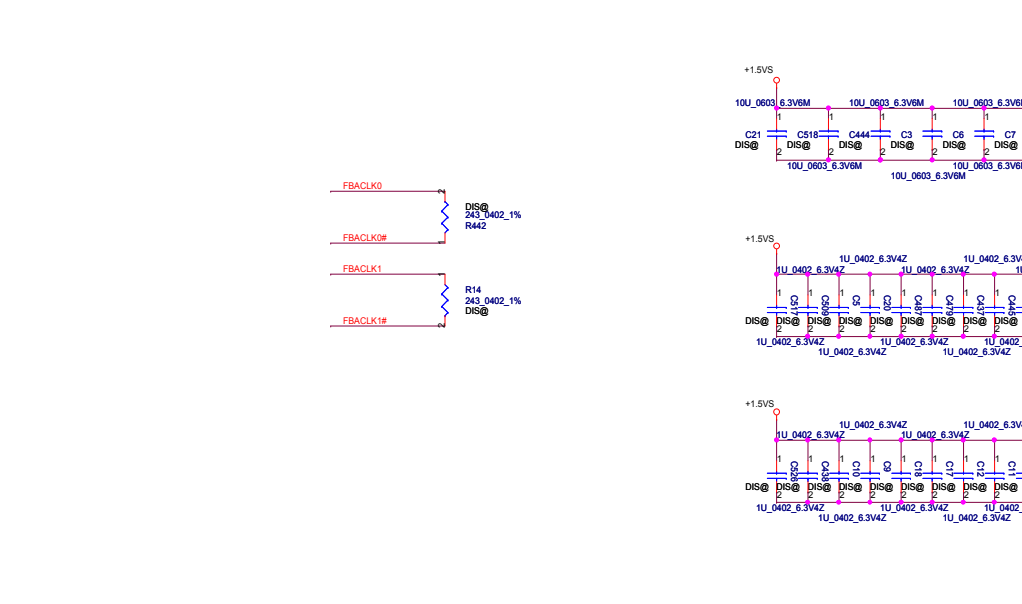
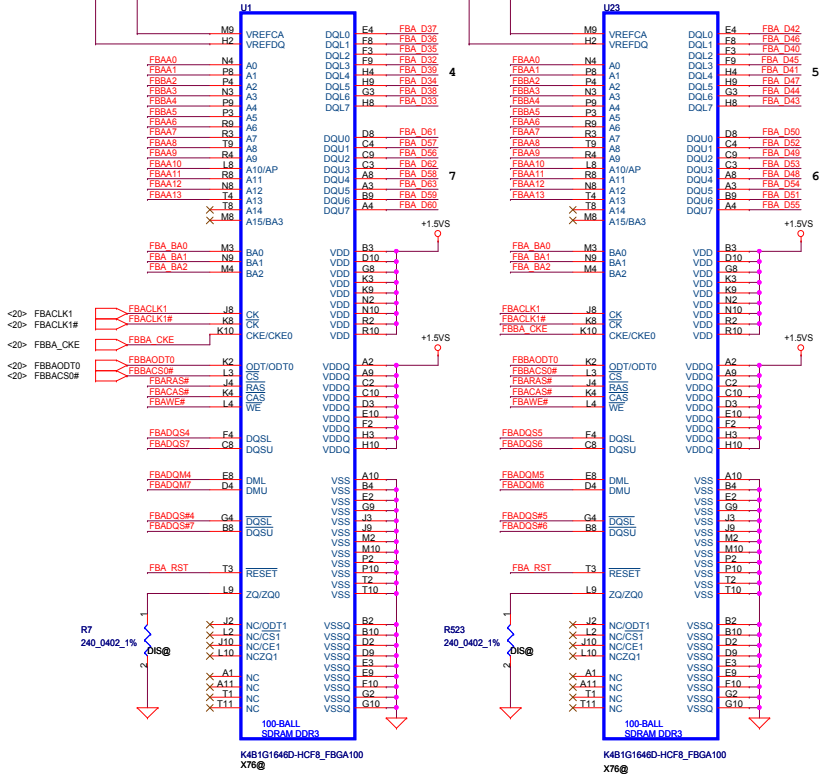
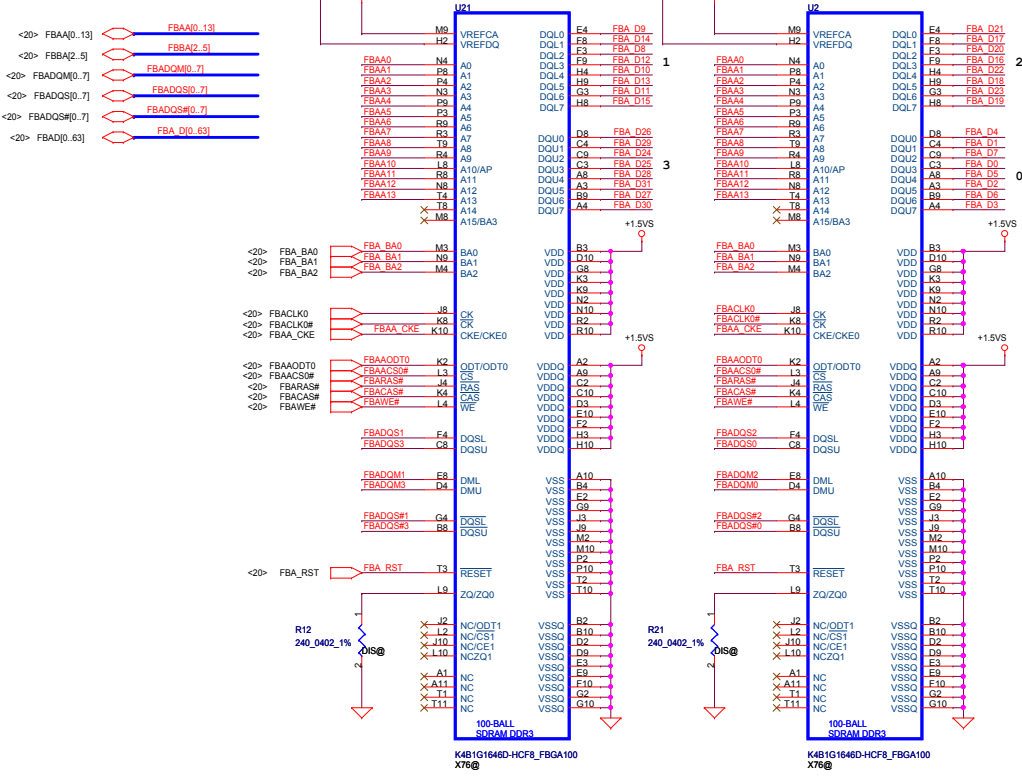
STRAP1 use for 3GIO_PADCFG to set 35K pull up.
 (PUN-04335-001_V10 HW9 update)

N11M-GE1 LP1	Memory/PKG	FBVDDQ	FB_CAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
	DDR3	+1.5VS	40.2 ohm	40.2 ohm	40.2/60.4 ohm

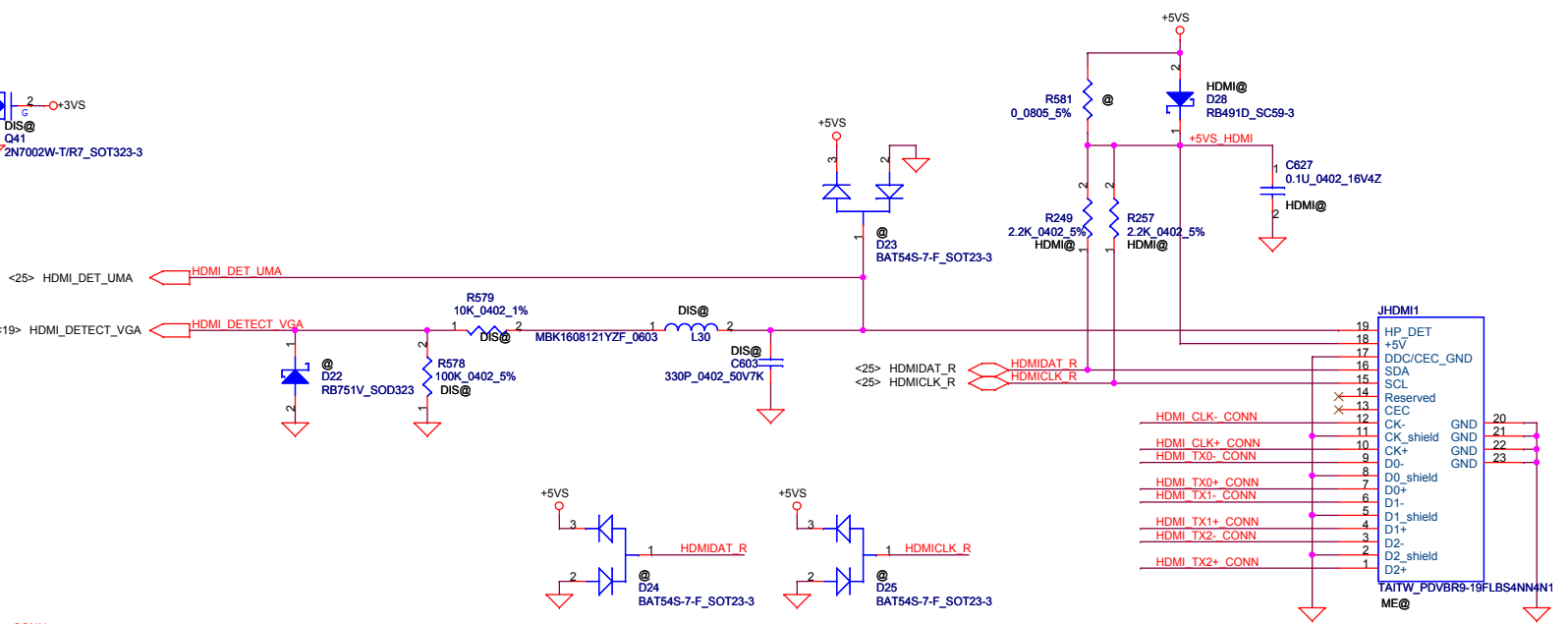
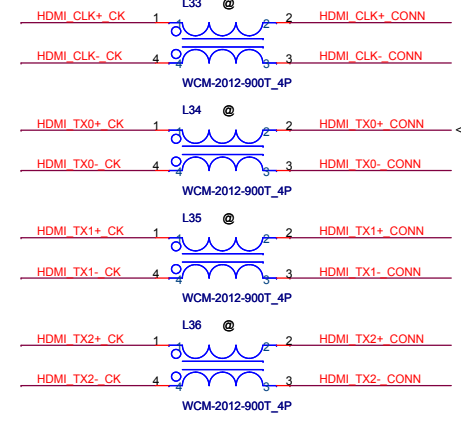
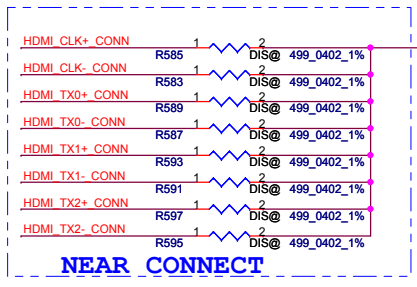
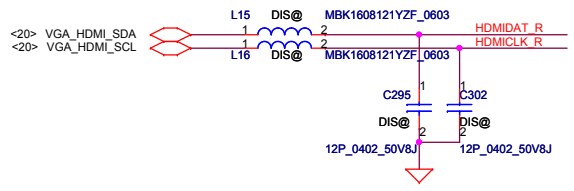
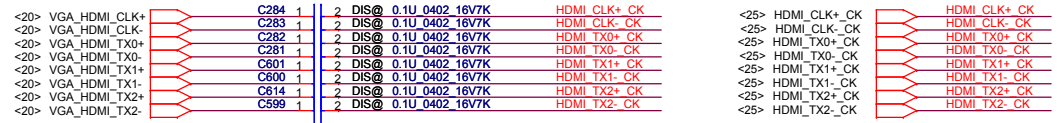
Must be used 1% resistor for driver calibration DG-04642-001-V01(May 22, 2009)

GPU	FB Memory (DDR3)	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N11M-GE1 LP1 (0x0A7D) 40nm	Samsung 800MHz	K4W1G1646E-HC12					
	(default)	64Mx16	PD 10K	PU 15K	PD 20K	PD 30K	PU 35K PU 45K
Hynix 800MHz	H5TQ1G63BFR-12C						
	64Mx16	PD 10K	PU 15K	PD 15K	PD 30K	PU 35K	PU 45K
				X76			

N11x 40nm DDR3 MAPPING
NVIDIA DOCUMENT FOR DA-3978-001

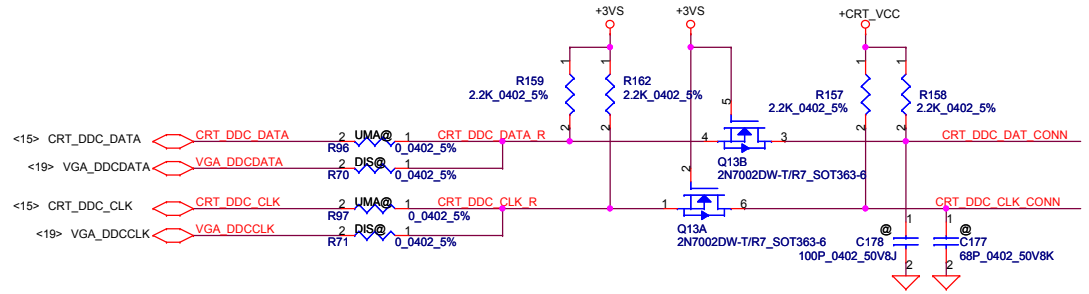
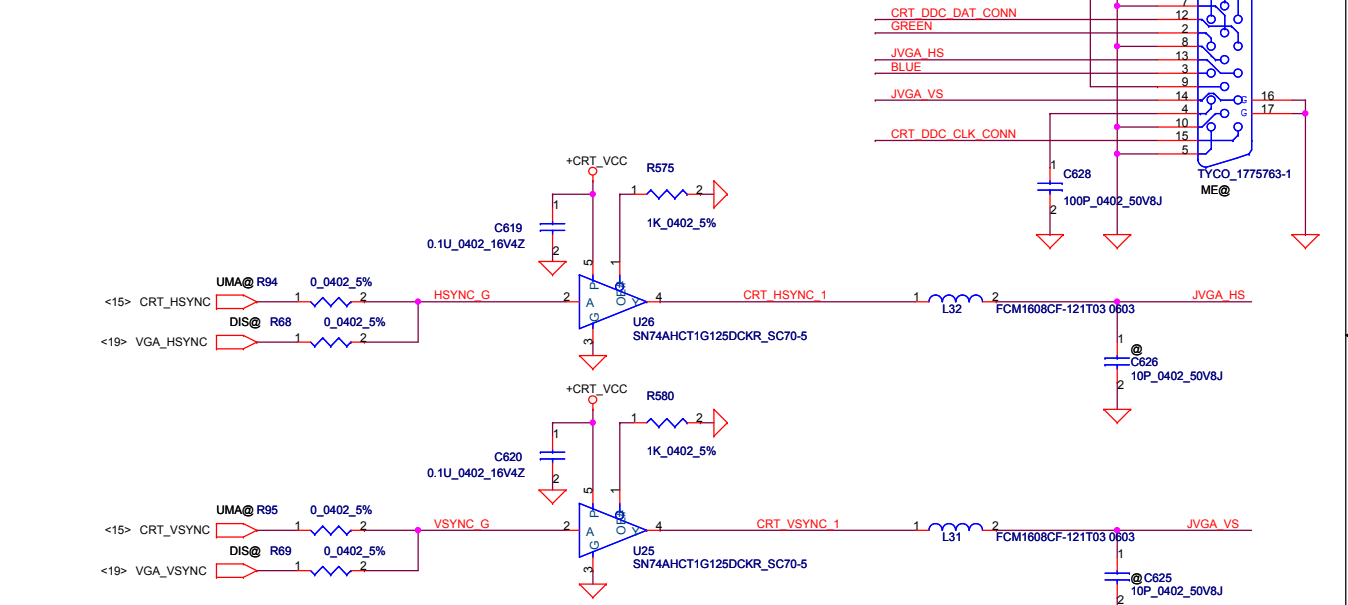
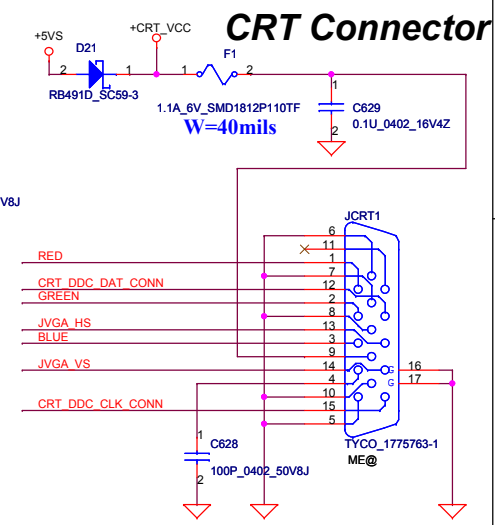
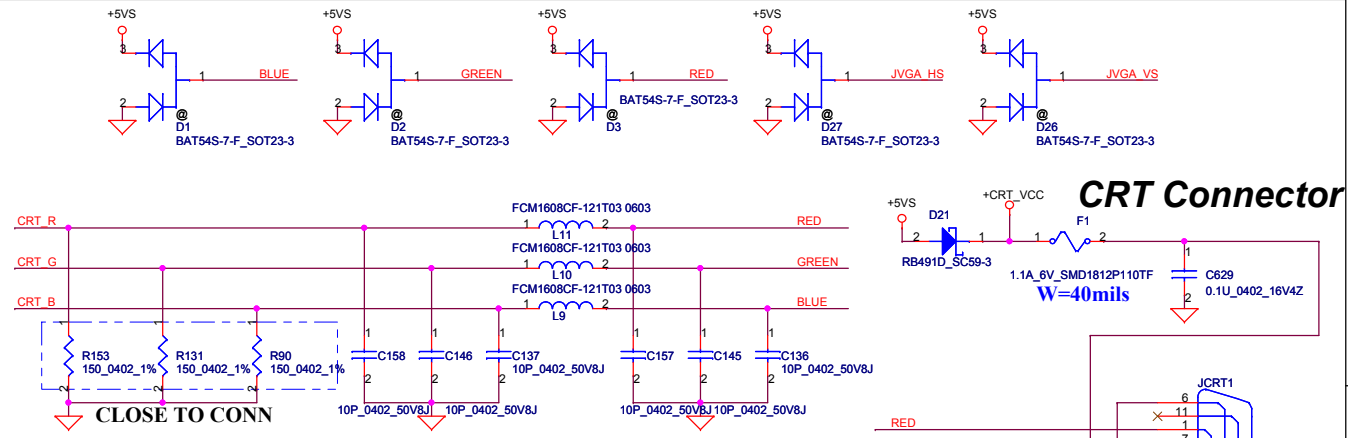
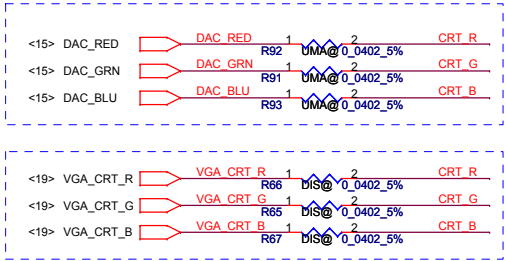


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Size	Document Number	Date		Rev
C	LA-5751	Thursday, October 26, 2006		0.3
			ISheet	23 of 51



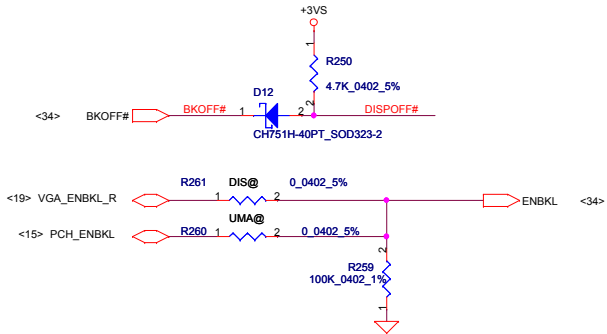
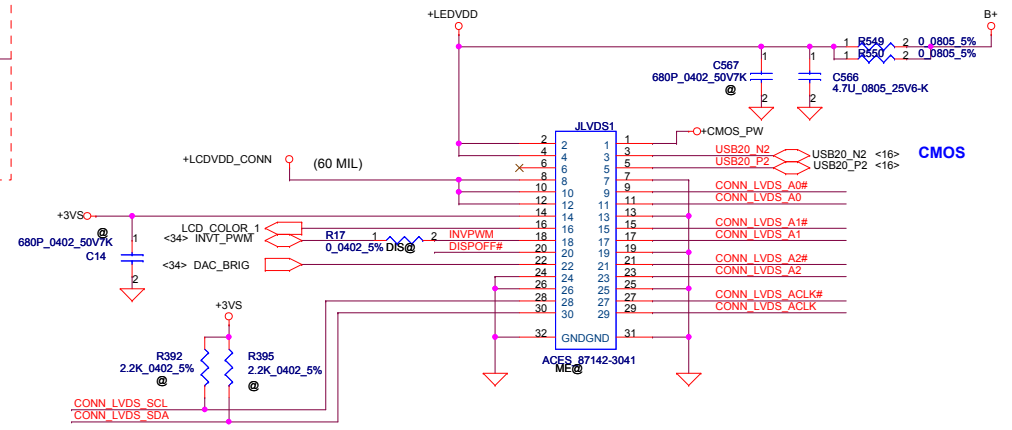
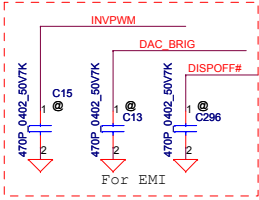
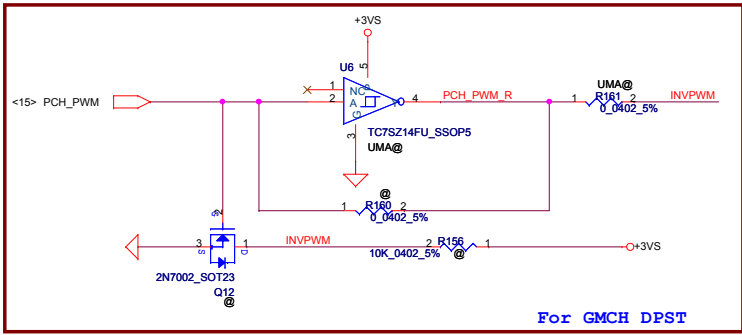
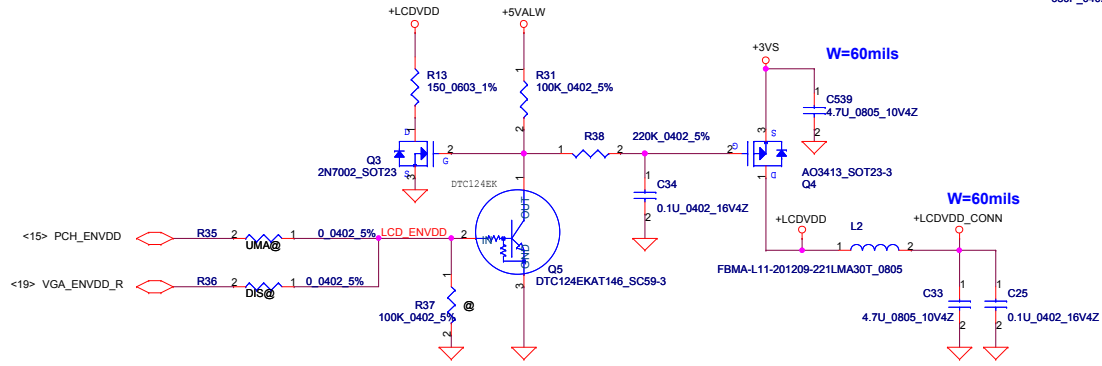
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Issued Date		Deciphered Date		HDMI CONN	
2008/03/25		2008/04/		Document Number	
				LA-5751	
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				Sheet 24 of 51	

Compal Electronics, Ltd.		Rev 0.3	
Title		Document Number	
HDMI CONN		LA-5751	
Date: Friday, October 30, 2009		Sheet 24 of 51	



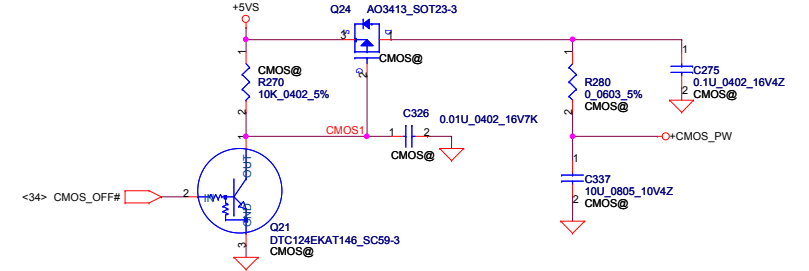
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Size	Document Number	Rev		0.3	
Custom	LA-5751				
Date:	Thursday, October 29, 2009	Sheet	26	of	51

LCD POWER CIRCUIT



- <19> VGA_LVDS_SCL VGA_LVDS_SCL 0.0402 5% 2 DIS@ 1 R390 CONN LVDS_SCL
- <19> VGA_LVDS_SDA VGA_LVDS_SDA 0.0402 5% 2 DIS@ 1 R391 CONN LVDS_SDA
- <20> VGA_LVDS_A0 VGA_LVDS_A0 0.0402 5% 2 DIS@ 1 R86 CONN LVDS_A0
- <20> VGA_LVDS_A0# VGA_LVDS_A0# 0.0402 5% 2 DIS@ 1 R85 CONN LVDS_A0#
- <20> VGA_LVDS_A1 VGA_LVDS_A1 0.0402 5% 2 DIS@ 1 R150 CONN LVDS_A1
- <20> VGA_LVDS_A1# VGA_LVDS_A1# 0.0402 5% 2 DIS@ 1 R128 CONN LVDS_A1#
- <20> VGA_LVDS_A2 VGA_LVDS_A2 0.0402 5% 2 DIS@ 1 R126 CONN LVDS_A2
- <20> VGA_LVDS_A2# VGA_LVDS_A2# 0.0402 5% 2 DIS@ 1 R127 CONN LVDS_A2#
- <20> VGA_LVDS_ACLK VGA_LVDS_ACLK 0.0402 5% 2 DIS@ 1 R84 CONN LVDS_ACLK
- <20> VGA_LVDS_ACLK# VGA_LVDS_ACLK# 0.0402 5% 2 DIS@ 1 R125 CONN LVDS_ACLK#
- <15> EDID_CLK EDID_CLK 0.0402 5% 2 UMA@ 1 R393 CONN LVDS_SCL
- <15> EDID_DATA EDID_DATA 0.0402 5% 2 UMA@ 1 R394 CONN LVDS_SDA
- <15> LVDS_A0 LVDS_A0 0.0402 5% 2 UMA@ 1 R383 CONN LVDS_A0
- <15> LVDS_A0# LVDS_A0# 0.0402 5% 2 UMA@ 1 R382 CONN LVDS_A0#
- <15> LVDS_A1 LVDS_A1 0.0402 5% 2 UMA@ 1 R389 CONN LVDS_A1
- <15> LVDS_A1# LVDS_A1# 0.0402 5% 2 UMA@ 1 R388 CONN LVDS_A1#
- <15> LVDS_A2 LVDS_A2 0.0402 5% 2 UMA@ 1 R386 CONN LVDS_A2
- <15> LVDS_A2# LVDS_A2# 0.0402 5% 2 UMA@ 1 R387 CONN LVDS_A2#
- <15> LVDS_ACLK LVDS_ACLK 0.0402 5% 2 UMA@ 1 R384 CONN LVDS_ACLK
- <15> LVDS_ACLK# LVDS_ACLK# 0.0402 5% 2 UMA@ 1 R385 CONN LVDS_ACLK#

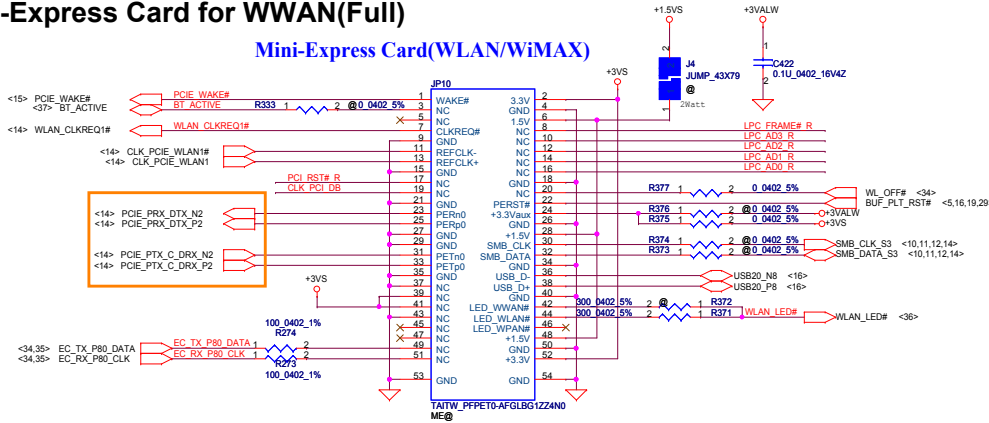
CMOS Camera



Security Classification	Compal Secret Data			Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Compal Electronics, Inc.	
				LVDS/CAMERA	
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				LA-5751	
				Date:	Friday, October 30, 2009
				Sheet	27 of 51
				Rev	0.3

Mini-Express Card for WLAN/WIMAX(Half) Mini-Express Card for WWAN(Full)

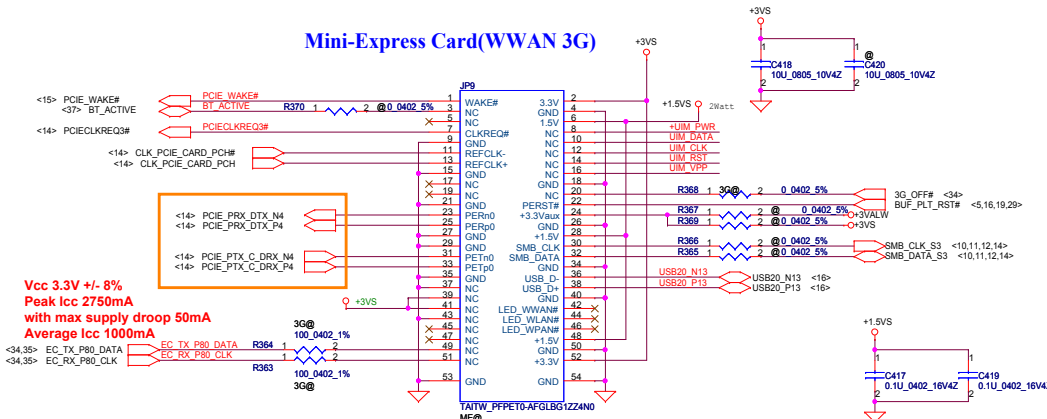
Mini-Express Card(WLAN/WIMAX)



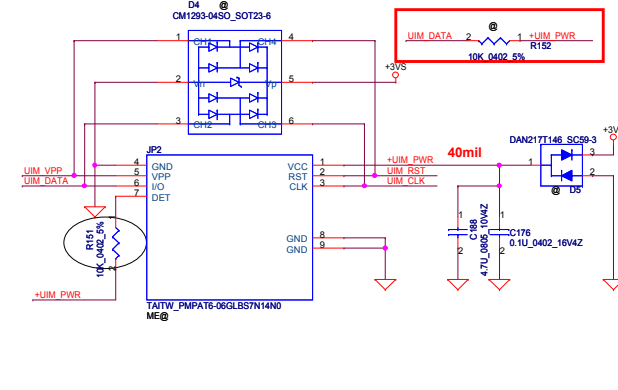
Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

LPC_FRAME# R	R284	1	2	0.0402 5%	LPC_FRAME#	LPC_FRAME#	<13,34>
LPC_AD3 R	R285	1	2	0.0402 5%	LPC_AD3	LPC_AD3	<13,34>
LPC_AD2 R	R286	1	2	0.0402 5%	LPC_AD2	LPC_AD2	<13,34>
LPC_AD1 R	R287	1	2	0.0402 5%	LPC_AD1	LPC_AD1	<13,34>
LPC_AD0 R	R288	1	2	0.0402 5%	LPC_AD0	LPC_AD0	<13,34>
PCI_RST# R	R290	1	2	0.0402 5%	PCI_RST#	PCI_RST#	<13,34>
CLK_PCl DB					CLK_PCl DB	CLK_PCl DB	<14>

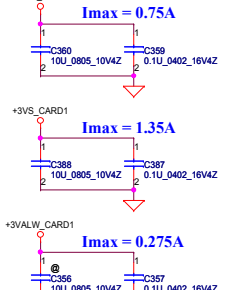
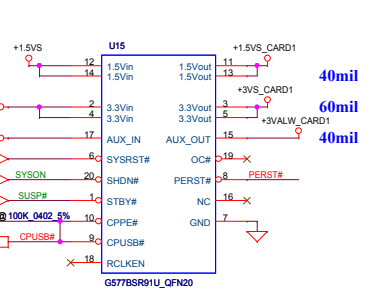
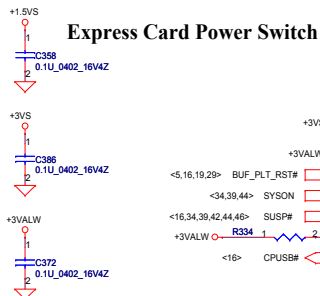
Mini-Express Card(WWAN 3G)



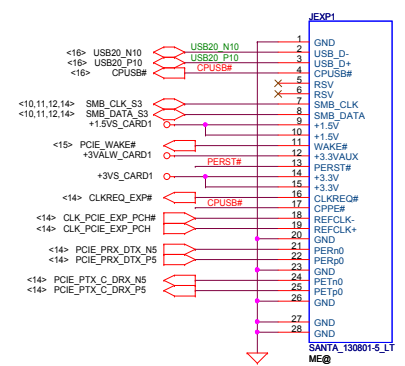
Vcc 3.3V +/- 8%
Peak Icc 2750mA
with max supply droop 50mA
Average Icc 1000mA



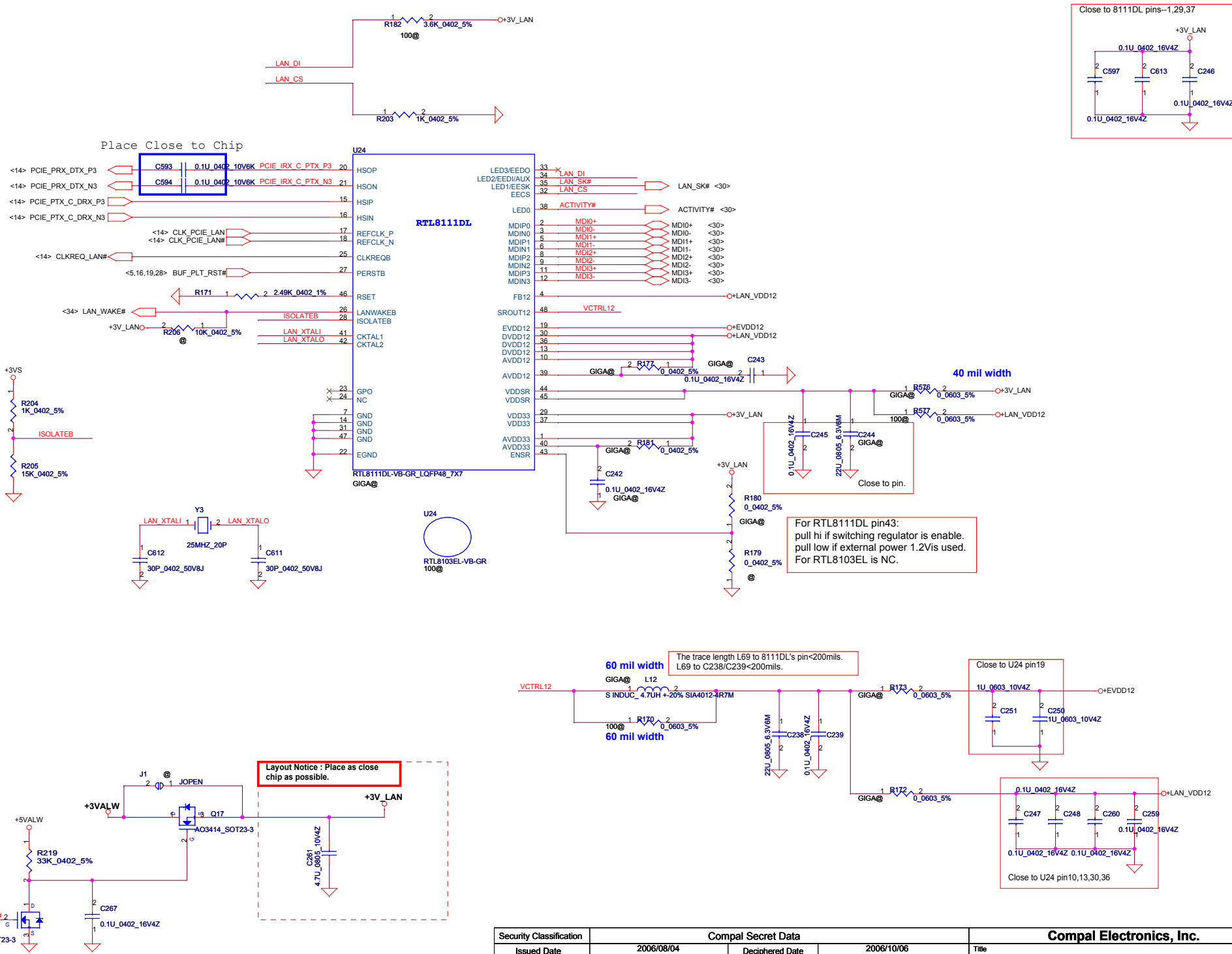
Express Card Power Switch



New Card 34mm Socket (Left/TOP)

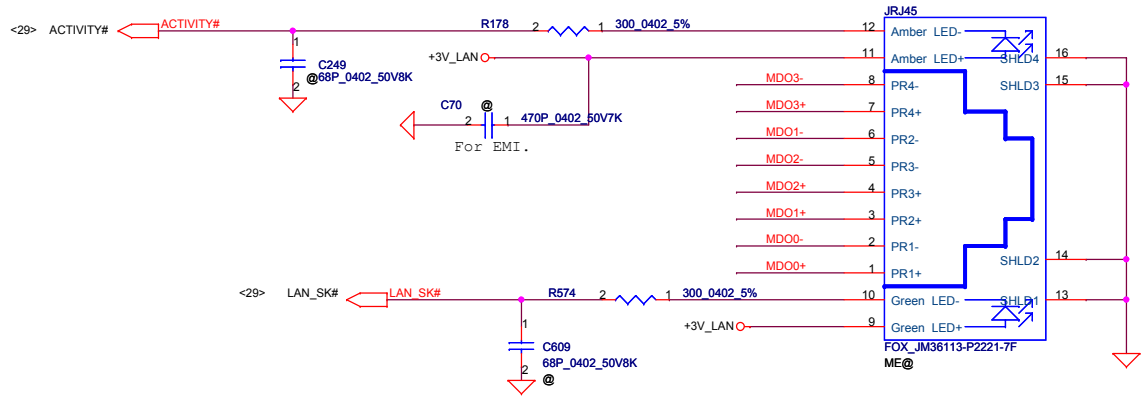
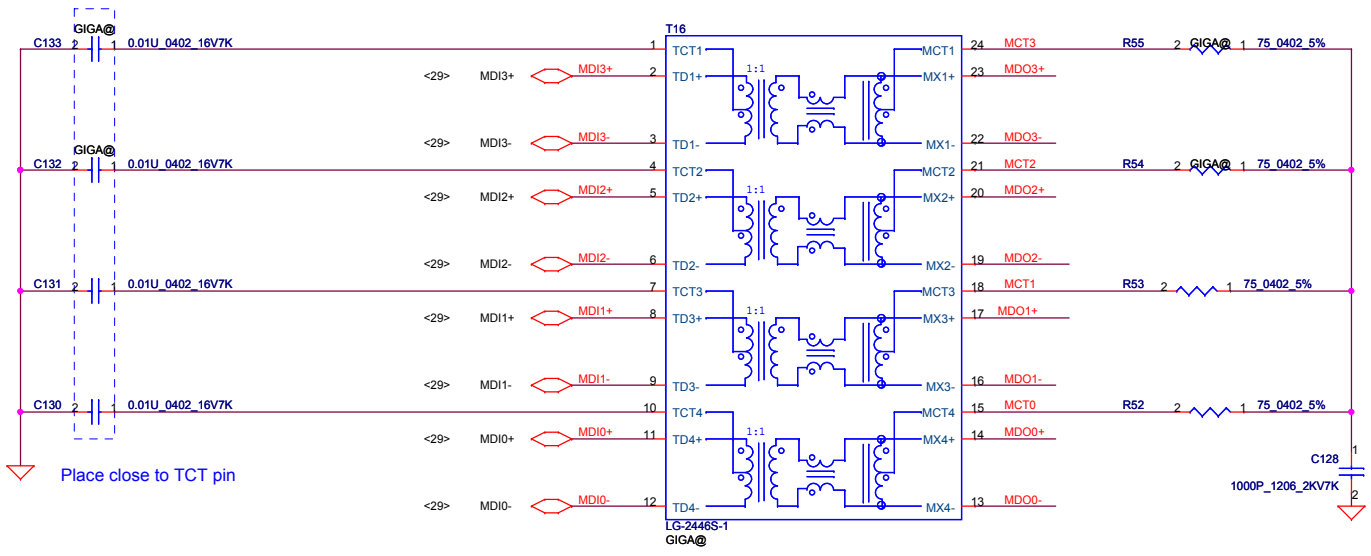


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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Mini-Card/Nwe Card/SIM
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Size	Document Number	LA-5751	Rev	0.3
Date:	Friday, October 30, 2009	Sheet	28	of 51



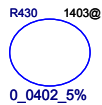
Security Classification		Compal Secret Data		Title	
Issued Date	2006/08/04	Deciphered Date	2006/10/06	RTL8103EL	
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Customer		LA-5751	Rev	0.3	
Date:	Friday, October 30, 2009	Sheet	29	of 51	

Close to T14

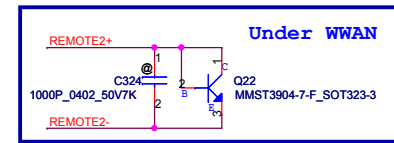
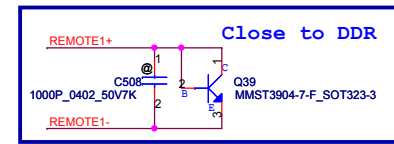
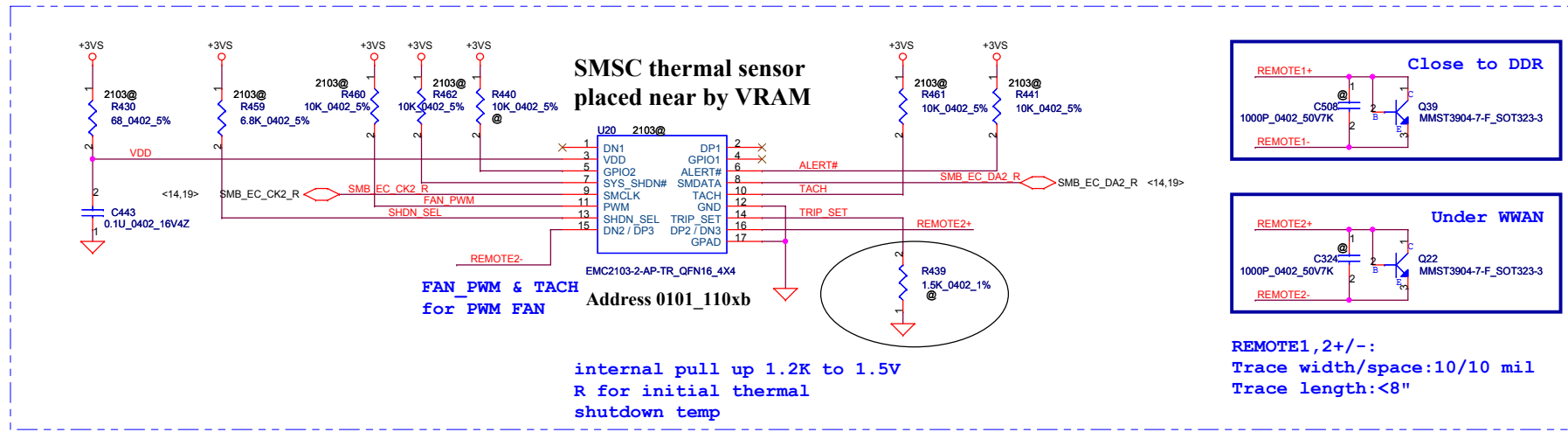


RJ45 Conn.

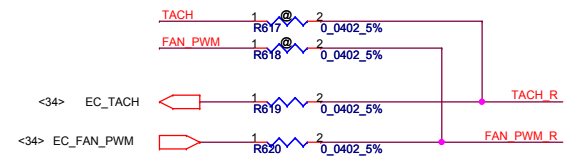
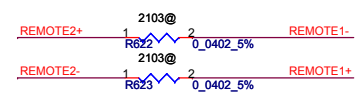
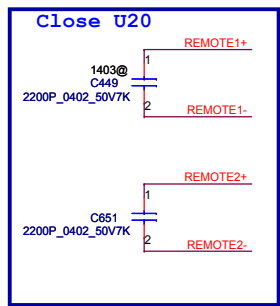
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/03/20	Deciphered Date	2010/03/20	Title	
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Size Custom	Document Number	LA-5751		Rev	0.3
Date:	Friday, October 30, 2009	Sheet	30	of	51



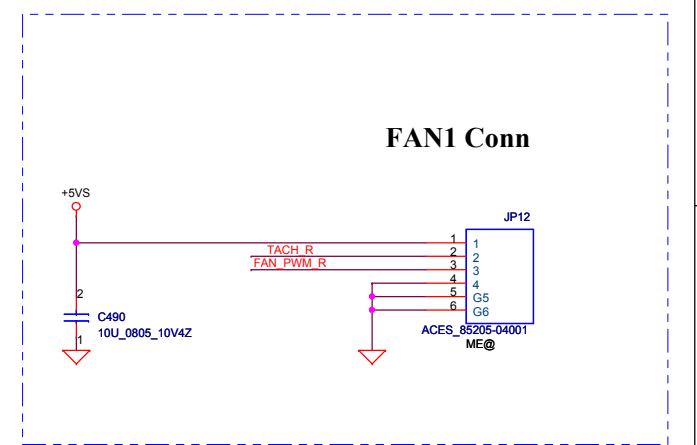
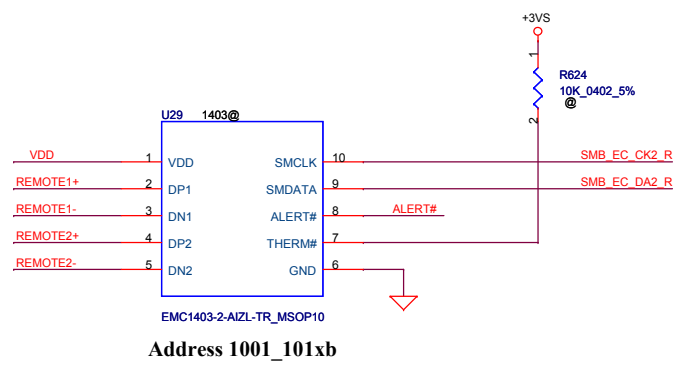
1403:
@C508/@C324=100p



REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

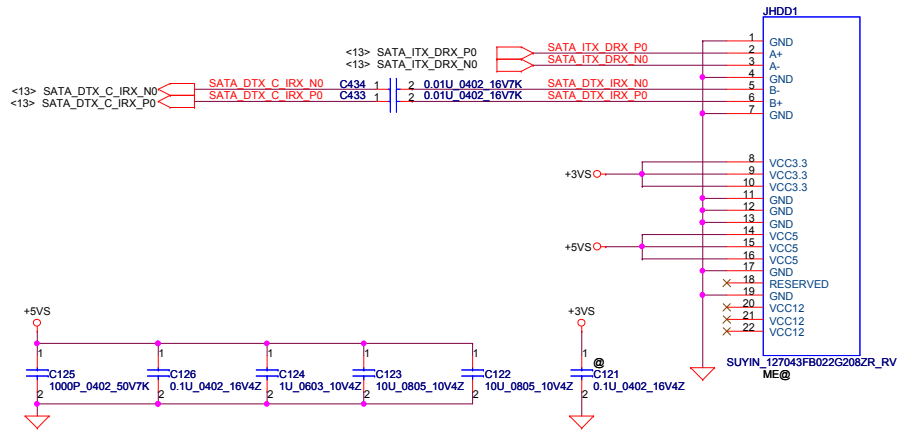


Shutdown Temp	TRIP_SET R439 (1%)
93	953ohm
94	1020ohm
95	1100ohm
96	1150ohm
97	1240ohm
98	1330ohm
99	1400ohm
100	1500ohm
101	1580ohm
102	1690ohm
103	1820ohm
104	1960ohm
105	2050ohm

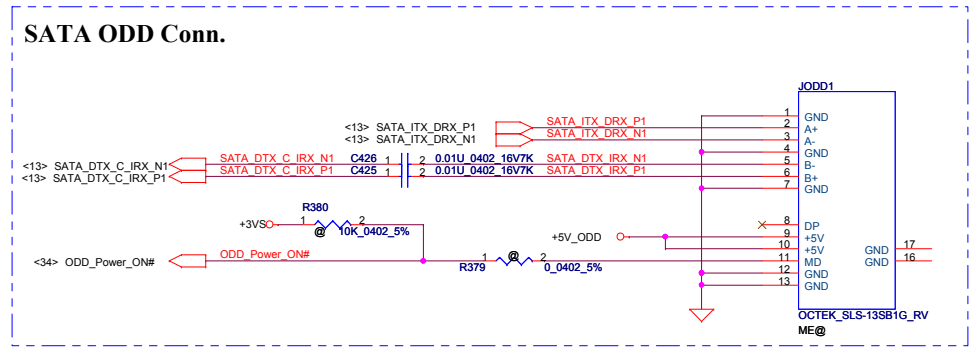


Security Classification		Compal Secret Data		Compal Electronics, Ltd.	
Issued Date	2008/03/25	Deciphered Date	2008/04/	Title	EMC2103/1403_Thermal sensor/FAN
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Date	Friday, October 30, 2009	Sheet	31 of 51	Rev	0.3

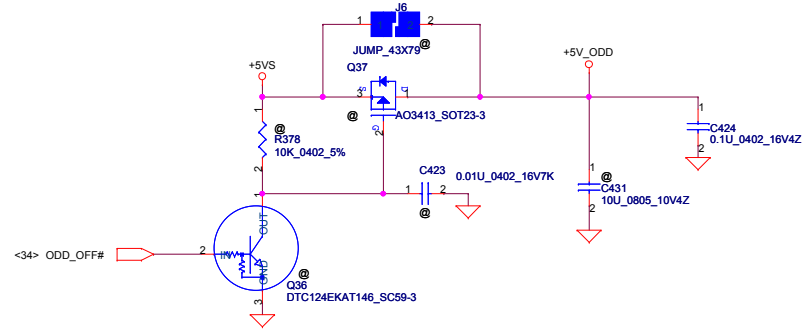
SATA HDD Conn.



SATA ODD Conn.

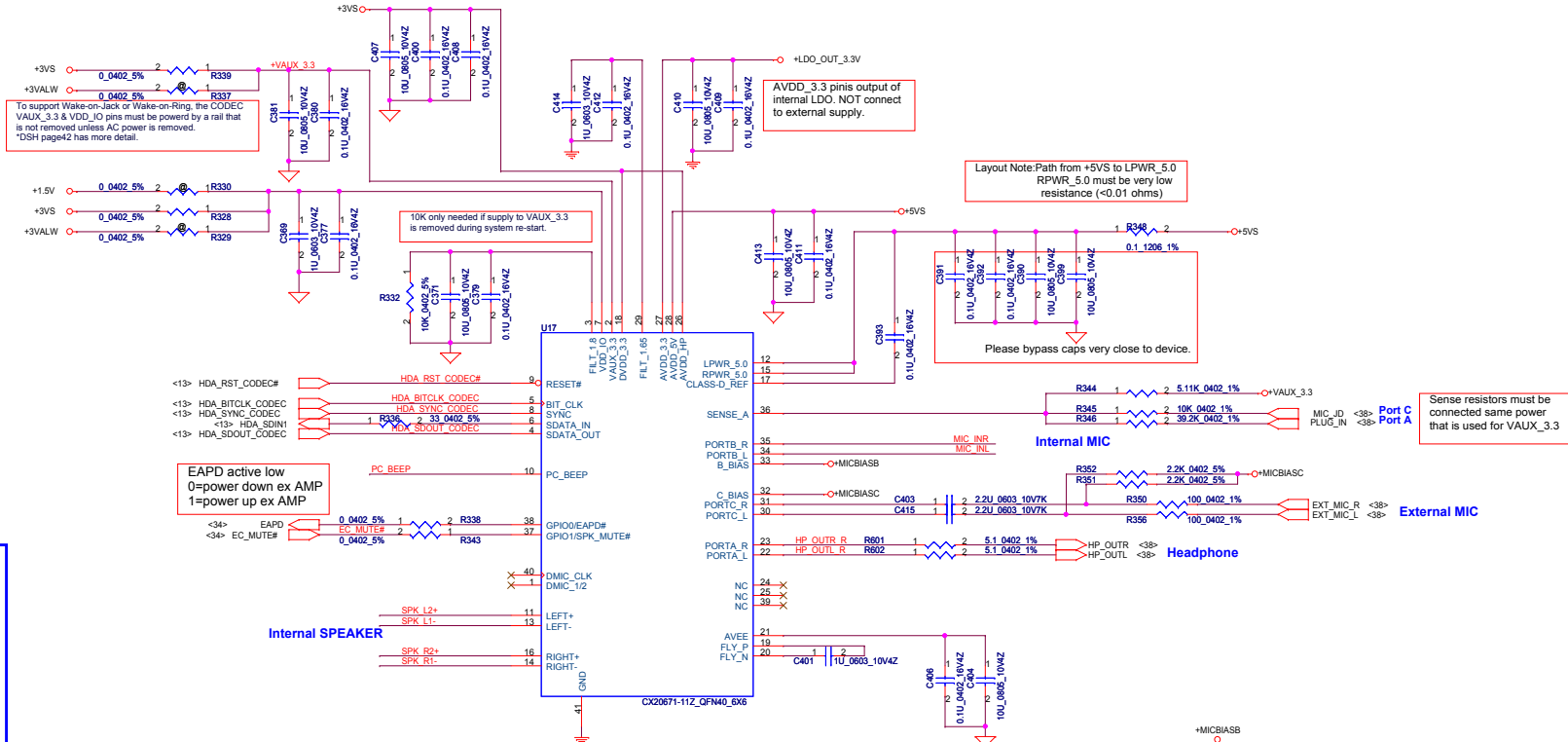
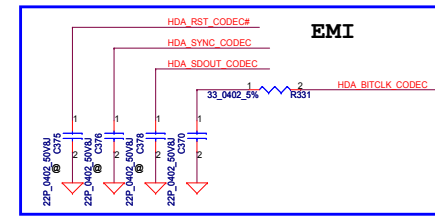


ODD Power Control



Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	HDD/ODD Connector	
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				Date: Friday, October 30, 2009	Rev 0.3
				Sheet 32	of 51

CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).



To support Wake-on-Lock or Wake-on-Ring, the CODEC VAUX_3.3 & VDD_IO pins must be powered by a rail that is not removed unless AC power is removed. DSH page42 has more detail.

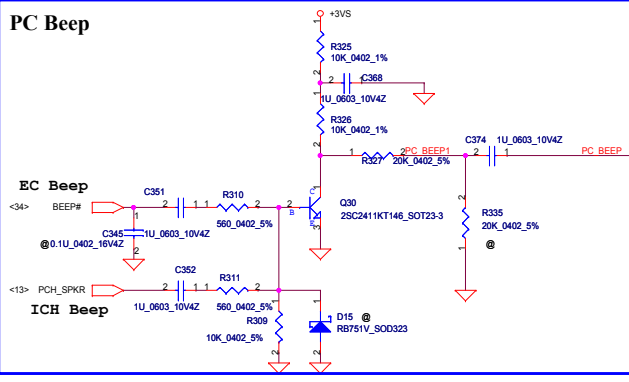
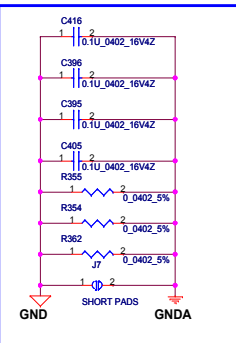
AVDD_3.3 pins output of internal LDO. NOT connect to external supply.

Layout Note: Path from +5VS to LPWR_5.0 RPWR_5.0 must be very low resistance (<0.01 ohms)

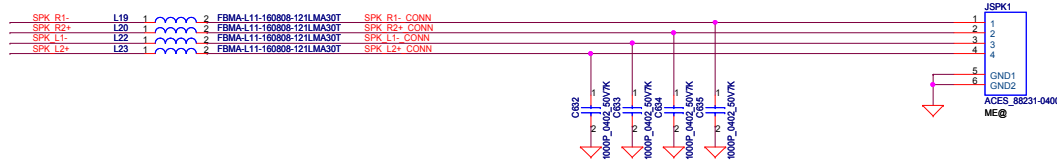
Please bypass caps very close to device.

Sense resistors must be connected same power that is used for VAUX_3.3

EAPD active low
 0=power down ex AMP
 1=power up ex AMP

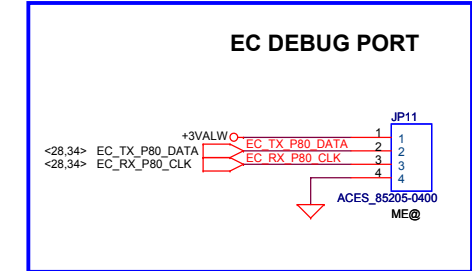
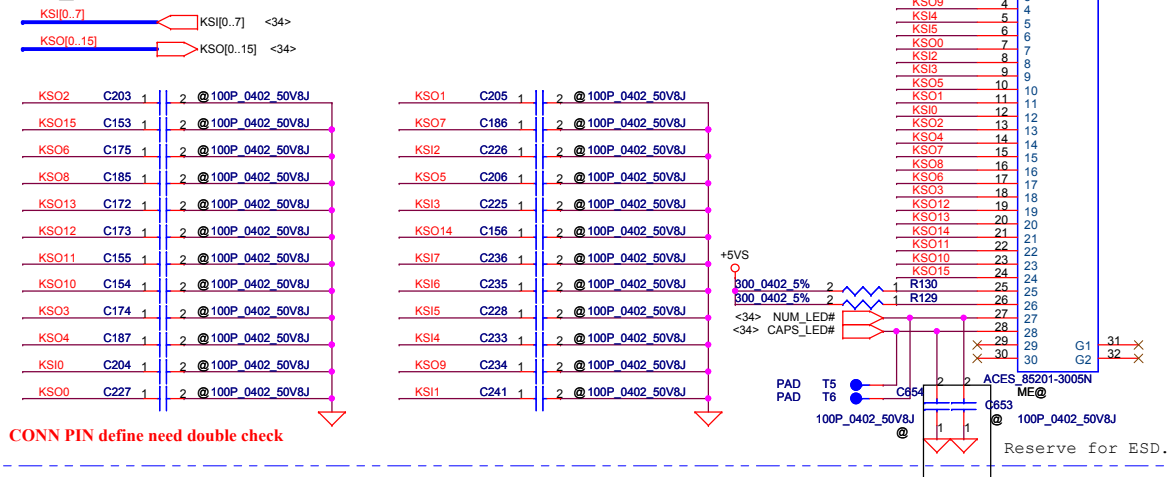


wide 20MIL

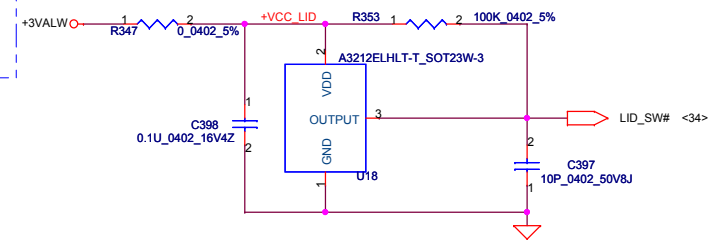


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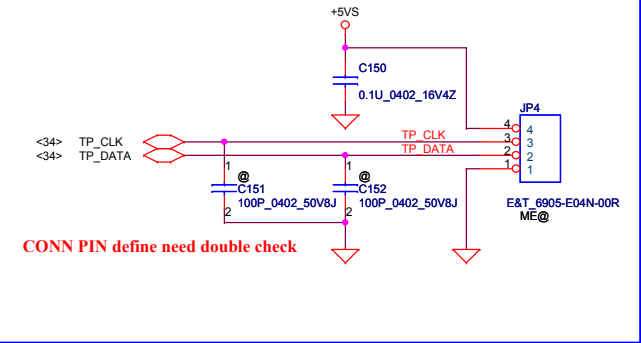
INT_KBD Conn.



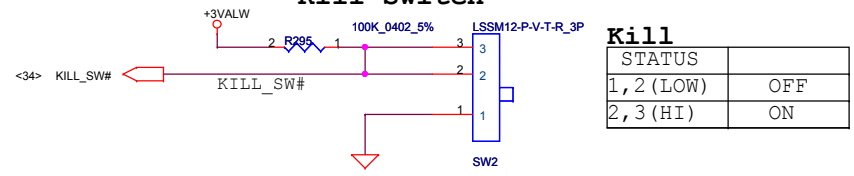
Lid Switch



To TP/B Conn.

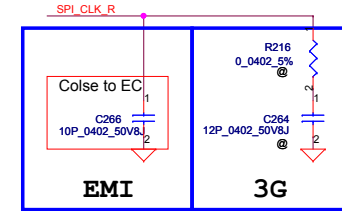
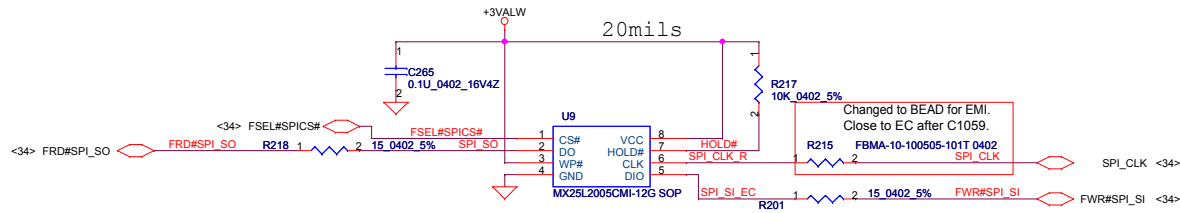


Kill Switch

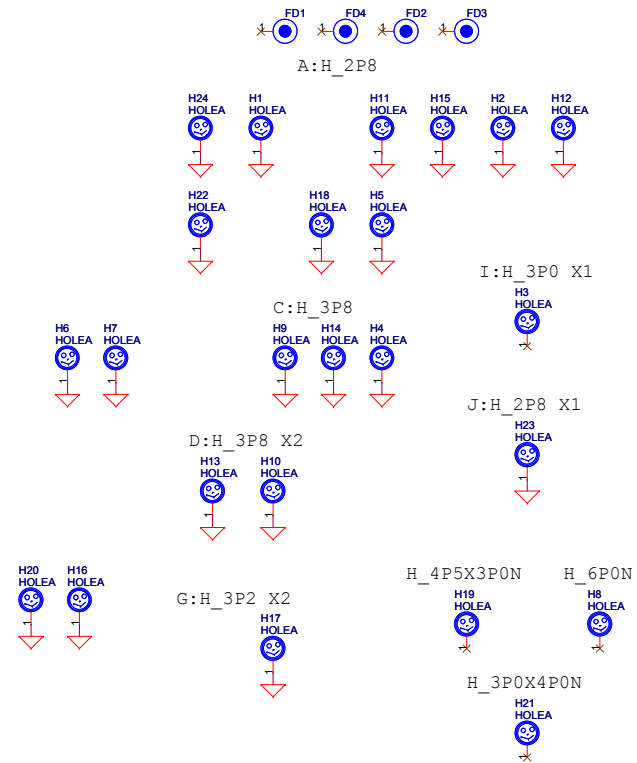
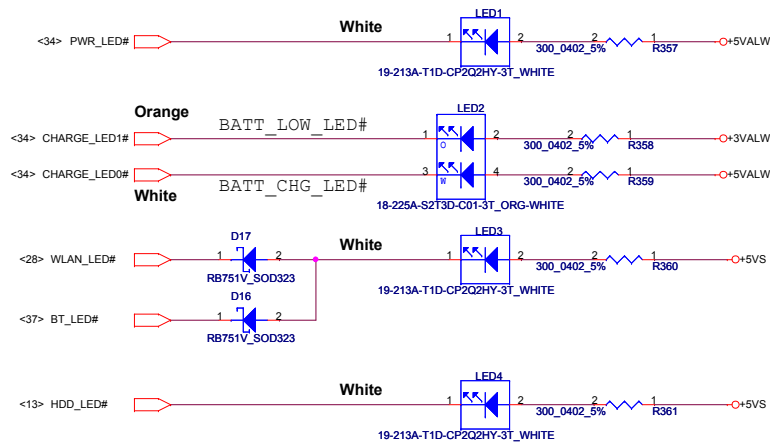


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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Compal Electronics, Inc.	
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Size	B	Document Number	LA-5751	Rev	0.3
Date:	Friday, October 30, 2009	Sheet	35	of	51

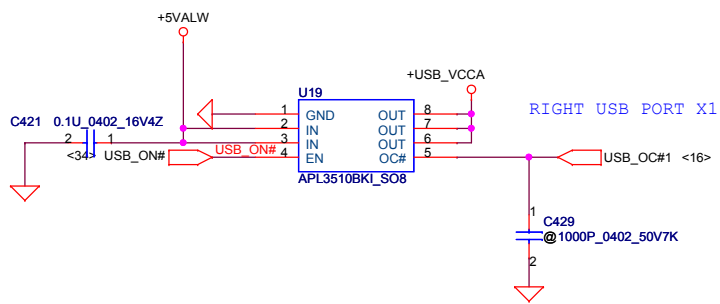
**FOR EC 256KB SPI ROM
(150mil PACKAGE)**



LED

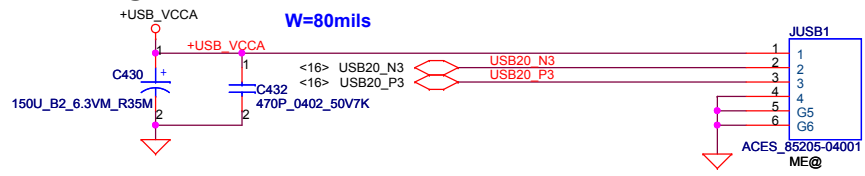


Security Classification	Compal Secret Data		Compal Electronics, Inc. LED/EC SPI ROM	
Issued Date	2007/10/15	Deciphered Date		
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Size B	Document Number	LA-5751	Rev	0.3
Date:	Friday, October 30, 2009	Sheet	36	of 51

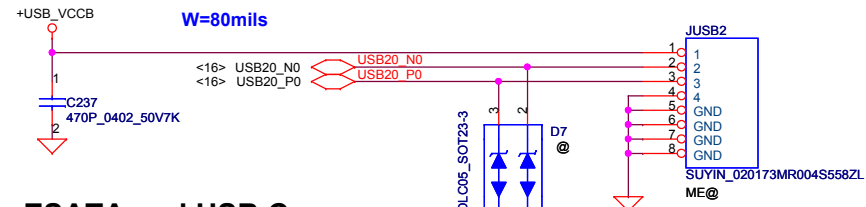


U19/U27 USB power switch need update symbol to SA000039E00 (Low enable)

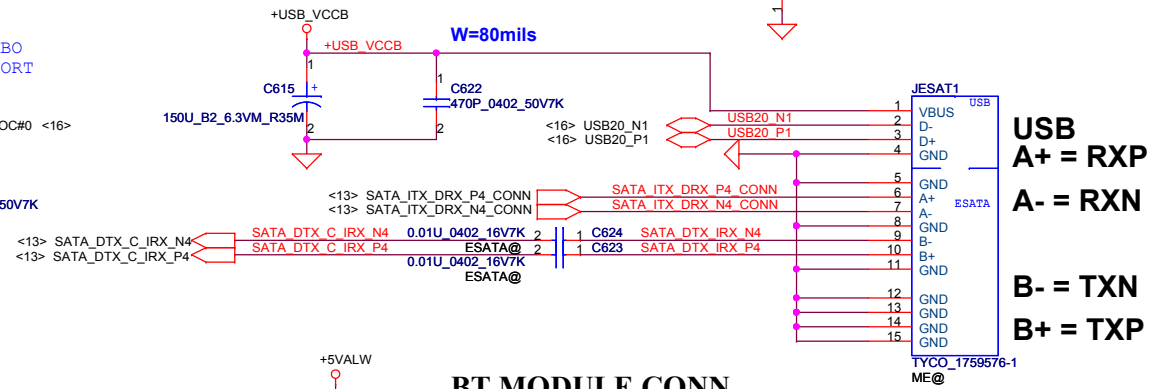
Right USB Conn.



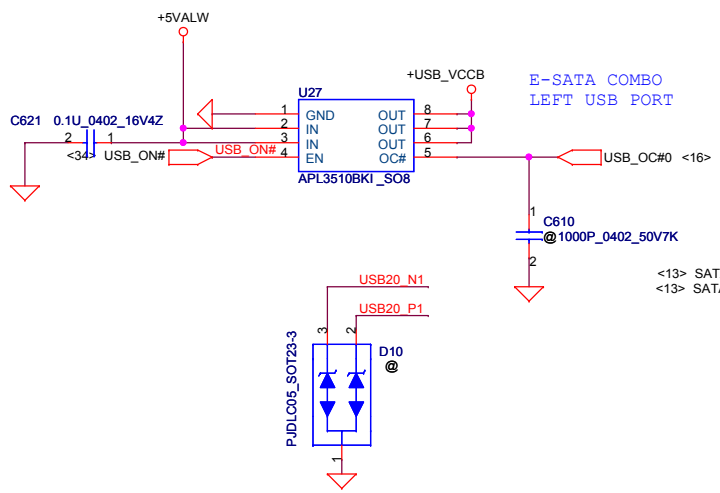
Left USB Conn.



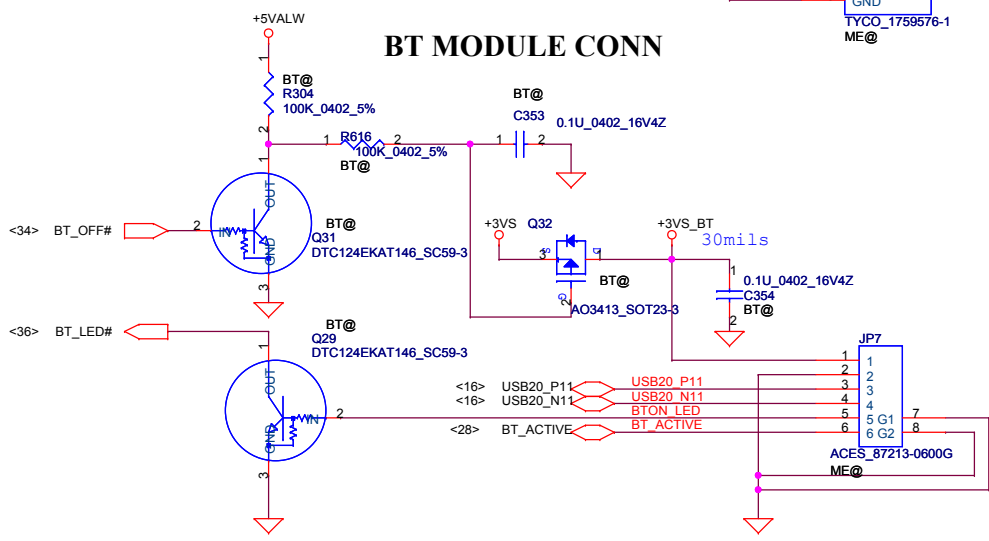
ESATA and USB Conn.



USB
A+ = RXP
A- = RXN
B- = TXN
B+ = TXP

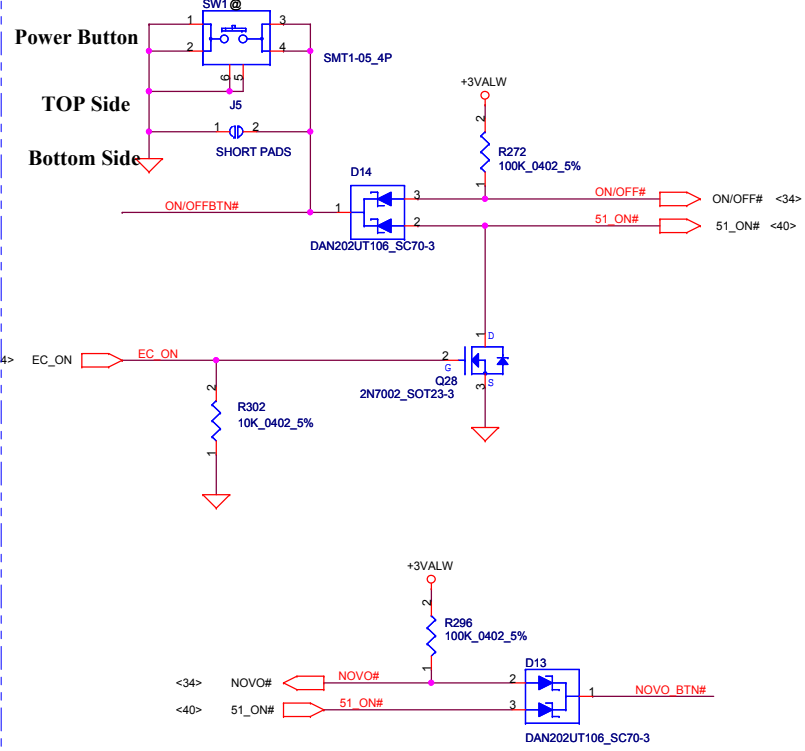


BT MODULE CONN

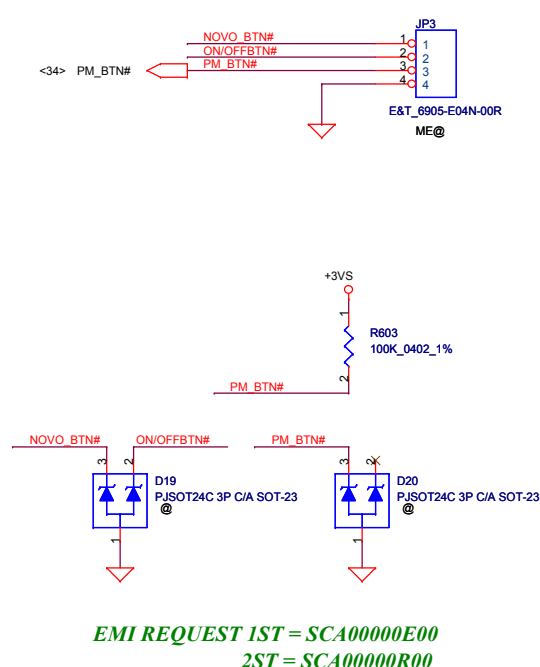


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Size	Document Number	Rev		Date	
Custom	LA-5751	0.3		Thursday, October 29, 2009	
				Sheet 37 of 51	

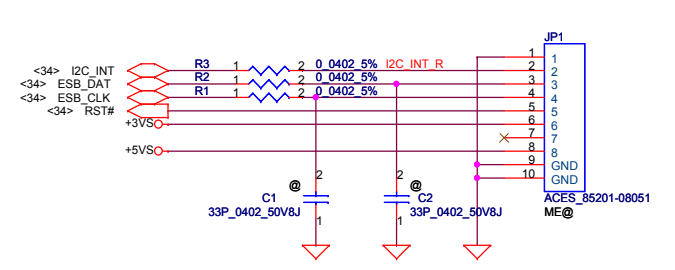
ON/OFF switch



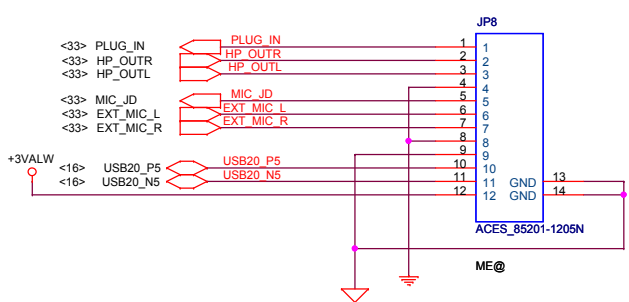
Power Bottom Board Conn. 4pin



Cap Sensor Board Conn. 6pin ENE SB3534

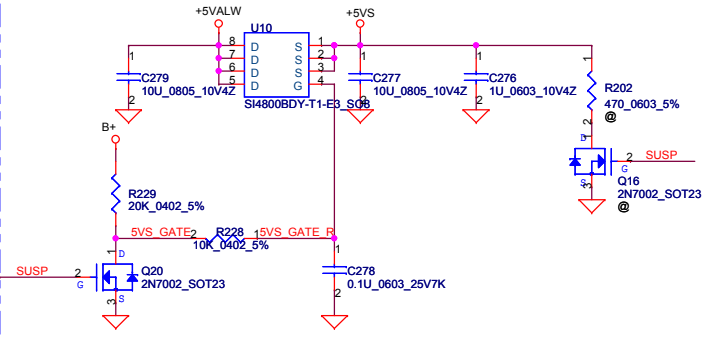


Card Reader/Audio Jack SB CONN

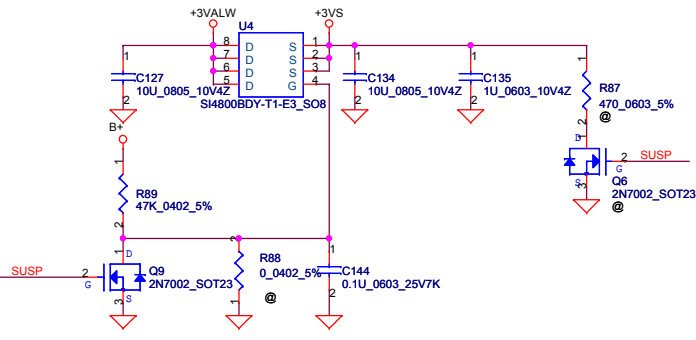


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				Size Custom
			LA-5751	0.3
Date: Friday, October 30, 2009		Sheet 38 of 51		

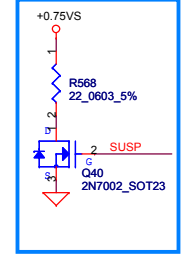
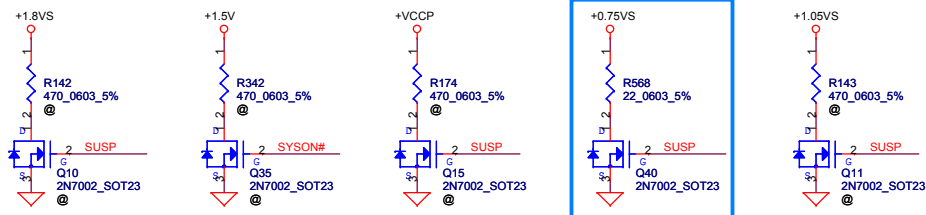
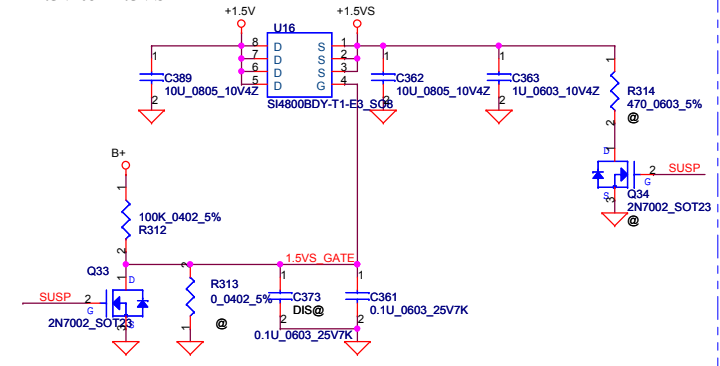
+5VALW TO +5VS



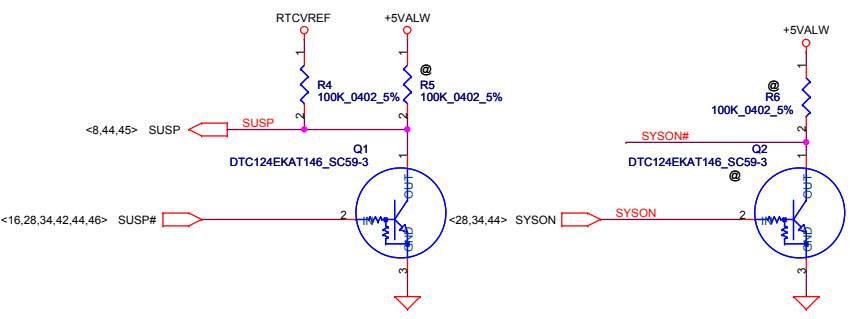
+3VALW TO +3VS



+1.5V to +1.5VS

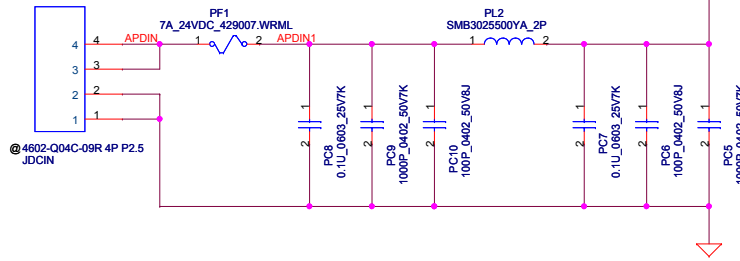


For Intel S3 Power Reduction.



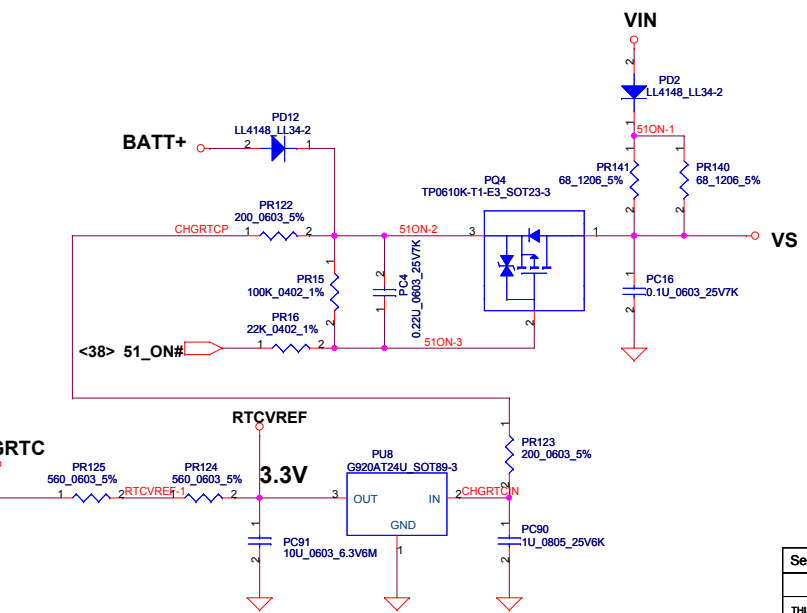
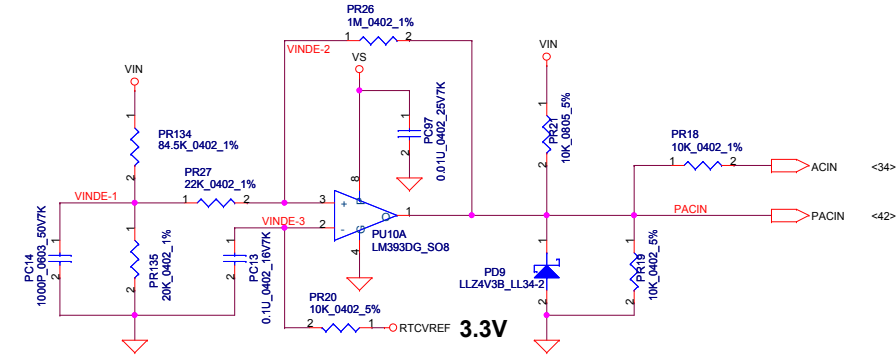
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Size	Document Number	Rev		0.3	
Custom	LA-5751	Date		Thursday, October 29, 2009	
				Sheet	39 of 51

DC030006J00



Vin Detector

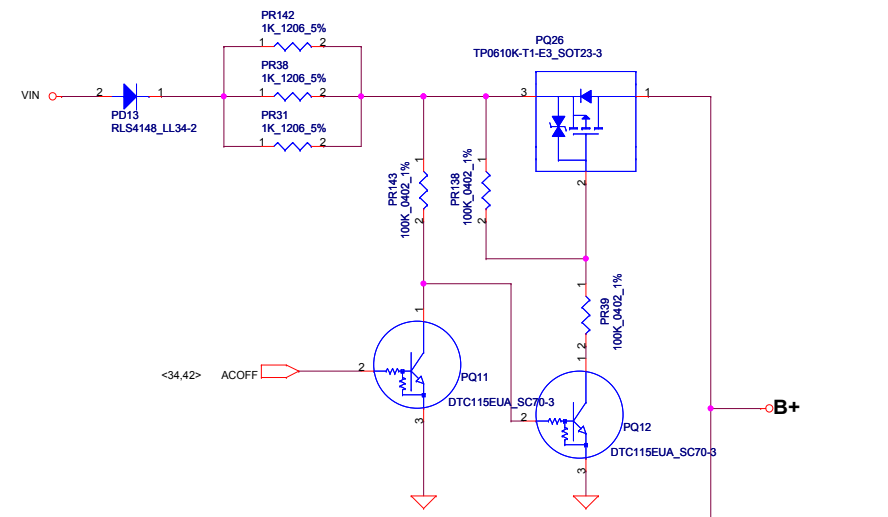
	Min.	typ.	Max.
L-->H	17.430V	17.901V	18.384V
H-->L	16.976V	17.262V	17.728V



ACIN

Precharge detector

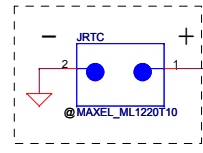
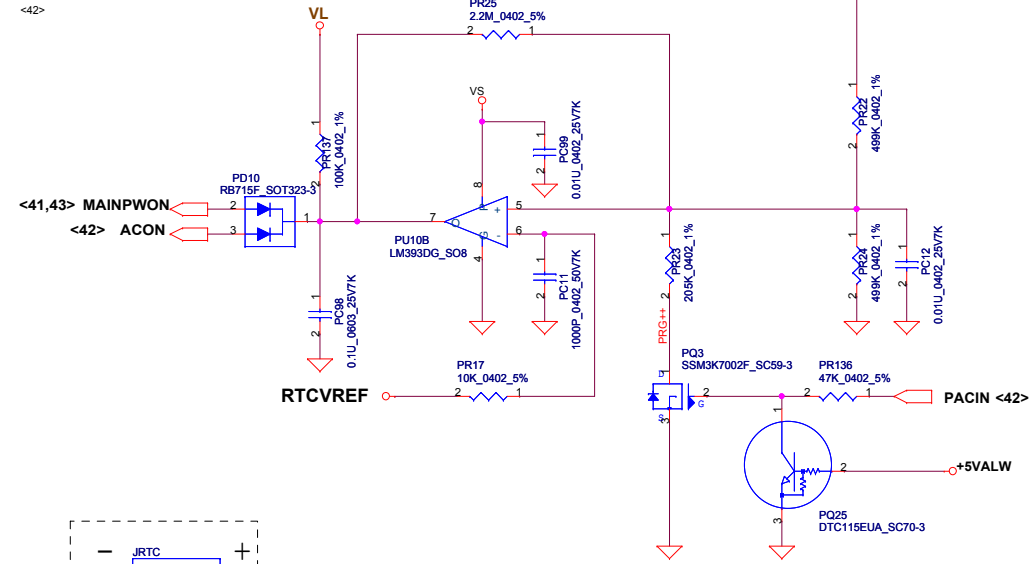
	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V



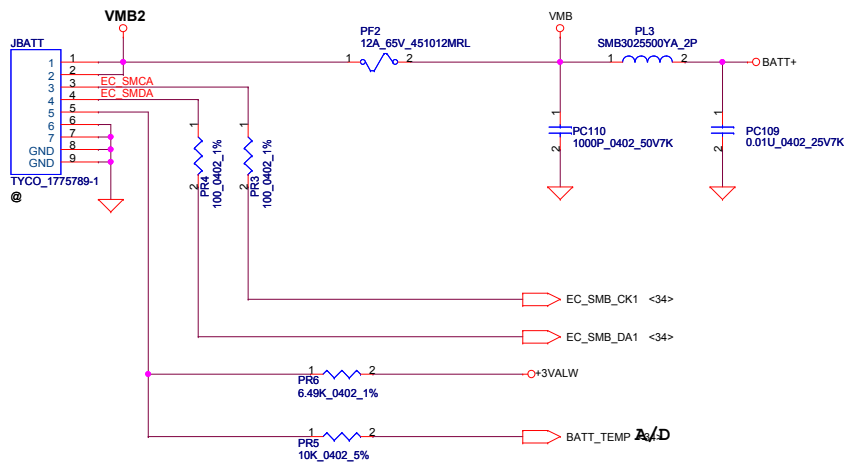
BATT ONLY

Precharge detector

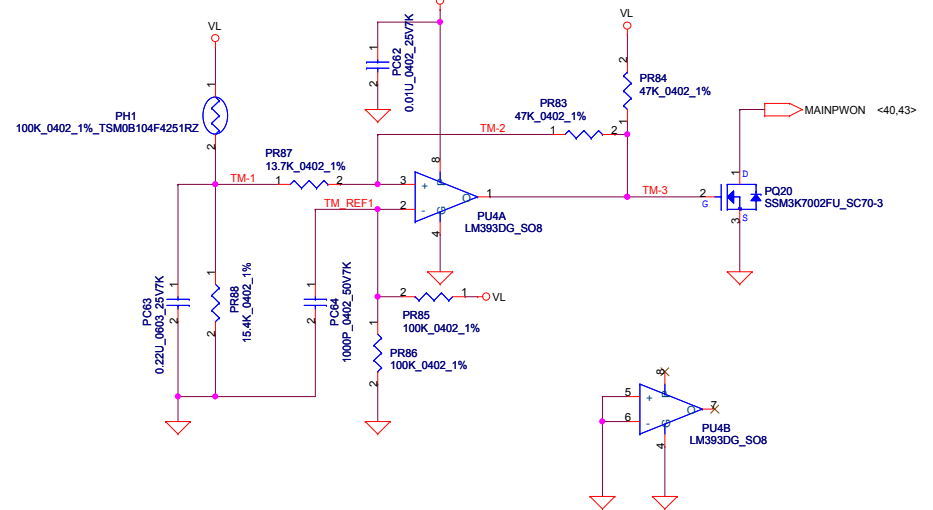
	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V



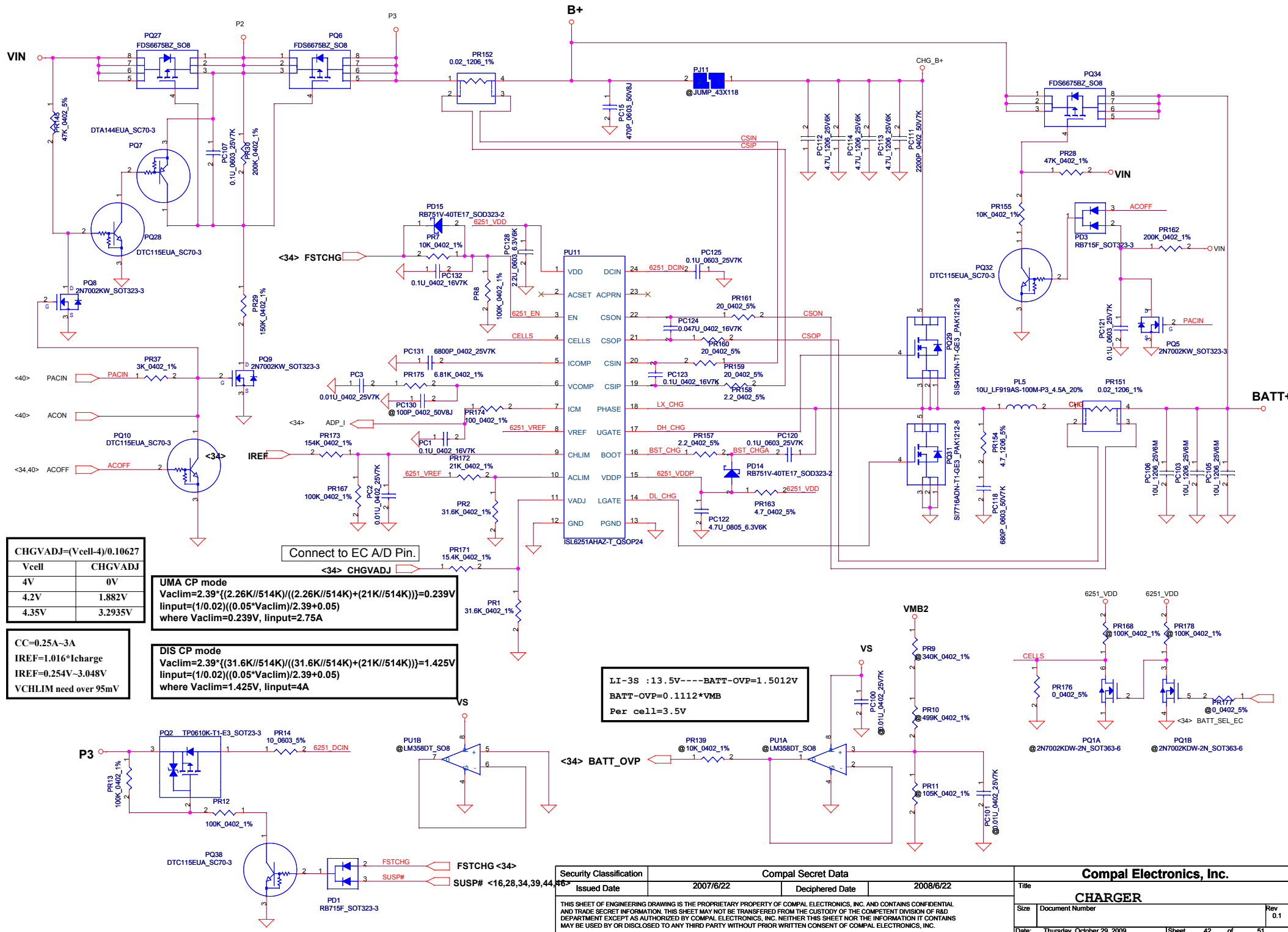
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Size	Document Number			Rev	0.1
Date:	Friday, October 30, 2009	Sheet	40	of	51



PH1 under CPU botten side :
 CPU thermal protection at 92 degree C
 Recovery at 56 degree C



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Size	Document Number			Rev	
Date:	Thursday, October 29, 2009	Sheet	41	of	51



CHGVADJ=(Vcell-4)/0.10627

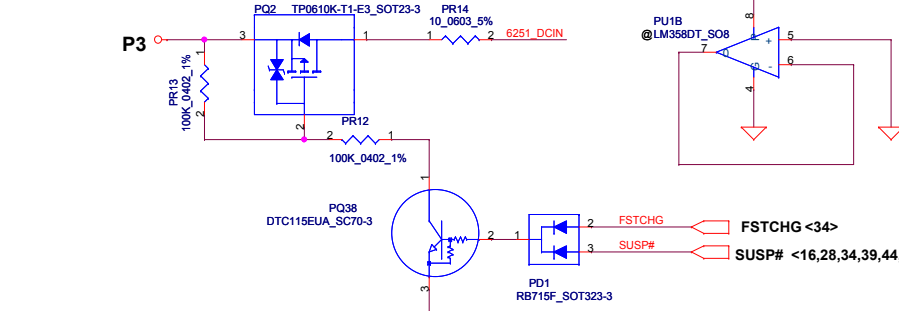
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A-3A
 IREF=1.016*Icharge
 IREF=0.254V-3.048V
 VCHLIM need over 95mV

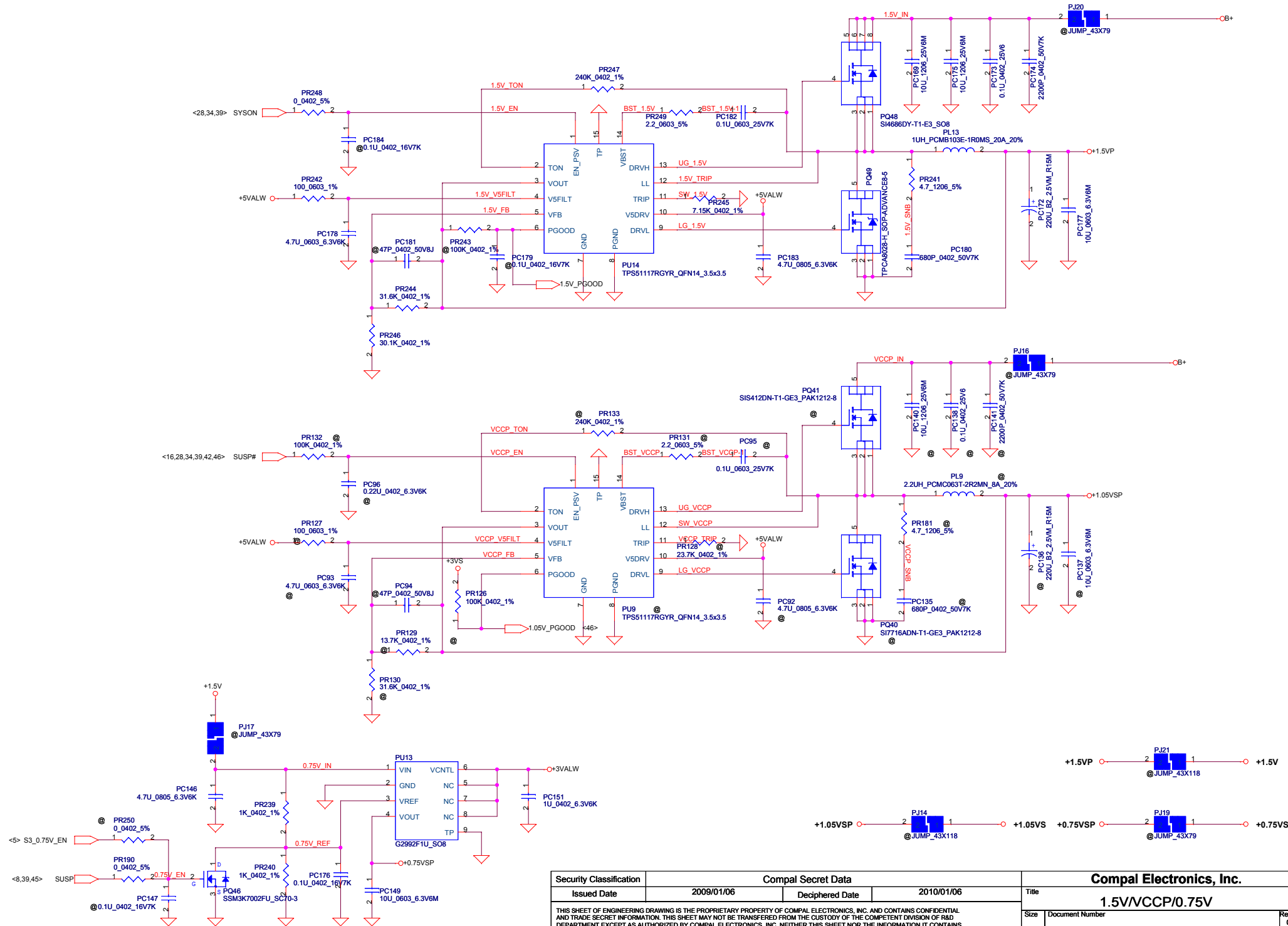
UMA CP mode
 $V_{a\lim} = 2.39 * ((2.26K // 514K) / ((2.26K // 514K) + (21K // 514K))) = 0.239V$
 $input = (1/0.02) * (0.05 * V_{a\lim}) / 2.39 + 0.05$
 where $V_{a\lim} = 0.239V$, $input = 2.75A$

DIS CP mode
 $V_{a\lim} = 2.39 * ((31.6K // 514K) / ((31.6K // 514K) + (21K // 514K))) = 1.425V$
 $input = (1/0.02) * (0.05 * V_{a\lim}) / 2.39 + 0.05$
 where $V_{a\lim} = 1.425V$, $input = 4A$

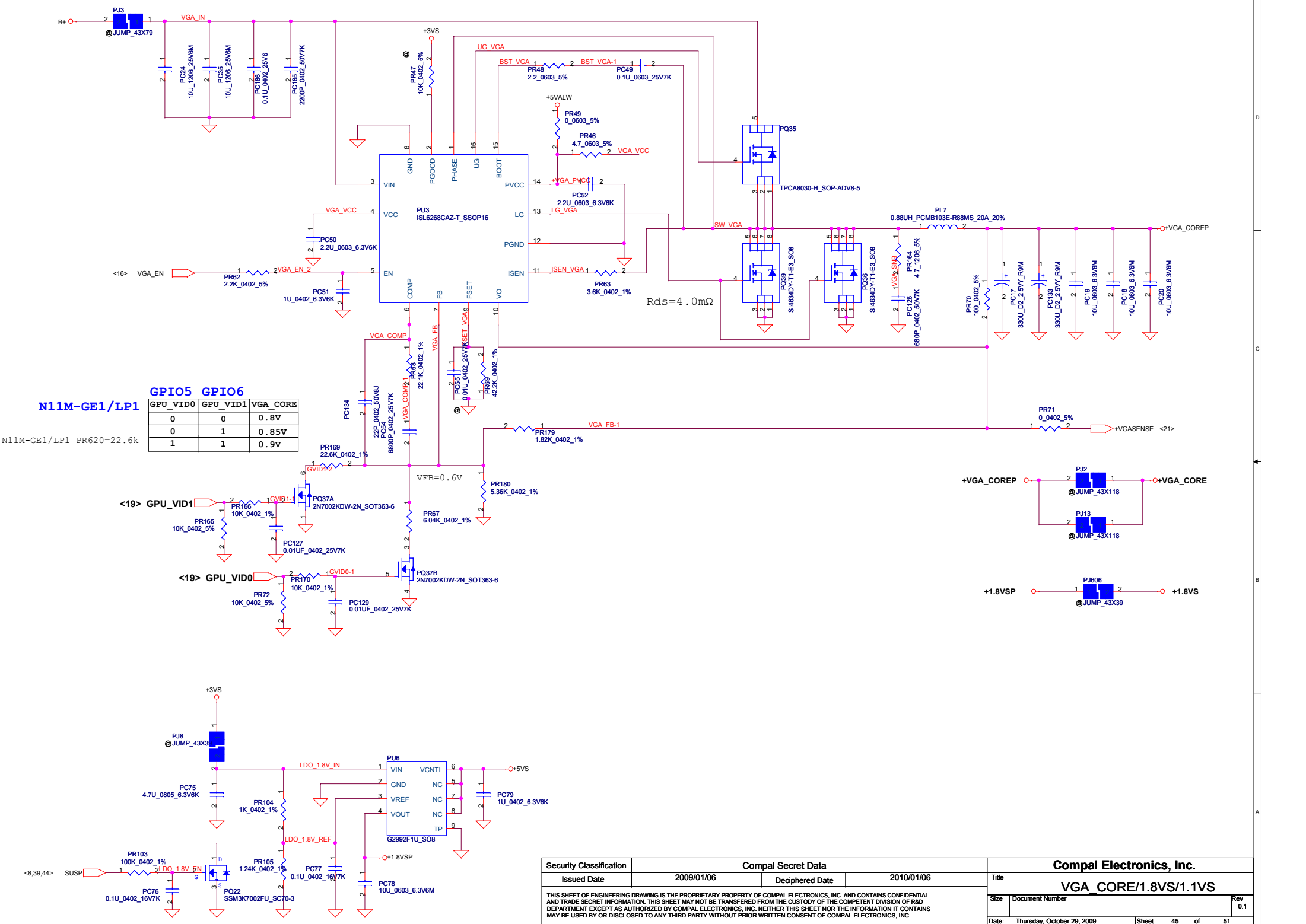
LI-3S : 13.5V --- BATT-OVP=1.5012V
 BATT-OVP=0.1112*VMB
 Per cell=3.5V



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				Document Number
				Rev
				0.1
Date: Thursday, October 29, 2009		Sheet 42 of 51		



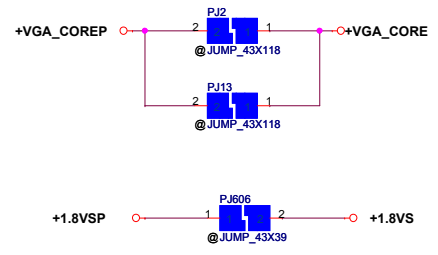
Security Classification		Compal Secret Data		Title	
Issued Date	2009/01/06	Deciphered Date	2010/01/06	1.5V/VCCP/0.75V	
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Date:	Friday, October 30, 2009	Sheet	44	of	51



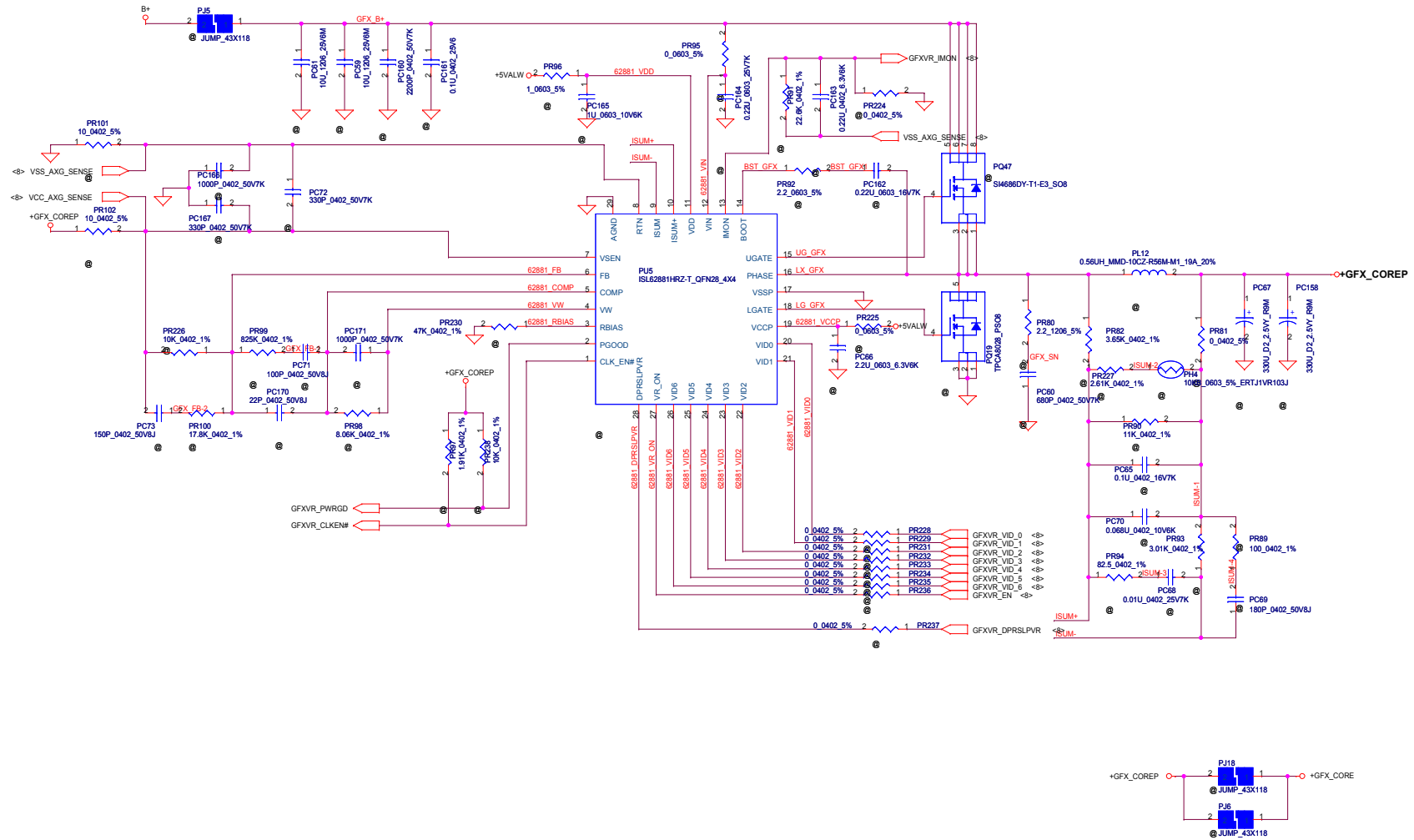
N11M-GE1/LP1

GPIO5	GPIO6	GPU_VID0	GPU_VID1	VGA_CORE
0	0	0	0	0.8V
0	1	0	1	0.85V
1	1	1	1	0.9V

N11M-GE1/LP1 PR620=22.6k

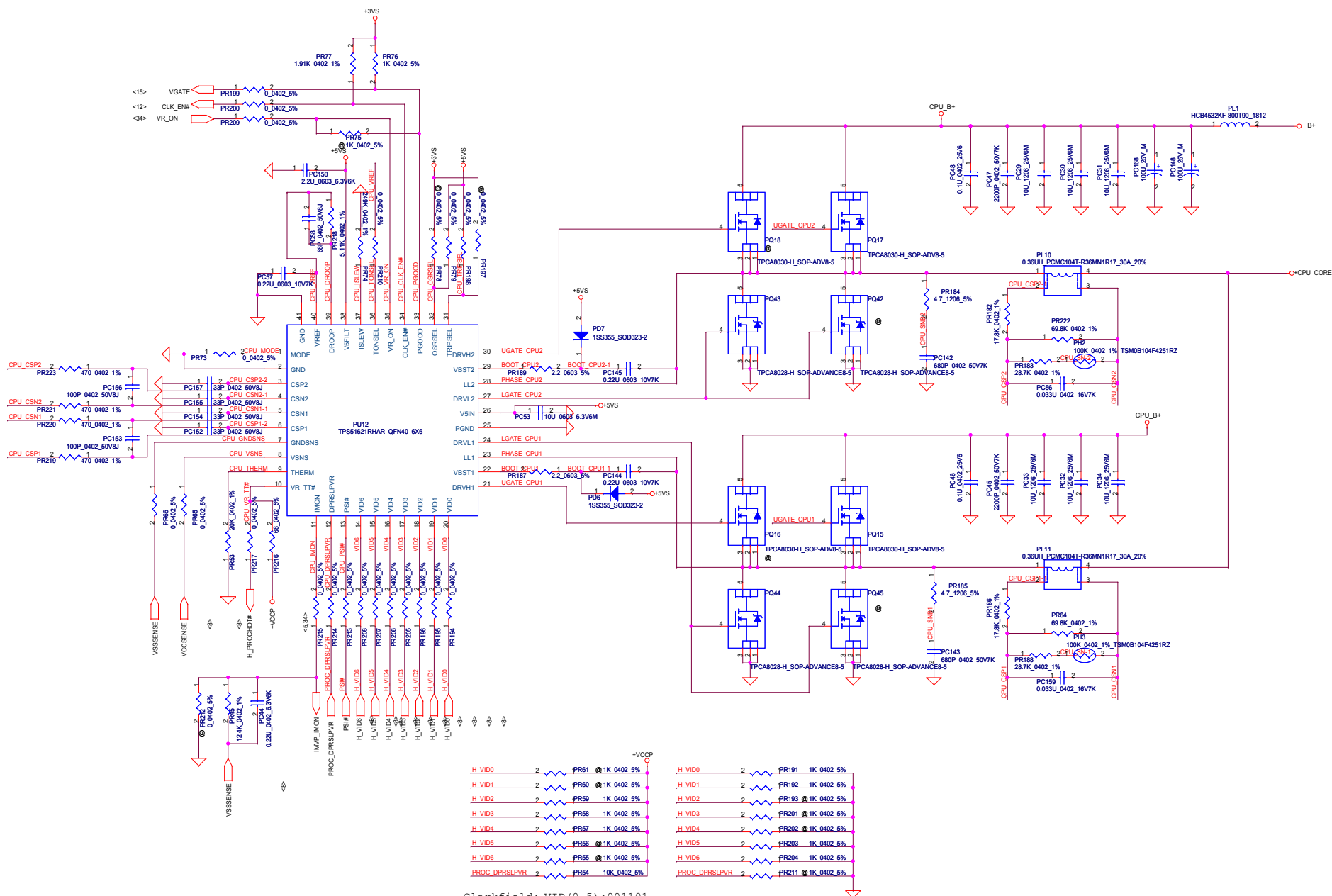


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Date:	Thursday, October 29, 2009	Sheet	45	of 51



(15A,600mils ,Via NO.= 30)

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				Rev
				0.1
Date: Friday, October 30, 2009				Sheet 47 of 51



Clarkfield: VID(0-5):001101
 Auburndale: VID(0-5):001110

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Date:	Thursday, October 28, 2009	Sheet	48	of 51

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17				20081022	

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				Size	Document Number
	Customer	<Doc>		0.1	
Date:	Thursday, October 29, 2009	Sheet	49	of	51

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE	EVT TO DVT
1		P15	Add C638-C645	For UMA HDMI	
2		P05	Add test point for BCLK_ITP, BCLK_ITP#, PRDY#	For XDP connector	
3		P32, P28	Change J6 size & unstuff ODD power control components Change J4 size	Disable ODD power control circuit	
4		P17	Stuff C262	For UMA CRT	
5		P34	Change R291, R294 from +3VALW to +3VS		
6		P38	Add R603 pull high to +3VS	For PM_BTN#	
7		P38	Change JP1 from 6 pin to 8 pin , Change JP8 from 14 pin to 12 pin , unstuff R322	For LED color changed Remove CLK_48M_CR	
8		P29, P34	Change EN_WOL to EN_WOL#	For identify clearly	
9		P34	EC pin26-> EC_FAN_PWM , pin75->PCH_TEMP_ALERT , pin34->PROCHOT# , pin66->NOVO#	EC GPIO arrangement	
10		P31	Change JP12 pin define	For EC FAN control	
11		P16	Change U5 pin3, pin5	POWER , GND reversed	
12		P15	Add U28 for ICH_POK & VGATE	Reserved	
13		P12	Unstuff R278, stuff R269 and change U14 to SA00003HQ00	For low power CLK GEN	
14		P13	Change U3 from 2MBytes to 4MBytes	For 4MBytes SPI ROM for PCH	
15		P29	Correct Q17 to P/N:SB000007600	For +3V_LAN power	
16		P16	Add C646 for BUF_PLT_RST#	Reserved for BUF_PLT_RST# overshoot problem	
17		P36	Change U9 from 2MBytes to 256KBytes	For 256KBytes SPI ROM for EC	
18		P03	UMA_HDMI@ , HDMI@ , BT@ , 3G@ , ESATA@ , CMOS@	New BOM structure	
19		P08	Add R608	For PSI# pull down	
20		P37	Delete D18		
21		P16	Unstuff R210, R212	Set Boot BIOS Strap to SPI	
22		P22	Change & stuff R475 to 30K, R51 to 15K Unstuff R474, R50	For N11M-GE1 QS sample	
23		P25	Unstuff R246	Level shift default setting	
24		P39	Change C373 to DIS@	for DIS power sequence	
25		P15, P16, P17	Change R436 from 1K to 10K Change C447 from 0.1u to 1u Delete R514 Unstuff C493, C494 Reserve R609	Check list Rev2.0 update	
27		P34	Add R607	Reserved for KB926 SPI STRAP PIN	
28		P36	Change LED1, LED3, LED4 to white color LED2 to orang\white color and orange connect to +3VALW		
29		P14	Change exp-card from PCIE port 1 to port 5	SW BIOS request	
30		P38	Unstuff SW1		
31		P13, P34	Change X1, X2 footprint		
32		P12	Change C348 to 22p, C349 to 22p	For Crystal matching	
33		P13, P20	Add C647-C650 12p, stuff C370->22p, R331->33	Reserved for RF team	
34		P36	Delete JP6	SPI ROM socket	
35		P37	Change C430, C615 footprint to B2 type		
36		P27, P32, P37	Change Q4, Q24, Q32, Q37 footprint to A03413		

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HW PIR		
Size B	Document Number LA-5751	Rev 0.3
Date:	Thursday, October 29, 2009	Sheet 50 of 51

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
37		P34	Change C320 to 0805 type	EVT TO DVT
38		P08	Unstuff C268 Change C252, C258 from 10u to 22u	For CPU VDDQ (DDR3 1.5V rails)
39		P34	Change ODD_power_on# from U13 pin28 to pin 76 Add EC_TACH on U13 pin28 to JP12	EC GPIO arrangement
40		P31	Change U20 to EMC1403, add C651	Change thermal sensor solution to EMC1403
41		P05	Add Q42, R610	Reserve for +0.75V enable option
42		P34, P35	Add C652, C653, C654	Reserve for NUM_LED#, CAPS_LED# ESD request
43		P34	Add R611, R612, R613	For EC_FAN_PWM, EC_TACH

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
				DVT TO PVT
1		P34	Reserve R614, R615.	EC_ID to identify KB926 D or E
2		P34	Stuff R607	KB926 SPI STRAP PIN
3		P33	Stuff C632-C635	EMI request
4		P16	Stuff C646	For PLT_RST# signal quality
5		P37	Add R616 100K, change R304 to 100K, C353 to 0.1u	For +3VS_BT power on rising time
6		P37	Changed R304 pin1 from +5VS to +5VALW	For +3VS_BT power on leakage
7		P5	Stuff R283, C338 0.01u	For S3 power reduction
8		P31	Add U29	Colay EMC2103/EMC1403 thermal sensor

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Title		
HW PIR		
Size B	Document Number LA-5751	Rev 0.3
Date:	Thursday, October 29, 2009	Sheet 51 of 51