MODEL	REV	CHANGE LIST
NT11 M/B BOARD	1A	FIRST RELEASE
	2A	PAGE 2 --- CHANGE R577 PULL-UP VOLTAGE TO COREVCC TO AVOID SYSTEM SHUTDOWN WHEN FIRST POWER-ON CHANGE R546 PULL-UP VOLTAGE CPUVIDVCC AS INTEL CRB RECOMMANDATION RESERVE 3V AS CONTROL OF CPUVIDVCC FOR THE ALTERNATIVE METHOD TO TURN-ON CPUVIDVCC CHANGE L46/L47 TO 10uH INDUCTOR AS CRB RECOMMANDATION PAGE 3 --- CHANGE FSBSEL0 TO PULL-UP FOR CORRECTIVE FSB DETECTION FROM CPU PAGE 6 --- CHANGE ICH5 PINB3/PINC2 TO GND AS INTEL RECOMMANDATION PAGE 7 --- CHANGE SODIMM DQMx SIGNAL AS CURRENT PCB REWORK. IT ALSO CAUSE SOME VTT PULL-UP DELETED. CHANGE CHANNEL B SODIMM ADDRESS TO 02 AS INTEL CRB RECOMMANDATION. PAGE 9 --- CORRECT RTC 32.768 XTAL FOOTPRINT RESERVE 1632PG AS SUSPEND POWER WELL CONTROL PIN TO FIX FIRST POWER-ON TOO LONG ISSUE PAGE 10 --- FIXED R205 TO GND FOR 8XAGP SETTING ON NV18M/NV31M PAGE 15 --- CHANGE STRAPING SETTING PER NVIDIA RECOMMANDATION. CHANGE LID SWITCH TO CABLE TYPE INCREASE R343 TO 47K FOR PROPER LCD BACKLIGHT CONTROL PAGE 16 --- CHANGE CB710 IDSEL TO AD17 PAGE 18 --- CHANGE 4-IN-1 FFC CONNECTOR TYPE FOR EASY INSATLLATION FFC CABLE PAGE 19 --- CHANGE 1394 ISDEL TO AD18 PAGE 20 --- CHANGE LAN IDSEL TO AD16 FIXED LANVDD25 CONNECTION ERROR IN DB1 PCB PAGE 21 --- CHANGE MINIPCI IDSEL TO AD19 PAGE 22 --- CHANGE MC7 TO 0.047U FOR NO DIAL-TONE ISSUE PAGE 23 --- REMOVE R620/R626/R3223 TO IMPROVE MIC QUALITY CHANGE CN8 PIN ASSIGNMENT FOR TRACE ROUTING PAGE 24 --- CHANGE R263 PULL-UP TO 3V PAGE 25 --- REVERSE HDD0-HDD7 PIN ASSIGNMENT FOR DESIGN MISTAKE CHANGE FAN1ON/FAN2ON TO FIX FAN NOISE ISSUE REMOVE ALL FAN3 RELATIVE COMPONENT PAGE 26 --- CHANGE ALL BUTTON SWITCH TYPE FOR M/E LIMIATION ADD 2 EXTRA POWER-ON LEDS AND BUFFERS CHANGE Q23 TO 2N7002 FOR DRIVING ISSUE CHANGE CN1 CONNECTOR TYPE FOR M/E LIMIATION PAGE 27 --- CHANGE K/B FFC CONNECTOR TYPE FOR EASY INSTALLATION CHANGE U48 FOOTPRINT TO FIX LAYOUT MISTAKE RESERVE PR8 FOR MX0-MX7 PULL-UP PAGE 28 --- ADD PD33/PD34 FOR CABLE DOCK DESIGN FINE-TUNE PR148/PR60 FOR BATTERY CHARGER PAGE 29 --- ADD Q51 FOR LAN POWER CONTROL PAGE 32 --- CHANGE PR123/PR128 FOR CORRECT COREVCC SENSE
	3A	PAGE 3 --- ADD 200ohm resistor on thermal IC power pin (Maxim recommand) PAGE 4 --- Change some SPD VGA pin to GND as INTEL design guide. PAGE 10 --- Change VGA thermal IC to MAX6649 (nVidai recommand). PAGE 15 --- Reserve VGA2.5V discharge circuit. PAGE 27 --- Reserve -LID pin also routing to EC. (SW request) PAGE 28 --- Change PR16/PR100 value for charger function.

Model / Page	MK1 M/B BOARD FM	MK1 M/B BOARD TO
1	1A	
2	1A	2A
3	1A	3A
4	1A	3A
5	1A	
6	1A	2A
7	1A	2A
8	1A	
9	1A	2A
10	1A	3A
11	1A	
12	1A	
13	1A	
14	1A	
15	1A	3A
16	1A	2A
17	1A	
18	1A	2A
19	1A	2A
20	1A	2A
21	1A	2A
22	1A	2A
23	1A	2A
24	1A	2A
25	1A	2A
26	1A	2A
27	1A	3A
28	1A	3A
29	1A	2A
30	1A	
31	1A	
32	1A	2A
33	1A	

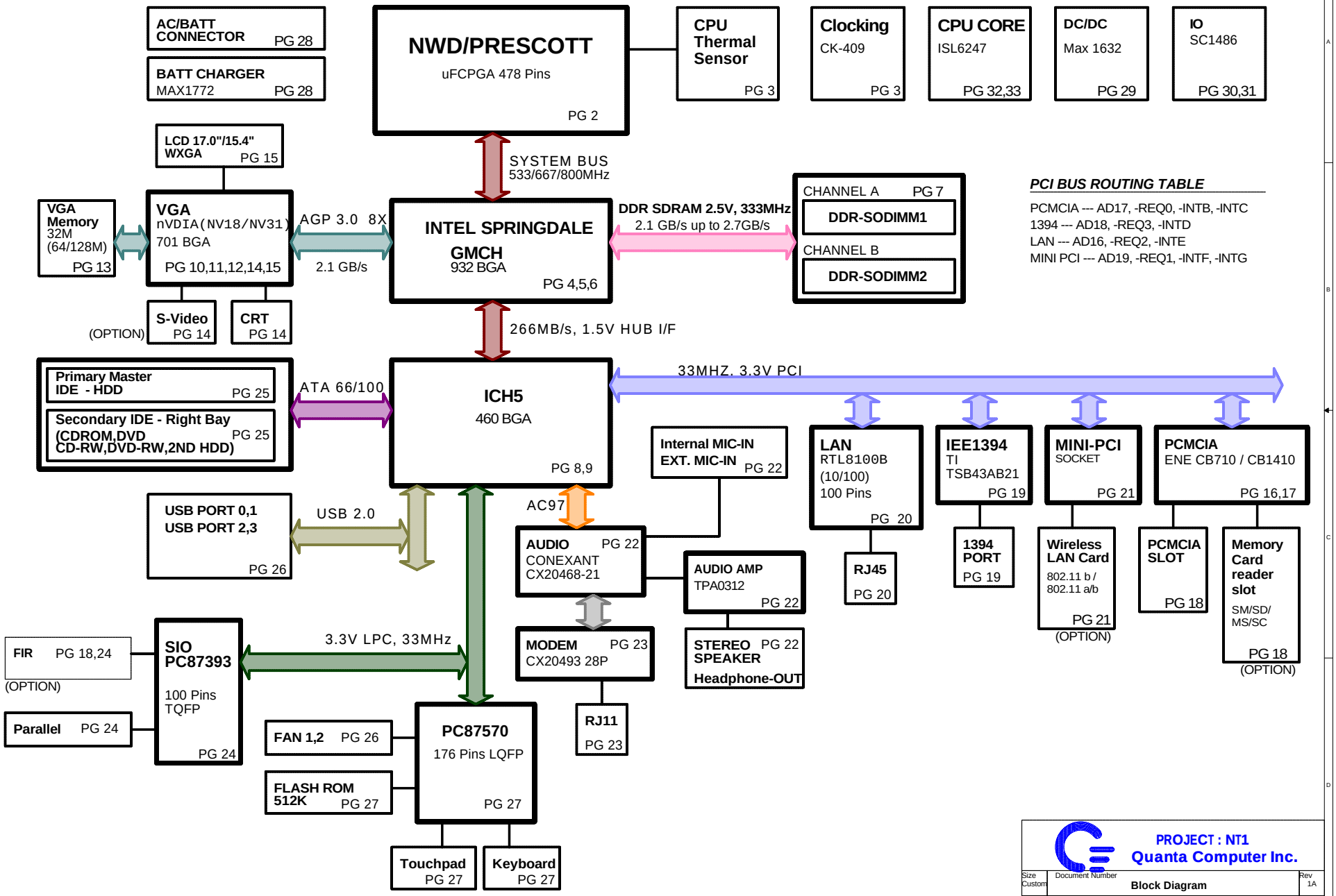
Quanta Computer Inc.	PROJECT : NT1	PCBA NO.31MNT1MB0010	REV :2B	DOC. NO:
	APPROVED BY :Tim Yys	CHECK BY:Carey Chen	DRAWING BY:Gill Peng	DATE :04/21/2003 SHEET 2

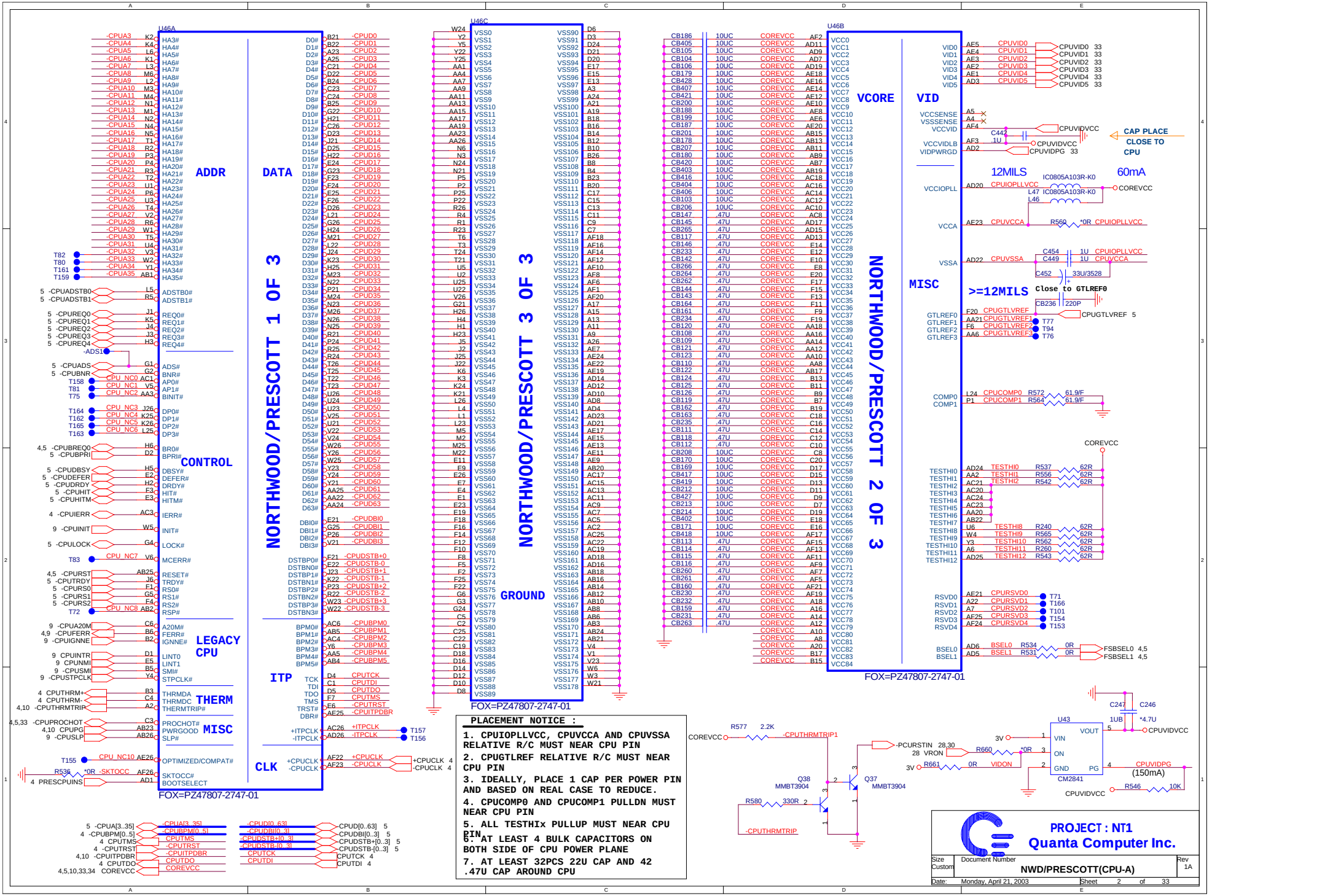
MODEL	REV	CHANGE LIST
NT11 M/B BOARD	4A	PAGE 11 --- ADD 2ND CHIP SELECT TO SUPPOT TWO CS TYPE 8Mx32 DDR VRAM. ADD NV31M PIN P27 AND D14 TO VRAM FOR2ND CS. PAGE 12 --- THE STRAPPED PINS NEED TO CHANGE FOR TWO CS TYPE VRAM; TO BE CONFIRMED BY NVIDIA. (TO BE CONFIRMED) PAGE 13 --- ADD 2ND CHIP SELECT TO SUPPOT TWO CS TYPE 8Mx32 DDR VRAM. ADD VRAM PIN L3 AS 2N CS. PAGE 26 --- INCREASE USB PORT POWER FROM 0.5A TO 1A TO SUPPORT USB HDD DEVICE. SHORT U33/U34 PIN 5 AND 8 TO INCREASE POWER. PAGE 28 --- CHNANGE BAT-IN INDUCTOR TO AVOID ME INTERFENCE IN SI1 UNIT. USE 2 FBMJ3216HS480 TO REPLACE FBMH453281-T. PAGE 29 --- ADD VGA2.5 DISCHARGE CIRCUIT TO MEET NVIDAI POWER SEQUENCE. ADD PQ74, PQ74, R172 AD R172 TO CONTROL DISCHARGE TIME. PAGE 30 --- FINE TUNE VGACORE CIRCUIT. 1. CHNAGE PU1 FROMLM358 TO LMV321. (POWERED BY 5V) 2. CHANGE PR1 FROM 10K TO 4.7K AND ADD PR173 4.7OHM RESISTOR TO IMPROVE RESPONSE TIME. 3. CHANGE PC80 BULK CAPACITOR FROM 100U TO 330U FOR BIG CURRENT. 4. ADD PC175 100PF TO FLTER HIGH FREQ NOISE.

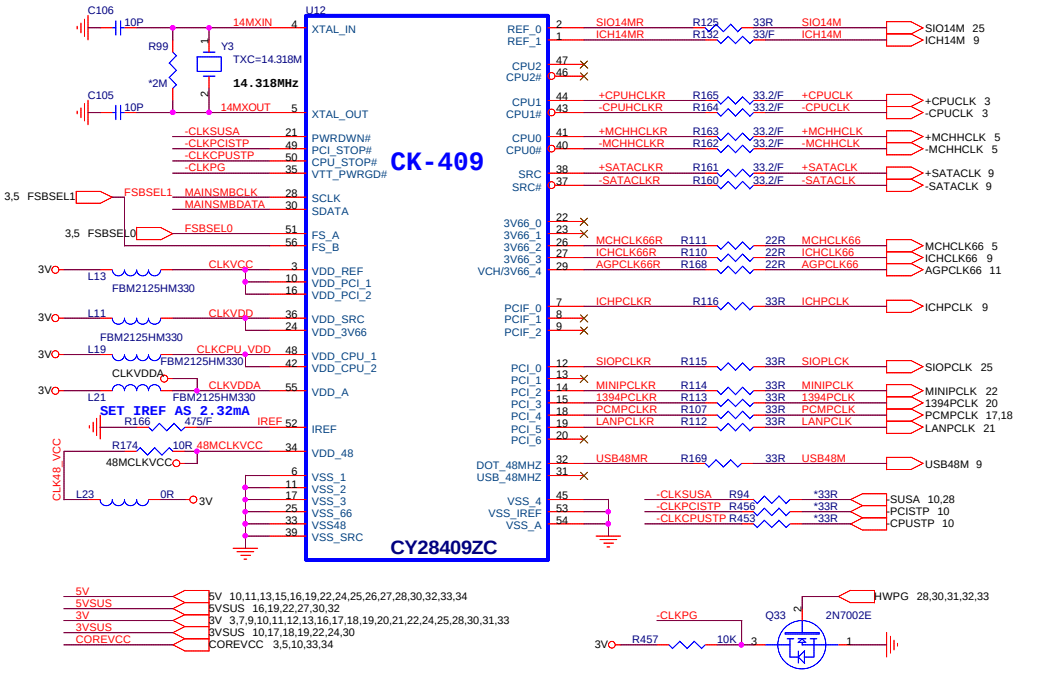
Model / Page	MK1 M/B BOARD FM	MK1 M/B BOARD TO
1	1A	
2	1A	2A
3	1A	3A
4	1A	3A
5	1A	
6	1A	2A
7	1A	2A
8	1A	
9	1A	2A
10	1A	3A
11	1A	4A
12	1A	4A
13	1A	4A
14	1A	
15	1A	3A
16	1A	2A
17	1A	
18	1A	2A
19	1A	2A
20	1A	2A
21	1A	2A
22	1A	2A
23	1A	2A
24	1A	2A
25	1A	2A
26	1A	4A
27	1A	3A
28	1A	4A
29	1A	4A
30	1A	4A
31	1A	
32	1A	2A
33	1A	

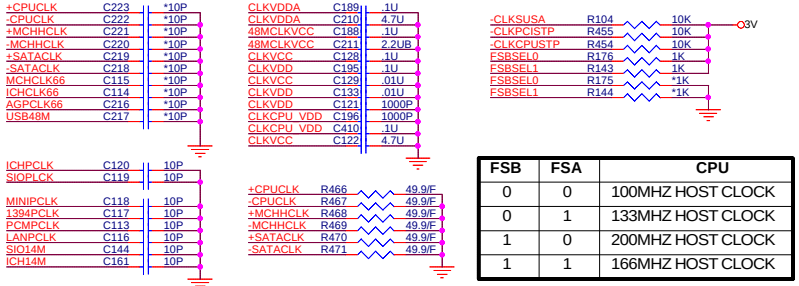
Quanta Computer Inc.	PROJECT : NT1	PCBA NO.31MNT1MB0010	REV : 2B	DOC. NO:
	APPROVED BY :Tim Yys	CHECK BY:Carey Chen	DRAWING BY:Gill Peng	DATE :04/21/2003 SHEET 1

NT1 - Block Diagram

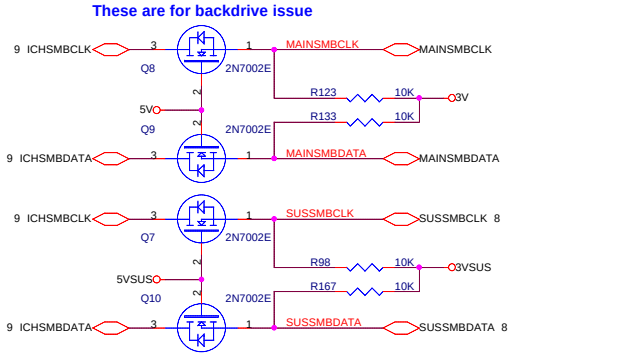



U46A
NORTHWOOD/PRESCOTT 1 OF 3
ADDR
DATA
CONTROL
LEGACY CPU
THERM
MISC
CLK
ITP
FOX=PZ47807-2747-01
U46C
NORTHWOOD/PRESCOTT 3 OF 3
GROUND
FOX=PZ47807-2747-01
U46B
NORTHWOOD/PRESCOTT 2 OF 3
VCORE
VID
MISC
FOX=PZ47807-2747-01
PLACEMENT NOTICE :
1. CPUIOPLLVCC, CPUVCCA AND CPUVSSA RELATIVE R/C MUST NEAR CPU PIN
2. CPUGTLREF RELATIVE R/C MUST NEAR CPU PIN
3. IDEALLY, PLACE 1 CAP PER POWER PIN AND BASED ON REAL CASE TO REDUCE.
4. CPUCOMP0 AND CPUCOMP1 PULLDN MUST NEAR CPU PIN
5. ALL TESTHIx PULLUP MUST NEAR CPU PIN
6. AT LEAST 4 BULK CAPACITORS ON BOTH SIDE OF CPU POWER PLANE
7. AT LEAST 32PCS 22U CAP AND 42 .47U CAP AROUND CPU
CAP PLACE CLOSE TO CPU
12MILS
60mA
>=12MILS
Close to GTLREF0
Q38 MMBT3904
Q37 MMBT3904
CM2841
(150mA)
PROJECT : NT1
Quanta Computer Inc.
NWD/PRESCOTT(CPU-A)
Monday, April 21, 2003
Sheet 2 of 33



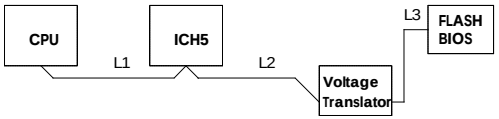


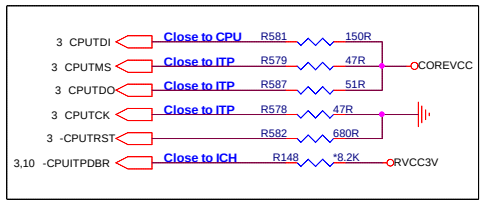
FSB	FSA	CPU
0	0	100MHZ HOST CLOCK
0	1	133MHZ HOST CLOCK
1	0	200MHZ HOST CLOCK
1	1	166MHZ HOST CLOCK

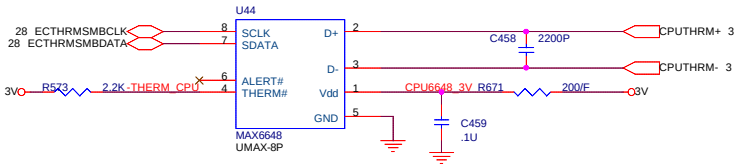


EX. -INIT

Trace Spacing	L1	L2	L3
5mils	17 inches maximum	2 inches maximum	10 inches maximum

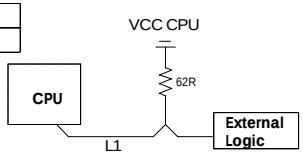


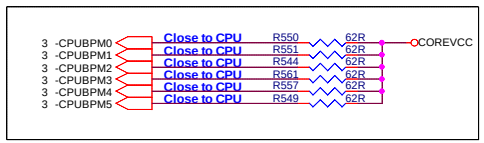




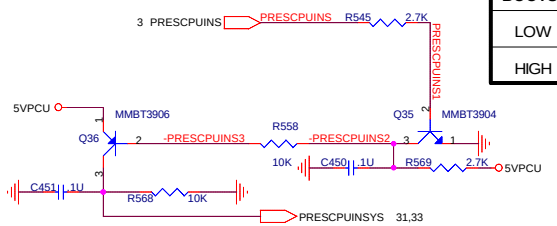
EX. -IERR

Trace Spacing	L1
7mils	1 inch maximum





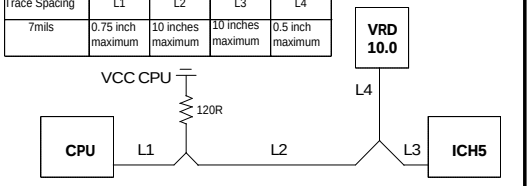
BOOTSEL	CPU	VTT_GMCH
LOW	NORTHWOOD	1.45V
HIGH	PRESCOOT	1.2V

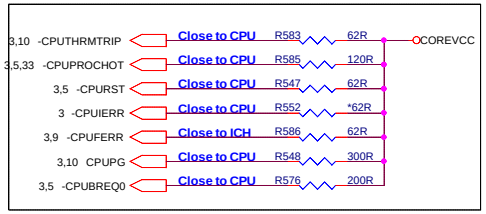


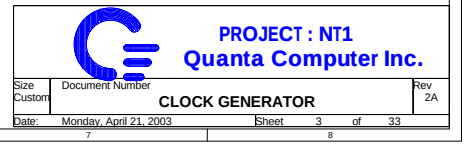
SHOULD CONSIDER WITH POWER CONTROL PIN MAINON AND VRON
VRON SHOULD CONSIDER -CPUINS TO TURN ON COREVCC

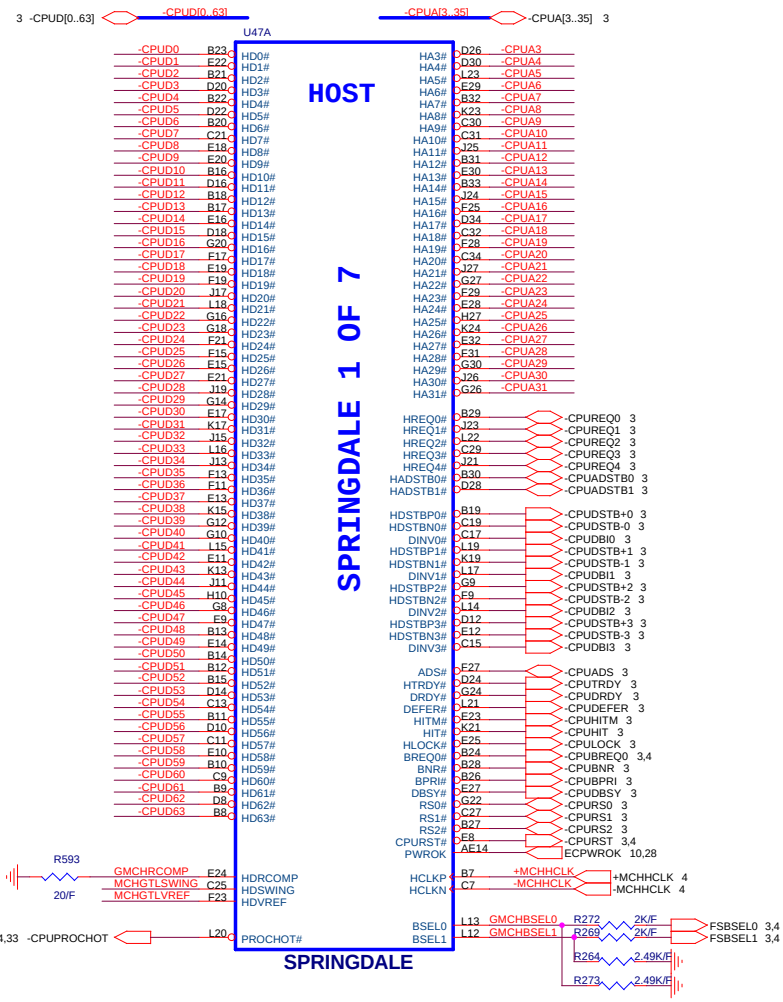
EX. -CPUPROCHOT

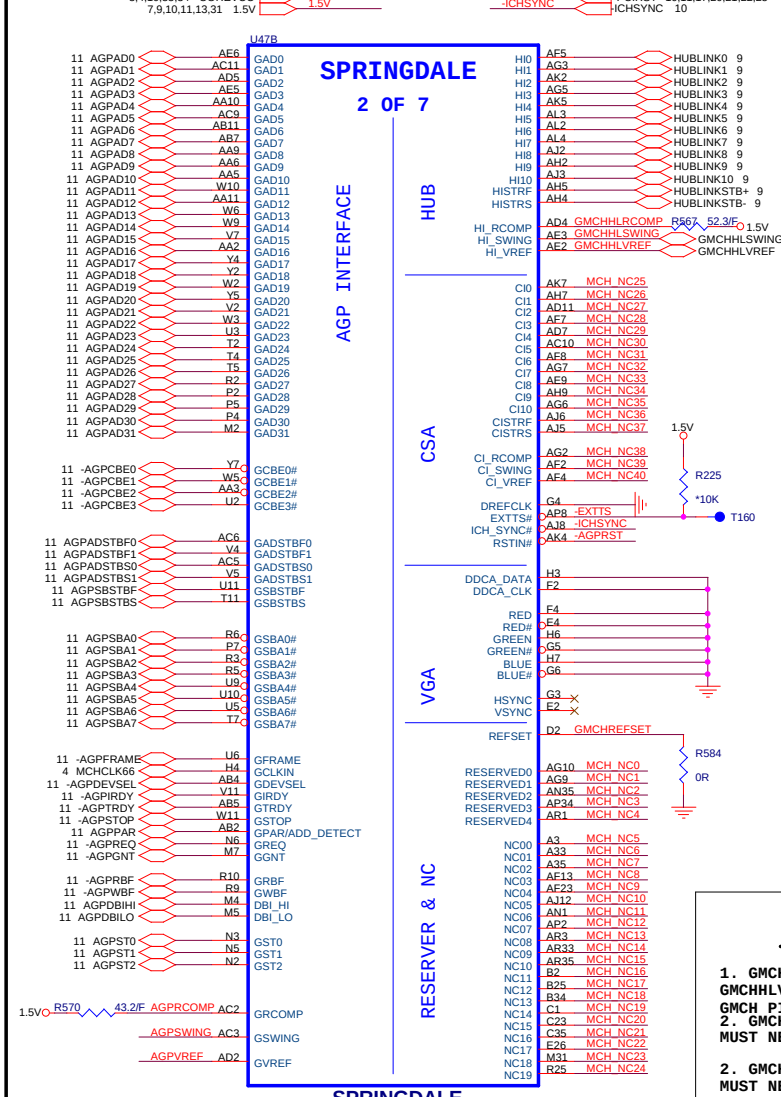
Trace Spacing	L1	L2	L3	L4
7mils	0.75 inch maximum	10 inches maximum	10 inches maximum	0.5 inch maximum

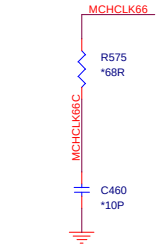










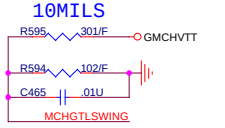


ANALOG RGB/CRT GUIDELINES FOR SPRINGDALE-P

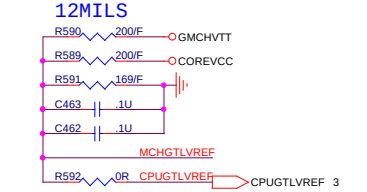
SIGNAL	GUIDELINE
RED,GREEN,BLUE	TIE DIRECTLY TO GND
RED#,GREEN#,BLUE#	TIE DIRECTLY TO GND
VCCA_DAC	TIE DIRECTLY TO GND
VSSA_DAC	TIE DIRECTLY TO GND
VCCA_DPLL	TIE DIRECTLY TO GND
REFSET	TIE DIRECTLY TO GND
DREFCLK	TIE DIRECTLY TO GND
HSYNC	NO CONNECT
VSYNC	NO CONNECT
DDCA_DATA	TIE DIRECTLY TO GND
DDCA_CLK	TIE DIRECTLY TO GND

PLACEMENT NOTICE :

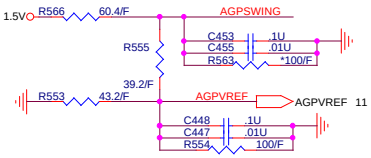
1. GMCHSWING, GMCHVREF, GMCHHLSWING, GMCHHLVREF RELATIVE R/C MUST NEAR GMCH PIN
2. GMCHRCOMP AND AGPRCOMP RELATIVE R/C MUST NEAR GMCH PIN
2. GMCHRCOMP AND AGPRCOMP RELATIVE R/C MUST NEAR GMCH PIN
3. GMCHREFSET R/C MUST NEAR GMCH PIN
4. GMCHHLRCOMP R/C MUST NEAR GMCH PIN
5. GMCHBSEL0 AND GMCHBSEL1 MUST NEAR GMCH PIN
6. -AGPRST R/C MUST NEAR GMCH PIN



GMCHSWING = 1/4 * GMCHVTT

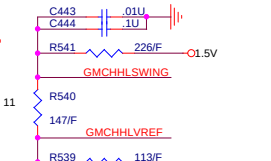


GMCHVREF = 0.63 * (GMCHVTT+COREVCC)/2



AGPSWING = 0.8V +/- 2%
AGPSVREF = 0.35V FOR 8X AGP
AGPSVREF = 0.75V FOR 4X AGP

Fixed as 8XAGP



GMCHHLSWING = 0.8V+/- 2%
GMCHHLVREF = 0.35V+/- 2%

PROJECT : NT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	GMCH(Processor System Bus)	2A
Date: Monday, April 21, 2003	Sheet 4 of 33	

U47C

SPRINGDALE

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DDR

CHANNEL A

DDRMDA0	AP10	SDQ_A0	SDQS_A0	AN11	DDRDQSA0
DDRMDA1	AP11	SDQ_A1	SDQS_A1	AP15	DDRDQSA1
DDRMDA2	AM12	SDQ_A2	SDQS_A2	AP23	DDRDQSA2
DDRMDA3	AN13	SDQ_A3	SDQS_A3	AM30	DDRDQSA3
DDRMDA4	AM10	SDQ_A4	SDQS_A4	AF34	DDRDQSA4
DDRMDA5	AL10	SDQ_A5	SDQS_A5	V34	DDRDQSA5
DDRMDA6	AL12	SDQ_A6	SDQS_A6	M32	DDRDQSA6
DDRMDA7	AP13	SDQ_A7	SDQS_A7	H31	DDRDQSA7
DDRMDA8	AP14	SDQ_A8			
DDRMDA9	AM14	SDQ_A9			
DDRMDA10	AL18	SDQ_A10	SDM_A0	AP12	SDMA0_NC → T84
DDRMDA11	AP19	SDQ_A11	SDM_A1	AP16	SDMA1_NC → T85
DDRMDA12	AL14	SDQ_A12	SDM_A2	AM24	SDMA2_NC → T95
DDRMDA13	AN15	SDQ_A13	SDM_A3	AP30	SDMA3_NC → T99
DDRMDA14	AP18	SDQ_A14	SDM_A4	AF31	SDMA4_NC → T102
DDRMDA15	AM18	SDQ_A15	SDM_A5	W33	SDMA5_NC → T106
DDRMDA16	AP22	SDQ_A16	SDM_A6	M34	SDMA6_NC → T107
DDRMDA17	AM22	SDQ_A17	SDM_A7	H32	SDMA7_NC → T109
DDRMDA18	AL24	SDQ_A18			
DDRMDA19	AN27	SDQ_A19			
DDRMDA20	AP21	SDQ_A20	SMAA_A0	AJ34	DDRMAA0
DDRMDA21	AL22	SDQ_A21	SMAA_A1	AL33	DDRMAA1
DDRMDA22	AP25	SDQ_A22	SMAA_A2	AK29	DDRMAA2
DDRMDA23	AP27	SDQ_A23	SMAA_A3	AN31	DDRMAA3
DDRMDA24	AP28	SDQ_A24	SMAA_A4	AL30	DDRMAA4
DDRMDA25	AP29	SDQ_A25	SMAA_A5	AL26	DDRMAA5
DDRMDA26	AP33	SDQ_A26	SMAA_A6	AL28	DDRMAA6
DDRMDA27	AM33	SDQ_A27	SMAA_A7	AN25	DDRMAA7
DDRMDA28	AM28	SDQ_A28	SMAA_A8	AP26	DDRMAA8
DDRMDA29	AN29	SDQ_A29	SMAA_A9	AP24	DDRMAA9
DDRMDA30	AM31	SDQ_A30	SMAA_A10	AJ33	DDRMAA10
DDRMDA31	AN34	SDQ_A31	SMAA_A11	AN23	DDRMAA11
DDRMDA32	AH32	SDQ_A32	SMAA_A12	AN21	DDRMAA12
DDRMDA33	AG34	SDQ_A33			
DDRMDA34	AF32	SDQ_A34			
DDRMDA35	AD32	SDQ_A35	SMAB_A1	AL34	DDRMAAB1_NC
DDRMDA36	AH31	SDQ_A36	SMAB_A2	AM34	DDRMAAB2_NC
DDRMDA37	AG33	SDQ_A37	SMAB_A3	AP32	DDRMAAB3_NC
DDRMDA38	AE34	SDQ_A38	SMAB_A4	AP31	DDRMAAB4_NC
DDRMDA39	AD34	SDQ_A39	SMAB_A5	AM26	DDRMAAB5_NC
DDRMDA40	AC34	SDQ_A40			
DDRMDA41	AB31	SDQ_A41			
DDRMDA42	V32	SDQ_A42	SWE_A#	AB34	-DDRWEA
DDRMDA43	V31	SDQ_A43	SCAS_A#	Y34	-DDRCASA
DDRMDA44	AD31	SDQ_A44	SRAS_A#	AC33	-DDRRASA
DDRMDA45	AB32	SDQ_A45			
DDRMDA46	U34	SDQ_A46			
DDRMDA47	U33	SDQ_A47	SBA_A0	AE33	DDRBAA0
DDRMDA48	T34	SDQ_A48	SBA_A1	AH34	DDRBAA1
DDRMDA49	T32	SDQ_A49			
DDRMDA50	K34	SDQ_A50			
DDRMDA51	K32	SDQ_A51	SCS_A0#	AA34	-DDRCSA0
DDRMDA52	T31	SDQ_A52	SCS_A1#	Y31	-DDRCSA1
DDRMDA53	P34	SDQ_A53	SCS_A2#	Y32	-DDRCSA2_NC
DDRMDA54	L34	SDQ_A54	SCS_A3#	W34	-DDRCSA3_NC
DDRMDA55	L33	SDQ_A55			
DDRMDA56	J33	SDQ_A56			
DDRMDA57	H34	SDQ_A57	SCKE_A0	AL20	DDRCKEA0
DDRMDA58	F33	SDQ_A58	SCKE_A1	AN19	DDRCKEA1
DDRMDA59	F33	SDQ_A59	SCKE_A2	AM20	DDRCKEA2_NC
DDRMDA60	K31	SDQ_A60	SCKE_A3	AP20	DDRCKEA3_NC
DDRMDA61	J34	SDQ_A61			
DDRMDA62	G34	SDQ_A62			
DDRMDA63	F34	SDQ_A63			
			SCMDCLK_A0	AK32	+DIMMCLKA0
			SCMDCLK_A0#	AK31	-DIMMCLKA0
			SCMDCLK_A1	AP17	+DIMMCLKA1
			SCMDCLK_A1#	AN17	-DIMMCLKA1
			SCMDCLK_A2	N33	+DIMMCLKA2
			SCMDCLK_A2#	N34	-DIMMCLKA2
			SCMDCLK_A3	AK33	+DIMMCLKA3_NC
			SCMDCLK_A3#	AK34	-DIMMCLKA3_NC
			SCMDCLK_A4	AM16	+DIMMCLKA4_NC
			SCMDCLK_A4#	AL16	-DIMMCLKA4_NC
			SCMDCLK_A5	P31	+DIMMCLKA5_NC
			SCMDCLK_A5#	P32	-DIMMCLKA5_NC
MEMVREFA	E34	SMVREF_A			
MEMXRCOMP	AK9	SMXRCOMP			
MEMXRCOMPVOH	AN9	SMXRCOMPVOH			
MEMXRCOMPVOL	AL9	SMXRCOMPVOL			

SPRINGDALE

U47D

SPRINGDALE

4 OF 7

DDR

CHANNEL B

DDRMDB0	AJ10	SDQ_B0	SDQS_B0	AF15	DDRDQSB0
DDRMDB1	AE15	SDQ_B1	SDQS_B1	AG13	DDRDQSB1
DDRMDB2	AL11	SDQ_B2	SDQS_B2	AG21	DDRDQSB2
DDRMDB3	AE16	SDQ_B3	SDQS_B3	AH27	DDRDQSB3
DDRMDB4	AL8	SDQ_B4	SDQS_B4	AD29	DDRDQSB4
DDRMDB5	AF12	SDQ_B5	SDQS_B5	U30	DDRDQSB5
DDRMDB6	AK11	SDQ_B6	SDQS_B6	L27	DDRDQSB6
DDRMDB7	AG12	SDQ_B7	SDQS_B7	J30	DDRDQSB7
DDRMDB8	AE17	SDQ_B8			
DDRMDB9	AL13	SDQ_B9			
DDRMDB10	AK17	SDQ_B10	SDM_B0	AG11	SDMB0_NC → T86
DDRMDB11	AL17	SDQ_B11	SDM_B1	AG15	SDMB1_NC → T89
DDRMDB12	AK13	SDQ_B12	SDM_B2	AE21	SDMB2_NC → T96
DDRMDB13	AJ14	SDQ_B13	SDM_B3	AJ28	SDMB3_NC → T100
DDRMDB14	AJ16	SDQ_B14	SDM_B4	AC31	SDMB4_NC → T103
DDRMDB15	AJ18	SDQ_B15	SDM_B5	U31	SDMB5_NC → T104
DDRMDB16	AE19	SDQ_B16	SDM_B6	M29	SDMB6_NC → T105
DDRMDB17	AE20	SDQ_B17	SDM_B7	J31	SDMB7_NC → T108
DDRMDB18	AG23	SDQ_B18			
DDRMDB19	AK23	SDQ_B19			
DDRMDB20	AL19	SDQ_B20	SMAA_B0	AG31	DDRMAB0
DDRMDB21	AK21	SDQ_B21	SMAA_B1	AJ31	DDRMAB1
DDRMDB22	AJ24	SDQ_B22	SMAA_B2	AD27	DDRMAB2
DDRMDB23	AE22	SDQ_B23	SMAA_B3	AE24	DDRMAB3
DDRMDB24	AK25	SDQ_B24	SMAA_B4	AK27	DDRMAB4
DDRMDB25	AH26	SDQ_B25	SMAA_B5	AG25	DDRMAB5
DDRMDB26	AG27	SDQ_B26	SMAA_B6	AL25	DDRMAB6
DDRMDB27	AF27	SDQ_B27	SMAA_B7	AF21	DDRMAB7
DDRMDB28	AJ26	SDQ_B28	SMAA_B8	AL23	DDRMAB8
DDRMDB29	AJ27	SDQ_B29	SMAA_B9	AJ22	DDRMAB9
DDRMDB30	AD25	SDQ_B30	SMAA_B10	AF29	DDRMAB10
DDRMDB31	AF28	SDQ_B31	SMAA_B11	AL21	DDRMAB11
DDRMDB32	AE30	SDQ_B32	SMAA_B12	AJ20	DDRMAB12
DDRMDB33	AC27	SDQ_B33			
DDRMDB34	AC30	SDQ_B34			
DDRMDB35	Y29	SDQ_B35	SMAB_B1	AE27	DDRMABB1_NC
DDRMDB36	AE31	SDQ_B36	SMAB_B2	AD26	DDRMABB2_NC
DDRMDB37	AB29	SDQ_B37	SMAB_B3	AL29	DDRMABB3_NC
DDRMDB38	AA26	SDQ_B38	SMAB_B4	AL27	DDRMABB4_NC
DDRMDB39	AA27	SDQ_B39	SMAB_B5	AE23	DDRMABB5_NC
DDRMDB40	AA30	SDQ_B40			
DDRMDB41	W30	SDQ_B41			
DDRMDB42	U27	SDQ_B42	SWE_B#	W27	-DDRWEB
DDRMDB43	T25	SDQ_B43	SCAS_B#	W31	-DDRCASB
DDRMDB44	AA31	SDQ_B44	SRAS_B#	W26	-DDRRASB
DDRMDB45	V29	SDQ_B45			
DDRMDB46	U25	SDQ_B46			
DDRMDB47	R27	SDQ_B47	SBA_B0	Y25	DDRBAB0
DDRMDB48	P29	SDQ_B48	SBA_B1	AA25	DDRBAB1
DDRMDB49	R30	SDQ_B49			
DDRMDB50	K28	SDQ_B50			
DDRMDB51	L30	SDQ_B51	SCS_B0#	U26	-DDRCSB0
DDRMDB52	R31	SDQ_B52	SCS_B1#	T29	-DDRCSB1
DDRMDB53	R26	SDQ_B53	SCS_B2#	V25	-DDRCSB2_NC
DDRMDB54	P25	SDQ_B54	SCS_B3#	W25	-DDRCSB3_NC
DDRMDB55	L32	SDQ_B55			
DDRMDB56	K30	SDQ_B56			
DDRMDB57	H29	SDQ_B57	SCKE_B0	AK19	DDRCKEB0
DDRMDB58	F32	SDQ_B58	SCKE_B1	AF19	DDRCKEB1
DDRMDB59	G33	SDQ_B59	SCKE_B2	AG19	DDRCKEB2_NC
DDRMDB60	N25	SDQ_B60	SCKE_B3	AE18	DDRCKEB3_NC
DDRMDB61	M25	SDQ_B61			
DDRMDB62	J29	SDQ_B62			
DDRMDB63	G32	SDQ_B63			
			SCMDCLK_B0	AG29	+DIMMCLKB0
			SCMDCLK_B0#	AG30	-DIMMCLKB0
			SCMDCLK_B1	AF17	+DIMMCLKB1
			SCMDCLK_B1#	AG17	-DIMMCLKB1
			SCMDCLK_B2	N27	+DIMMCLKB2
			SCMDCLK_B2#	N26	-DIMMCLKB2
			SCMDCLK_B3	AJ30	+DIMMCLKB3_NC
			SCMDCLK_B3#	AH29	-DIMMCLKB3_NC
			SCMDCLK_B4	AK15	+DIMMCLKB4_NC
			SCMDCLK_B4#	AL15	-DIMMCLKB4_NC
			SCMDCLK_B5	N31	+DIMMCLKB5_NC
			SCMDCLK_B5#	N30	-DIMMCLKB5_NC
MEMVREFB	AP9	SMVREF_B			
MEMYRCOMP	AA33	SMYRCOMP			
MEMYRCOMPVOH	R34	SMYRCOMPVOH			
MEMYRCOMPVOL	R33	SMYRCOMPVOL			

SPRINGDALE

+DIMMCLKA[0..2] → +DIMMCLKA[0..2] 8
-DIMMCLKA[0..2] → -DIMMCLKA[0..2] 8
DDRMDA[0..63] → DDRMDA[0..63] 8
DDRMAA[0..12] → DDRMAA[0..12] 8

DDRBAA[0..1] → DDRBAA[0..2] 8
DDRDQSA[0..7] → DDRDQSA[0..7] 8

-DDRCSA[0..1] → -DDRCSA[0..1] 8
DDRCKEA[0..1] → DDRCKEA[0..1] 8
-DDRRASA → -DDRRASA 8
-DDRCASA → -DDRCASA 8
-DDRWEA → -DDRWEA 8

+DIMMCLKB[0..2] → +DIMMCLKB[0..2] 8
-DIMMCLKB[0..2] → -DIMMCLKB[0..2] 8
DDRMDB[0..63] → DDRMDB[0..63] 8
DDRMAB[0..12] → DDRMAB[0..12] 8

DDRBAB[0..1] → DDRBAB[0..2] 8
DDRDQSB[0..7] → DDRDQSB[0..7] 8

-DDRCSB[0..1] → -DDRCSB[0..1] 8
DDRCKEB[0..1] → DDRCKEB[0..1] 8
-DDRRASB → -DDRRASB 8
-DDRCASB → -DDRCASB 8
-DDRWEB → -DDRWEB 8

2.55VSUS → 2.55VSUS 7,8,16,32

PLACEMENT NOTICE :

1. MEMXRCOMP AND MEMYRCOMP RELATIVE R/C MUST NEAT GMCH PIN

2. MEMXRCOMPVOH AND MEMYRCOMPVOH RELATIVE R/C MUST NEAT GMCH PIN

2. MEMXRCOMPVOL AND MEMYRCOMPVOL RELATIVE R/C MUST NEAT GMCH PIN

3. MEMVREFA AND MEMVREFB RELATIVE R/C MUST NEAT GMCH PIN

MEMXRCOMP — R230 42.2/F — 2.55VSUS; R229 42.2/F; 2.55VSUS — C259 .01U; C260 *2.2UB

MEMXRCOMPVOL — R227 31.6K/F — 2.55VSUS; R226 10K/F; 2.55VSUS — C257 .01U; C256 *2.2UB

VALUES STILL NEED VERIFICATION

MEMXRCOMPVOH — R241 10K/F — 2.55VSUS; R242 31.6K/F; 2.55VSUS — C267 .01U; C266 *2.2UB

MEMVREFA — R596 150/F — 2.55VSUS; R597 150/F — C468 .01U; C467 *2.2UB

PLACE RESISTORS WITHIN 1 INCH OF DIMMS

MEMYRCOMP — R281 42.2/F — 2.55VSUS; R280 42.2/F; 2.55VSUS — C279 .01U; C280 *2.2UB

MEMYRCOMPVOL — R286 31.6K/F — 2.55VSUS; R285 10K/F; 2.55VSUS — C283 .01U; C282 *2.2UB

VALUES STILL NEED VERIFICATION

MEMYRCOMPVOH — R288 10K/F — 2.55VSUS; R287 31.6K/F; 2.55VSUS — C292 .01U; C288 *2.2UB

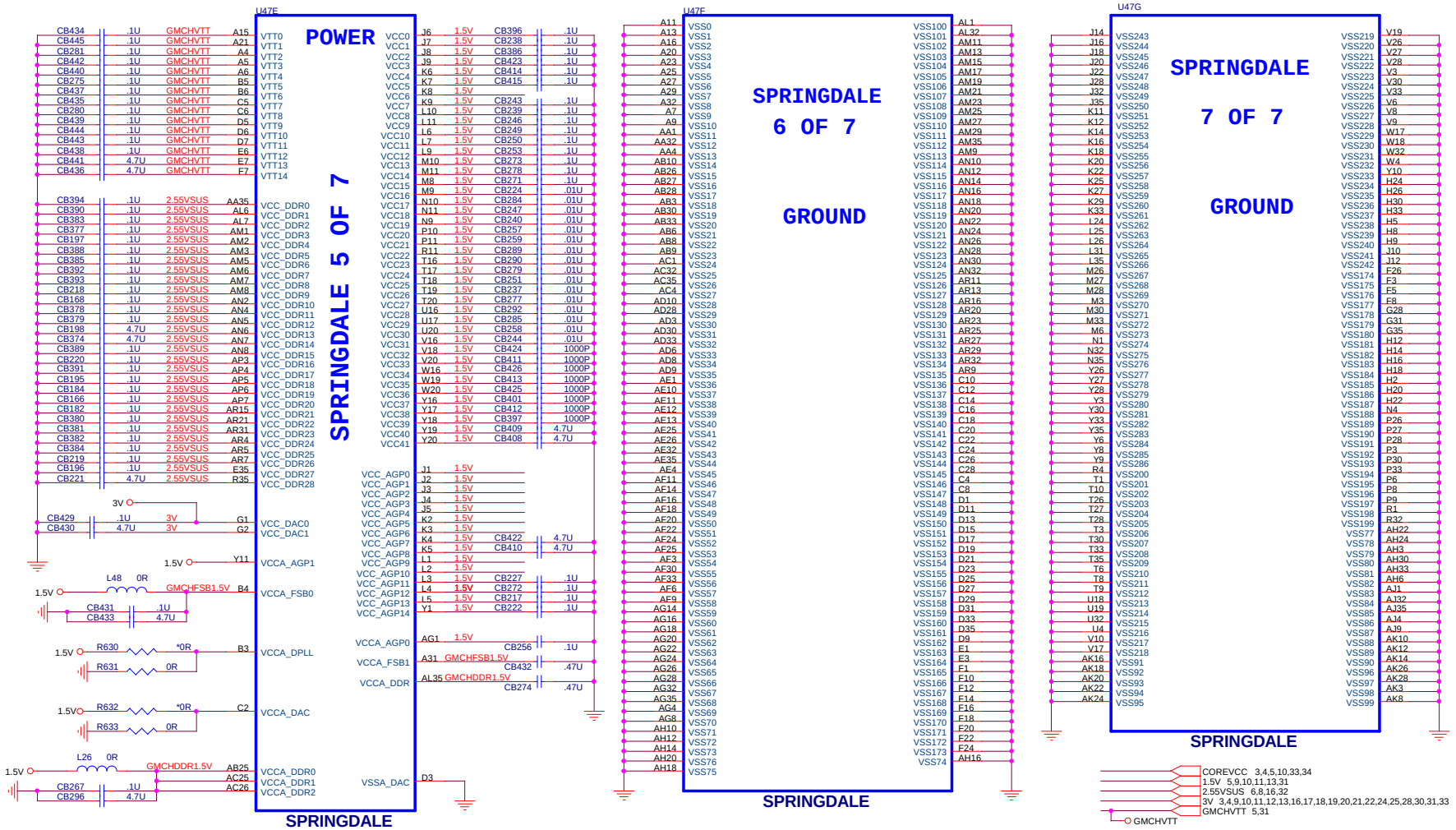
PLACE RESISTORS WITHIN 1 INCH OF DIMMS

MEMVREFB — C262 .01U; C263 2.2UB

PROJECT : NT1

Quanta Computer Inc.

Size	Document Number	Rev
Custom	GMCH DDR CHANNEL A	1A
Date: Monday, April 21, 2003	Sheet 5 of 33	

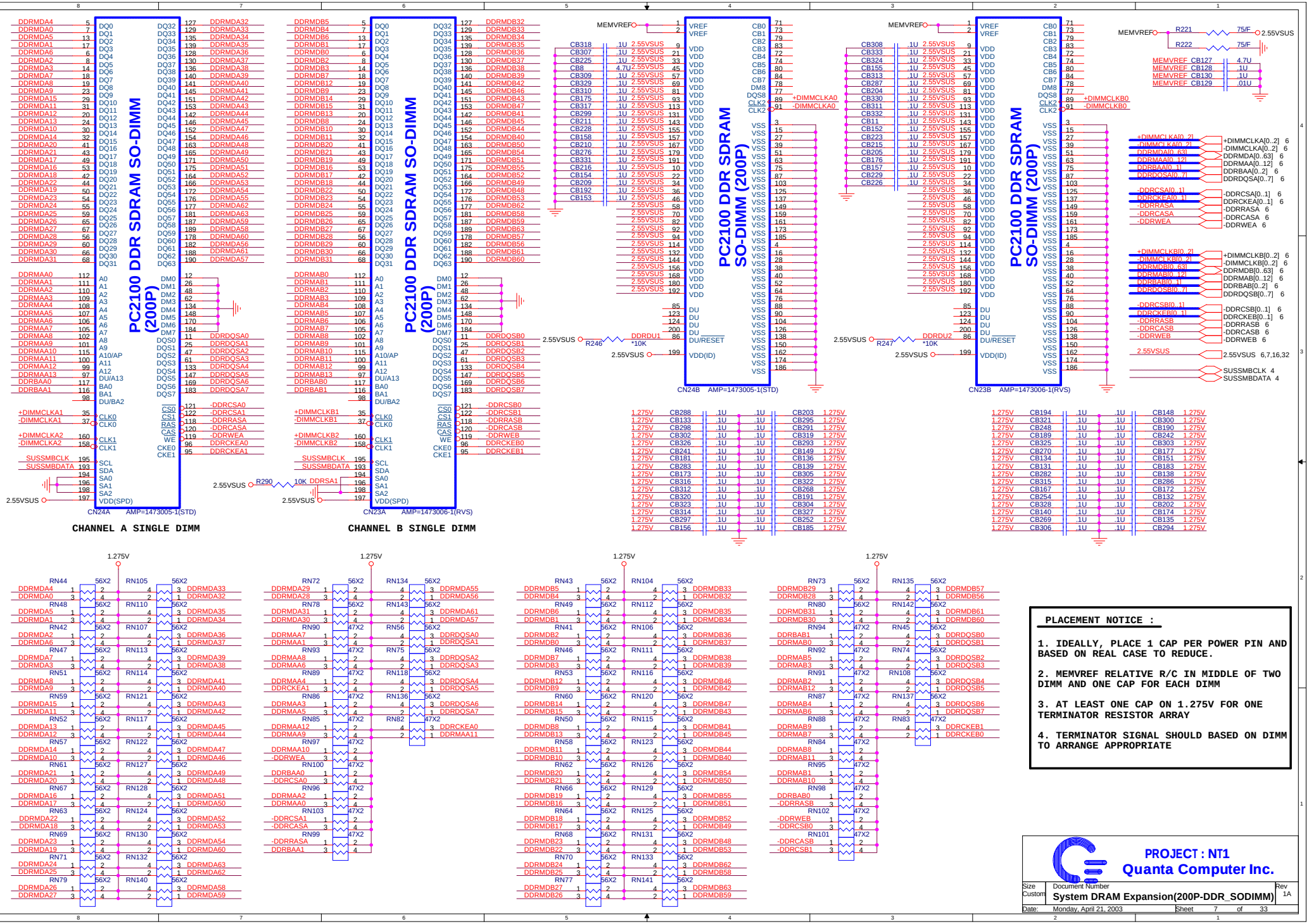


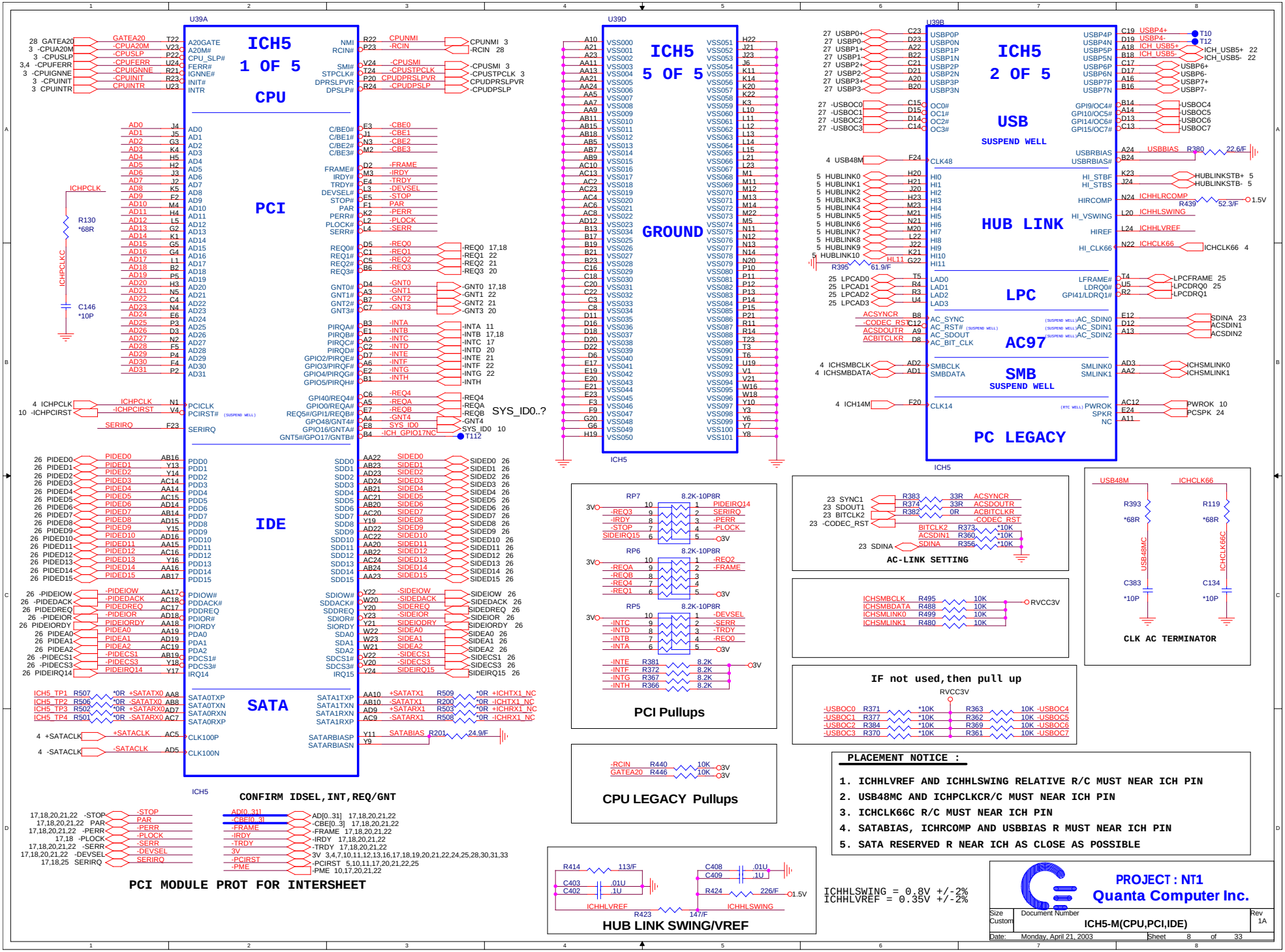
PLACEMENT NOTICE :

1. IDEALLY, PLACE 1 CAP PER POWER PIN AND BASED ON REAL CASE TO REDUCE.
2. GMCHFSB1.5V RELATIVE R/C MUST NEAR GMCH PIN
3. GMCHDACPLL1.5V RELATIVE R/C MUST NEAR GMCH PIN
4. GMCHDAC1.5V RELATIVE R/C MUST NEAR GMCH PIN
5. GMCHDDR1.5V RELATIVE R/C MUST NEAR GMCH PIN

PROJECT : NT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	GMCH(DDRA & B)	1A
Date: Monday, April 21, 2003	Sheet 6 of 33	


PC2100 DDR SDRAM SO-DIMM (200P)
CN24A AMP=1473005-1(STD)
CHANNEL A SINGLE DIMM
PC2100 DDR SDRAM SO-DIMM (200P)
CN23A AMP=1473006-1(RVS)
CHANNEL B SINGLE DIMM
PC2100 DDR SDRAM SO-DIMM (200P)
CN24B AMP=1473005-1(STD)
PC2100 DDR SDRAM SO-DIMM (200P)
CN23B AMP=1473006-1(RVS)
PLACEMENT NOTICE :
1. IDEALLY, PLACE 1 CAP PER POWER PIN AND BASED ON REAL CASE TO REDUCE.
2. MEMVREF RELATIVE R/C IN MIDDLE OF TWO DIMM AND ONE CAP FOR EACH DIMM
3. AT LEAST ONE CAP ON 1.275V FOR ONE TERMINATOR RESISTOR ARRAY
4. TERMINATOR SIGNAL SHOULD BASED ON DIMM TO ARRANGE APPROPRIATE
PROJECT : NT1
Quanta Computer Inc.
System DRAM Expansion(200P-DDR_SODIMM)
Size: Custom
Rev: 1A
Date: Monday, April 21, 2003
Sheet 7 of 33


U39A
ICH5
1 OF 5
CPU
PCI
IDE
SATA
U39D
ICH5
5 OF 5
VSS000
VSS001
VSS002
VSS003
VSS004
VSS005
VSS006
VSS007
VSS008
VSS009
VSS010
VSS011
VSS012
VSS013
VSS014
VSS015
VSS016
VSS017
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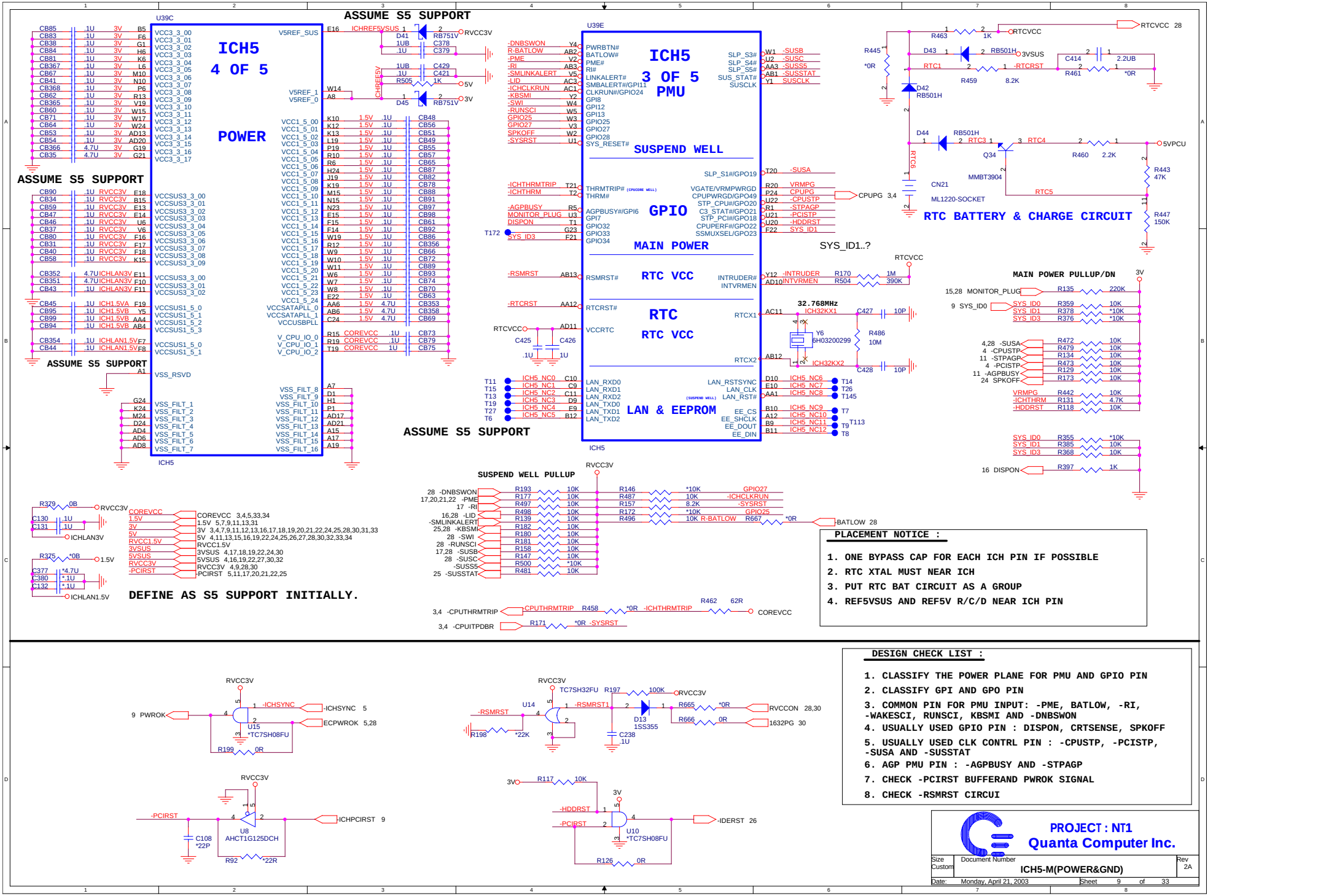
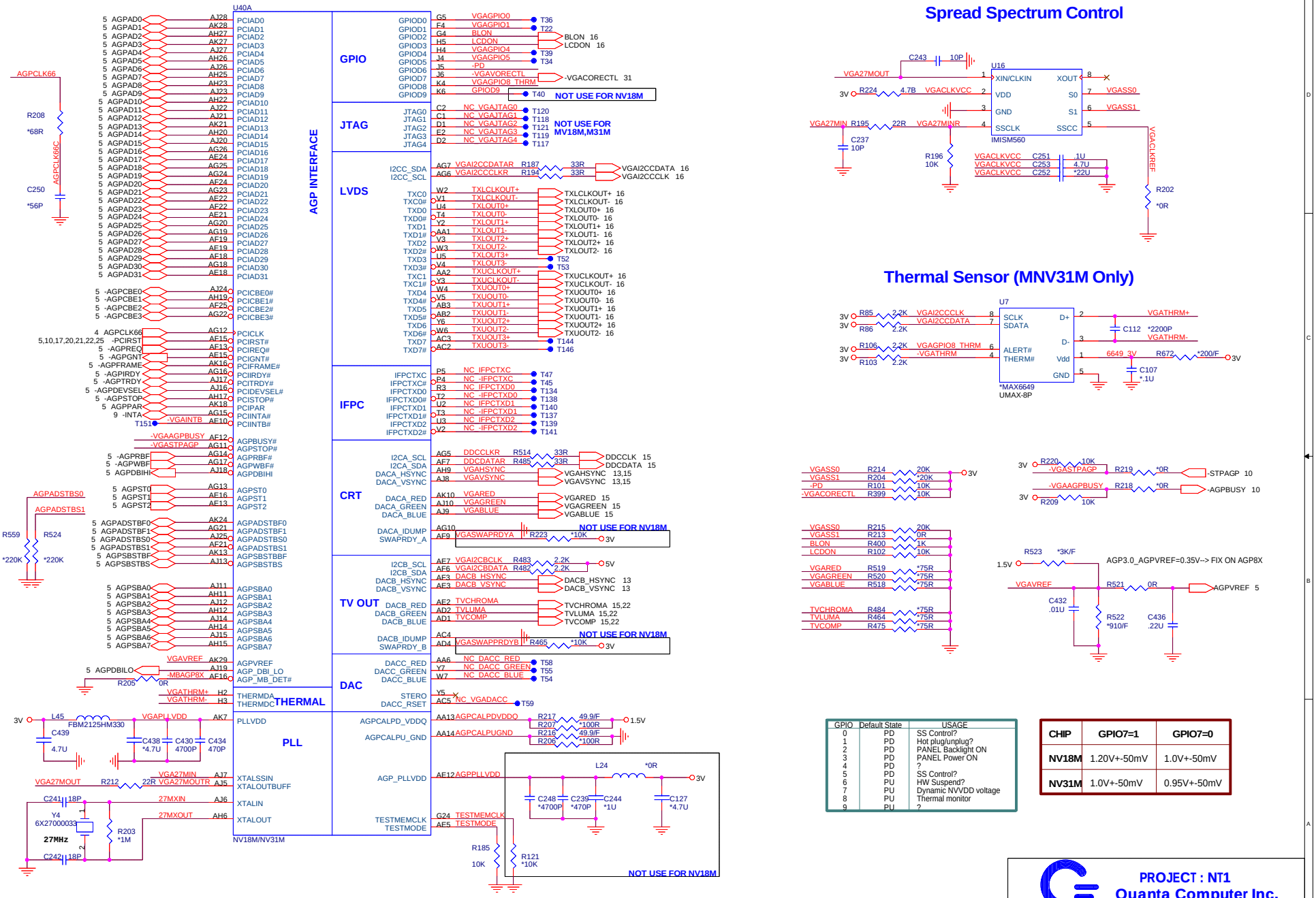
VSS039
VSS040
VSS041
VSS042
VSS043
VSS044
VSS045
VSS046
VSS047
VSS048
VSS049
VSS050
GROUND
VSS051
VSS052
VSS053
VSS054
VSS055
VSS056
VSS057
VSS058
VSS059
VSS060
VSS061
VSS062
VSS063
VSS064
VSS065
VSS066
VSS067
VSS068
VSS069
VSS070
VSS071
VSS072
VSS073
VSS074
VSS075
VSS076
VSS077
VSS078
VSS079
VSS080
VSS081
VSS082
VSS083
VSS084
VSS085
VSS086
VSS087
VSS088
VSS089
VSS090
VSS091
VSS092
VSS093
VSS094
VSS095
VSS096
VSS097
VSS098
VSS099
VSS100
VSS101
U39B
ICH5
2 OF 5
USB
SUSPEND WELL
HUB LINK
LPC
AC97
SMB
SUSPEND WELL
PC LEGACY
ICH5
CONFIRM IDSEL,INT,REQ/GNT
PCI MODULE PROT FOR INTERSHEET
PCI Pullups
CPU LEGACY Pullups
AC-LINK SETTING
IF not used,then pull up
RVCC3V
CLK AC TERMINATOR
HUB LINK SWING/VREF
PLACEMENT NOTICE :
1. ICHHLVREF AND ICHHLSWING RELATIVE R/C MUST NEAR ICH PIN
2. USB48MC AND ICHPCLKCR/C MUST NEAR ICH PIN
3. ICHCLK66C R/C MUST NEAR ICH PIN
4. SATABIAS, ICHRCOMP AND USBBIAS R MUST NEAR ICH AS CLOSE AS POSSIBLE
5. SATA RESERVED R NEAR ICH AS CLOSE AS POSSIBLE
ICHHLSWING = 0.8V +/-2%
ICHHLVREF = 0.35V +/-2%
PROJECT : NT1
Quanta Computer Inc.
ICH5-M(CPU,PCI,IDE)
Monday, April 21, 2003


ASSUME S5 SUPPORT
ICH5
4 OF 5
POWER
ASSUME S5 SUPPORT
ASSUME S5 SUPPORT
ASSUME S5 SUPPORT
ICH5
3 OF 5
PMU
SUSPEND WELL
GPIO
MAIN POWER
RTC VCC
RTC
RTC VCC
LAN & EEPROM
ICH5
SYS_ID1..?
RTC BATTERY & CHARGE CIRCUIT
MAIN POWER PULLUP/DN
SUSPEND WELL PULLUP
DEFINE AS S5 SUPPORT INITIALLY.
PLACEMENT NOTICE :
1. ONE BYPASS CAP FOR EACH ICH PIN IF POSSIBLE
2. RTC XTAL MUST NEAR ICH
3. PUT RTC BAT CIRCUIT AS A GROUP
4. REF5VSUS AND REF5V R/C/D NEAR ICH PIN
DESIGN CHECK LIST :
1. CLASSIFY THE POWER PLANE FOR PMU AND GPIO PIN
2. CLASSIFY GPI AND GPO PIN
3. COMMON PIN FOR PMU INPUT: -PME, BATLOW, -RI, -WAKESCI, RUNSCI, KBSMI AND -DNBSWON
4. USUALLY USED GPIO PIN : DISPON, CRTSENSE, SPKOFF
5. USUALLY USED CLK CONTRL PIN : -CPUSTP, -PCISTP, -SUSA AND -SUSSTAT
6. AGP PMU PIN : -AGPBUSY AND -STPAGP
7. CHECK -PCIRST BUFFERAND PWROK SIGNAL
8. CHECK -RSMRST CIRCUI
PROJECT : NT1
Quanta Computer Inc.
Size Custom
Document Number ICH5-M(POWER&GND)
Rev 2A
Date: Monday, April 21, 2003
Sheet 9 of 33



GPIO	Default State	USAGE
0	PD	SS Control?
1	PD	Hot plug/unplug?
2	PD	PANEL Backlight ON
3	PD	PANEL Power ON
4	PD	?
5	PD	SS Control?
6	PU	HW Suspend?
7	PU	Dynamic NVVDD voltage
8	PU	Thermal monitor
9	PU	?

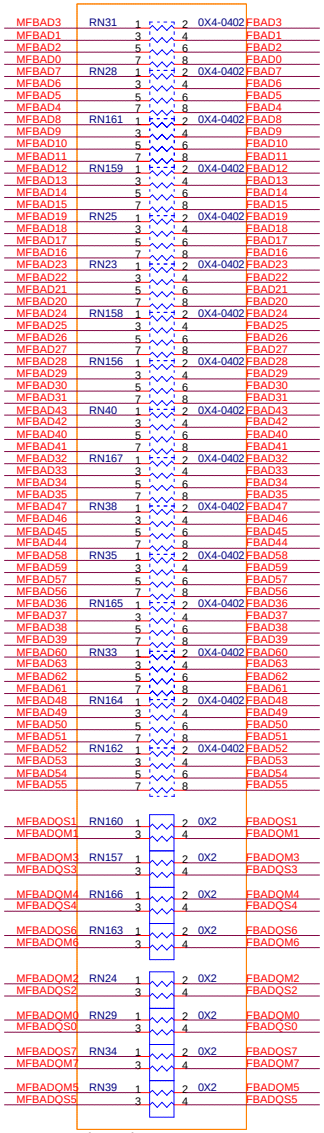
CHIP	GPIO7=1	GPIO7=0
NV18M	1.20V+-50mV	1.0V+-50mV
NV31M	1.0V+-50mV	0.95V+-50mV

PROJECT : NT1
Quanta Computer Inc.

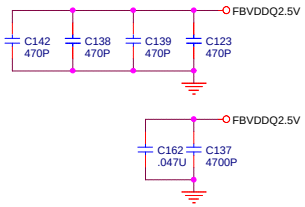
Size	Document Number	Rev
Custom	NV18M/NV31M HOST/VIDEO	2A
Date: Monday, April 21, 2003	Sheet 10 of 33	

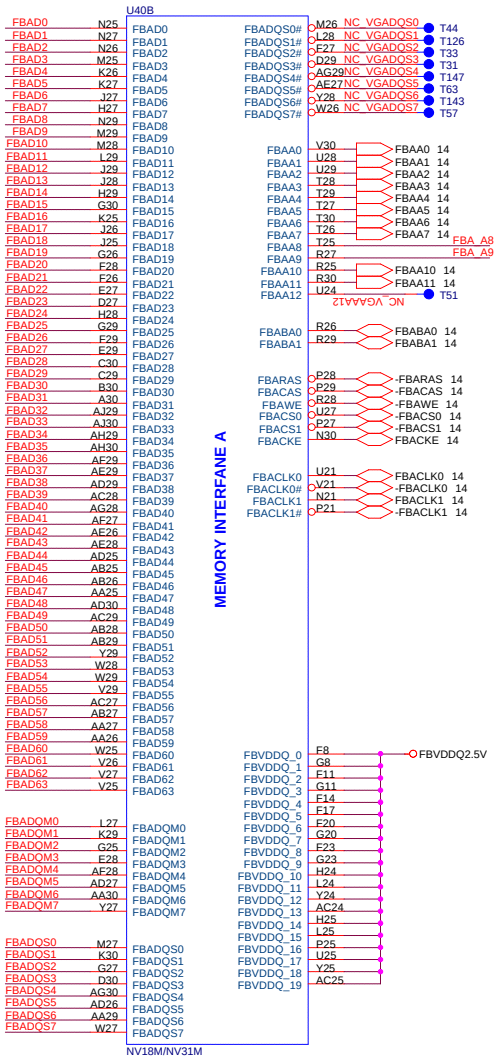
15X4 For NV31M(over 300MHz)

15X4 For NV31M(over 300MHz)

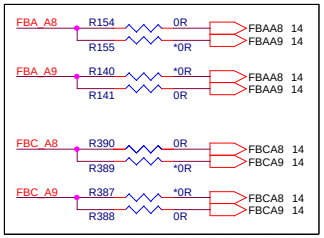


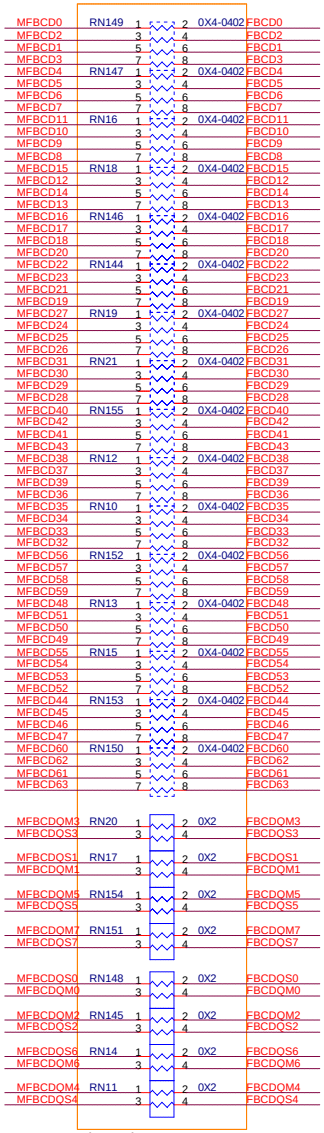
Place close to memory



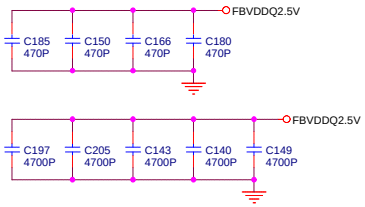


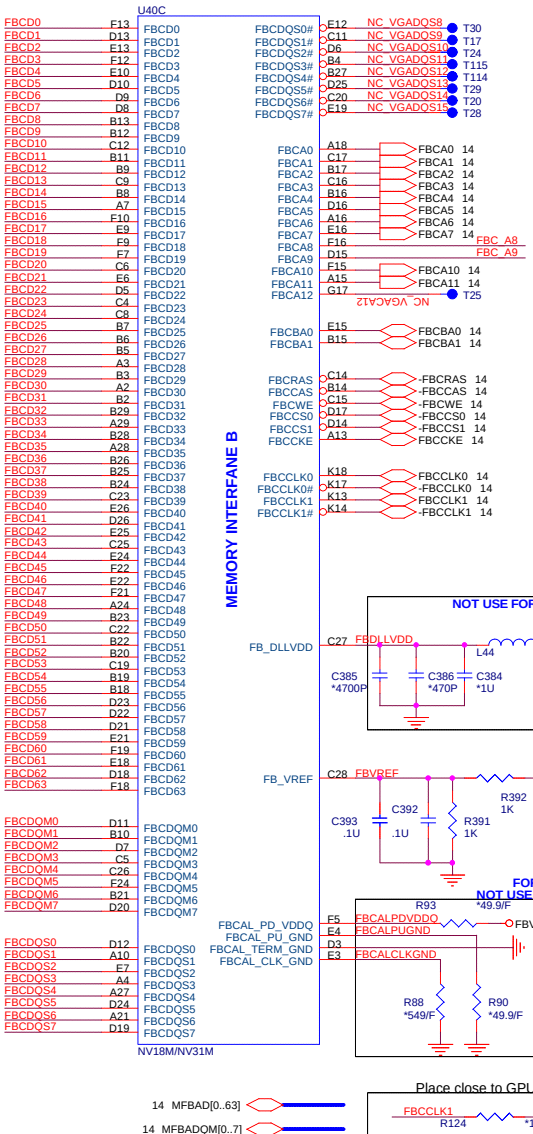
SWAP FOR 8X32M TYPE / NV18M Only

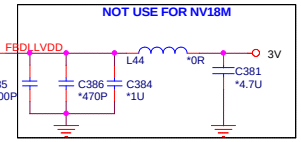


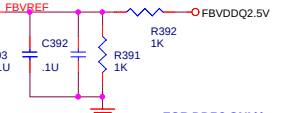


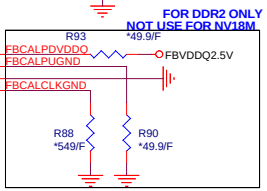
Place close to memory



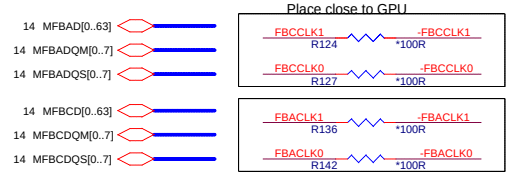






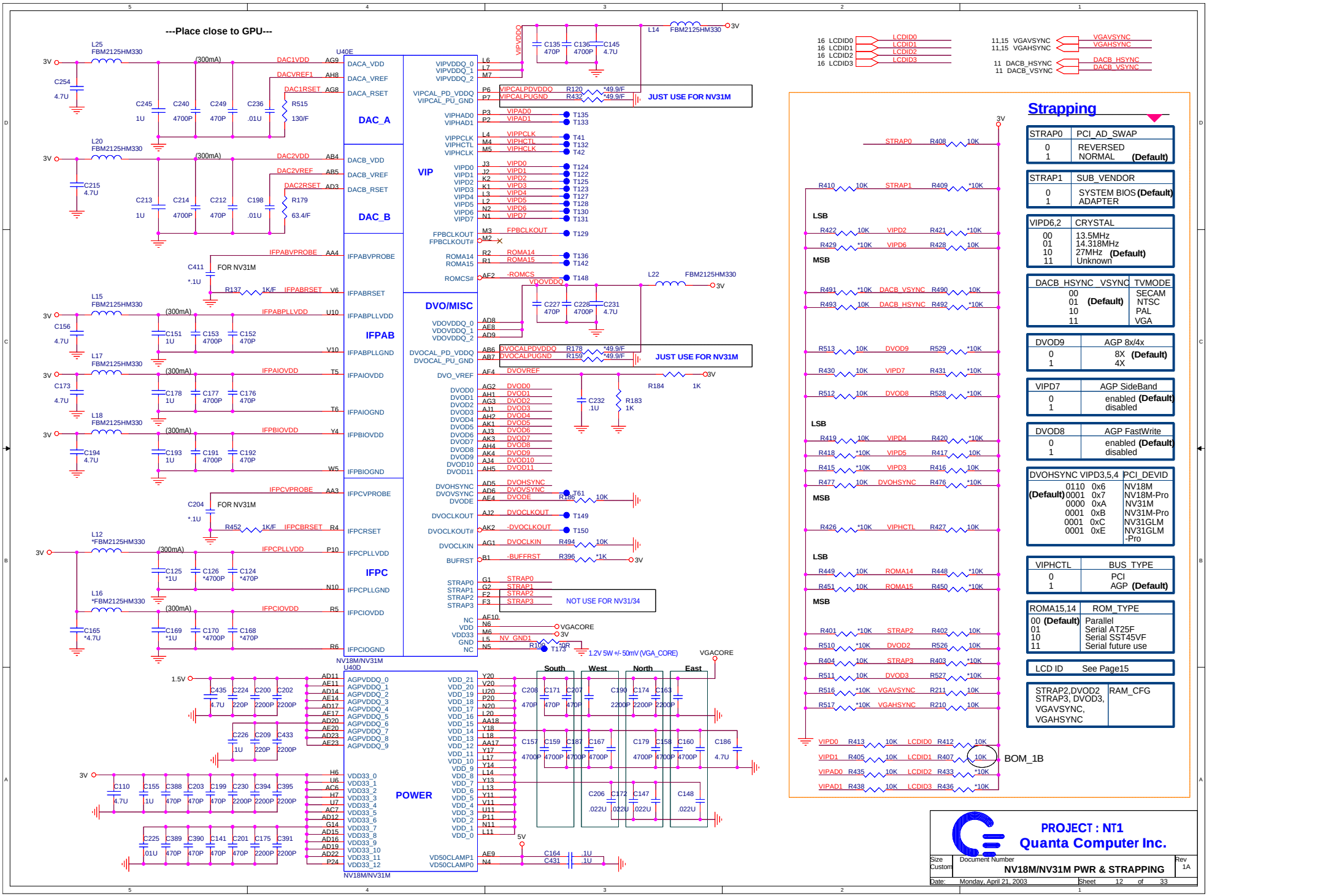


Place close to GPU

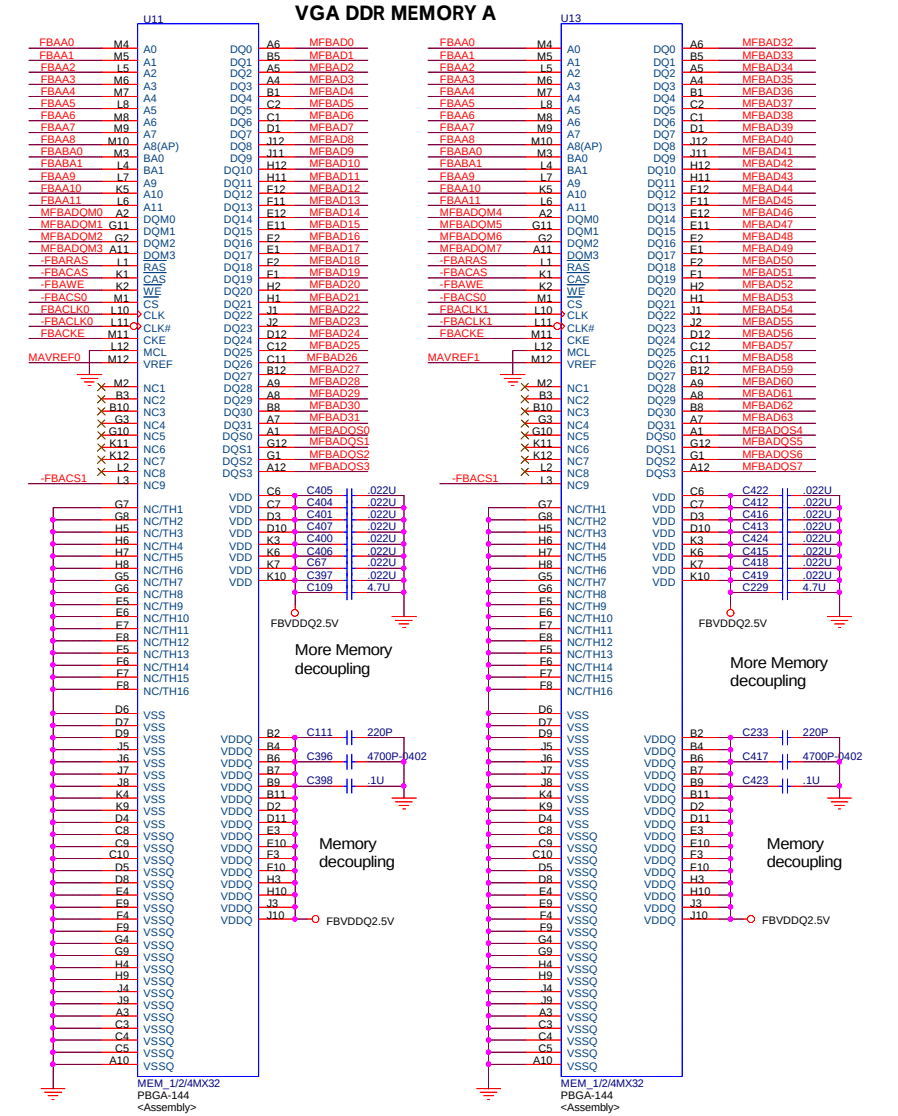


PROJECT : NT1
Quanta Computer Inc.

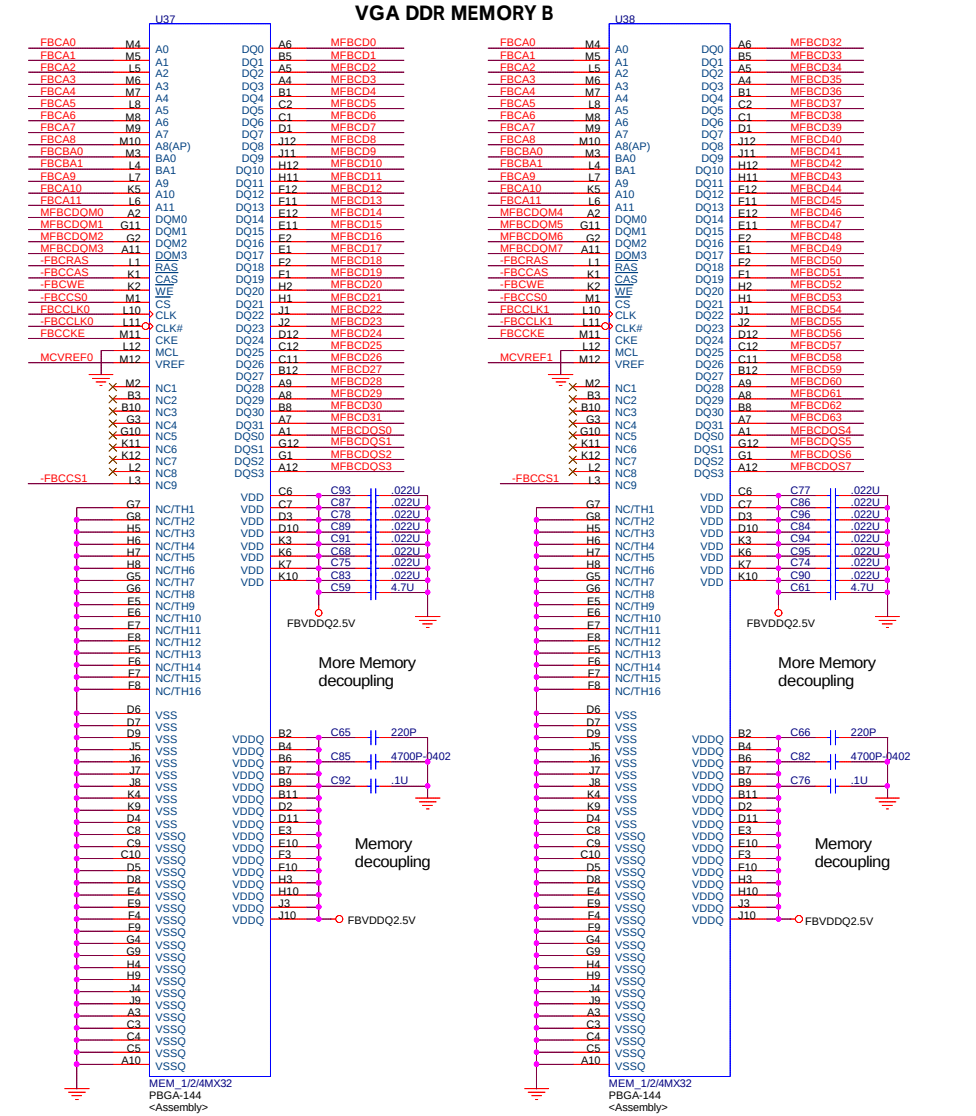
Size	Document Number	Rev
Custom	NV18M/NV31M MEMORY	1A
Date: Monday, April 21, 2003	Sheet 11 of 33	


---Place close to GPU---
U40E
NV18M/NV31M
U40D
DAC_A
DAC_B
IFPAB
IFPC
VIP
DVO/MISC
POWER
JUST USE FOR NV31M
NOT USE FOR NV31/34
Strapping
STRAP0 PCI_AD_SWAP
0 REVERSED
1 NORMAL (Default)
STRAP1 SUB_VENDOR
0 SYSTEM BIOS (Default)
1 ADAPTER
VIPD6,2 CRYSTAL
00 13.5MHz
01 14.318MHz
10 27MHz (Default)
11 Unknown
DACB_HSYNC VSYNC TVMODE
00 SECAM
01 (Default) NTSC
10 PAL
11 VGA
DVOD9 AGP 8x/4x
0 8X (Default)
1 4X
VIPD7 AGP SideBand
0 enabled (Default)
1 disabled
DVOD8 AGP FastWrite
0 enabled (Default)
1 disabled
DVOHSYNC VIPD3,5,4 PCI_DEVID
(Default) 0110 0x6 NV18M
0001 0x7 NV18M-Pro
0000 0xA NV31M
0001 0xB NV31M-Pro
0001 0xC NV31GLM
0001 0xE NV31GLM-Pro
VIPHCTL BUS_TYPE
0 PCI
1 AGP (Default)
ROMA15,14 ROM_TYPE
00 (Default) Parallel
01 Serial AT25F
10 Serial SST45VF
11 Serial future use
LCD ID See Page15
STRAP2,DVOD2 STRAP3, DVOD3, VGAVSYNC, VGAHSYNC RAM_CFG
BOM_1B
PROJECT : NT1
Quanta Computer Inc.
Size Custom
Document Number NV18M/NV31M PWR & STRAPPING
Rev 1A
Date: Monday, April 21, 2003
Sheet 12 of 33

VGA DDR MEMORY A

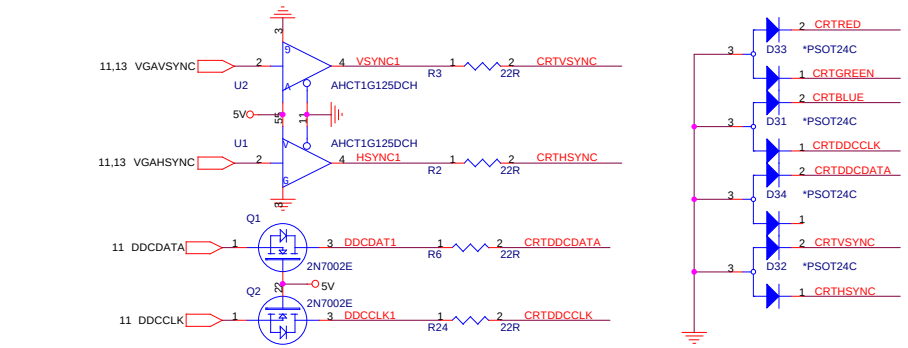


VGA DDR MEMORY B

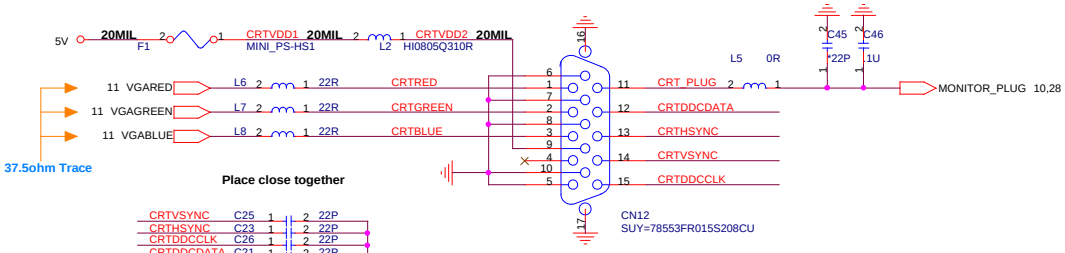


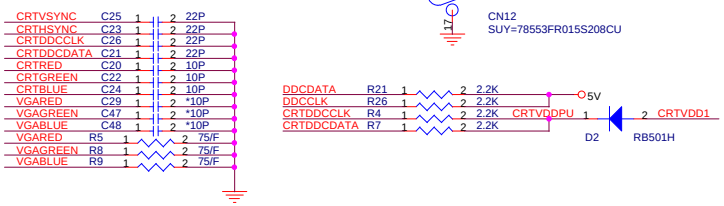
PROJECT : NT1
Quanta Computer Inc.

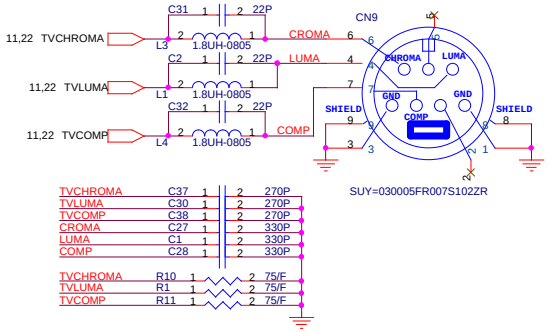
Size	Document Number	Rev
Custom	NV18M/NV31M MEMORY A/B	1A
Date: Monday, April 21, 2003	Sheet 13 of 33	



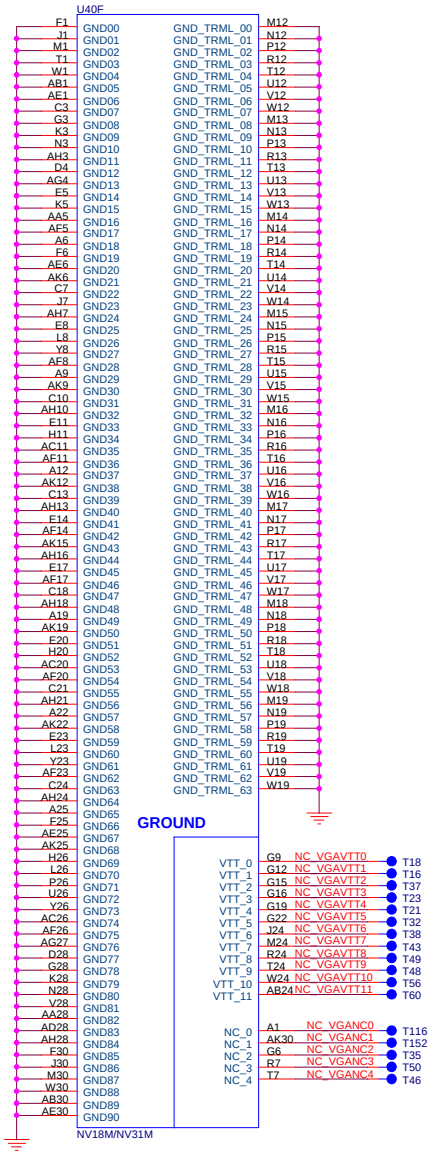
CRT PORT







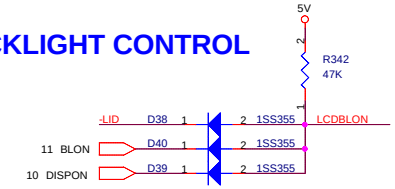
NV18M/NV31M GND

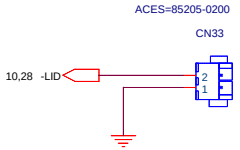


PROJECT : NT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT & TV-OUT , VGA GND	1A
Date: Monday, April 21, 2003	Sheet 14 of 33	

BACKLIGHT CONTROL



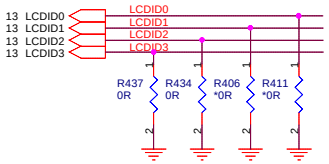


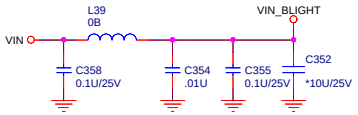
-LID : from hardware control
BLON : from VGA CHIP control
DISP_ON : from ICH5 control

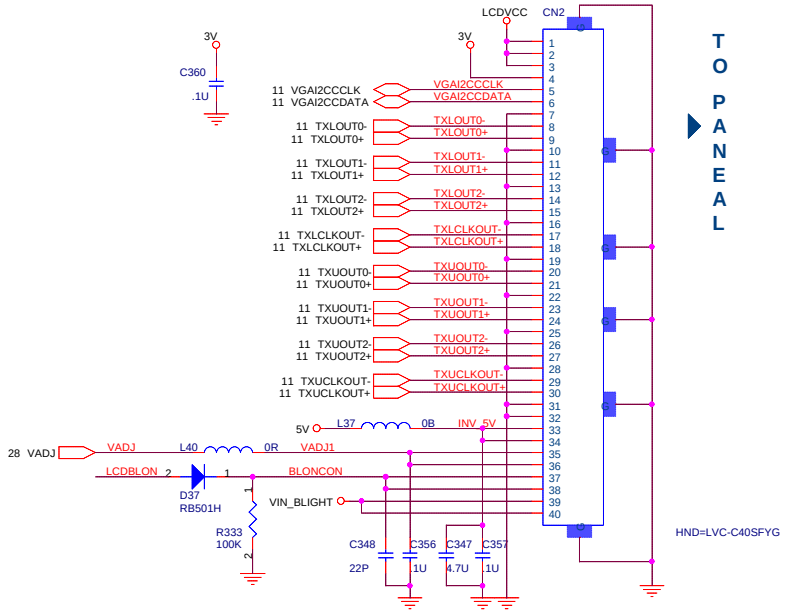
LCDBLON = 1 : LCD BACKLIGHT ON
LCDBLON = 0 : LCD BACKLIGHT OFF

PANEL ID:

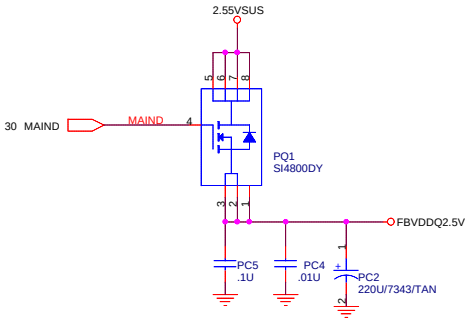
		PANEL_ID3	PANEL_ID2	PANEL_ID1	PANEL_ID0
ID3	17" WXGA	0	0	0	1

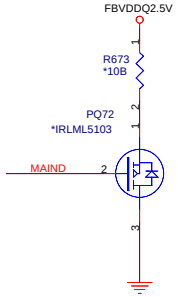




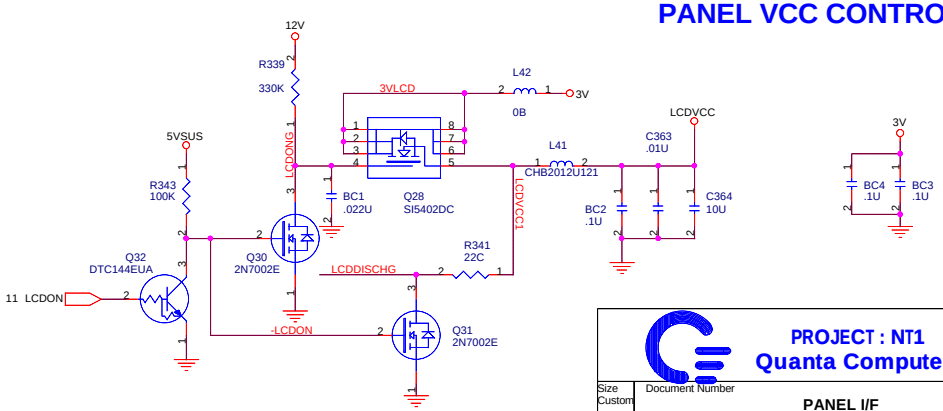


VGA DDR POWER





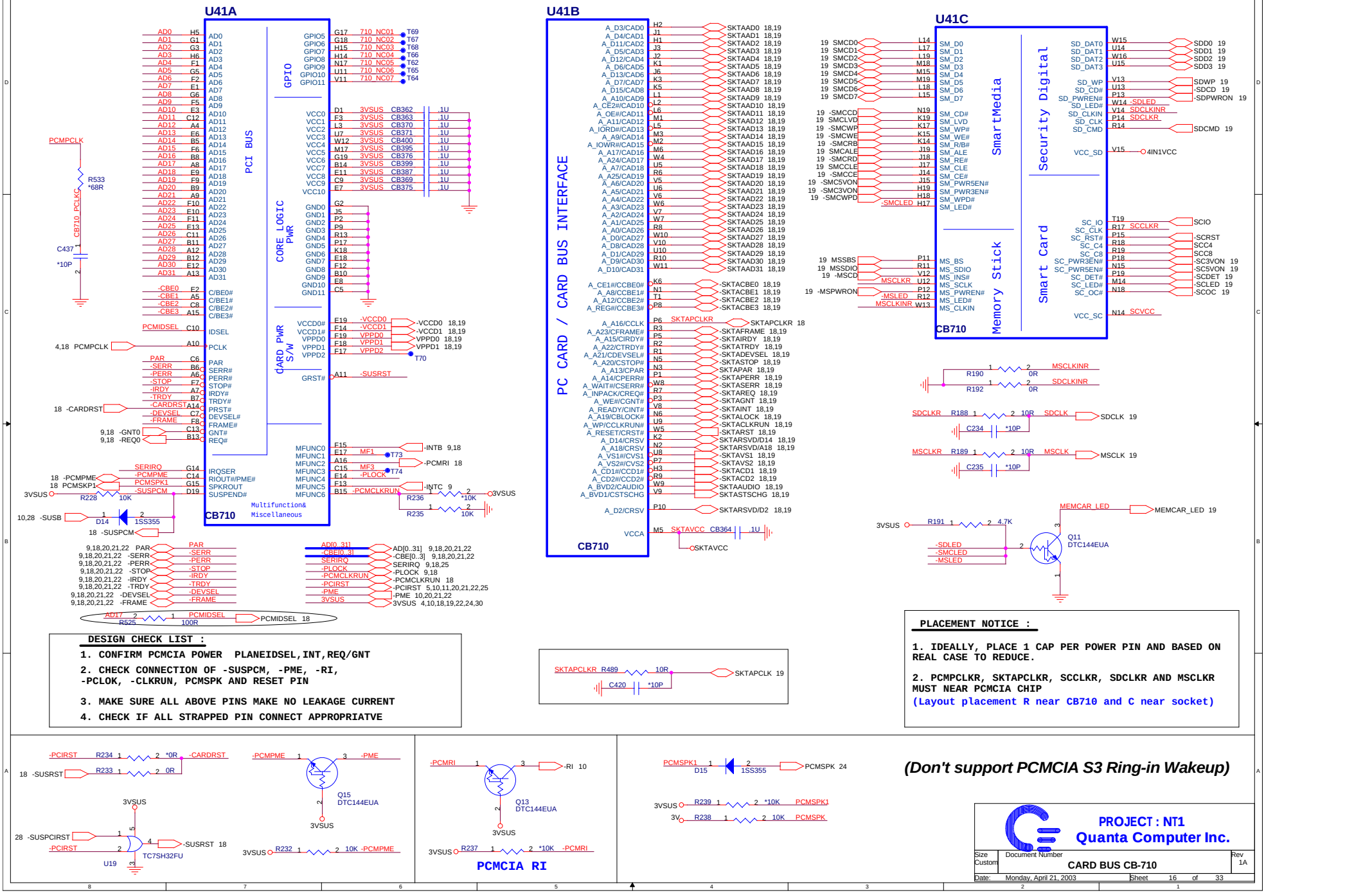
PANEL VCC CONTROL



PROJECT : NT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PANEL I/F	2A
Date: Monday, April 21, 2003	Sheet 15 of 33	

CARDBUS CONTROLLER - CB710(PCI I/F , CB I/F , Memorystick I/F)



DESIGN CHECK LIST :

1. CONFIRM PCMCIA POWER PLANEIDSEL,INT,REQ/GNT
2. CHECK CONNECTION OF -SUSPCM, -PME, -RI, -PCLOK, -CLKRUN, PCMSPK AND RESET PIN
3. MAKE SURE ALL ABOVE PINS MAKE NO LEAKAGE CURRENT
4. CHECK IF ALL STRAPPED PIN CONNECT APPROPRIATVE

PLACEMENT NOTICE :

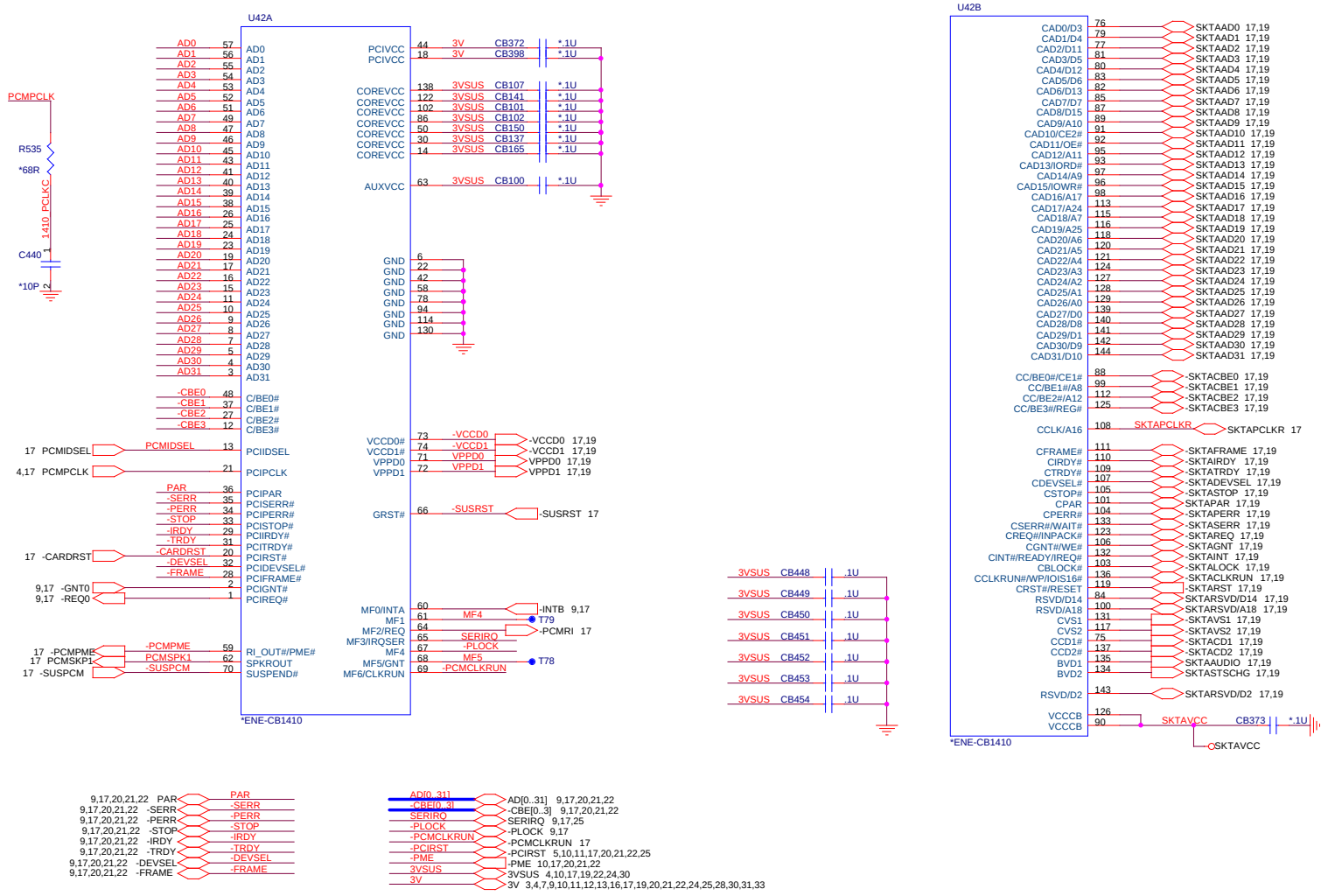
1. IDEALLY, PLACE 1 CAP PER POWER PIN AND BASED ON REAL CASE TO REDUCE.
2. PCMPCLKR, SKTAPCLKR, SCCLKR, SDCLKR AND MSCLKR MUST NEAR PCMCIA CHIP
(Layout placement R near CB710 and C near socket)

(Don't support PCMCIA S3 Ring-in Wakeup)

PROJECT : NT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CARD BUS CB-710	1A
Date: Monday, April 21, 2003	Sheet 16 of 33	

CARDBUS CONTROLLER - CB1410



DESIGN CHECK LIST :

1. CONFIRM PCMCIA POWER PLANEIDSEL,INT,REQ/GNT
2. CHECK CONNECTION OF -SUSPCM, -PME, -RI, -PCLOK, -CLKRUN, PCMSPK AND RESET PIN
3. MAKE SURE ALL ABOVE PINS MAKE NO LEAKAGE CURRENT
4. CHECK IF ALL STRAPPED PIN CONNECT APPROPRIATVE

PLACEMENT NOTICE :

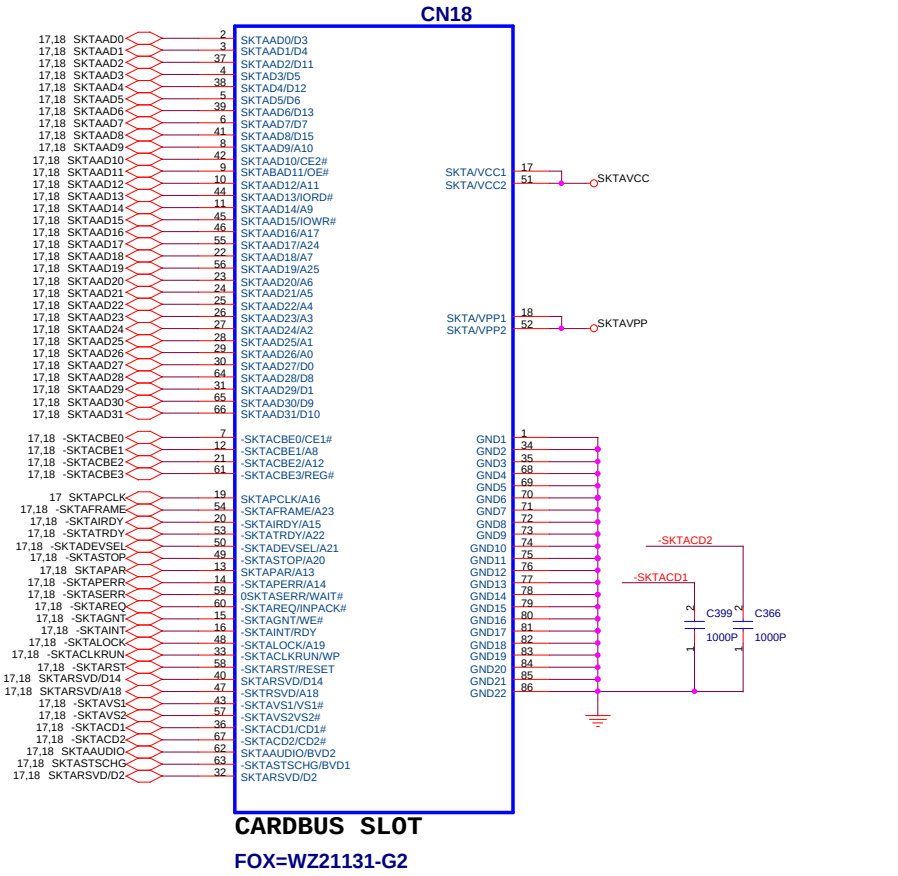
1. IDEALLY, PLACE 1 CAP PER POWER PIN AND BASED ON REAL CASE TO REDUCE.
2. PCMPCLKR, SKTAPCLKR, SCCLKR, SDCLKR AND MSCLKR MUST NEAR PCMCIA CHIP

(Layout placement R near TI1410 and C near socket)
(when placing the series damping resistor , it is recommended to keep the stub less than 1 cm in length)

PROJECT : NT1
Quanta Computer Inc.

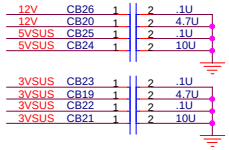
Size	Document Number	Rev
Custom	CARD BUS ENE1410	1A
Date: Monday, April 21, 2003	Sheet 17 of 33	

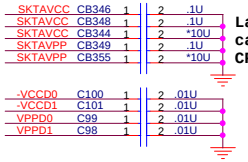
4-IN-1 MEDIA BAY



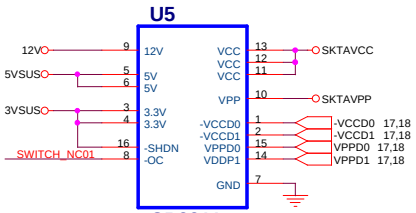
CARDBUS SLOT

FOX=WZ21131-G2

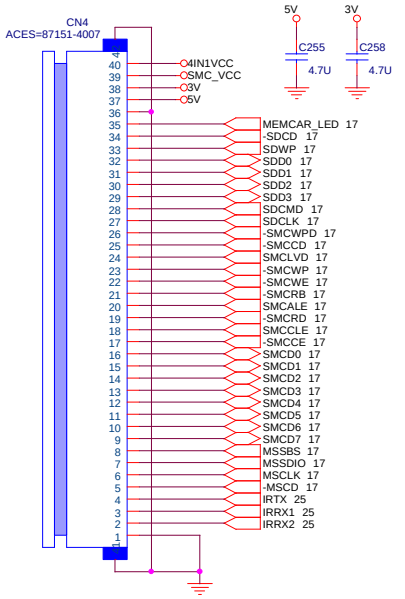


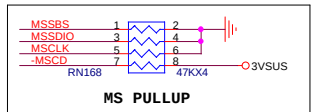


Layout placement capacities near CP2211

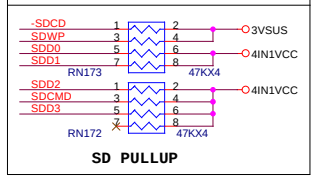


CP2211

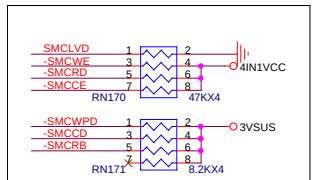




MS PULLUP

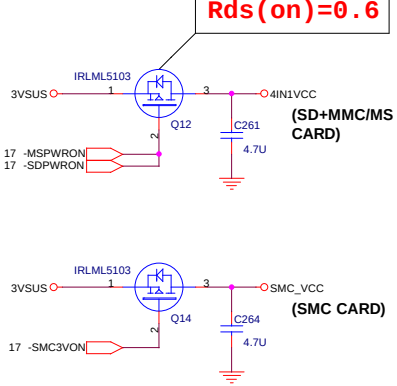


SD PULLUP

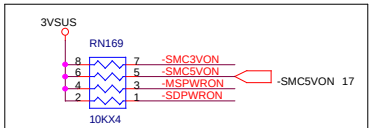


pll-hi to 3V with a 8.2K

SMC PULLUP

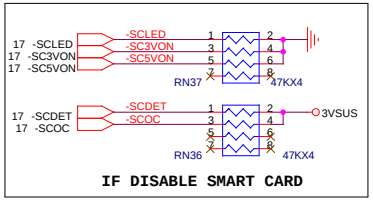


System can choice just support 3.3V SM card only.or use CP2211 to switch 3.3V & 5V



pll-hi to 3V with a 8.2K

4IN1 POWER CONTROL



IF DISABLE SMART CARD

IRLML5103
Rds(on)=0.6

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	CARD BUS SLOT	2A
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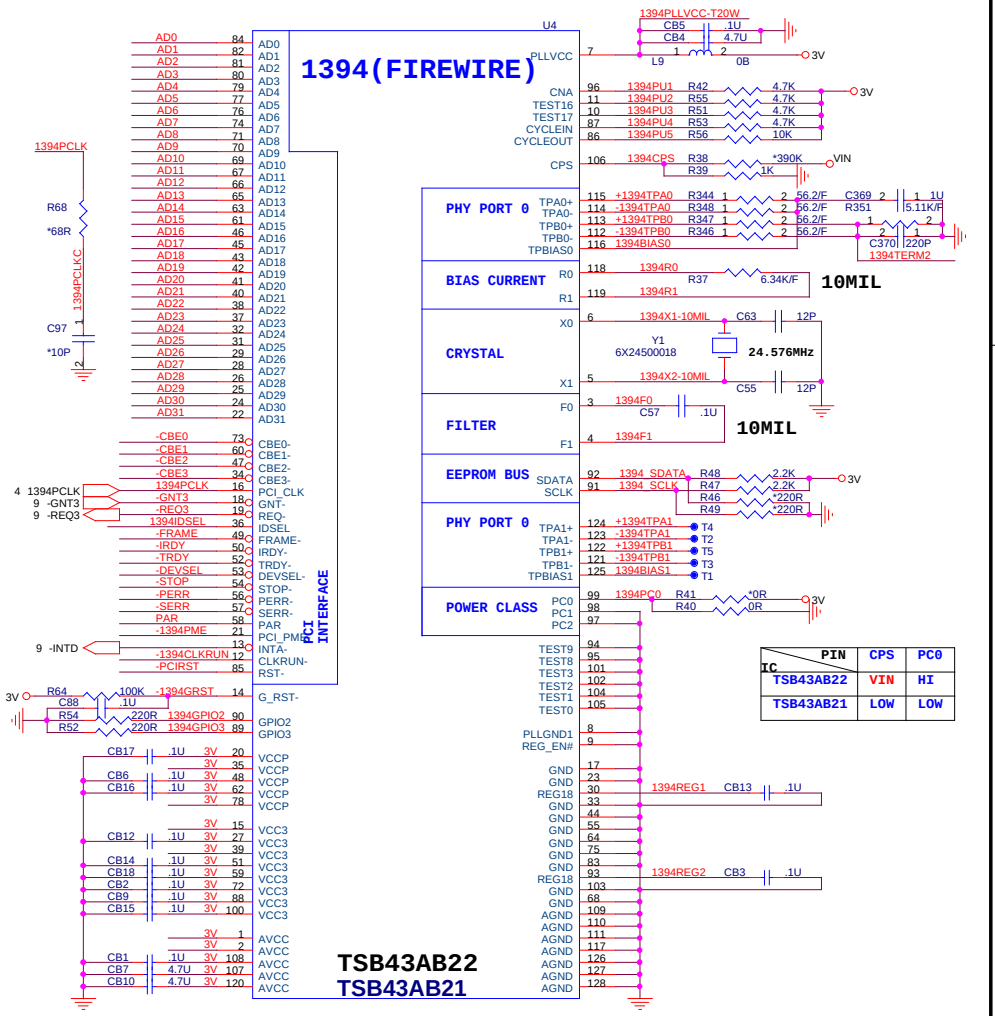
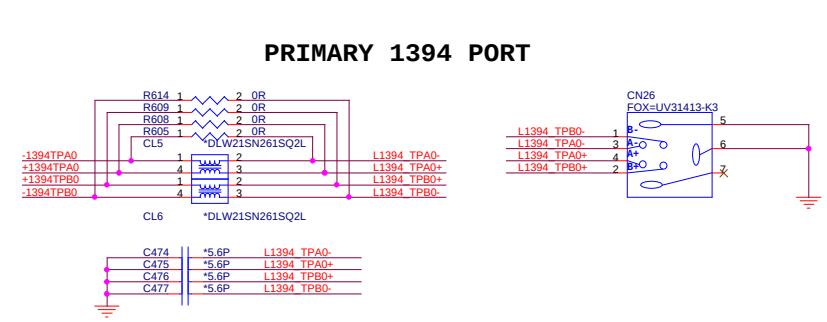


IC \ PIN	CPS	PC0
TSB43AB22	VIN	HI
TSB43AB21	LOW	LOW

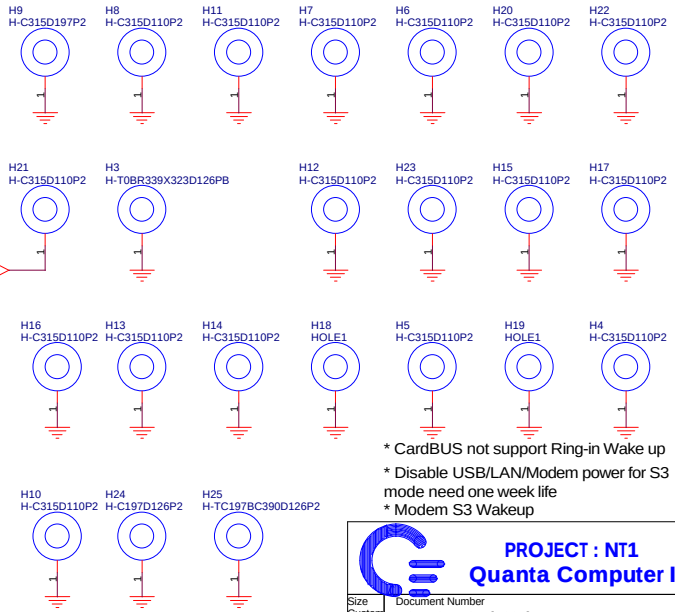


DESIGN CHECK LIST :

1. CONFIRM 1394 POWER PLANE, IDSEL,INT,REQ/GNT
2. CHECK CONNECTION OF -SUSPCM, -PME, -RI, -PCLOK, -CLKRUN, PCMSPK AND RESET PIN
3. MAKE SURE ALL ABOVE PINS MAKE NO LEAKAGE CURRENT
4. CHECK IF ALL STRAPPED PIN CONNECT APPROPRIATVE

PLACEMENT NOTICE :

1. IDEALLY, PLACE 1 CAP PER POWER PIN AND BASED ON REAL CASE TO REDUCE.
2. PCMPCLKC RELATIVE R/C MUST NEAR 1394 CHIP
3. 1394PLVCC-T20W MUST NEAR 1394 CHIP
4. ALL 1394 TERMINATOR R/C MUST NEAR 1394 CHIP
5. 1394R0 AND 1394 R1 MUST NEAR 1394 CHIP
6. XTAL AND CAP MUST NEAR 1394 CHIP
7. 1394REG1 AND 1394REQ2 CAP MUST NEAR 1394 CHIP
8. 1394F0 AND 1394F1 CAP MUST NEAR 1394 CHIP



* CardBUS not support Ring-in Wake up

* Disable USB/LAN/Modem power for S3 mode need one week life

* Modem S3 Wakeup

PROJECT : NT1

Quanta Computer Inc.

Size	Document Number	Rev
Custom	TSB43AB21 (1394)	1A
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less than 12cm

should be placed closely to the 10/100M magnetic

U9

RTL8101L

PLACEMENT CAREFULLY

CONFIRM IDSEL,INT,REQ/GNT

CHECK POWER PLANE FOR -PME

U35 H0013

CN3 ACES=88266-0200

CN10 AMP=C-1470620

PLACEMENT CAREFULLY

as close as possible

DESIGN CHECK LIST :

1. CONFIRM LAN POWER PLANE, IDSEL,INT,REQ/GNT
2. CHECK CONNECTION OF -SUSPCM, -PME, -RI, -PCLOK, -CLKRUN, PCMSPK AND RESET PIN
3. MAKE SURE ALL ABOVE PINS MAKE NO LEAKAGE CURRENT
4. CHECK IF ALL STRAPPED PIN CONNECT APPROPRIATVE

PLACEMENT NOTICE :

1. IDEALLY, PLACE 1 CAP PER POWER PIN AND BASED ON REAL CASE TO REDUCE.
2. LANPCLKC RELATIVE R/C MUST NEAR LAN CHIP
3. LAN2.5V REGULATOR MUST NEAR LAN CHIP
4. +/-LANPHYRX, +/-LANPHYTX RELATIVE R/C MUST NEAR ????
5. +/-LANRX, +/-LANRX RELATIVE R/C TERMINATOR MUST NEAR ????
6. LAN TRNAFORMAER RELATIVE TERMINATOR MUST NEAR ????
7. MODEM TIP AND RING SIGNAL MUST HAVE AT LEAST 2.54 ISOLATION
8. XTAL AND ITS CAP MUST NEAR LAN CHIP
9. LAN3V RELATIVE L/C MUST NEAR LAN CHIP

the crystal should be placed far away from I/O ports , important or high frequency signal traces(Tx , Rx , power)

(Don't support LAN S5 WOL)

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	LAN interface RTL8101	2A
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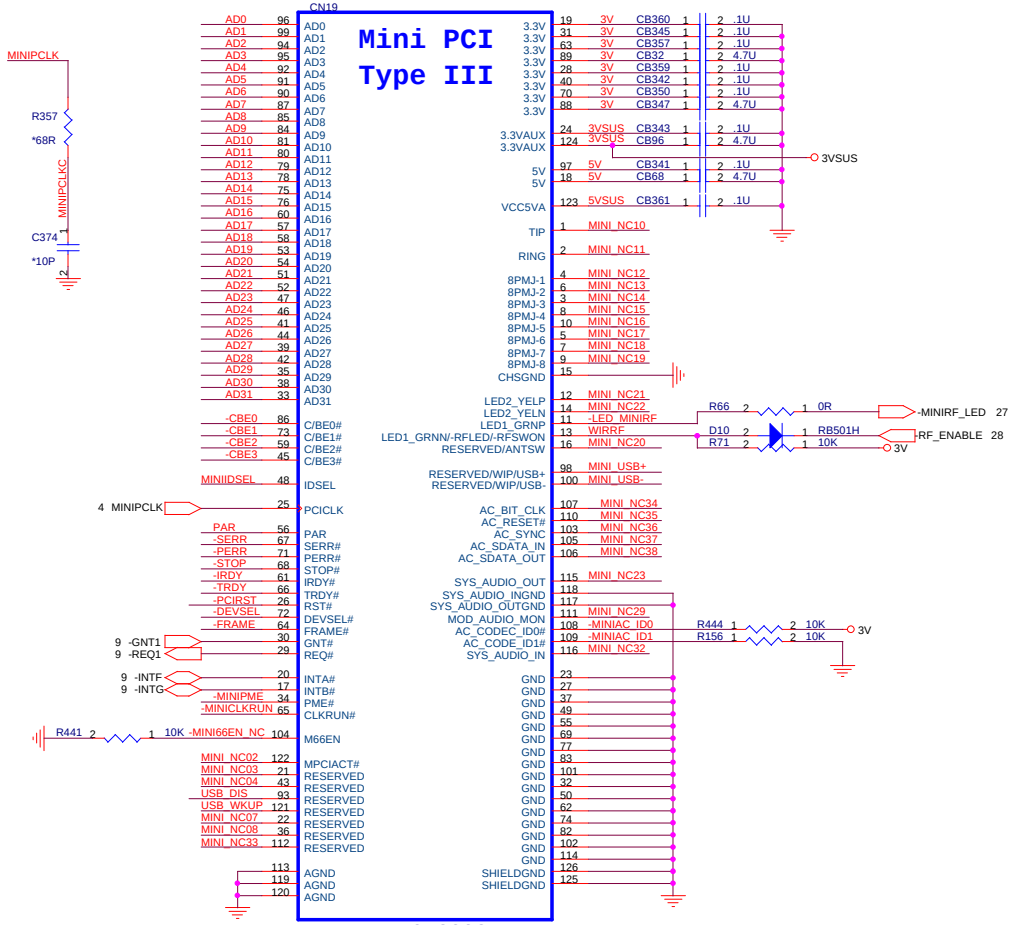
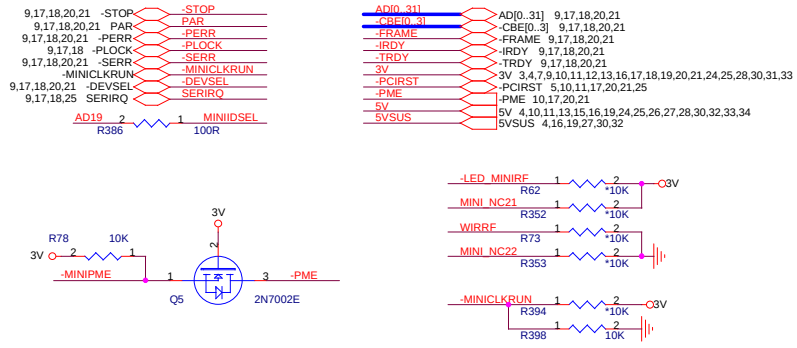
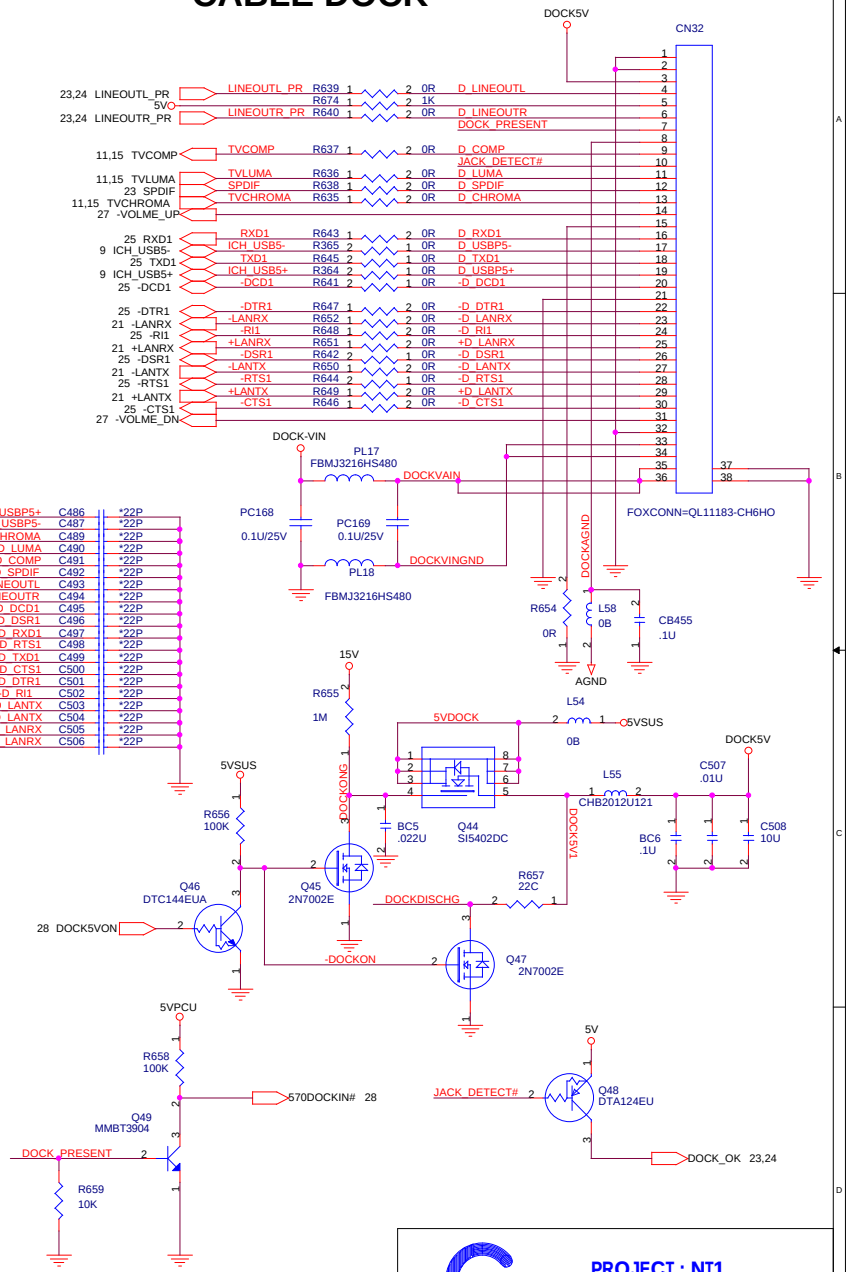
(Don't support AC-LINK)



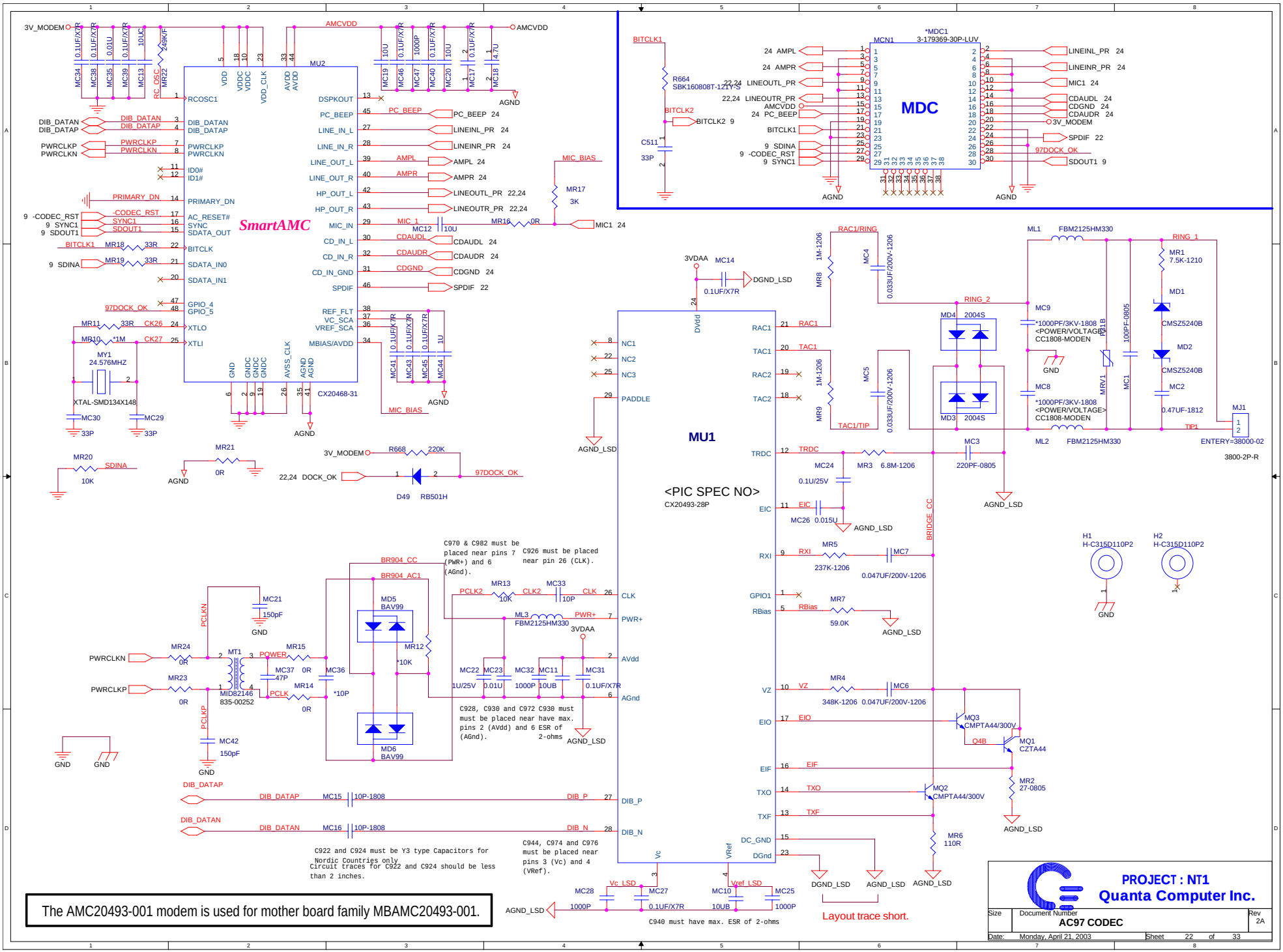


CABLE DOCK



PROJECT : NT1
Quanta Computer Inc.

Size	Document Number	Rev
	MINI-PCI	1A
Date: Monday, April 21, 2003	Sheet 21 of 33	


MU2
SmartAMC
CX20468-31
MU1
<PIC SPEC NO>
CX20493-28P
MDC
*MDC1
3-179369-30P-LUV
MCN1
The AMC20493-001 modem is used for mother board family MBAMC20493-001.
Layout trace short.
PROJECT : NT1
Quanta Computer Inc.
AC97 CODEC
Size
Document Number
Rev
2A
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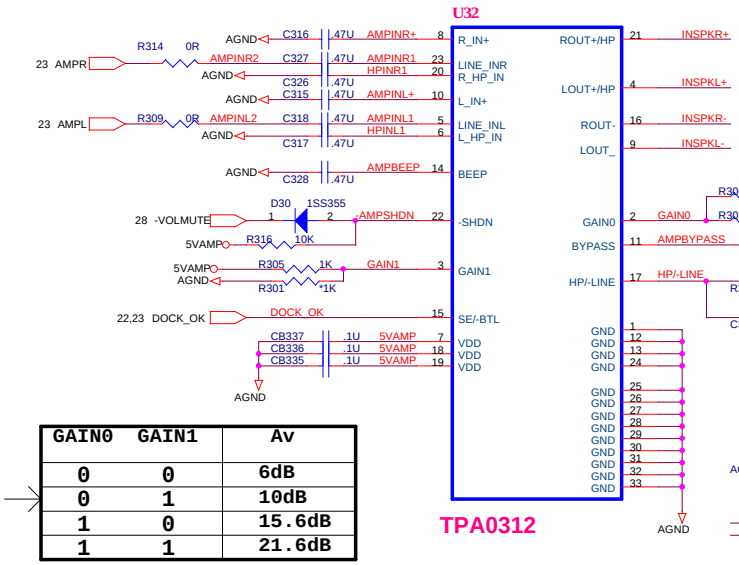
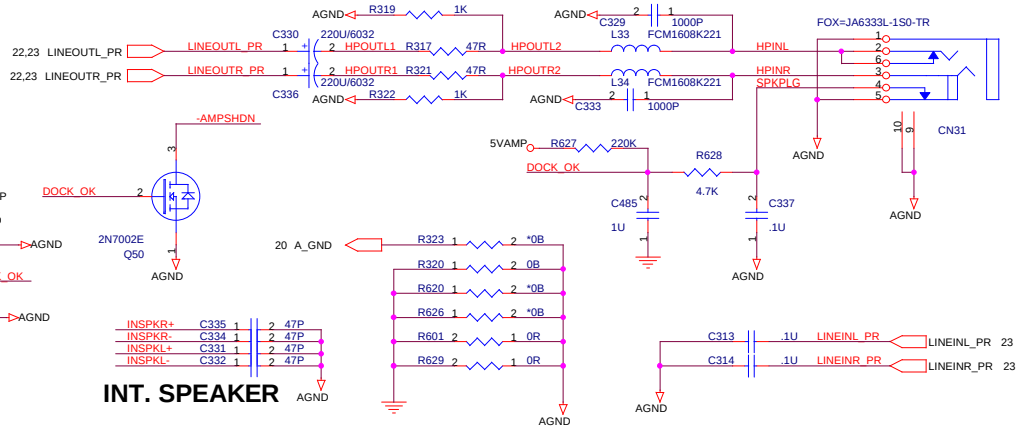
AUDIO AMPLIFIER



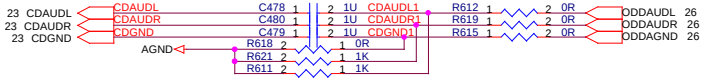
GAIN0	GAIN1	Av
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

HEADPHONE

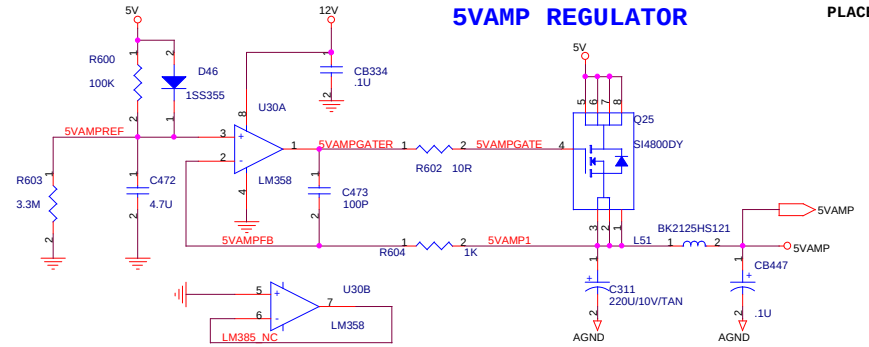


INT. SPEAKER

CD/PHONE INPUT & MONOOUT

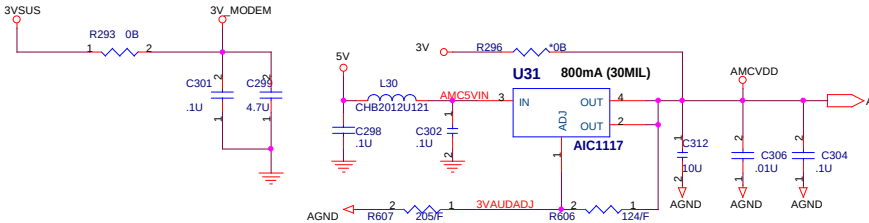


5VAMP REGULATOR

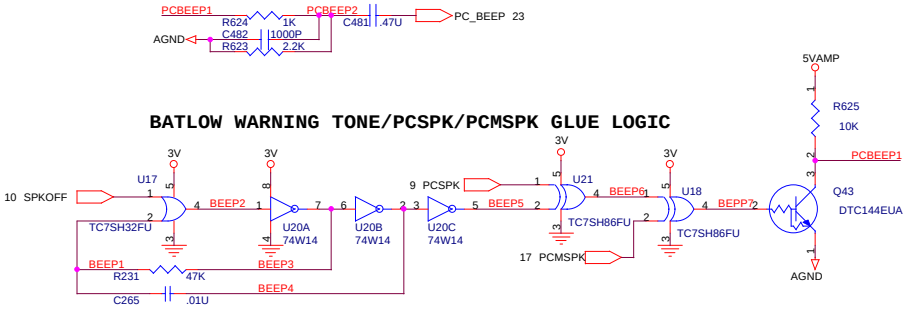


PLACE 5VAMP RELATIVE COMPONENT AS GROUT AND PUT BULK CAP NEAR OUTPUT

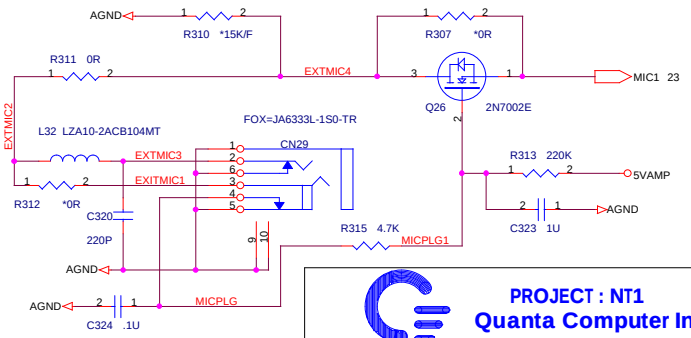
3VAUD REGULATOR



BATLOW WARNING TONE/PCSPK/PCMSPK GLUE LOGIC

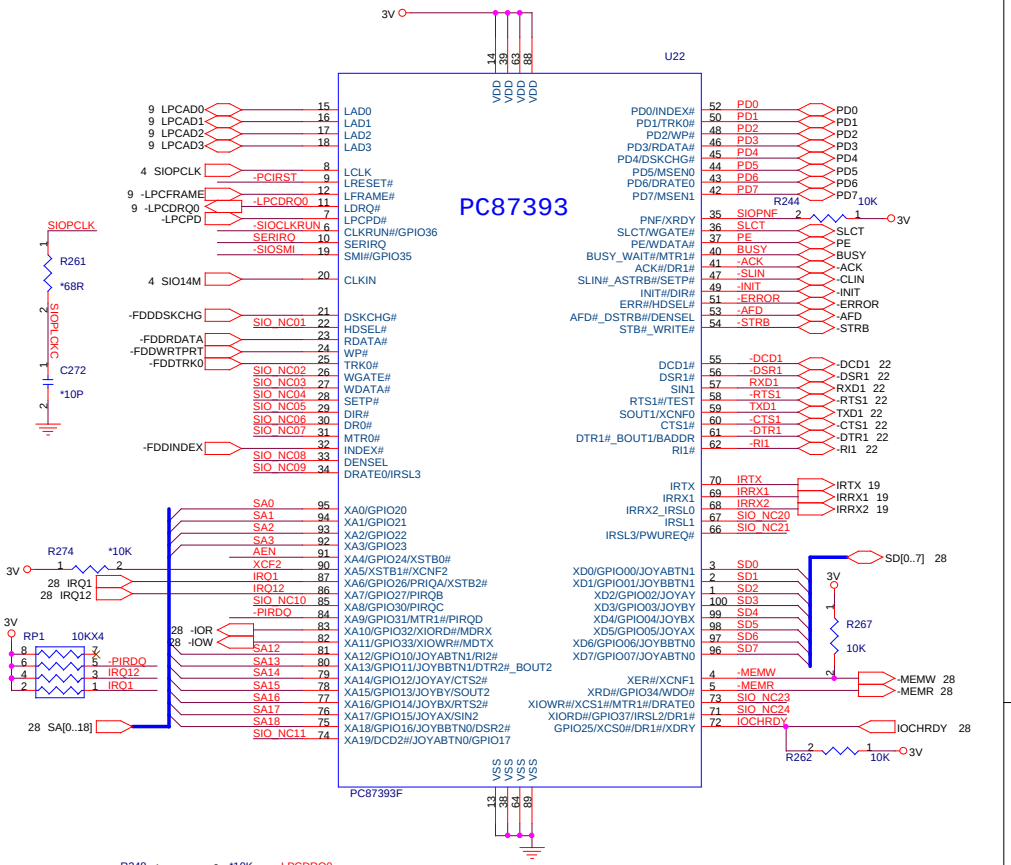


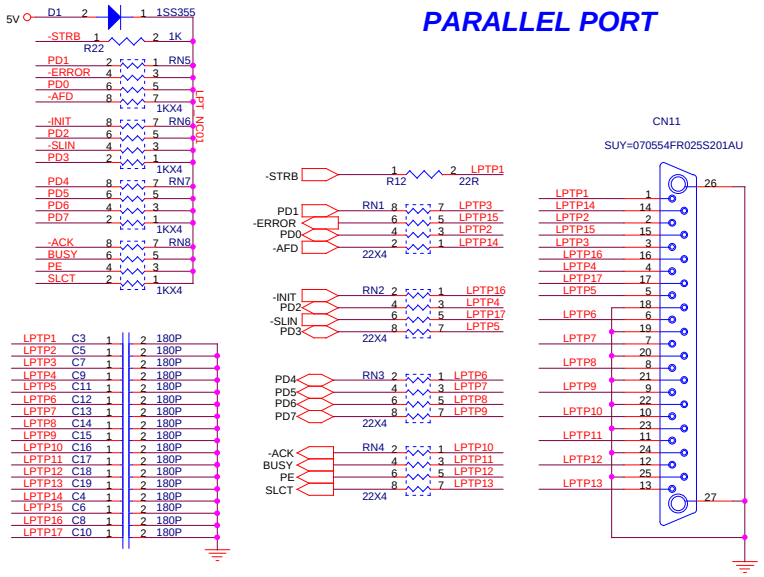
EXT MIC



PROJECT : NT1
Quanta Computer Inc.

Size	Document Number	Rev
	AUDIO AMP,HEADPHONE&SPEAKER	1A
Date: Monday, April 21, 2003	Sheet 23 of 33	





PLACEMENT NOTICE :

1. IDEALLY, PLACE 1 CAP PER POWER PIN AND BASED ON REAL CASE TO REDUCE.
2. SIOPCLKC RELATIVE R/C MUST NEAR SIO CHIP
3. 3243V+/- CAP MUST NEAR 3243 CHIP
4. IRVCC,IRDPR AND IRGND RELATIVE R/C MUST NEAR IR MODULE
5. COM AND PARALLEL PORT RELATIVE R/C MUST NEAR CONNECTOR
6. FDD PULLUP MUST NEAR FDD CONNECTOR

PROJECT : NT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SIO PC87391	1A
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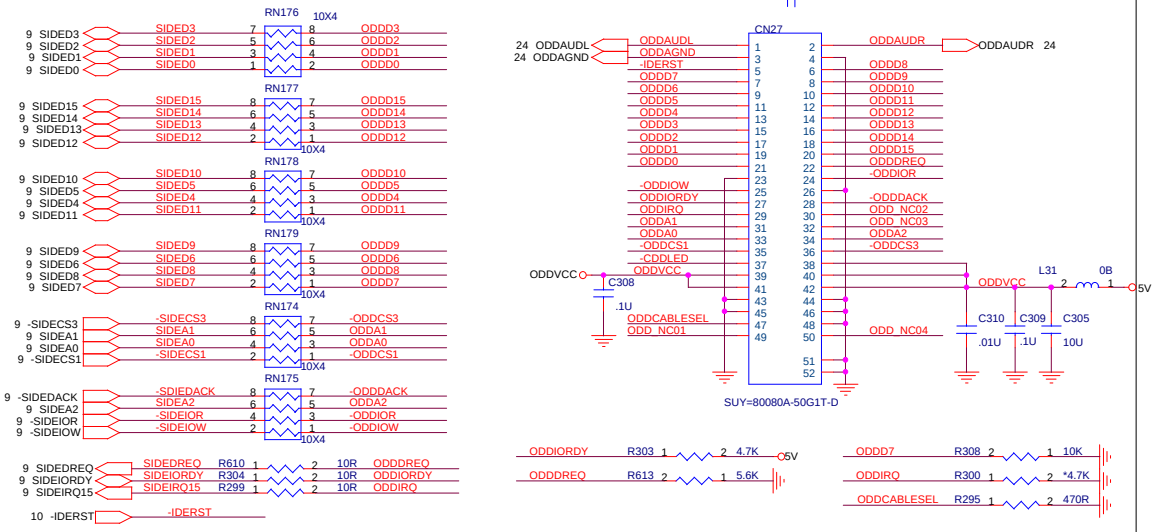
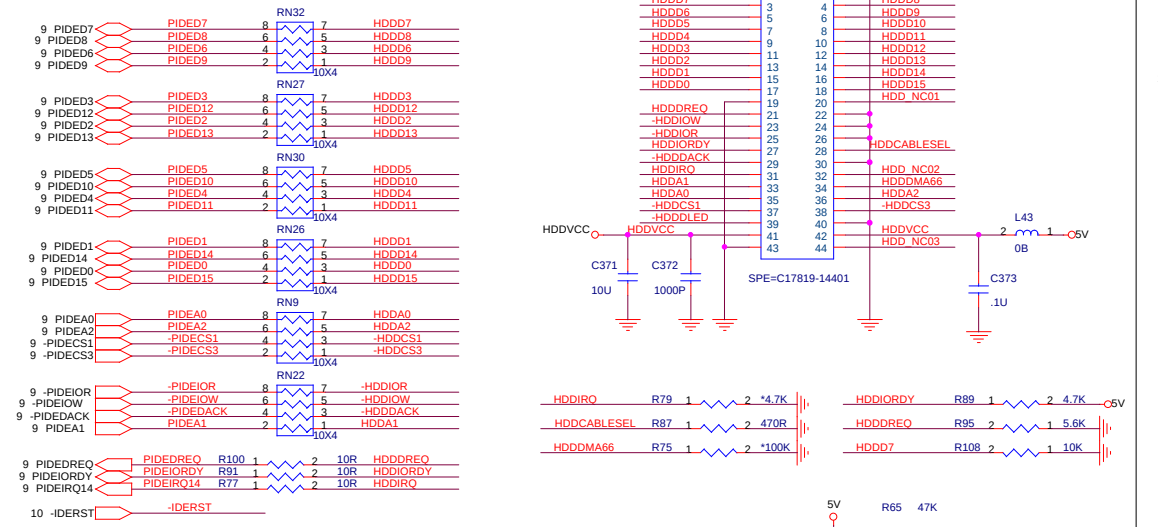
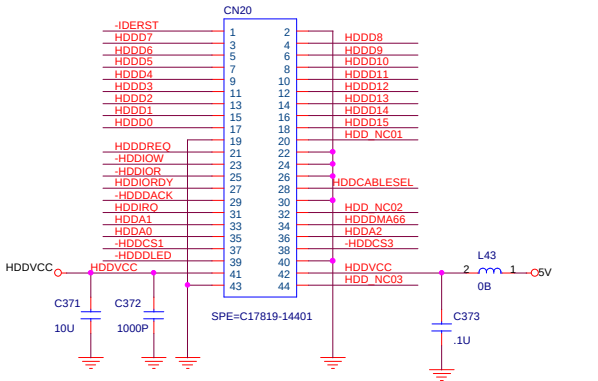
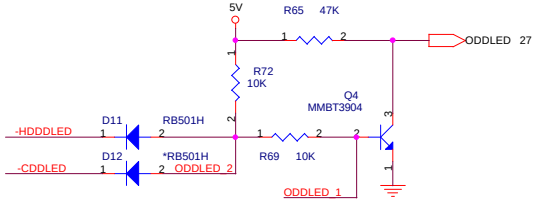
ODD CONNECTOR



HDD CONNECTOR



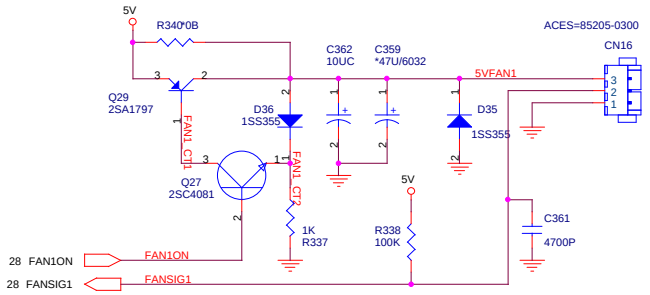




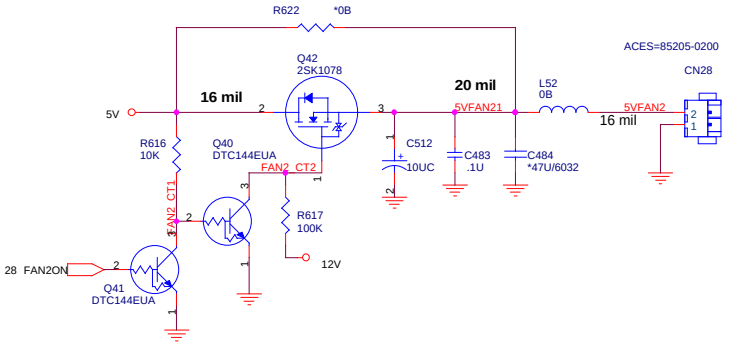
PLACEMENT NOTICE :

1. PUT THE BYPASS CAP AND INDUCTOR NEAR THE HDD AND ODD CONNECTOR
2. ALL DAMPING RESISTORS SHOULD NEAR ODD AND HDD CONNECOTR RESPECTIVELY
3. ALL PULLUP AND PULLDN SHOULD NEAR THE CONNECTOR
4. ALL IDE TRACE SHOULD KEEP 5:15 ID POSSIBLE AND 5:10 IS MINIMUM REQUIREMENT

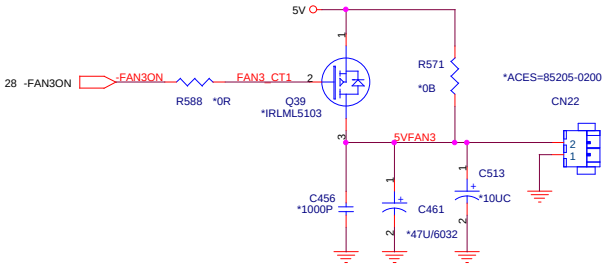
FAN1 OUT CONNECTOR



FAN2 OUT CONNECTOR



FAN3 OUT CONNECTOR



PROJECT : NT1
Quanta Computer Inc.

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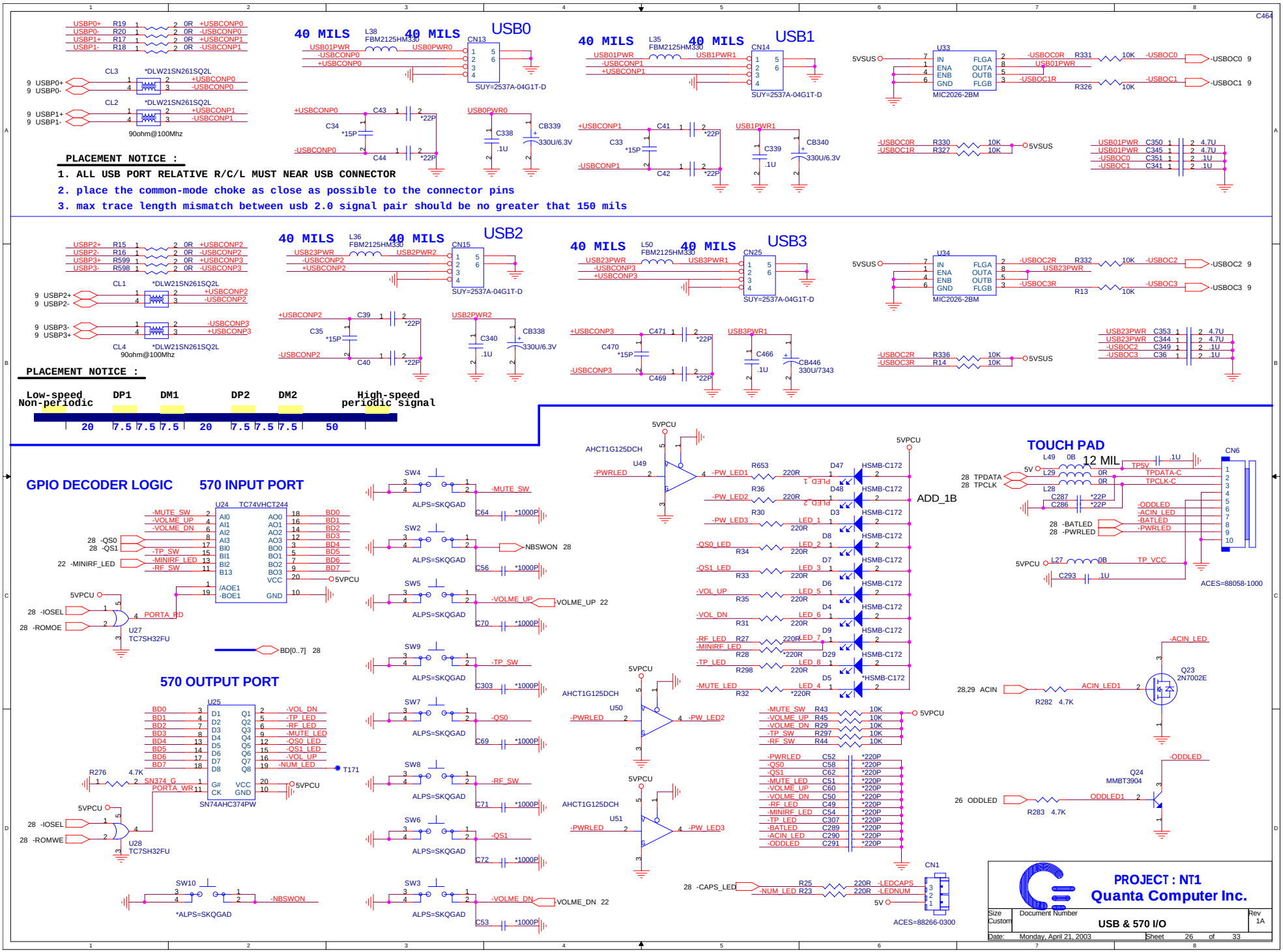
USB0
USB1
USB2
USB3
40 MILS
L38 FBM2125HM330
L35 FBM2125HM330
L36 FBM2125HM330
L50 FBM2125HM330
CN13
CN14
CN15
CN25
SUY=2537A-04G1T-D
MIC2026-2BM
U33
U34
90ohm@100Mhz
PLACEMENT NOTICE :
1. ALL USB PORT RELATIVE R/C/L MUST NEAR USB CONNECTOR
2. place the common-mode choke as close as possible to the connector pins
3. max trace length mismatch between usb 2.0 signal pair should be no greater that 150 mils
PLACEMENT NOTICE :
Low-speed Non-periodic
DP1
DM1
DP2
DM2
High-speed periodic signal
20
7.5
7.5
7.5
20
7.5
7.5
7.5
50
GPIO DECODER LOGIC
570 INPUT PORT
570 OUTPUT PORT
U24 TC74VHCT244
U25 SN74AHC374PW
U27 TC7SH32FU
U28 TC7SH32FU
U49
U50
U51
AHCT1G125DCH
ADD_1B
TOUCH PAD
12 MIL
CN6
ACES=88058-1000
CN1
ACES=88266-0300
Q23 2N7002E
Q24 MMBT3904
PROJECT : NT1
Quanta Computer Inc.
USB & 570 I/O
Size Custom
Document Number
Rev 1A
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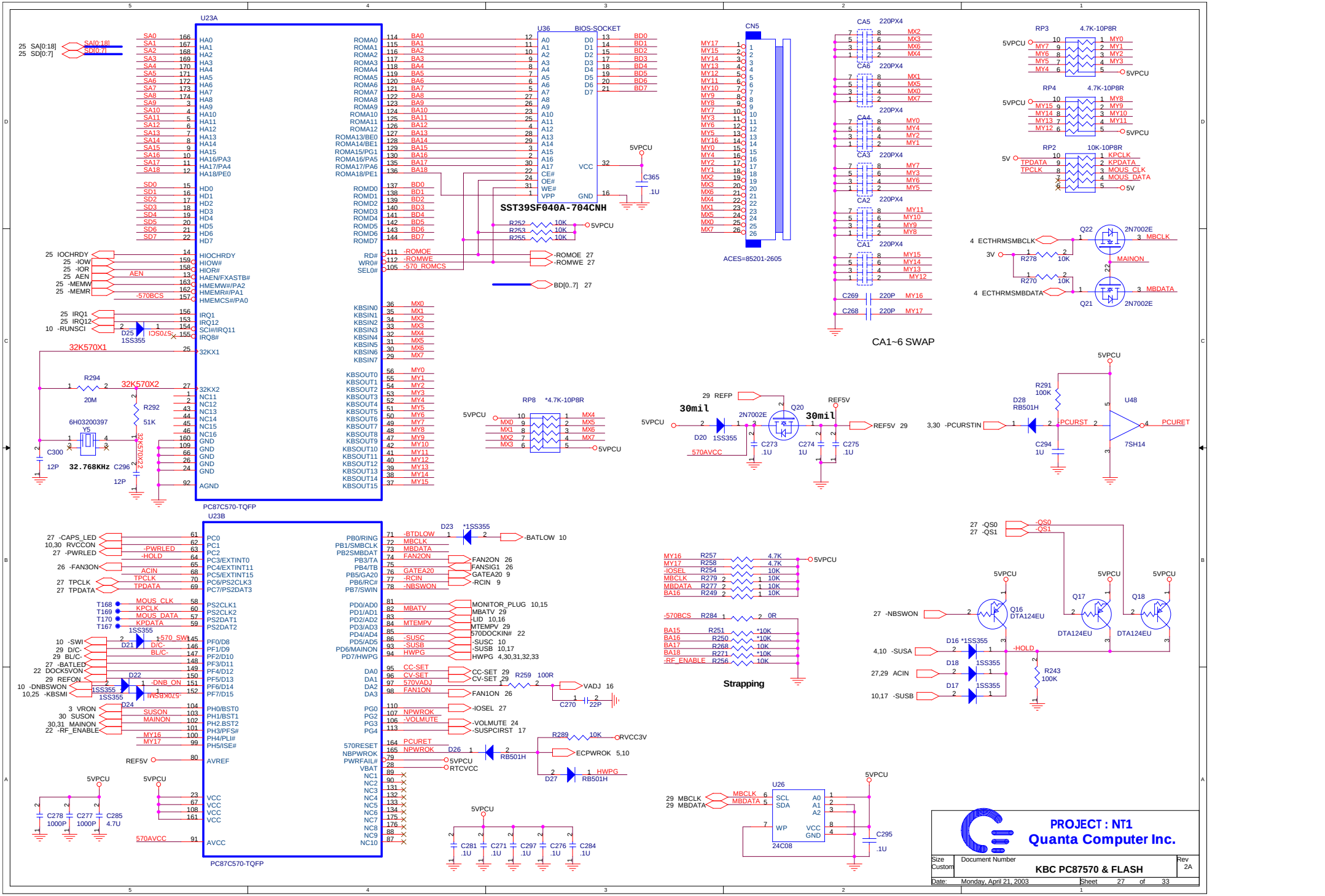
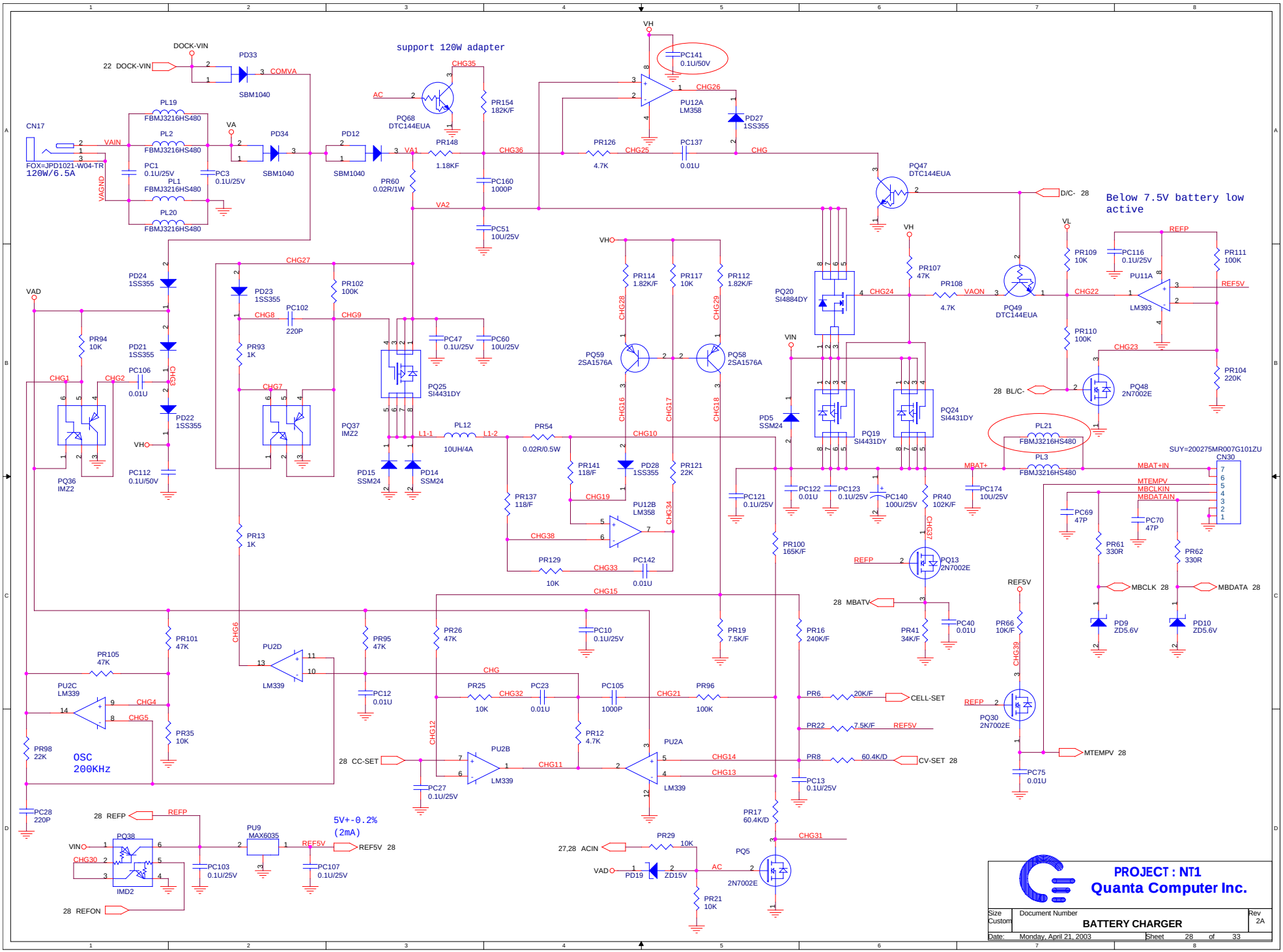

U23A
PC87C570-TQFP
SST39SF040A-704CNH
U36 BIOS-SOCKET
CN5
ACES=85201-2605
CA1~6 SWAP
RP3 4.7K-10P8R
RP4 4.7K-10P8R
RP2 10K-10P8R
RP8 *4.7K-10P8R
32K570X1
32K570X2
32.768KHz
6H03200397
U23B
PC87C570-TQFP
Strapping
U26
24C08
PROJECT : NT1
Quanta Computer Inc.
KBC PC87570 & FLASH
Monday, April 21, 2003


support 120W adapter
DOCK-VIN
22 DOCK-VIN
PD33
SBM1040
COMVA
CN17
FOX=JPD1021-W04-TR
120W/6.5A
VAIN
VAGND
PL19
PL2
PL1
PL20
FBMJ3216HS480
PC1
0.1U/25V
PC3
0.1U/25V
VA
PD34
PD12
VA1
PR148
1.18KF
PR60
0.02R/1W
CHG35
AC
PQ68
DTC144EUA
PR154
182K/F
CHG36
VA2
PC160
1000P
PC51
10U/25V
VH
PC141
0.1U/50V
PU12A
LM358
CHG26
PD27
1SS355
PR126
4.7K
CHG25
PC137
0.01U
CHG
PQ47
DTC144EUA
D/C- 28
Below 7.5V battery low active
VL
REFP
PR109
10K
PC116
0.1U/25V
PR111
100K
PU11A
LM393
REF5V
CHG22
PR110
100K
CHG23
PR104
220K
28 BL/C-
PQ48
2N7002E
PR107
47K
PR108
4.7K
VAON
PQ49
DTC144EUA
PQ20
SI4884DY
CHG24
VIN
PQ24
SI4431DY
PQ19
SI4431DY
PD5
SSM24
PL21
FBMJ3216HS480
PL3
FBMJ3216HS480
MBAT+
MBAT+IN
SUY=200275MR007G101ZU
CN30
MTEMPV
MBCLKIN
MBDATAIN
PC69
47P
PC70
47P
PR61
330R
PR62
330R
MBCLK 28
MBDATA 28
PD9
ZD5.6V
PD10
ZD5.6V
PC121
0.1U/25V
PC122
0.01U
PC123
0.1U/25V
PC140
100U/25V
PR40
102K/F
PC174
10U/25V
CHG37
PQ13
2N7002E
REFP
28 MBATV
PR41
34K/F
PC40
0.01U
REF5V
PR66
10K/F
CHG39
PQ30
2N7002E
MTEMPV 28
PC75
0.01U
PR100
165K/F
PR19
7.5K/F
PR16
240K/F
PR6
20K/F
CELL-SET
PR22
7.5K/F
REF5V
PR8
60.4K/D
CV-SET 28
PC13
0.1U/25V
PR17
60.4K/D
CHG31
PR29
10K
27,28 ACIN
PQ5
2N7002E
PD19
ZD15V
PR21
10K
VAD
PD24
1SS355
PD21
1SS355
PD22
1SS355
PD23
1SS355
PC102
220P
CHG8
CHG9
CHG27
PR102
100K
PR93
1K
CHG7
PR94
10K
CHG1
CHG2
PC106
0.01U
CHG3
PC112
0.1U/50V
PR13
1K
PQ36
IMZ2
PQ37
IMZ2
PQ25
SI4431DY
PC47
0.1U/25V
PC60
10U/25V
PD15
SSM24
PD14
SSM24
L1-1
PL12
10UH/4A
L1-2
PR54
0.02R/0.5W
PR114
1.82K/F
PR117
10K
PR112
1.82K/F
CHG28
CHG29
PQ59
2SA1576A
PQ58
2SA1576A
CHG16
CHG17
CHG18
PR141
118/F
PD28
1SS355
PR121
22K
CHG10
CHG19
PU12B
LM358
CHG34
CHG38
PR137
118/F
PR129
10K
PC142
0.01U
CHG33
CHG15
PR101
47K
PR105
47K
PU2C
LM339
CHG4
CHG5
PR35
10K
PR98
22K
OSC
200KHz
PC28
220P
CHG6
PU2D
LM339
PR95
47K
PC12
0.01U
PR26
47K
CHG
PC10
0.1U/25V
PR25
10K
CHG32
PC23
0.01U
PC105
1000P
CHG21
PR96
100K
PR12
4.7K
CHG12
28 CC-SET
PU2B
LM339
CHG11
PU2A
LM339
CHG14
CHG13
PC27
0.1U/25V
28 REFP
REFP
PU9
MAX6035
REF5V
REF5V 28
5V+-0.2%
(2mA)
PQ38
IMD2
CHG30
VIN
PC103
0.1U/25V
PC107
0.1U/25V
28 REFON
PROJECT : NT1
Quanta Computer Inc.
Size
Custom
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BATTERY CHARGER
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2A
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Monday, April 21, 2003
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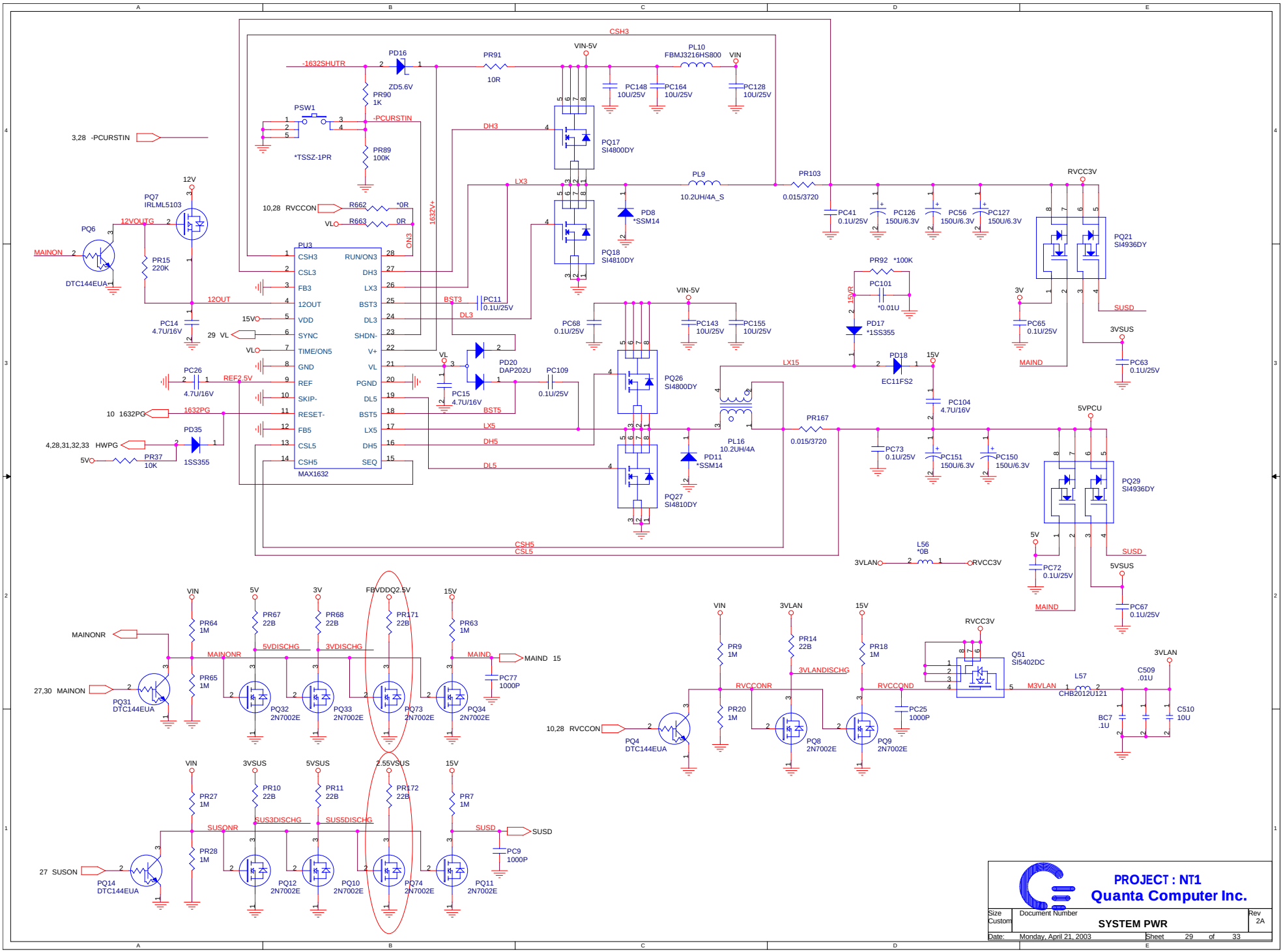

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Quanta Computer Inc.

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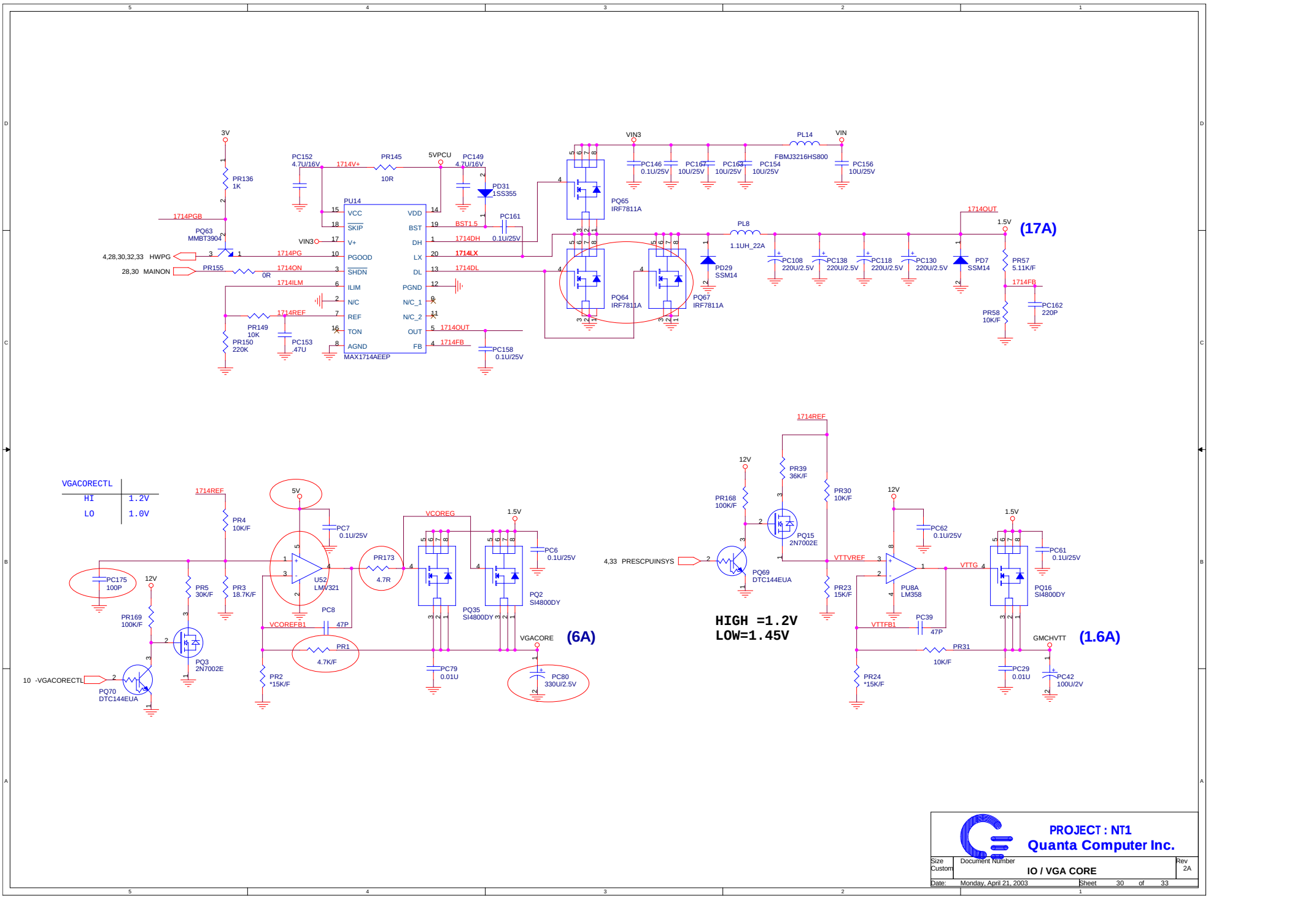
3V
PR136 1K
1714PGB
PQ63 MMBT3904
4,28,30,32,33 HWPG
28,30 MAINON
PR155 0R
1714PG
1714ON
1714ILM
1714REF
PR149 10K
PR150 220K
PC153 .47U
PC152 4.7U/16V
1714V+
PR145 10R
5VPCU
PC149 4.7U/16V
PD31 1SS355
PC161 0.1U/25V
BST1.5
1714DH
1714LX
1714DL
1714OUT
1714FB
PC158 0.1U/25V
PU14
MAX1714AEEP
VCC
SKIP
V+
PGOOD
SHDN
ILIM
N/C
REF
TON
AGND
VDD
BST
DH
LX
DL
PGND
N/C_1
N/C_2
OUT
FB
VIN3
PC146 0.1U/25V
PC147 10U/25V
PC163 10U/25V
PC154 10U/25V
PC156 10U/25V
PL14
FBMJ3216HS800
VIN
PQ65 IRF7811A
PQ64 IRF7811A
PQ67 IRF7811A
PD29 SSM14
PL8
1.1UH_22A
PC108 220U/2.5V
PC138 220U/2.5V
PC118 220U/2.5V
PC130 220U/2.5V
PD7 SSM14
PR57 5.11K/F
PR58 10K/F
PC162 220P
1.5V
(17A)
VGACORECTL
HI 1.2V
LO 1.0V
PR4 10K/F
PR5 30K/F
PR3 18.7K/F
PC175 100P
PR169 100K/F
PQ3 2N7002E
PQ70 DTC144EUA
10 -VGACORECTL
U52 LMV321
PC7 0.1U/25V
PC8 47P
PR1 4.7K/F
PR2 *15K/F
PR173 4.7R
VCOREG
PQ35 SI4800DY
PQ2 SI4800DY
PC6 0.1U/25V
PC79 0.01U
PC80 330U/2.5V
VGACORE
(6A)
PR168 100K/F
PR39 36K/F
PR30 10K/F
PQ15 2N7002E
PQ69 DTC144EUA
4,33 PRESCPUINSYS
VTTVREF
PR23 15K/F
PR24 *15K/F
PU8A LM358
PC62 0.1U/25V
PC39 47P
VTTFB1
PR31 10K/F
VTTG
PC61 0.1U/25V
PQ16 SI4800DY
PC29 0.01U
PC42 100U/2V
GMCHVTT
(1.6A)
HIGH =1.2V
LOW=1.45V
PROJECT : NT1
Quanta Computer Inc.
Size Custom
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IO / VGA CORE
Rev 2A
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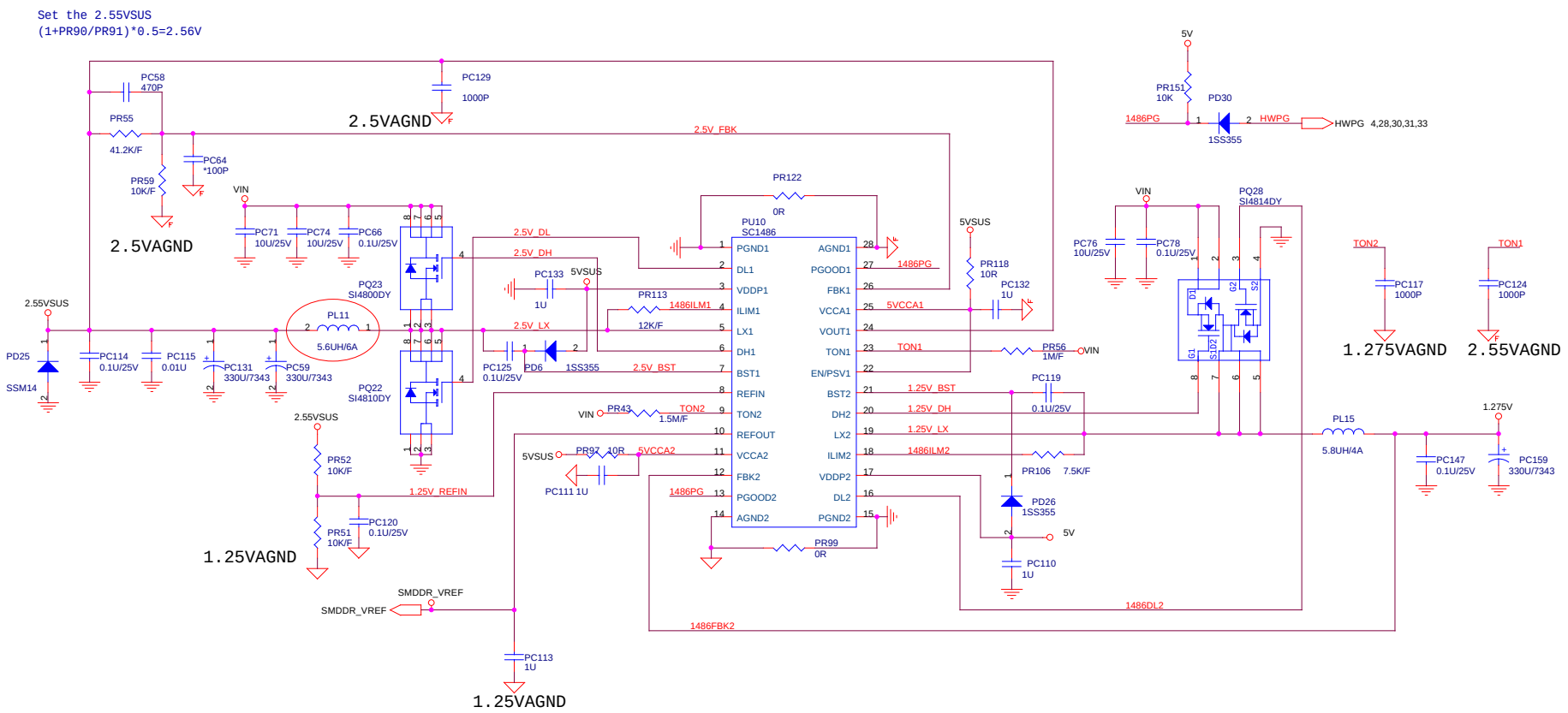
Set the 2.55VSUS
(1+PR90/PR91)*0.5=2.56V
PC58 470P
PR55 41.2K/F
PR59 10K/F
PC64 *100P
2.5VAGND
PC129 1000P
2.5VAGND
2.5V_FBK
VIN
PC71 10U/25V
PC74 10U/25V
PC66 0.1U/25V
PQ23 SI4800DY
PQ22 SI4810DY
PL11 5.6UH/6A
2.55VSUS
PD25 SSM14
PC114 0.1U/25V
PC115 0.01U
PC131 330U/7343
PC59 330U/7343
2.5V_DL
2.5V_DH
2.5V_LX
2.5V_BST
PC133 1U
5VSUS
PR113 12K/F
1486ILM1
PC125 0.1U/25V
PD6 1SS355
PR122 0R
PU10 SC1486
PGND1 DL1 VDDP1 ILIM1 LX1 DH1 BST1 REFIN TON2 REFOUT VCCA2 FBK2 PGOOD2 AGND2
AGND1 PGOOD1 FBK1 VCCA1 VOUT1 TON1 EN/PSV1 BST2 DH2 LX2 ILIM2 VDDP2 DL2 PGND2
1486PG
5VCCA1
TON1
1.25V_BST
1.25V_DH
1.25V_LX
1486ILM2
5VCCA2
PR118 10R
PC132 1U
PR56 1M/F
PC119 0.1U/25V
PR106 7.5K/F
PD26 1SS355
PC110 1U
PR99 0R
PR43 1.5M/F
TON2
PR97 10R
PC111 1U
1.25V_REFIN
PR52 10K/F
PR51 10K/F
PC120 0.1U/25V
1.25VAGND
SMDDR_VREF
PC113 1U
1.25VAGND
1486FBK2
1486DL2
5V
PR151 10K
PD30 1SS355
1486PG
HWPG
HWPG 4,28,30,31,33
PQ28 SI4814DY
PC76 10U/25V
PC78 0.1U/25V
PC117 1000P
PC124 1000P
1.275VAGND
2.55VAGND
PL15 5.8UH/4A
PC147 0.1U/25V
PC159 330U/7343
1.275V
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Quanta Computer Inc.
Size Custom
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2.55SUS / 1.275SUS
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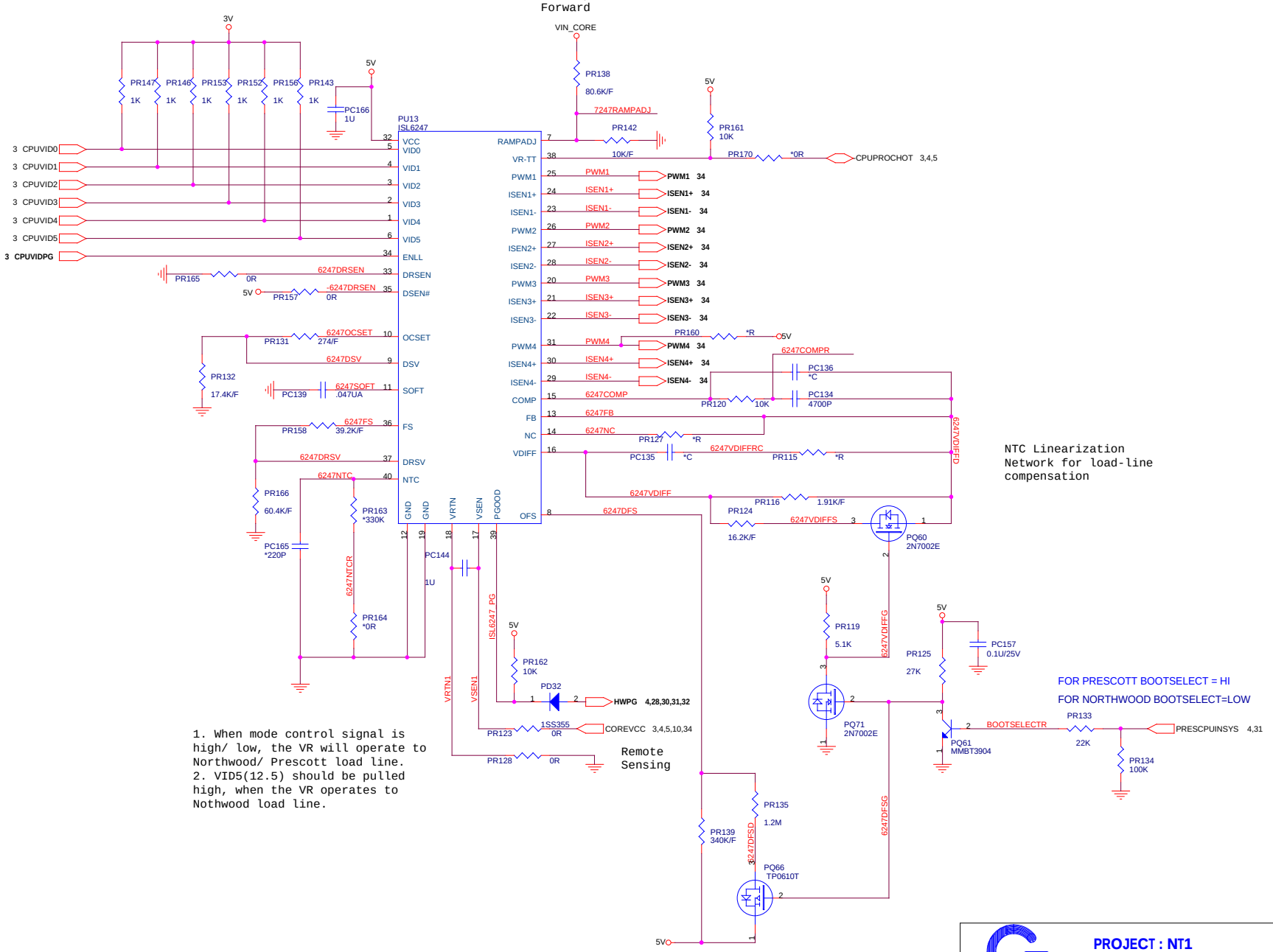
Battery Feed Forward
VIN_CORE
PR138
80.6K/F
7247RAMPADJ
PR142
PR161
10K
PR170
*0R
CPUPROCHOT 3,4,5
PU13
ISL6247
RAMPADJ
VR-TT
PWM1
ISEN1+
ISEN1-
PWM2
ISEN2+
ISEN2-
PWM3
ISEN3+
ISEN3-
PWM4
ISEN4+
ISEN4-
COMP
FB
NC
VDIFF
OFS
VCC
VID0
VID1
VID2
VID3
VID4
VID5
ENLL
DRSEN
DSEN#
OCSET
DSV
SOFT
FS
DRSV
NTC
GND
GND
VRTN
VSEN
PGOOD
3 CPUVID0
3 CPUVID1
3 CPUVID2
3 CPUVID3
3 CPUVID4
3 CPUVID5
3 CPUVIDPG
PR147 1K
PR146 1K
PR153 1K
PR152 1K
PR156 1K
PR143 1K
PC166 1U
PR165 0R
6247DRSEN
-6247DRSEN
PR157 0R
PR131 274/F
6247OCSET
6247DSV
PR132 17.4K/F
PC139 .047UA
6247SOFT
PR158 39.2K/F
6247FS
6247DRSV
6247NTC
PR166 60.4K/F
PR163 *330K
PC165 *220P
6247NTCR
PR164 *0R
PC144 1U
PWM1 34
ISEN1+ 34
ISEN1- 34
PWM2 34
ISEN2+ 34
ISEN2- 34
PWM3 34
ISEN3+ 34
ISEN3- 34
PR160 *R
PWM4 34
ISEN4+ 34
ISEN4- 34
6247COMP
PC136 *C
PR120 10K
PC134 4700P
6247FB
6247NC
PR127 *R
PC135 *C
6247VDIFFRC
PR115 *R
6247VDIFFFD
6247VDIFF
PR116 1.91K/F
PR124 16.2K/F
6247VDIFFS
PQ60 2N7002E
6247DFS
5V
PR119 5.1K
6247VDIFFG
PR125 27K
PC157 0.1U/25V
PQ71 2N7002E
PQ61 MMBT3904
BOOTSELECTR
PR133 22K
PR134 100K
PRESCPUINSYS 4,31
FOR PRESCOTT BOOTSELECT = HI
FOR NORTHWOOD BOOTSELECT=LOW
PR162 10K
PD32
1SS355
HWPG 4,28,30,31,32
COREVCC 3,4,5,10,34
PR123 0R
PR128 0R
ISL6247_PG
VRTN1
VSEN1
Remote Sensing
PR135 1.2M
PR139 340K/F
6247DFSD
6247DFSG
PQ66 TP0610T
NTC Linearization Network for load-line compensation
1. When mode control signal is high/ low, the VR will operate to Northwood/ Prescott load line.
2. VID5(12.5) should be pulled high, when the VR operates to Nothwood load line.
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Quanta Computer Inc.
Size Custom
Document Number
CORE VCC
Rev 2A
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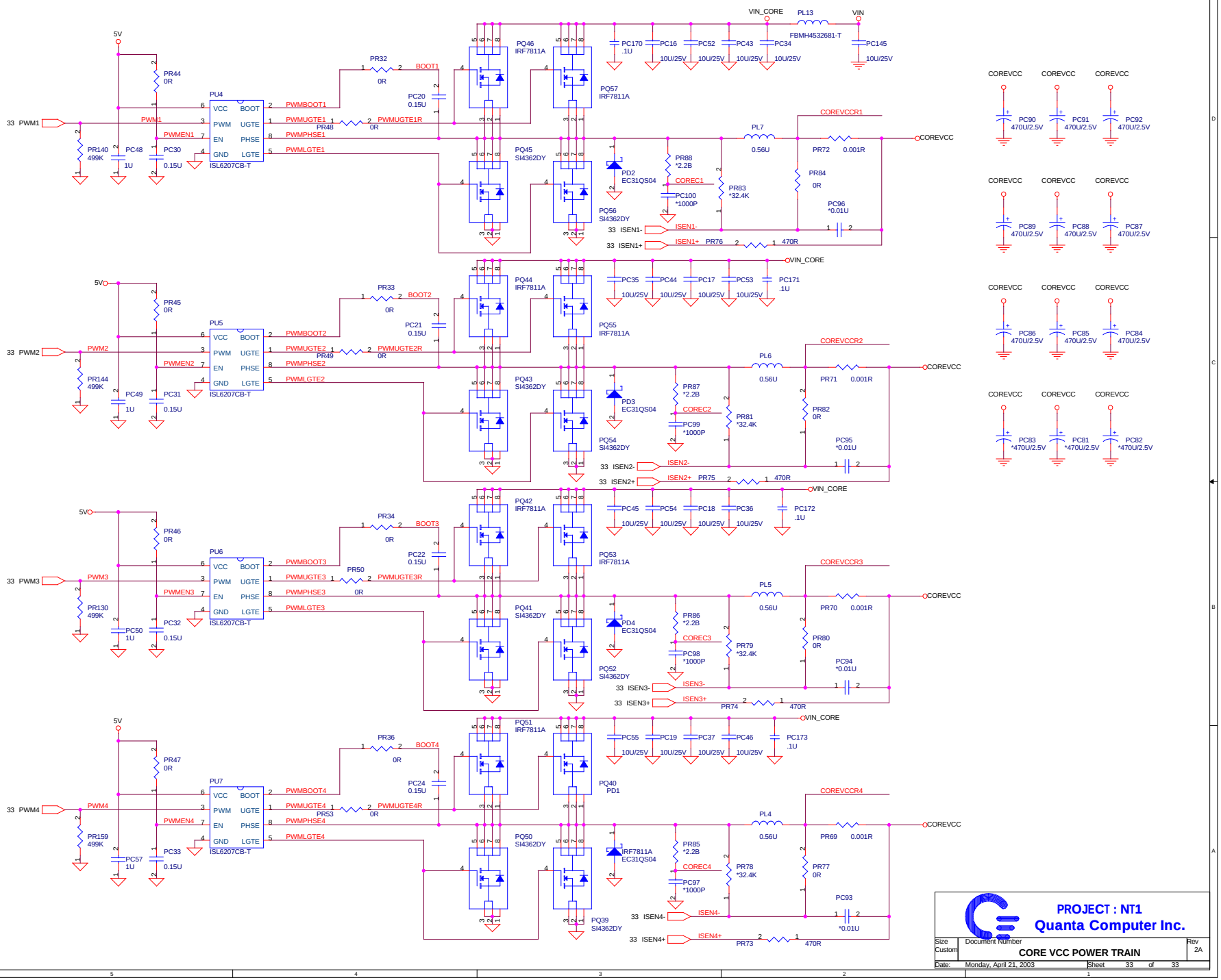
5V
VIN_CORE
PL13
FBMH4532681-T
VIN
PC145
10U/25V
PR44
0R
PU4
VCC
BOOT
PWM
UGTE
EN
PHSE
GND
LGTE
ISL6207CB-T
33 PWM1
PWM1
PWMEN1
PR140
499K
PC48
1U
PC30
0.15U
PR32
0R
BOOT1
PC20
0.15U
PWMBOOT1
PWMUGTE1
PR48
0R
PWMUGTE1R
PWMPHSE1
PWMLGTE1
PQ46
IRF7811A
PQ57
IRF7811A
PC170
.1U
PC16
10U/25V
PC52
10U/25V
PC43
10U/25V
PC34
10U/25V
PL7
0.56U
COREVCCR1
PR72
0.001R
COREVCC
PR88
*2.2B
COREC1
PC100
*1000P
PD2
EC31QS04
PR83
*32.4K
PR84
0R
PC96
*0.01U
PQ56
SI4362DY
PQ45
SI4362DY
33 ISEN1-
ISEN1-
33 ISEN1+
ISEN1+
PR76
470R
PC90
470U/2.5V
PC91
470U/2.5V
PC92
470U/2.5V
PC89
470U/2.5V
PC88
470U/2.5V
PC87
470U/2.5V
5V
PR45
0R
PU5
PWM2
PWMEN2
PR144
499K
PC49
1U
PC31
0.15U
PR33
0R
BOOT2
PC21
0.15U
PWMBOOT2
PWMUGTE2
PR49
0R
PWMUGTE2R
PWMPHSE2
PWMLGTE2
PQ44
IRF7811A
PQ55
IRF7811A
PC35
10U/25V
PC44
10U/25V
PC17
10U/25V
PC53
10U/25V
PC171
.1U
PL6
0.56U
COREVCCR2
PR71
0.001R
PR87
*2.2B
COREC2
PC99
*1000P
PD3
EC31QS04
PR81
*32.4K
PR82
0R
PC95
*0.01U
PQ54
SI4362DY
PQ43
SI4362DY
33 ISEN2-
ISEN2-
33 ISEN2+
ISEN2+
PR75
470R
PC86
470U/2.5V
PC85
470U/2.5V
PC84
470U/2.5V
PC83
*470U/2.5V
PC81
*470U/2.5V
PC82
*470U/2.5V
5V
PR46
0R
PU6
PWM3
PWMEN3
PR130
499K
PC50
1U
PC32
0.15U
PR34
0R
BOOT3
PC22
0.15U
PWMBOOT3
PWMUGTE3
PR50
0R
PWMUGTE3R
PWMPHSE3
PWMLGTE3
PQ42
IRF7811A
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10U/25V
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10U/25V
PC172
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1U
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PR36
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BOOT4
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PQ51
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PC37
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ISEN4+
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470R
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