R7X AMD SYSTEM DIAGRAM

01

+3V/+5V S5 PG.35
+1.1VS5/+2.5V PG.36
+1.2V PG.37
CPU Core PG.38~39
DDR3L PG.40
Charge PG.34
Dis-Charge PG.41
+VGACORE PG.42
+1.5 VGA PG.43
+1.0V/+1.8/ +3 VGA PG.44

SODIMM1 Max. 4GB PG.12 — 1600MT/s DDR3 L Channel A
SODIMM2 Max. 4GB PG.13 — 1600MT/s DDR3 L Channel B

AMD
35mm X 35mm
RICHLAND 722 pin uPGA
TDP 35W
DP0 DP1 DP2
PG.2~5

PCI-E x8
AMD
Sun XT
29mm X 29mm
64bit M2 package
25W
PG.13~19

eDP (5.4Gb/s)
DDI (5.4Gb/s)
DDR3 900MHz
VRAM
128Mx16x4 or 256Mx16x4 1GHz
PG.20~21

DP UMI

AMD FCH
BOLTON M3
24.5mm X 24.5mm
656pin FCBGA
TDP 4.7W
PG.6~10

eDP PG.23
eDP
REALTEK 2136R
DP to LVDS Converter
PAGE 22
LVDS Interface
LVDS PG.23
DP Port B
HDMI PG.25
CRT
CRT PG.24

PCI-E x 1
HDD PG.31 — SATA0
ODD PG.31 — SATA1

LANE1
LAN RTL8166EH 10/100 PG.29
WLAN BT COMBO PG.32 — USB 2.0 PORT8
LANE0
PCI-E x 1
LANE3

USB 3.0 PORT1,2
USB3.0 Ports X2 PG.28
Webcam PG.23
USB 2.0 PORT11,12 PORT2
PORT0 PORT3
USB2.0 Ports PG.29
Touch Screen (option) PG.26

Accelerometer PG.32
SMBUS
Card Reader RTS5239 PG.26

KBC ITE8528 PG.33 — LPC
KB PG.30
TP PG.30
ROM PG.33
FAN PG.31

TPM SLB9635 (option) PG.25

AUDIO CODEC ALC3227-CG PG.27
Speaker PG.27
COMBO JACK HP/MIC PG.28
DIGITAL MIC PG.23

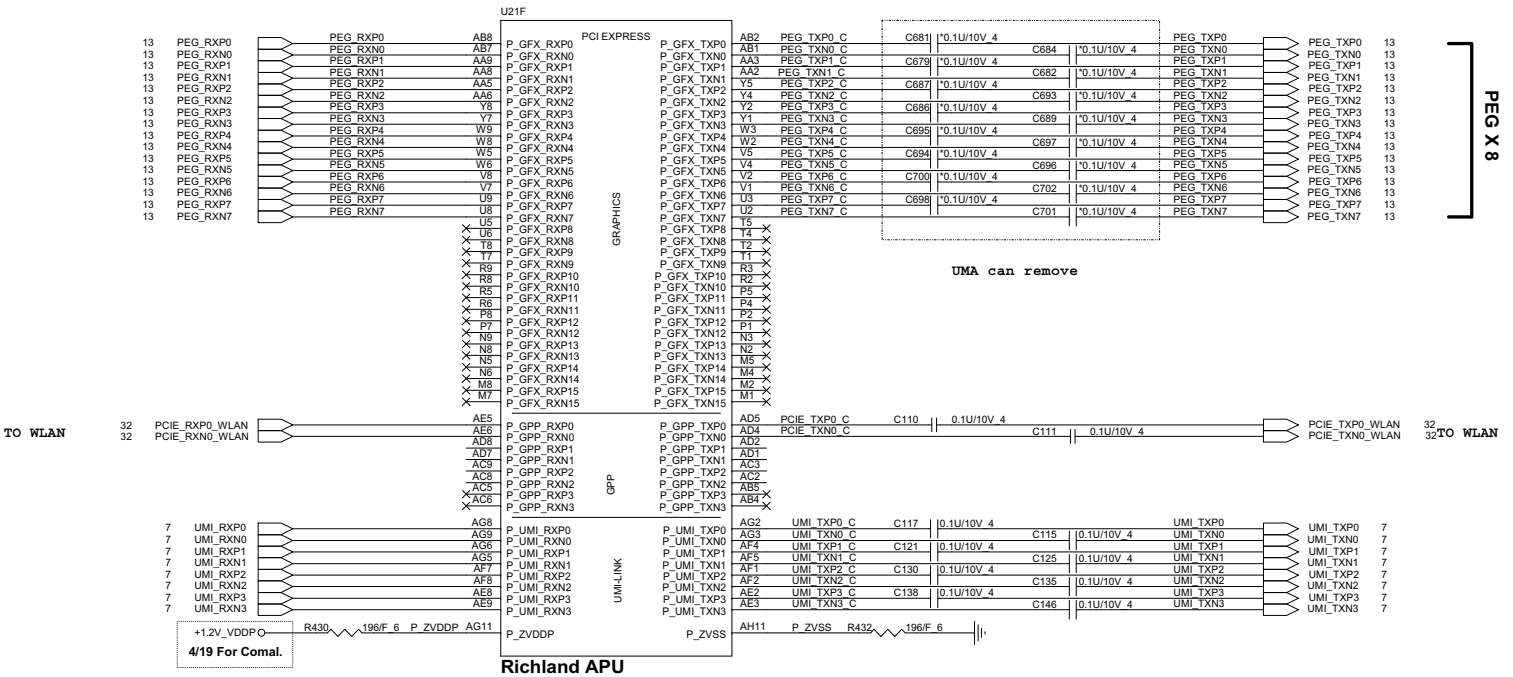
Stackup
TOP
GND
IN1
IN2
VCC
BOT

NB5

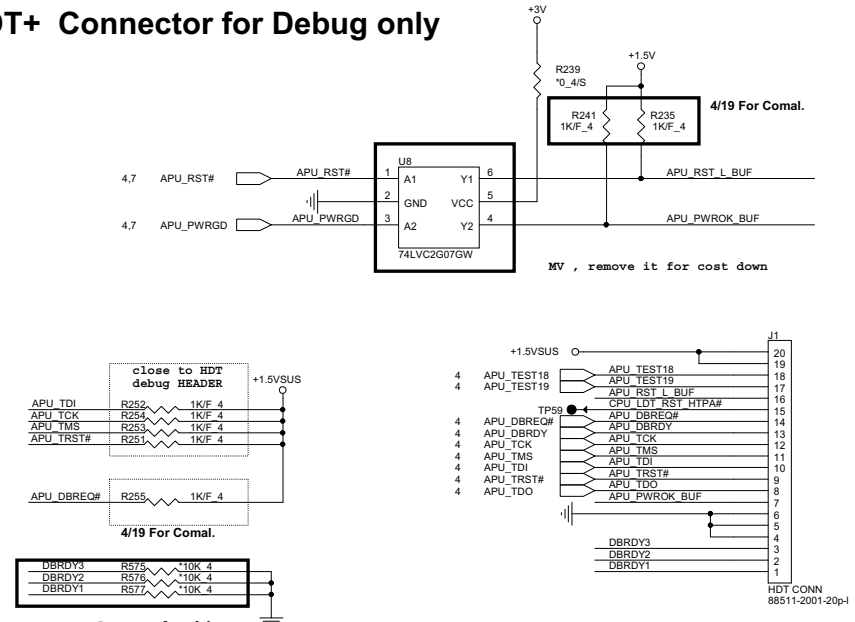
PROJECT : R7X
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

Date: Tuesday, March 12, 2013 Sheet 1 of 43

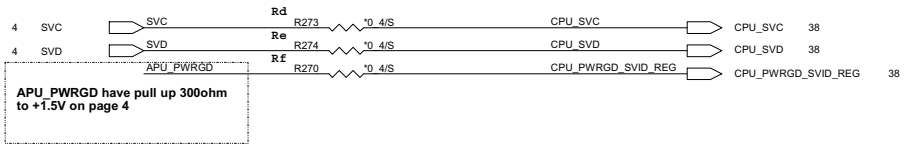


HDT+ Connector for Debug only

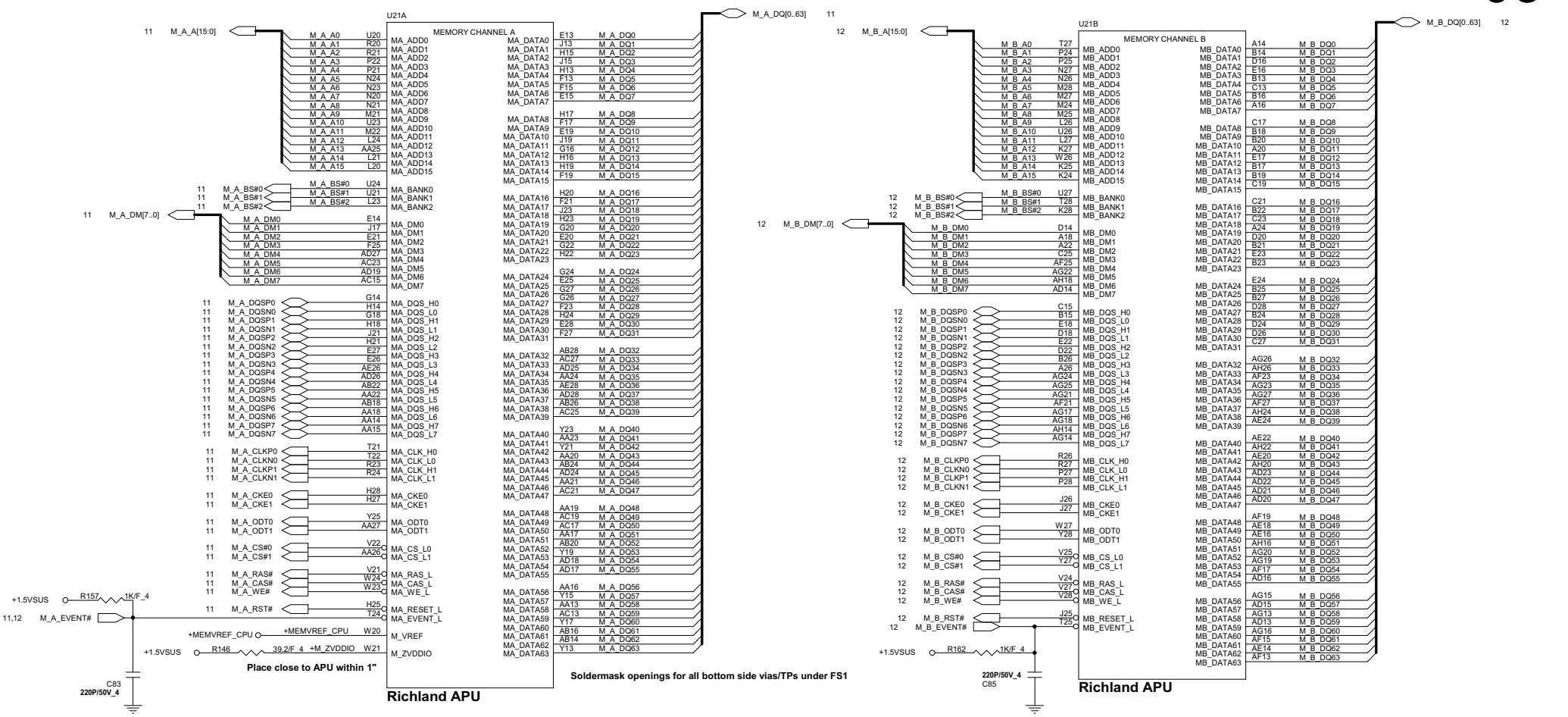


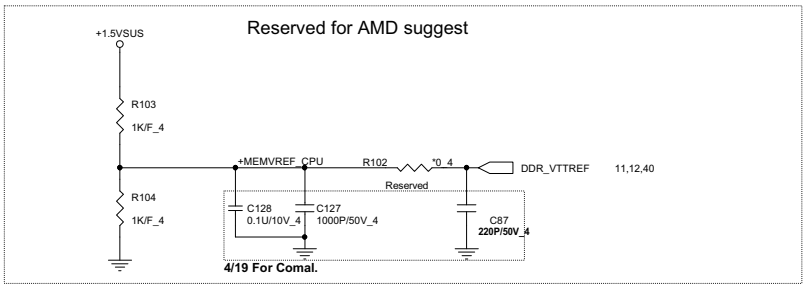
VID Override Circuit

		BOOT VOLTAGE	
SVC	SVD	VFIX +VDD =VCC/GND	VFIX +VDD =OPEN
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8



NB5	PROJECT : R7X Quanta Computer Inc.
Size: Custom	Document Number: APU 1/4(PCIE/UMI/GPP/HDT)
Rev: 1A	
Date: Tuesday, March 12, 2013	Sheet 2 of 43





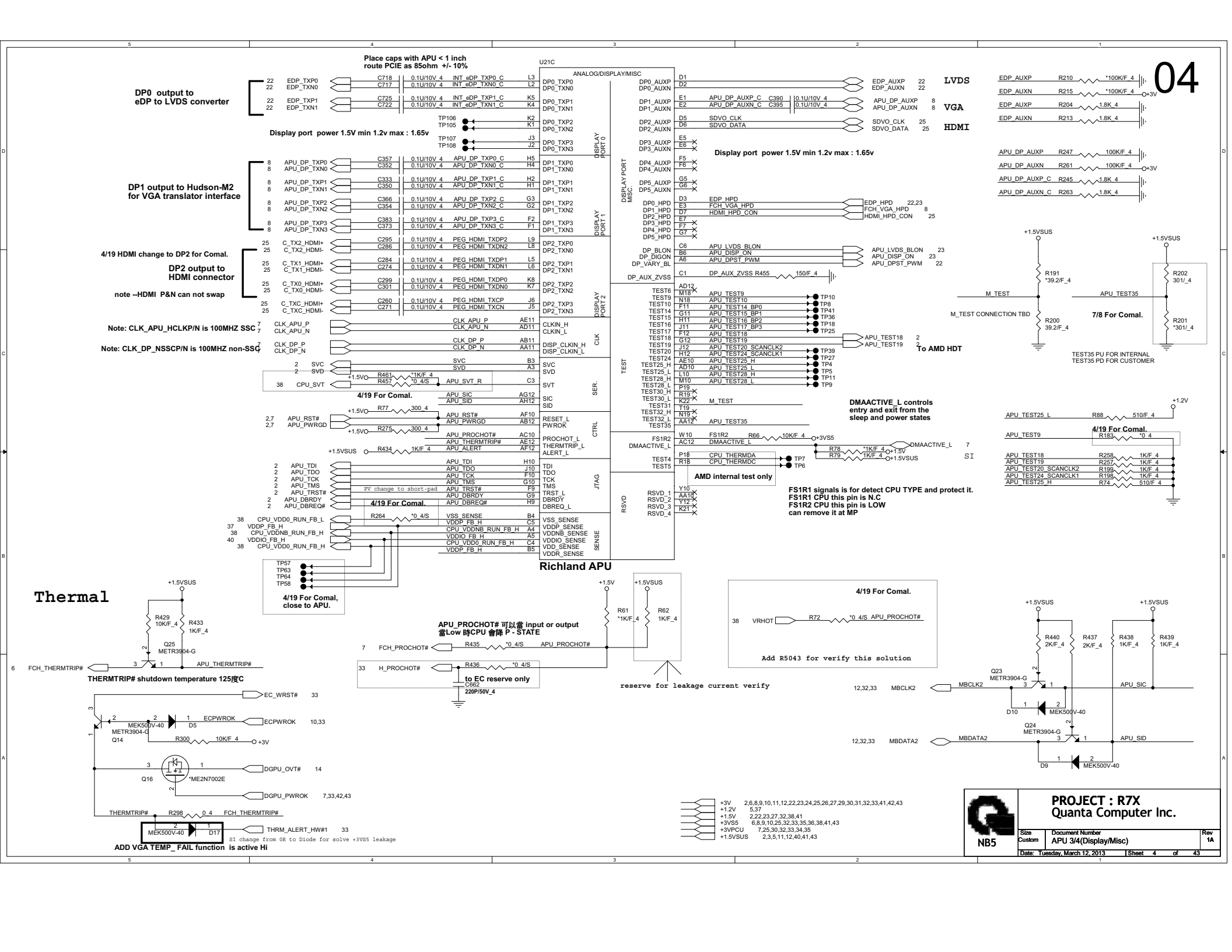
+3VS5 4,6,8,9,10,25,32,33,35,36,38,41,43
+1.5VSUS 2,4,5,11,12,40,41,43

NB5

PROJECT : R7X
Quanta Computer Inc.

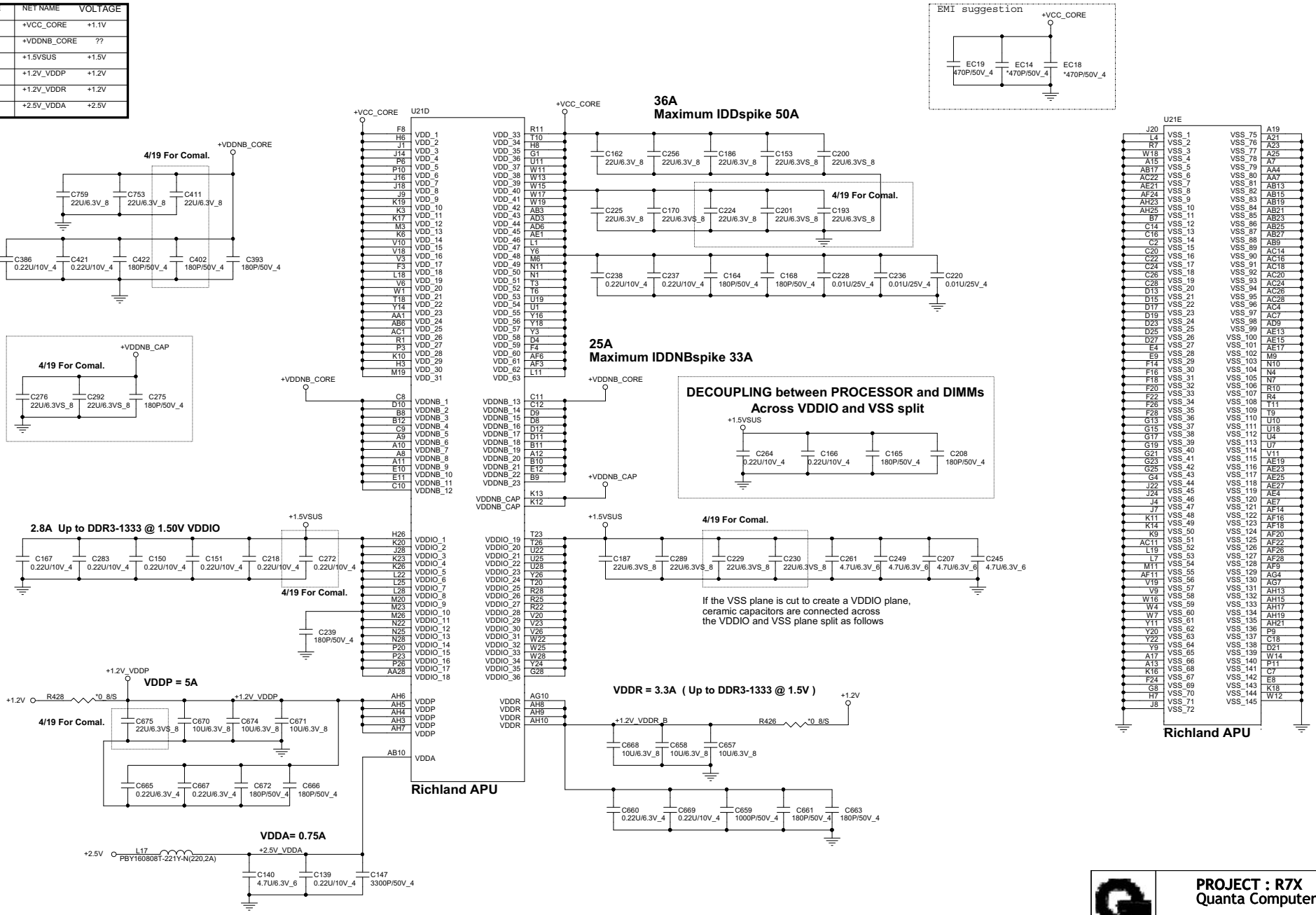
Size	Document Number	Rev
Custom	APU 2/4(DDR3 MEM I/F)	1A

Date: Tuesday, March 12, 2013 Sheet 3 of 43


04
Place caps with APU < 1 inch
route PCIE as 85ohm +/- 10%
U21C
ANALOG/DISPLAY/MISC
Richland APU
DP0 output to
eDP to LVDS converter
Display port power 1.5V min 1.2v max : 1.65v
DP1 output to Hudson-M2
for VGA translator interface
4/19 HDMI change to DP2 for Comal.
DP2 output to
HDMI connector
note --HDMI P&N can not swap
Note: CLK_APU_HCLKP/N is 100MHZ SSC
Note: CLK_DP_NSSCP/N is 100MHZ non-SSC
4/19 For Comal.
4/19 For Comal,
close to APU.
LVDS
VGA
HDMI
To AMD HDT
TEST35 PU FOR INTERNAL
TEST35 PD FOR CUSTOMER
7/8 For Comal.
DMAACTIVE_L controls
entry and exit from the
sleep and power states
AMD internal test only
FS1R1 signals is for detect CPU TYPE and protect it.
FS1R1 CPU this pin is N.C
FS1R2 CPU this pin is LOW
can remove it at MP
Thermal
THERMTRIP# shutdown temperature 125度C
APU_PROCHOT# 可以當 input or output
當Low 時CPU 會降 P - STATE
to EC reserve only
reserve for leakage current verify
Add R5043 for verify this solution
ADD VGA TEMP_ FAIL function is active Hi
SI change from 0R to Diode for solve +3VS5 leakage
+3V 2,6,8,9,10,11,12,22,23,24,25,26,27,29,30,31,32,33,41,42,43
+1.2V 5,37
+1.5V 2,22,23,27,32,38,41
+3VS5 6,8,9,10,25,32,33,35,36,38,41,43
+3VPCU 7,25,30,32,33,34,35
+1.5VSUS 2,3,5,11,12,40,41,43
PROJECT : R7X
Quanta Computer Inc.
NB5
Size Custom
Document Number APU 3/4(Display/Misc)
Rev 1A
Date: Tuesday, March 12, 2013
Sheet 4 of 43

APU POWER TABLE

PIN NAME	NET NAME	VOLTAGE
VDD	+VCC_CORE	+1.1V
VDDNB	+VDDNB_CORE	??
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V



NB5	PROJECT : R7X Quanta Computer Inc.	
Size: Custom	Document Number: APU 4/4(POWER/GND)	Rev: 1A
Date: Tuesday, March 12, 2013	Sheet 5 of 43	

remove PCIE_RST2# from AMD recommend

BOLTON-M3
Part 4 of 5

U28A

TP78 PCIE_RST2# AB6
TP112 RI# T2
W1
33 SUSB# SUSB# T3
33 SUSC# SUSC# W2
33 DNBSWON# DNBSWON# J4
10 FCH_PWRGD FCH_PWRGD N7

4/19 For Comal.

TP74 FCH_TEST0 T9
TP85 FCH_TEST1 T10
FCH_TEST2 V9
TP82 EC_A20GATE AE22

GEVENT0# internal pull Hi 8.2K to +3V
GEVENT1# internal pull Hi 8.2K to +3V
33 EC_A20GATE
33 EC_RCIN# EC_RCIN# AG19
TP76 FCH_PME# R9
SIO_EXT_SMI# C26

GEVENT23# internal pull Hi 8.2K to +3V
GEVENT5# internal pull Hi 8.2K to +3VS5
33 SIO_EXT_SMI#
33 SIO_EXT_SCI#
R497 *0_4/S GEVENT5# T5
SYS_RST# U4

PCIE_WAKE# no need to pull
Hi resistor from check list
29,32 PCIE_WAKE# PCIE_WAKE# K1
V9

GEVENT2# internal pull Hi 10K to +3VS5
C827 *100P/50V_4 FCH_THERMTRIP# R10
4 FCH_THERMTRIP# +3VO R366 10K/F_4 WD_PWRGD AF19

33 RSMRST# RSMRST# U2

CLK_REQ4# internal pull Hi 8.2K to +3V
CLK_REQ3# internal pull Hi 8.2K to +3V
26 CLK_PCIE_REQ2# CLK_PCIE_REQ2# AG24
29 PCIE_CLKREQ_LAN# PCIE_CLKREQ_LAN# AE24
AE26
AF22
AH17
AG18
AF24

27 ACZ_SPKR R378 *0_4/S FCH_GPIO66
11,12,22 SMB_RUN_CLK SMB_RUN_CLK AD26
11,12,22 SMB_RUN_DAT SMB_RUN_DAT AD25
30 SMB_PCH_CLK SMB_PCH_CLK T7
30 SMB_PCH_DAT SMB_PCH_DAT R7

CLK_REQ2# internal pull Hi 8.2K to +3V
32 PCIE_CLKREQ_WLAN# PCIE_CLKREQ_WLAN# AG25
CLKREQ1# AG22

LLB# Not Implemented ,left unconnected.
TP113 LLB# J2
TP100 SMARTVOLT2 AG26

This pin is used to power down VGA DAC regulators when CRT no connected
9 VGA_POWER_DOWN R358 *0_4/S VGA_PD V8
TP81 GBE_LED0 W8
8 SPI_HOLD# Y6
V10
AA8
TP98 AF25

TP115 M7
TP110 R8

GEVENT16# internal pull Hi 8.2K to +3VS5
31 ODD_PLUGIN# ODD_PLUGIN# T1
31 ODD_DA#_FCH ODD_DA#_FCH P6

GEVENT15# internal pull Hi 8.2K to +3VS5
TP83 F5
4/19 For Comal.
TP109 FCH_JTAG_TCK P5
TP114 FCH_JTAG_TDI J7
For Zero ODD
TP84 FCH_JTAG_RST# T6

R509 *10K/F_4 ACZ_BCLK_R AB3
ACZ_SDOUT_R AB1
HD audio interface is +3V_S5 voltage
TP125 ACZ_SDIN0 AA2
TP111 ACZ_SDIN1 Y5
TP116 ACZ_SDIN2_R Y3
TP117 ACZ_SDIN3_R Y1
ACZ_SYNC_R AD6
ACZ_RST#_R AE4

TP95 K19
TP96 J19
J21

32 BT_COMBO_OFF# BT_COMBO_OFF# D21
C20
13 VGA_RSTB VGA_RSTB D23
33 VGA_ON_SB VGA_ON_SB C22

F21
E20
F20
A22
E18
A20
J18
H18
G18
B21
K18
D19
A18
C18
B19
B17
A24
D17

BLINK/USB_OC7#/GEVENT18#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GEVENT17#
USB_OC4#/IR_RX0/GEVENT16#
USB_OC3#/AC_PRES/TDO/GEVENT15#
USB_OC2#/TCK/GEVENT14#
USB_OC1#/TDI/GEVENT13#
USB_OC0#/SPI_TPM_CS#/TRST#/GEVENT12#

AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO167
AZ_SDIN1/GPIO168
AZ_SDIN2/GPIO169
AZ_SDIN3/GPIO170
AZ_SYNC
AZ_RST#

PS2_DAT/SDA4/GPIO187
PS2_CLK/CEC/SCL4/GPIO188
SPI_CS2#/GBE_STAT2/GPIO166

PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192

KSO_0/GPIO209
KSO_1/GPIO210
KSO_2/GPIO211
KSO_3/GPIO212
KSO_4/GPIO213
KSO_5/GPIO214
KSO_6/GPIO215
KSO_7/GPIO216
KSO_8/GPIO217
KSO_9/GPIO218
KSO_10/GPIO219
KSO_11/GPIO220
KSO_12/GPIO221
KSO_13/GPIO222
KSO_14/XDBI/GPIO223
KSO_15/XDB1/GPIO224
KSO_16/XDB2/GPIO225
KSO_17/XDB3/GPIO226

EMBEDDED CTRL

GPIO
ACPI /WAKE UP EVENTS
USB 1.1
USB MISC
USB 2.0
USB OC
HD AUDIO
USB 3.0

USBCLK/14M_25M_48M_OSC G8
USB_RCOMP B9 USB_RCOMP_SB R514 11.8K/F_6
USB_FSD1P/GPIO186 H1
USB_FSD1N H3
USB_FSD0P/GPIO185 H6
USB_FSD0N H5
USB_HSD13P H10
USB_HSD13N G10
USB_HSD12P K10
USB_HSD12N J12
USB_HSD11P G12 USBP11+ USBP11+ 28
USB_HSD11N F12 USBP11- USBP11- 28 Left side USB Combo 3.0/2.0.
USB_HSD10P K12 USBP10+ USBP10+ 28
USB_HSD10N K13 USBP10- USBP10- 28 Left side USB Combo 3.0/2.0.
USB_HSD9P B11
USB_HSD9N D11
USB_HSD8P E10 USBP8+ 23
USB_HSD8N F10 USBP8- 23 Camera USB
USB_HSD7P C10 USBP7+ TP119
USB_HSD7N A10 USBP7- TP118
USB_HSD6P H9
USB_HSD6N G9
USB_HSD5P A8
USB_HSD5N C8
USB_HSD4P F8
USB_HSD4N E8
USB_HSD3P C6 USBP3+ 26
USB_HSD3N A6 USBN3- 26
USB_HSD2P C5 USBP2+ 32
USB_HSD2N A5 USBP2- 32 WLAN Min-Card
USB_HSD1P C1
USB_HSD1N C3
USB_HSD0P E1 USBP0+ 29
USB_HSD0N E3 USBP0- 29 Right side USB 2.0 Connector
USBSS_CALRP C16 USBSS_CALRP R531 1K/F_4
USBSS_CALRN A16 USBSS_CALRN R529 1K/F_4 +FCH_VDD_11_SSUSB_S
USB_SS_TX3P A14
USB_SS_TX3N C14
USB_SS_RX3P C12
USB_SS_RX3N A12
USB_SS_TX2P D15
USB_SS_TX2N B15
USB_SS_RX2P E14
USB_SS_RX2N F14
USB_SS_TX1P F15 USB30_TX1+ 28
USB_SS_TX1N G15 USB30_TX1- 28
USB_SS_RX1P H13 USB30_RX1+ 28
USB_SS_RX1N G13 USB30_RX1- 28
USB_SS_TX0P J16 USB30_TX0+ 28
USB_SS_TX0N H16 USB30_TX0- 28
USB_SS_RX0P J15 USB30_RX0+ 28
USB_SS_RX0N K15 USB30_RX0- 28

USB 3.0 Not Implemented: left unconnected

USB_SS_TX/RX0P/N	USB_HSD10P/N
USB_SS_TX/RX1P/N	USB_HSD11P/N
USB_SS_TX/RX2P/N	USB_HSD12P/N
USB_SS_TX/RX3P/N	USB_HSD13P/N

SCL2/GPIO193 H19 SCL2
SDA2/GPIO194 G19 SDA2
SCL3_LV/GPIO195 G22 SCL3
SDA3_LV/GPIO196 G21 SDA3
E22
EC_PWM0/EC_TIMER0/GPIO197 H22
EC_PWM1/EC_TIMER1/GPIO198
EC_PWM2/EC_TIMER2/WOL_EN/GPIO199 J22 EC_PWM2 EC_PWM2 10
EC_PWM3/EC_TIMER3/GPIO200 H21
No need for GPIO200
K21
KSI_0/GPIO201 K22
KSI_1/GPIO202 F22
KSI_2/GPIO203 F24
KSI_3/GPIO204 E24
KSI_4/GPIO205 B23
KSI_5/GPIO206 C24
KSI_6/GPIO207 F18
KSI_7/GPIO208

SCL3 of a TSI-capable APU's thermal bus,Pulled up to APU_VDDIO. Resistor value verified in the relevant APU design guide.

Bolton-M3

+3V
R369 2.2K_4 SMB_RUN_CLK
R365 2.2K_4 SMB_RUN_DAT
to DDR3 SMBUS
+3VS5
R508 *1K_4
J2 1 2 SYS_RST#
*SOLDERJUMPER-2
SYS_RST# internal 10K pull up

+3VS5
R370 10K/F_4 SCL3
R371 10K/F_4 SDA3
R364 2.2K_4 SCL2
R367 2.2K_4 SDA2
R344 2.2K_4 SMB_PCH_CLK
R343 2.2K_4 SMB_PCH_DAT
R360 *4.7K_4 FCH_THERMTRIP#
C551 *0.01U/25V_4
R544 *10K/F_4 PCIE_CLKREQ_WLAN#
R494 10K/F_4 DNBSWON#
R570 *10K/F_4 ODD_DA#_FCH
DB reserve

To Azalia

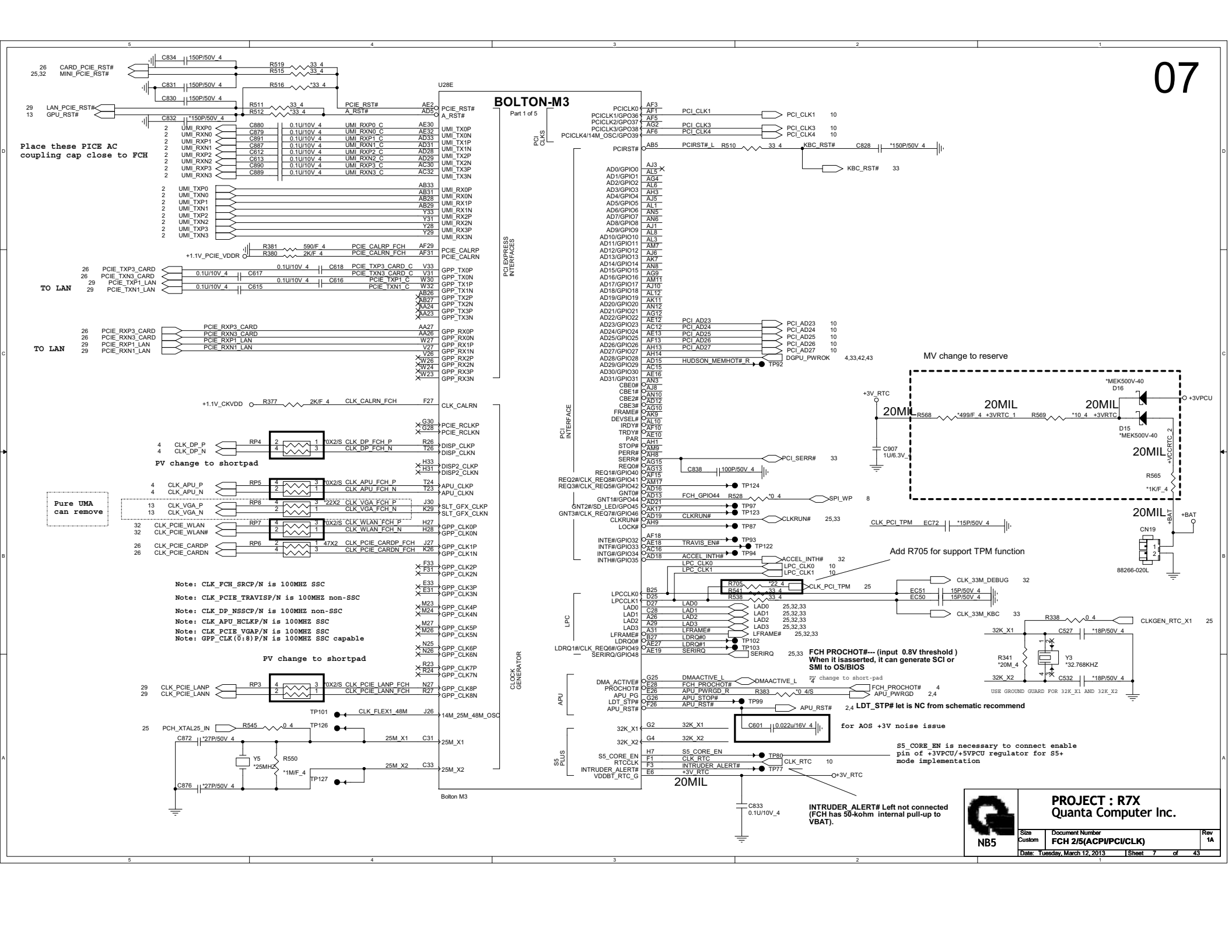
ACZ_SDOUT_R R496 33_4 ACZ_SDOUT_AUDIO 27
ACZ_SYNC_R R524 33_4 ACZ_SYNC_AUDIO 27
ACZ_BCLK_R R495 33_4 BIT_CLK_AUDIO 27
ACZ_RST#_R R522 33_4 ACZ_RST#_AUDIO 27
ACZ_SDIN0 ACZ_SDIN0 27

Pure UMA can remove
CLK_REQ# already internal pull up 8.2K
43 VGA_REQ 1 D6 2 CLKREQ1#
*MEK500V-40

Size: Custom	Document Number: FCH 1/5(GPIO/USB/AZ)		Rev: 1A
Date: Tuesday, March 12, 2013	Sheet 6 of 43		

NB5

PROJECT : R7X
Quanta Computer Inc.


07
BOLTON-M3
Part 1 of 5
U28E
Place these PICE AC coupling cap close to FCH
TO LAN
TO LAN
Pure UMA can remove
PV change to shortpad
PV change to shortpad
Note: CLK_FCH_SRCP/N is 100MHZ SSC
Note: CLK_PCIE_TRAVISP/N is 100MHZ non-SSC
Note: CLK_DP_NSSCP/N is 100MHZ non-SSC
Note: CLK_APU_HCLKP/N is 100MHZ SSC
Note: CLK_PCIE_VGAP/N is 100MHZ SSC
Note: GPP_CLK(0:8)P/N is 100MHZ SSC capable
PCI EXPRESS INTERFACES
CLOCK GENERATOR
PCI INTERFACE
LPC
APU
SS PLUS
PCI CLKS
MV change to reserve
Add R705 for support TPM function
FCH PROCHOT#--- (input 0.8V threshold) When it isasserted, it can generate SCI or SMI to OS/BIOS
LDT_STP# let is NC from schematic recommend
for AOS +3V noise issue
S5_CORE_EN is necessary to connect enable pin of +3VPCU/+5VPCU regulator for S5+ mode implementation
INTRUDER_ALERT# Left not connected (FCH has 50-kohm internal pull-up to VBAT).
USE GROUND GUARD FOR 32K_X1 AND 32K_X2
Bolton M3
NB5
PROJECT : R7X
Quanta Computer Inc.
Size Custom
Document Number FCH 2/5(ACPI/PCI/CLK)
Rev 1A
Date: Tuesday, March 12, 2013
Sheet 7 of 43

Vender	Size	P/N
AMIC	2M	AKE38ZN0801
WINBOND	2M	AKE38FP0N01
Socket		DFHS08FS023

08

FCH SPI ROM

Reserve for support quad read

Change U17 VDD from +3V to +3VS5 for AMD DG.

*MX25L1605DM2I-12G

ICT need TP2675 size test point

R place close to PCH

Reserve for debug

VGA Hot-plug

PLACE SATA AC COUPLING CAPS CLOSE TO HUDSON-M2/M3

PLACE SATA_CAL RES VERY CLOSE TO BALL OF HUDSON-M2/M3

4/19 For Comal.

Integrated Clock Mode: Leave unconnected.

Add GPIO for G-sensor LED control

GPIO52 internal pull Hi 8.2K to +3V
GPIO53 internal pull Hi 8.2K to +3V
GPIO54 internal pull Hi 8.2K to +3V
GPIO56 internal pull Hi 8.2K to +3V
GPIO57 internal pull Hi 8.2K to +3V
GPIO58 internal pull Hi 8.2K to +3V

TEMP(0 - 3)
Temp Monitor Not Implemented
10-KΩ 5% pull-up to +3VS5
or 10-KΩ 5% pull-down

VIN (0 - 7)
Voltage Monitor Not Implemented
10-KΩ 5% pull-up to +3VS5
or 10-KΩ 5% pull-down

ID4	ID3	ID2	ID1	ID0	CONFIG	31- Level BOM	Item
0	0	0	0	0	UMA		1
0	0	0	1	0			2
0	0	1	0	0			3
0	0	1	1	0			4
0	1	0	1	0			5
0	1	1	1	0			6
1	0	0	1	0			7
1	0	1	1	0			8
0	0	0	0	1	DIS		9
0	0	1	0	1			10
1	0	0	1	1			11
1	0	1	1	1			12

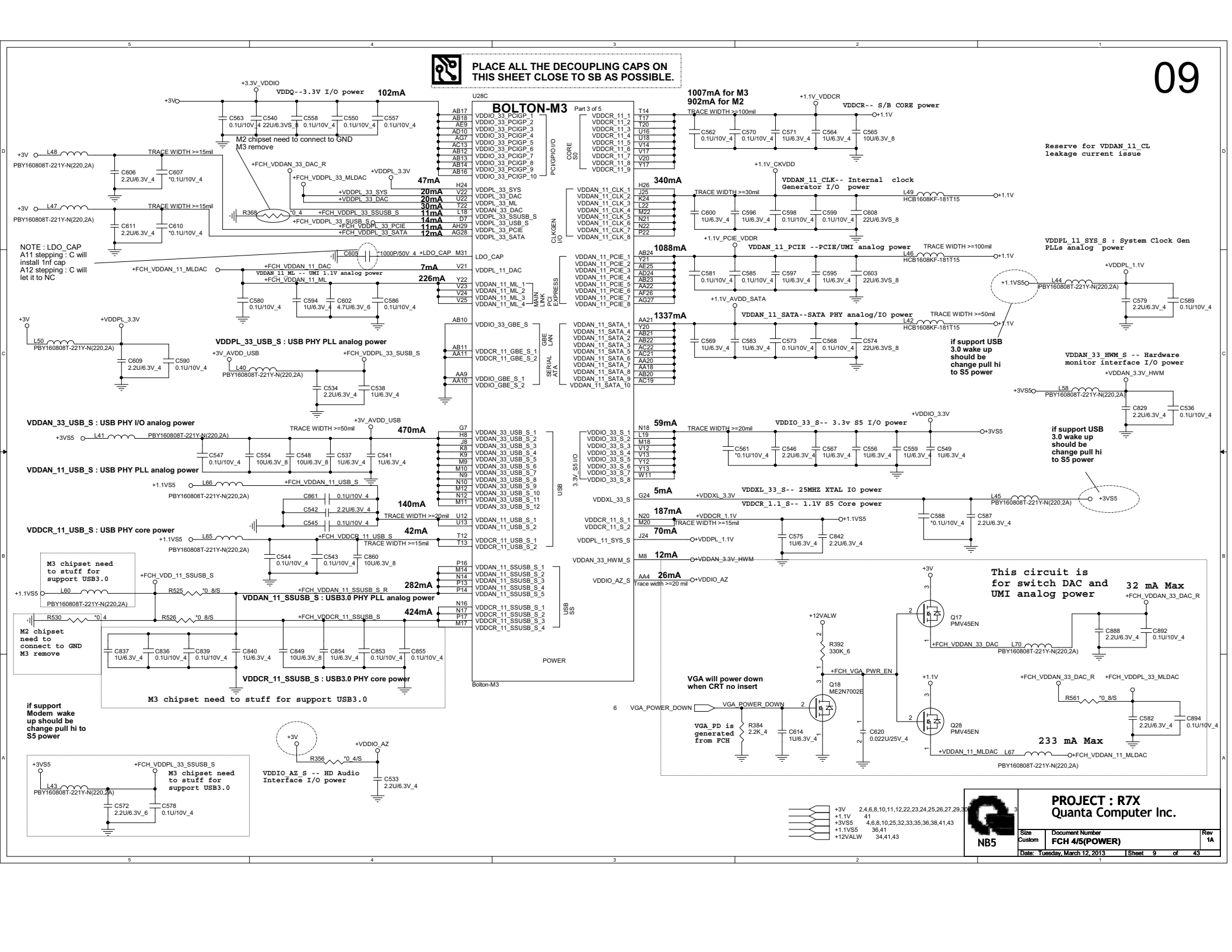
SIDE_PORT_ID2	SIDE_PORT_ID1	SIDE_PORT_ID0	
0	0	0	Samsung
0	0	1	Hynix
0	1	0	NC
0	1	1	no supprot side port

PROJECT : R7X
Quanta Computer Inc.

NB5

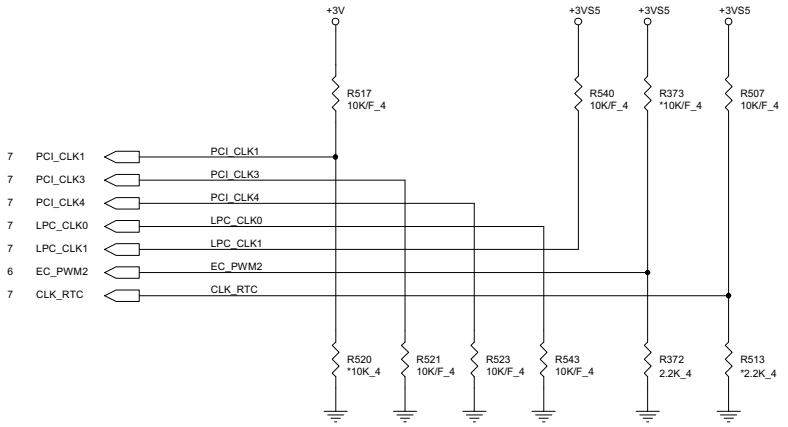
Size: Custom | Document Number: FCH 3/5(SATA/VGA/GND/SPI) | Rev: 1A

Date: Tuesday, March 12, 2013 | Sheet 8 of 43


09
PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.
BOLTON-M3
Part 3 of 5
U28C
VDDQ--3.3V I/O power
102mA
1007mA for M3
902mA for M2
VDDCR-- S/B CORE power
M2 chipset need to connect to GND
M3 remove
Reserve for VDDAN_11_CL leakage current issue
VDDAN_11_CLK-- Internal clock Generator I/O power
340mA
VDDAN_11_PCIE --PCIE/UMI analog power
1088mA
VDDPL_11_SYS_S : System Clock Gen PLLs analog power
VDDAN_11_SATA--SATA PHY analog/IO power
1337mA
if support USB 3.0 wake up should be change pull hi to S5 power
VDDAN_33_HWM_S -- Hardware monitor interface I/O power
VDDPL_33_USB_S : USB PHY PLL analog power
VDDIO_33_S-- 3.3v S5 I/O power
59mA
VDDXL_33_S-- 25MHZ XTAL IO power
5mA
VDDCR_1.1_S-- 1.1V S5 Core power
187mA
VDDAN_33_USB_S : USB PHY I/O analog power
470mA
VDDAN_11_USB_S : USB PHY PLL analog power
140mA
VDDCR_11_USB_S : USB PHY core power
42mA
70mA
12mA
26mA
M3 chipset need to stuff for support USB3.0
282mA
VDDAN_11_SSUSB_S : USB3.0 PHY PLL analog power
424mA
VDDCR_11_SSUSB_S : USB3.0 PHY core power
M3 chipset need to stuff for support USB3.0
if support Modem wake up should be change pull hi to S5 power
VDDIO_AZ_S -- HD Audio Interface I/O power
This circuit is for switch DAC and UMI analog power
32 mA Max
233 mA Max
VGA will power down when CRT no insert
VGA_PD is generated from FCH
PROJECT : R7X
Quanta Computer Inc.
NB5
FCH 4/5(POWER)
Size Custom
Rev 1A
Date: Tuesday, March 12, 2013
Sheet 9 of 43

STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



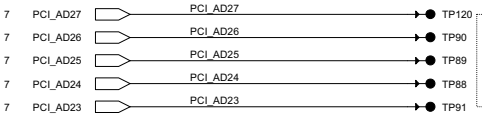
REQUIRED STRAPS

	--------	PCI_CLK1	--------	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	CLK_RTC
PULL HIGH	--------	ALLOW PCIE Gen2 DEFAULT	--------	USE DEBUG STRAP	non_Fusion CLOCK MODE	AMD internal EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	--------	FORCE PCIE Gen1	--------	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

DEBUG STRAPS

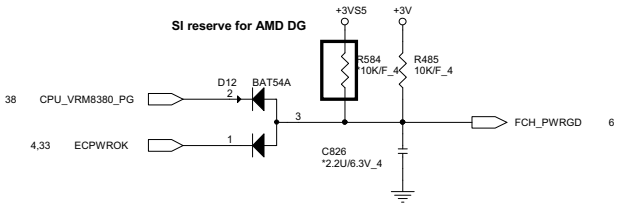
10

FCH has 15K Internal Pull Up for PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

FCH PWRGD

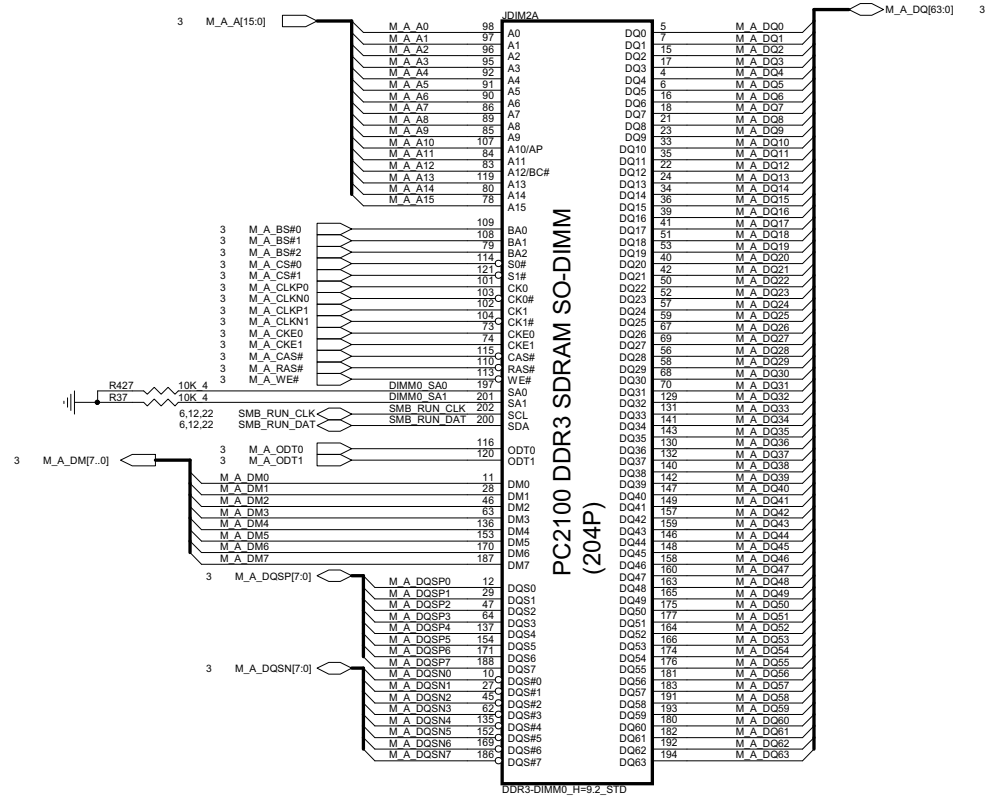


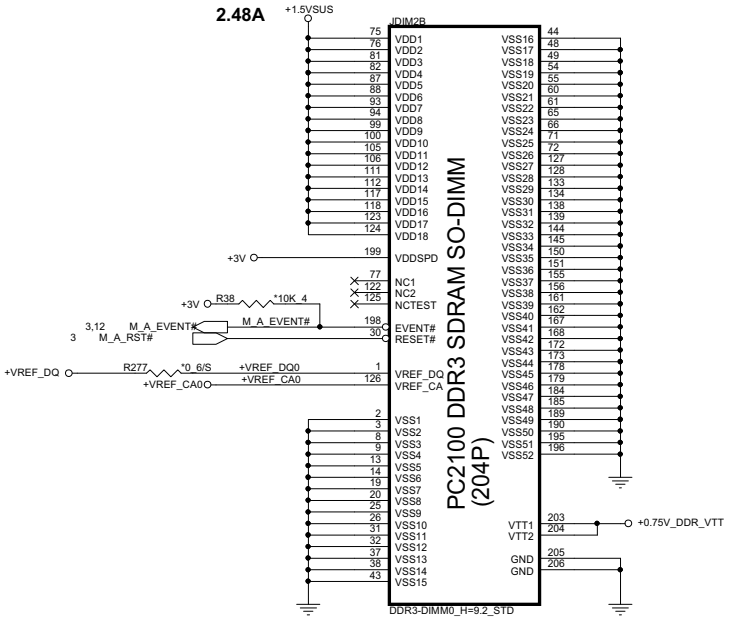
PROJECT : R7X
Quanta Computer Inc.

Size	Document Number	Rev
Custom	FCH 5/5(Strap &PWRGD)	1A

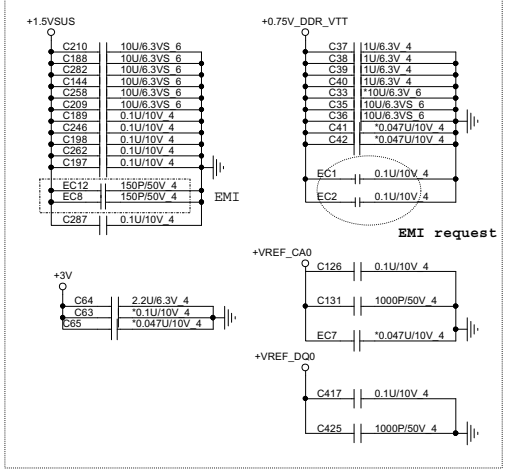
NB5

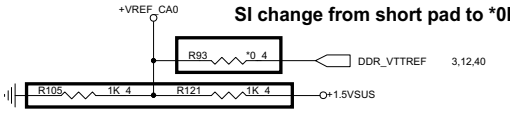
Date: Tuesday, March 12, 2013 Sheet 10 of 43





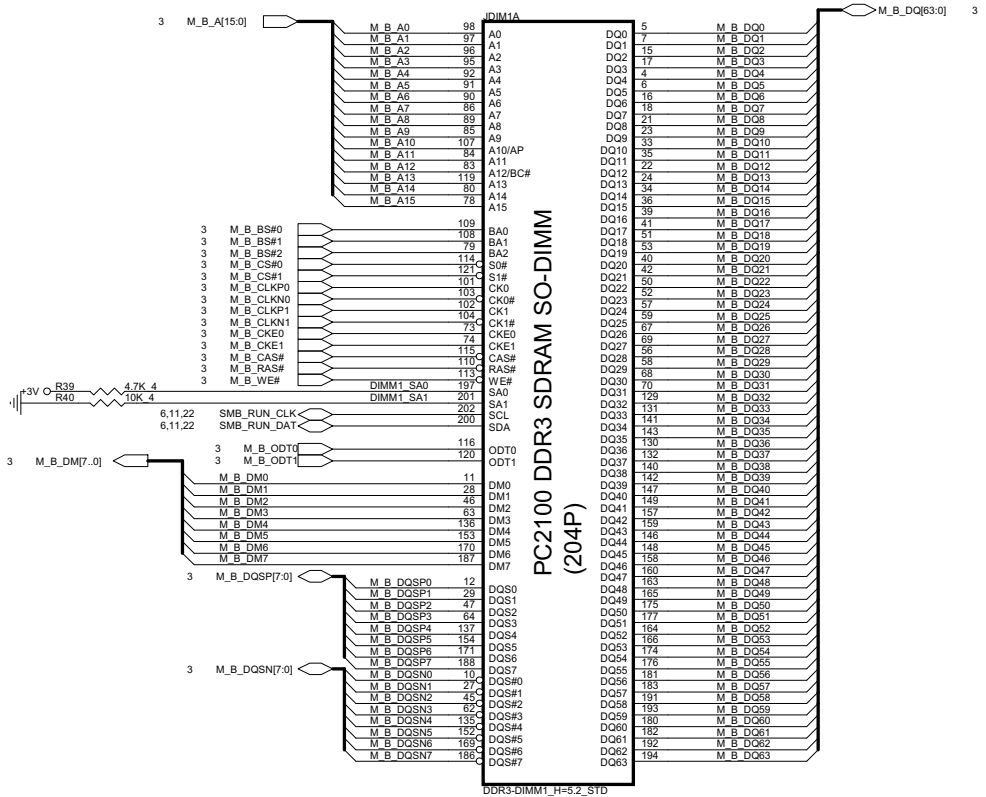
Place these Caps near So-Dimm0.

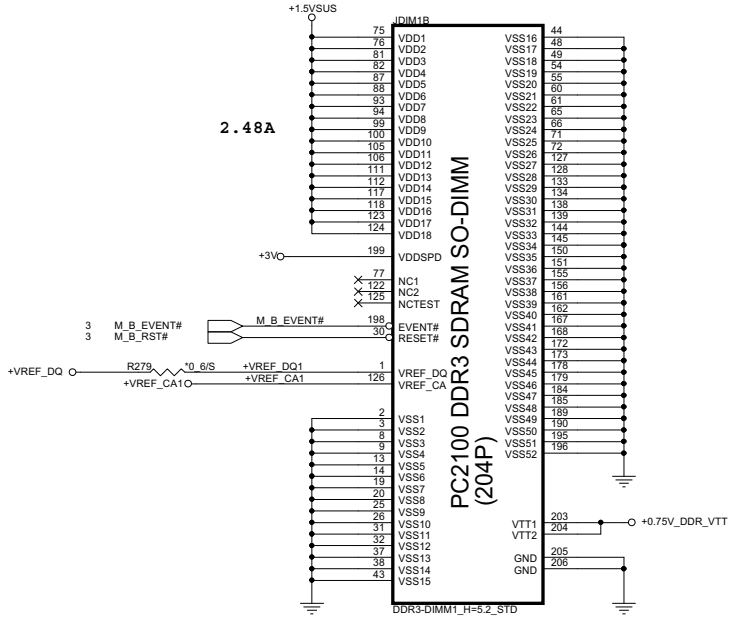


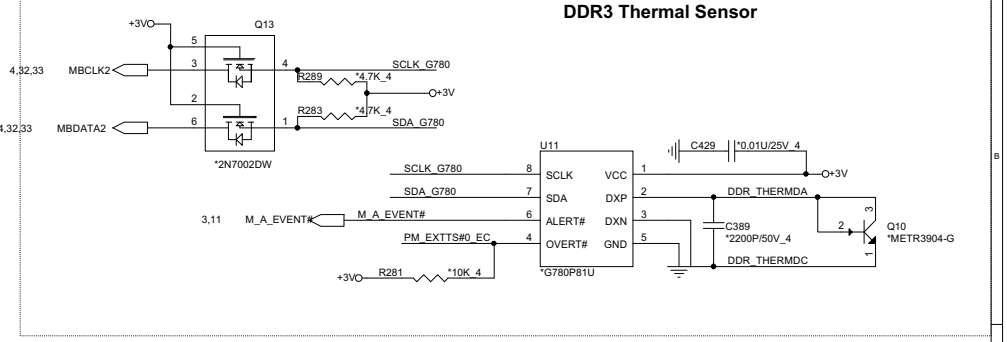


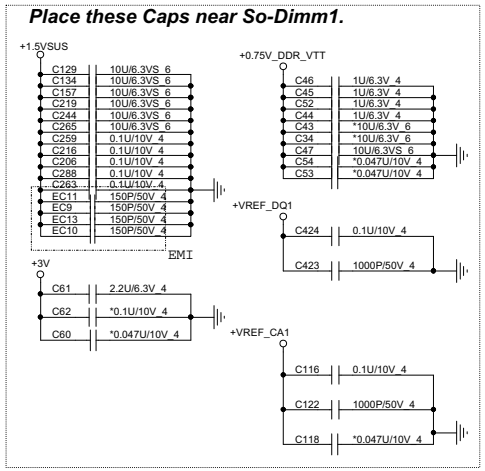
+3V 2,4,6,8,9,10,12,22,23,24,25,26,27,29,30,31,32,33,41,42,43
+1.5V 2,4,22,23,27,32,38,41
+3VPCU 7,25,30,32,33,34,35
+1.5VSUS 2,3,4,5,12,40,41,43
+0.75V_DDR_VTT 12,40

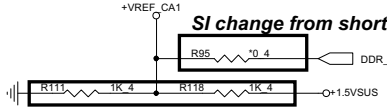
NB5	**PROJECT : R7X** Quanta Computer Inc.	
Size: Custom	Document Number: **DDR3 DIMM0-STD (9.2H)**	Rev: 1A
Date: Tuesday, March 12, 2013	Sheet 11 of 43	

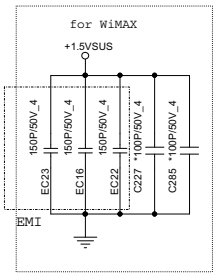


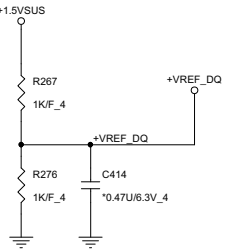












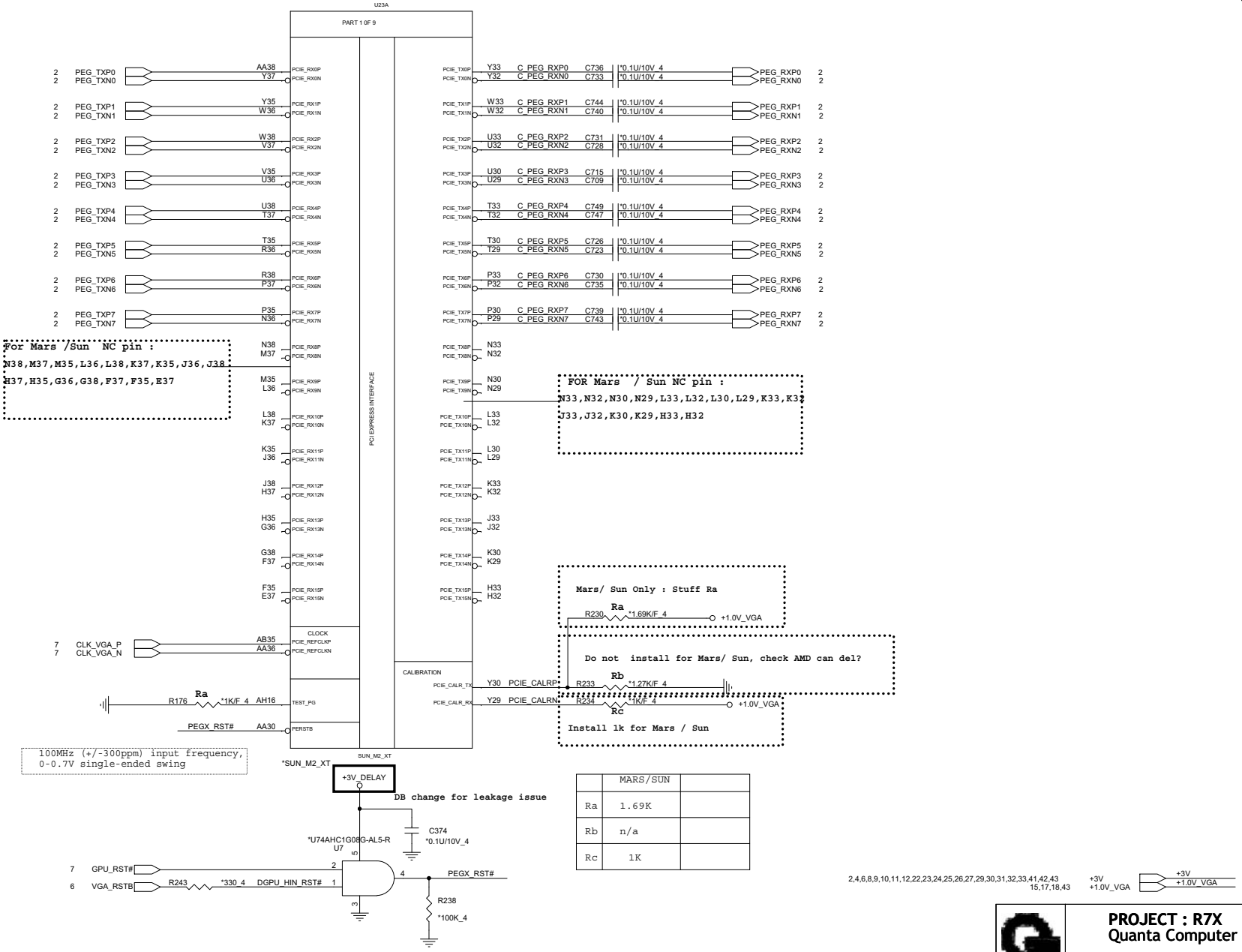
+0.75V_DDR_VTT 11,40
+1.5VSUS 2,3,4,5,11,40,41,43
+3VPCU 7,25,30,32,33,34,35
+3V 2,4,6,8,9,10,11,22,23,24,25,26,27,29,30,31,32,33,41,42,43

PROJECT : R7X
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	DDR3 DIMM1-STD (5.2H)	1A

Date: Tuesday, March 12, 2013 Sheet 12 of 43



	MARS/SUN	
Ra	1.69K	
Rb	n/a	
Rc	1K	

PROJECT : R7X
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	SUN_PCIE_Interface	1A

Date: Tuesday, March 12, 2013 Sheet 13 of 43

PS3 BIT3=>BIT1 [3:0]	Vendor		Vendor P/N	QCI P/N (TOP B/S)
011	Hynix	128Mx16 *4	H5TC2G63FFR-11C	AKD5MZDTW02
100	Micron	128Mx16 *4	MT41J128M16JT-093G:K	AKD5MGSTL16
101	Samsung	128Mx16 *4	K4W2G1646E-BC1A	AKD5MGGT534
Only for Test				
PS3 BIT3=>BIT1 [3:0]	Vendor		Vendor P/N	QCI P/N
000	Hynix	256Mx16 *4	H5TC4G63AFR-11C	AKD5PGWTW07
001	Micron	256Mx16 *4	MT41J256M16HA-093G:E	AKD5PZSTL00
010	Samsung	256Mx16 *4	K4W4G1646B-HC1A	AKD5PZDT500

Samsung 2GB VRAM	AKD5MGGT535	K4W2G1646E-BC1A
Samsung 4GB VRAM	AKD5PZDT501	K4W4G1646B-HC1A
Hynix 2GB VRAM	AKD5MZDTW03	H5TC2G63FFR-11C
Hynix 4GB VRAM	AKD5PGWTW08	H5TC4G63AFR-11C
Micron 2G VRAM	AKD5MGSTL17	MT41J128M16JT-093G:K
Micron 4G VRAM	AKD5PZSTL01	MT41J256M16HA-093G:E

For Mars / Sun : AR1/AW8/AR3/AR8/AU8: NC pin

For Sun only : AD29 /AC29 /AJ21 /AK21: NC pin

For Mars / Sun : DP A to D Port: all NC pin

For Sun only :
AP10 /AV11 /AT11 /AR12 /AW12 / AU12 /AP12 : NC pin

SI stuff

Access to SMBBus ans SDA/SCL is mandatory on all designs
Add test points on SMBBus and SDA/SCL for debug

PV change to shortpad

SI add TEMP FAIL circuit for SUN XT

FOR SUN GPIO NC PIN : AJ19/ AK19 / AK24 / AM14 / AN14 / AJ24/ AH26 / AH24 / AJ20
AK20/ AH18 / AN16 / AK17 / AK16 / AL16/ AM16

Mars: stuff
For Sun Nc: R140, R124, C148

Thermal Solution(Close to GPU)
Main:AL000781039 G781-1P8(9Ah)
2nd:AL001412005 EMC1412-2-ACZL-TR(9Ah)

Reserve for Power Play

For Mars: Stuff Ra, Rc=> VDDC 1.1V
For Thems: Stuff Ra, Rb, Na Rc=> VDDC 1.0V

FOR MARS: AD37/ AE38 / AD35 AVSSN to GND
FOR SUN : AD37/ AE38 / AD35 NC pin
FOR SUN : R222/R224/R225 -->NC

FOR SUN : R226/R216/R448/R184/R219 -->NC
FOR SUN NC PIN : AD34/ AE34 / AC33 / AC34 / AD39 / AE36
AF37/ AC36 / AC38 / AB34 /

For Mars / Sun:NC pin
AL30, AM30, AL29, AM29, AN21, AM21, AK30, AK29

For Sun Only :NC pin
AL27, AM27, AM20, AN20, AN26, AM26, AL19, ,
AM19, AJ30, AJ31

MLPS Implementation
- Connect GPIO_28 to 10K pulldown to enable MLPS
- If any of PS_0/1/2/3 is not used, leave "no connect"
- R_pu, R_pd and C must be properly populated per tables below
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Total DC resistance of trace between C and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance

Capacitor Lookup Table

C (nF)	Bits(5,4)
680	00
82	01
10	10
NC	11

Resistor Divider Lookup Table:

R_pu (Ohm)	R_pd (Ohm)	Bits(3,2,1)
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

PS_0[3:1]	romiddfg[2:0]	Memory aperture size or ROM type select: If bios_rom_en = 0, romiddfg[2:0] define memory aperture size If bios_rom_en = 1, romiddfg[2:0] define ROM type	xxx	gpio_13 gpio_12 gpio_11
PS_0[4]	n/a	Reserved	1	genlk_vsync
PS_1[1]	bif_gen3_en_a	PCIe Gen3 capability: 1=Gen3 supported, 0=Gen3 not supported	x	gpio_2
PS_1[2]	bif_clk_pm_en	PCIe Clk PM capability: 1 = CLKREQB supported	x	gpio_8
PS_1[3]	n/a	Reserved		genlk_clk
PS_1[4]	tx_pwrs_enb	PCIe Tx power savings: 0=50% swing, 1=full swing	x	gpio_0
PS_1[5]	tx_deemph_en	PCIe Tx de-emphasis: 1=Tx de-emphasis enabled	x	gpio_1
PS_2[1]	n/a	Reserved		n/a
PS_2[2]	n/a	Reserved		n/a
PS_2[3]	bios_rom_en	Enable external BIOS ROM: 1=External ROM connected	x	gpio_22
PS_2[4]	vga_dis	VGA disable: 1=Disable this GPU as the system's VGA controller	0	gpio_9
PS_2[5]	n/a	Reserved		n/a
PS_3[1]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[2]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[3]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[5] PS_3[4] PS_0[5]	aud_port_cp[2] aud_port_cp[1] aud_port_cp[0]	3-bit field indicating number of audio-capable display outputs	xxx	n/a

BIT5 => BIT1

PS0	=>	11001
PS1	=>	11001
PS2	=>	00000
PS3	=>	11011

DB no stuff

PS3 BIT3=>BIT1	ID	Memory Type	Configuration	Row x Col x Bank bits	Channel Size
000	0				
001	1				
010	2				
011	3				
100	4				
101	5				

13,15,17,18,43 +1.0V_VGA +1.0V_VGA
15,17,18,25,43 +1.8V_VGA +1.8V_VGA
13,16,17 +3V_DELAY +3V_DELAY

NB5

PROJECT : R7X
Quanta Computer Inc.

Size: Custom | Document Number: SUN_Main & GND | Rev: 1A
Date: Tuesday, March 12, 2013 | Sheet 14 of 43

For Mars/ Sun
Change La, Lb
Bead to 0 ohm

La

+1.8V_VGA — L25 *0_6/S — +1.8V_DPLL_PVDD

Display Phase Lock Loop Power
DPLL_PVDD : 1.8V @ 75mA

C273 *10U/6.3V_8 | C277 *1U/6.3V_4 | C278 *0.1U/10V_4

PV change to shortpad

Lb

+1.0V_VGA — L24 *0_6/S — +1.0V_DPLL_VDDC

DPLL_VDDC : 0.935V @ 140mA

1.0V(125mA DPLL_VDDC)

C267 *10U/6.3V_8 | C280 *1U/6.3V_4 | C279 *0.1U/10V_4

+1.0V_DPLL_VDDC

DPLL_PVSS

+1.8V_MPLL_PVDD

MPLL_PVDD : 1.8V @ 150mA

+1.8V_VGA — *HCB1608KF-471T10 L36 — +1.8V_MPLL_PVDD

C449 *10U/6.3V_8 | C446 *1U/6.3V_4 | C447 *0.1U/10V_4

+1.8V_SPLL_PVDD

SPLL_PVDD : 1.8V @ 75mA

+1.8V_VGA — L19 *TB160808U121N005(120 0.4A) — +1.8V_SPLL_PVDD

C160 *10U/6.3V_8 | C172 *1U/6.3V_4 | C190 *0.1U/10V_4

+1.0V_SPLL_VDDC

SPLL_VDDC : 0.935V @ 150mA

+1.0V_VGA — L22 *HCB1608KF-471T10 — +1.0V_SPLL_VDDC

1.0V(125mA DPLL_VDDC)

C178 *10U/6.3V_8 | C242 *1U/6.3V_4 | C232 *0.1U/10V_4

SPLL_PVSS

+1.8V_DPLL_PVDD — R188 Ra *0_4 — R192 Rb *0_4

reserve Ra, Rb for future ASIC

Memory Type	
DDR3	27-MHz (± 30 ppm) crystal connected to XTALIN/XTALOUT, or 27-MHz (1.8 V) oscillator connected to XTALIN.
GDDR5	27-MHz (3.3 V) oscillator connected to XO_IN, and 100-MHz (3.3 V) oscillator connected to XO_IN2. (By default, this clock should not be spread since internal spreading is used.)

U23I — PART 9 OF 9 — PLLS/XTAL — SUN_M2_XT

AM32 DPLL_PVDD
AN31 DPLL_VDDC
AN32 DPLL_PVSS
H7 MPLL_PVDD
H8 MPLL_PVDD
AM10 SPLL_PVDD
AN9 SPLL_VDDC
AN10 SPLL_PVSS
AF30 NC_XTAL_PVDD
AF31 NC_XTAL_PVSS

DB change from X0_IN for AMD suggestion

R443 *0_4 — GPU_XTAL27_IN — 25

XTALIN AV33 EVGA-XTALI — *22P/50V_4 C250

R181 *10M — Y2 *7A27000010

XTALOUT AU34 EVGA-XTALO — *22P/50V_4 C251

XO_IN AW34 — DP55

DB change to XTAI_IN for AMD suggestion

XO_IN2 AW35 — R446 *0_4

CLKTESTA AK10 CLKTESTA
CLKTESTB AL10 CLKTESTB

C192 *0.1U/10V_4 | C248 *0.1U/10V_4

Debug only,
for clock observation,
if not needed, DNI

R145 *51.1/F_4 | R163 51.1/F_4

route 50ohms
single-ended/
100ohms diff and keep short

U23F — PART 6 OF 9 — SUN_M2_XT

AB39	PCIE_VSS	GND	A3
E39	PCIE_VSS	GND	A37
F34	PCIE_VSS	GND	AA16
F39	PCIE_VSS	GND	AA18
G33	PCIE_VSS	GND	AA2
G34	PCIE_VSS	GND	AA21
H31	PCIE_VSS	GND	AA23
H34	PCIE_VSS	GND	AA26
H39	PCIE_VSS	GND	AA28
J31	PCIE_VSS	GND	AA6
J34	PCIE_VSS	GND	AB12
K31	PCIE_VSS	GND	AB15
K34	PCIE_VSS	GND	AB17
K39	PCIE_VSS	GND	AB20
L31	PCIE_VSS	GND	AB22
L34	PCIE_VSS	GND	AB24
M34	PCIE_VSS	GND	AB27
M39	PCIE_VSS	GND	AC11
N31	PCIE_VSS	GND	AC13
N34	PCIE_VSS	GND	AC16
P31	PCIE_VSS	GND	AC18
P34	PCIE_VSS	GND	AC2
P39	PCIE_VSS	GND	AC21
R34	PCIE_VSS	GND	AC23
T31	PCIE_VSS	GND	AC26
T34	PCIE_VSS	GND	AC28
T39	PCIE_VSS	GND	AC5
U31	PCIE_VSS	GND	AD15
U34	PCIE_VSS	GND	AD17
V34	PCIE_VSS	GND	AD20
V39	PCIE_VSS	GND	AD22
W31	PCIE_VSS	GND	AD24
W34	PCIE_VSS	GND	AD27
Y34	PCIE_VSS	GND	AD9
Y39	PCIE_VSS	GND	AE2
		GND	AE6
		GND	AF10
		GND	AF16
		GND	AF18
		GND	AF21
		GND	AG17
		GND	AG2
		GND	AG20
		GND	AG22
		GND	AG6
F15	GND	GND	AG9
F17	GND	GND	AH21
F19	GND	GND	AJ10
F21	GND	GND	AJ11
F23	GND	GND	AJ2
F25	GND	GND	AJ28
F27	GND	GND	AJ6
F29	GND	GND	AK11
F31	GND	GND	AK31
F33	GND	GND	AK7
F7	GND	GND	AL11
F9	GND	GND	AL14
G2	GND	GND	AL17
G6	GND	GND	AL2
H9	GND	GND	AL20
J2	GND		
J27	GND	GND	AL23
J6	GND	GND	AL26
J8	GND	GND	AL32
K14	GND	GND	AL6
K7	GND	GND	AL8
L11	GND	GND	AM11
L17	GND	GND	AM31
L2	GND	GND	AM9
L22	GND	GND	AN11
L24	GND	GND	AN2
L6	GND	GND	AN30
M17	GND	GND	AN6
M22	GND	GND	AN8
M24	GND	GND	AP11
N16	GND	GND	AP7
N18	GND	GND	AP9
N2	GND	GND	AR5
N21	GND	GND	B11
N23	GND	GND	B13
N26	GND	GND	B15
N6	GND	GND	B17
R15	GND	GND	B19
R17	GND	GND	B21
R2	GND	GND	B23
R20	GND	GND	B25
R22	GND	GND	B27
R24	GND	GND	B29
R27	GND	GND	B31
R6	GND	GND	B33
T11	GND	GND	B7
T13	GND	GND	B9
T16	GND	GND	C1
T18	GND	GND	C39
T21	GND	GND	E35
T23	GND	GND	E5
T26	GND	GND	F11
U15	GND	GND	F13
U17	GND		
U2	GND		
U20	GND		
U22	GND		
U24	GND		
U27	GND		
U6	GND		
V11	GND		
V16	GND		
V18	GND		
V21	GND		
V23	GND		
V26	GND		
W2	GND		
W6	GND		
Y15	GND		
Y17	GND		
Y20	GND		
Y22	GND	VSS_MECH	A39
Y24	GND	VSS_MECH	AW1
Y27	GND	VSS_MECH	AW39

Mars/Sun AG22 is nc pin

13,17,18,43 +1.0V_VGA → +1.0V_VGA

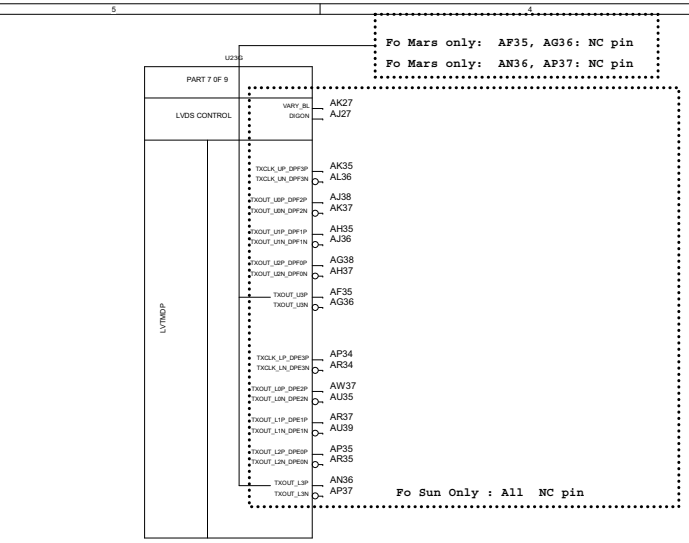
14,17,18,25,43 +1.8V_VGA → +1.8V_VGA

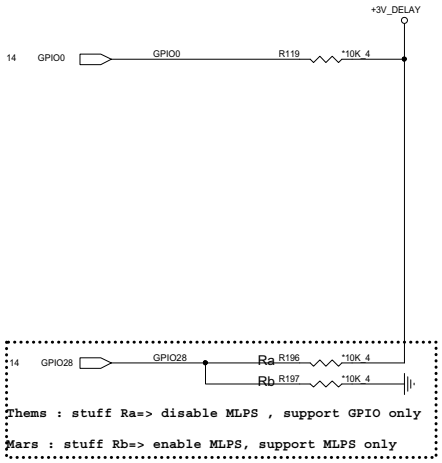
PROJECT : R7X
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	SUN_XTAL	1A

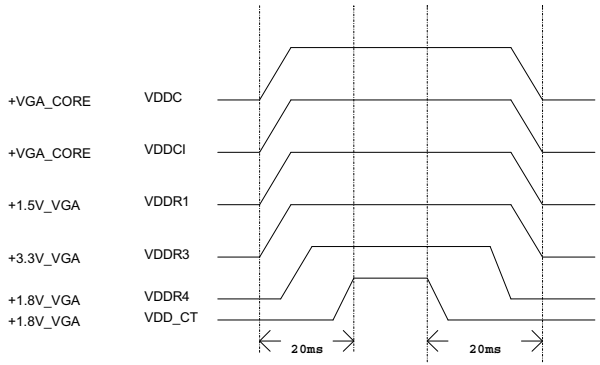
Date: Tuesday, March 12, 2013 Sheet 15 of 43





CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET				
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	0
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	1
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIE Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	1
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIE Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	001
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	0
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled, It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled Reserve for future ASIC	1
			NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOS ARE USEED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET	
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	GENLK_CLK GPIO8 GPIO21 GENERICC	Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	111

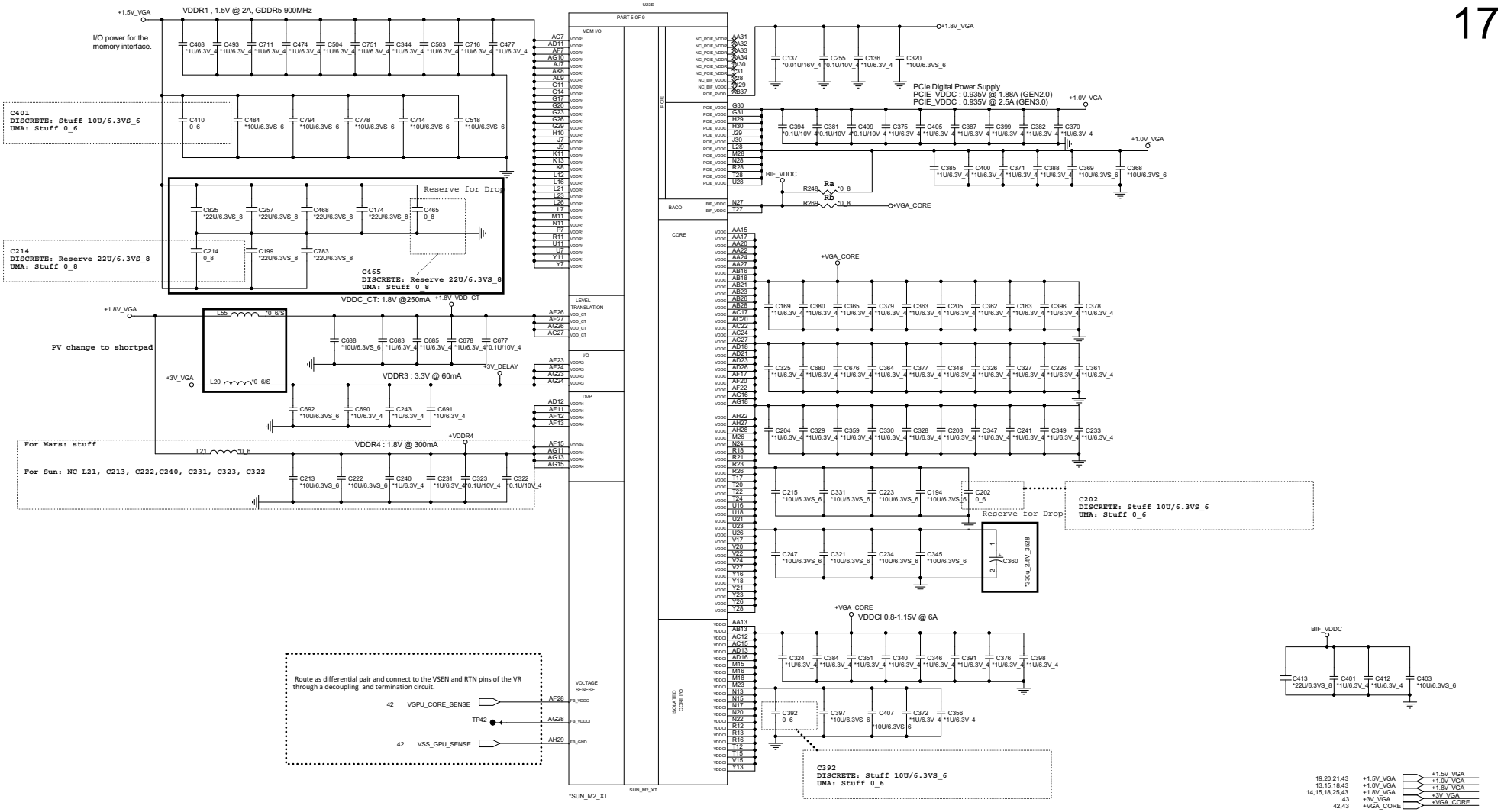
Power Up/Down Sequence



NB5

PROJECT : R7X
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SUN_LVDS / STRAP	1A
Date: Tuesday, March 12, 2013	Sheet 16 of 43	



Support BACO Mode

Notel. 1. No BACO Support :BIF_VDDC shorts with VDDC (Install Ra)

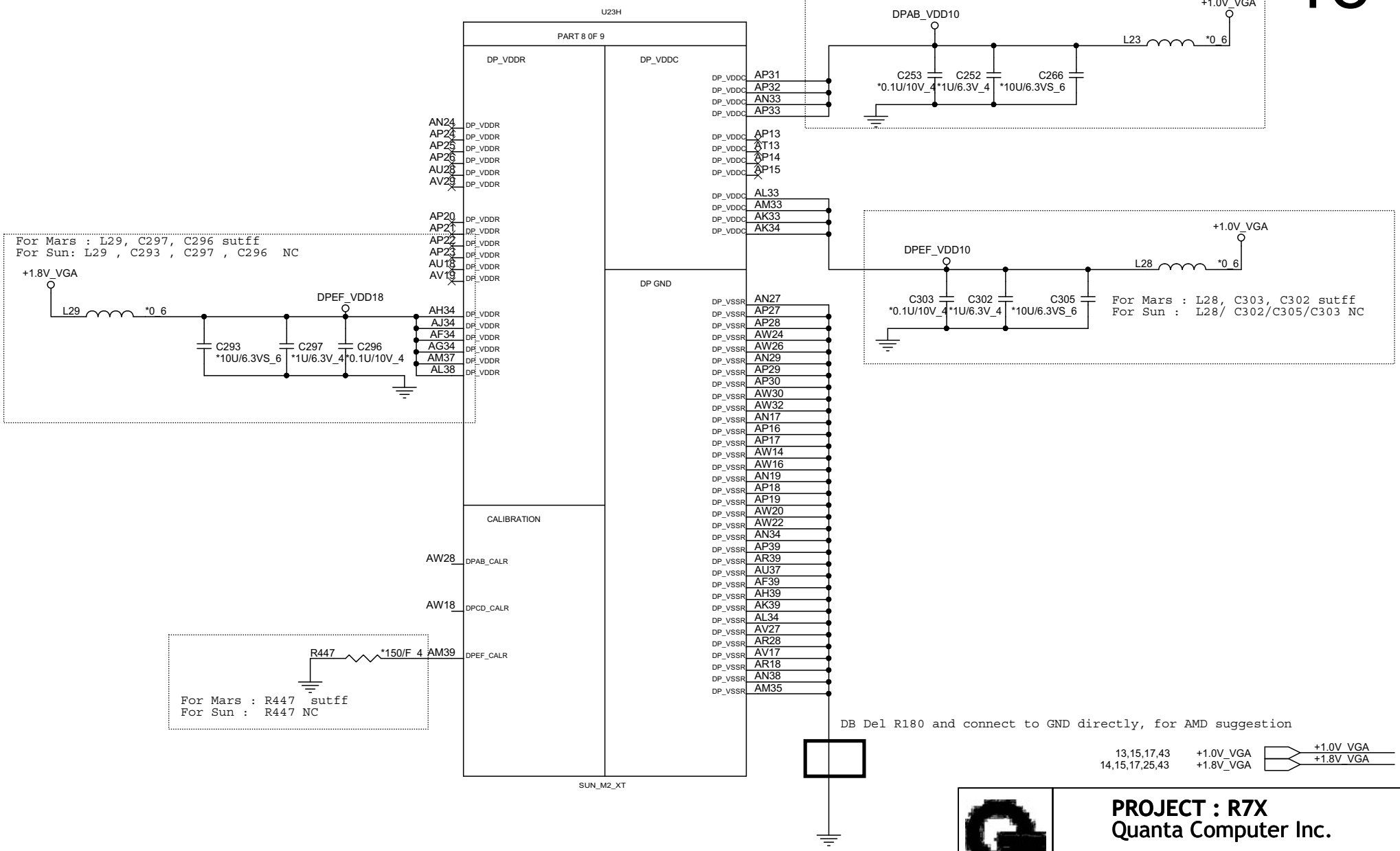
2. BACO Support: Refer to the BACO reference schematics/Application note for detail about BIF_VDDC Rail if BACO is Supported (Uninstall Ra)

PX_EN = 0, for Normal Operation
PX_EN = 1, for BACO MODE

	PROJECT : R7X	
NB5	Quanta Computer Inc.	
Size: Custom	Document Number: SUN_Power & BACO	Rev: 1A
Date: Tuesday, March 12, 2013	Sheet 17 of 43	

For Mars : L23, C253, C252 sutff

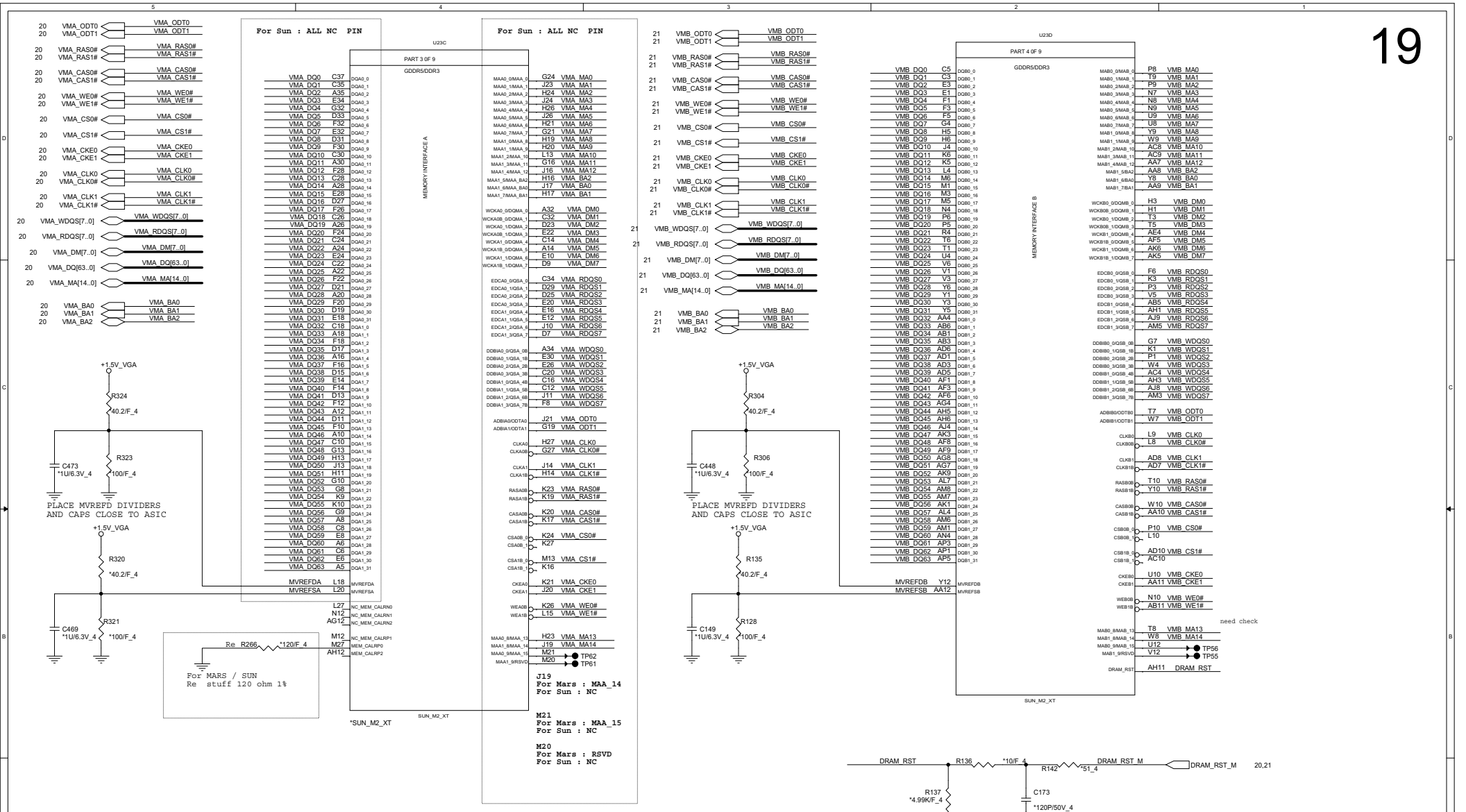
For Sun: L23 , C247 , C266 , C252 NC



PROJECT : R7X
Quanta Computer Inc.

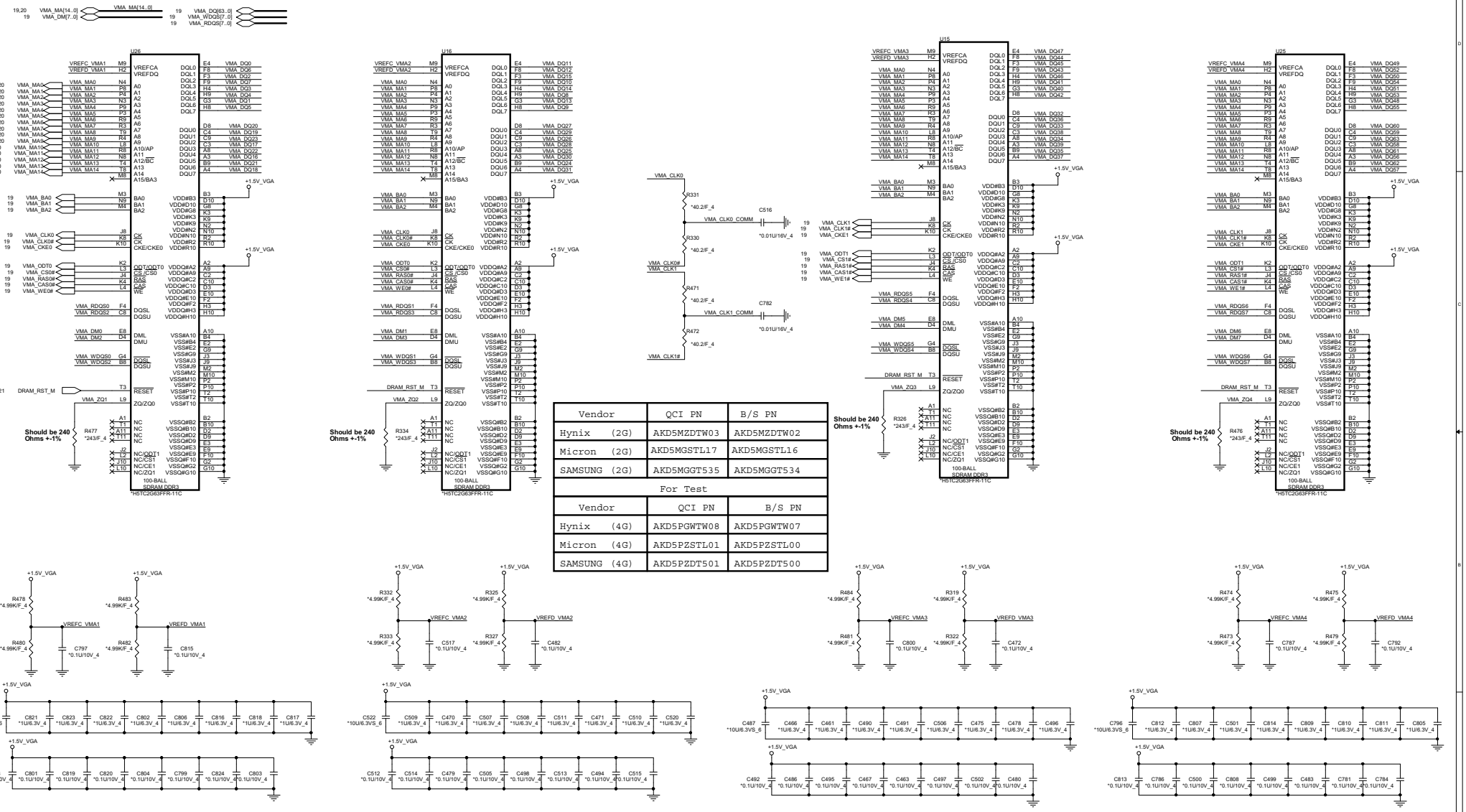
NB5

Size	Document Number	Rev
Custom	SUN_DP Powers	1A
Date: Tuesday, March 12, 2013	Sheet 18 of 43	



PROJECT : R7X	Quanta Computer Inc.
NB5	Size: Custom; Document Number: SUN_MEM_Interface; Rev: 1A
Date: Tuesday, March 12, 2013	Sheet 19 of 43

CHANNEL A: 256MB/512MB DDR3

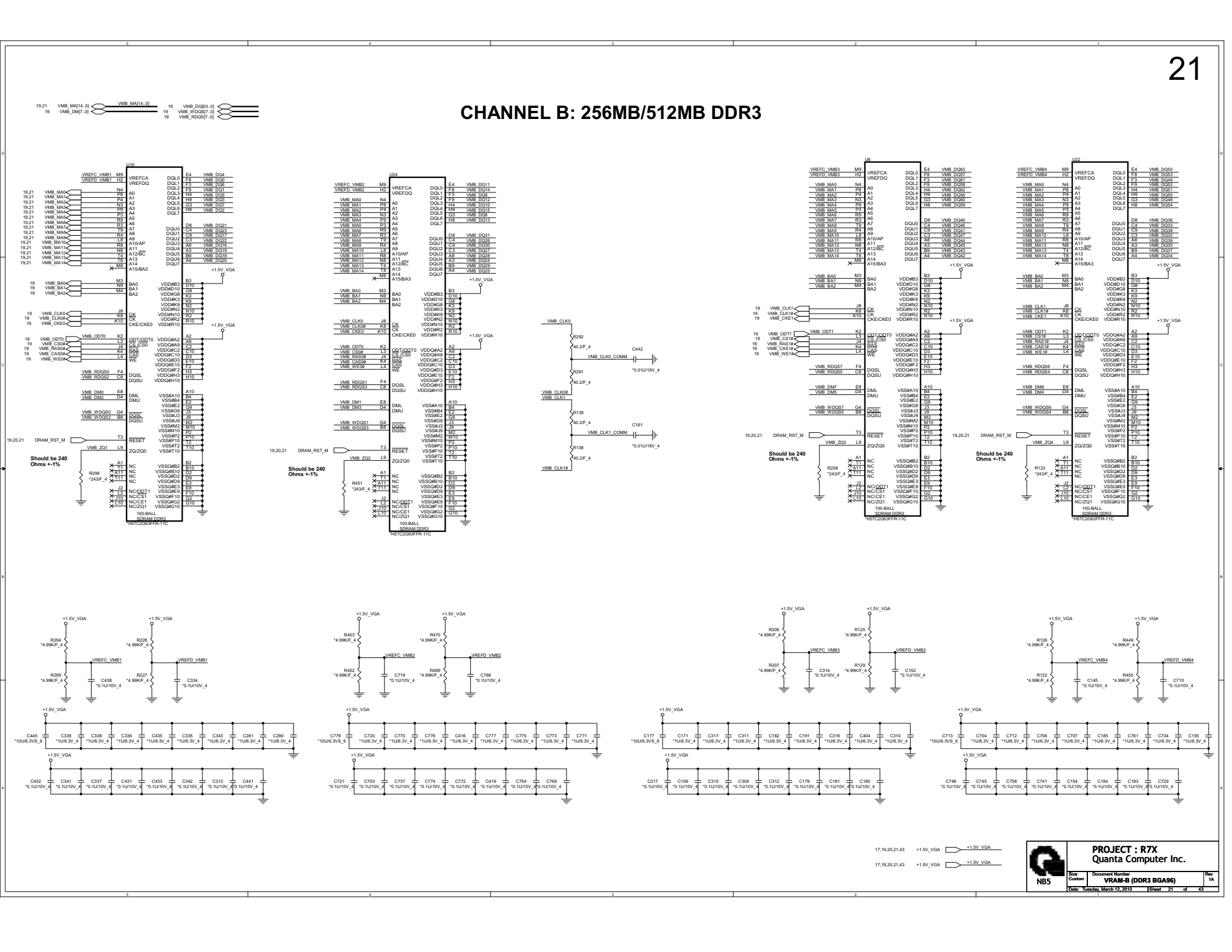


Vendor	QCI PN	B/S PN
Hynix (2G)	AKD5MZDTW03	AKD5MZDTW02
Micron (2G)	AKD5MGSTL17	AKD5MGSTL16
SAMSUNG (2G)	AKD5MGGT535	AKD5MGGT534
For Test		
Vendor	QCI PN	B/S PN
Hynix (4G)	AKD5PGWTW08	AKD5PGWTW07
Micron (4G)	AKD5PZSTL01	AKD5PZSTL00
SAMSUNG (4G)	AKD5PZDT501	AKD5PZDT500

17,19,21,43 +1.5V_VGA +1.5V_VGA

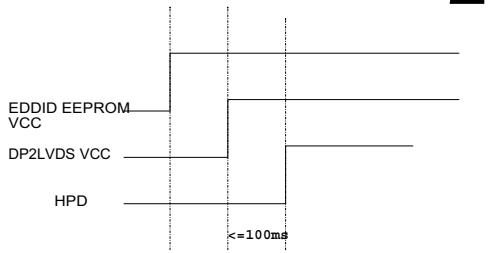
NB5	PROJECT : R7X Quanta Computer Inc.
Size: Custom	Document Number: VRAM-A (DDR3 BGA96) Rev: 3A
Date: Tuesday, March 12, 2013	Sheet 20 of 43

CHANNEL B: 256MB/512MB DDR3



PROJECT : R7X	
Quanta Computer Inc.	
NB5	Size: Custom; Document Number: VRAM-B (DDR3 BGA96); Rev: 1A
Date: Tuesday, March 12, 2013	Sheet 21 of 43

RTD2136S Power Up Sequence



RTD2136 Dual Channel only

Pine 18: keep 80 Mile Trace

Pine 20: keep 80 Mile Trace

IC底部需接GND VIA*9

RTD2136R

EC

SMBUS

PV change to shortpad

DB change from SMB_PCH_CLK/DAT to SMB_RUN_CLK/DAT

Use 1% Res on R5553

RTD2136R combined level shift already

Reserve

*M24C02
Should be using M24C64

L69: need use CV-4709MN00 for Vendor suggestion

RTD2136R
R107;R114: NA
R106;R115: Stuff

SWR: Stuff L5066
LDO: Stuff R9098

keep 80 Mile Trace

CLOSE TO Pin22

Close to Pin18
C2142 close to IC side

Close to Pin5

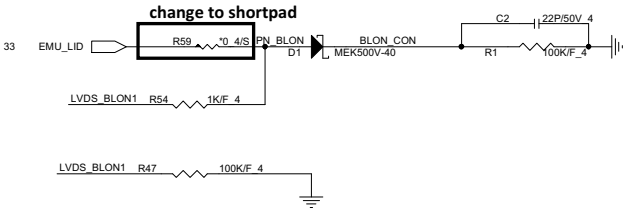
Close to Pin11

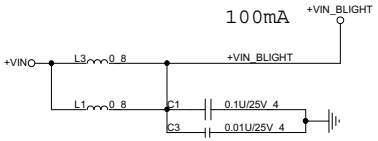
Close to Pin17

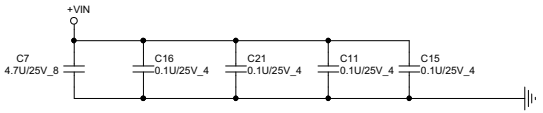
Close to Pin43

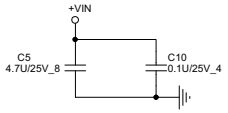
NB5	PROJECT : R7X Quanta Computer Inc.		
Size: Custom	Document Number: LVDS converter RTD2136	Rev: 1A	
Date: Tuesday, March 12, 2013	Sheet 22 of 43		

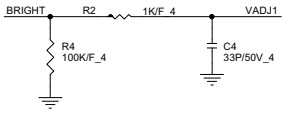
LID Switch

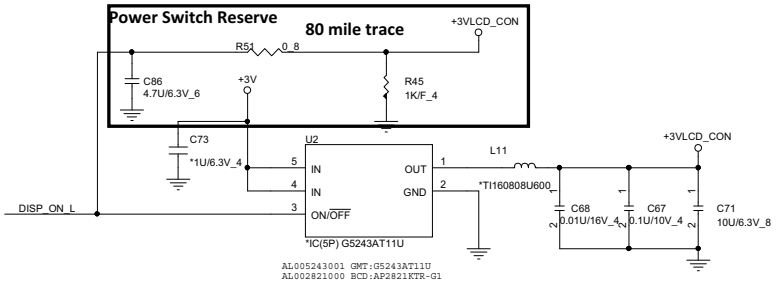


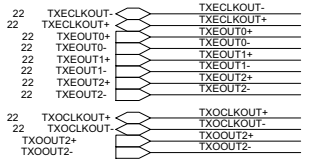


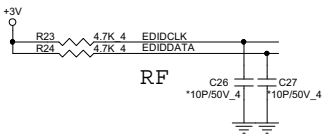


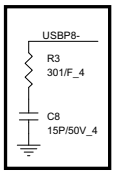


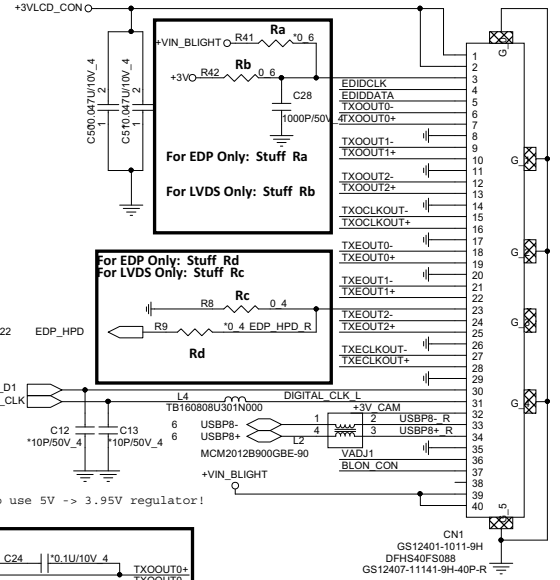


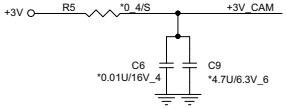




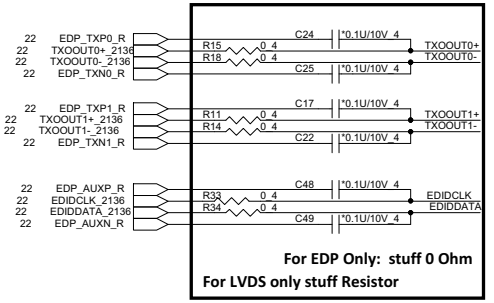


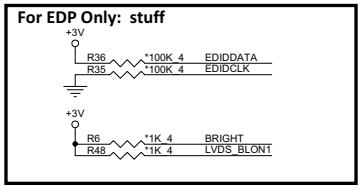


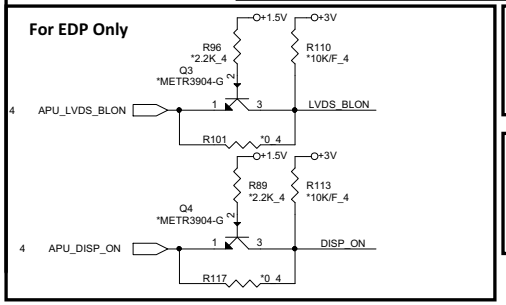


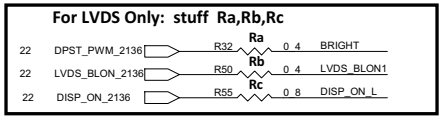


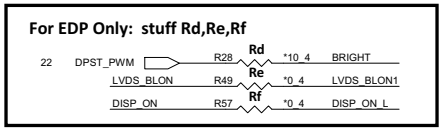
Please note that 2011 camera is +3V a We do not need to use 5V -> 3.95V regulator!

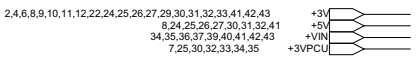








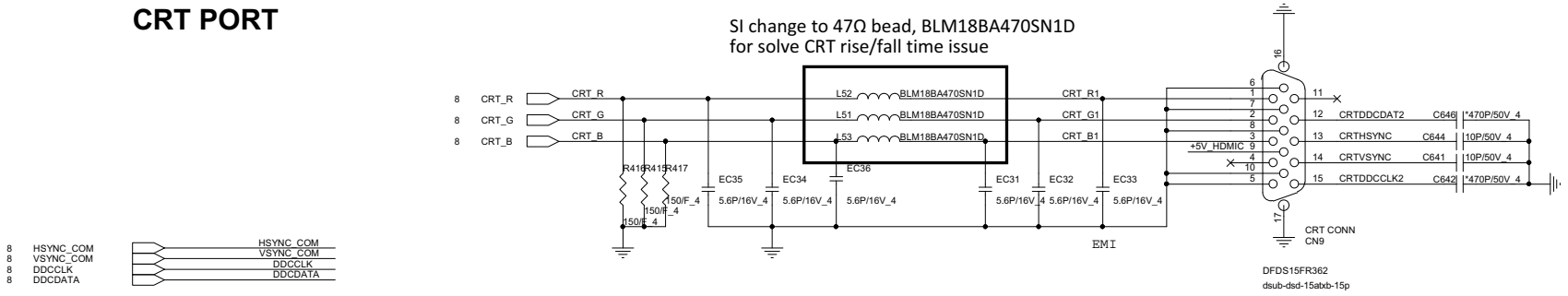


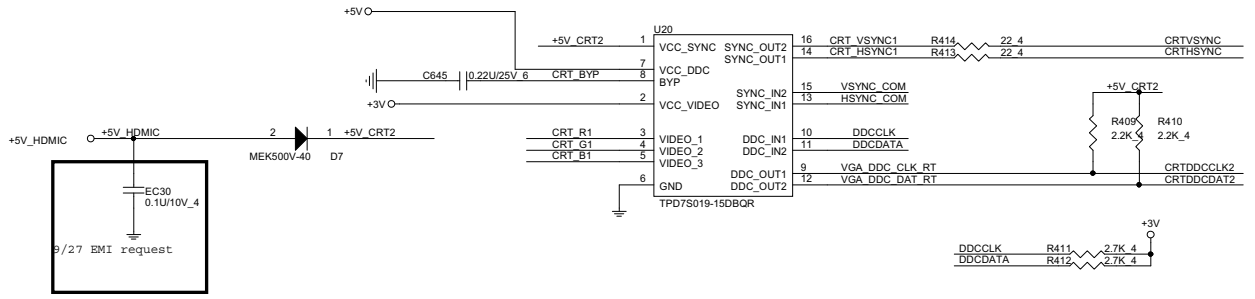


NB5	PROJECT : R7X Quanta Computer Inc.	
Size: Custom	Document Number: LCD CONN/LID/CAM	Rev: 1A
Date: Tuesday, March 12, 2013	Sheet 23 of 43	

CRT PORT

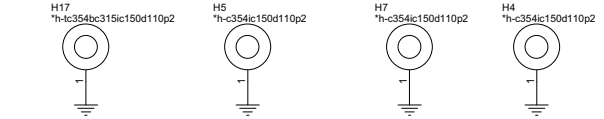
SI change to 47Ω bead, BLM18BA470SN1D
for solve CRT rise/fall time issue

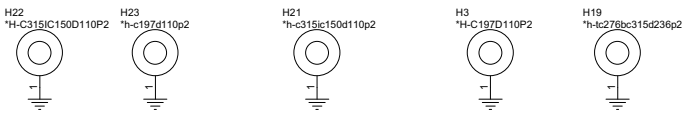


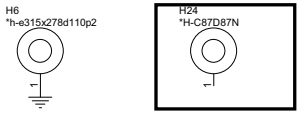


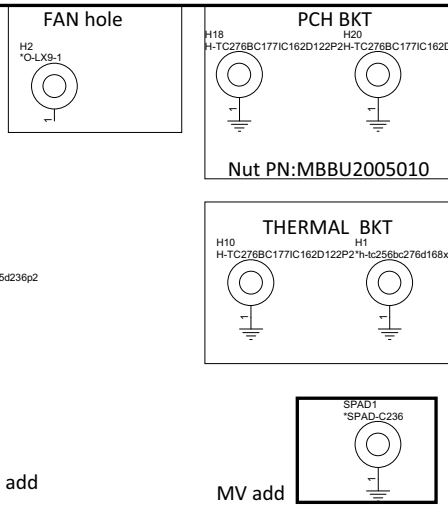
HOLE

HOLE









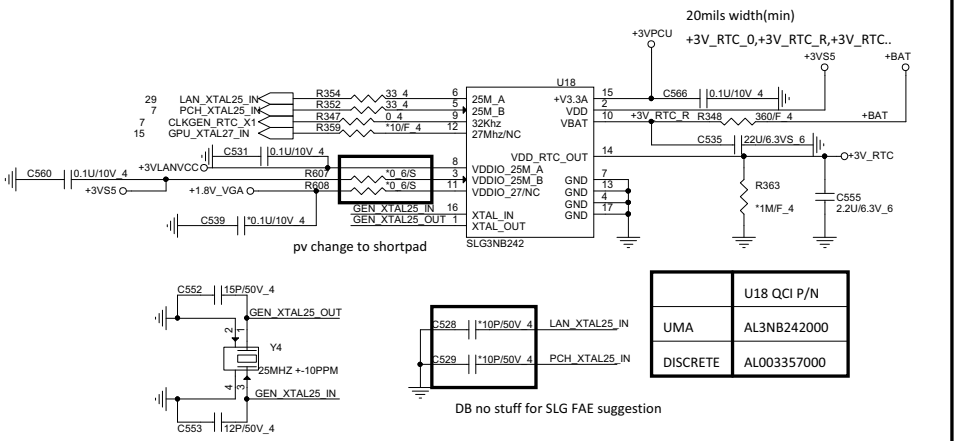
NB5

PROJECT : R7X
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT,Hole	1A

Date: Tuesday, March 12, 2013 Sheet 24 of 43

Green CLK Circuitry



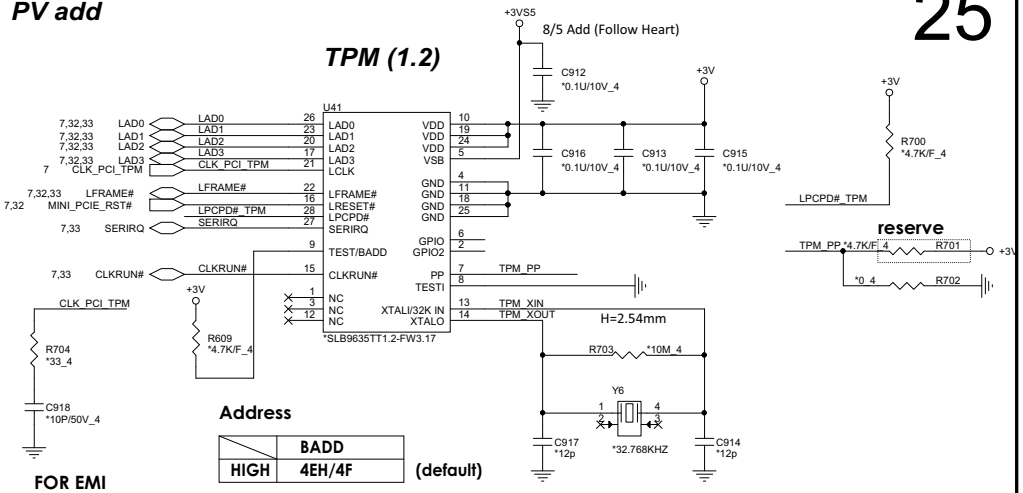
	U18 QCI P/N
UMA	AL3NB242000
DISCRETE	AL003357000

PV add

25

8/5 Add (Follow Heart)

TPM (1.2)



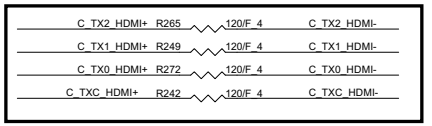
Address

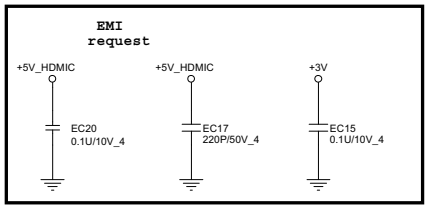
	BADD
HIGH	4EH/4F

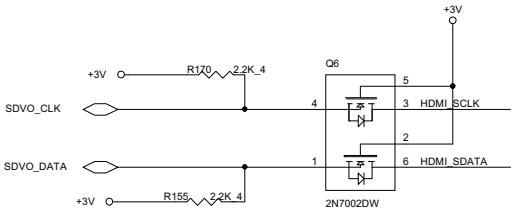
(default)

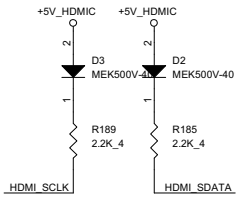
DISCRETE HDMI I2C SELECT
Close to HDMI Connector

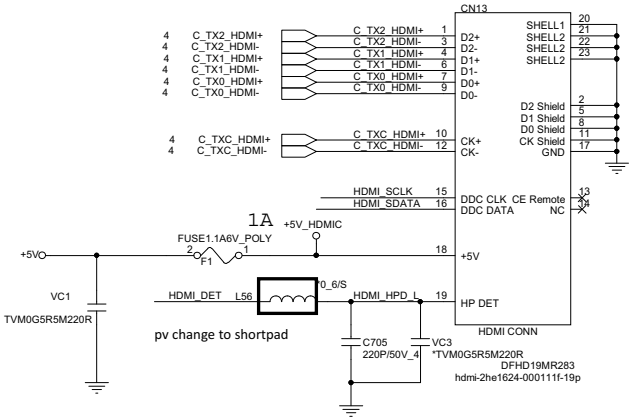
EMI request

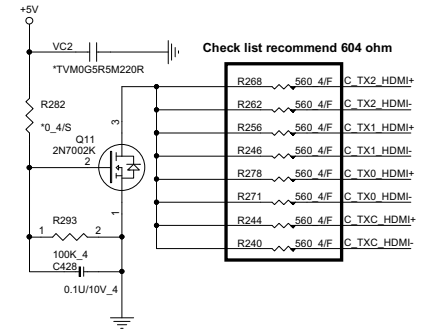


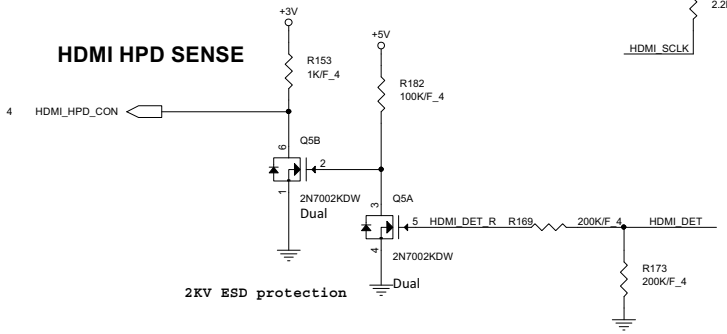


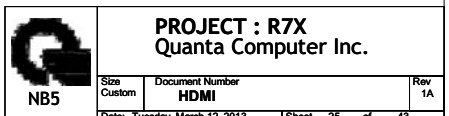


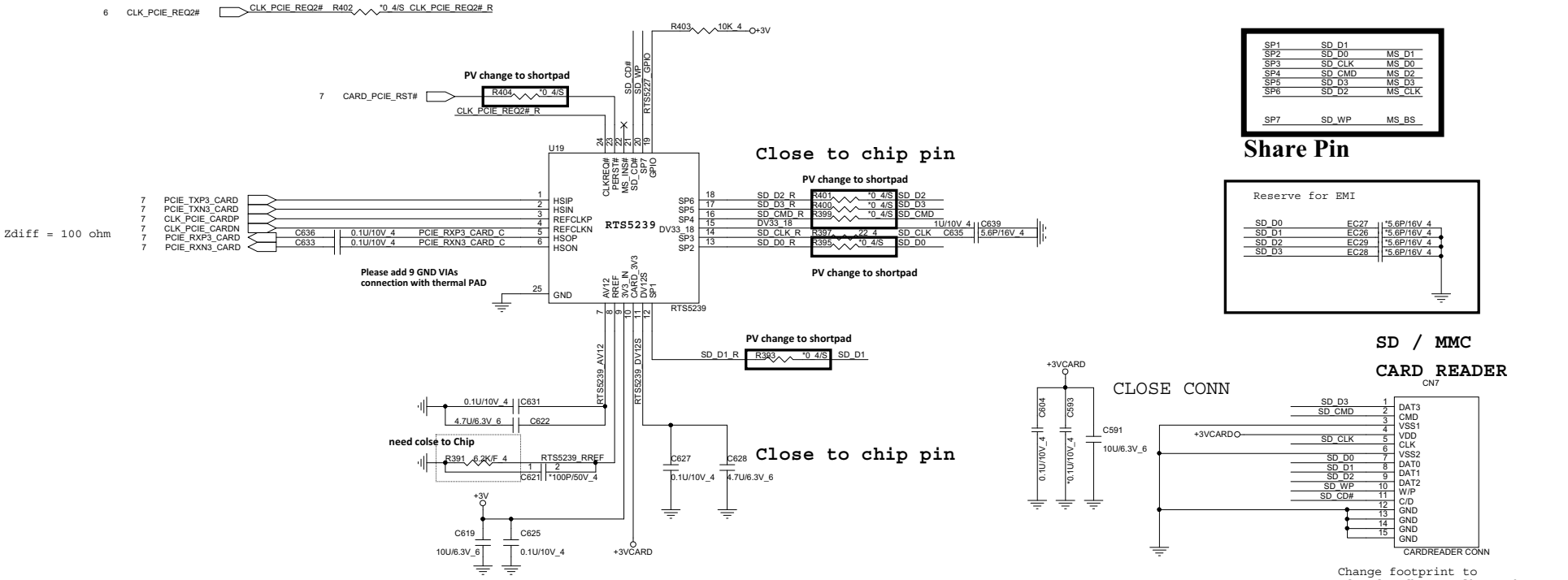












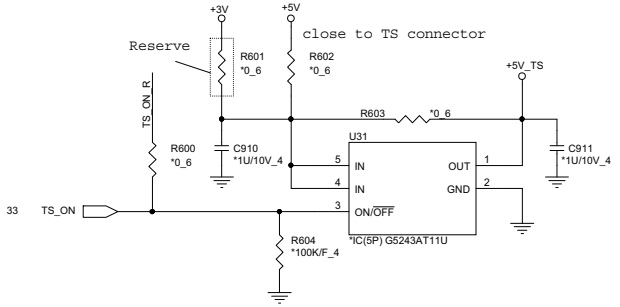
Share Pin

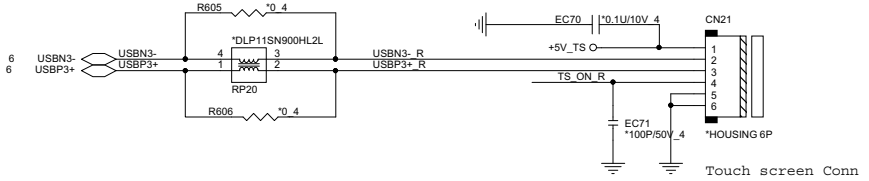
SD / MMC

CARD READER

Change footprint to
sdcard-psdbtc-09glbs1nn4h3-11p

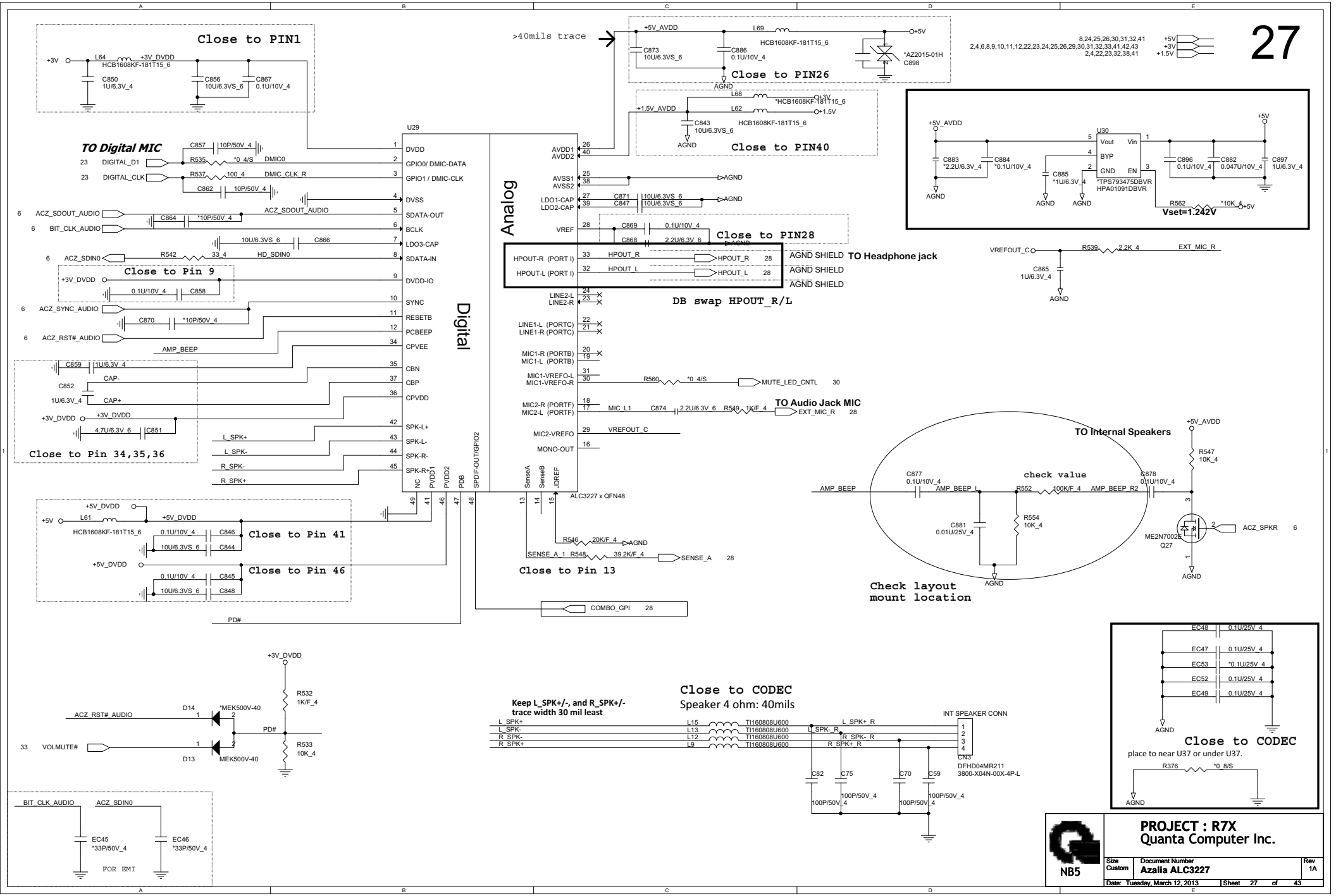
Touch Screen Connector



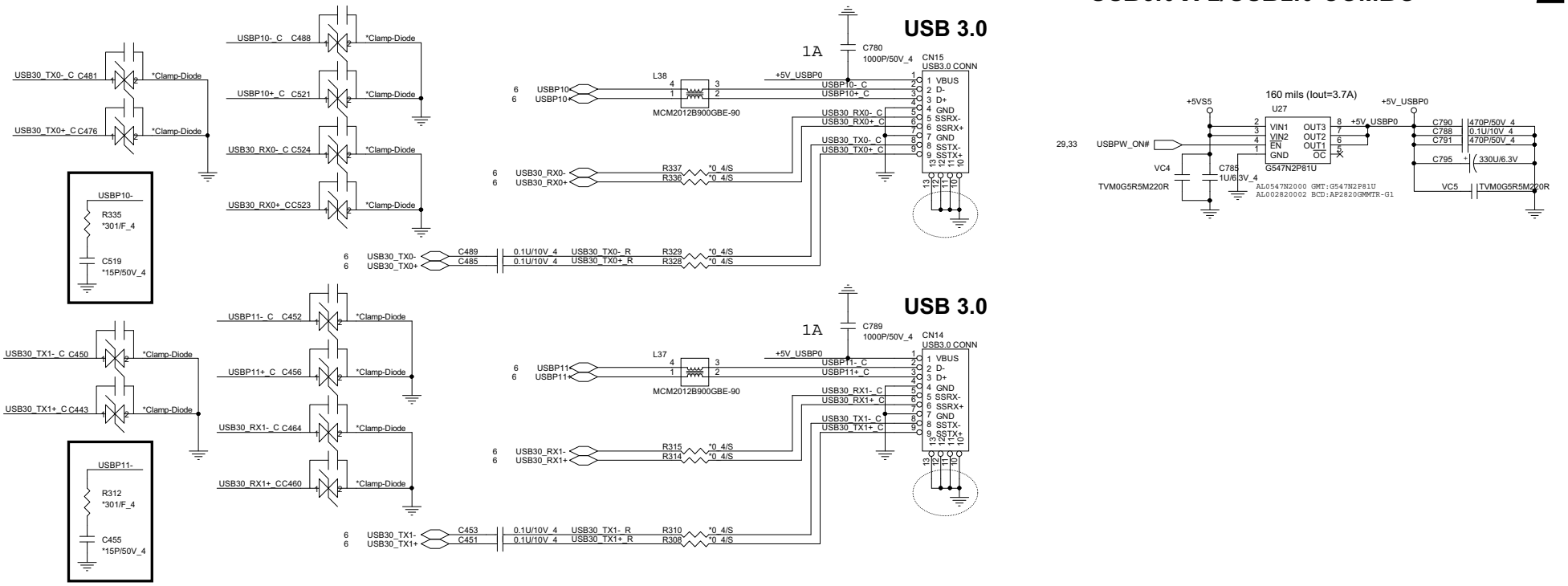


Touch screen Conn

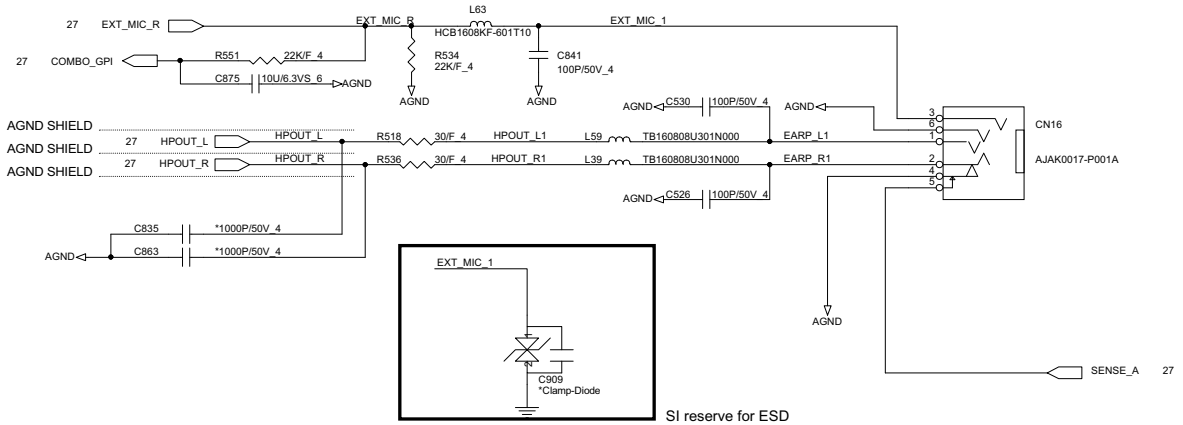
NB5	PROJECT : R7X Quanta Computer Inc.	
	Size: Custom Document Number: RTS5229 & CR SOCKET	Rev: 1A
	Date: Tuesday, March 12, 2013	Sheet 26 of 43


Close to PIN1
+3V
L64
+3V_DVDD
HCB1608KF-181T15_6
C850
1U/6.3V_4
C856
10U/6.3VS_6
C867
0.1U/10V_4
>40mils trace
+5V_AVDD
L69
HCB1608KF-181T15_6
+5V
C873
10U/6.3VS_6
C886
0.1U/10V_4
*AZ2015-01H
C898
Close to PIN26
AGND
L68
+3V
*HCB1608KF-181T15_6
+1.5V_AVDD
L62
+1.5V
C843
10U/6.3VS_6
HCB1608KF-181T15_6
AGND
Close to PIN40
8,24,25,26,30,31,32,41
2,4,6,8,9,10,11,12,22,23,24,25,26,29,30,31,32,33,41,42,43
2,4,22,23,32,38,41
+5V
+3V
+1.5V
27
+5V_AVDD
U30
Vout
Vin
BYP
GND
EN
*TPS793475DBVR
HPA01091DBVR
C883
*2.2U/6.3V_4
C884
*0.1U/10V_4
C885
*1U/6.3V_4
C896
0.1U/10V_4
C882
0.047U/10V_4
C897
1U/6.3V_4
R562
*10K_4
Vset=1.242V
TO Digital MIC
C857
10P/50V_4
23 DIGITAL_D1
R535
*0_4/S
DMIC0
23 DIGITAL_CLK
R537
100_4
DMIC_CLK_R
C862
10P/50V_4
6 ACZ_SDOUT_AUDIO
ACZ_SDOUT_AUDIO
C864
*10P/50V_4
6 BIT_CLK_AUDIO
10U/6.3VS_6
C866
6 ACZ_SDIN0
R542
33_4
HD_SDIN0
Close to Pin 9
+3V_DVDD
0.1U/10V_4
C858
6 ACZ_SYNC_AUDIO
C870
*10P/50V_4
6 ACZ_RST#_AUDIO
AMP_BEEP
C859
1U/6.3V_4
C852
CAP-
1U/6.3V_4
CAP+
+3V_DVDD
+3V_DVDD
4.7U/6.3V_6
C851
Close to Pin 34,35,36
U29
Digital
DVDD
GPIO0/ DMIC-DATA
GPIO1 / DMIC-CLK
DVSS
SDATA-OUT
BCLK
LDO3-CAP
SDATA-IN
DVDD-IO
SYNC
RESETB
PCBEEP
CPVEE
CBN
CBP
CPVDD
SPK-L+
SPK-L-
SPK-R-
SPK-R+
L_SPK+
L_SPK-
R_SPK-
R_SPK+
NC
PVDD1
PVDD2
PDB
SPDIF-OUT/GPIO2
Analog
AVDD1
AVDD2
AVSS1
AVSS2
LDO1-CAP
LDO2-CAP
VREF
C871
10U/6.3VS_6
C847
10U/6.3VS_6
C869
0.1U/10V_4
C868
2.2U/6.3V_6
Close to PIN28
HPOUT-R (PORT I)
HPOUT-L (PORT I)
HPOUT_R
HPOUT_L
AGND SHIELD
TO Headphone jack
DB swap HPOUT_R/L
LINE2-L
LINE2-R
LINE1-L (PORTC)
LINE1-R (PORTC)
MIC1-R (PORTB)
MIC1-L (PORTB)
MIC1-VREFO-L
MIC1-VREFO-R
R560
*0_4/S
MUTE_LED_CNTL
MIC2-R (PORTF)
MIC2-L (PORTF)
MIC_L1
C874
2.2U/6.3V_6
R549
1K/F_4
EXT_MIC_R
TO Audio Jack MIC
MIC2-VREFO
VREFOUT_C
MONO-OUT
SenseA
SenseB
JDREF
ALC3227 x QFN48
R546
20K/F_4
SENSE_A_1
R548
39.2K/F_4
SENSE_A
Close to Pin 13
COMBO_GPI
PD#
VREFOUT_C
R539
2.2K_4
EXT_MIC_R
C865
1U/6.3V_4
TO Internal Speakers
+5V_AVDD
R547
10K_4
check value
AMP_BEEP
C877
0.1U/10V_4
AMP_BEEP_L
R552
100K/F_4
AMP_BEEP_R2
C878
0.1U/10V_4
C881
0.01U/25V_4
R554
10K_4
ME2N7002E
Q27
ACZ_SPKR
6
Check layout
mount location
+5V
+5V_DVDD
L61
+5V_DVDD
HCB1608KF-181T15_6
0.1U/10V_4
C846
10U/6.3VS_6
C844
Close to Pin 41
+5V_DVDD
0.1U/10V_4
C845
10U/6.3VS_6
C848
Close to Pin 46
+3V_DVDD
R532
1K/F_4
ACZ_RST#_AUDIO
D14
*MEK500V-40
PD#
33 VOLMUTE#
D13
MEK500V-40
R533
10K_4
Keep L_SPK+/-, and R_SPK+/-
trace width 30 mil least
Close to CODEC
Speaker 4 ohm: 40mils
L_SPK+
L_SPK-
R_SPK-
R_SPK+
L15
L13
L12
L9
TI160808U600
L_SPK+_R
L_SPK-_R
R_SPK-_R
R_SPK+_R
INT SPEAKER CONN
CN3
DFHD04MR211
3800-X04N-00X-4P-L
C82
C75
C70
C59
100P/50V_4
EC48
EC47
EC53
EC52
EC49
0.1U/25V_4
*0.1U/25V_4
Close to CODEC
place to near U37 or under U37.
R376
*0_8/S
BIT_CLK_AUDIO
ACZ_SDIN0
EC45
*33P/50V_4
EC46
*33P/50V_4
FOR EMI
AGND
NB5
PROJECT : R7X
Quanta Computer Inc.
Size
Custom
Document Number
Azalia ALC3227
Rev
1A
Date: Tuesday, March 12, 2013
Sheet 27 of 43

USB3.0 X 2/USB2.0 COMBO



COMBO JACK



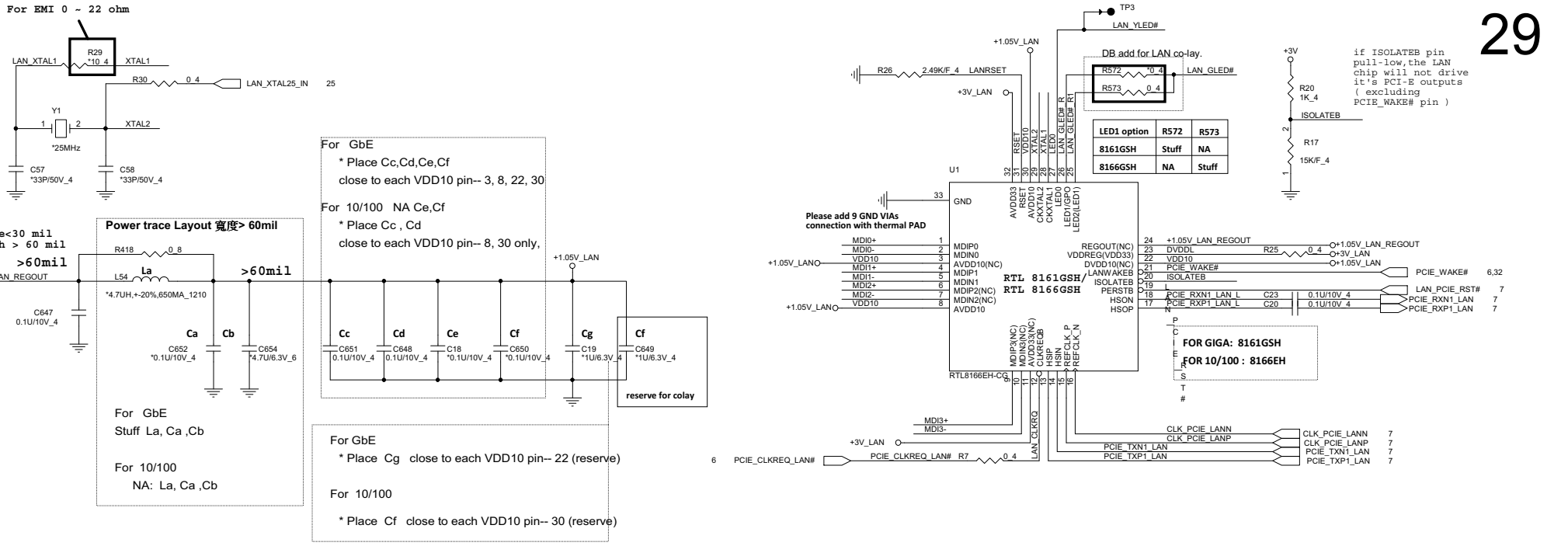
SI reserve for ESD

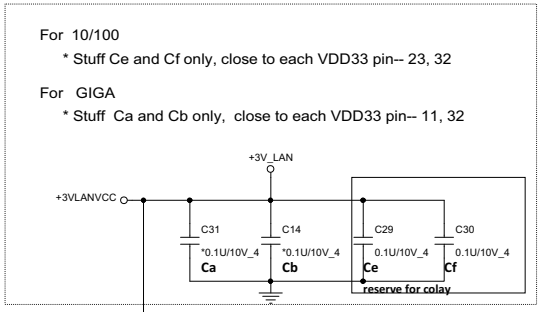
NB5

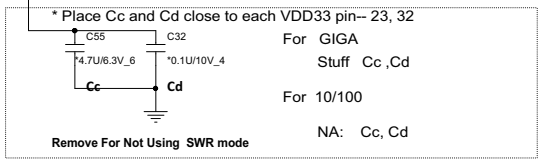
PROJECT : R7X
Quanta Computer Inc.

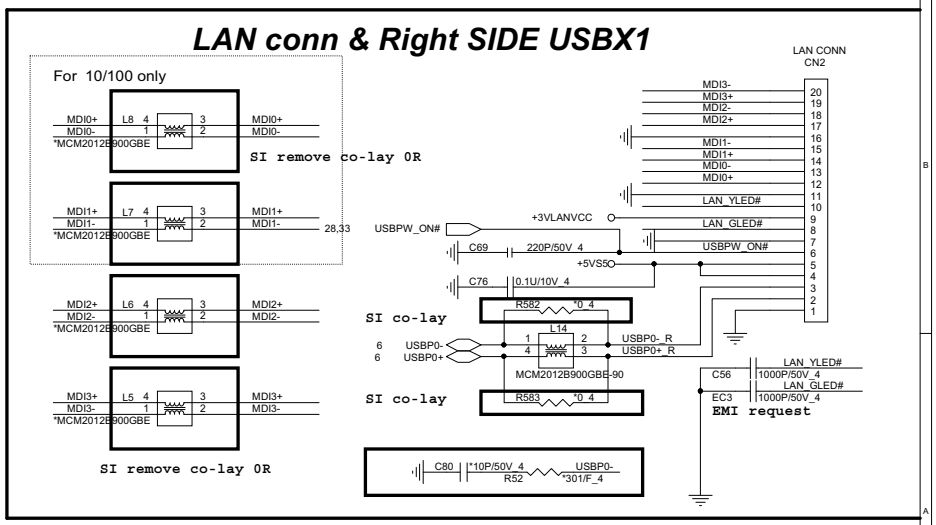
Size	Document Number	Rev
Custom	USB/Audio JacK	1A

Date: Tuesday, March 12, 2013 Sheet 28 of 43





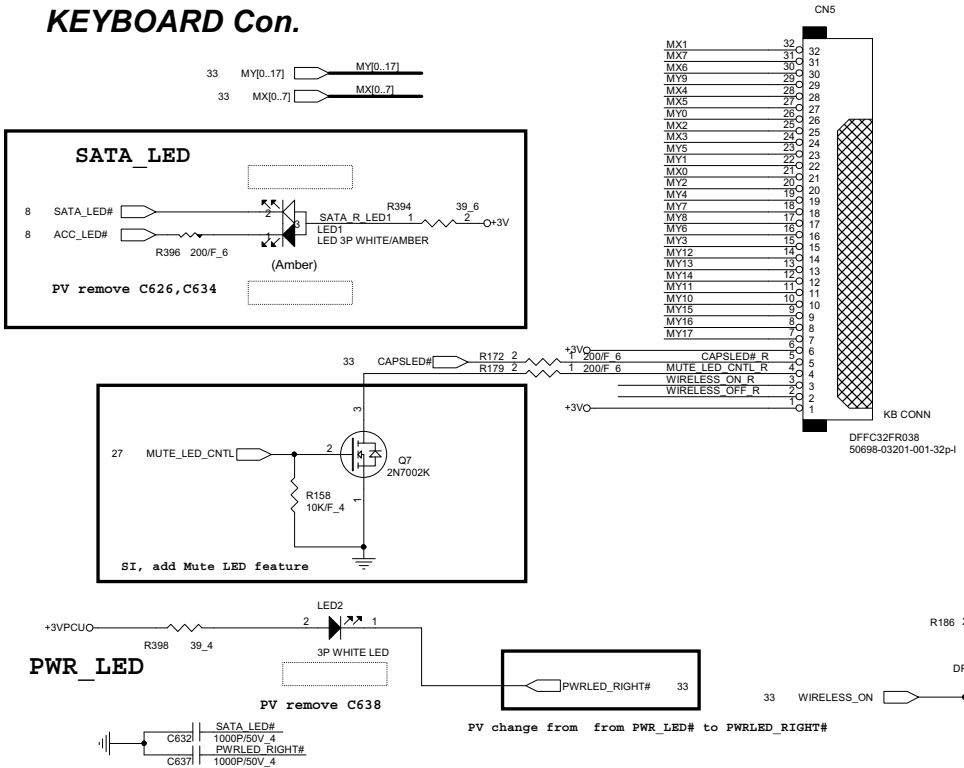




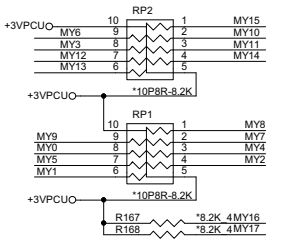
2,4,6,8,9,10,11,12,22,23,24,25,26,27,30,31,32,33,41,42,43 +3V
25,41 +3VLANVCC

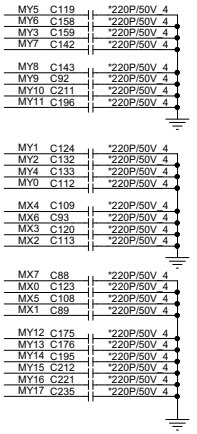
NB5	PROJECT : R7X Quanta Computer Inc.		
	Size: Custom	Document Number: RTL 8105E/RJ45	Rev: 1A
	Date: Tuesday, March 12, 2013	Sheet 29 of 43	

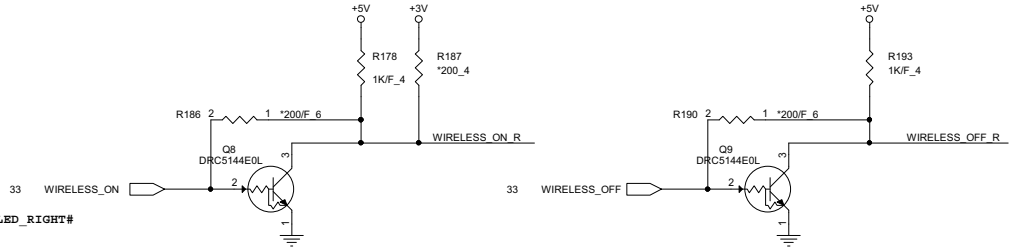
KEYBOARD Con.



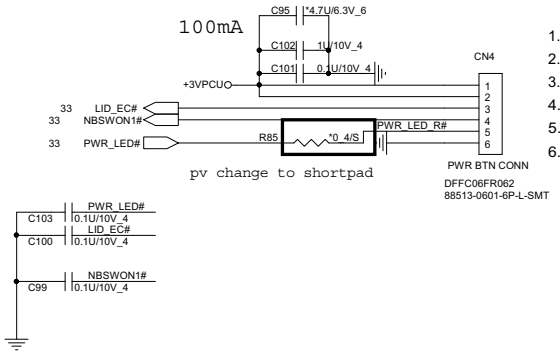
KEYBOARD PULL-UP



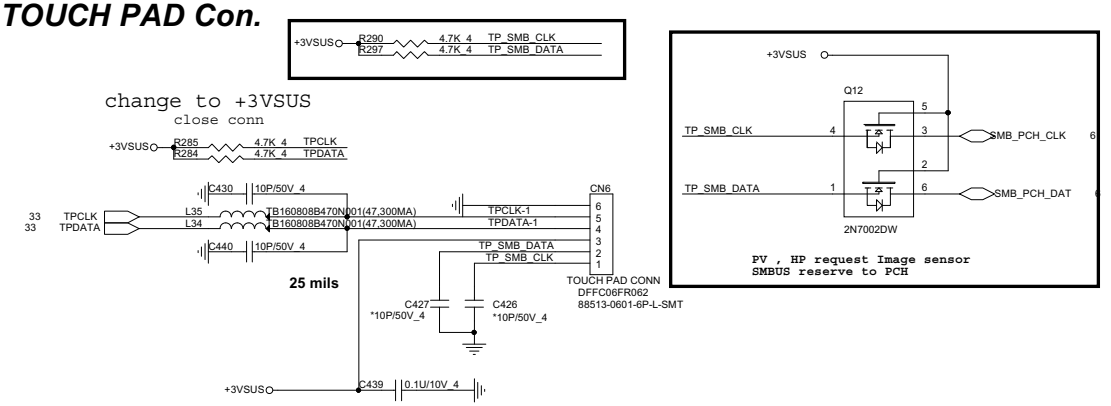




POWER BOTTON CONNECT



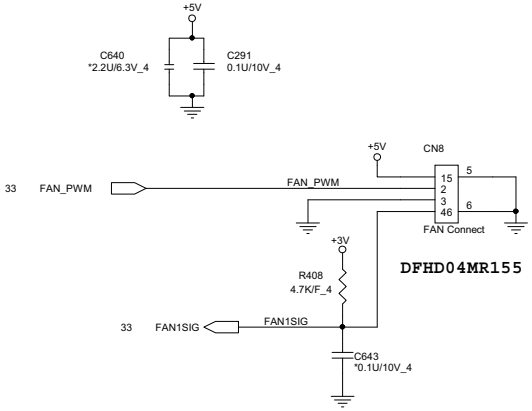
TOUCH PAD Con.



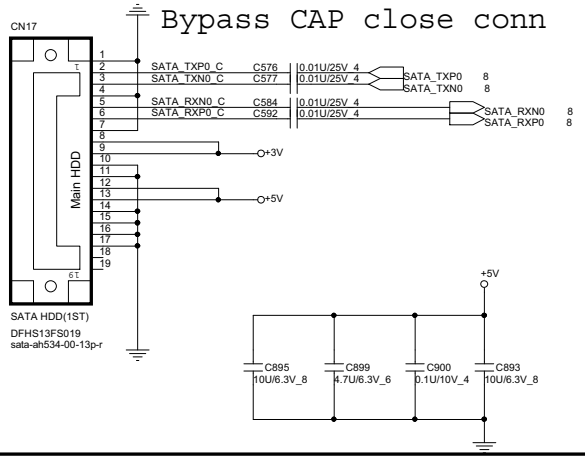
7,25,32,33,34,35 +3VPCU
8,24,25,26,27,31,32,41 +5V
41 +3VSUS
2,4,6,8,9,10,11,12,22,23,24,25,26,27,29,31,32,33,41,42,43 +3V

NB5	PROJECT : R7X Quanta Computer Inc.	
Size: Custom	Document Number: LED/KB/SW/TP	Rev: 1A
Date: Tuesday, March 12, 2013	Sheet 30 of 43	

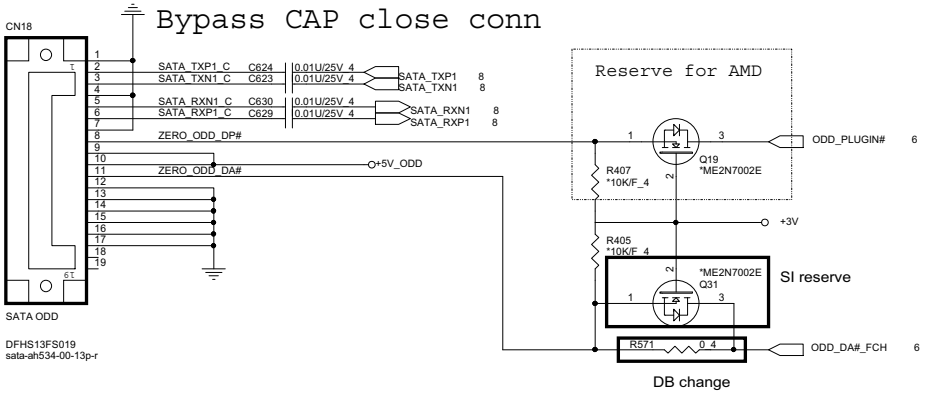
CPU FAN

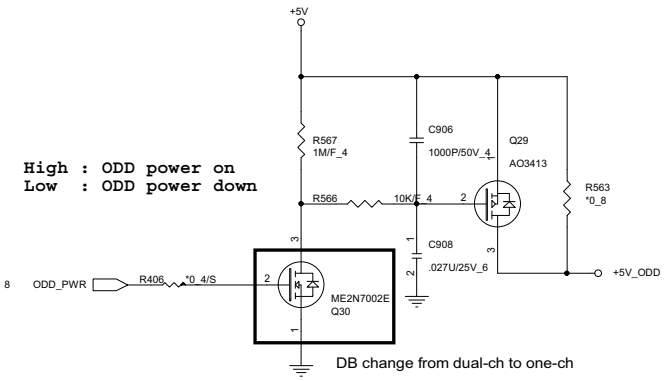


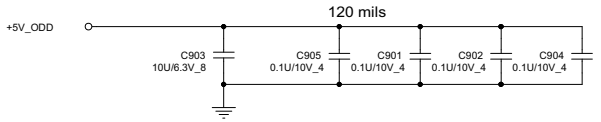
SATA HDD CONNECTOR



SATA ODD CONNECTOR







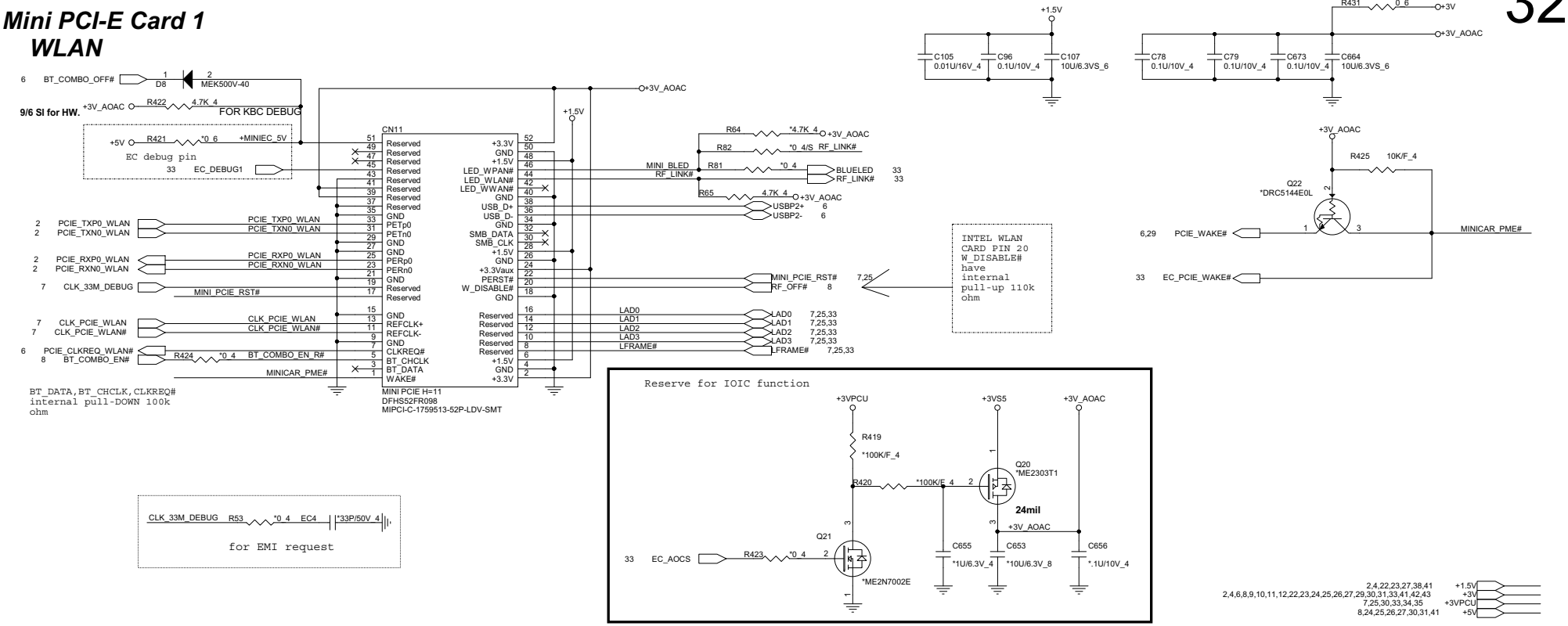
NB5

PROJECT : R7X
Quanta Computer Inc.

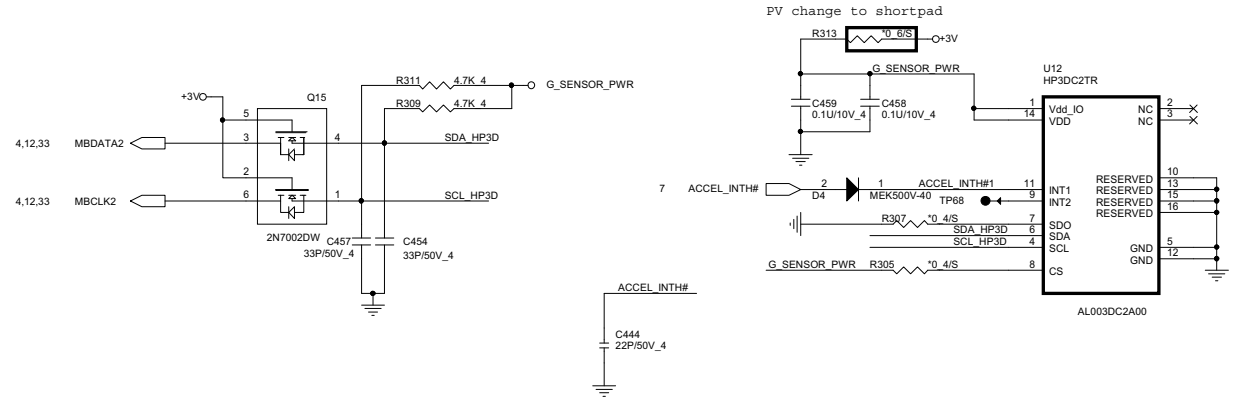
Size	Document Number	Rev
Custom	HDD/ODD/FAN	1A

Date: Tuesday, March 12, 2013 Sheet 31 of 43

Mini PCI-E Card 1
WLAN



Accelerometer Sensor



NB5	PROJECT : R7X Quanta Computer Inc.		
	Size: Custom	Document Number: MINI PCIE CONN & G-sensor	Rev: 1A
	Date: Tuesday, March 12, 2013	Sheet 32 of 43	

ITE pin 100 , 104 , 106 default can not pull up to +3VPCU it will cause chip into test mode

+3VPCU CAP close to EC pin

Smart adapter Type check

Change to 1SS355 as Current loss

D11 1SS355

DGPU Thermal protect

4M SPI EC ROM

128K byte SPI EC ROM

IO Thrm Protect

For 65 degree, 1.8v limit, (SW)

For 75 degree, 1.2v limit, (HW)

For +VIN noise

Vender	Size	P/N
AMIC	4M	AKE39ZN0800
EON	4M	AKE39ZN0Q03
WINBOND	4M	AKE39FN0N01
Socket		DFHS08FS023

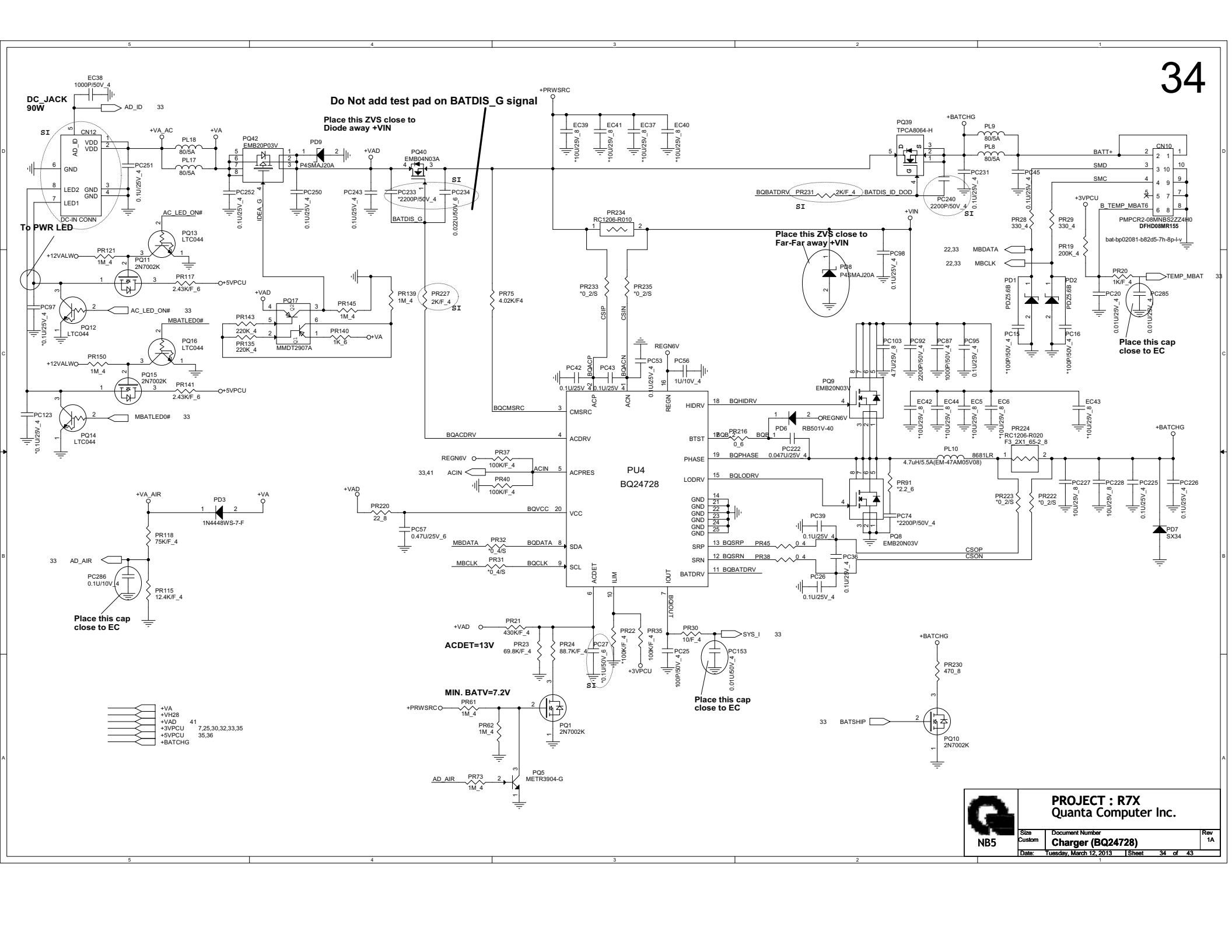
Adapter select

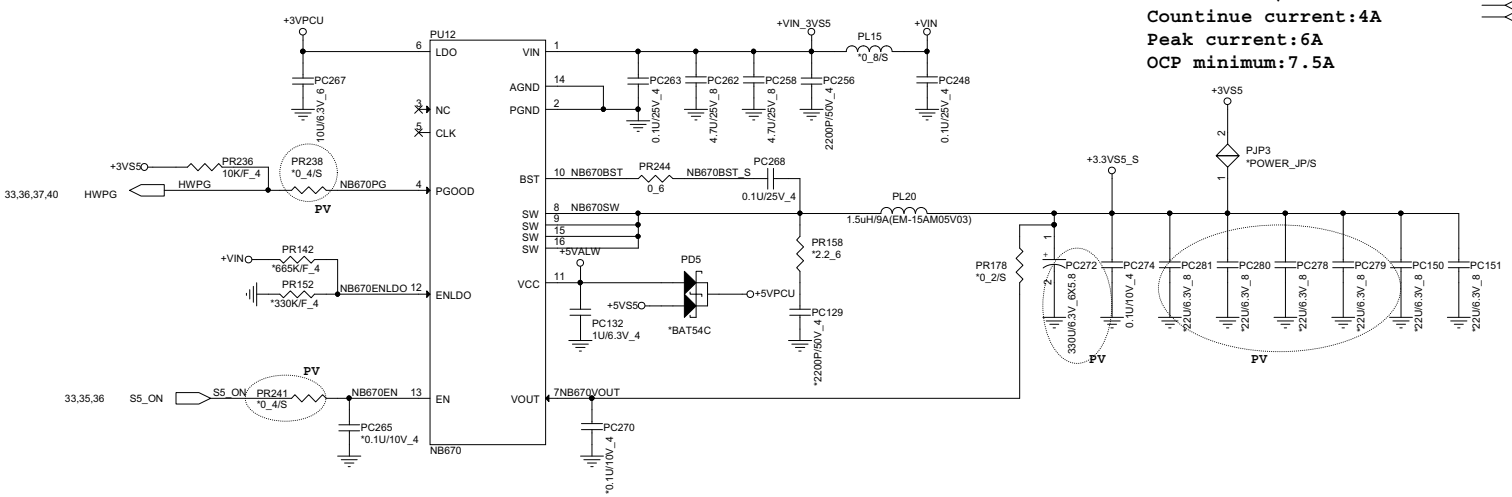
Platform model	GPIO42	adapter
SG/DIS	High	90W
UMA	Low	65W

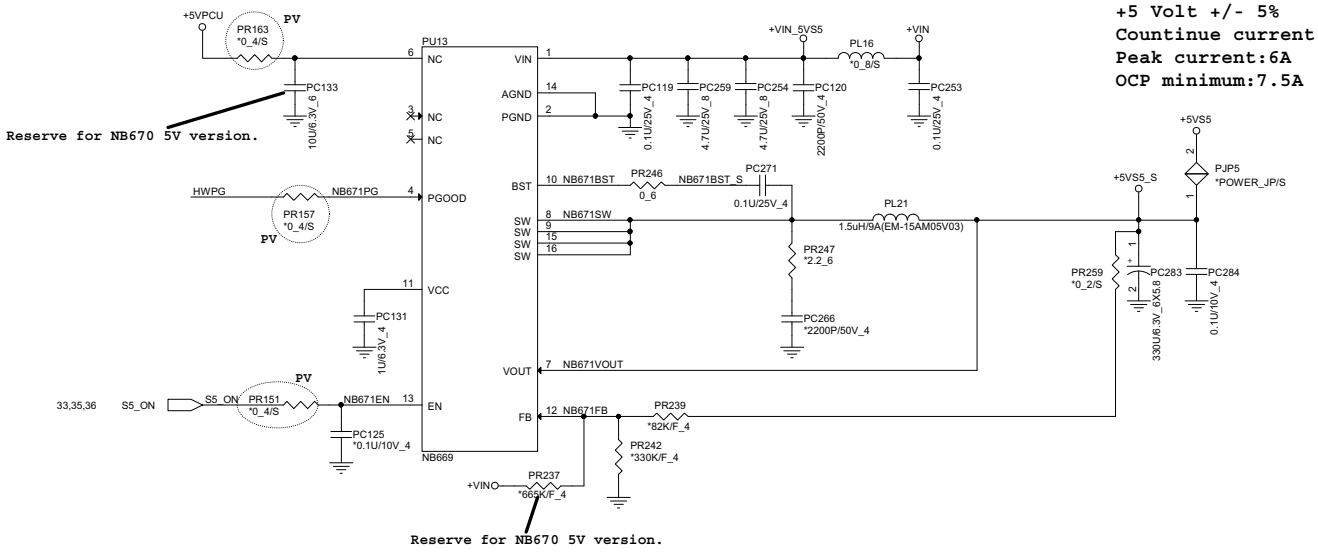
Hi ==> DIS/SG
Low ==>UMA

PROJECT :	R7X
Quanta Computer Inc.	
Size: Custom	Document Number: EC (IT8518E/HX)/ROM
Rev: 1A	
Date: Tuesday, March 12, 2013	Sheet 33 of 43

NB5

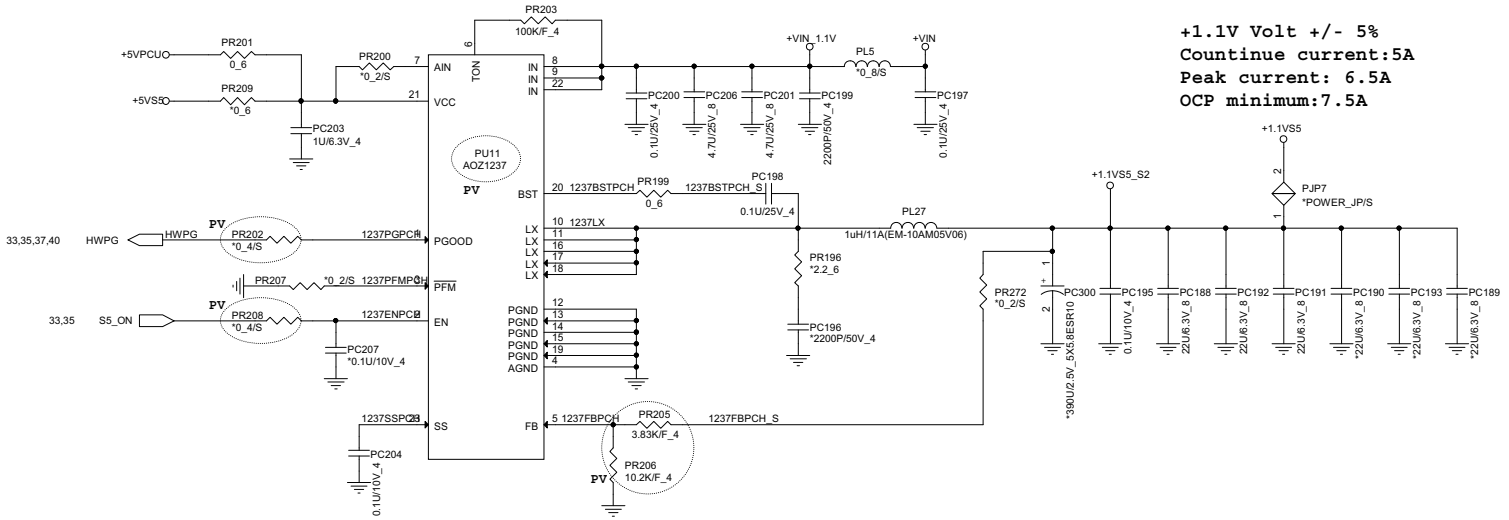

DC_JACK
90W
Do Not add test pad on BATDIS_G signal
Place this ZVS close to
Diode away +VIN
To PWR LED
Place this ZVS close to
Far-Far away +VIN
Place this cap
close to EC
Place this cap
close to EC
Place this cap
close to EC
ACDET=13V
MIN. BATV=7.2V
PU4
BQ24728
PROJECT : R7X
Quanta Computer Inc.
NB5
Charger (BQ24728)
Tuesday, March 12, 2013

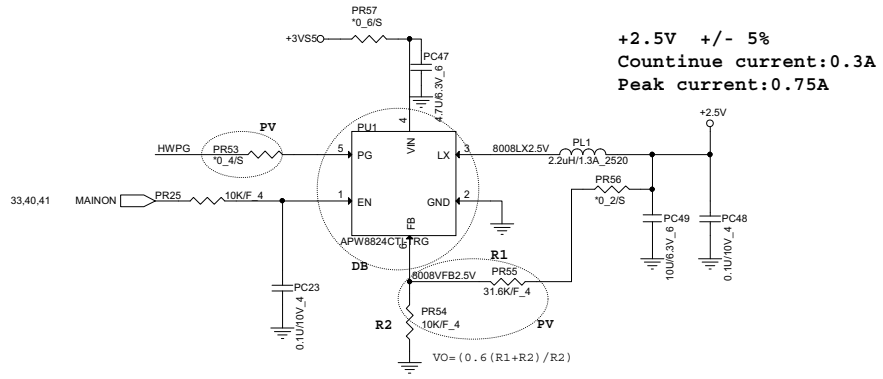




PROJECT : R7X
Quanta Computer Inc.

Size	Document Number	Rev
Custom	3/5VS5 (NB670/NB671)	1A
NB5	Date: Tuesday, March 12, 2013	Sheet 35 of 43





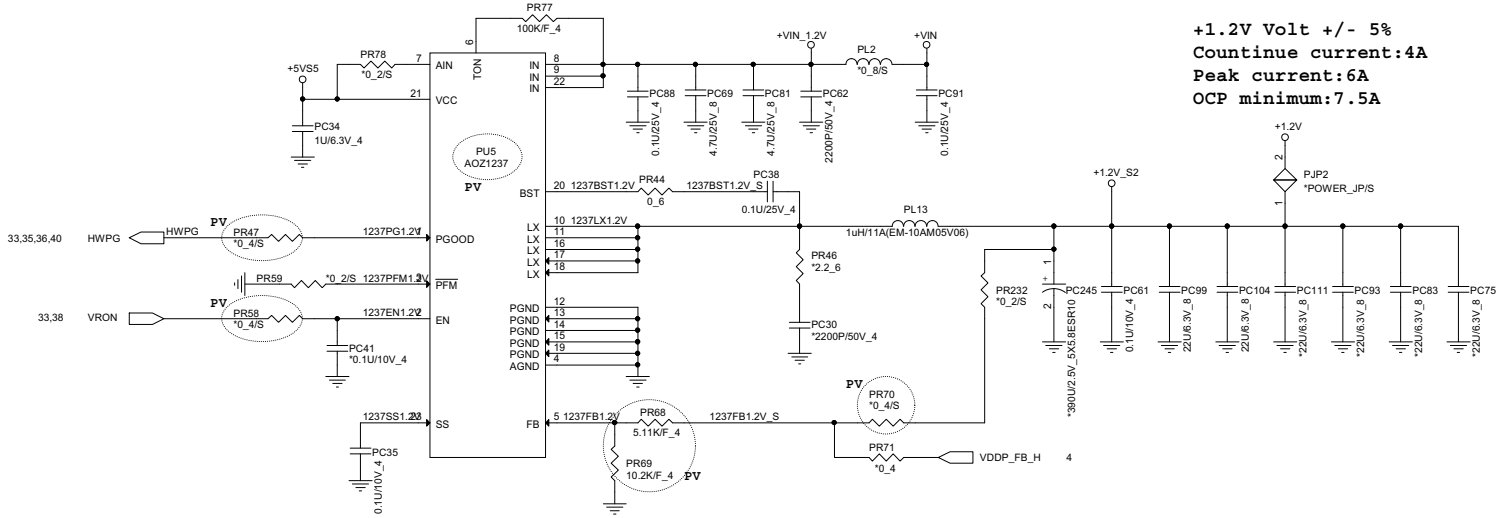
+VIN	23,34,35,37,39,40,41,42,43
+2.5V	5
+3VS5	4,6,8,9,10,25,32,33,35,38,41,43
+5VS5	28,29,35,37,38,39,40,41,42,43
+1.1VS5	9,41
+5VPCU	34,35

NB5

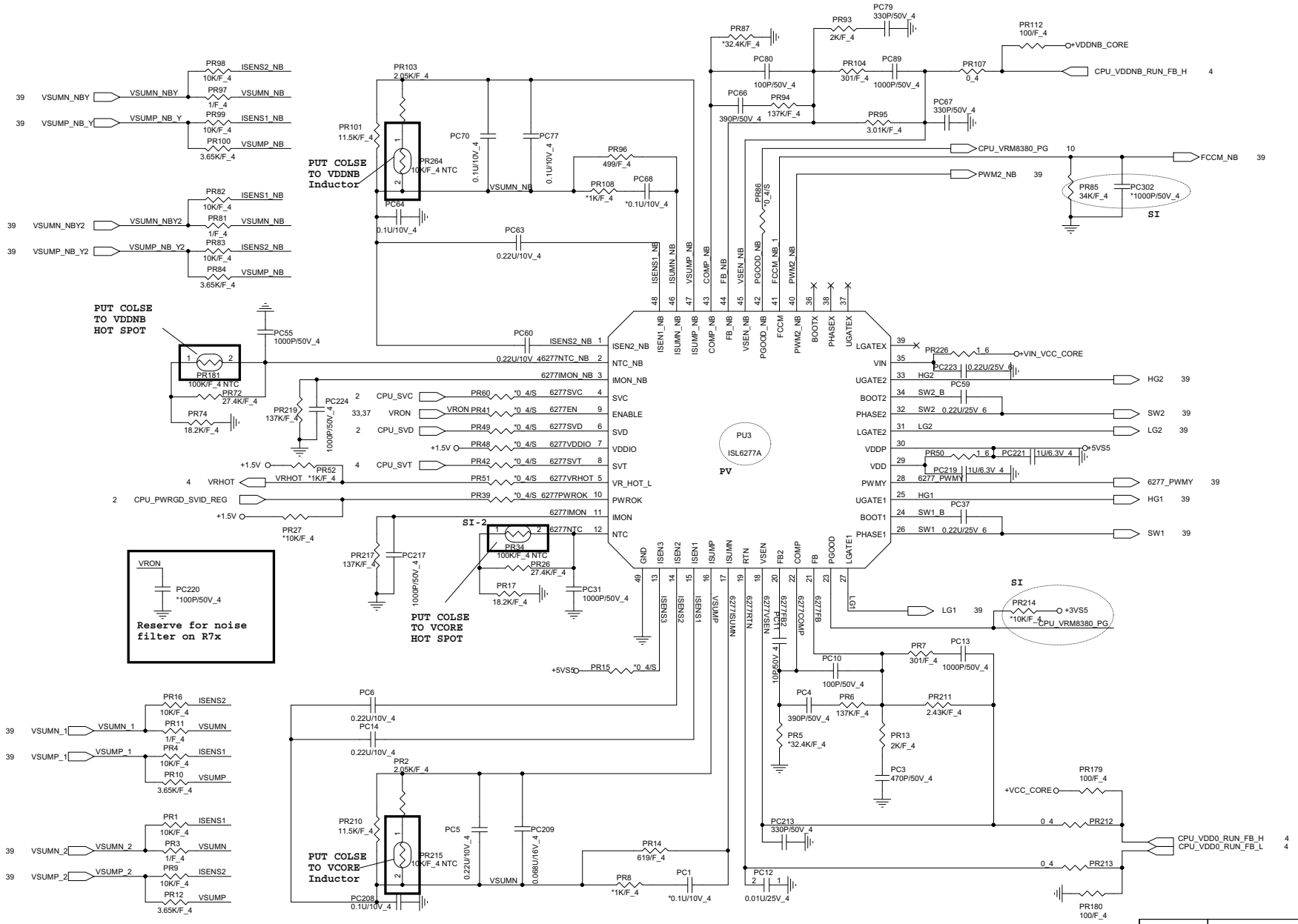
PROJECT : R7X
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.1VS5 (AOZ1237)/2.5V	1A

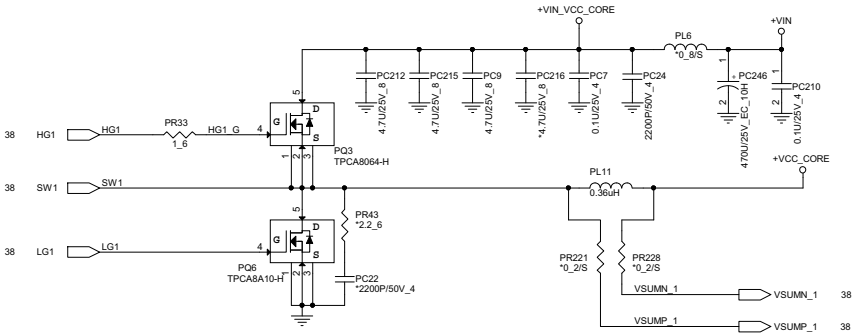
Date: Tuesday, March 12, 2013 Sheet 36 of 43

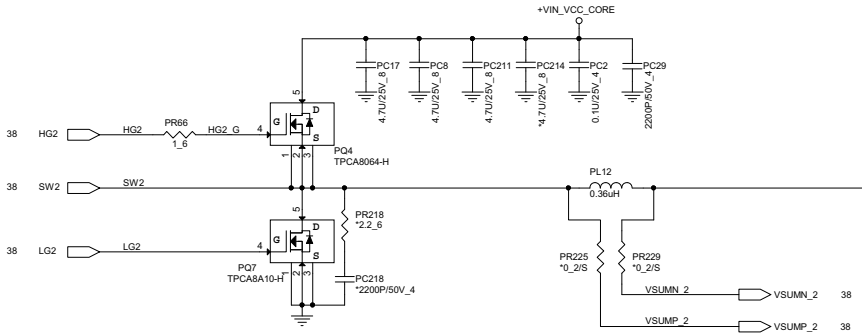


NB5	PROJECT : R7X Quanta Computer Inc.		
	Size: Custom	Document Number: +1.2V (AOZ1237)	Rev: 1A
	Date: Tuesday, March 12, 2013	Sheet 37 of 43	

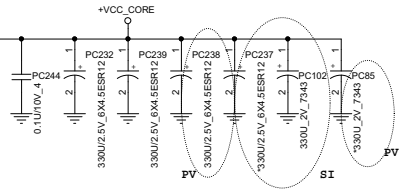


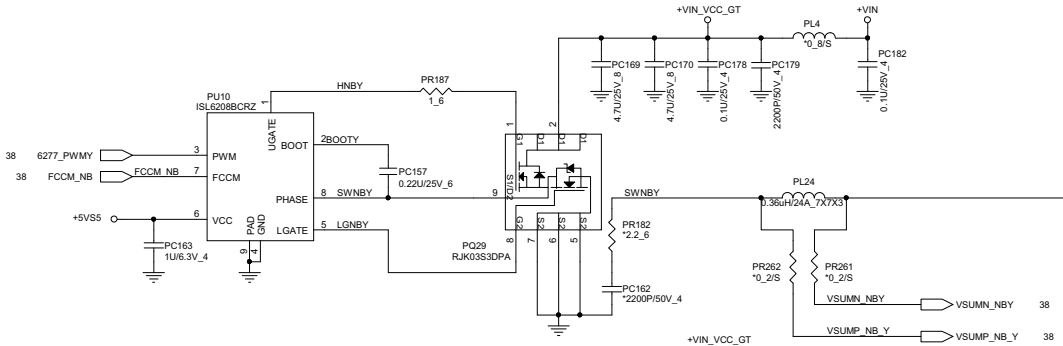
PROJECT : R7X	
Quanta Computer Inc.	
NB5	Size: Custom
Document Number: CPU Core1 (ISL6277)	Rev: 1A
Date: Tuesday, March 12, 2013	Sheet 38 of 43



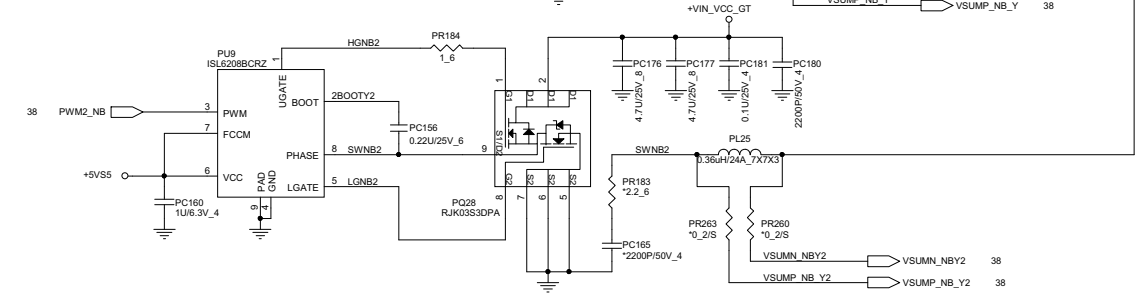


CPU CORE Volt
Countinue current:36A
Peak current:50A
OCP minimum:60A

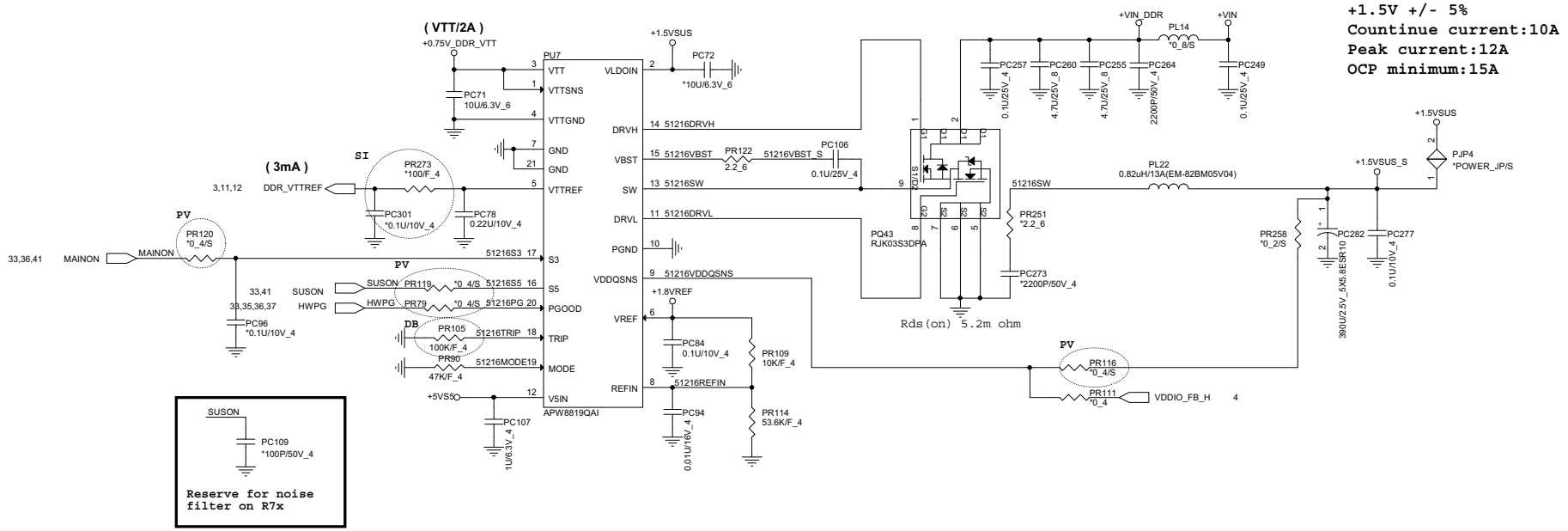




VDDNB Volt
Countinue current:25A
Peak current:33A
OCP minimum:40A

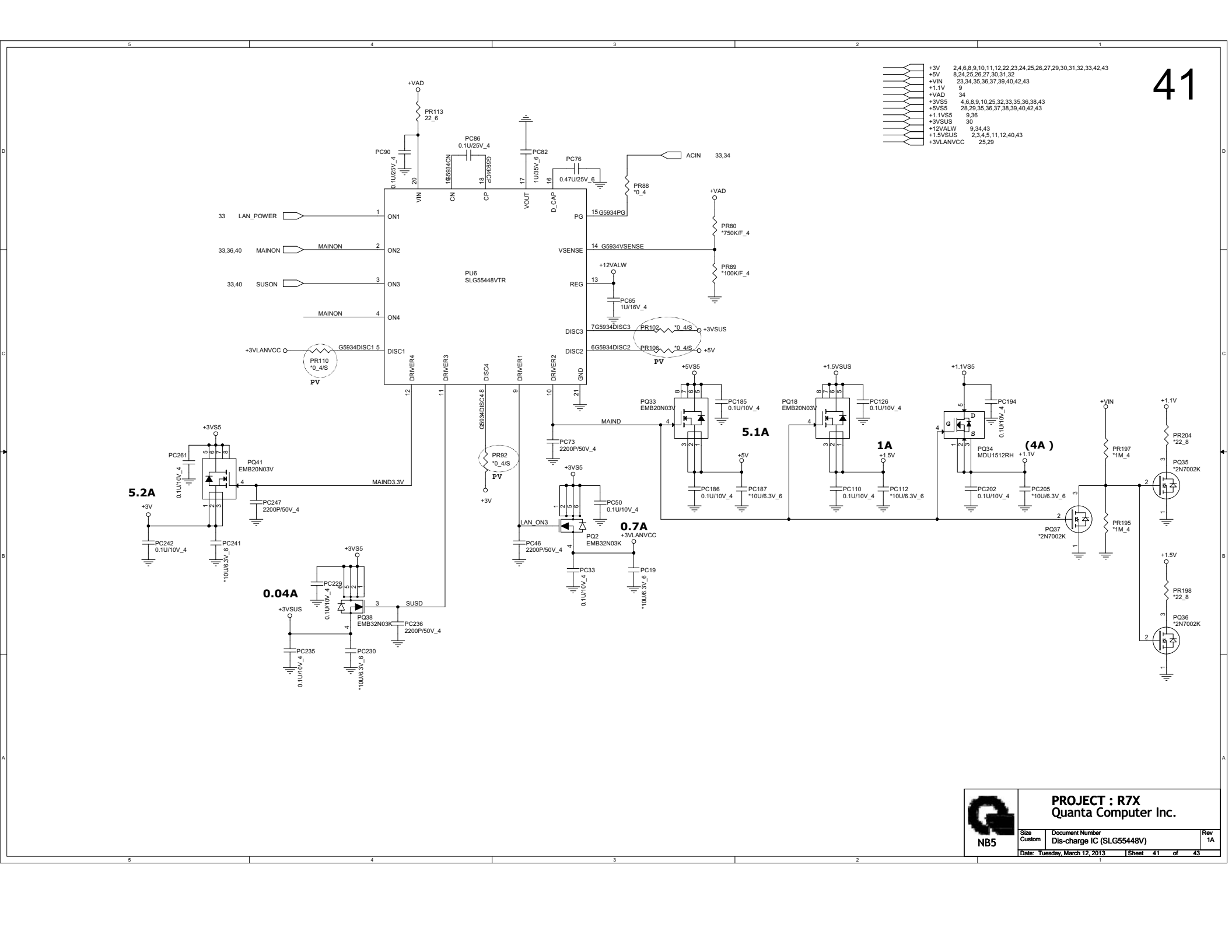


NB5	**PROJECT : R7X** Quanta Computer Inc.	
Size: Custom	Document Number: **CPU Core2 (ISL6208)**	Rev: 1A
Date: Tuesday, March 12, 2013	Sheet 39 of 43	



+1.5V +/- 5%
Countinue current:10A
Peak current:12A
OCP minimum:15A

NB5	**PROJECT : R7X** Quanta Computer Inc.	
Size: Custom	Document Number: **DDR3L(TPS51216)**	Rev: 1A
Date: Tuesday, March 12, 2013	Sheet 40 of 43	



PROJECT : R7X	
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: Dis-charge IC (SLG55448V)
Rev: 1A	
Date: Tuesday, March 12, 2013	Sheet 41 of 43

VGA Core

+VGA_CORE 17,43

GPIO10 GPIO12 GPIO16 GPIO20 GPIO15 Mars XT

PWRCNTL5	PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1	V-CORE	
0	1	1	1	1	1.125V	
1	0	0	0	0	1.100V	Default
1	0	0	0	1	1.075V	
1	0	0	1	0	1.050V	
1	0	0	1	1	1.025V	
1	0	1	0	0	1.000V	
1	0	1	0	1	0.975V	
1	0	1	1	0	0.950V	
1	0	1	1	1	0.925V	
1	1	0	0	0	0.900V	
1	1	0	0	1	0.875V	
1	1	0	1	0	0.850V	
1	1	0	1	1	0.825V	
1	1	1	0	0	0.800V	

Mars (25W)

+VGA_CORE
Countinue current: 25A
Peak current: 30A
OCP minimum: 33A
L-L: 0mV/A

PU8
***NCP3218G**

DCR_1.4m ohm

This NTC Close to Phase 1 MOSFET

Shortest the net trace

Close to Phase 1 Inductor

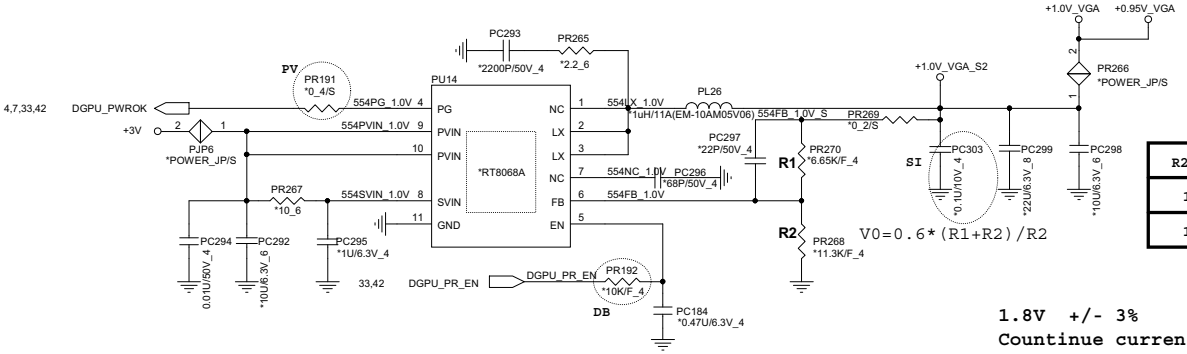
PROJECT : R7X
Quanta Computer Inc.

NB5

Size: Custom | Document Number: +VGACORE (NCP3218G) | Rev: 1A

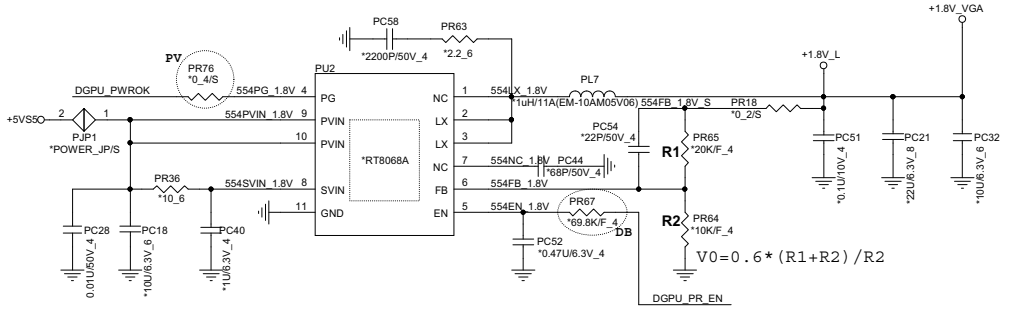
Date: Tuesday, March 12, 2013 | Sheet 42 of 43

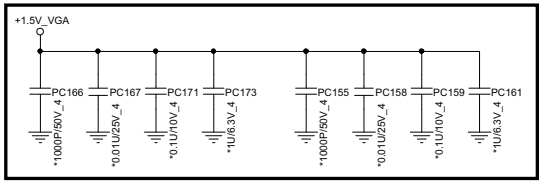
+0.95V +/- 3%
Countinue current:2A
Peak current:3A
OCP minimum:4A

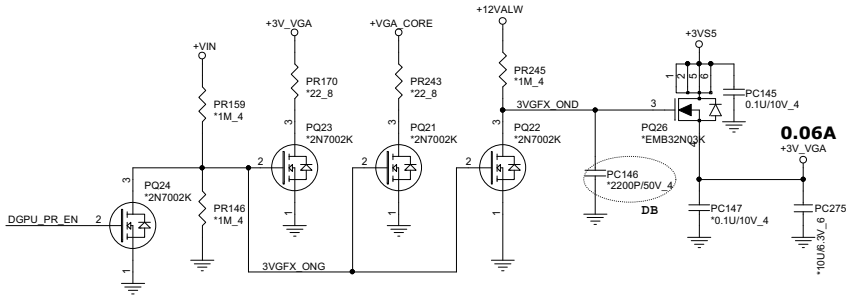


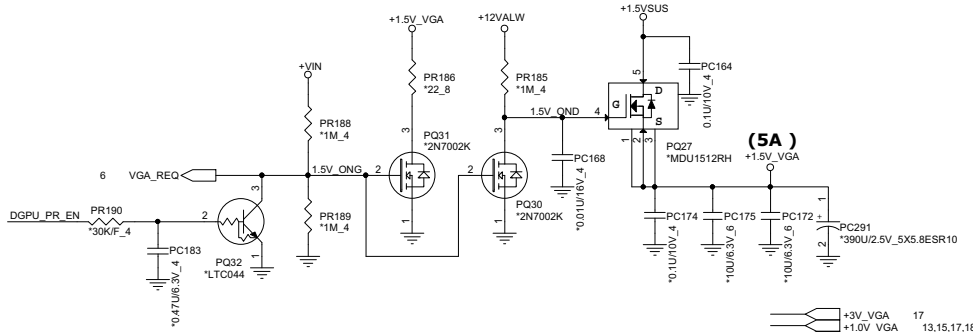
R2 Value	P/N	1.0V_VGA
10K	CS31002FB26	1.0V
11.3K	CS31132FB07	0.95V

1.8V +/- 3%
Countinue current:2A
Peak current:3A
OCP minimum:4A









PROJECT : R7X
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.0V_VGA/1.8V_VGA/3V_VGA	1A

NB5

Date: Tuesday, March 12, 2013 Sheet 43 of 43