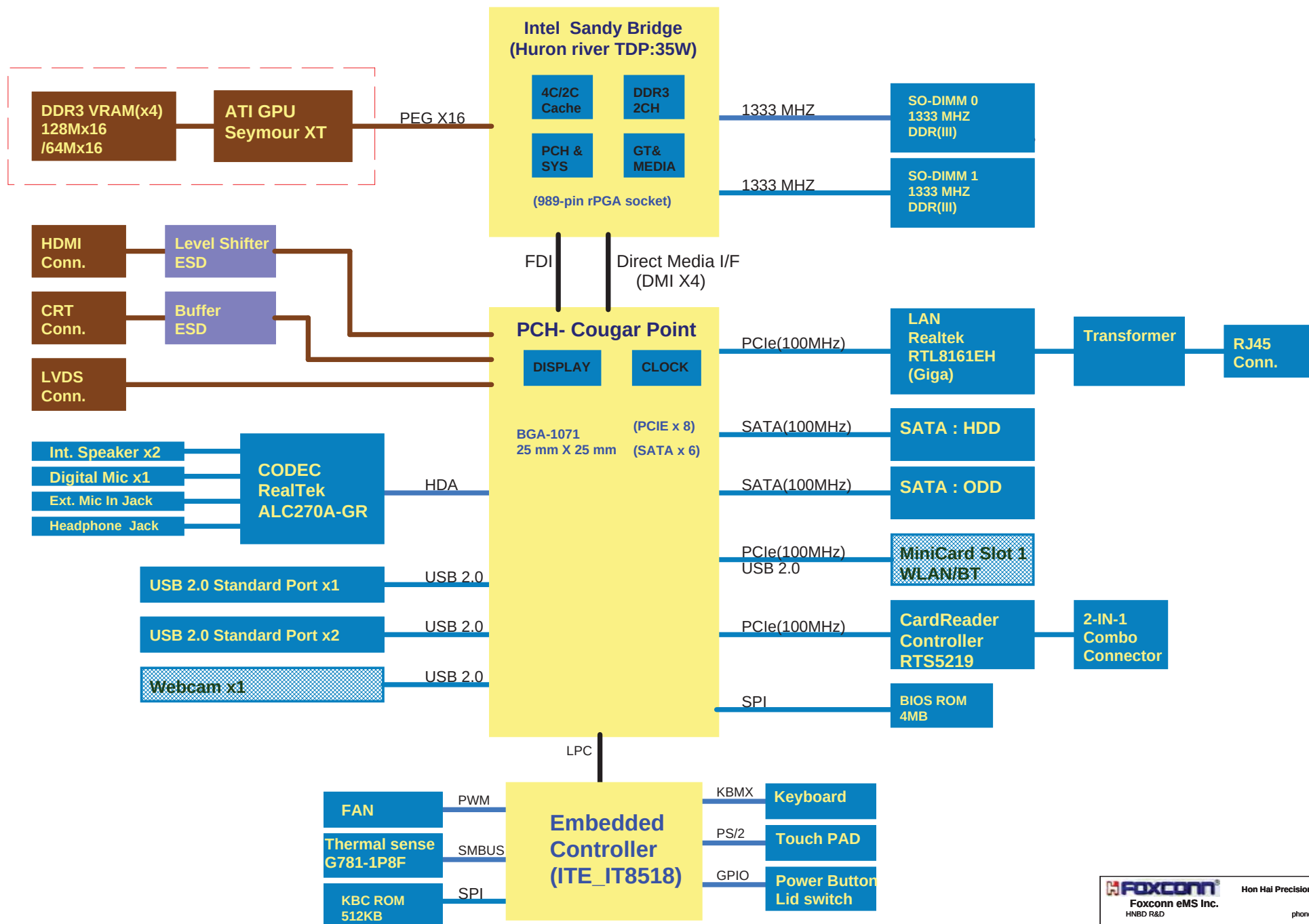
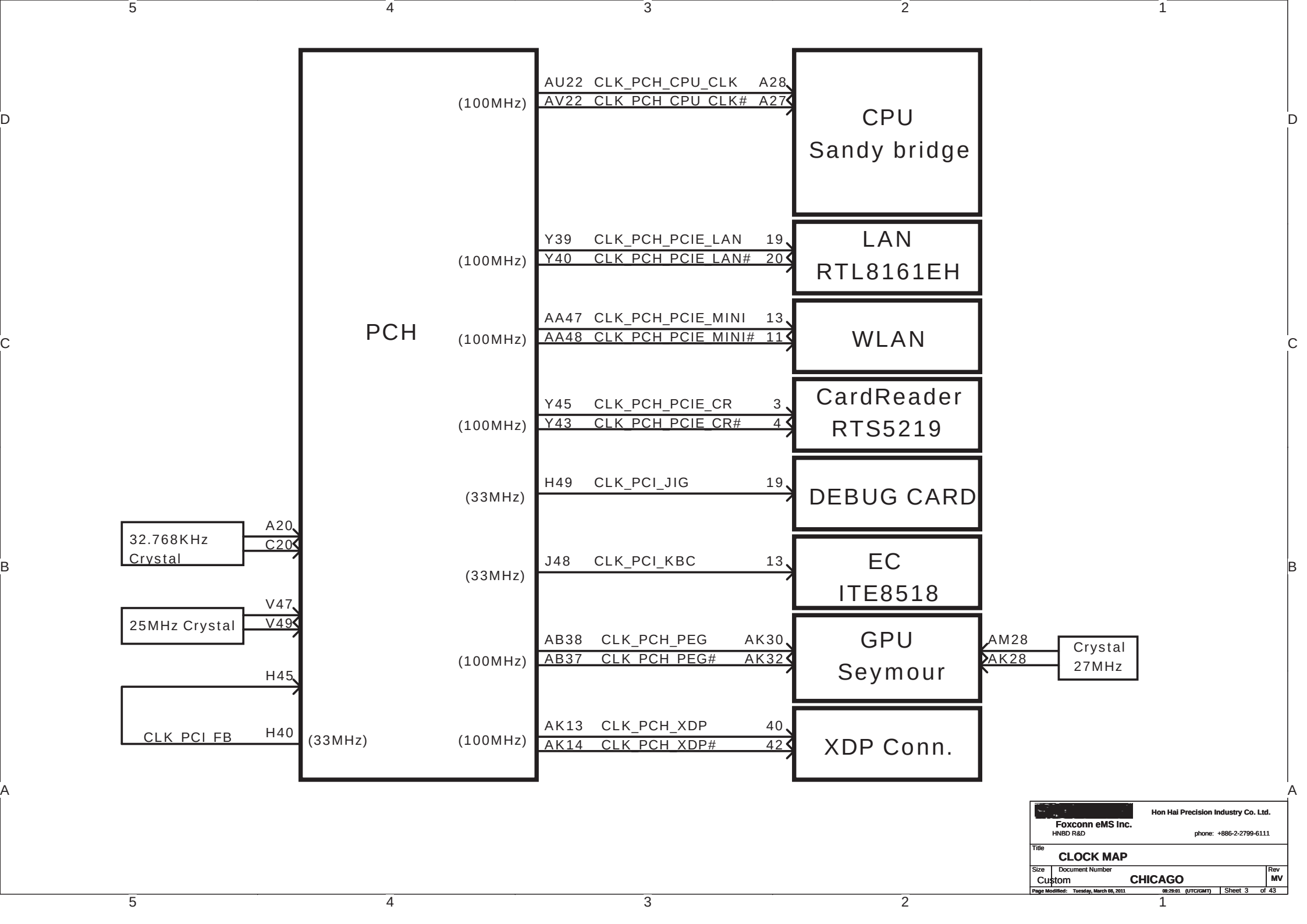
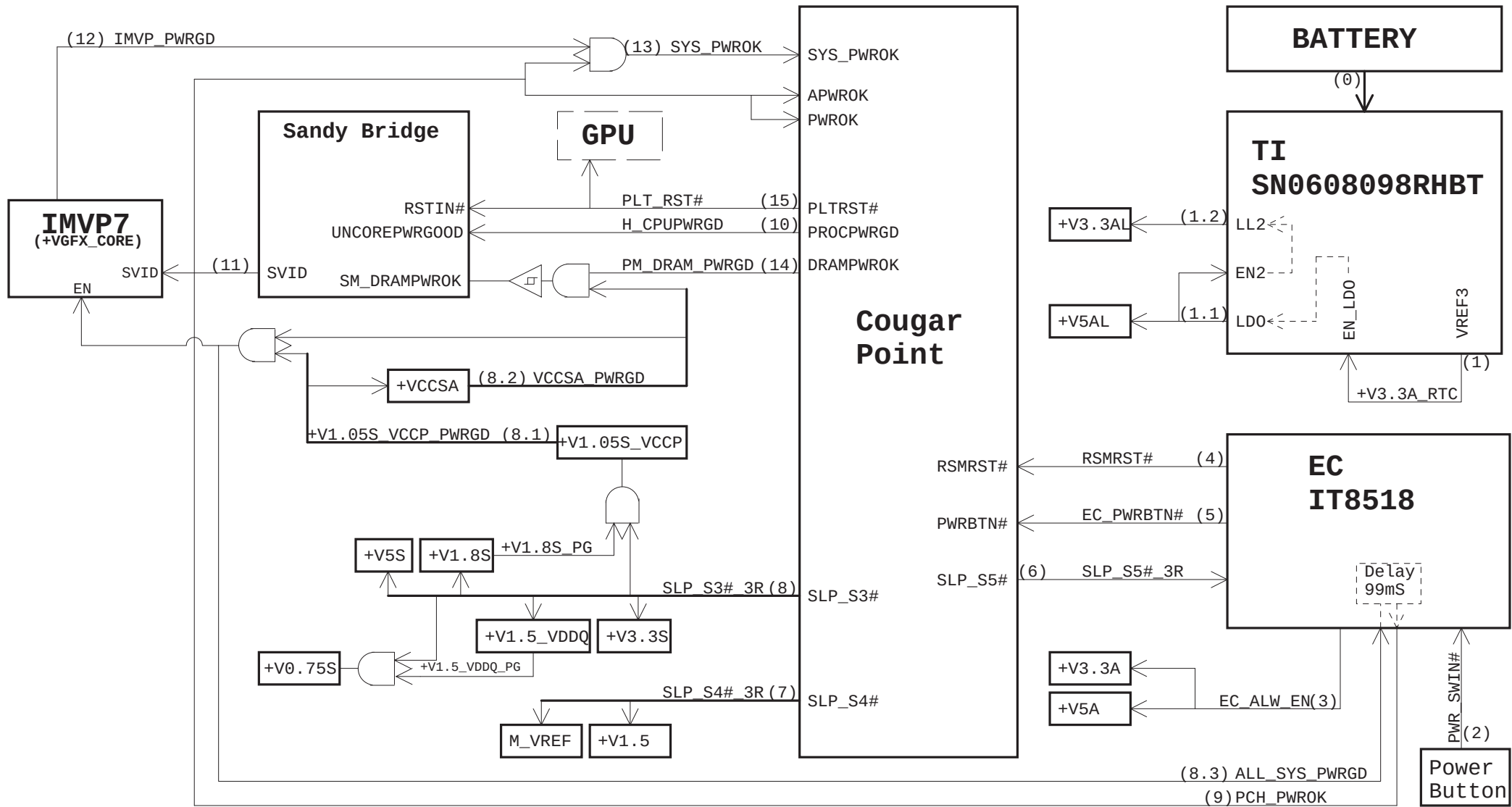
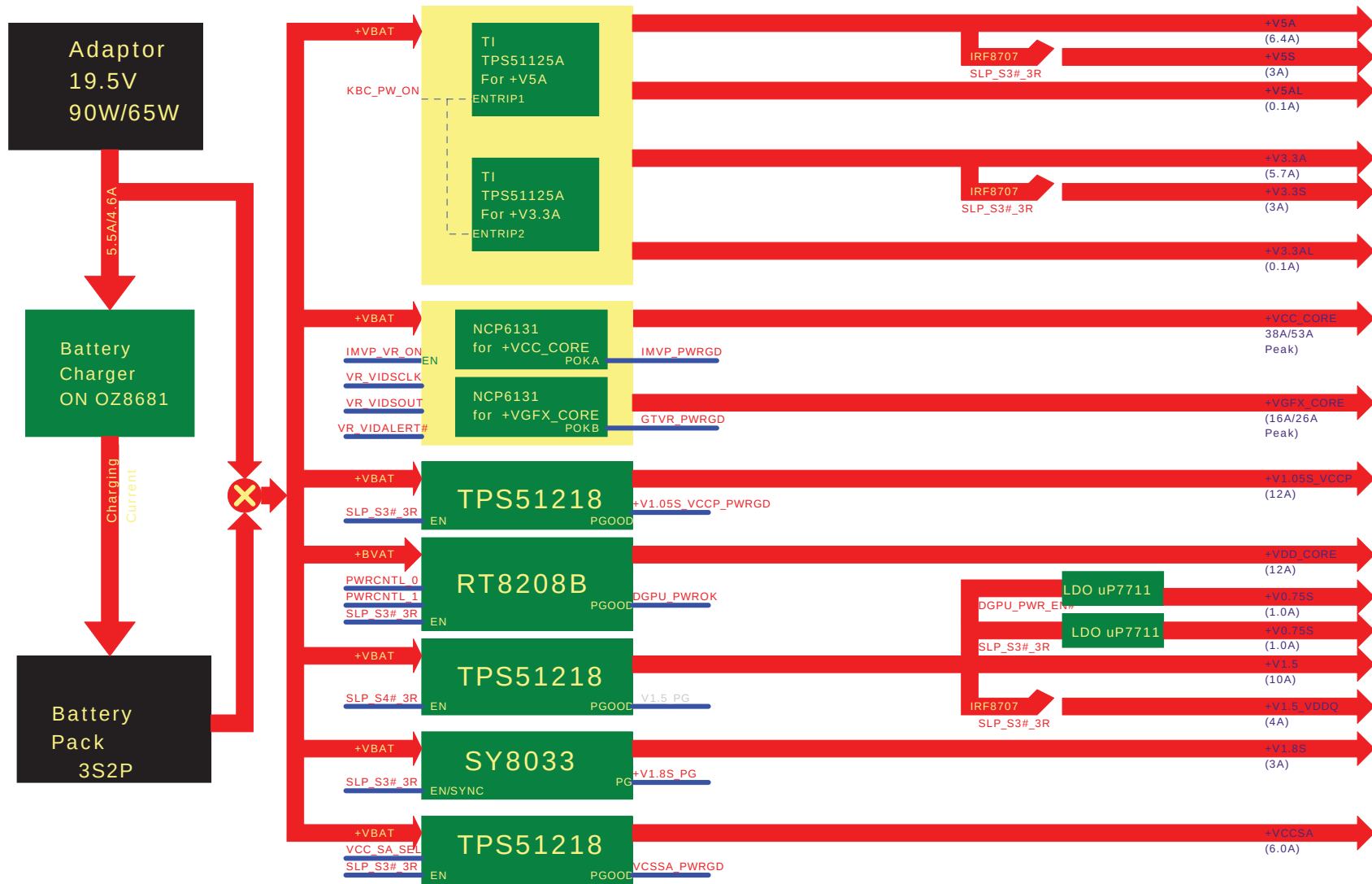


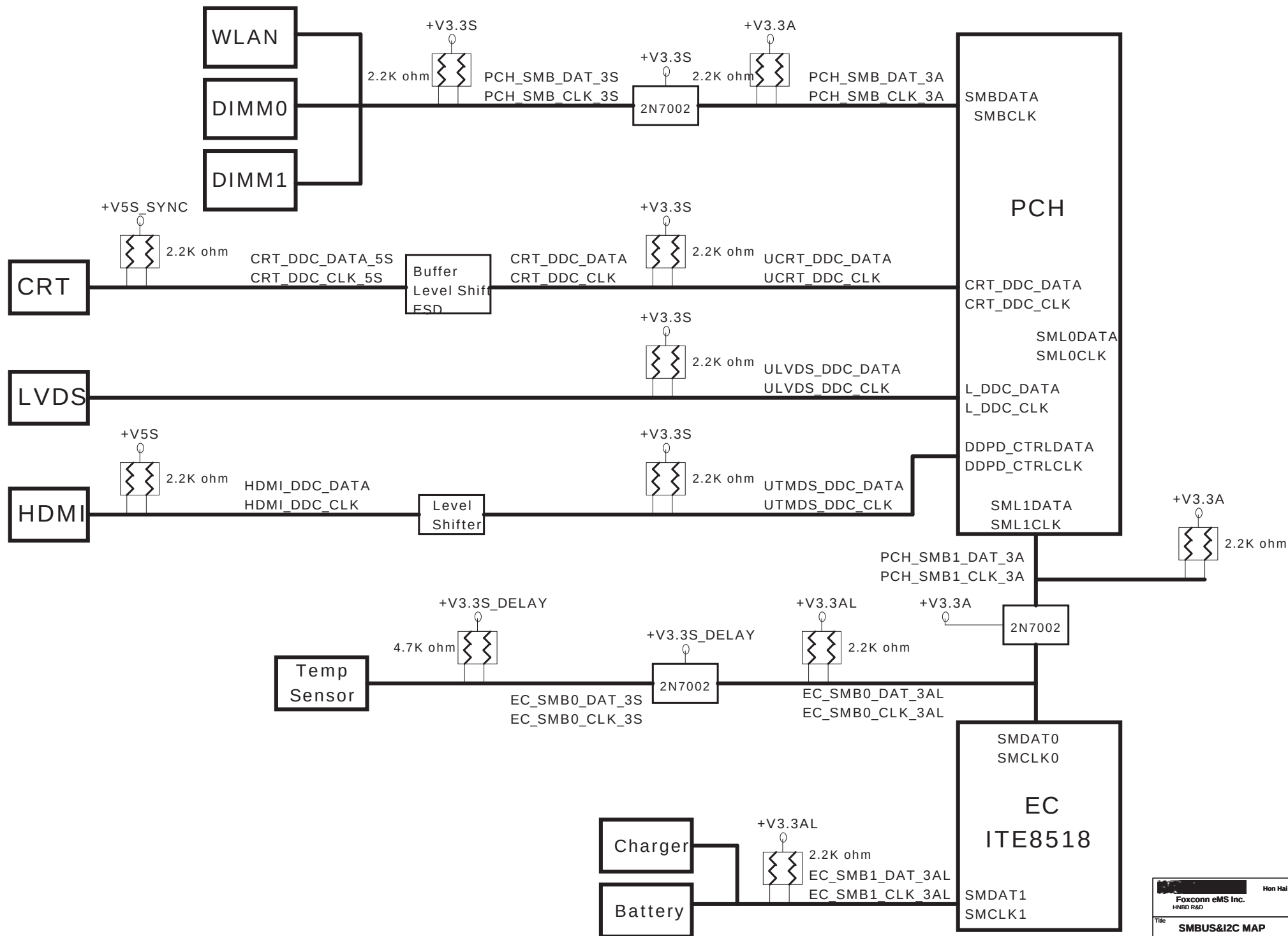






POWER MAP

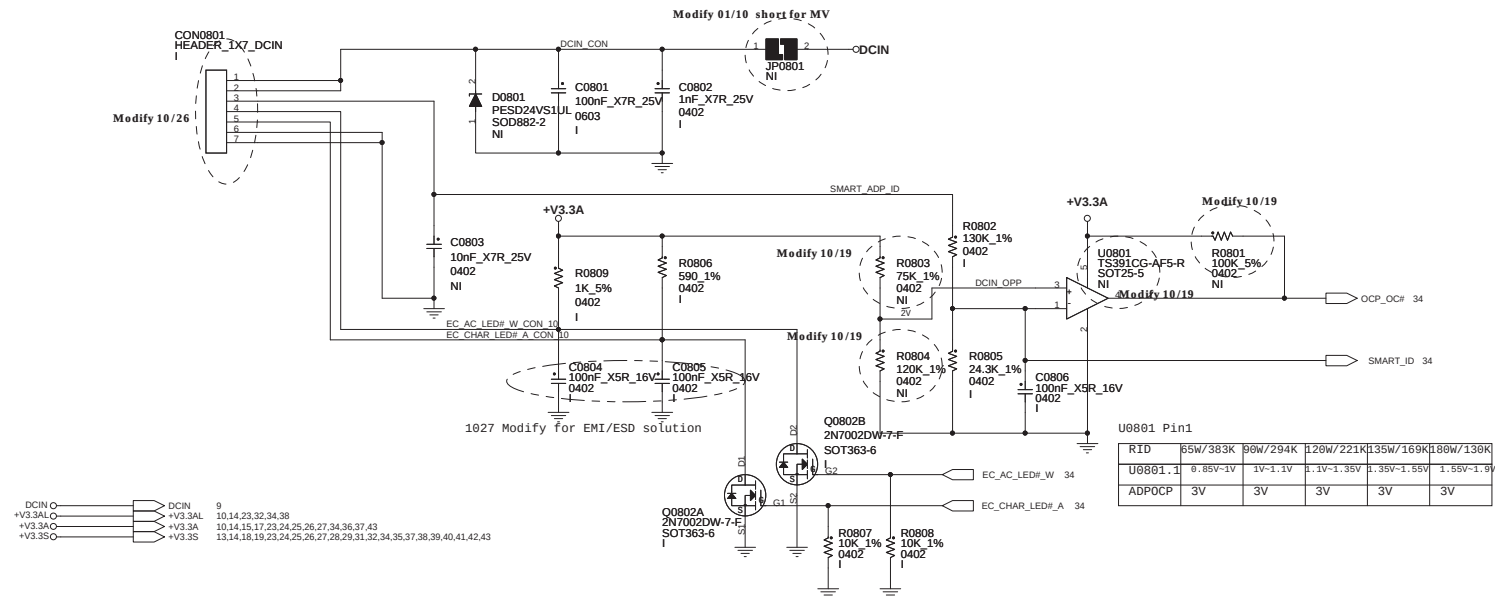




5					4					3					2					1				
D																								
C																								
B																								
A																								

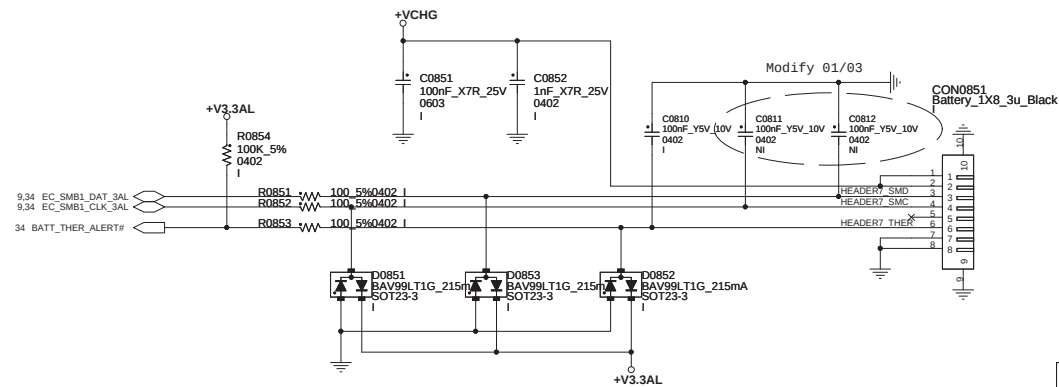
		Hon Hai Precision Industry Co. Ltd.	
Foxconn eMS Inc.			
HNBD R&D		phone: +886-2-2799-6111	
Title			
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Size	Document Number		Rev
A	CHICAGO		MV
Page Modified: Tuesday, March 08, 2011		08:28:58 (UTC/GMT)	Sheet 7 of 43

2010.1203.0

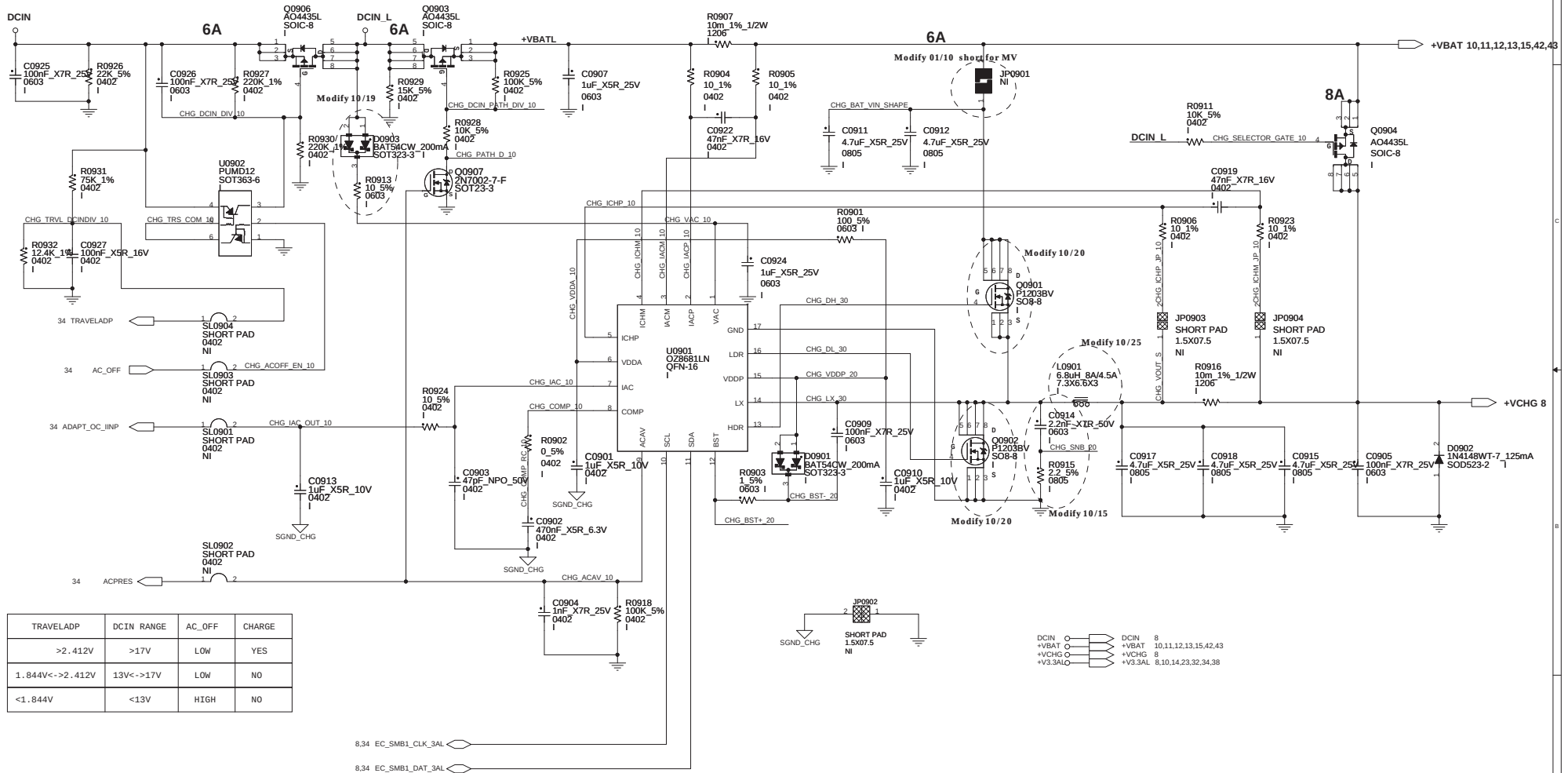


BATTERY CONNECTOR

2010.0914.0



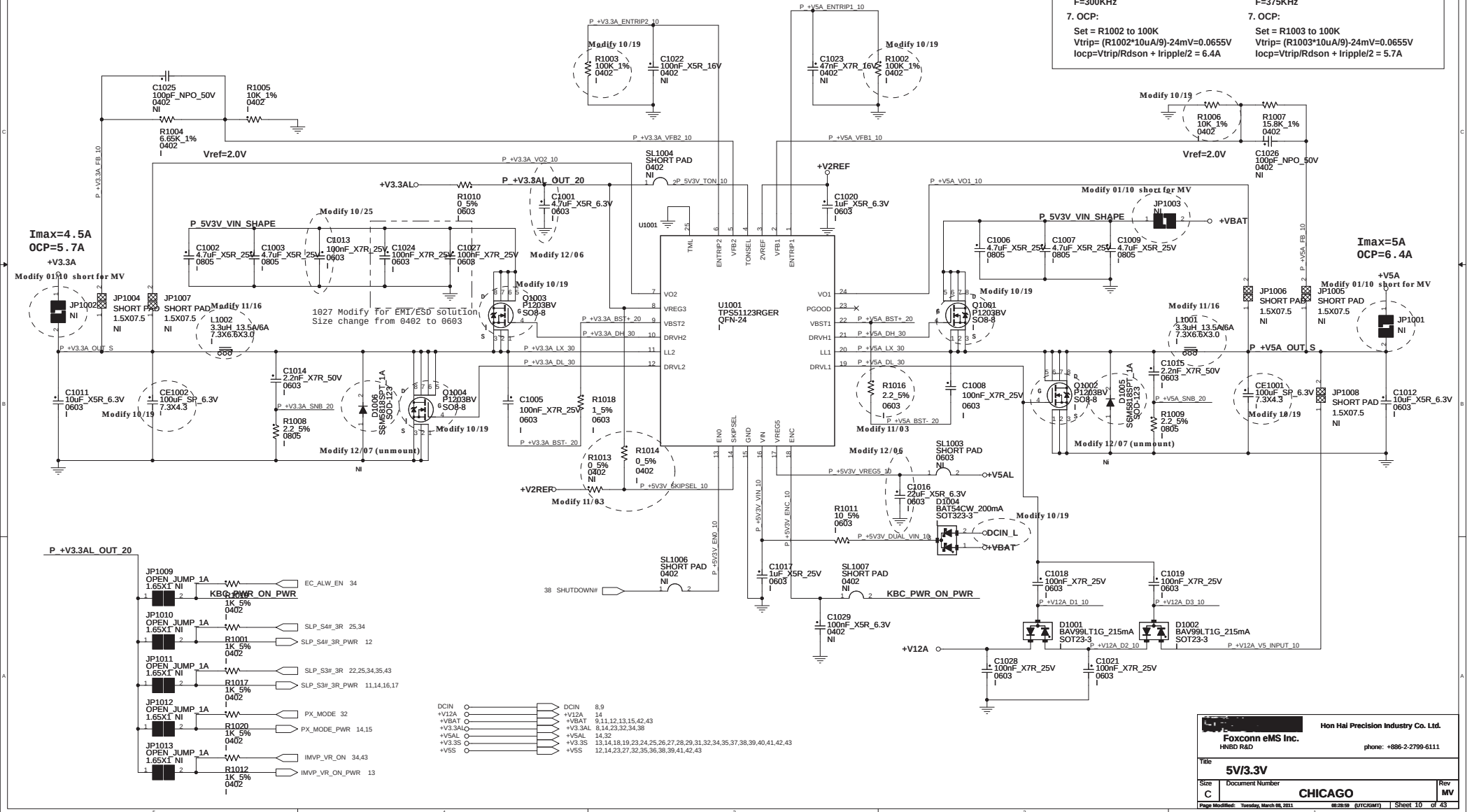
BATTERY CHARGER



+V5A / +V3.3A POWER SUPPLY

2010.1103.0

+V5A: 1. I/P Current: $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 3.7A$ 2. Ripple Current: $I_{rip} = 3.72A$ 3. Ripple Voltage: ESR/1=15mohm $V_{rip} = 55.8mV$ 4. Inductor Spec: Isat=13.5A Idc=6A DCR=30mohm 5. MOSFET Spec: H-side MOSFET: IRF8707PBF Rds(ON)=17.5mohm (Vgs=4.5 V) I cont = 11A (T=25 °C) I peak = 88A (Pause =10 us) 6. Frequency: F=300KHz 7. OCP: Set = R1002 to 100K $V_{trip} = (R1002 \cdot 10uA/9) - 24mV = 0.0655V$ $I_{ocp} = V_{trip} / R_{dson} + I_{ripple} / 2 = 6.4A$	+V3.3A: 1. I/P Current: $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 2.2A$ 2. Ripple Current: $I_{rip} = 2.21A$ 3. Ripple Voltage: ESR/1=15mohm $V_{rip} = 33.15mV$ 4. Inductor Spec: Isat=13.5A Idc=6A DCR=30mohm 5. MOSFET Spec: L-side MOSFET: IRF8707PBF Rds(ON)=17.5mohm (Vgs=4.5 V) I cont = 11A (T=25 °C) I peak = 88A (Pause =10 us) 6. Frequency: F=375KHz 7. OCP: Set = R1003 to 100K $V_{trip} = (R1003 \cdot 10uA/9) - 24mV = 0.0655V$ $I_{ocp} = V_{trip} / R_{dson} + I_{ripple} / 2 = 5.7A$
--	---

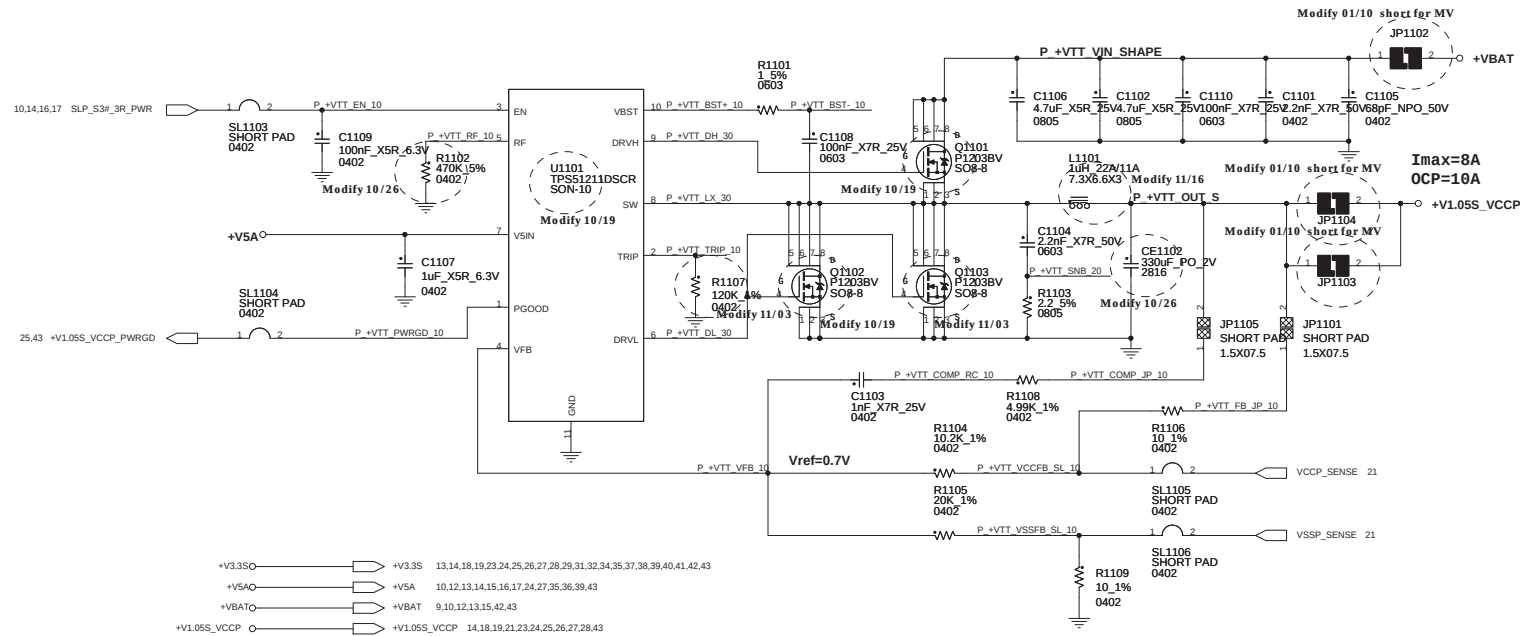


2010.1103.0

+V1.05S_VCCP:

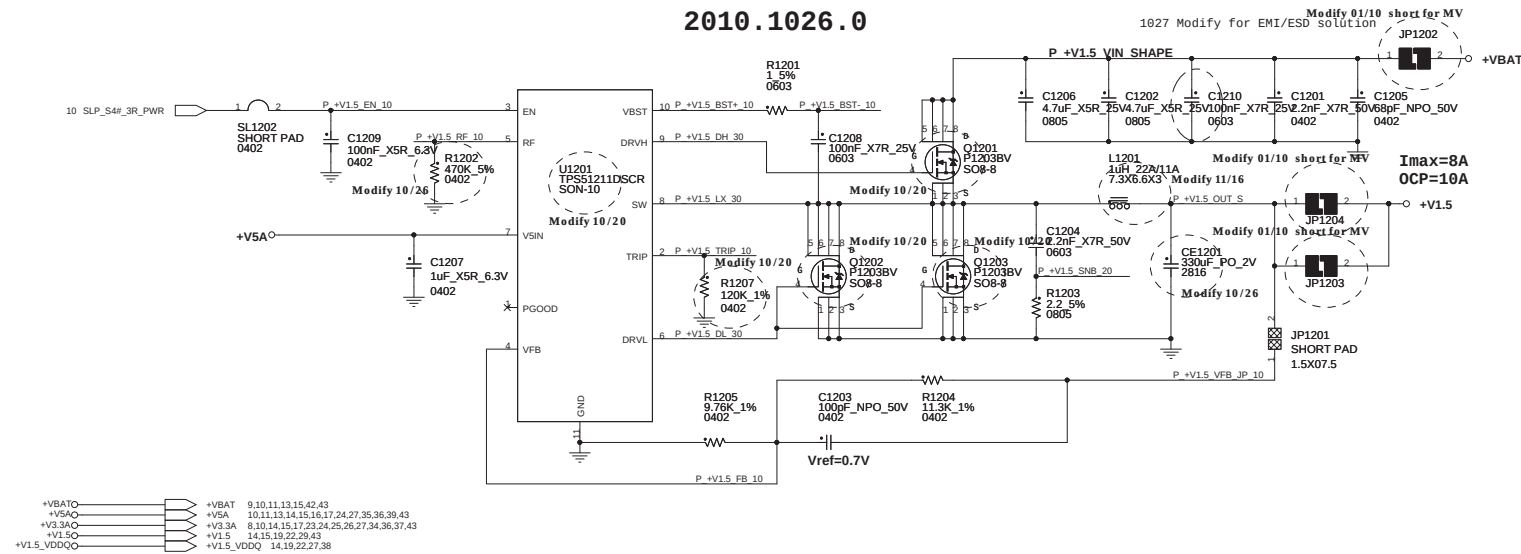
1. I/P Current:
 $I_{in} = V_o \cdot I_o / ((0.75 \cdot V_{in}) = 1.24A$
2. Ripple Current:
 $I_{rip} = 3.42A$
3. Ripple Voltage:
 $ESR/1 = 9m\Omega$
 $V_{rip} = 30.78mV$
4. Inductor Spec:
 $I_{sat} = 36A$
 $I_{dc} = 18A$
 $DCR = 3.3m\Omega$
5. MOSFET Spec:

H-side MOSFET: IRF8707PBF	L-side MOSFET: IRF8707PBF
$R_{ds}(ON) = 17.5m\Omega$ ($V_{gs} = 4.5V$)	$R_{ds}(ON) = 17.5m\Omega$ ($V_{gs} = 4.5V$)
$I_{cont} = 11A$ ($T = 25^\circ C$)	$I_{cont} = 11A$ ($T = 25^\circ C$)
$I_{peak} = 88A$ (Pause = 10 us)	$I_{peak} = 88A$ (Pause = 10 us)
6. Frequency:
 $F = 290KHz$ ($R_{1102} = 0\Omega$)
7. OCP:
 $Set = R_{1107} \text{ to } 120K$
 $V_{trip} = R_{1107} \cdot I_{Oa} \cdot 1.2V$
 $I_{ocp} = (V_{trip} / 8 \cdot R_{dson}) + I_{ripple} / 2 = 10A$

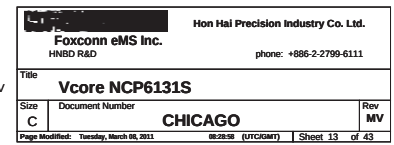


+V1.5 POWER SUPPLY

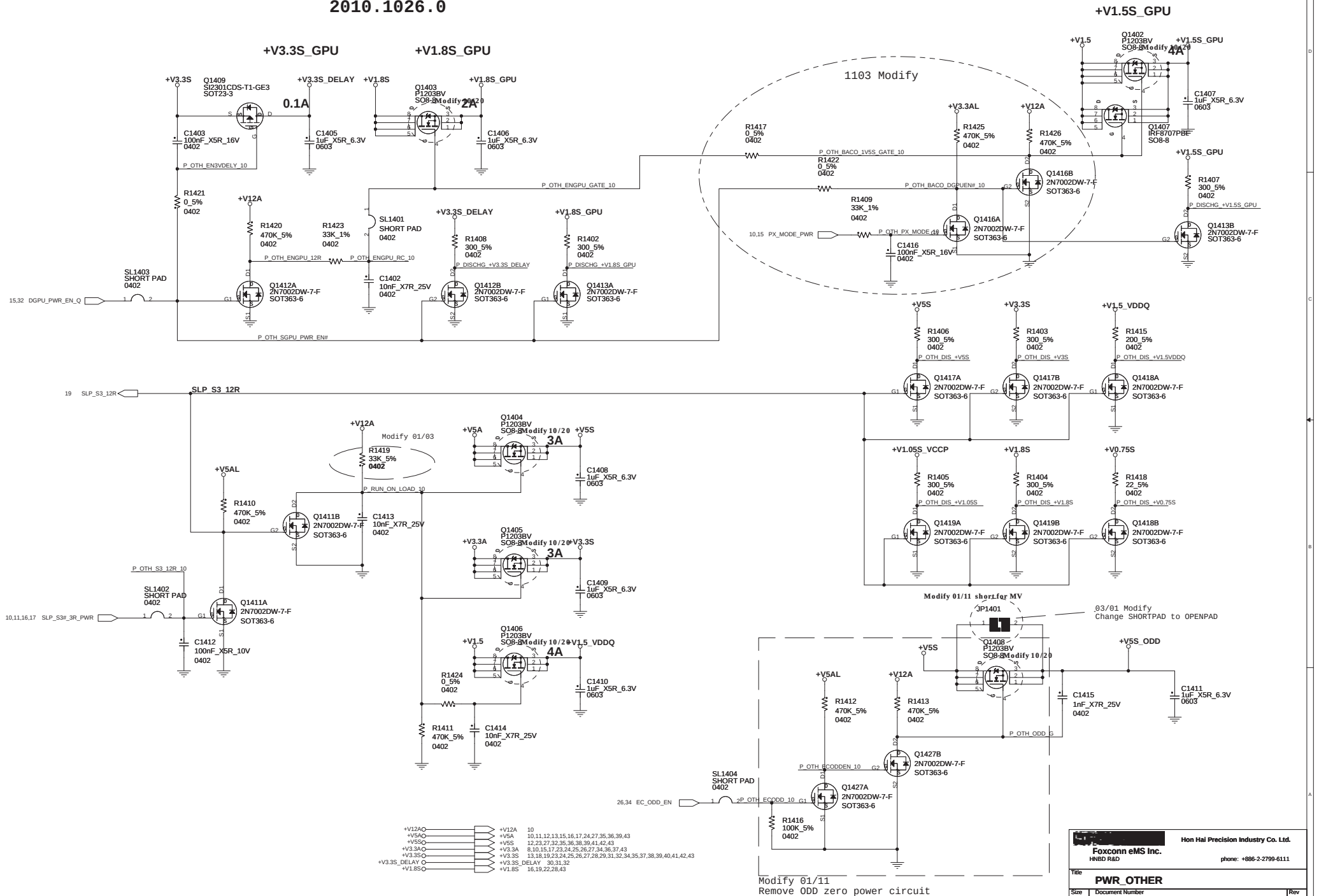
2010.1026.0



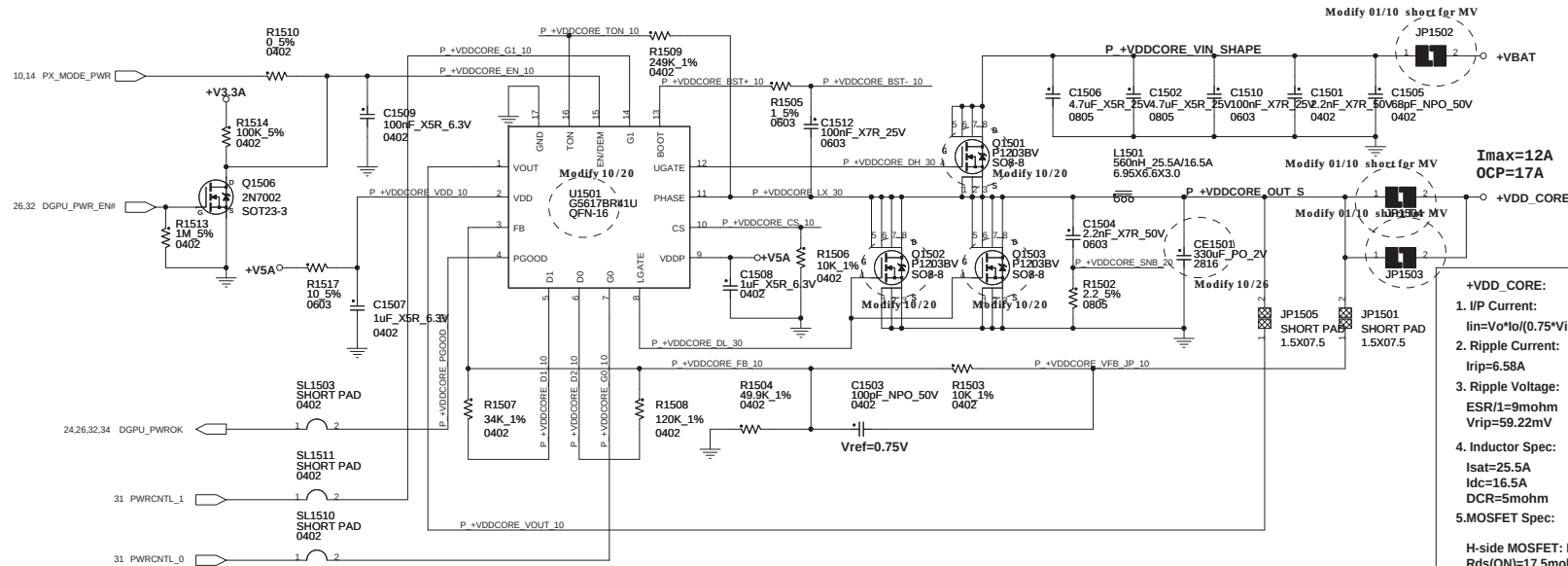
IMVP7 CPU VCORE POWER SUPPLY



2010.1026.0



2010.1026.0

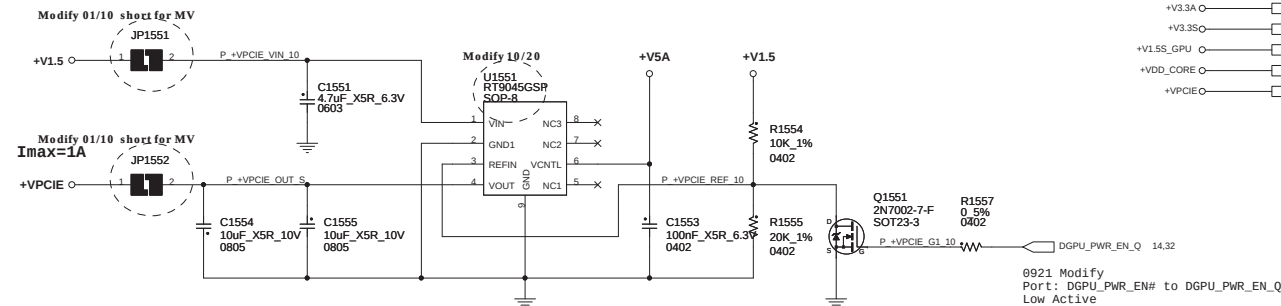


PWRCNTL_1	PWRCNTL_0	VDD_CORE
0	---	1.121V
---	---	---
1	---	0.9V
---	---	---

+VDD_CORE:

1. I/P Current:
lin=Vo*Io/(0.75*Vin)=1.48A
2. Ripple Current:
Irip=6.58A
3. Ripple Voltage:
ESR/1=9mohm
Vrip=59.22mV
4. Inductor Spec:
Isat=25.5A
Idc=16.5A
DCR=5mohm
5. MOSFET Spec:
- | | |
|------------------------------|------------------------------|
| H-side MOSFET: IRF8707PBF | L-side MOSFET: IRF8707PBF |
| Rds(ON)=17.5mohm (Vgs=4.5 V) | Rds(ON)=17.5mohm (Vgs=4.5 V) |
| I cont = 11A (T =25 °C) | I cont = 11A (T =25 °C) |
| I peak = 88A (Pause =10 us) | I peak = 88A (Pause =10 us) |
6. Frequency:
TON=9.6P*R1509*(VOUT+0.1) / (VIN-0.3)+50ns=206ns
F=VOUT/(VIN*TON)=286KHz
7. OCP:
Set = R1506 to 10K
Vtrip= R1206*10uA=0.1V
Iocp=(Vtrip/Rdson) + Iripple/2 = 17A

2010.1020.0 +VPCIE POWER SUPPLY



+VBATO		+VBAT	9.10.11.12.13.42.43
+V5AC		+V5A	10.11.12.13.14.16.17.24.27.35.36.39.43
+V2.3A		+V3.3A	8.10.14.17.23.24.25.26.27.34.36.37.43
+V3.3SC		+V3.3S	13.14.18.19.23.24.25.26.27.28.29.31.32.34.35.37.38.39.40.41.42.43
+V1_SS_GPU		+V1_SS_GPU	14.30.32.33.43
+VDD_CORE		+VDD_CORE	32.43
+VPCIEC		+VPCIE	30.31.32.43

```
0921 Modify
Port: DGPU_PWR_EN# to DGPU_PWR_EN_Q
Low Active
```

+V1.8S POWER SUPPLY

2010.1025.0

+V1.8S:

1. I/P Current:

$$I_{in} = V_o * I_o / (0.75 * V_{in}) = 1.44A$$

2. Ripple Current:

$$I_{rip} = 0.53A$$

3. Ripple Voltage:

$$ESR/3 = 3.3m\Omega$$

$$V_{rip} = 1.75mV$$

4. Inductor Spec:

$$I_{sat} = 14A$$

$$I_{dc} = 8A$$

$$DCR = 20m\Omega$$

5. MOSFET Spec:

H-side P-MOSFET:

L-side N-MOSFET:

$$R_{ds(ON)} = 110m\Omega \quad (V_{gs} = 4.5V)$$

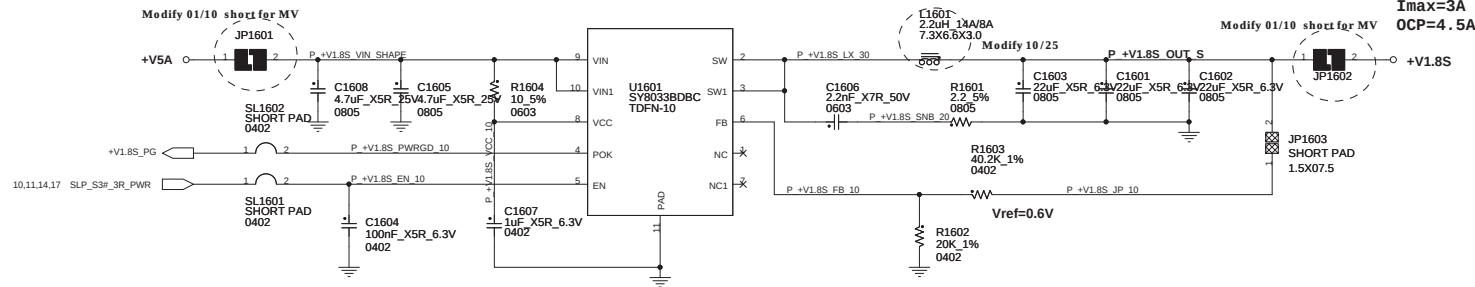
$$R_{ds(ON)} = 75m\Omega \quad (V_{gs} = 4.5V)$$

6. Frequency:

$$F = 1MHz \quad (\min = 800KHz, \max = 1.2MHz)$$

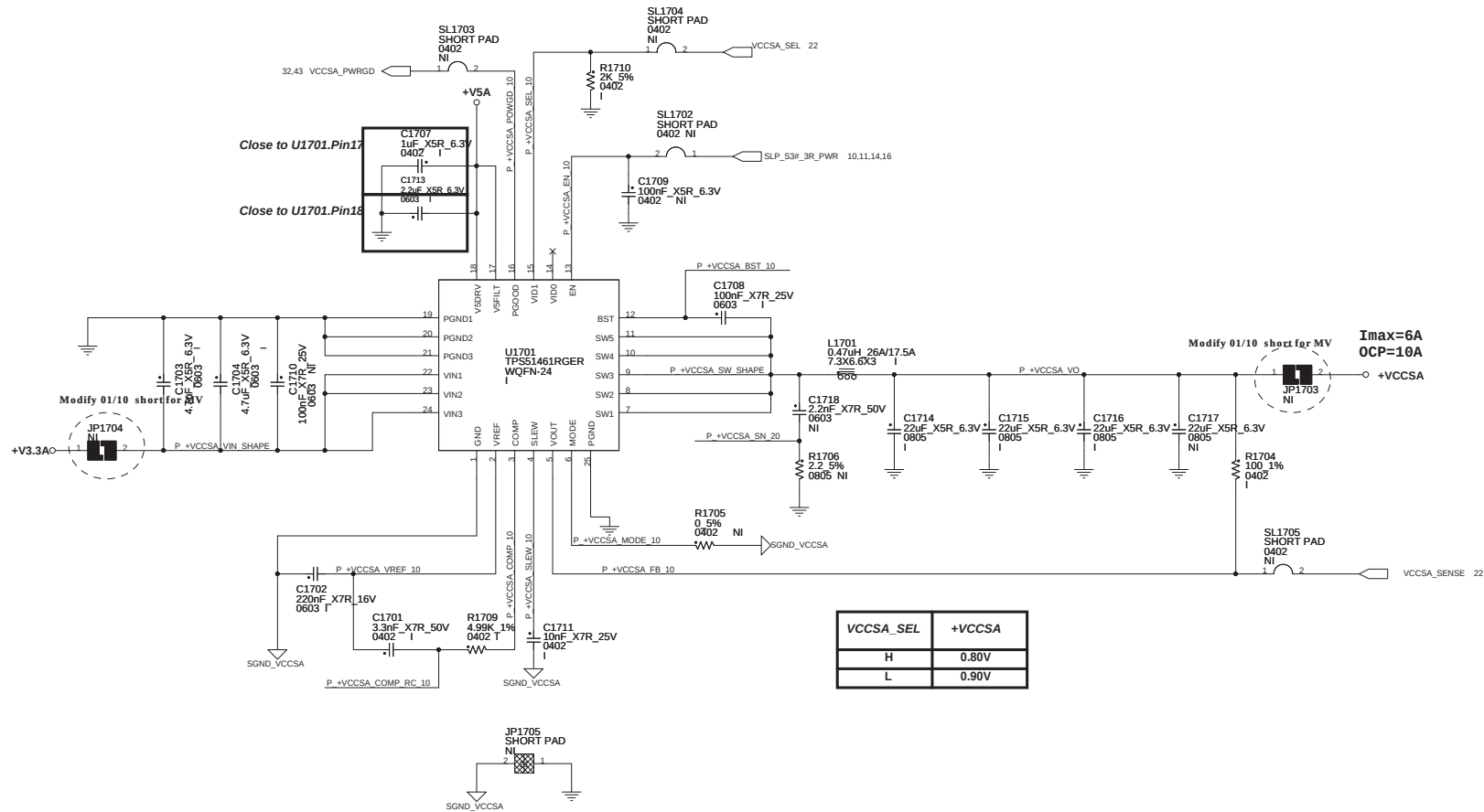
7. OCP:

$$I_{ocp} = 4A(\min) / 4.5A(\text{typ}) / 5A(\max)$$



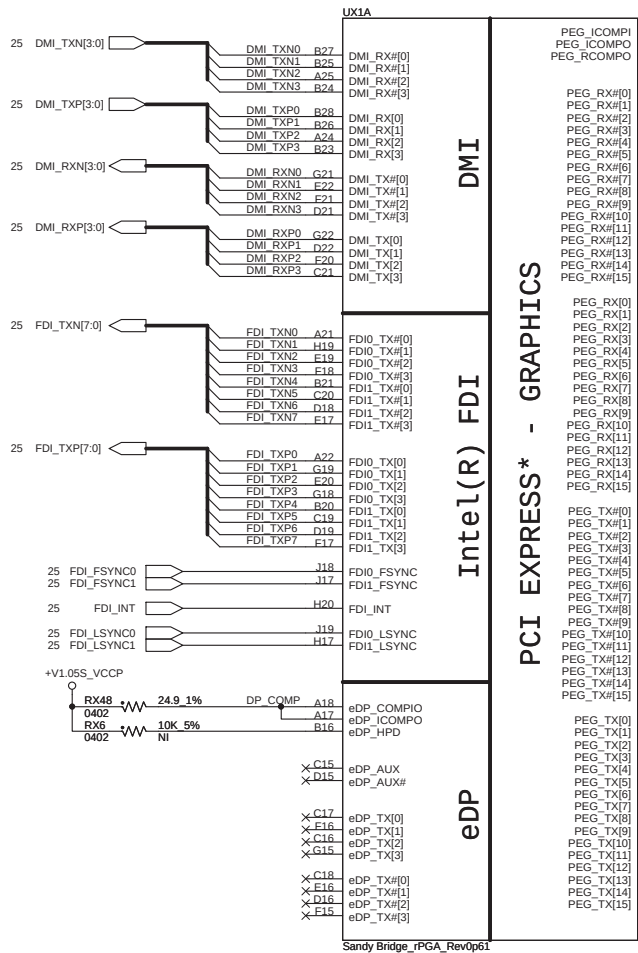
+VCCSA POWER SUPPLY

2010.1026.0

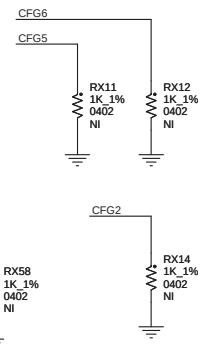
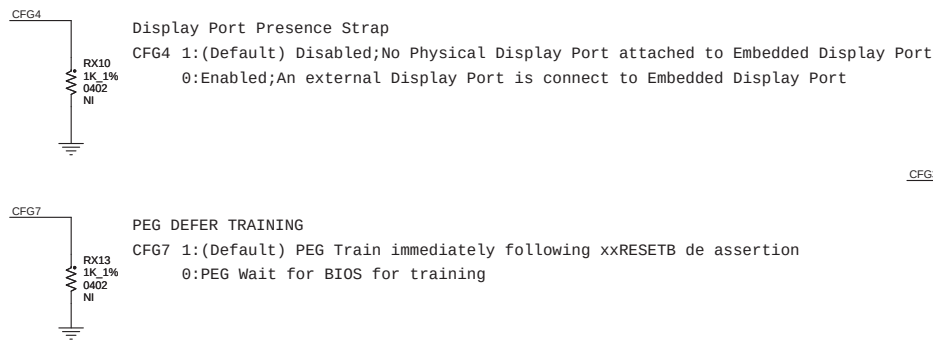
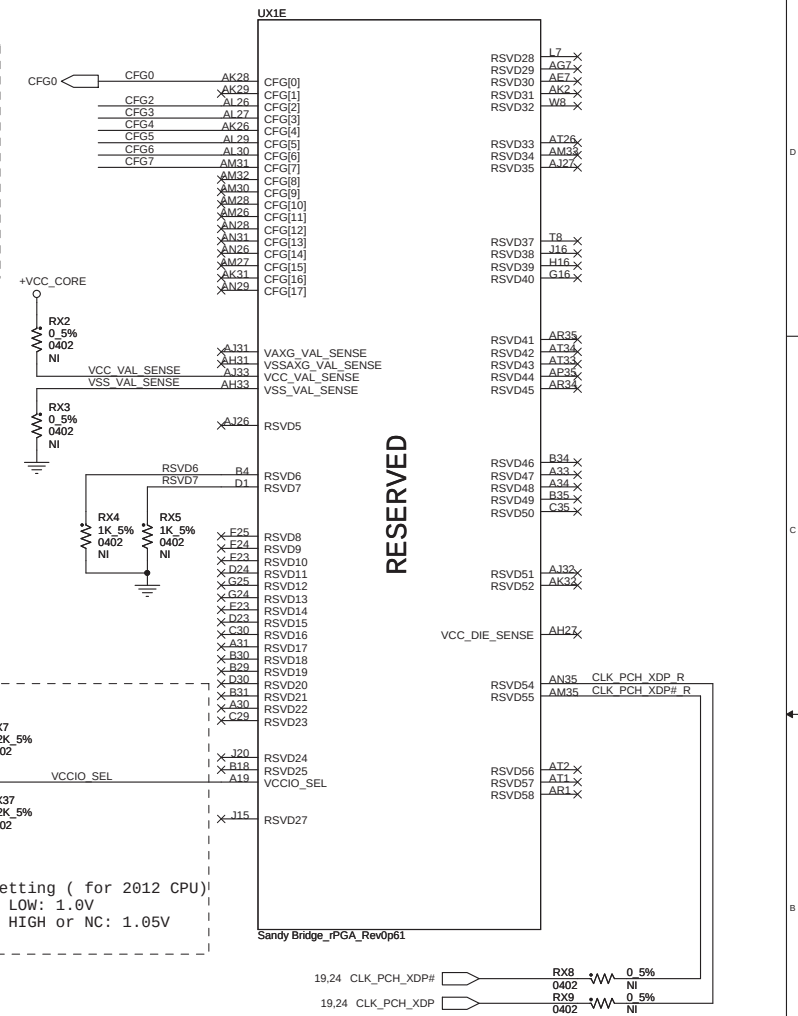
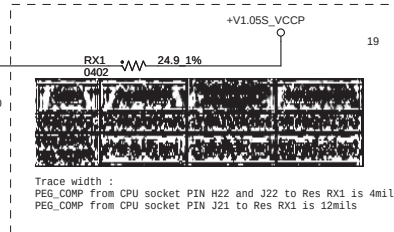
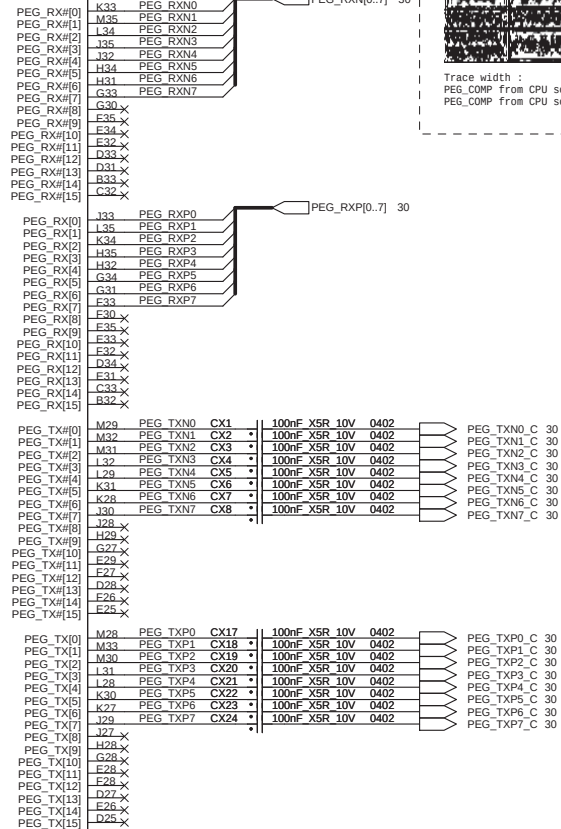


- +VCCSA:**
1. I/P Current:
 $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 2.18A$
 2. Ripple Current:
 $I_{rip} = 1.39A$
 3. Ripple Voltage:
 $ESR/4 = 1m\Omega$
 $V_{rip} = 1.39mV$
 4. Inductor Spec:
 $I_{sat} = 26A$
 $I_{dc} = 17.5A$
 $DCR = 4.2m\Omega$
 5. MOSFET Spec:
 6. Frequency:
 $F = 1MHz$ (R1705=Open)
 7. OCP:
Min : 6A / Typ : 7.5A

+V3.3S0 —————> +V3.3S 13,14,19,23,24,25,26,27,28,29,31,32,34,35,37,38,39,40,41,42,43
+V1.05S_VCCP —————> +V1.05S_VCCP 11,14,19,21,23,24,25,26,27,28,43



PCI EXPRESS * - GRAPHICS



PCIe Port Bifurcation Straps

CFG[6:5] 11:(Default) x16 - Device 1 functions & 2 disabled
10:x8,x8 - Device 1 function 1 enabled ; function 2 disabled
01:Reserved - (Device 1 function 1 disabled ; function 2 enabled
00:x8,x4,x4 - (Device 1 functions 1 & 2 enabled

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Title

PROCESSOR(1 of 5)

Size

Document Number

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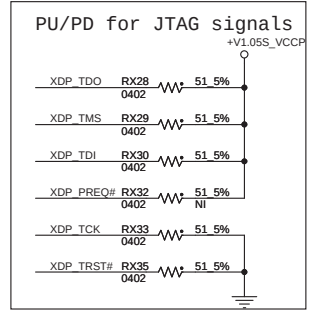
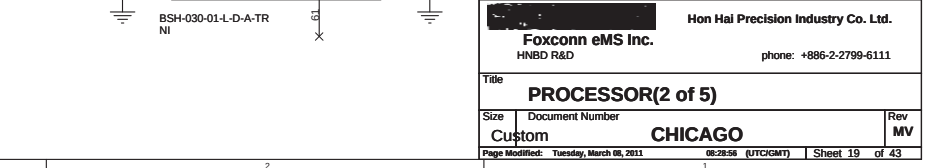
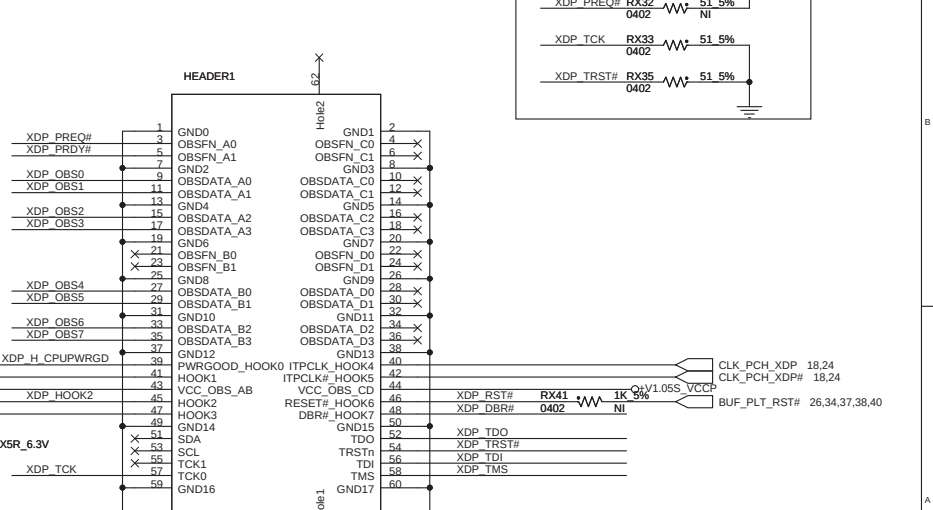
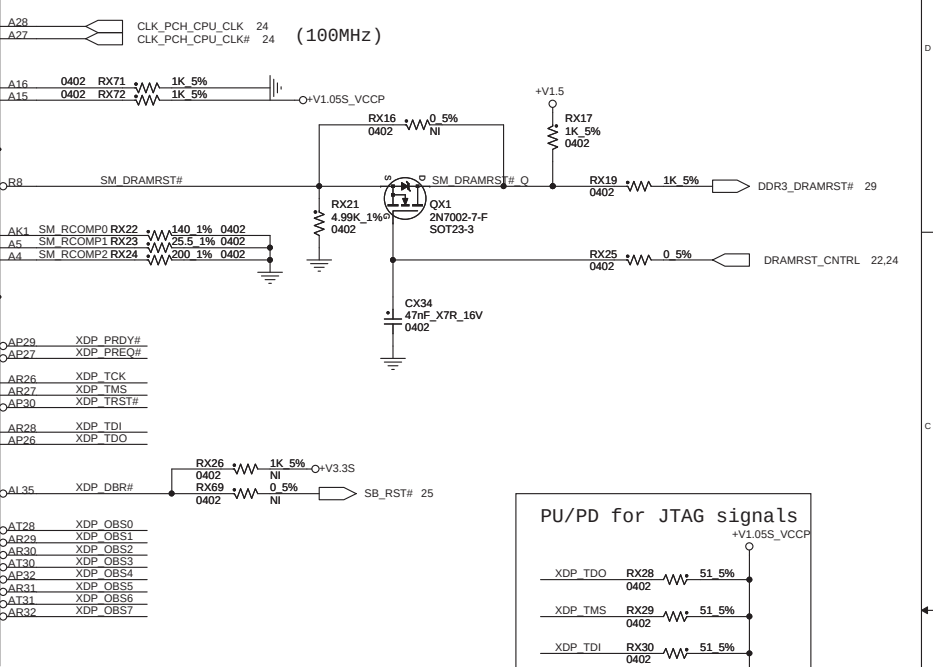
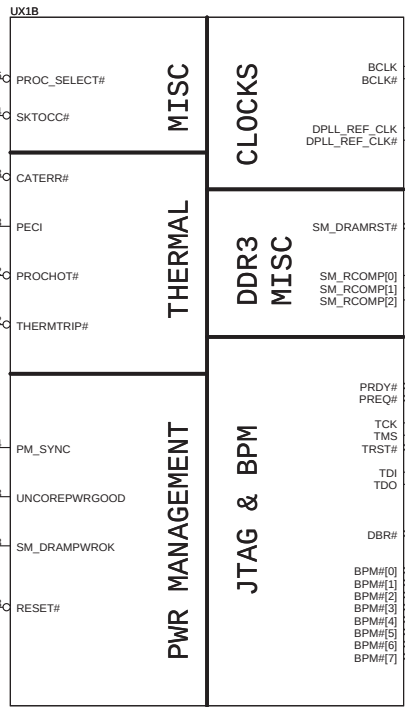
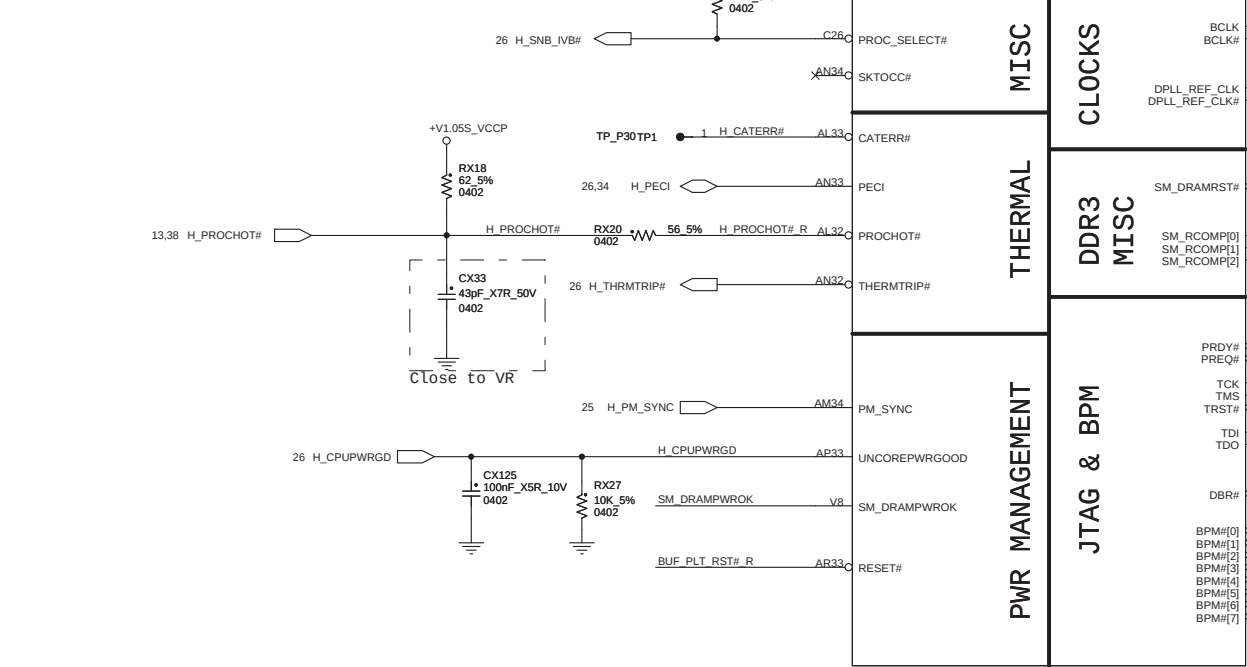
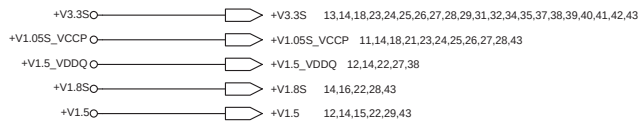
Rev

MV

Page Modified: Tuesday, March 06, 2011

08:29:01 (UTC+GMT)

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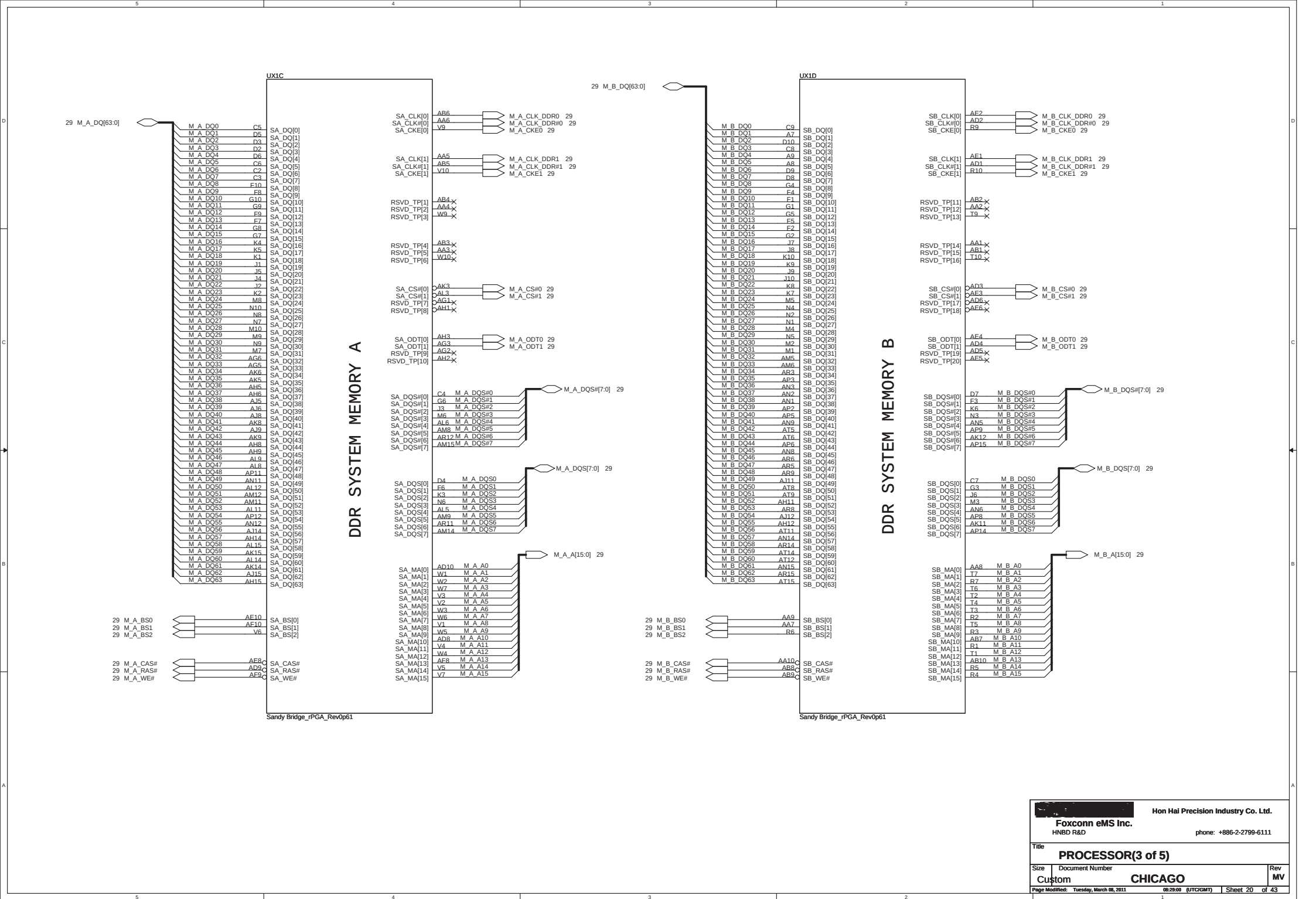
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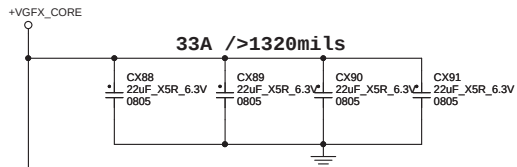
Hon Hai Precision Industry Co. Ltd.

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Size: Document Number
Custom **CHICAGO** Rev **MV**

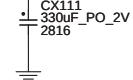
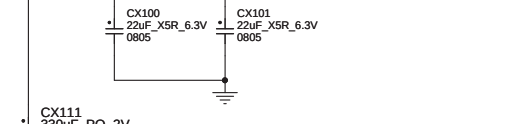
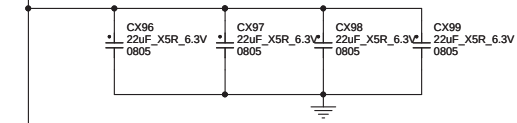
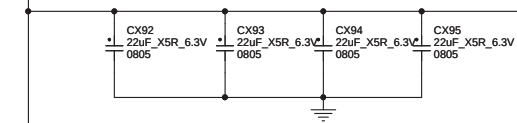
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FOR VAXG:
 2x 330 μ F Bottom Edge,
 4x 0805 22 μ F Top & Bottom Cavity,
 8x 0805 22 μ F Top & Bottom Edge,

POWER



UX1G

VAXG1
VAXG2
VAXG3
VAXG4
VAXG5
VAXG6
VAXG7
VAXG8
VAXG9
VAXG10
VAXG11
VAXG12
VAXG13
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VAXG52
VAXG53
VAXG54

GRAPHICS

SENSE LINES

VREF

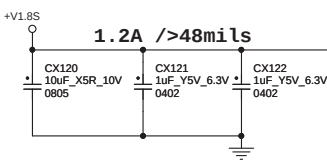
DDR3 -1.5V RAILS

SA RAIL

MISC

1.8V RAIL

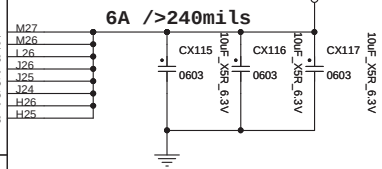
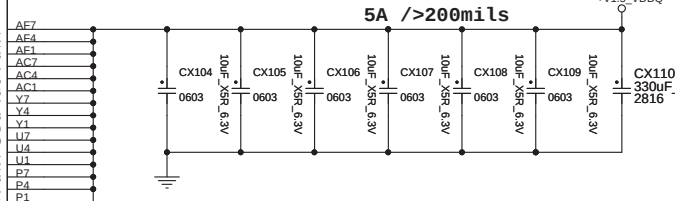
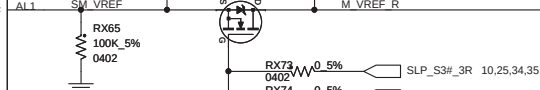
Sandy Bridge_rPGA_Rev0p61



FOR VCCPLL:
 1x 330 μ F Bottom Edge,
 2x 0402 1 μ F Bottom Edge,
 1x 0805 10 μ F Bottom Edge,

+VCCSAO $\rightarrow$ +VCCSA 17
 +V1.8SQ $\rightarrow$ +V1.8S 14,16,19,28,43
 +V1.5O $\rightarrow$ +V1.5 12,14,15,19,29,43
 +V1.5_VDDQO $\rightarrow$ +V1.5_VDDQ 12,14,19,27,38
 +VGFX_COREO $\rightarrow$ +VGFX_CORE 13,43

AK35 $\rightarrow$ GFX_VCC_SENSE 13
 AK34 $\rightarrow$ GFX_VSS_SENSE 13



VCCSA1
VCCSA2
VCCSA3
VCCSA4
VCCSA5
VCCSA6
VCCSA7
VCCSA8

VCCSA_SENSE 17
 FC_C22
 VCCSA_VID1

H_FC_C22
 VCCSA_SEL 17

RX67 10K 5%
 RX68 10K 5%

UX1I

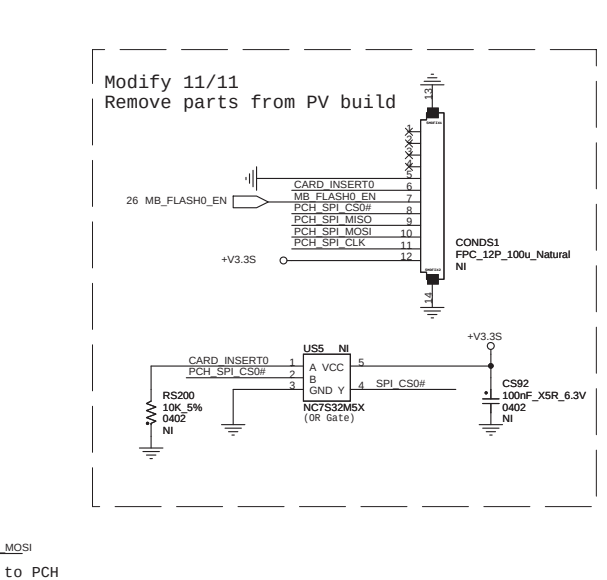
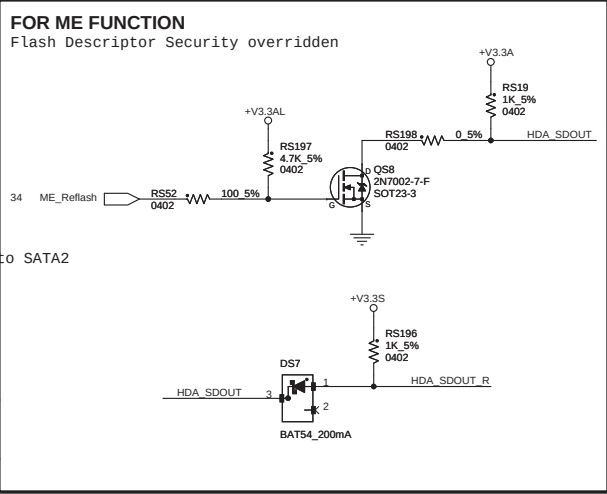
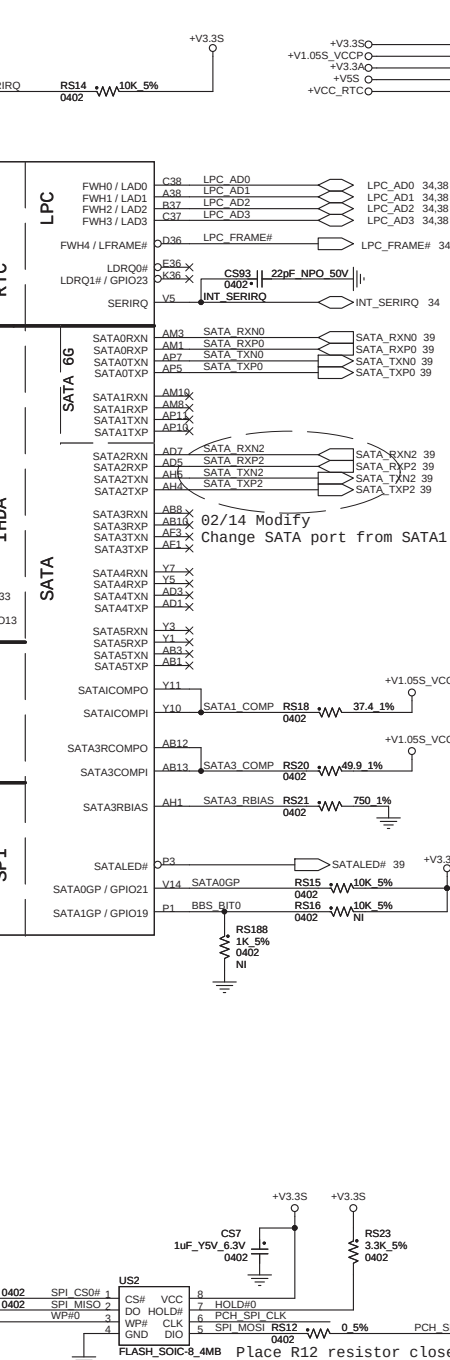
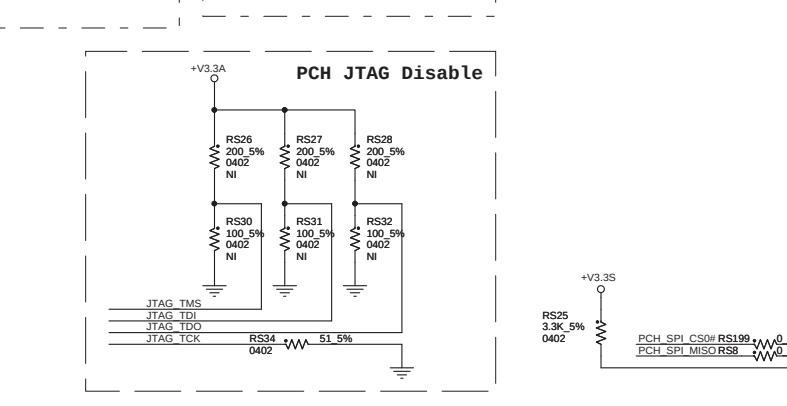
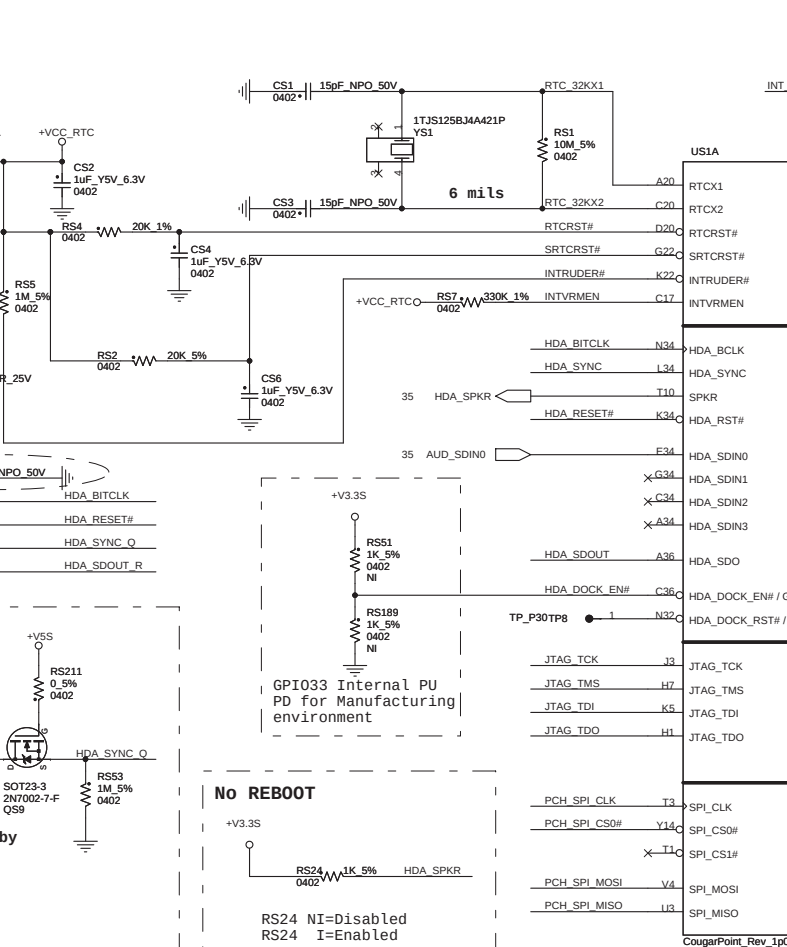
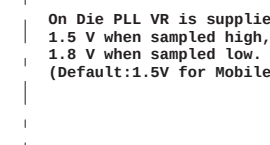
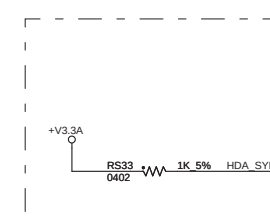
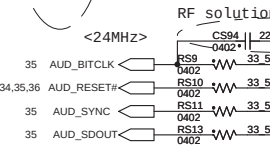
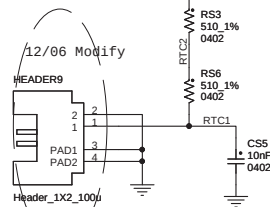
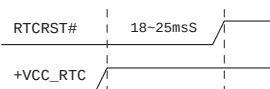
VSS161
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VSS233

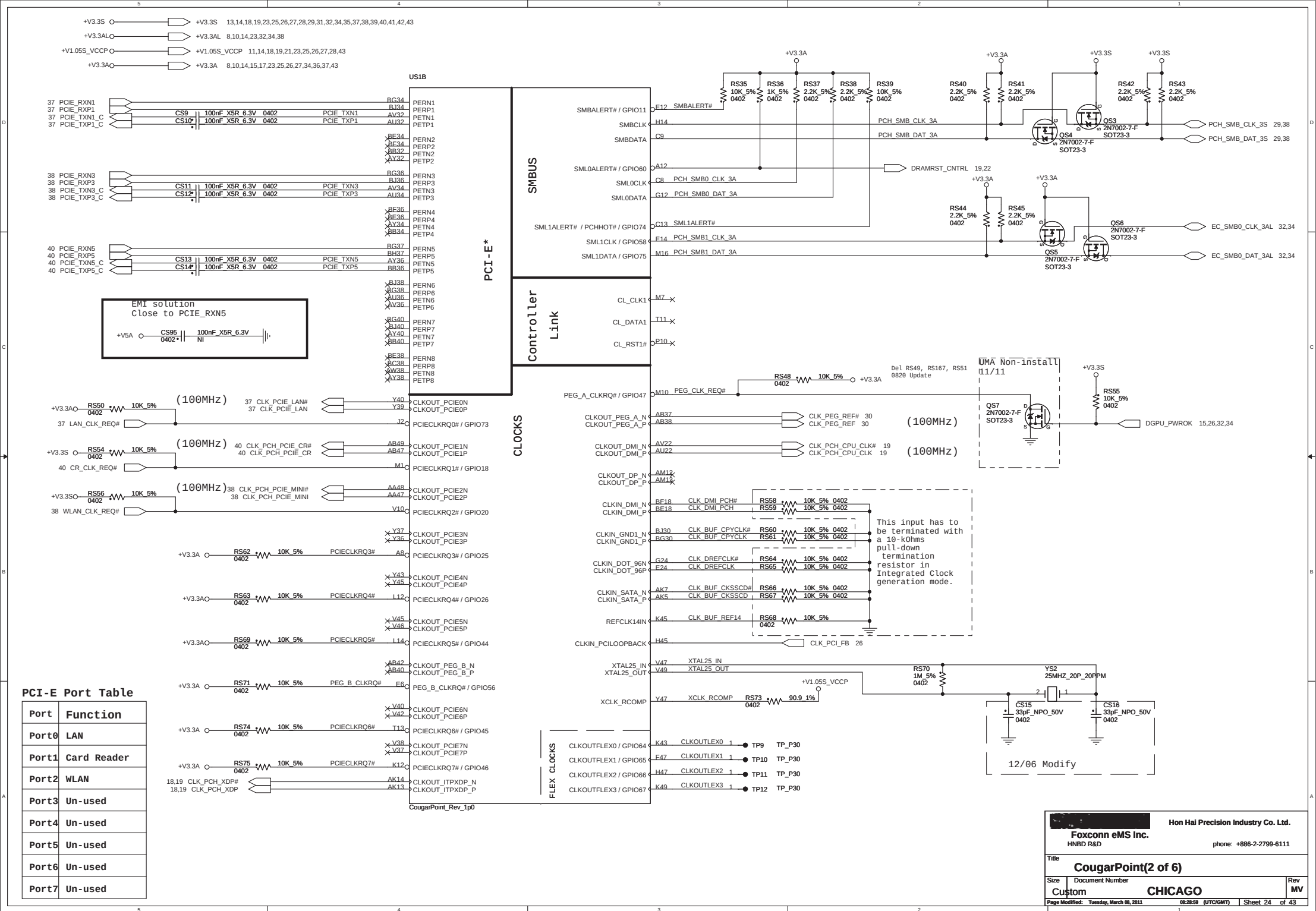
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VSS235
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VSS285

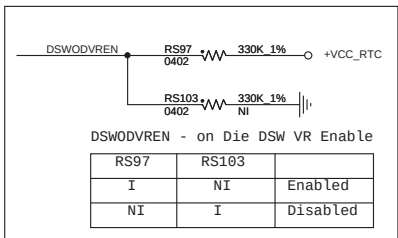
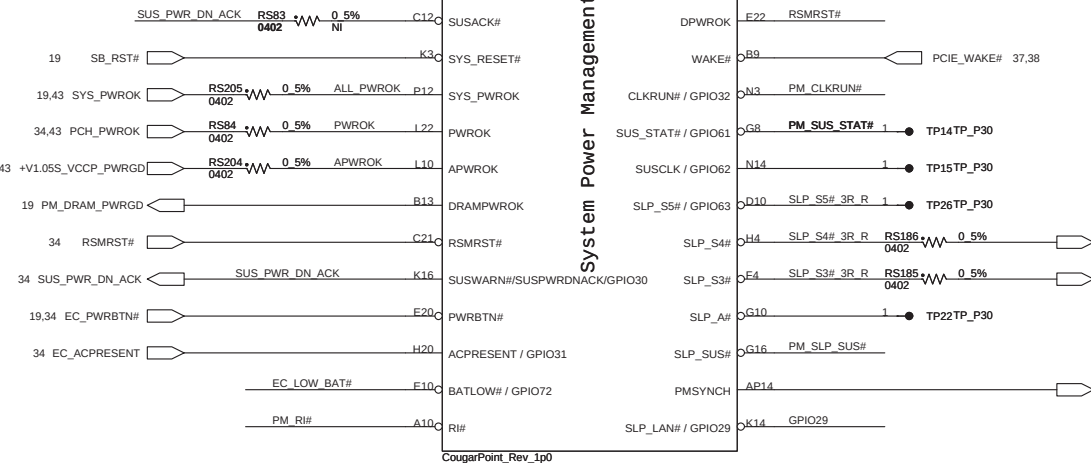
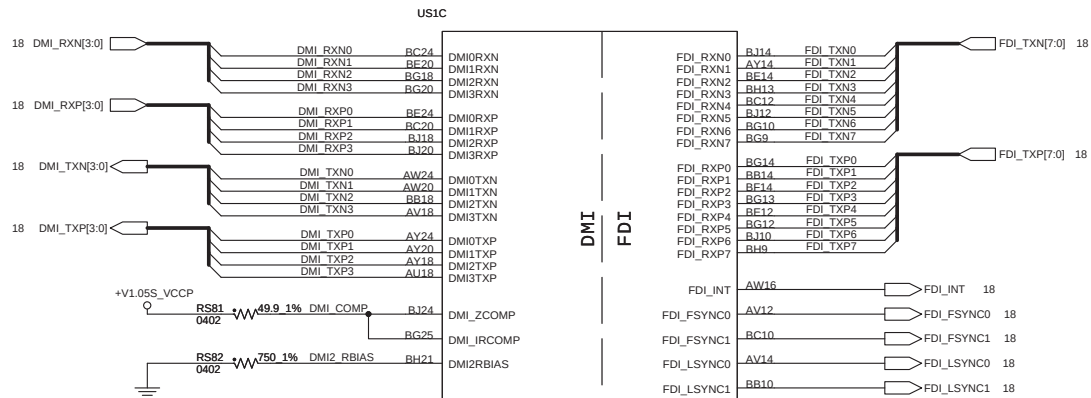
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F2
F1
D35
D32
D29
D26
D20
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B5
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A3

VSS

Sandy Bridge_rPGA_Rev0p61

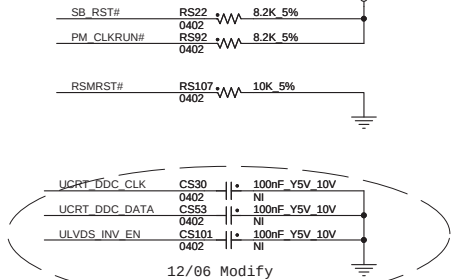




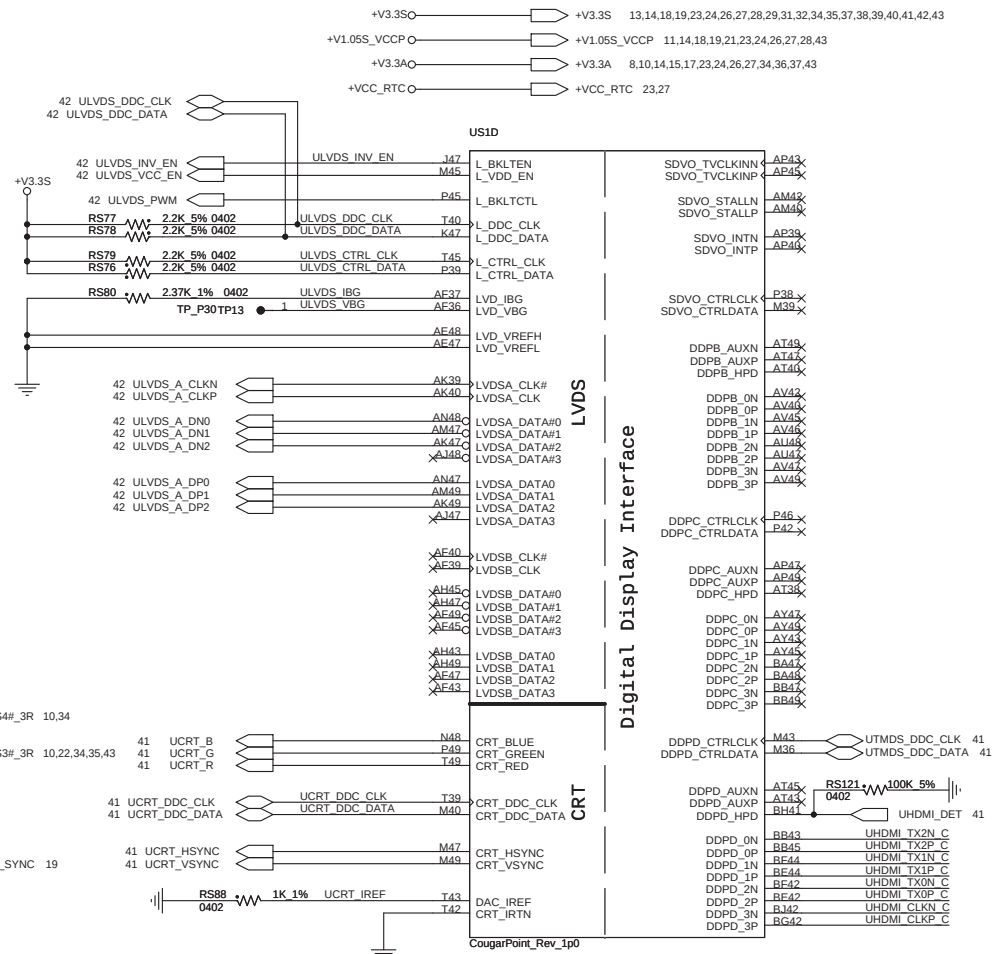


System Power Management

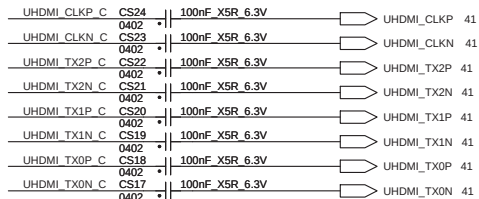
CougarPoint_Rev_1p0



Modify CS30/CS53/CS101 to non-stuff on 01/11



Digital Display Interface



Foxconn eMS Inc. Hon Hai Precision Industry Co. Ltd.

HNBD R&D phone: +886-2-2799-6111

Title: CougarPoint(3 of 6)

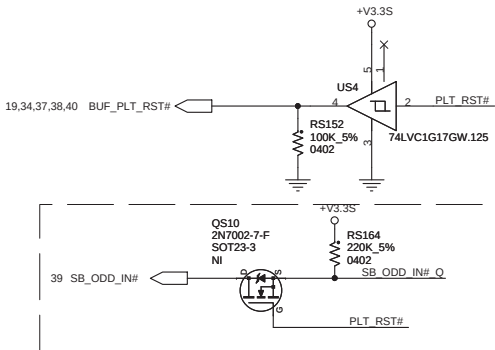
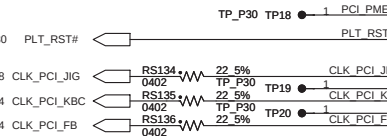
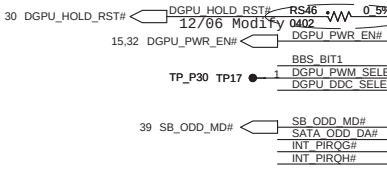
Size: Document Number Custom CHICAGO Rev: MV

Page Modified: Tuesday, March 08, 2011 08:29:00 (UTC+GMT) Sheet 25 of 43

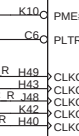
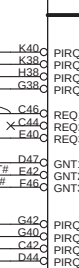
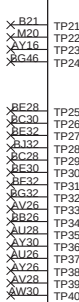
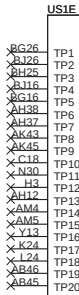
Boot BIOS Strap		
BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI



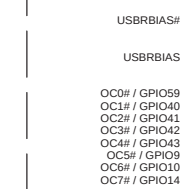
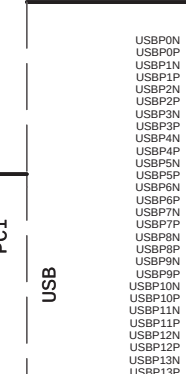
Del RS121 8.2Kohm to +V3.3S
0820 Update



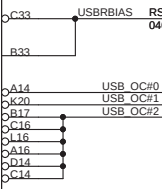
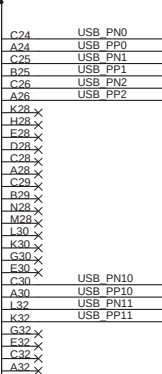
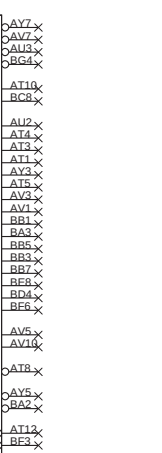
02/24 Modify
same as the PV build



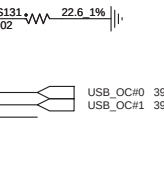
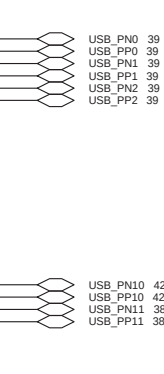
CougarPoint_Rev_1p0



CougarPoint_Rev_1p0



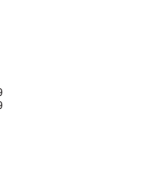
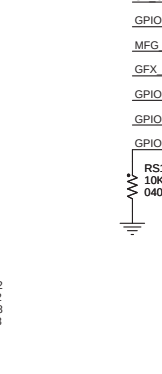
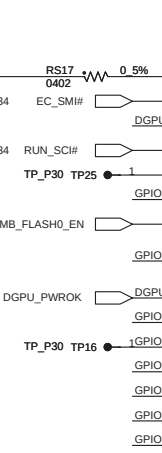
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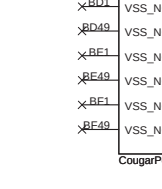
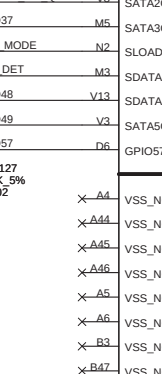
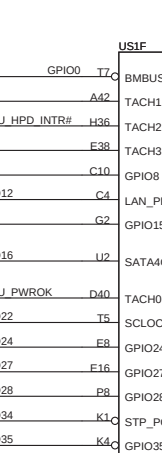
CougarPoint_Rev_1p0

USB PORT	Function	OC#
PORT-0	USB Port	OC0#
PORT-1	USB Port	OC0#
PORT-2	USB Port	OC1#
PORT-3	NC	
PORT-4	NC	
PORT-5	NC	
PORT-6	NC	
PORT-7	NC	
PORT-8	NC	
PORT-9	NC	
PORT-10	Camera	
PORT-11	WLAN/BT	
PORT-12	NC	
PORT-13	NC	

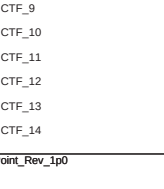
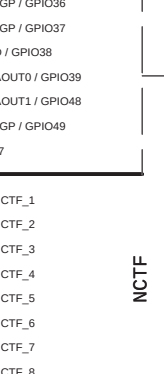
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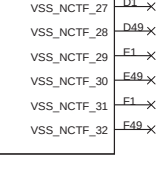
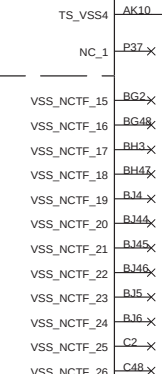
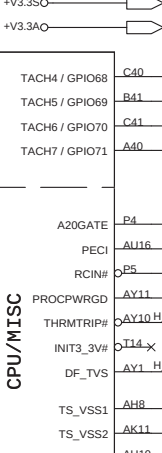
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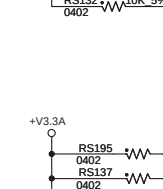
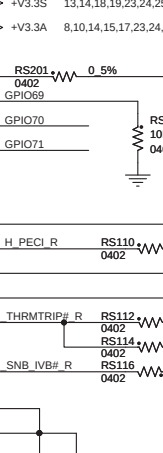
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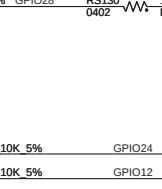
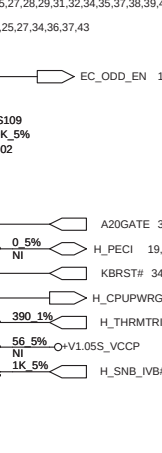
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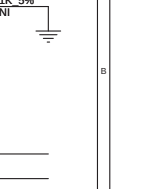
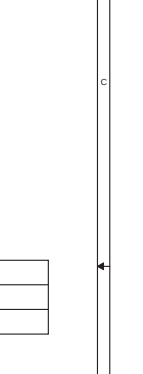
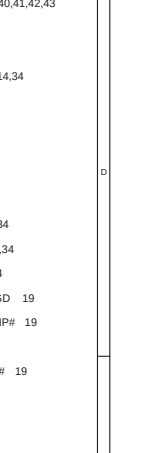
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CougarPoint_Rev_1p0

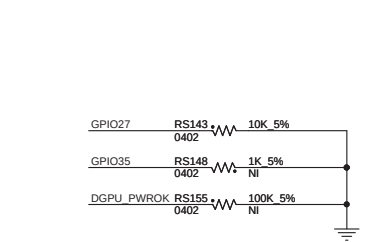
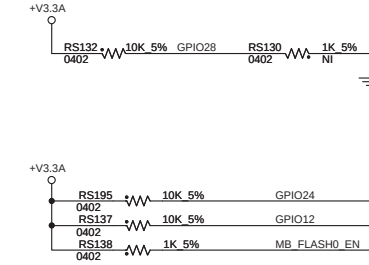


CougarPoint_Rev_1p0



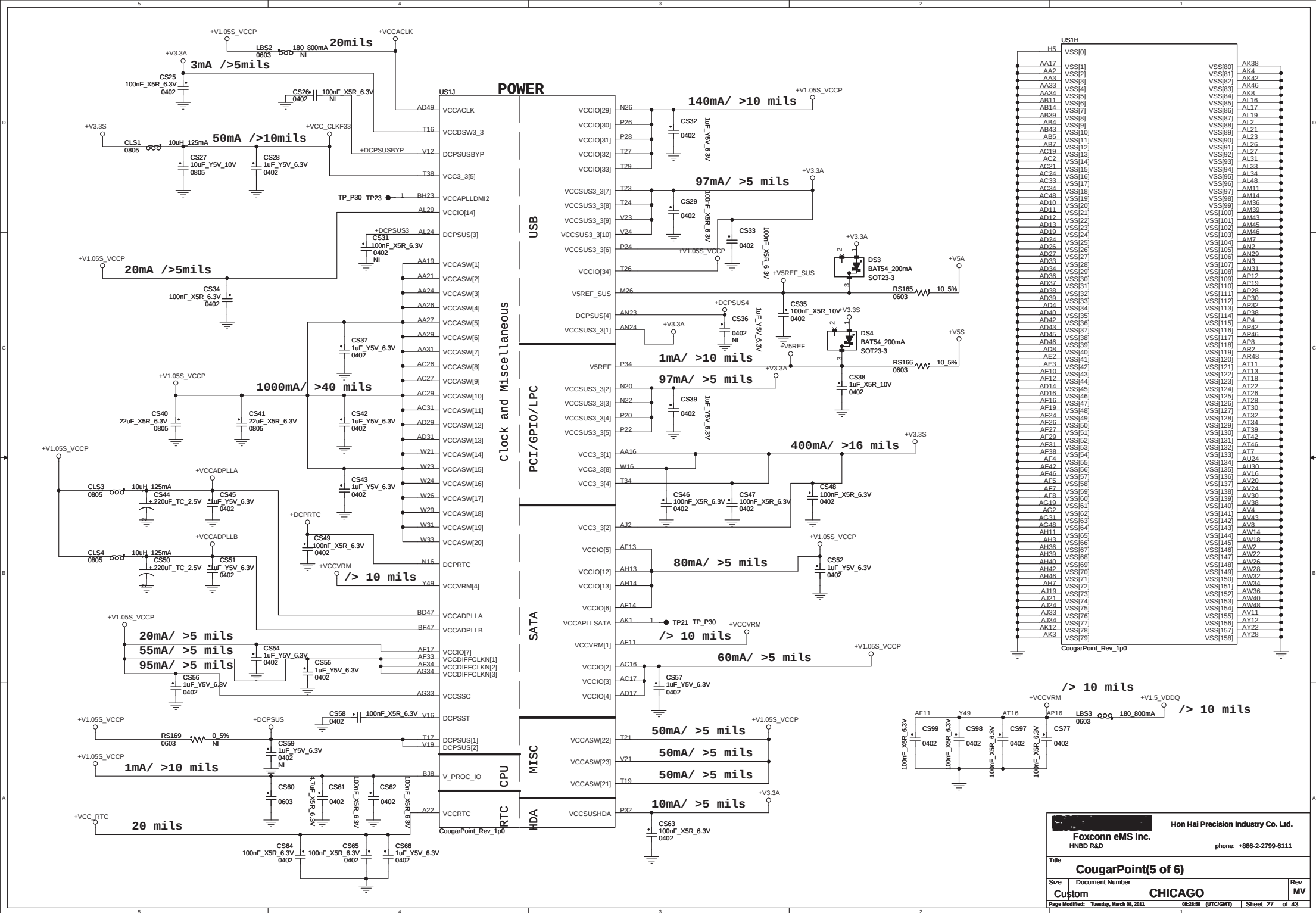
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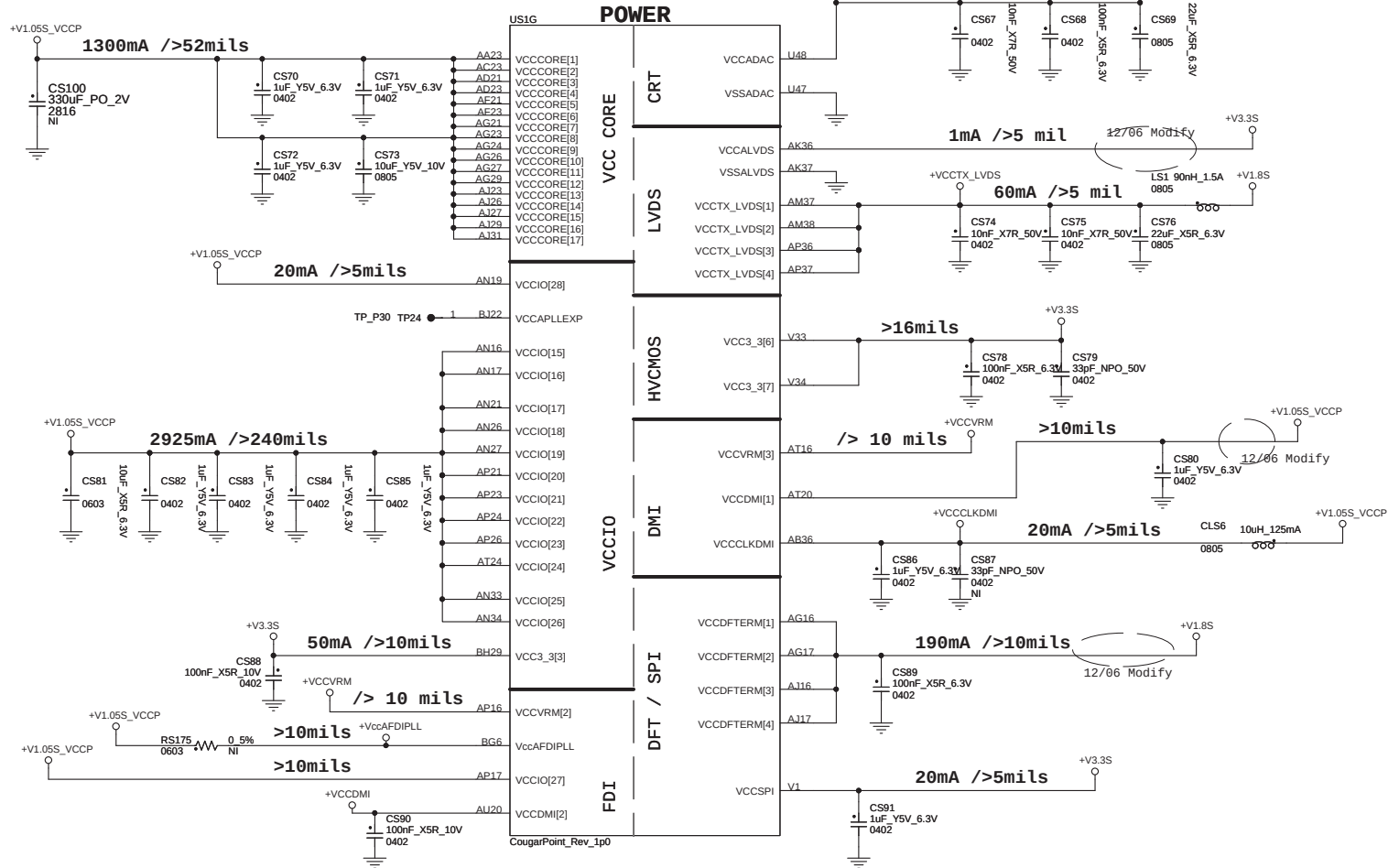
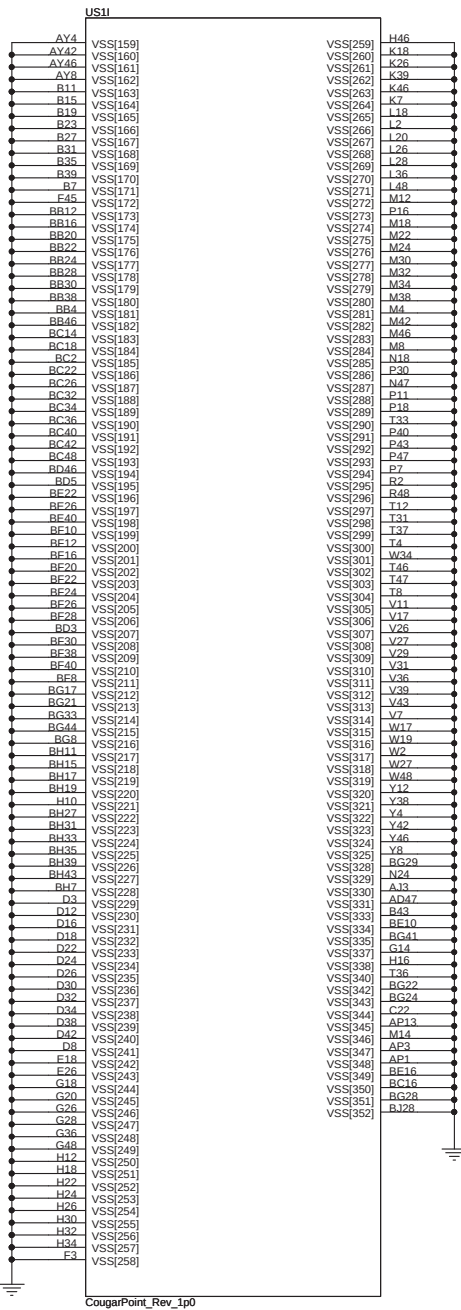
PLL ON DIE VR ENABLE		
GP28	0	disable
GP28	1	Enable(Default)

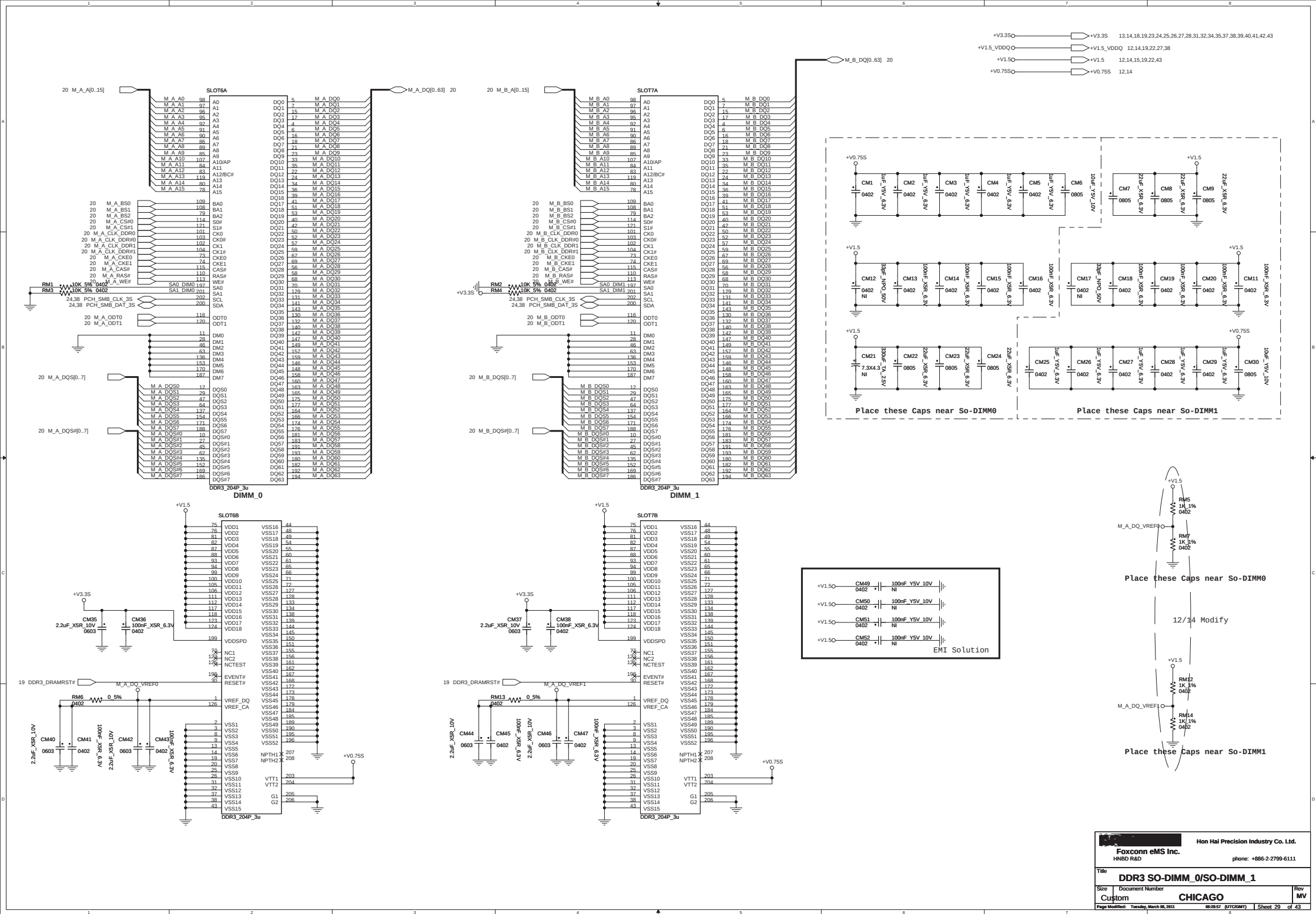


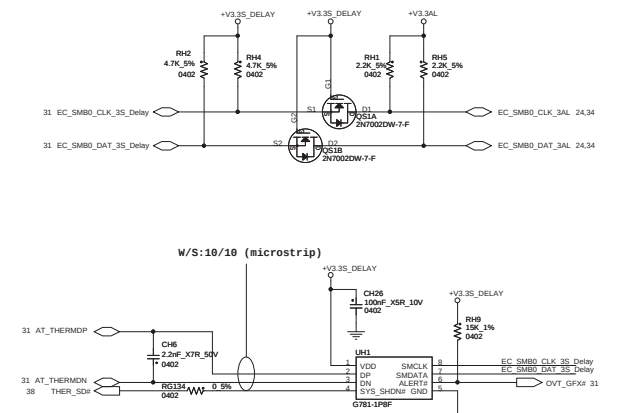
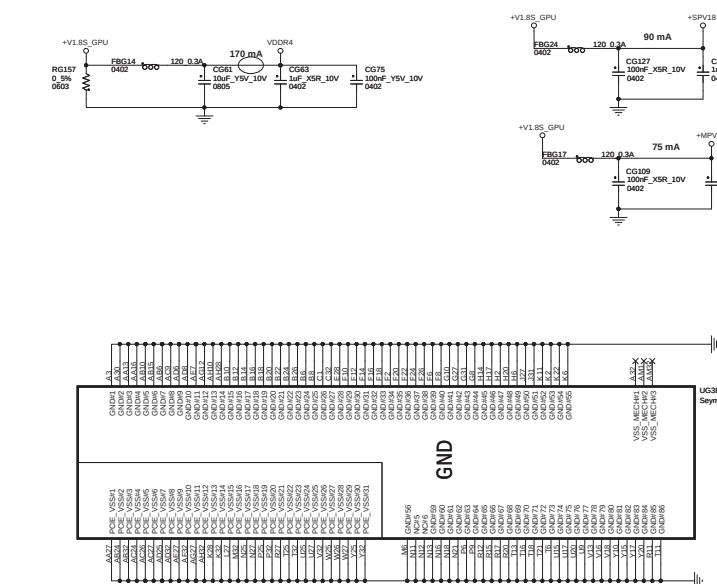
Foxconn eMS Inc.		
Size	Document Number	Rev
Custom	CHICAGO	MV

Page Modified: Tuesday, March 08, 2011 08:28:59 (UTC/GMT) Sheet 26 of 43

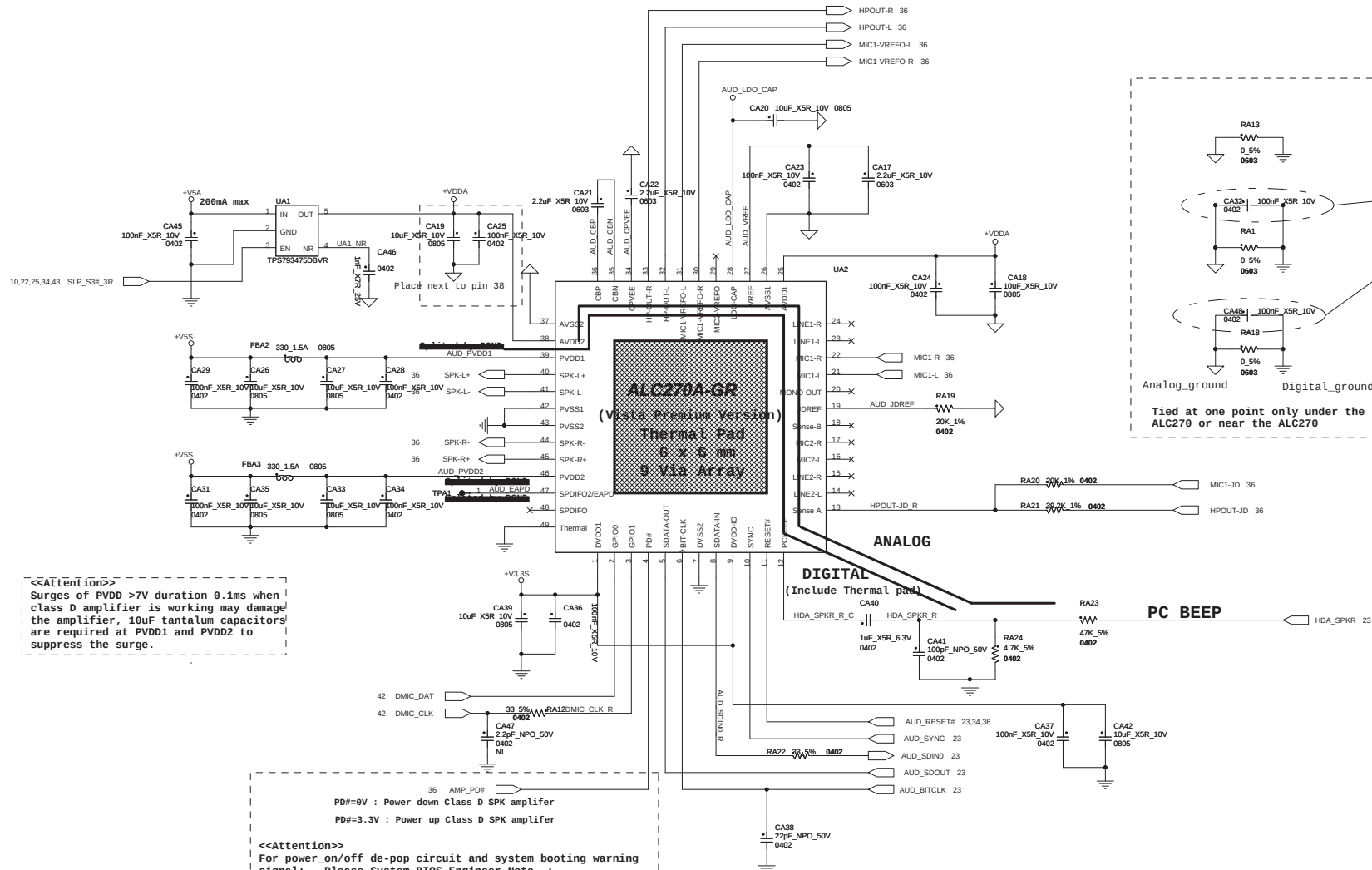






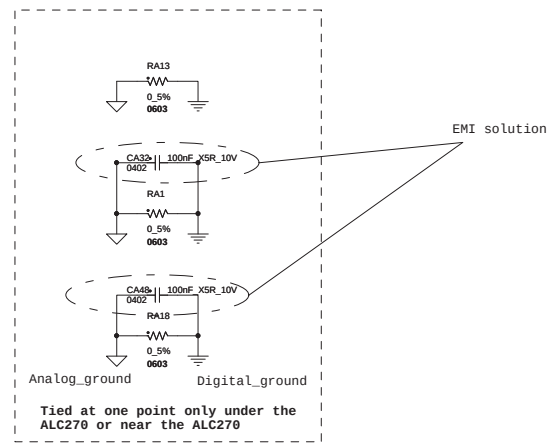


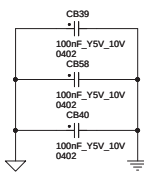
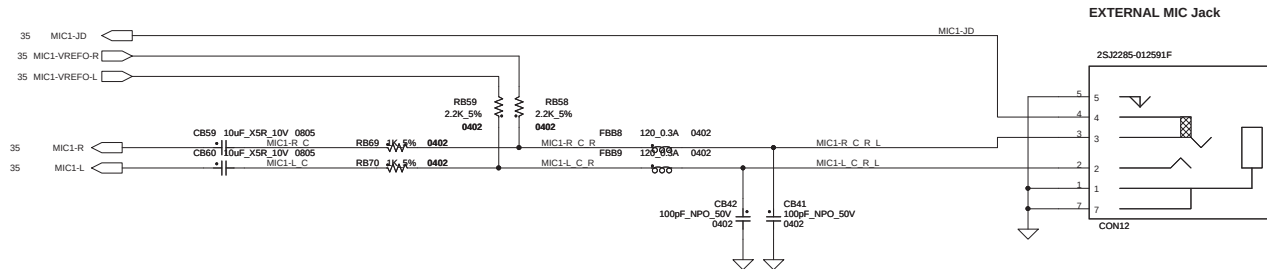
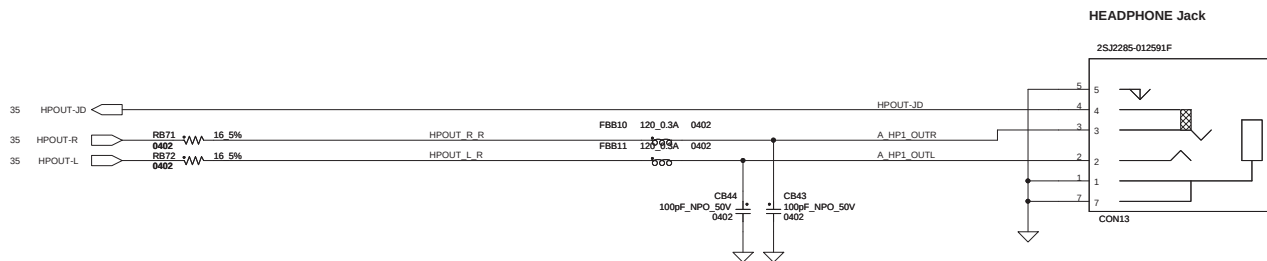
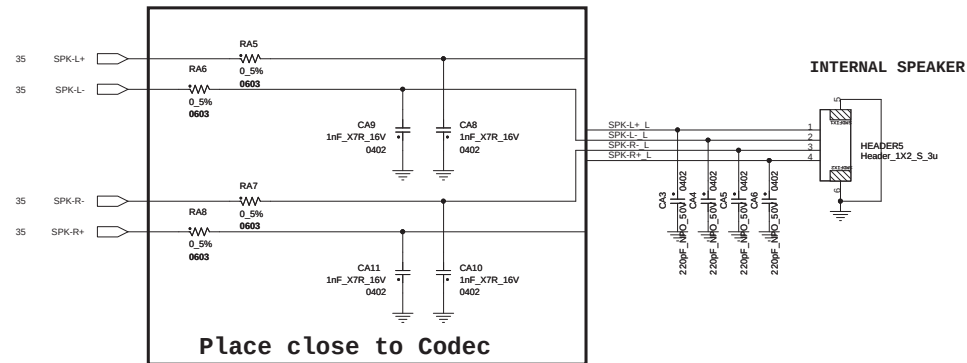
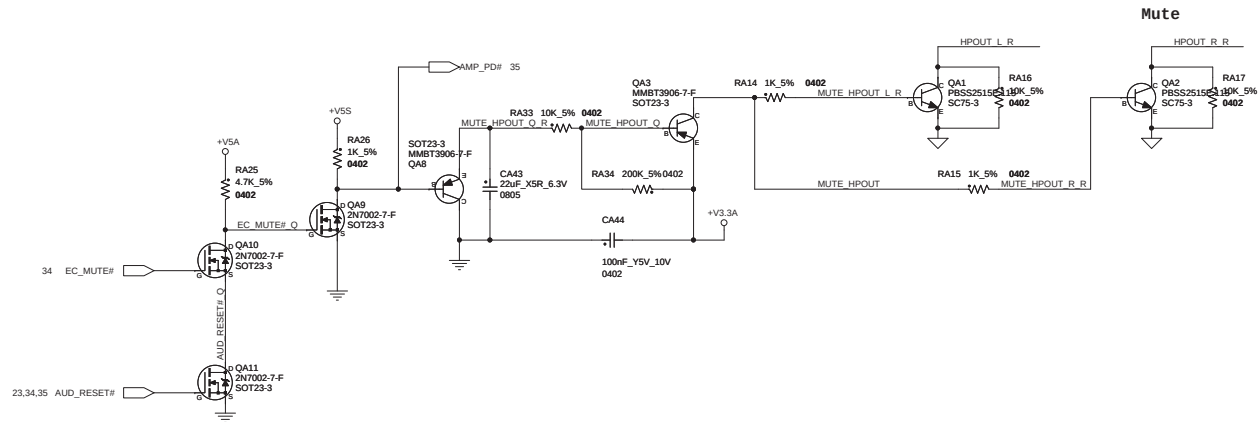
		Hon Hai Precision Industry Co. Ltd.	
Foxconn eMS Inc.		phone: +886-2-2799-6111	
HVBND R&D			
Title VGA_S3 (POWER) 3/3			
Size	Document Number		
Custom	CHICAGO		
Page Modified: Tuesday, March 03, 2015		48-2939 (JTC/GMT)	Sheet 32 of 4

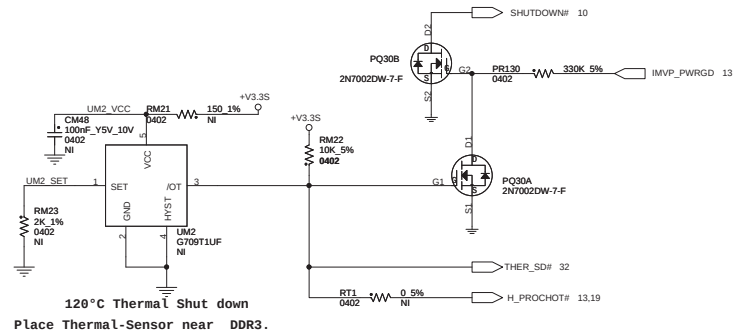
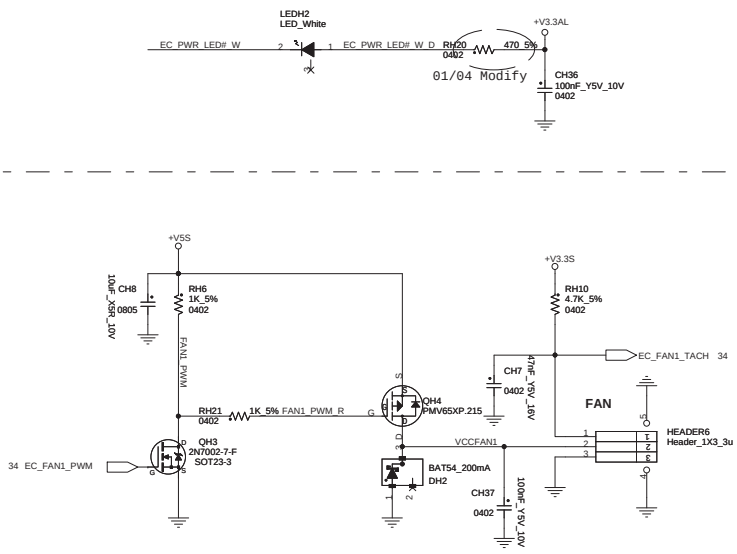


<<Attention>>
Surges of PVDD >7V duration 0.1ms when
class D amplifier is working may damage
the amplifier, 10uF tantalum capacitors
are required at PVDD1 and PVDD2 to
suppress the surge.

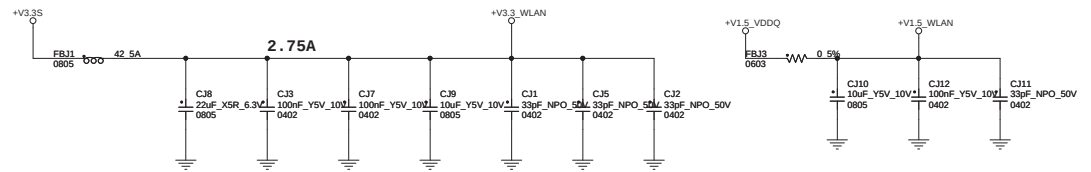
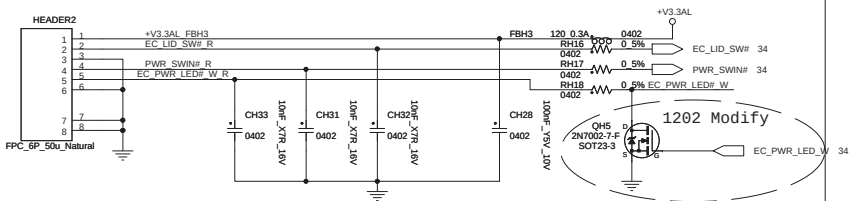
<<Attention>>
For power_on/off de-pop circuit and system booting warning
signal: Please System BIOS Engineer Note :
1. If you want the system make warning signal after power on
, please let EC_MUTE# High first.
2. When you want to exit your Bios Programming Code, please let
the EC_MUTE# Low. (The programming is different from before .)



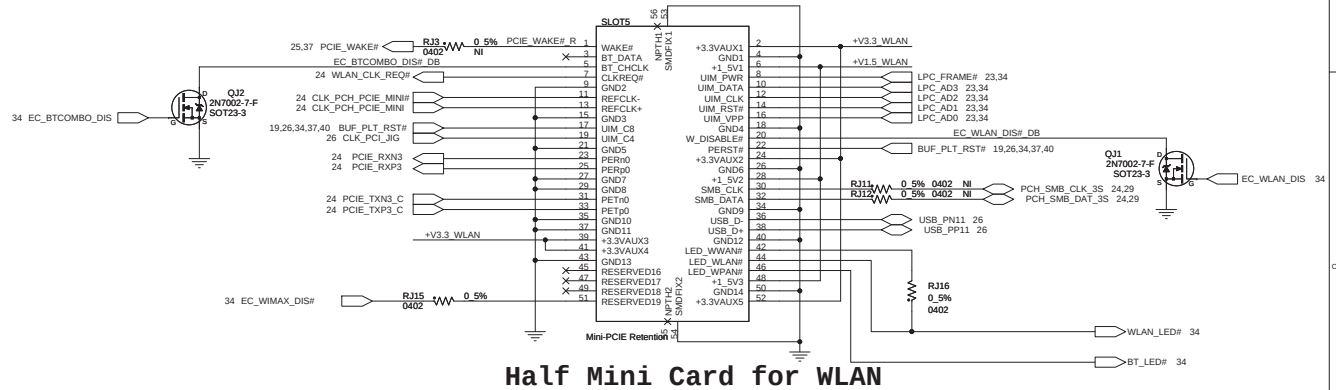




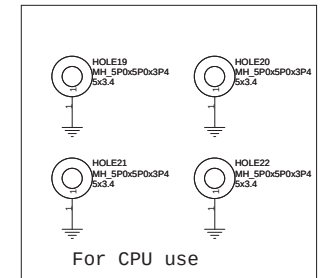
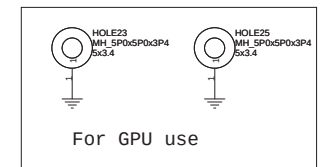
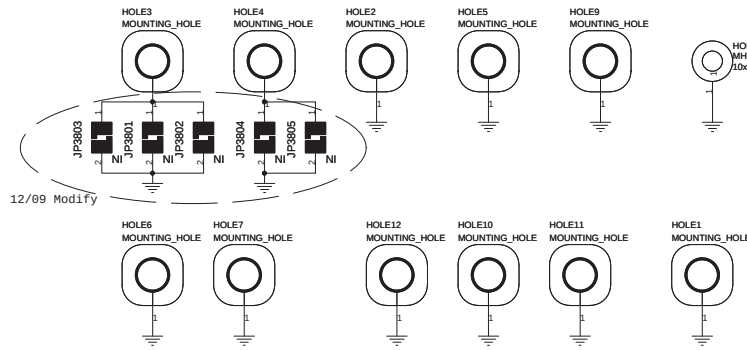
PWR Board CONN.



+1.5V=>0.5A Peak/0.375A Normal
+3.3VAux=>2.75A Peak/1.1A Normal

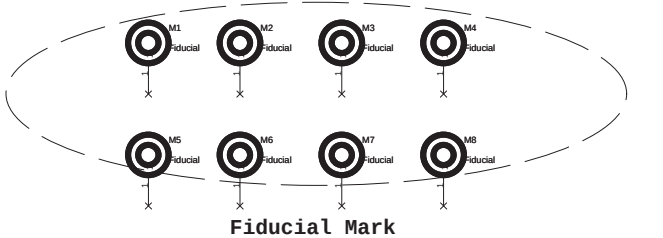


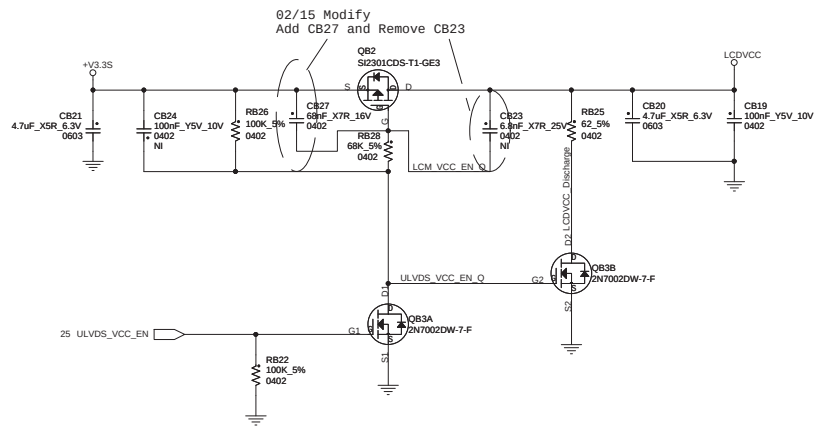
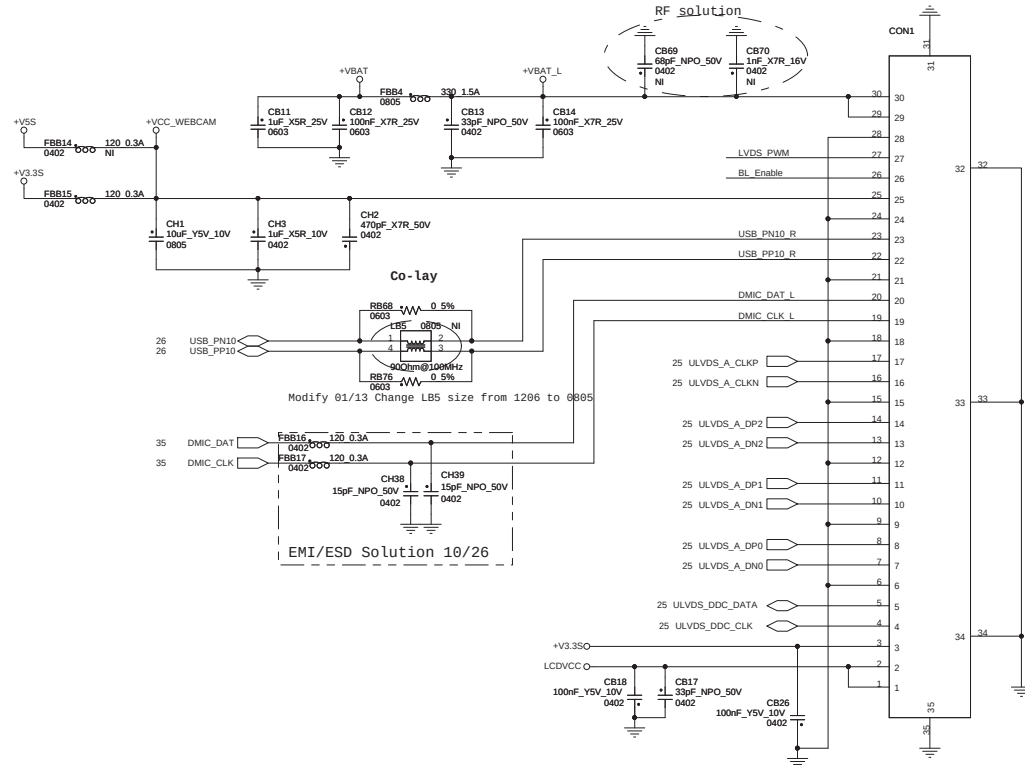
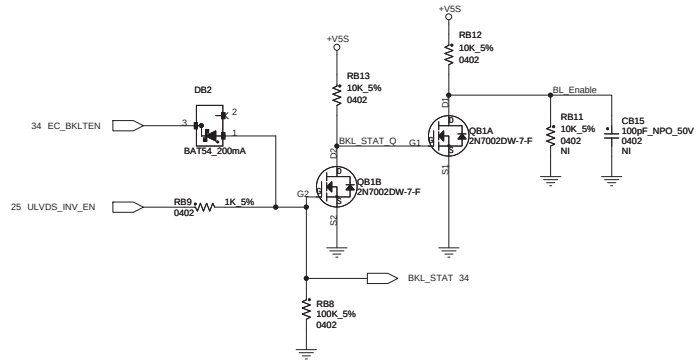
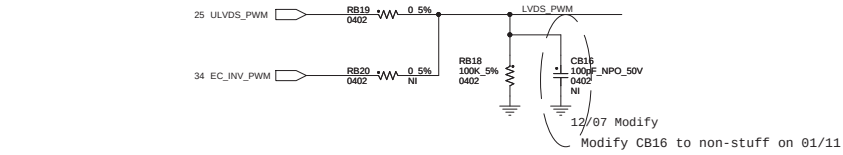
Half Mini Card for WLAN

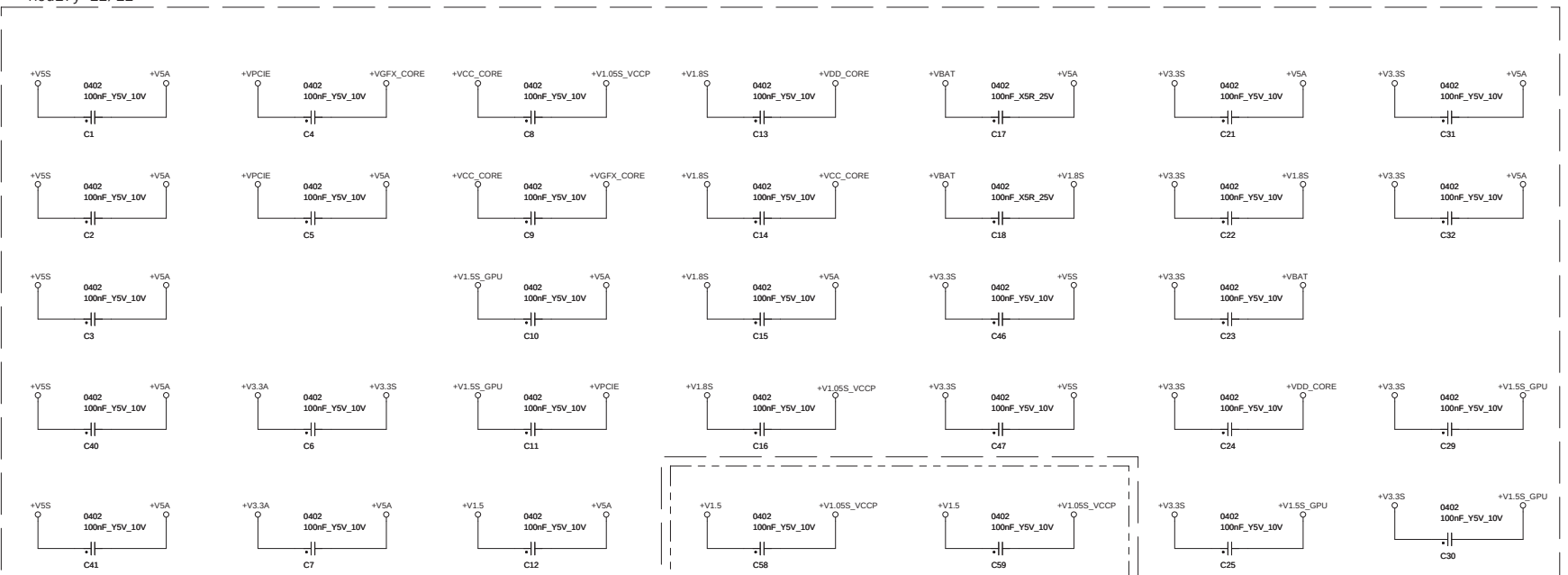
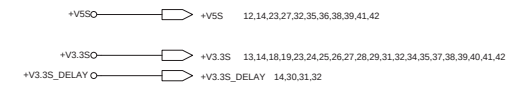


Mounting HOLE

02/09 Modify
Change PCBfootprint from FIDUCIAL_1P_3P_B to FIDUCIAL_MARK







EMI/ESD Solution 10/26

The diagram illustrates the placement of decoupling capacitors for the VBAT and V1.5 power rails. The components are as follows:

- C48:** 100nF XSR_25V 0402, connected to +VBAT.
- C49:** 100nF XSR_25V 0402, connected to +VBAT.
- C50:** 100nF XSR_25V 0402, connected to +VBAT.
- C51:** 100nF XSR_25V 0402, connected to +VBAT.
- C52:** 100nF XSR_25V 0402, connected to +VBAT.
- C53:** 100nF XSR_25V 0402, connected to +VBAT.
- C54:** 100nF Y5V_10V 0402, connected to +V1.5.
- C55:** 100nF Y5V_10V 0402, connected to +V1.5.
- C56:** 100nF Y5V_10V 0402, connected to +V1.5.
- C57:** 100nF Y5V_10V 0402, connected to +V1.5.