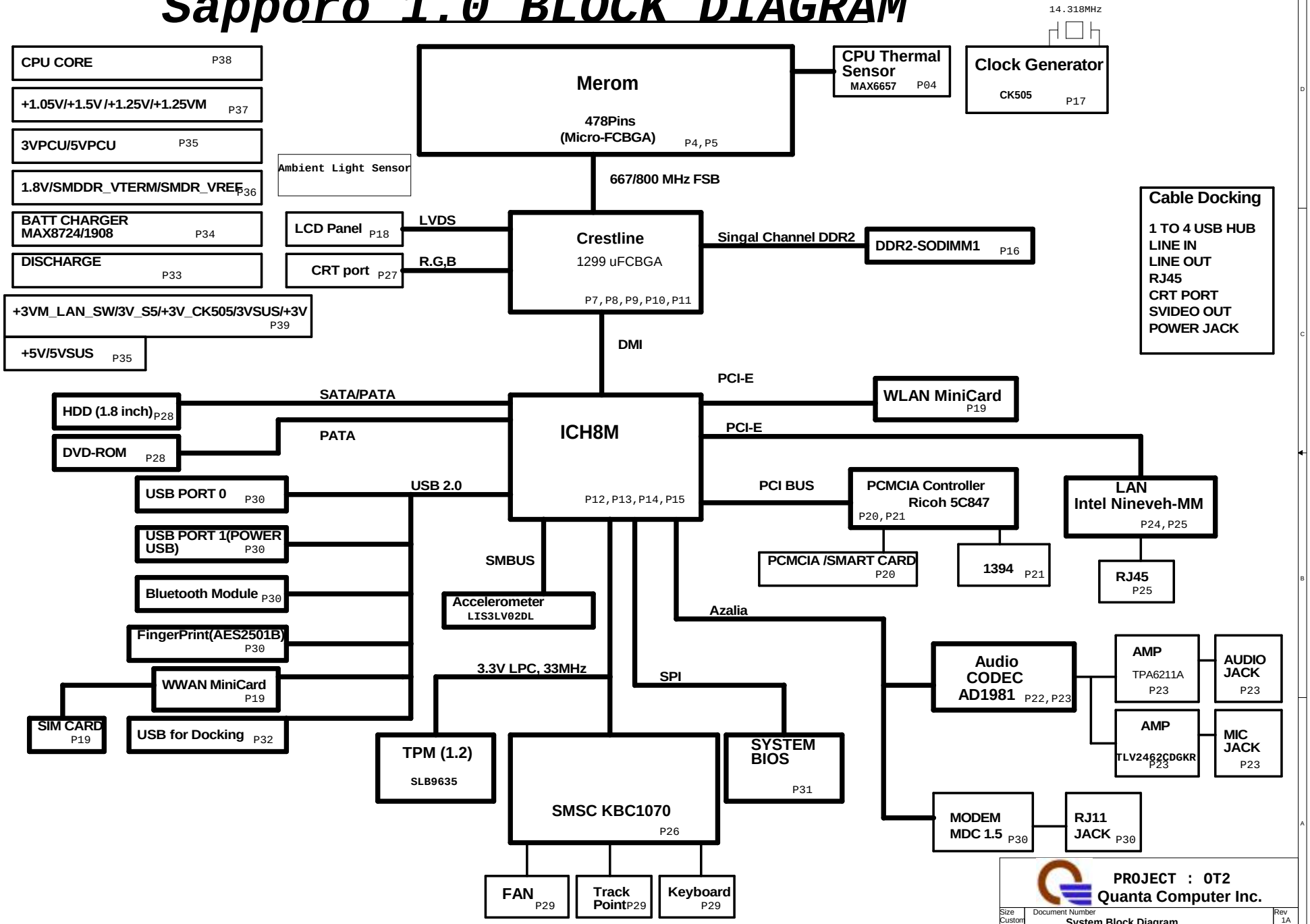
Sapporo 1.0 BLOCK DIAGRAM



INDEX

Power & Ground

Label	ACTIVE	Description	Control Signal
VIN	S0, S3, S4, S5.M0.M1.Moff	AC ADAPTER (19V)	
MBAT	S0, S3, S4, S5.M0.M1.Moff	MAIN BATTERY + (10~17V)	
VCCRTC	S0, S3, S4, S5.M0.M1.Moff	RTC & KBC POWER (3_3V)	
+15V	S0, S3, S4, S5.M0.M1.Moff	+15V	
CPU_CORE	S0	CPU CORE POWER (1.25/1.15V)	VRON
+1.05V	S0	FSB POWER (1.05V)	MAIND
+1.05VM	M0.M1		IAMT_ON
+3V	S0		MAIND
3VSUS	S0, S3		SUSON
3V_S5	S0, S3, S4, S5		S5_ON
3VPCU	S0, S3, S4, S5.M0.M1.Moff	ALWAYS POWER (3V)	
+5V	S0		MAIND
5VSUS	S0, S3		SUSON
5V_S5	S0, S3, S4, S5		S5_ON
5VPCU	S0, S3, S4, S5.M0.M1.Moff	ALWAYS POWER (5V)	
+1.5V	S0		MAIND
+1.5VM	M0.M1		IAMT_ON
1.8VSUS	S0, S3	DDR CORE POWER	SUSON
+2.5V	S0		MAINON
SMDDR_VTERM	S0	DDR COMMAND & CONTROL PULL UP POWER	MAINON
SMDDR_VREF	S0, S3	DDR REF POWER	SUSON
VDDA	S0	AUDIO ANALOG POWER (5V)	MAINON
+3V_CK505	M0.M1		IAMT_ON
+3V_LAN_SW	M0.M1		IAMT_ON
+1.25V	S0		MAIND
+1.25VM	M0.M1		IAMT_ON

PCI DEVICES IRQ ROUTING

DEVICE	IDSEL #	REQ/GNT #	PCI_INT

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : IN3
LAYER 7 : GND
LAYER 8 : BOT

SM BUS

DEVICE	ADDRESS	BUS
CLOCK GENERATOR		
DDR II		
Accelemter sensor		
CHARGER		
CPU THERMAL SENSOR		

PROJECT : 0T2
Quanta Computer Inc.

Size	Document Number	Rev
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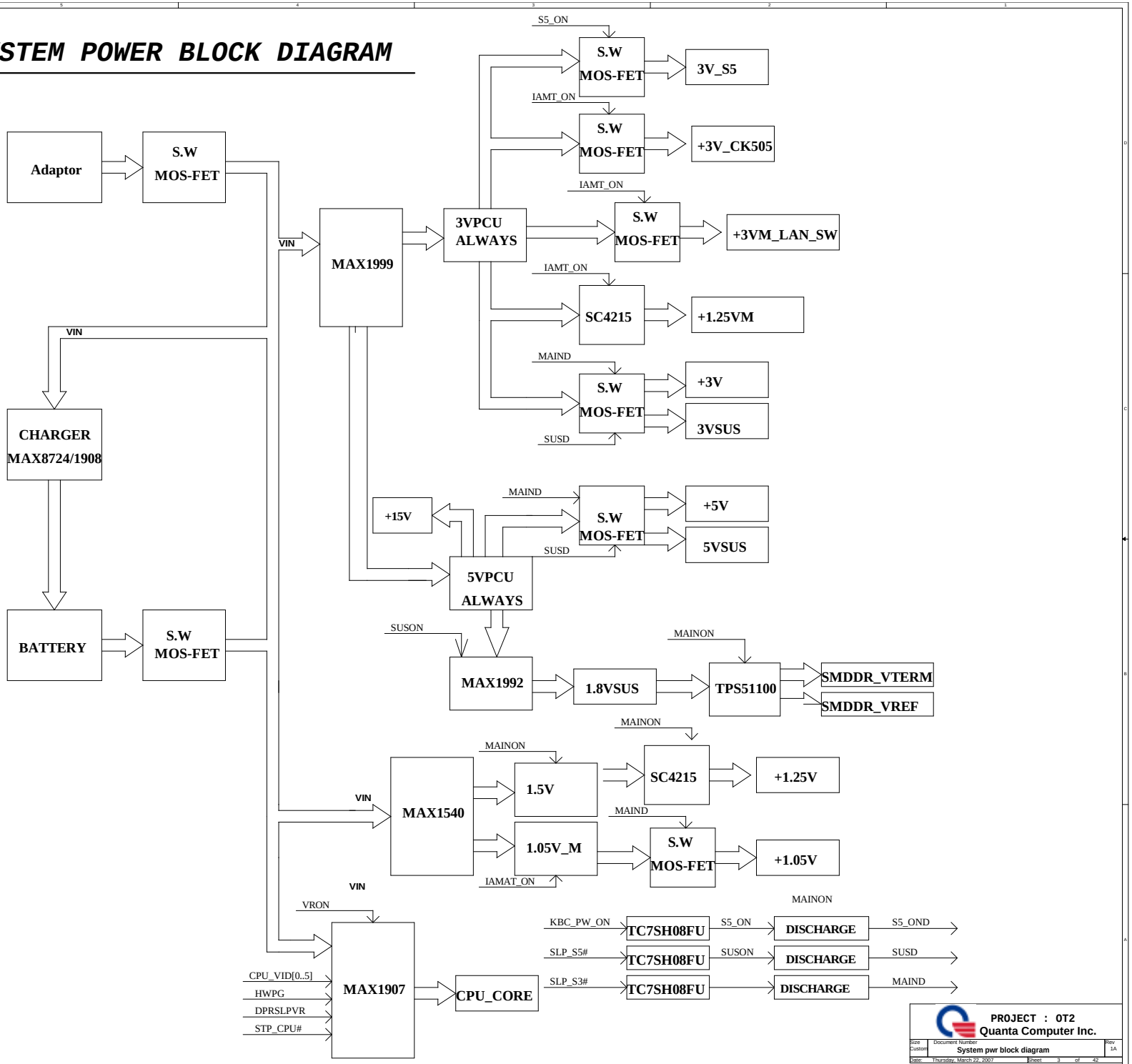
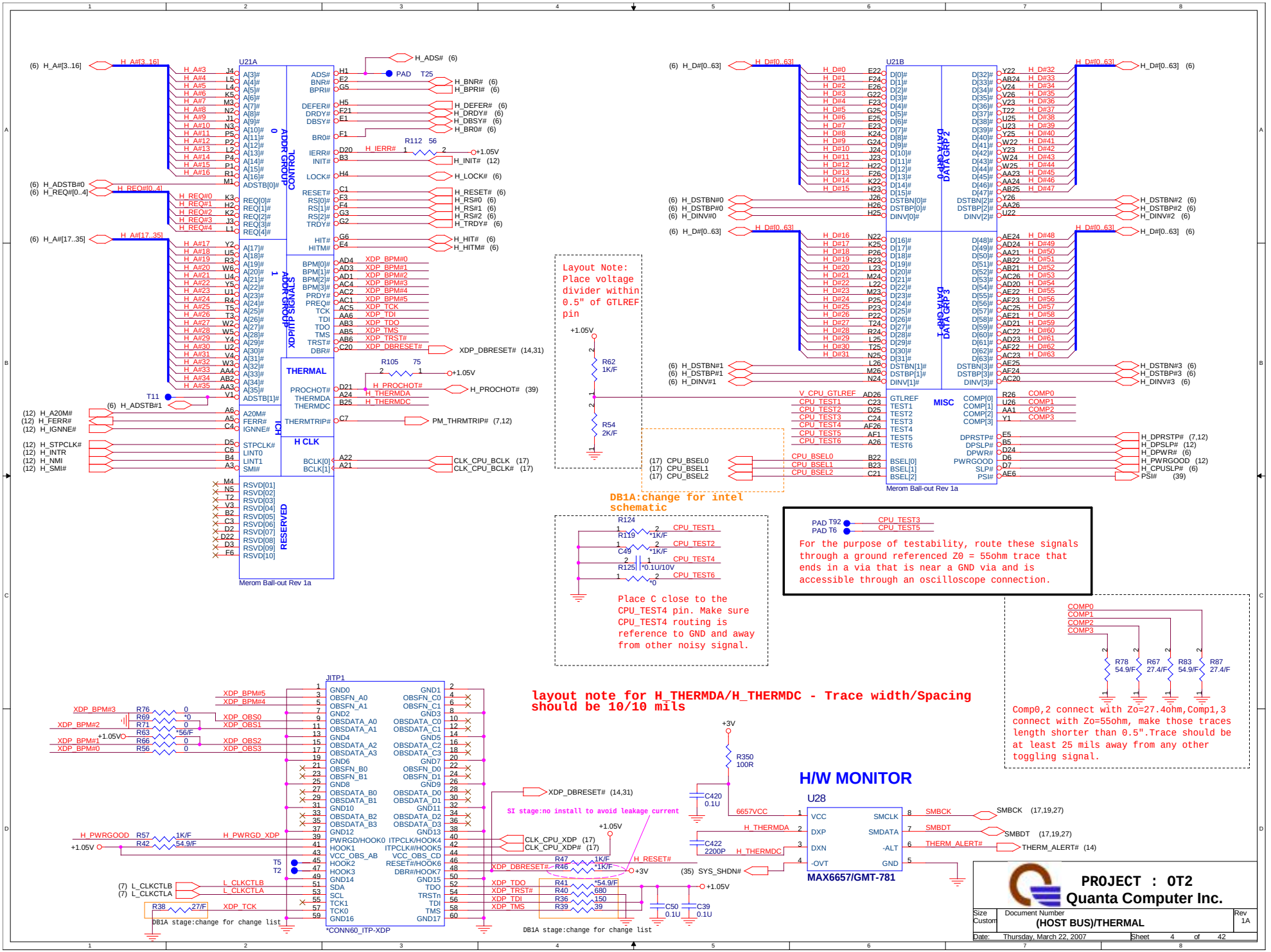
SYSTEM POWER BLOCK DIAGRAM



PROJECT : 0T2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	System pwr block diagram	1A
Date: Thursday, March 22, 2007	Sheet 3 of 42	


U21A
ADDR GROUP 0
ADDR GROUP 1
XDP/ITP SIGNALS
THERMAL
H CLK
RESERVED
ICH
Merom Ball-out Rev 1a
U21B
DATA GRP 2
DATA GRP 1
DATA GRP 3
DATA GRP 0
MISC
Merom Ball-out Rev 1a
Layout Note: Place voltage divider within 0.5" of GTLREF pin
DB1A:change for intel schematic
Place C close to the CPU_TEST4 pin. Make sure CPU_TEST4 routing is reference to GND and away from other noisy signal.
For the purpose of testability, route these signals through a ground referenced Z0 = 55ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.
Comp0,2 connect with Zo=27.4ohm,Comp1,3 connect with Zo=55ohm, make those traces length shorter than 0.5".Trace should be at least 25 mils away from any other toggling signal.
layout note for H_THERMDA/H_THERMDC - Trace width/Spacing should be 10/10 mils
JITP1
*CONN60_ITP-XDP
DB1A stage:change for change list
SI stage:no install to avoid leakage current
H/W MONITOR
U28
MAX6657/GMT-781
PROJECT : 0T2
Quanta Computer Inc.
(HOST BUS)/THERMAL
Size Custom
Document Number
Rev 1A
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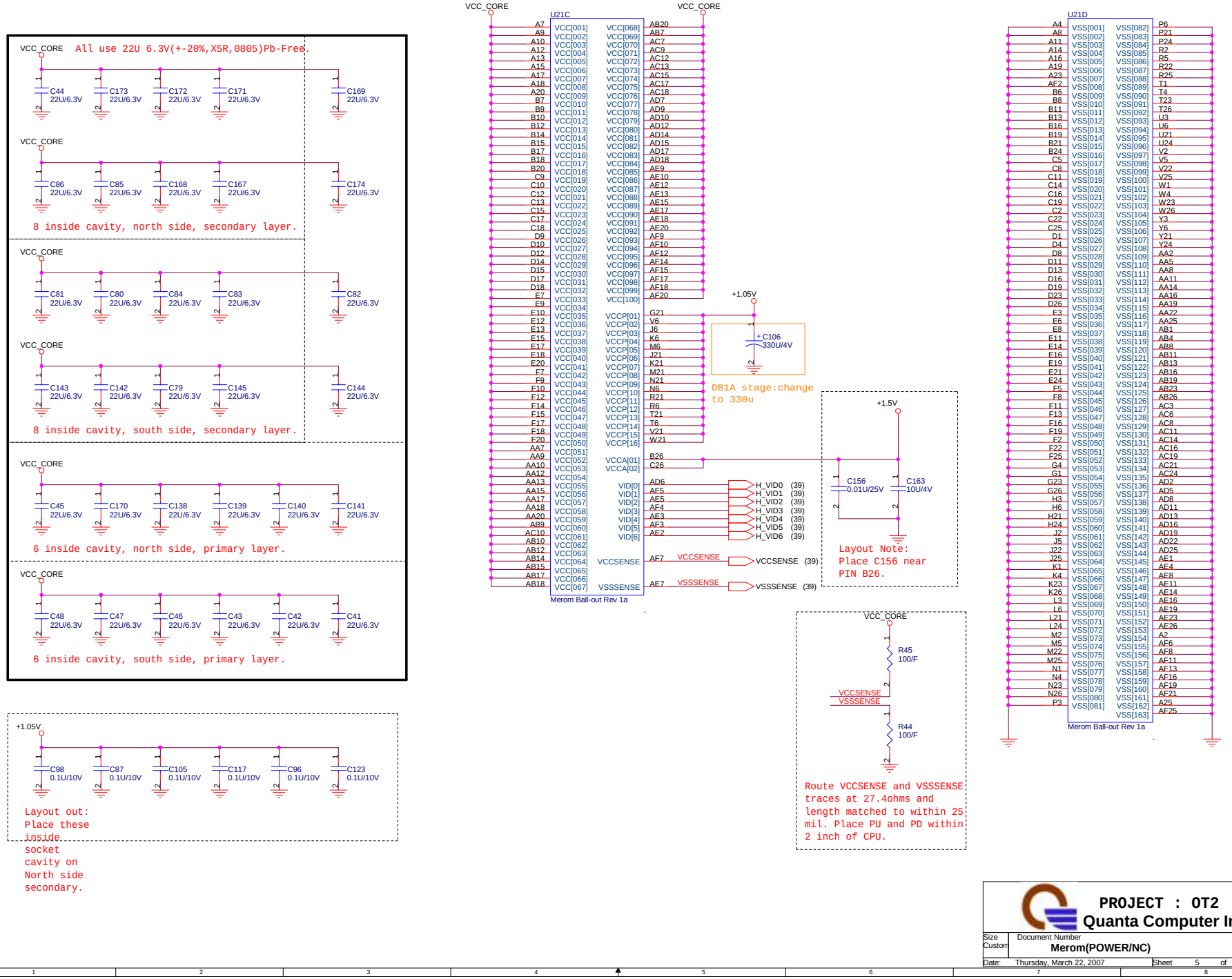
All use 22U 6.3V(+-20%,X5R,0805)Pb-Free.
VCC_CORE
C44 22U/6.3V
C173 22U/6.3V
C172 22U/6.3V
C171 22U/6.3V
C169 22U/6.3V
C86 22U/6.3V
C85 22U/6.3V
C168 22U/6.3V
C167 22U/6.3V
C174 22U/6.3V
8 inside cavity, north side, secondary layer.
C81 22U/6.3V
C80 22U/6.3V
C84 22U/6.3V
C83 22U/6.3V
C82 22U/6.3V
C143 22U/6.3V
C142 22U/6.3V
C79 22U/6.3V
C145 22U/6.3V
C144 22U/6.3V
8 inside cavity, south side, secondary layer.
C45 22U/6.3V
C170 22U/6.3V
C138 22U/6.3V
C139 22U/6.3V
C140 22U/6.3V
C141 22U/6.3V
6 inside cavity, north side, primary layer.
C48 22U/6.3V
C47 22U/6.3V
C46 22U/6.3V
C43 22U/6.3V
C42 22U/6.3V
C41 22U/6.3V
6 inside cavity, south side, primary layer.
+1.05V
C98 0.1U/10V
C87 0.1U/10V
C105 0.1U/10V
C117 0.1U/10V
C96 0.1U/10V
C123 0.1U/10V
Layout out:
Place these
inside
socket
cavity on
North side
secondary.
VCC_CORE
U21C
Merom Ball-out Rev 1a
+1.05V
C106 330U/4V
DB1A stage:change
to 330u
+1.5V
C156 0.01U/25V
C163 10U/4V
Layout Note:
Place C156 near
PIN B26.
H_VID0 (39)
H_VID1 (39)
H_VID2 (39)
H_VID3 (39)
H_VID4 (39)
H_VID5 (39)
H_VID6 (39)
VCCSENSE (39)
VSSSENSE (39)
R45 100/F
R44 100/F
Route VCCSENSE and VSSSENSE
traces at 27.4ohms and
length matched to within 25
mil. Place PU and PD within
2 inch of CPU.
U21D
Merom Ball-out Rev 1a
PROJECT : 0T2
Quanta Computer Inc.
Size Custom
Document Number
Merom(POWER/NC)
Rev 1A
Date: Thursday, March 22, 2007
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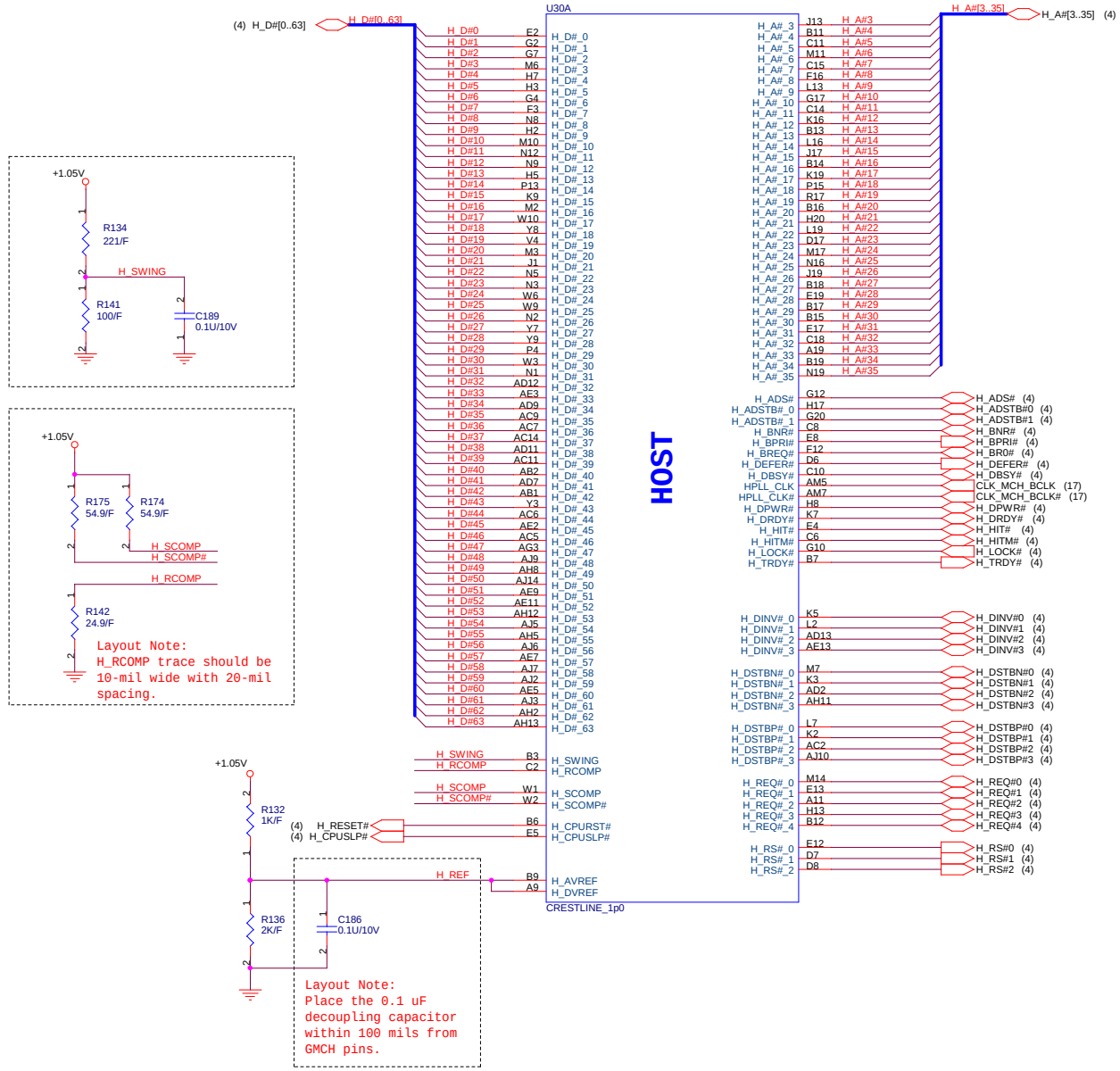

PROJECT : 0T2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Crestline_1(HOST)	1A

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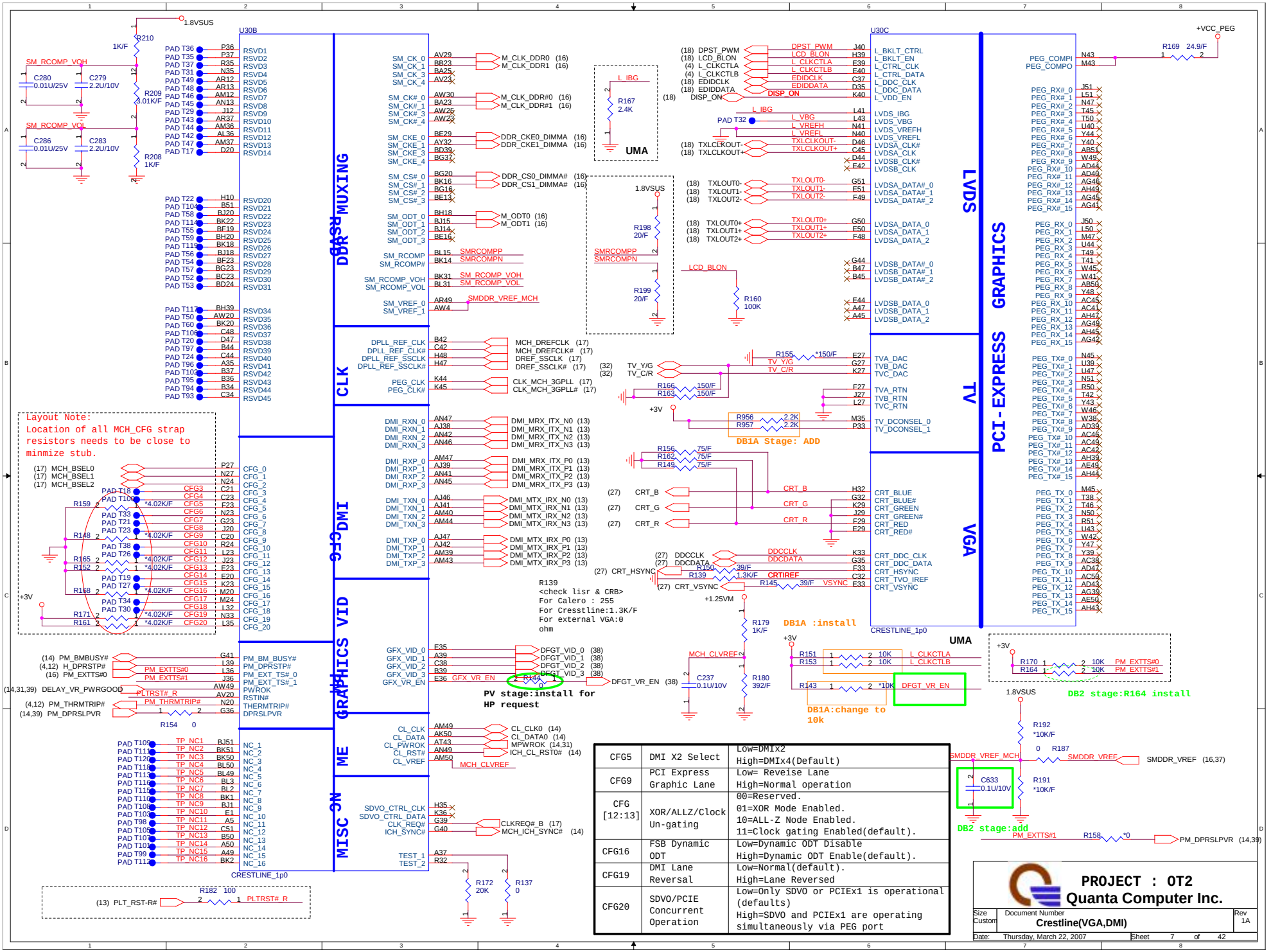
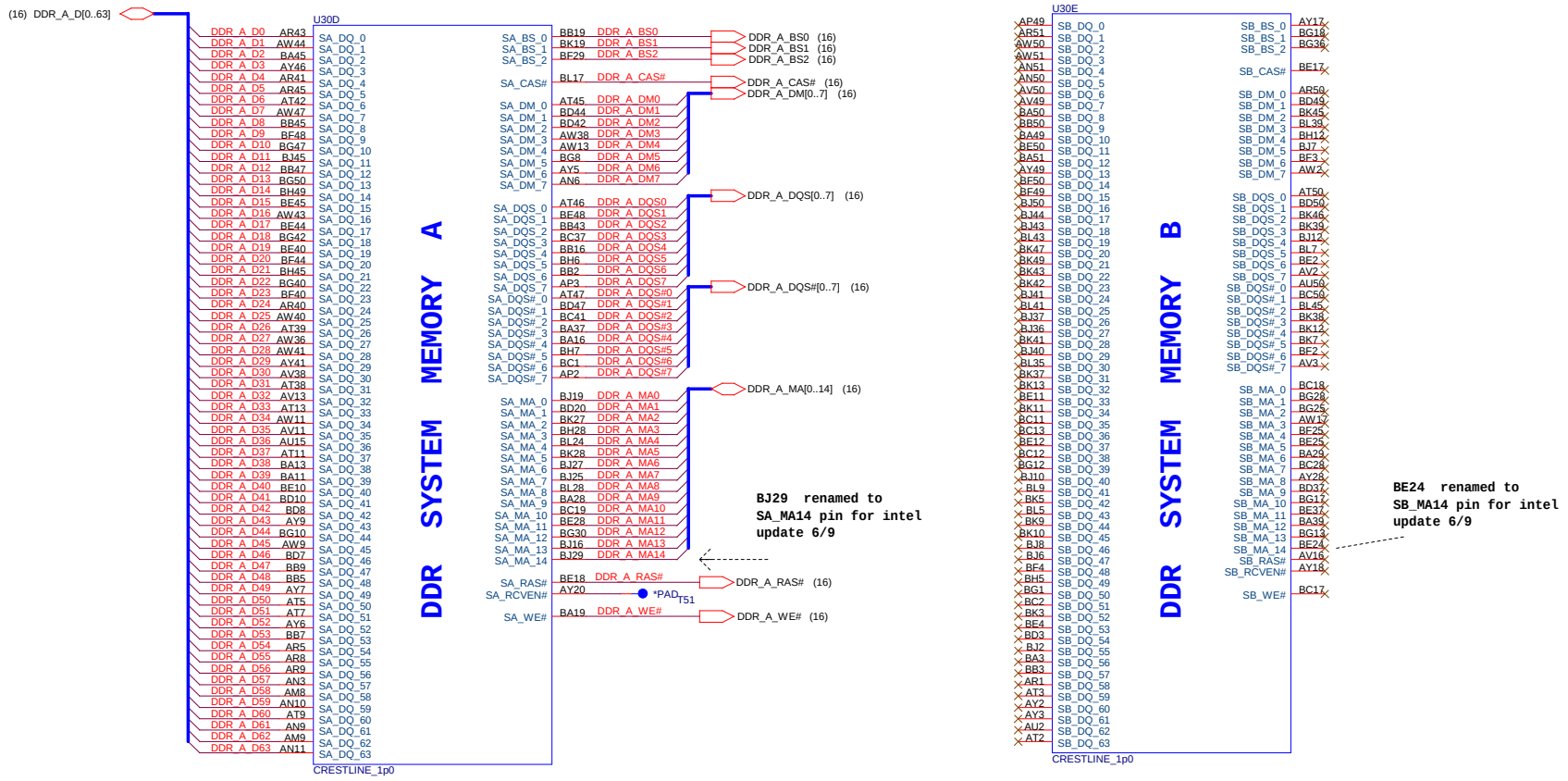


CFG5	DMI X2 Select	Low=DMIx2 High=DMIx4(Default)
CFG9	PCI Express Graphic Lane	Low= Reveise Lane High=Normal operation
CFG [12:13]	XOR/ALLZ/Clock Un-gating	00=Reserved. 01=XOR Mode Enabled. 10=ALL-Z Node Enabled. 11=Clock gating Enabled(default).
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default).
CFG19	DMI Lane Reversal	Low=Normal(default). High=Lane Reversed
CFG20	SDVO/PCIE Concurrent Operation	Low=Only SDVO or PCIEx1 is operational (defaults) High=SDVO and PCIEx1 are operating simultaneously via PEG port



PROJECT : 0T2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Crestline(DDR2)	1A
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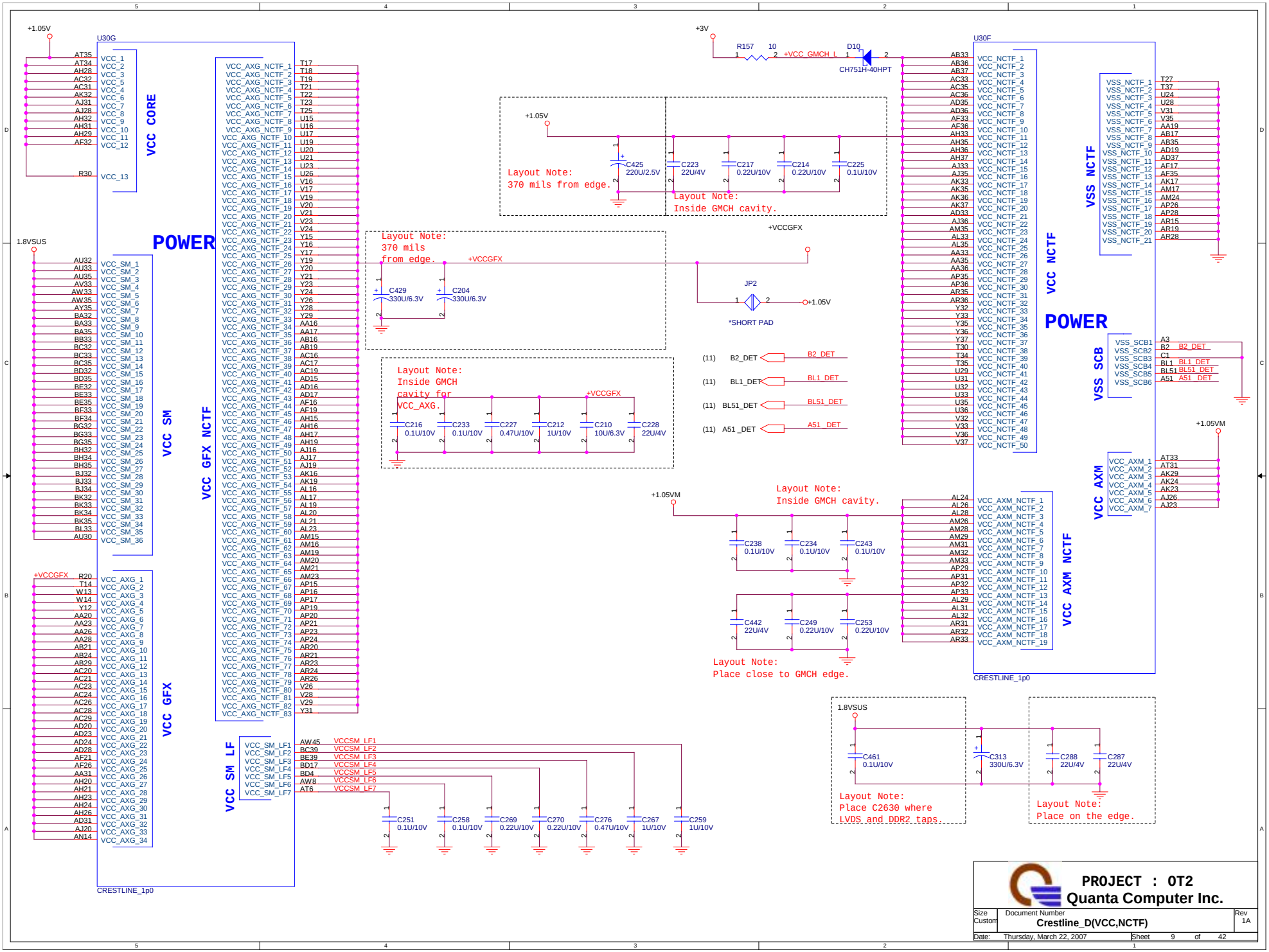
U30G
POWER
VCC CORE
VCC SM
VCC GFX NCTF
VCC GFX
VCC SM LF
CRESTLINE_1p0
U30F
VCC NCTF
VSS NCTF
VSS SCB
VCC AXM
VCC AXM NCTF
+1.05V
1.8VSUS
+VCCGFX
+3V
+1.05VM
R157 10
D10
CH751H-40HPT
+VCC_GMCH_L
JP2
*SHORT PAD
Layout Note:
370 mils from edge.
Layout Note:
Inside GMCH cavity.
Layout Note:
370 mils
from edge.
Layout Note:
Inside GMCH
cavity for
VCC_AXG.
Layout Note:
Place close to GMCH edge.
Layout Note:
Place C2630 where
LVDS and DDR2 taps.
Layout Note:
Place on the edge.
B2_DET
BL1_DET
BL51_DET
A51_DET
PROJECT : 0T2
Quanta Computer Inc.
Crestline_D(VCC,NCTF)
Size Custom
Rev 1A
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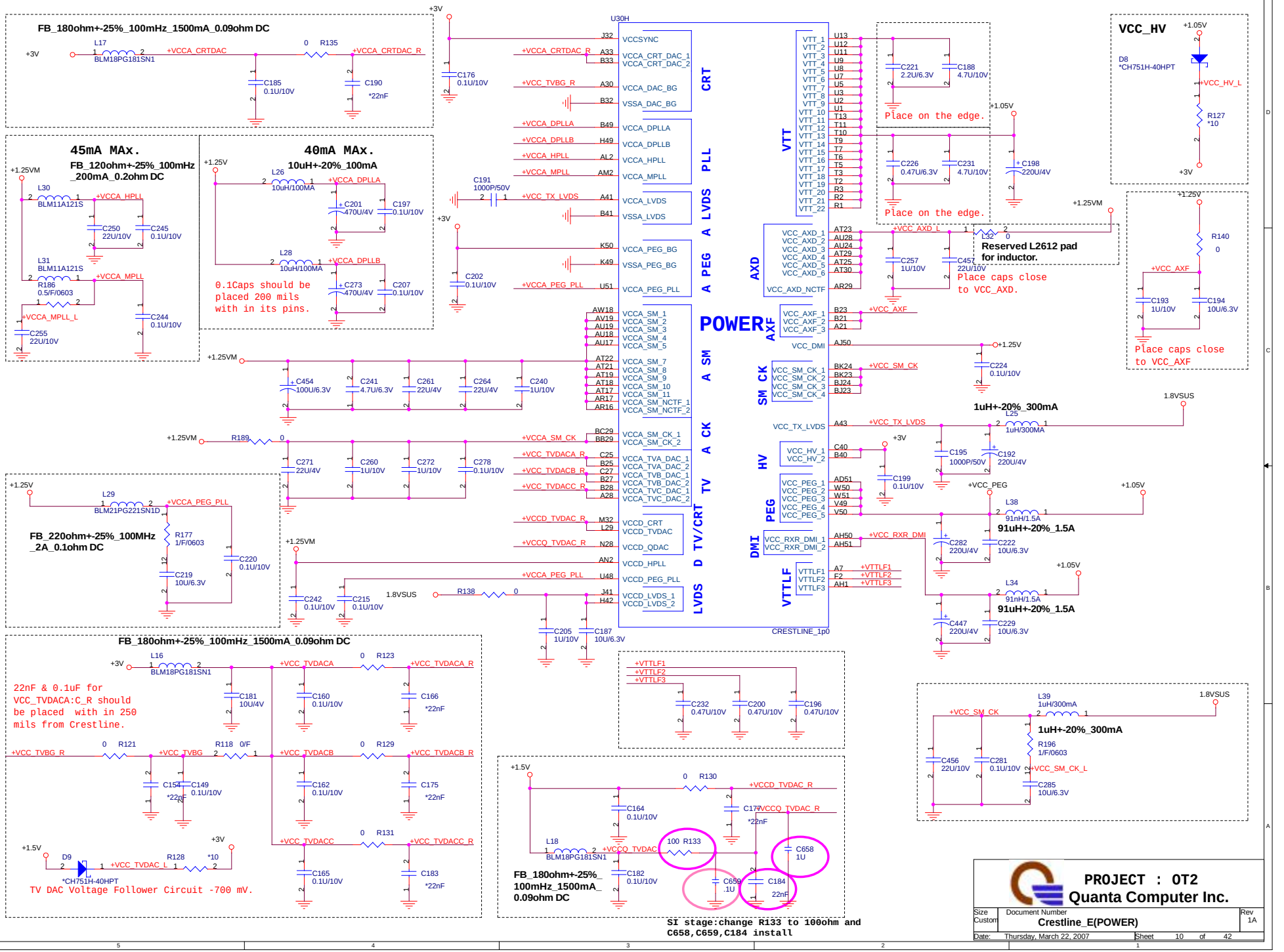
FB_180ohm+-25%_100mHz_1500mA_0.09ohm DC
45mA MAx.
FB_120ohm+-25%_100mHz_200mA_0.2ohm DC
40mA MAx.
10uH+-20%_100mA
0.1Caps should be placed 200 mils with in its pins.
FB_220ohm+-25%_100MHz_2A_0.1ohm DC
FB_180ohm+-25%_100mHz_1500mA_0.09ohm DC
22nF & 0.1uF for VCC_TVDACA:C_R should be placed with in 250 mils from Crestline.
TV DAC Voltage Follower Circuit -700 mV.
FB_180ohm+-25%_100mHz_1500mA_0.09ohm DC
U30H
POWER
CRESTLINE_1p0
CRT
PLL
LVDS
PEG
SM CK
HV
DMI
VTTLF
Place on the edge.
Place on the edge.
Reserved L2612 pad for inductor.
Place caps close to VCC_AXD.
Place caps close to VCC_AXF
VCC_HV
D8 *CH751H-40HPT
1uH+-20%_300mA
91uH+-20%_1.5A
91uH+-20%_1.5A
1uH+-20%_300mA
SI stage:change R133 to 100ohm and C658,C659,C184 install
PROJECT : 0T2
Quanta Computer Inc.
Crestline_E(POWER)
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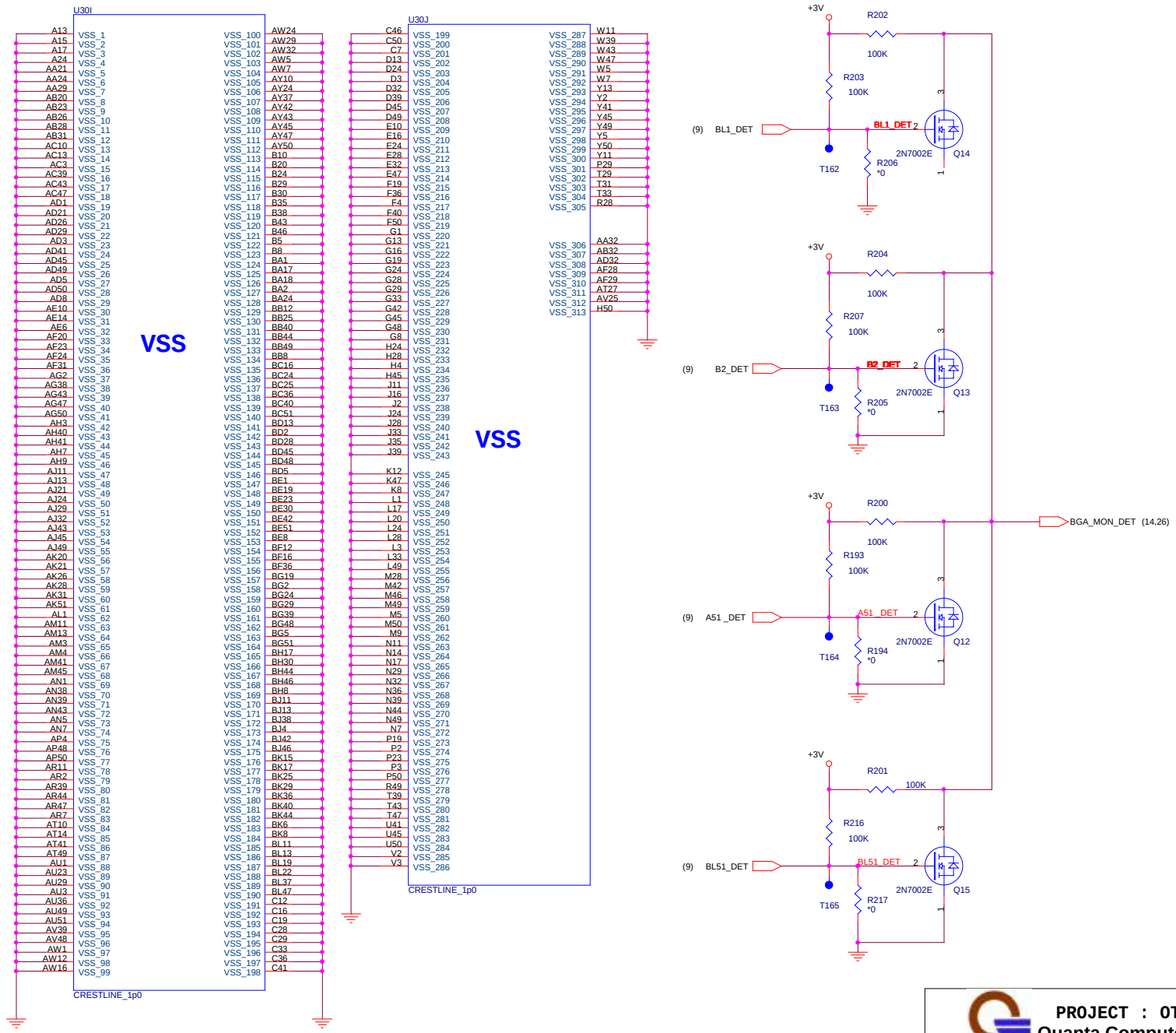
SI stage: add test pin



PROJECT : 0T2

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Crestline(VSS)	1A
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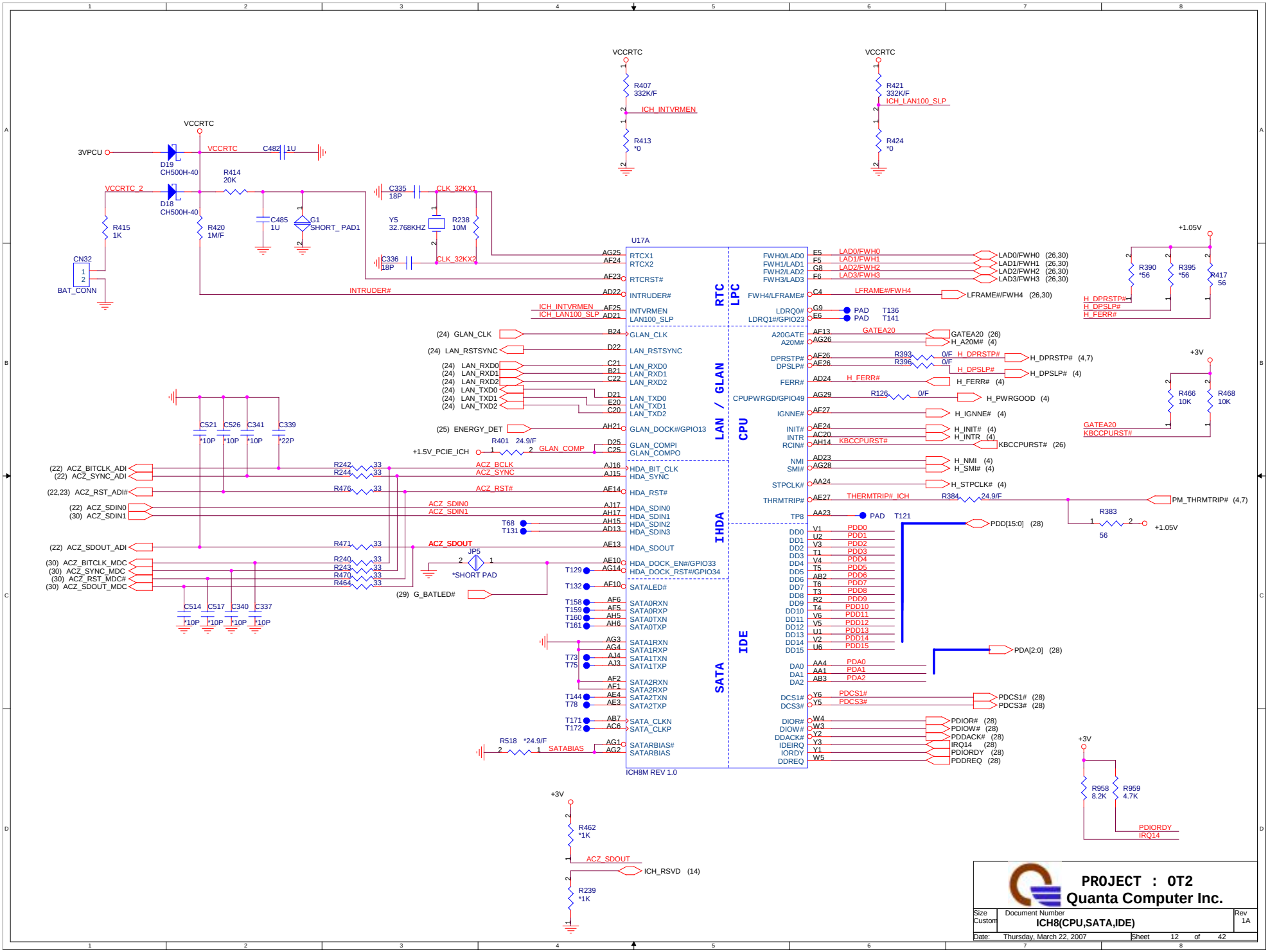
VCCRTC
R407 332K/F
ICH_INTVRMEN
R413 *0
R421 332K/F
ICH_LAN100_SLP
R424 *0
3VPCU
D19 CH500H-40
C482 1U
D18 CH500H-40
R414 20K
R415 1K
R420 1M/F
C485 1U
G1 SHORT_ PAD1
CN32
BAT_CONN
C335 18P
C336 18P
Y5 32.768KHZ
R238 10M
CLK_32KX1
CLK_32KX2
INTRUDER#
U17A
RTCX1
RTCX2
RTCRST#
INTRUDER#
INTVRMEN
LAN100_SLP
RTC
LPC
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
LAD0/FWH0 (26,30)
LAD1/FWH1 (26,30)
LAD2/FWH2 (26,30)
LAD3/FWH3 (26,30)
LFRAME#/FWH4 (26,30)
+1.05V
R390 *56
R395 *56
R417 56
H_DPRSTP#
H_DPSLP#
H_FERR#
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#/GPIO13
GLAN_COMPI
GLAN_COMPO
LAN / GLAN
CPU
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD/GPIO49
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
TP8
GATEA20 (26)
H_A20M# (4)
H_DPRSTP# (4,7)
H_DPSLP# (4)
H_FERR# (4)
H_PWRGOOD (4)
H_IGNNE# (4)
H_INIT# (4)
H_INTR (4)
KBCCPURST# (26)
H_NMI (4)
H_SMI# (4)
H_STPCLK# (4)
PM_THRMTRIP# (4,7)
+3V
R466 10K
R468 10K
GATEA20
KBCCPURST#
R383 56
+1.05V
PDD[15:0] (28)
(24) GLAN_CLK
(24) LAN_RSTSYNC
(24) LAN_RXD0
(24) LAN_RXD1
(24) LAN_RXD2
(24) LAN_TXD0
(24) LAN_TXD1
(24) LAN_TXD2
(25) ENERGY_DET
+1.5V_PCIE_ICH
R401 24.9/F
GLAN_COMP
C521 *10P
C526 *10P
C341 *10P
C339 *22P
(22) ACZ_BITCLK_ADI
(22) ACZ_SYNC_ADI
(22,23) ACZ_RST_ADI#
(22) ACZ_SDIN0
(30) ACZ_SDIN1
(22) ACZ_SDOUT_ADI
(30) ACZ_BITCLK_MDC
(30) ACZ_SYNC_MDC
(30) ACZ_RST_MDC#
(30) ACZ_SDOUT_MDC
R242 33
R244 33
R476 33
R471 33
R240 33
R243 33
R470 33
R464 33
ACZ_BCLK
ACZ_SYNC
ACZ_RST#
ACZ_SDIN0
ACZ_SDIN1
ACZ_SDOUT
C514 *10P
C517 *10P
C340 *10P
C337 *10P
JP5
*SHORT PAD
(29) G_BATLED#
IHDA
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
T68
T131
T129
T132
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
R518 *24.9/F
SATABIAS
SATA
IDE
DD0
DD1
DD2
DD3
DD4
DD5
DD6
DD7
DD8
DD9
DD10
DD11
DD12
DD13
DD14
DD15
PDD0
PDD1
PDD2
PDD3
PDD4
PDD5
PDD6
PDD7
PDD8
PDD9
PDD10
PDD11
PDD12
PDD13
PDD14
PDD15
DA0
DA1
DA2
PDA0
PDA1
PDA2
PDA[2:0] (28)
DCS1#
DCS3#
PDCS1# (28)
PDCS3# (28)
DIOR#
DIOW#
DDACK#
IDEIRQ
IORDY
DDREQ
PDIOR# (28)
PDIOW# (28)
PDDACK# (28)
IRQ14 (28)
PDIORDY (28)
PDDREQ (28)
+3V
R958 8.2K
R959 4.7K
PDIORDY
IRQ14
ICH8M REV 1.0
+3V
R462 *1K
ACZ_SDOUT
ICH_RSVD (14)
R239 *1K
PROJECT : 0T2
Quanta Computer Inc.
Size Custom
Document Number
ICH8(CPU,SATA,IDE)
Rev 1A
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MINI CARD PCI-E

(19) PCIE_RXN2 → PCIE_RXN2 M27
(19) PCIE_RXP2 → PCIE_RXP2 M26
(19) PCIE_TXN2 → C466 0.1U → PCIE_TXN2_C L29
(19) PCIE_TXP2 → C465 0.1U → PCIE_TXP2_C L28

Intel LAN

(24) PCIE_RXN6 → PCIE_RXN6 D27
(24) PCIE_RXP6 → PCIE_RXP6 D26
(24) PCIE_TXN6 → C468 0.1U → PCIE_TXN6_C C29
(24) PCIE_TXP6 → C467 0.1U → PCIE_TXP6 C28

U17D

PCI-Express Direct Media Interface

P27	PERN1	DMI0RXN	V27 → DMI_MTX_IRX_N0 (7)
P26	PERP1	DMI0RXP	V26 → DMI_MTX_IRX_P0 (7)
N29	PETN1	DMI0TXN	U29 → DMI_MRX_ITX_N0 (7)
N28	PETP1	DMI0TXP	U28 → DMI_MRX_ITX_P0 (7)
	PERN2	DMI1RXN	Y27 → DMI_MTX_IRX_N1 (7)
	PERP2	DMI1RXP	Y26 → DMI_MTX_IRX_P1 (7)
	PETN2	DMI1TXN	W29 → DMI_MRX_ITX_N1 (7)
	PETP2	DMI1TXP	W28 → DMI_MRX_ITX_P1 (7)
K27	PERN3	DMI2RXN	AB26 → DMI_MTX_IRX_N2 (7)
K26	PERP3	DMI2RXP	AB25 → DMI_MTX_IRX_P2 (7)
J29	PETN3	DMI2TXN	AA29 → DMI_MRX_ITX_N2 (7)
J28	PETP3	DMI2TXP	AA28 → DMI_MRX_ITX_P2 (7)
H27	PERN4	DMI3RXN	AD27 → DMI_MTX_IRX_N3 (7)
H26	PERP4	DMI3RXP	AD26 → DMI_MTX_IRX_P3 (7)
G29	PETN4	DMI3TXN	AC29 → DMI_MRX_ITX_N3 (7)
G28	PETP4	DMI3TXP	AC28 → DMI_MRX_ITX_P3 (7)
F27	PERN5	DMI_CLKN	T26 → CLK_PCIE_ICH# (17)
F26	PERP5	DMI_CLKP	T25 → CLK_PCIE_ICH (17)
E29	PETN5		
E28	PETP5		
		DMI_ZCOMP	
		DMI_IRCOMP	
		DMI_COMP	Y23 / Y24

R412 24.9/F
+1.5V_PCIE_ICH

Place within 500mils of ICH8

SPI

SPI_CLK	C23
SPI_CS0#	B23
SPI_CS1#	E22
SPI_MOSI	D23
SPI_MISO	F21

(31) SPI_CLK
(31) SPI_CS0#
(14,26) SPI_CS1#
R398 15
R403 15
R410 15
SPI_CS1_R#

PV stage:change R399 to 15 ohm for intel request

(31) SPI_SI → R399 15 → SPI_MOSI
(31) SPI_SO → R409 0/F → SPI_MISO

USB

USBP0N	G3	USBP0-	(30)
USBP0P	G2	USBP0+	(30)
USBP1N	H5	USBP1-	(30)
USBP1P	H4	USBP1+	(30)
USBP2N	H2	USBP2-	PAD T77
USBP2P	H1	USBP2+	PAD T76
USBP3N	J3	USBP3-	PAD T149
USBP3P	J2	USBP3+	PAD T145
USBP4N	K5		PAD T155
USBP4P	K4		PAD T156
USBP5N	K2	USBP5-	(30)
USBP5P	K1	USBP5+	(30)
USBP6N	L3	USBP6-	(30)
USBP6P	L2	USBP6+	(30)
USBP7N	M5	USBP7-	(32)
USBP7P	M4	USBP7+	(32)
USBP8N	M2	USBP8-	(19)
USBP8P	M1	USBP8+	(19)
USBP9N	N3	USBP9-	PAD T146
USBP9P	N2	USBP9+	PAD T79

SYSTEM(RIGHT)
FINGER PRINT
DB1A stage:change for HP request

SYSTEM(LEFT)
Bluetooth Module
Docking
WWAN

OC0#
OC1#/GPIO40
OC2#/GPIO41
OC3#/GPIO42
OC4#/GPIO43
OC5#/GPIO29
OC6#/GPIO30
OC7#/GPIO31
OC8#
OC9#

USBRBIAS# F2
USBRBIAS F3 → R512 22.6/F

ICH8M REV 1.0

Short F2 and F3 at the package and keep length to less than 500mils. Trace Impedance should be 60ohms +/- 15%.

SI stage:Change power source to avoid leakage current

SI2 stage:Change power source to avoid leakage current

3V_S5 → RP31 8.2KX8

3V_S5	6	5	USBOC#3
USBOC#4	7	4	USBOC#7
USBOC#0	8	3	USBOC#2
USBOC#6	9	2	USBOC#1
	10	1	USBOC#8

3V_S5 → R241 8.2K → USBOC#9

(19) WWAN_OFF# → R455 0/F
(30) BT_OFF → R456 0/F

USBOC#0	AJ19	USBOC#0
USBOC#1	AG16	USBOC#1
USBOC#2	AG15	USBOC#2
USBOC#3	AE15	USBOC#3
USBOC#4	AF15	USBOC#4
USBOC#5	AG17	USBOC#5
USBOC#6	AD12	USBOC#6
USBOC#7	AJ18	USBOC#7
USBOC#8	AD14	USBOC#8
USBOC#9	AH18	USBOC#9

USBOC#0	C644	0.1U/10V	
USBOC#2	C646	0.1U/10V	
USBOC#4	C647	0.1U/10V	
USBOC#6	C649	0.1U/10V	
USBOC#7	C650	0.1U/10V	
USBOC#8	C651	0.1U/10V	
USBOC#9	C652	0.1U/10V	

SI stage:add to avoid WWAN Noise

SPI_CS1_R# → R501 1K, R411 *1K

Boot BIOS Strap

		GNT0#	SPI_CS1#
LPC	11	No stuff	No stuff
PCI	10	No stuff	Stuff
SPI	01	Stuff	No stuff

PCI DEVICES IRQ ROUTING

DEVICE	IDSEL #	REQ/GNT #	PCI_INT
CardBus	AD22	2	C,D,E

U17B

(20) AD[31..0]

PCI

AD0	D20	REQ0#	A4 → REQ0# → PAD T74
AD1	E19	GNT0#	D7 → GNT0# → PAD T140
AD2	D19	REQ1#/GPIO50	E18 → REQ1# → PAD T127
AD3	A20	GNT1#/GPIO51	C18 → GNT1# → PAD T123
AD4	D17	REQ2#/GPIO52	B19 → REQ2# → REQ2# (20)
AD5	A21	GNT2#/GPIO53	F18 → GNT2# → GNT2# (20)
AD6	A19	REQ3#/GPIO54	A11 → REQ3# → PAD T70
AD7	C19	GNT3#/GPIO55	C10 → GNT3# → PAD T134
AD8	A18		
AD9	B16	C/BE0#	C17 → C/BE0# → C/BE0# (20)
AD10	A12	C/BE1#	E15 → C/BE1# → C/BE1# (20)
AD11	E16	C/BE2#	F16 → C/BE2# → C/BE2# (20)
AD12	A14	C/BE3#	E17 → C/BE3# → C/BE3# (20)
AD13	G16		
AD14	A15	IRDY#	C8 → IRDY# → IRDY# (20)
AD15	B6	PAR	D9 → PAR → PAR (20)
AD16	C11	PCIRST#	G6 → PCI_RST#_G
AD17	A9	DEVSEL#	D16 → DEVSEL# → DEVSEL# (20)
AD18	D11	PERR#	A7 → PERR# → PERR# (20)
AD19	B12	PLOCK#	B7 → LOCK#
AD20	C12	SERR#	F10 → SERR_1# → SERR_1# (20)
AD21	D10	STOP#	C16 → STOP# → STOP# (20)
AD22	C7	TRDY#	C9 → TRDY# → TRDY# (20)
AD23	F13	FRAME#	A17 → FRAME# → FRAME# (20)
AD24	E11		
AD25	E13	PLTRST#	AG24 → PLT_RST-R# → PLT_RST-R# (7)
AD26	E12	PCICLK	B10 → CLK_PCI_ICH → CLK_PCI_ICH (17)
AD27	D8	PME#	G7 → PCI_PME# → PCI_PME# (20)
AD28	A6		
AD29	E8		
AD30	D6		
AD31	A3		

Interrupt I/F

INTA#	F9	PIRQA#	PIRQE#/GPIO2
INTB#	B5	PIRQB#	PIRQF#/GPIO3
INTC#	C5	PIRQC#	PIRQG#/GPIO4
INTD#	A10	PIRQD#	PIRQH#/GPIO5

(20) INTC#
(20) INTD#

F8 → INTE# → INTE# (20)
G11 → INTF#
F12 → INTG#
B3 → SES_INT → SES_INT (27)

ICH8M REV 1.0

CLK_PCI_ICH → R479 *10 → C525 *8.2P/16V

Reserved for EMI.
Place resister and cap close to ICH.

SERR_1# → D33 CH751H-40HPT → SERR# → SERR# (26)

SI stage:add to avoid leakage currurt

3V_S5 → R448 8.2K
SI stage:Change power source to avoid leakage current
(30) USBOC#5 → USBOC#5

RP30 8.2KX8

STOP#	6	5	REQ2#
	7	4	REQ1#
	8	3	FRAME#
	9	2	DEVSEL#
+3V	10	1	+3V

RP32 8.2KX8

INTF#	6	5	
INTG#	7	4	
REQ3#	8	3	
INTD#	9	2	TRDY#
+3V	10	1	SERR_1#

RP33 8.2KX8

IRDY#	6	5	REQ0#
INTA#	7	4	INTB#
INTE#	8	3	INTC#
LOCK#	9	2	PERR#
+3V	10	1	

Add Buffers as needed for Loading and fanout concerns.

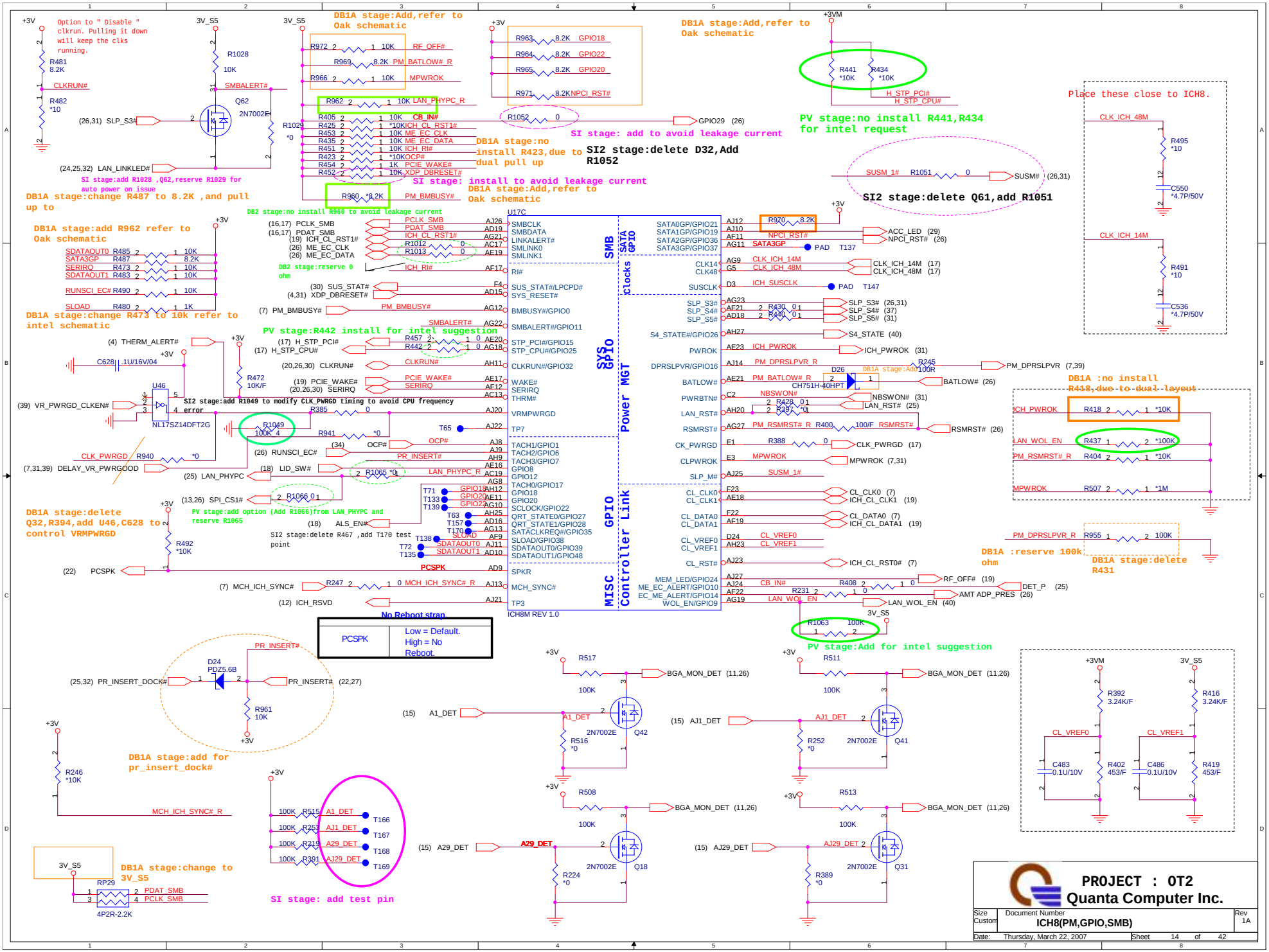
C539 0.047U/10V
U36 7SH32
PCI_RST#_G → PCIRST# (20)
R489 *0
R990 100K
DB1A stage:add

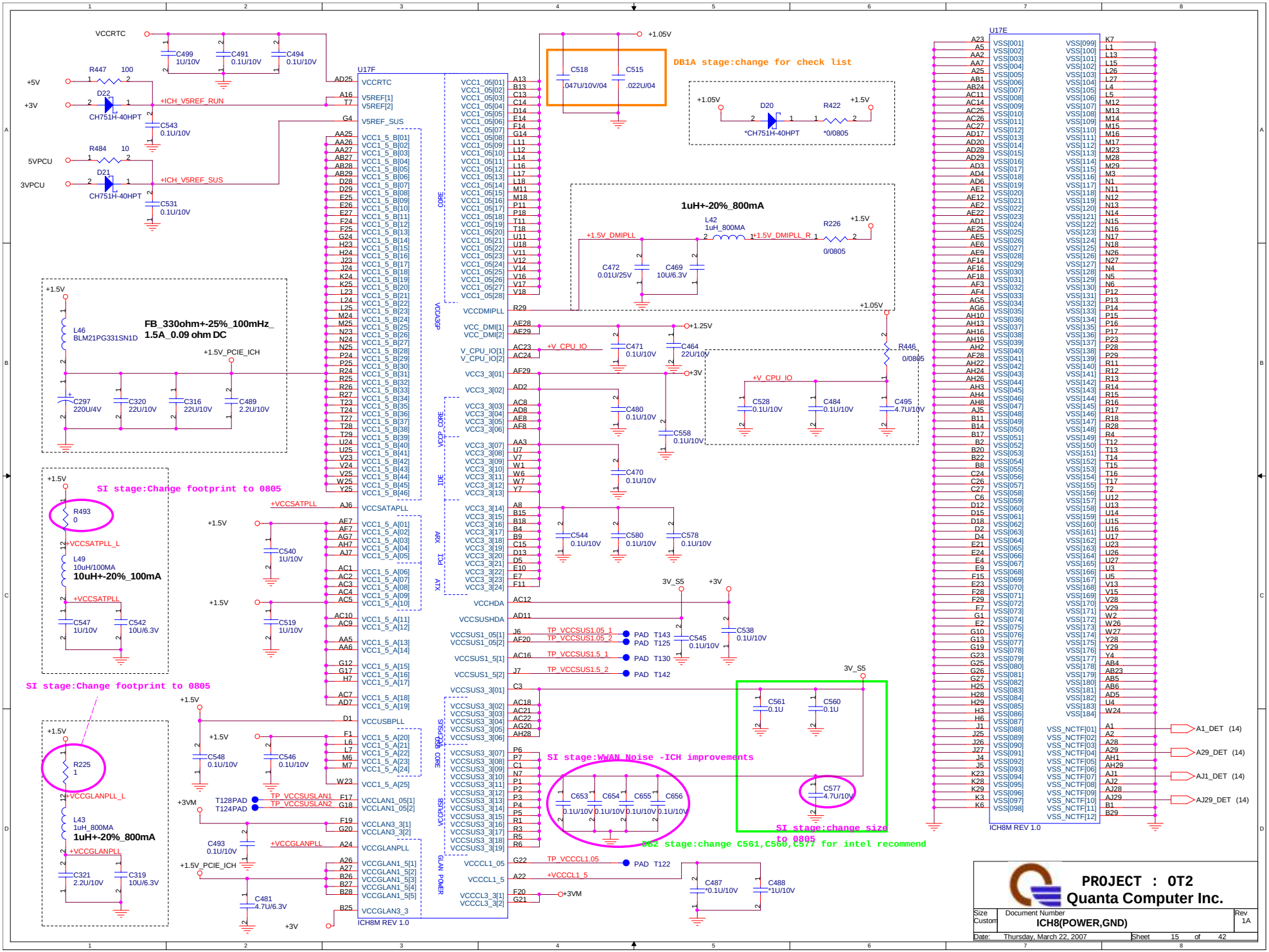
C490 0.047U/10V
U32 7SH32
PLT_RST-R# → PLTRST# (19,26,28,30)
R991 100K

PROJECT : 0T2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH8(USB,PCIE,DMI)	1A

Date: Thursday, March 22, 2007 Sheet 13 of 42


Option to " Disable " clkrun. Pulling it down will keep the clks running.
DB1A stage:Add,refer to Oak schematic
DB1A stage:Add,refer to Oak schematic
PV stage:no install R441,R434 for intel request
Place these close to ICH8.
SI stage:add R1028 ,Q62,reserve R1029 for auto power on issue
SI stage: add to avoid leakage current
DB1A stage:no install R423,due to dual pull up
SI2 stage:delete D32,Add R1052
SI stage: install to avoid leakage current
DB1A stage:Add,refer to Oak schematic
SI2 stage:delete Q61,add R1051
DB1A stage:change R487 to 8.2K ,and pull up to
DB2 stage:no install R960 to avoid leakage current
DB1A stage:add R962 refer to Oak schematic
DB2 stage:reserve 0 ohm
PV stage:R442 install for intel suggestion
DB1A stage:change R473 to 10k refer to intel schematic
SI2 stage:add R1049 to modify CLK_PWRGD timing to avoid CPU frequency error
DB1A :no install R418,due to dual layout
DB1A stage:delete Q32,R394,add U46,C628 to control VRMPWRGD
PV stage:add option (Add R1066)from LAN_PHYPC and reserve R1065
SI2 stage:delete R467 ,add T170 test point
DB1A :reserve 100k ohm
DB1A stage:delete R431
No Reboot strap
PCSPK
Low = Default.
High = No Reboot.
PV stage:Add for intel suggestion
DB1A stage:add for pr_insert_dock#
DB1A stage:change to 3V_S5
SI stage: add test pin
U17C
SMB
SATA GPIO
clocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
ICH8M REV 1.0
PROJECT : 0T2
Quanta Computer Inc.
ICH8(PM,GPIO,SMB)
Thursday, March 22, 2007
Sheet 14 of 42


VCCRTC
C499 1U/10V
C491 0.1U/10V
C494 0.1U/10V
+5V
+3V
R447 100
D22
CH751H-40HPT
+ICH_V5REF_RUN
C543 0.1U/10V
5VPCU
3VPCU
R484 10
D21
CH751H-40HPT
+ICH_V5REF_SUS
C531 0.1U/10V
U17F
VCCRTC
V5REF[1]
V5REF[2]
V5REF_SUS
VCC1_5_B[01]
VCC1_5_B[02]
VCC1_5_B[03]
VCC1_5_B[04]
VCC1_5_B[05]
VCC1_5_B[06]
VCC1_5_B[07]
VCC1_5_B[08]
VCC1_5_B[09]
VCC1_5_B[10]
VCC1_5_B[11]
VCC1_5_B[12]
VCC1_5_B[13]
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VCC1_5_A[20]
VCC1_5_A[21]
VCC1_5_A[22]
VCC1_5_A[23]
VCC1_5_A[24]
VCC1_5_A[25]
VCCLAN1_05[1]
VCCLAN1_05[2]
VCCLAN3_3[1]
VCCLAN3_3[2]
VCCGLANPLL
VCCGLAN1_5[1]
VCCGLAN1_5[2]
VCCGLAN1_5[3]
VCCGLAN1_5[4]
VCCGLAN1_5[5]
VCCGLAN3_3
ICH8M REV 1.0
VCC1_05[01]
VCC1_05[02]
VCC1_05[03]
VCC1_05[04]
VCC1_05[05]
VCC1_05[06]
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VCC1_05[10]
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VCCSUS3_3[19]
VCCCL1_05
VCCCL1_5
VCCCL3_3[1]
VCCCL3_3[2]
VCC3GDP
VCC3_GDP
VCC3_
VCC3_ATX
ATX
SUS3_CORE
CORE
VCCSUS3_3
GLAN POWER
C518 .047U/10V/04
C515 .022U/04
+1.05V
DB1A stage:change for check list
D20
*CH751H-40HPT
R422 *0/0805
1uH+-20%_800mA
L42 1uH_800MA
+1.5V_DMIPLL
+1.5V_DMIPLL_R
R226 0/0805
C472 0.01U/25V
C469 10U/6.3V
R446 0/0805
C471 0.1U/10V
C464 22U/10V
C480 0.1U/10V
C558 0.1U/10V
C528 0.1U/10V
C484 0.1U/10V
C495 4.7U/10V
C470 0.1U/10V
C544 0.1U/10V
C580 0.1U/10V
C578 0.1U/10V
+1.25V
+3V
+V_CPU_IO
3V_S5
C538 0.1U/10V
C545 0.1U/10V
TP_VCCSUS1.05_1
TP_VCCSUS1.05_2
TP_VCCSUS1.5_1
TP_VCCSUS1.5_2
PAD T143
PAD T125
PAD T130
PAD T142
C561 0.1U
C560 0.1U
C577 4.7U/10V
C653 0.1U/10V
C654 0.1U/10V
C655 0.1U/10V
C656 0.1U/10V
SI stage:WWAN Noise -ICH improvements
SI stage:change size to 0805
DB2 stage:change C561,C560,C577 for intel recommend
TP_VCCCL1.05
PAD T122
+VCCCL1_5
C487 *0.1U/10V
C488 *1U/10V
+3VM
L46 BLM21PG331SN1D
FB_330ohm+-25%_100mHz_ 1.5A_0.09 ohm DC
+1.5V_PCIE_ICH
C297 220U/4V
C320 22U/10V
C316 22U/10V
C489 2.2U/10V
SI stage:Change footprint to 0805
R493 0
+VCCSATPLL_L
L49 10uH/100MA
10uH+-20%_100mA
+VCCSATPLL
C547 1U/10V
C542 10U/6.3V
C540 1U/10V
C519 1U/10V
SI stage:Change footprint to 0805
R225 1
+VCCGLANPLL_L
L43 1uH_800MA
1uH+-20%_800mA
+VCCGLANPLL
C321 2.2U/10V
C319 10U/6.3V
C548 0.1U/10V
C546 0.1U/10V
T128PAD
T124PAD
TP_VCCSUSLAN1
TP_VCCSUSLAN2
C493 0.1U/10V
C481 4.7U/6.3V
U17E
VSS[001]
VSS[002]
VSS[003]
VSS[004]
VSS[005]
VSS[006]
VSS[007]
VSS[008]
VSS[009]
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VSS_NCTF[11]
VSS_NCTF[12]
ICH8M REV 1.0
A1_DET (14)
A29_DET (14)
AJ1_DET (14)
AJ29_DET (14)
PROJECT : 0T2
Quanta Computer Inc.
Size Custom
Document Number
ICH8(POWER,GND)
Rev 1A
Date: Thursday, March 22, 2007
Sheet 15 of 42

A is required to route to Top SoDIMM for AMT to function.This will need to change for M08

BOT

JDIM1

PC4800 DDR2 SDRAM SO-DIMM (200P)

FOX_AS0A426-M2SN-7F

Add for intel update

Add for intel update

Place these Caps near So-Dimm1.

Place these Caps near So-Dimm1.

Please these resistor closely DIMMA,all trace length<750 mil.

TOP

Layout note: Place 1 cap close to every 1 R-pack terminated to SMDDR_VTERM.

BOT

DB2 stage:on install for C327,C219---C331 for only one channel DIMM

DB2 stage:reaerve

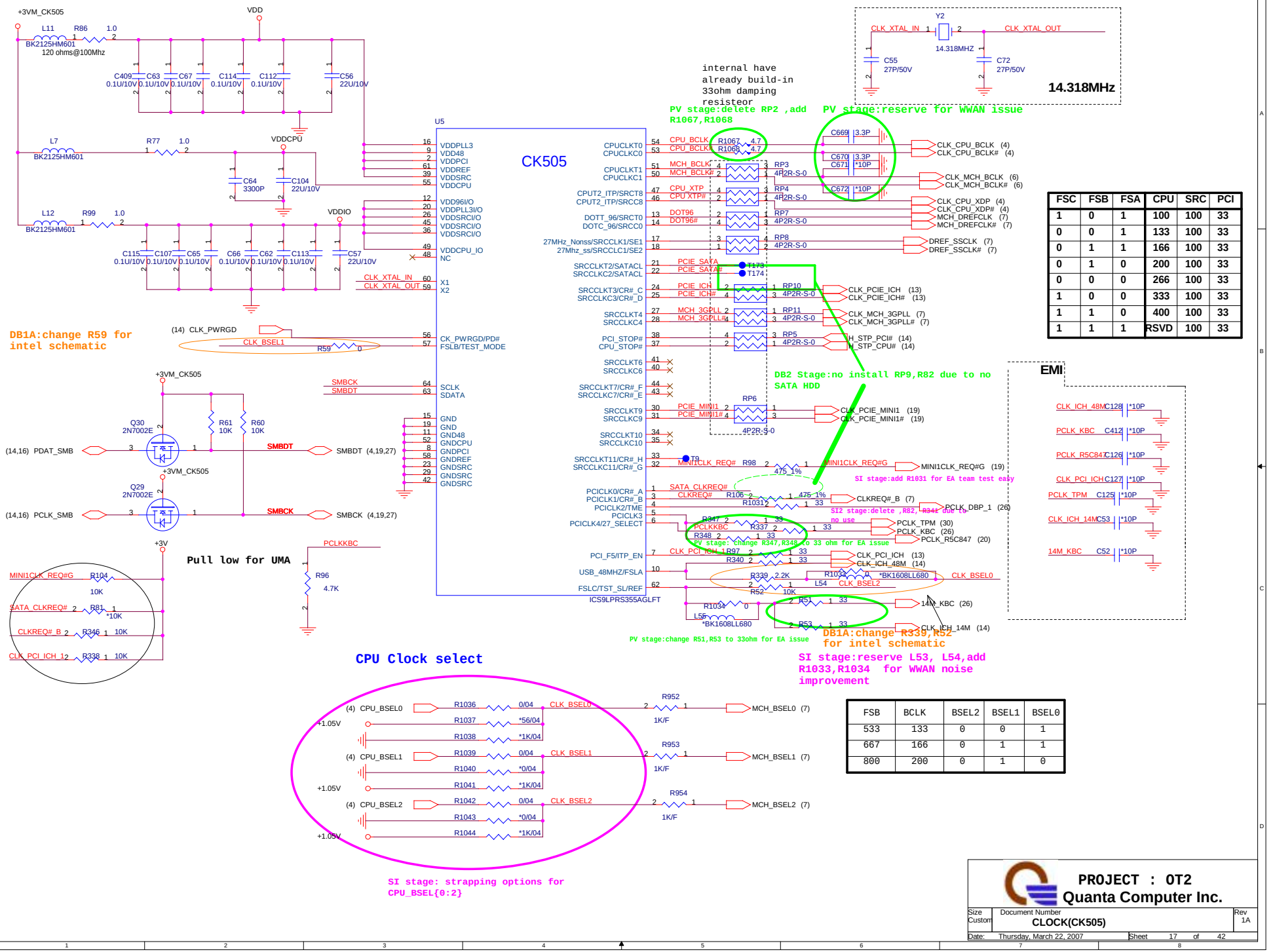
SMbus address A0

CLOCK 0,1
CKE 0,1

PROJECT : 0T2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR2 SO-DIMM(200P)	1A

Date: Thursday, March 22, 2007 Sheet 16 of 42



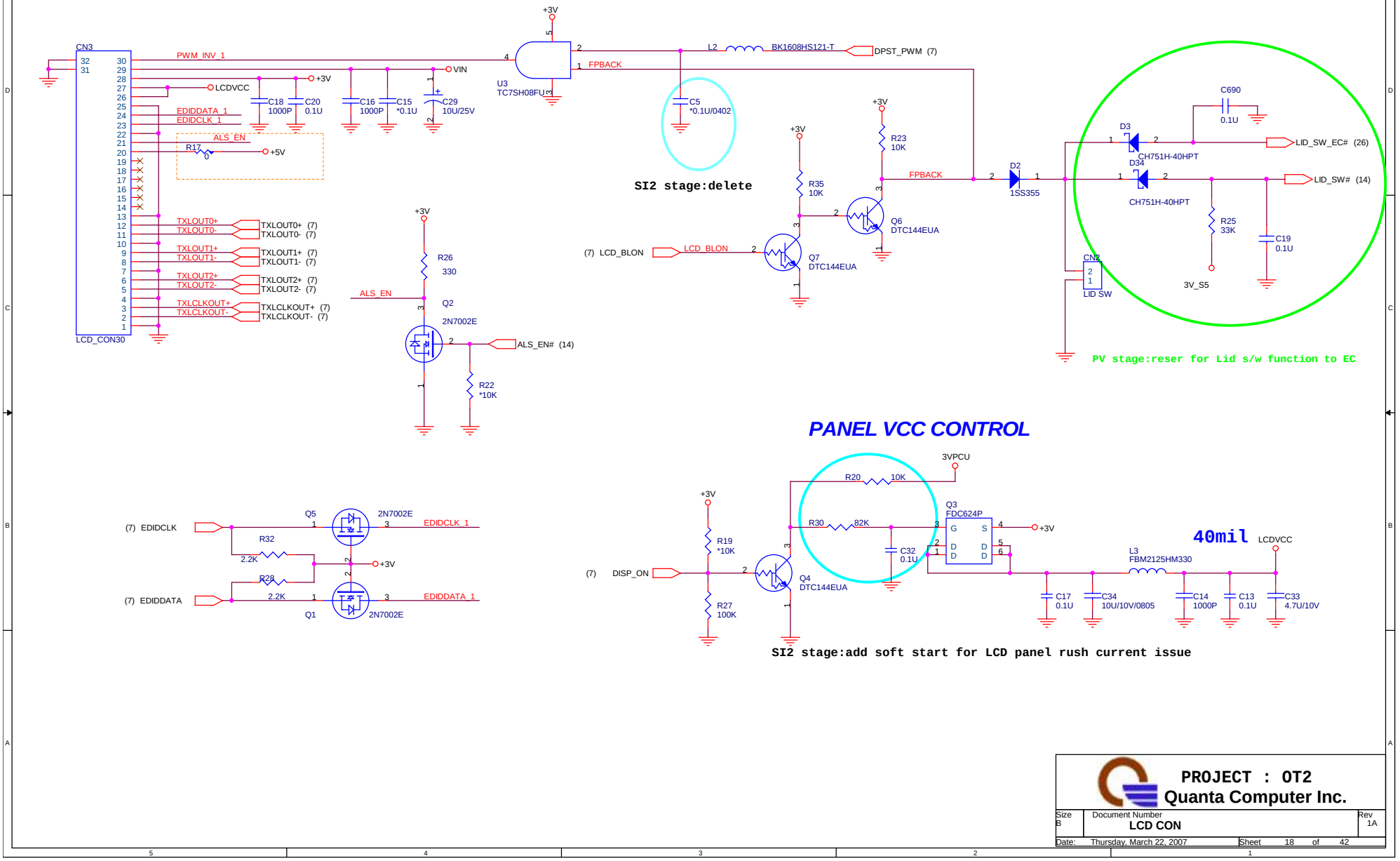
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

PROJECT : 0T2
Quanta Computer Inc.

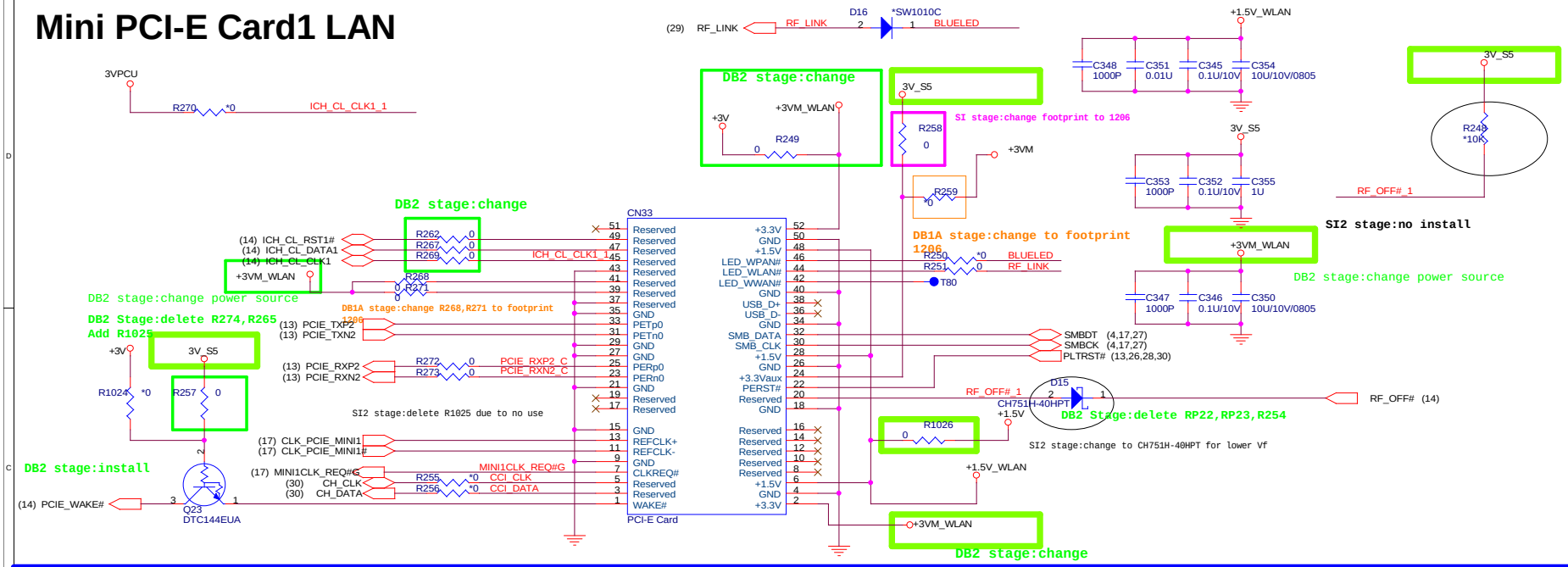
Size	Document Number	Rev
Custom	CLOCK(CK505)	1A

Date: Thursday, March 22, 2007 Sheet 17 of 42

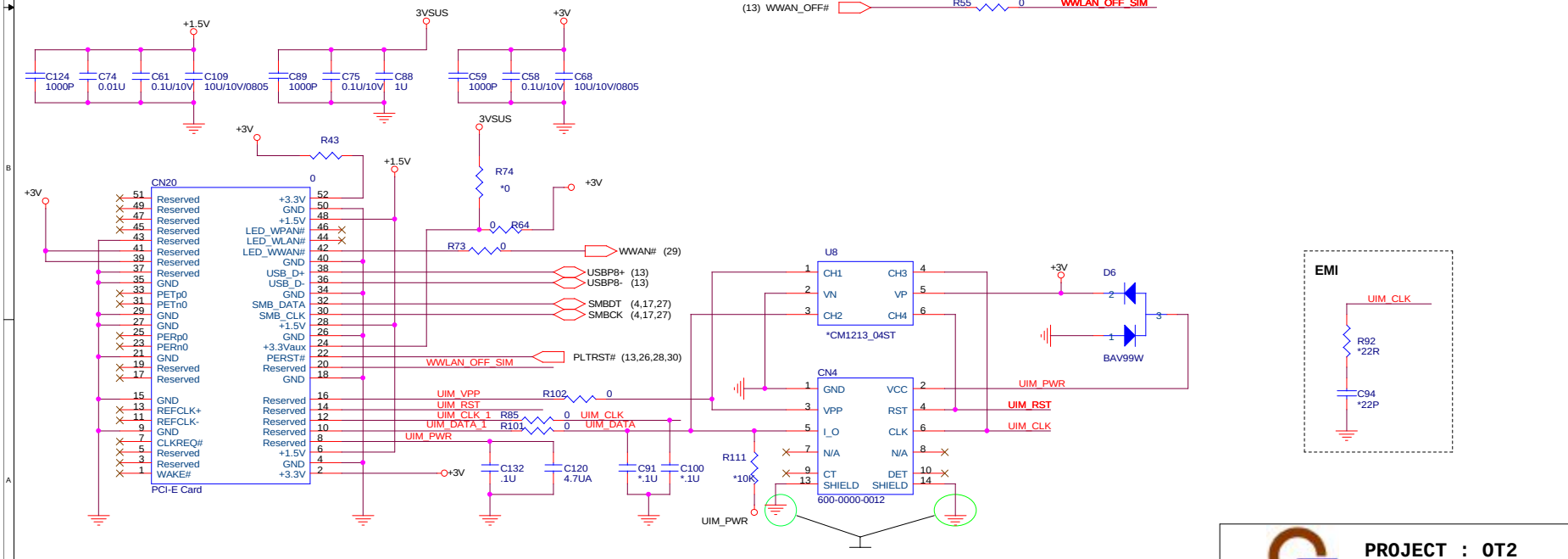


PROJECT : 0T2		
Quanta Computer Inc.		
Size: B	Document Number: LCD CON	Rev: 1A
Date: Thursday, March 22, 2007	Sheet 18 of 42	

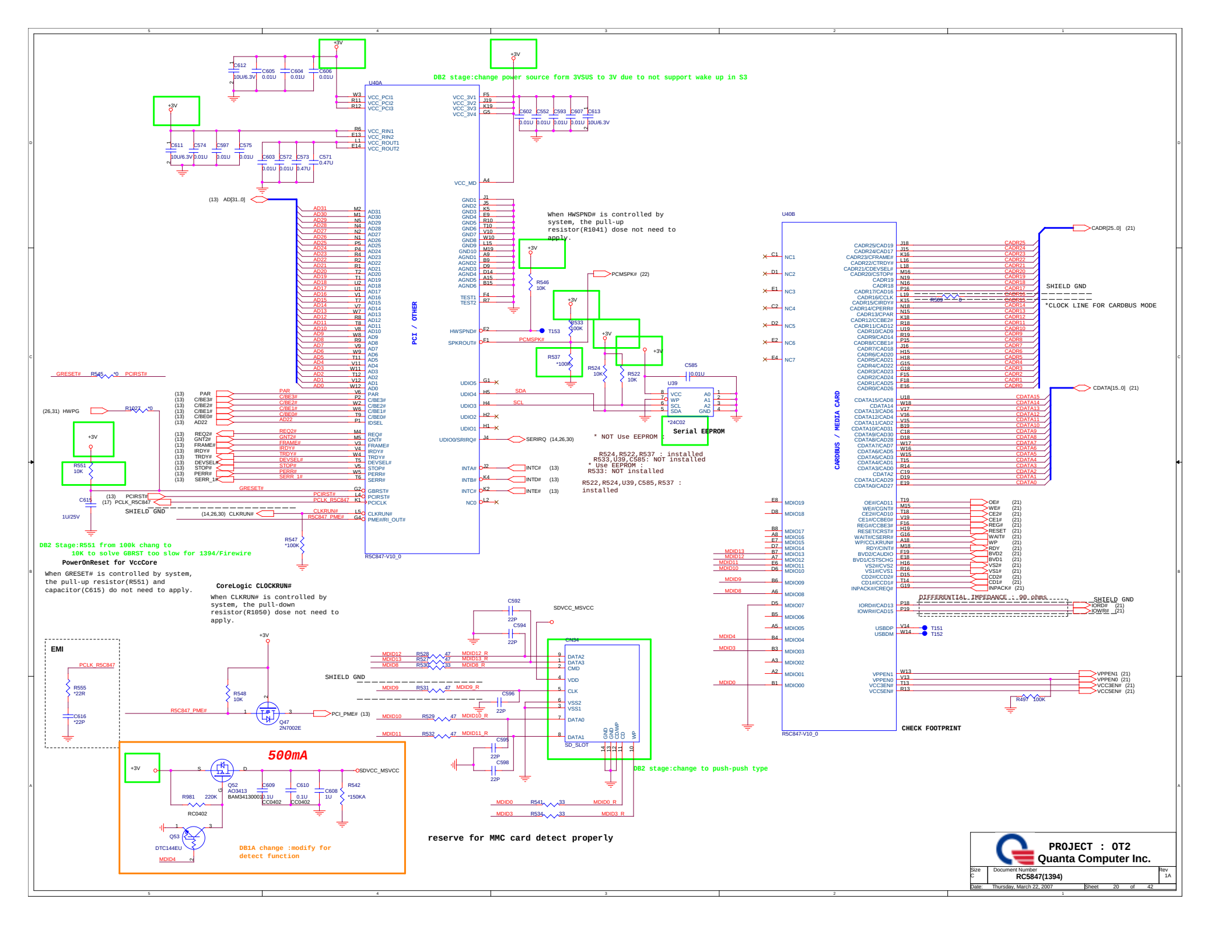
Mini PCI-E Card1 LAN

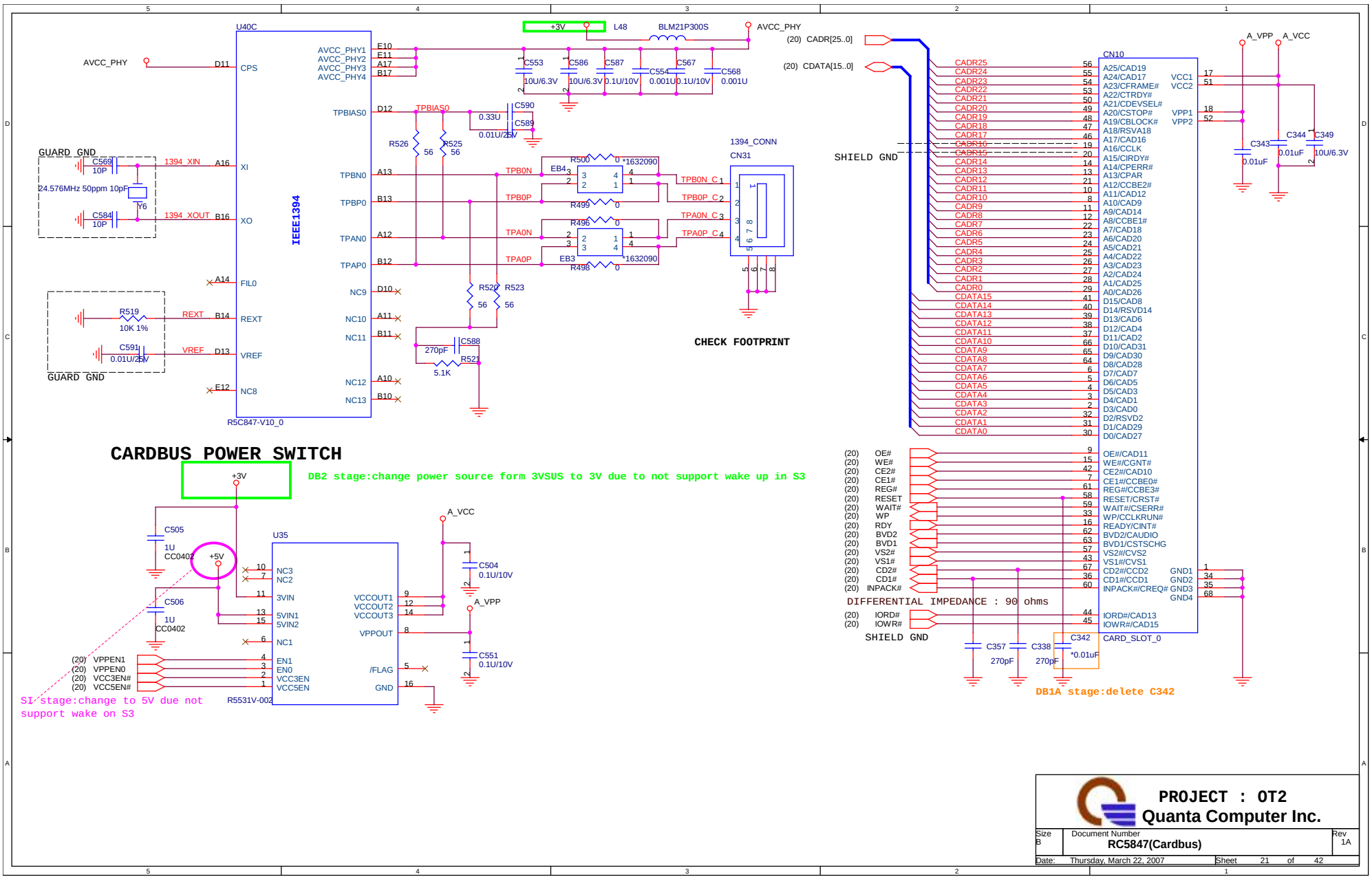


Mini PCI-E Card2 WWAN

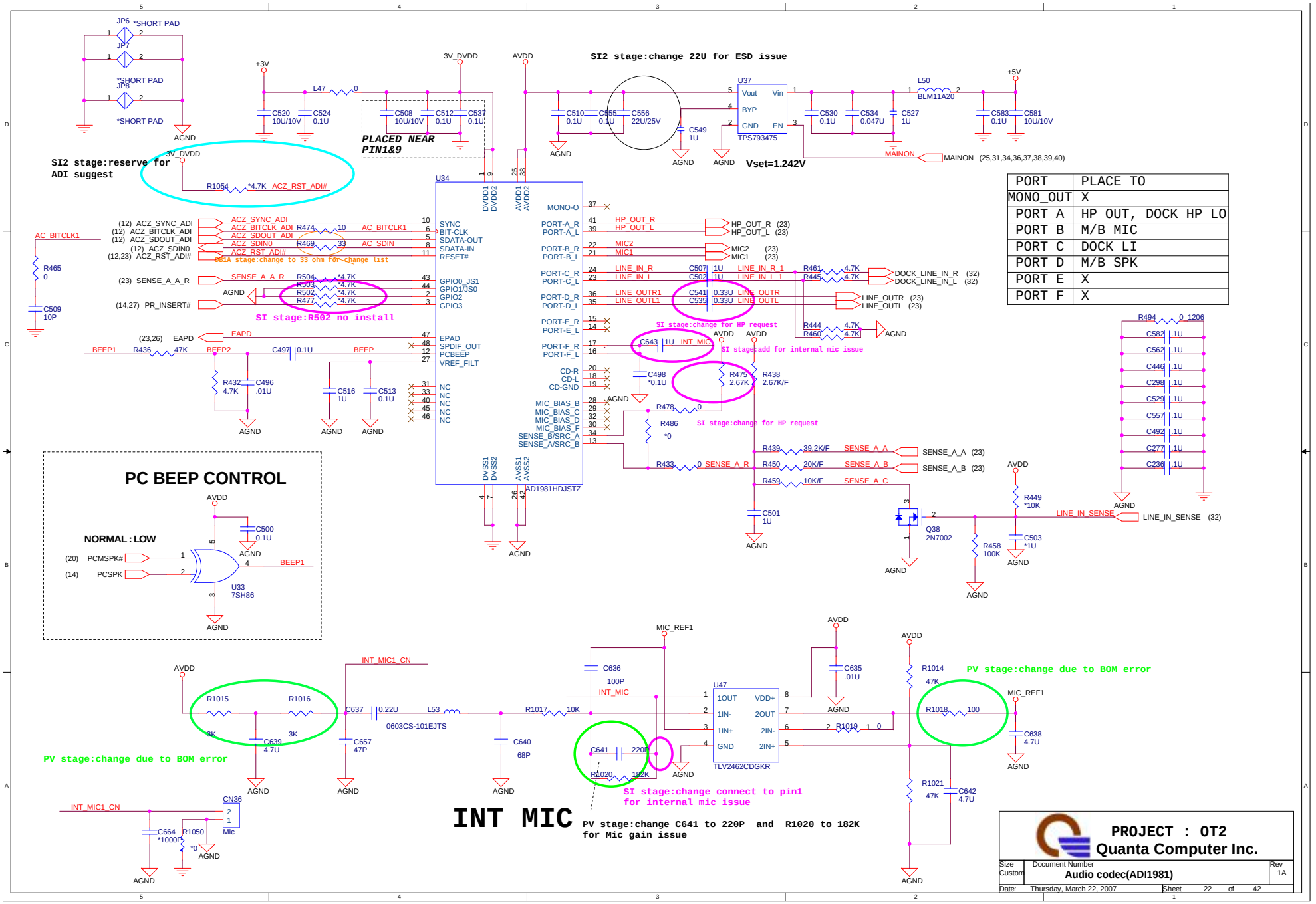


PROJECT : 0T2 Quanta Computer Inc.		
Size: Custom	Document Number: WAN/WWAN CARD	Rev: 1A
Date: Thursday, March 22, 2007	Sheet 19 of 42	

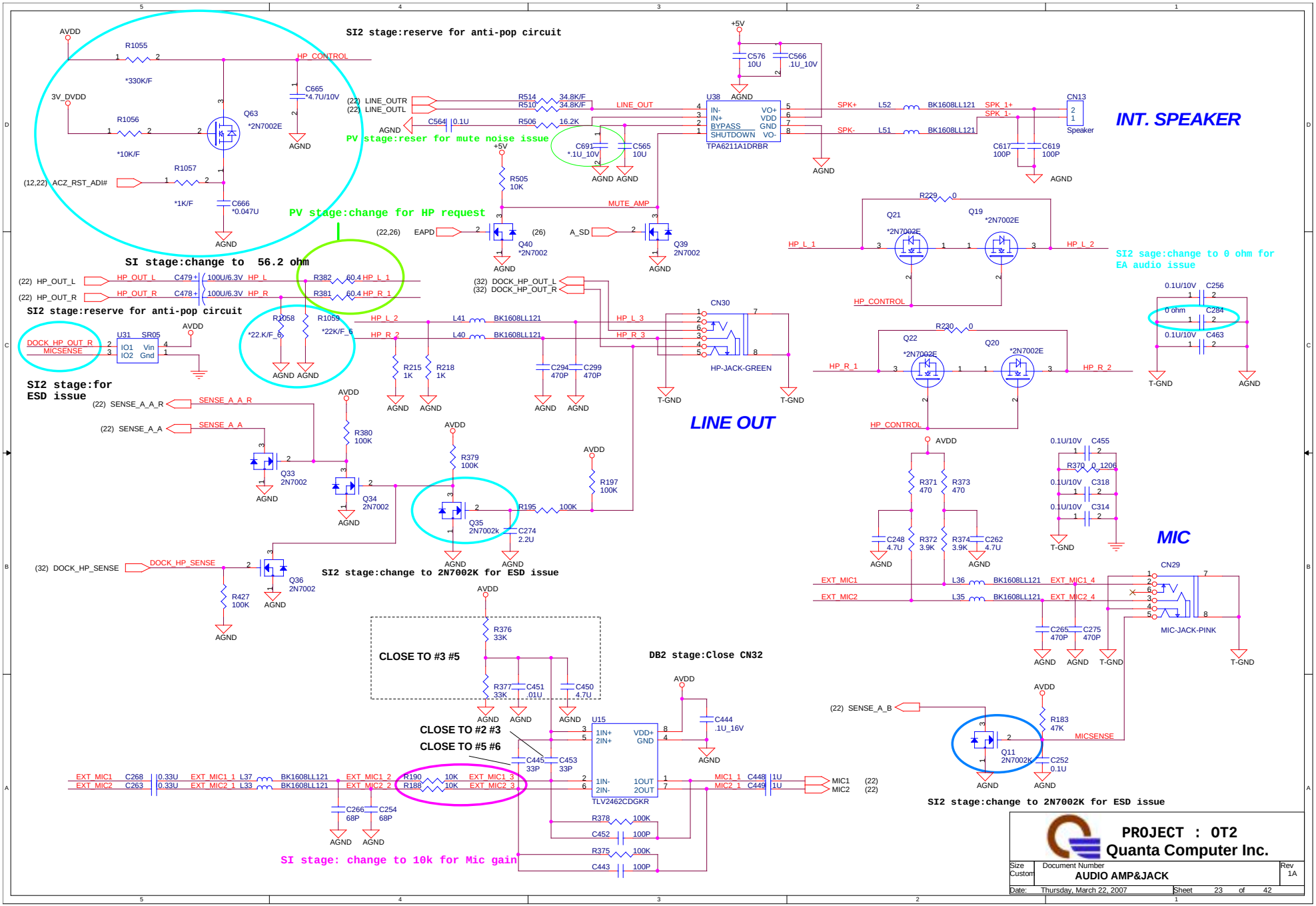

DB2 stage:change power source form 3VSUS to 3V due to not support wake up in S3
When HWSPND# is controlled by system, the pull-up resistor(R1041) dose not need to apply.
PCI / OTHER
CARDBUS / MEDIA CARD
Serial EEPROM
* NOT Use EEPROM :
R524,R522,R537 : installed
R533,U39,C585: NOT installed
* Use EEPROM :
R533: NOT installed
R522,R524,U39,C585,R537 : installed
DB2 Stage:R551 from 100k chang to 10K to solve GBRST too slow for 1394/Firewire
PowerOnReset for VccCore
When GRESET# is controlled by system, the pull-up resistor(R551) and capacitor(C615) do not need to apply.
CoreLogic CLOCKRUN#
When CLKRUN# is controlled by system, the pull-down resistor(R1050) dose not need to apply.
SHIELD GND
*CLOCK LINE FOR CARDBUS MODE
DIFFERENTIAL IMPEDANCE : 90 ohms
CHECK FOOTPRINT
EMI
500mA
DB1A change :modify for detect function
DB2 stage:change to push-push type
reserve for MMC card detect properly
PROJECT : 0T2
Quanta Computer Inc.
Document Number
RC5847(1394)
Rev 1A
Size C
Date: Thursday, March 22, 2007
Sheet 20 of 42



PROJECT : 0T2		
Quanta Computer Inc.		
Size: B	Document Number: RC5847(Cardbus)	Rev: 1A
Date: Thursday, March 22, 2007	Sheet 21 of 42	



PORT	PLACE TO
MONO_OUT	X
PORT A	HP OUT, DOCK HP LO
PORT B	M/B MIC
PORT C	DOCK LI
PORT D	M/B SPK
PORT E	X
PORT F	X


SI2 stage:reserve for anti-pop circuit
PV stage:reser for mute noise issue
PV stage:change for HP request
SI stage:change to 56.2 ohm
SI2 stage:reserve for anti-pop circuit
SI2 stage:for ESD issue
SI2 stage:change to 2N7002K for ESD issue
SI2 sage:change to 0 ohm for EA audio issue
SI2 stage:change to 2N7002K for ESD issue
DB2 stage:Close CN32
CLOSE TO #3 #5
CLOSE TO #2 #3
CLOSE TO #5 #6
SI stage: change to 10k for Mic gain
INT. SPEAKER
LINE OUT
MIC
HP-JACK-GREEN
MIC-JACK-PINK
TPA6211A1DRBR
TLV2462CDGKR
PROJECT : 0T2
Quanta Computer Inc.
AUDIO AMP&JACK
Thursday, March 22, 2007
Sheet 23 of 42

PV stage:reserve for EMI

GLAN_CLK

C689 *0.1U

JKCLK Pin
Power down 0MHz
10Mbps 5MHz
100Mbps 50MHz
1000Mbps 62.5MHz

SI stage:change to 1%

(12) GLAN_CLK — R84 33_F

Link Speed	LCI	GLCI
1000Mbps	Runing	Runing
100Mbps	Runing	Idle
10Mbps	Runing	Idle
No Link	Runing or power down	Idle
Power_down	Power_down	Power_down

(12) LAN_TXD0 — R320 — LAN_TXD0_R
(12) LAN_TXD1 — R334 — LAN_TXD1_R
(12) LAN_TXD2 — R327 — LAN_TXD2_R
(12) LAN_RXD0 — R324 — LAN_RXD0_R
(12) LAN_RXD1 — R315 — LAN_RXD1_R
(12) LAN_RXD2 — R313 — LAN_RXD2_R

(13) PCIE_RXP6 — C400 0.1U/10V — PCIE_RXP6_R
(13) PCIE_RXN6 — C404 0.1U/10V — PCIE_RXN6_R
(13) PCIE_TXP6
(13) PCIE_TXN6

Layout Note:
Place the resistors less than 1" from LAN controller.

R335 1.4K/F — LAN_KMRN_RCOMP_P — LAN_KMRN_RCOMP_N

(14,25,32) LAN_LINKLED#
(25,32) LOM_ACTLED#

(25) TX0P_R — TX0P_R
(25) TX0N_R — TX0N_R
(25) TX1P_R — TX1P_R
(25) TX1N_R — TX1N_R
(25) TX2P_R — TX2P_R
(25) TX2N_R — TX2N_R
(25) TX3P_R — TX3P_R
(25) TX3N_R — TX3N_R

R307 *0 — LAN_ATEST_P — LAN_ATEST_N

Layout Note:
Keep this resistor on top side.

Layout Note:
Connect the resistor to GND near ball E6

R336 1.4K/F — LAN_RBIAS_P

PAD T85 — R306 100/F

SI2 stage:add R1053 for LAN issue R1053

C410 27P/50V
Y4 25MHz
C411 27P/50V
LOM_XTAL2
LOM_XTAL1

DB2 stage:change to vender: KDS for intel recommend

U6

E2	JKCLK-JCLK		
E3	JRSTSYNC		
D1	JTXD0	LCI	
E3	JTXD1	LCI	
F1	JTXD2	LCI	
D3	JRXD0	LCI	
D2	JRXD1	LCI	
C1	JRXD2	LCI	
H2	GLAN_TXP-NC	GLCI	
J2	GLAN_TXN-NC	GLCI	
J4	GLAN_RXP-NC	GLCI	
H4	GLAN_RXN-NC	GLCI	
G7	KBIAS_P-RBIAS100	GLCI	
H7	KBIAS_N-RBIAS10	GLCI	
A4	LED0-LINK_UP_N		
B4	LED1-ACT_LED_N		
A5	LED2-SPEED_LED_N		
B8	MDI_PLUS[0]-TDP	MDI	
B9	MDI_MINUS[0]-TDN	MDI	
D9	MDI_PLUS[1]-RDP	MDI	
D8	MDI_MINUS[1]-RDN	MDI	
F9	MDI_PLUS[2]-NC	MDI	
F8	MDI_MINUS[2]-NC	MDI	
H8	MDI_PLUS[3]-NC	MDI	
H9	MDI_MINUS[3]-NC	MDI	
A7	IEEE_TEST_P-NC		
B7	IEEE_TEST_N-NC		
J6	RSVD_J6-NC		
J7	RSVD_J7-NC		
E7	RBIAS_P-NC		
E6	RBIAS_N-NC		
B5	RSVD_B5-NC		
A6	RSVD_A6-ADV10/LAN_DIS_N		
C5	RSVD_C5-NC		
B6	TEST_EN		
H5	XTAL2-X2		
H6	XTAL1-X1		
G1	JTAG_TCK-ISOL_TCK	JTAG	
H1	JTAG_TDI-ISOL_TI	JTAG	
G3	JTAG_TDO-TOUT	JTAG	
G2	JTAG_TMS-ISOL_EXEC	JTAG	

J9	VSSA[17]-NC	
J8	VSSA[16]-NC	
J5	VSSA[15]-VSSA2	
J3	VSSA[14]-VSS	
J1	VSSA[13]-NC	
G9	VSSA[12]-VSS	
G8	VSSA[11]-VSS	
G6	VSSA[10]-VSS	
F6	VSSA[09]-VSS	
E9	VSSA[08]-VSS	
D6	VSSA[07]-VSS	
C9	VSSA[06]-VSS	
C8	VSSA[05]-VSS	
C7	VSSA[04]-VSS	
C6	VSSA[03]-VSSR	
A9	VSSA[02]-NC	
A8	VSSA[01]-VSS	
F4	VSS[04]-VSS	
E1	VSS[03]-VSSP	
C4	VSS[02]-VSS	
A1	VSS[01]-NC	
F7	VDD1P0[03]-VCCA	+1.0V_LOM
E8	VDD1P0[02]-VCCT	
D7	VDD1P0[01]-VCCR	
E5	VCCF1P0-VCC	
H3	VCCFC1P0-VCC	
F2	VCC3P3[02]-VCCP	+3VM_LAN_SW
B3	VCC3P3[01]-VCC	
G5	VCC1P8[04]-NC	+1.8V_LOM
F5	VCC1P8[03]-NC	
D5	VCC1P8[02]-NC	
C2	VCC1P8[01]-NC	
G4	VCC1P0-VCCA2	+1.0V_LOM
E4	VCC[02]	
D4	VCC[01]	
B1	V1P0_OUT-NC	+1.8V_LOM
C3	CTRL_10-NC	CTRL_10
B2	CTRL_18-NC	CTRL_18
A2	THERM_D_P-NC	LAN_THERM_D_P
A3	THERM_D_N-NC	LAN_THERM_D_N

R305 *0

Layout Note:
Keep this resistor on top side.

NINEVEH-EKRON_N (REV 1p0)

PAD T14
PAD T16
PAD T90
PAD T15

R982 *200
R983 *200

DB1A stage:reserve

+3VM_LAN_SW

C396 0.1U/10V
C77 4.7U/10V

CTRL_10 — Q10 BCP69T1 — C377 0.01U/25V — C367 0.1U/10V — C40 4.7U/10V — C78 10U/6.3V — +1.0V_LOM
CTRL_18 — Q9 BCP69T1 — C376 0.01U/25V — C368 0.1U/10V — C54 4.7U/10V — C70 10U/6.3V — +1.8V_LOM

TX1N_R TX1P_R — R317 49.9/F — R321 49.9/F — C391 0.1U/10V
TX0N_R TX0P_R — R314 49.9/F — R311 49.9/F — C385 0.1U/10V
TX2N_R TX2P_R — R325 49.9/F — R328 49.9/F — C397 0.1U/10V
TX3N_R TX3P_R — R330 49.9/F — R332 49.9/F — C407 0.1U/10V

Layout Note:
Place termination resistors close to LAN controller(less than 0.25").

+1.8V_LOM
C71 22U/4V — C406 0.1U/10V — C402 0.1U/10V — C395 0.1U/10V — C388 0.1U/10V — C375 0.1U/10V — C382 470P/50V

+1.0V_LOM
C69 22U/4V — C378 0.1U/10V — C401 0.1U/10V — C393 0.1U/10V — C387 0.1U/10V — C379 0.1U/10V — C405 0.1U/10V — C394 0.1U/10V — C380 0.1U/10V — C392 470P/50V

PROJECT : 0T2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LAN(Nineveh)	1A
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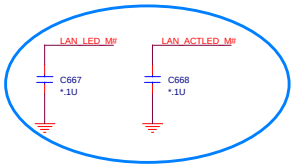
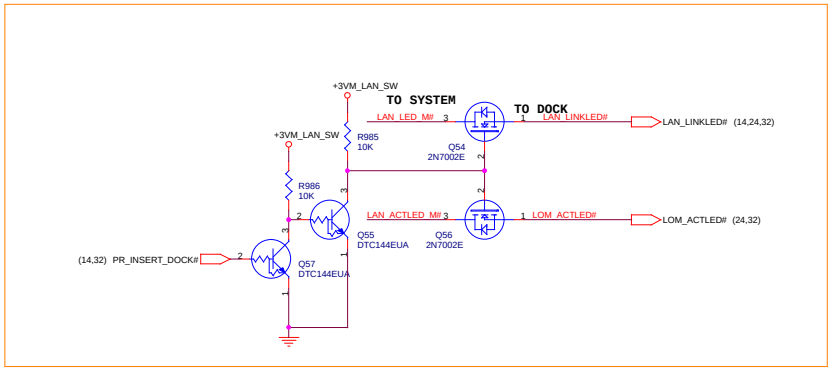
LAN

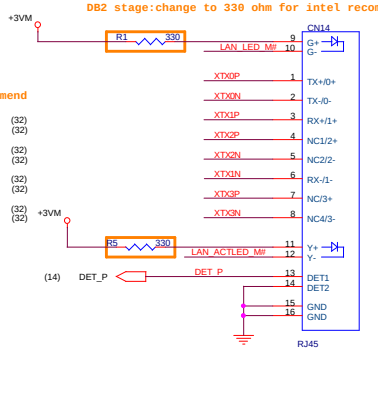
RJ45 Connector

SI2 stage:EMI suggest

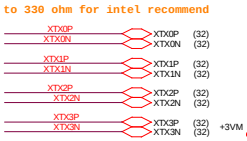


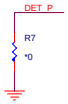


DB2 stage:change to 330 ohm for intel recommend



DB2 stage:change to 330 ohm for intel recommend



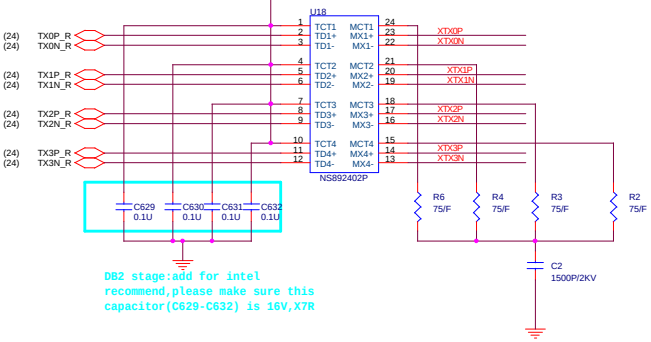


DB1A tage:Remove U1, RP24, RP25, RP26, RP27, and RP1,C24,C26,C28,R941-R951

DB2 stage:change to +1.8V_LOM for intel recommend

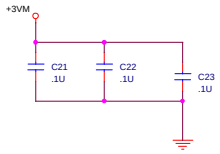
LAN TRANSFORMER

PV stage:add for EMI



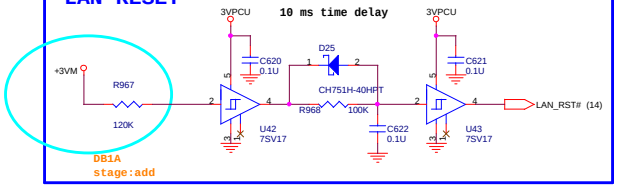
DB2 stage:add for intel recommend,please make sure this capacitor(C629-C632) is 16V,X7R

SI2 stage:change power source for HP request



PVstage:delete C27

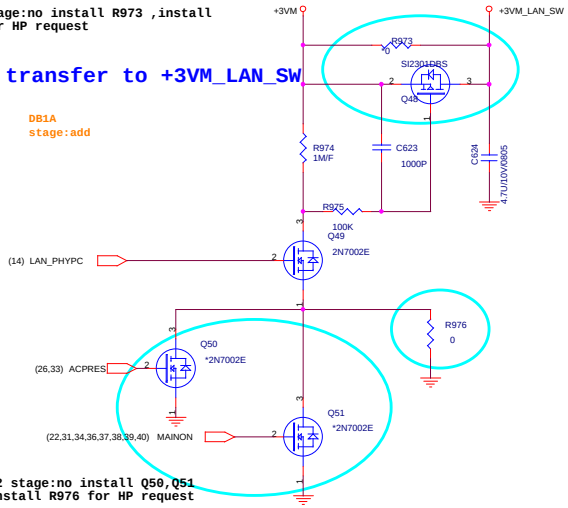
LAN RESET



SI2 stage:no install R973 ,install Q48 for HP request

+3VM transfer to +3VM_LAN_SW

DB1A
stage:add

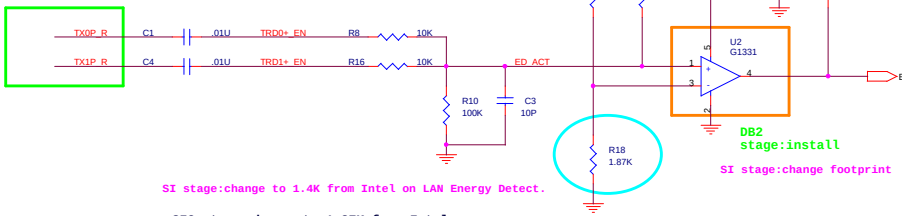


SI2 stage:no install Q50,Q51 ,install R976 for HP request

PV stage:change to +3VM for ACBS issue

LAN Energy Detect circuit

82556 Support Deep Smart Power Down Feature for power saving



DB2
stage:install

SI stage:change footprint

SI stage:change to 1.4K from Intel on LAN Energy Detect.

SI2 stage:change to 1.87K for Intel suggestion

PROJECT : 0T2
Quanta Computer Inc.

Size	Document Number	Rev
C	Transformer&RJ45	1A

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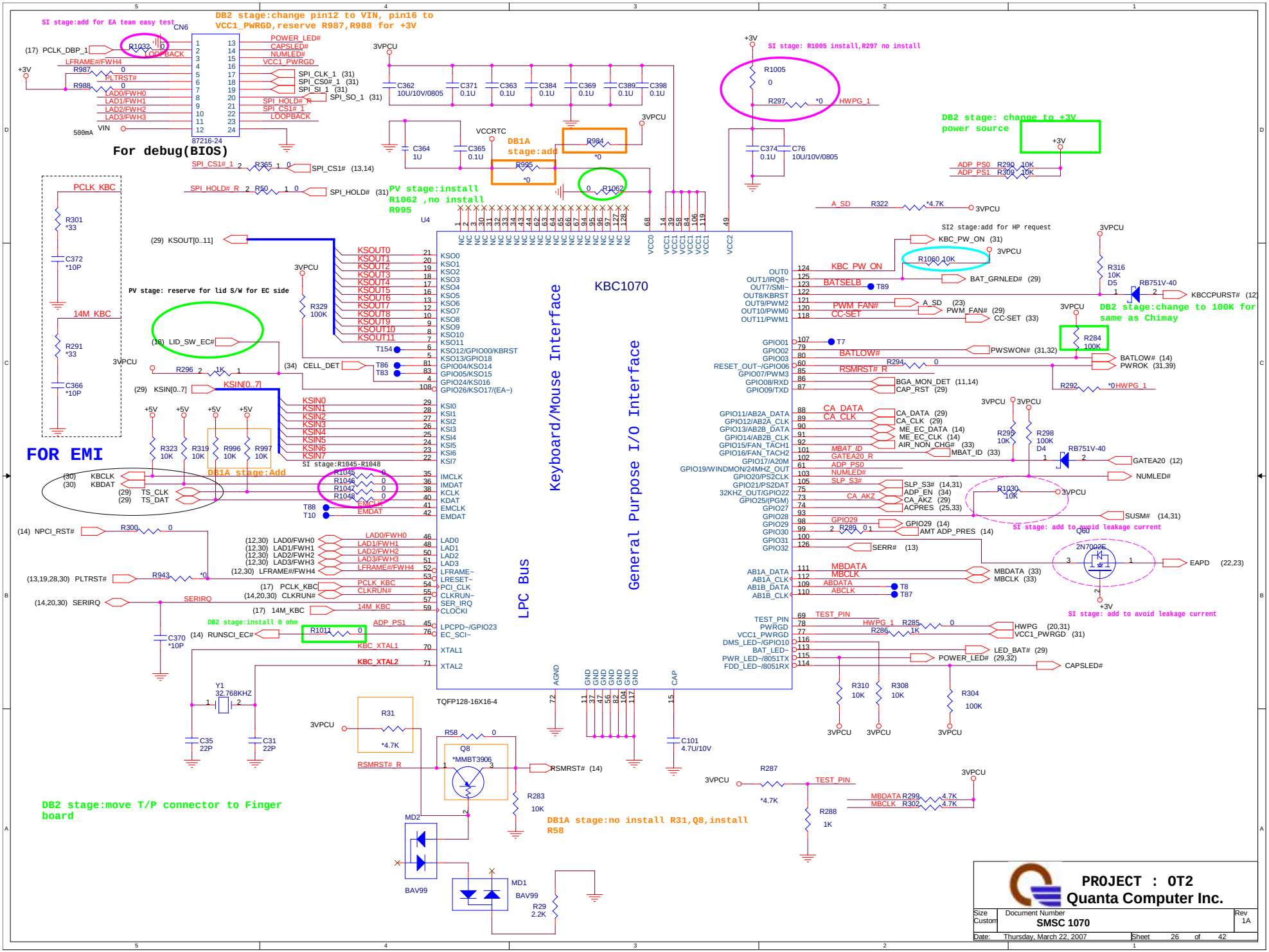
SI stage:add for EA team easy test
DB2 stage:change pin12 to VIN, pin16 to VCC1_PWRGD,reserve R987,R988 for +3V
CN6
87216-24
For debug(BIOS)
SI stage: R1005 install,R297 no install
DB2 stage: change to +3V power source
DB1A stage:add
PV stage:install R1062 ,no install R995
U4
KBC1070
Keyboard/Mouse Interface
General Purpose I/O Interface
LPC Bus
TQFP128-16X16-4
PV stage: reserve for lid S/W for EC side
FOR EMI
DB1A stage:Add
SI stage:R1045-R1048
DB2 stage:install 0 ohm
DB2 stage:move T/P connector to Finger board
DB1A stage:no install R31,Q8,install R58
SI2 stage:add for HP request
DB2 stage:change to 100K for same as Chimay
SI stage: add to avoid leakage current
SI stage: add to avoid leakage current
PROJECT : 0T2
Quanta Computer Inc.
SMSC 1070
Thursday, March 22, 2007
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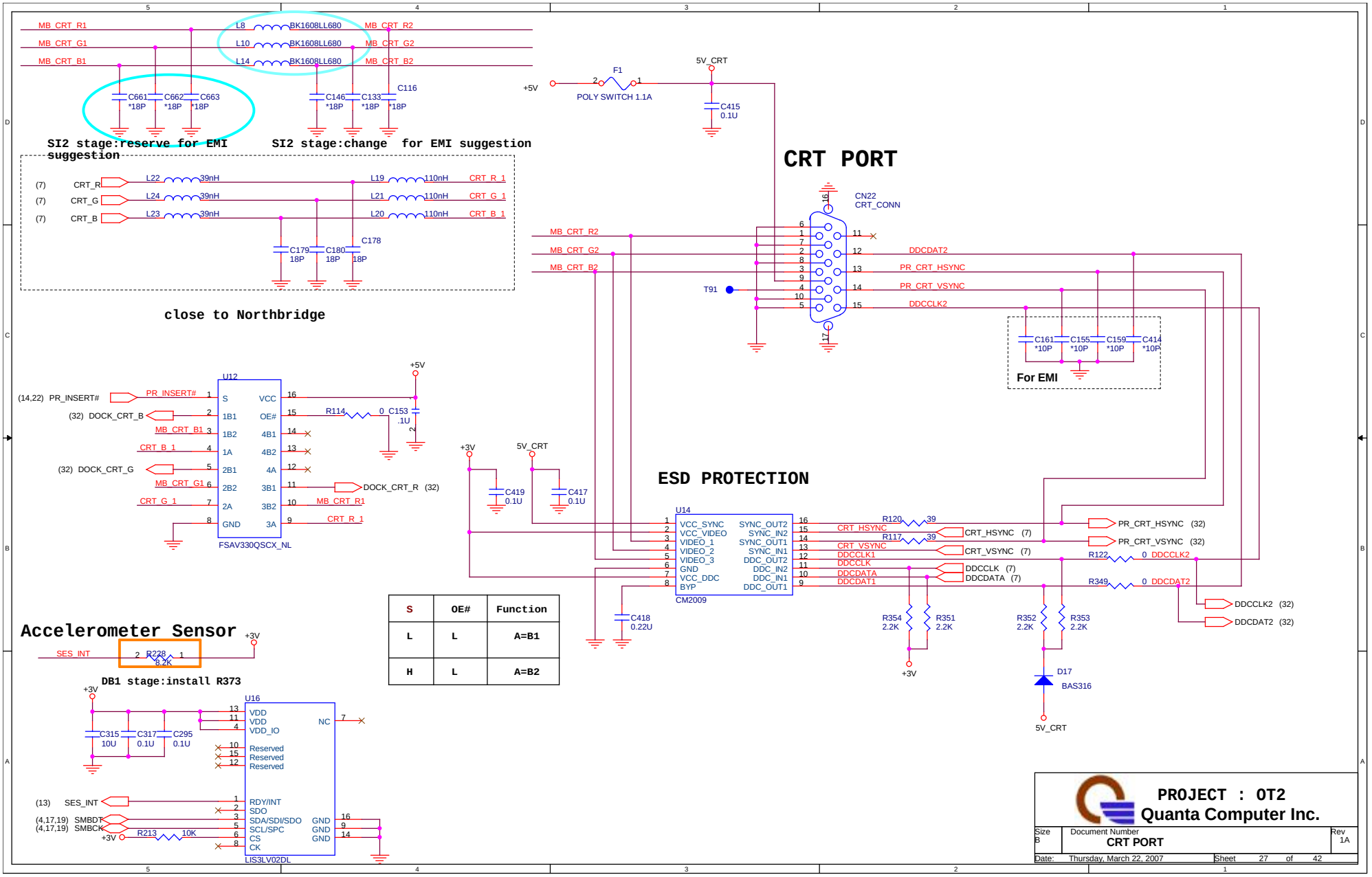

S	OE#	Function
L	L	A=B1
H	L	A=B2

Quanta Computer Inc.

PROJECT : 0T2

Size	Document Number	Rev
B	CRT PORT	1A

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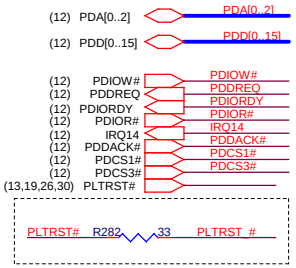
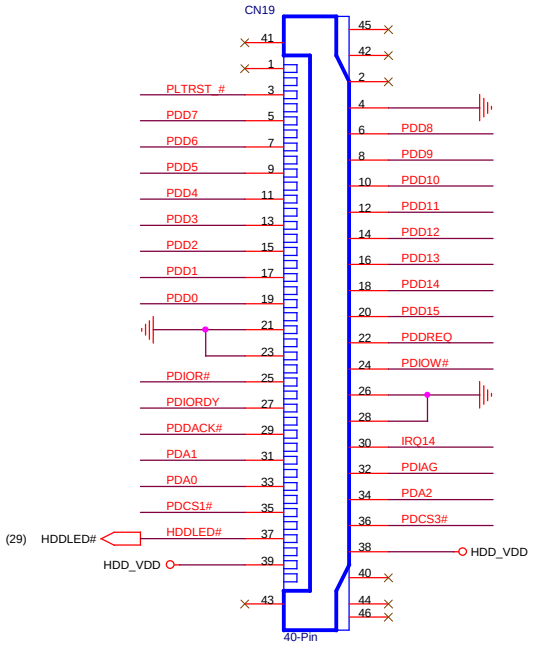
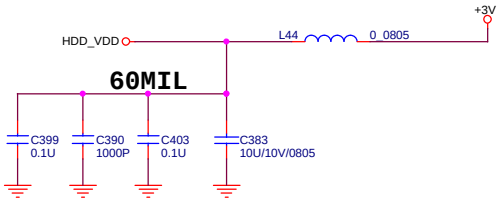
HDD, CD-ROM



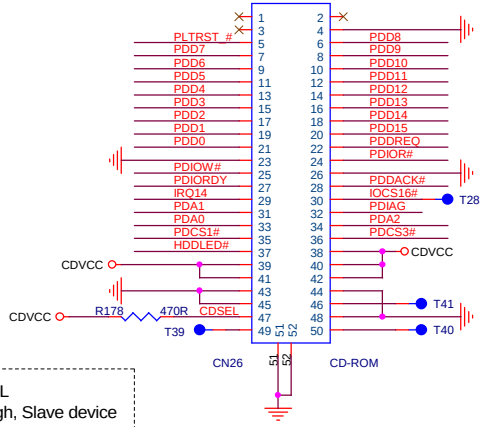
1.8 inch HDD CONNECTOR



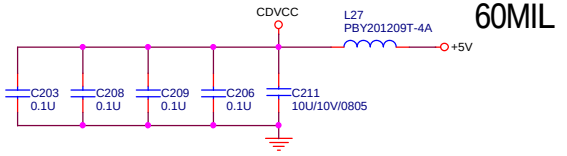


DB2 Stage:delete CN9,R463,C533,C532,C522,C523,C511,R488

CD-ROM



CDSEL
--> High, Slave device



PROJECT : 0T2
Quanta Computer Inc.

Size	Document Number	Rev
B	HDD,CD-ROM	1A

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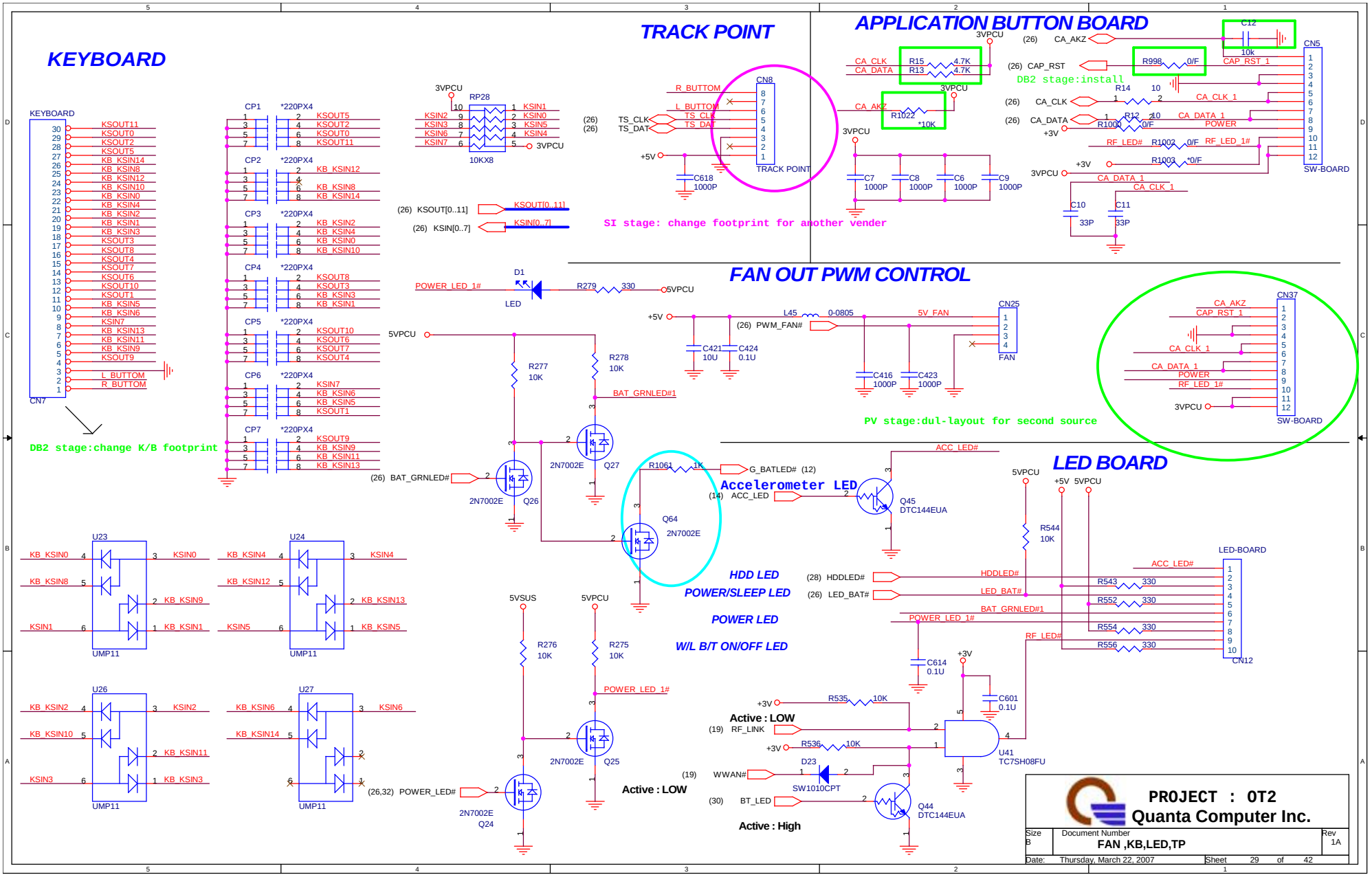
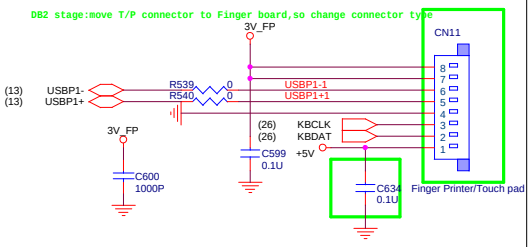

KEYBOARD
TRACK POINT
APPLICATION BUTTON BOARD
FAN OUT PWM CONTROL
LED BOARD
SI stage: change footprint for another vender
DB2 stage:install
PV stage:dul-layout for second source
DB2 stage:change K/B footprint
Accelerometer LED
HDD LED
POWER/SLEEP LED
POWER LED
W/L B/T ON/OFF LED
Active : LOW
Active : High
PROJECT : 0T2
Quanta Computer Inc.
FAN ,KB,LED,TP
Thursday, March 22, 2007

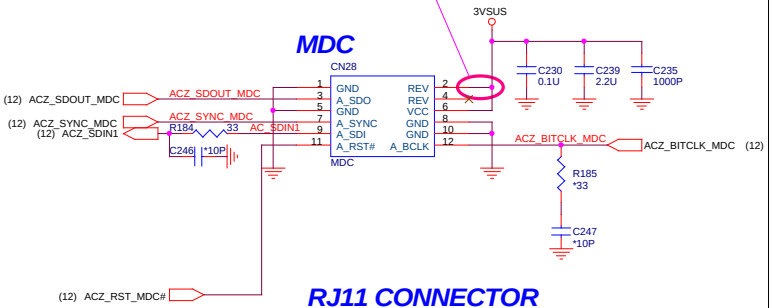
FINGER PRINT

DB2 stage:move T/P connector to Finger board,so change connector type

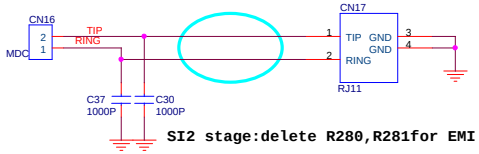


SI stage:it make for a much smoother transition when modems transition to deriving the IO voltage from that pin

MDC

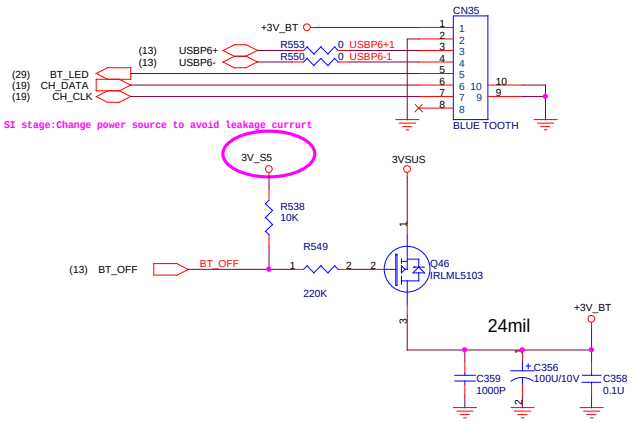


RJ11 CONNECTOR

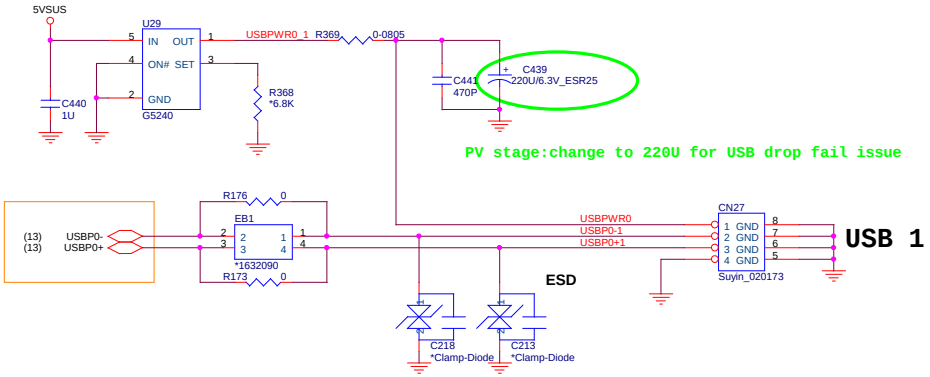


SI2 stage:delete R280,R281for EMI suggestion

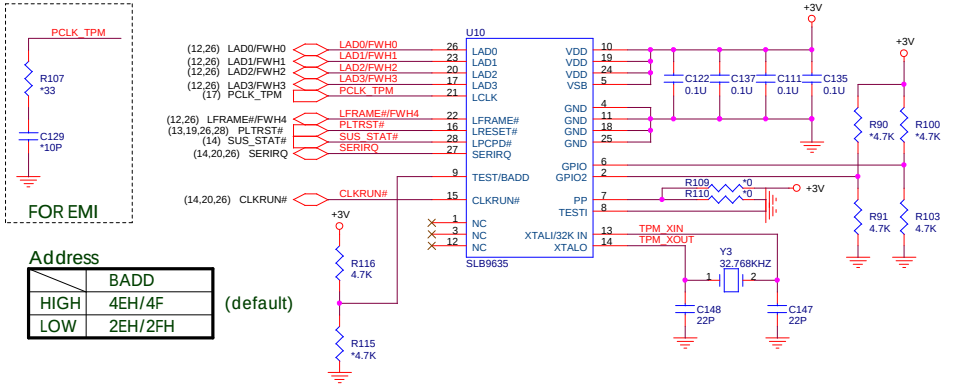
BLUE TOOTH



USB 1



TPM (1.2)



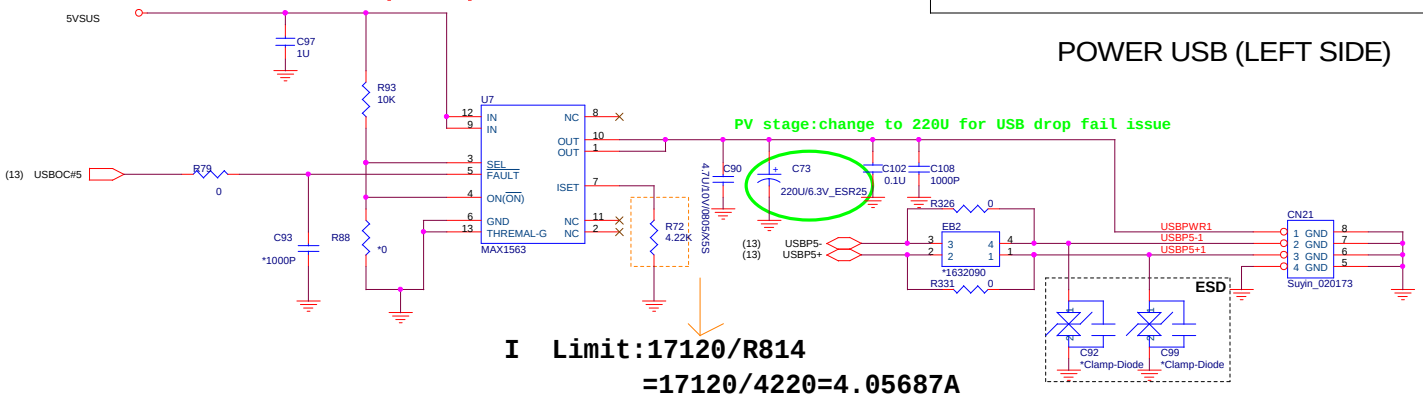
Address

	BADD
HIGH	4EH/4F
LOW	2EH/2FH

(default)

POWER USB (LEFT SIDE)

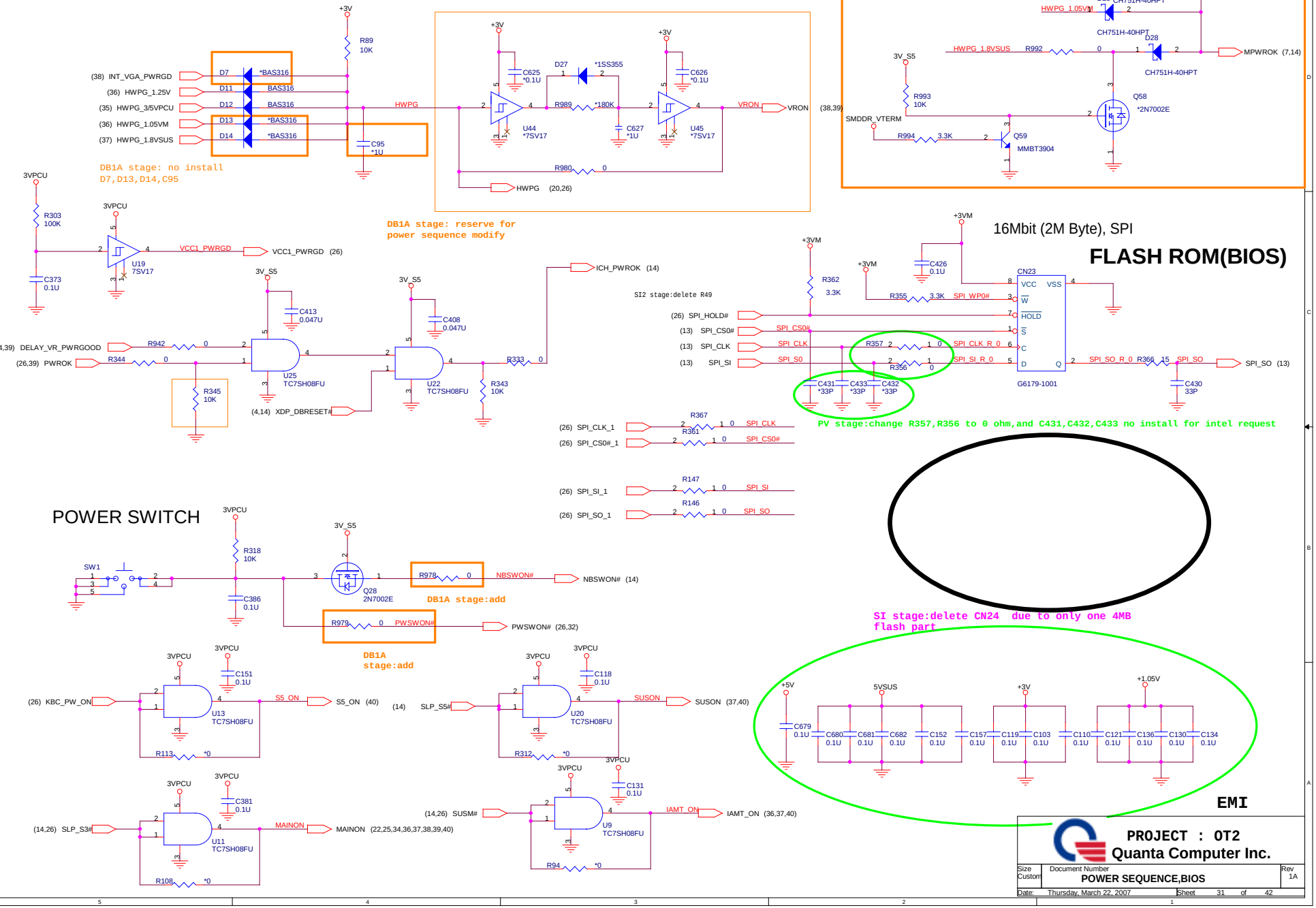
USB 2



I Limit:17120/R814
=17120/4220=4.05687A

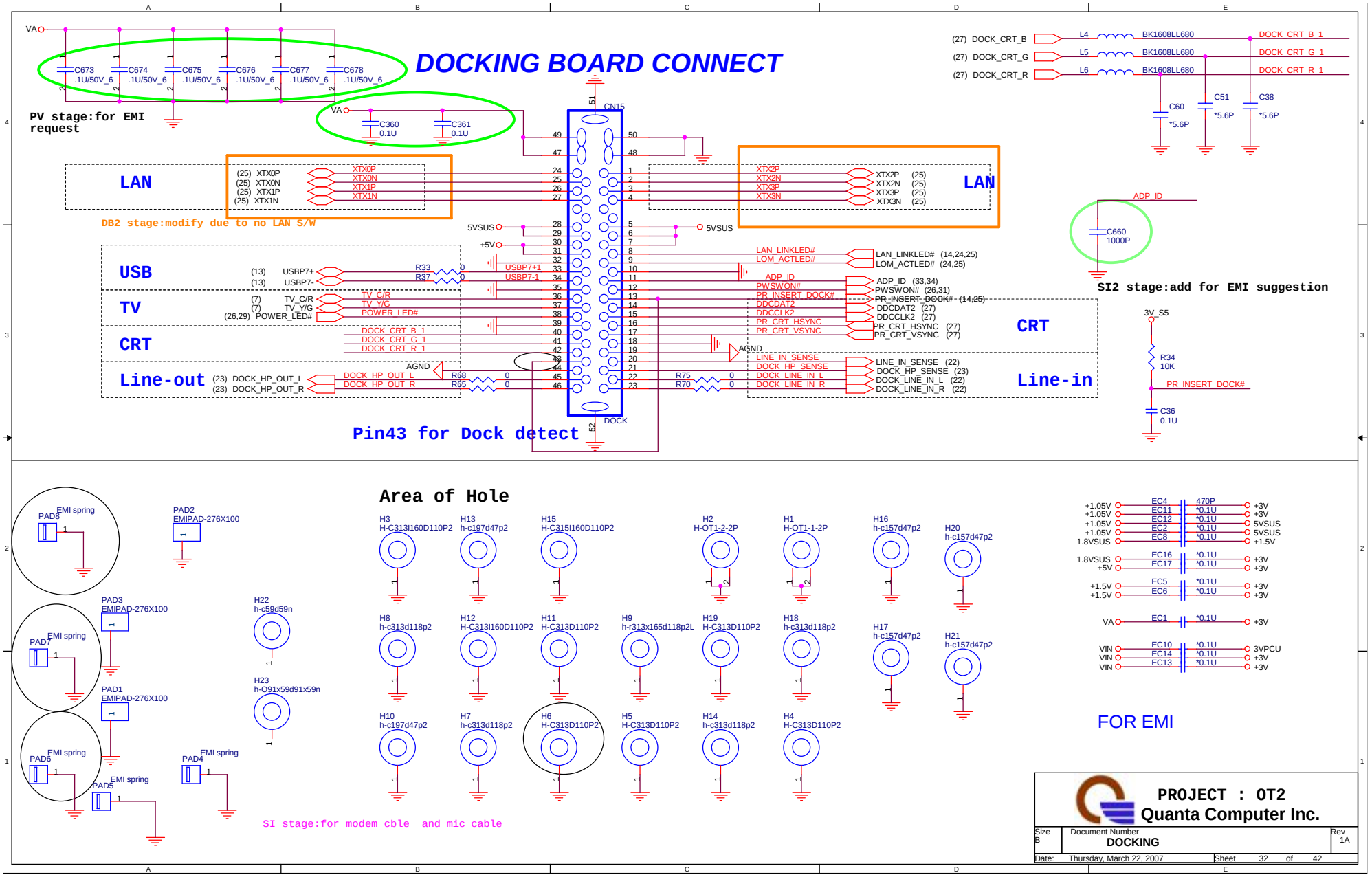
PROJECT : OT2			
Quanta Computer Inc.			
Size: Custom	Document Number: USB,BT,FP,TPM,MDC		Rev: 1A
Date: Thursday, March 22, 2007	Sheet 30 of 42		

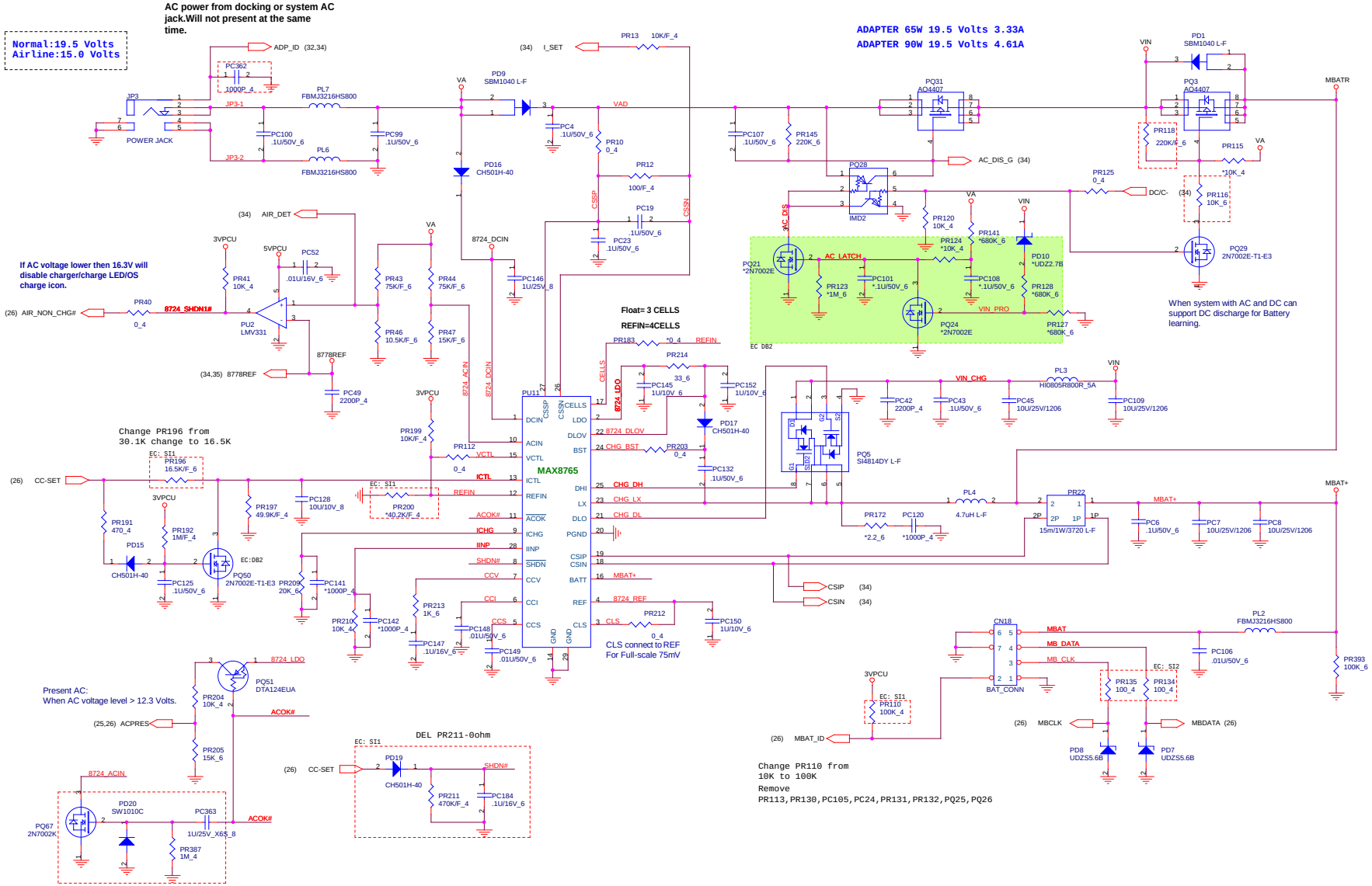
POWER SEQUENCE

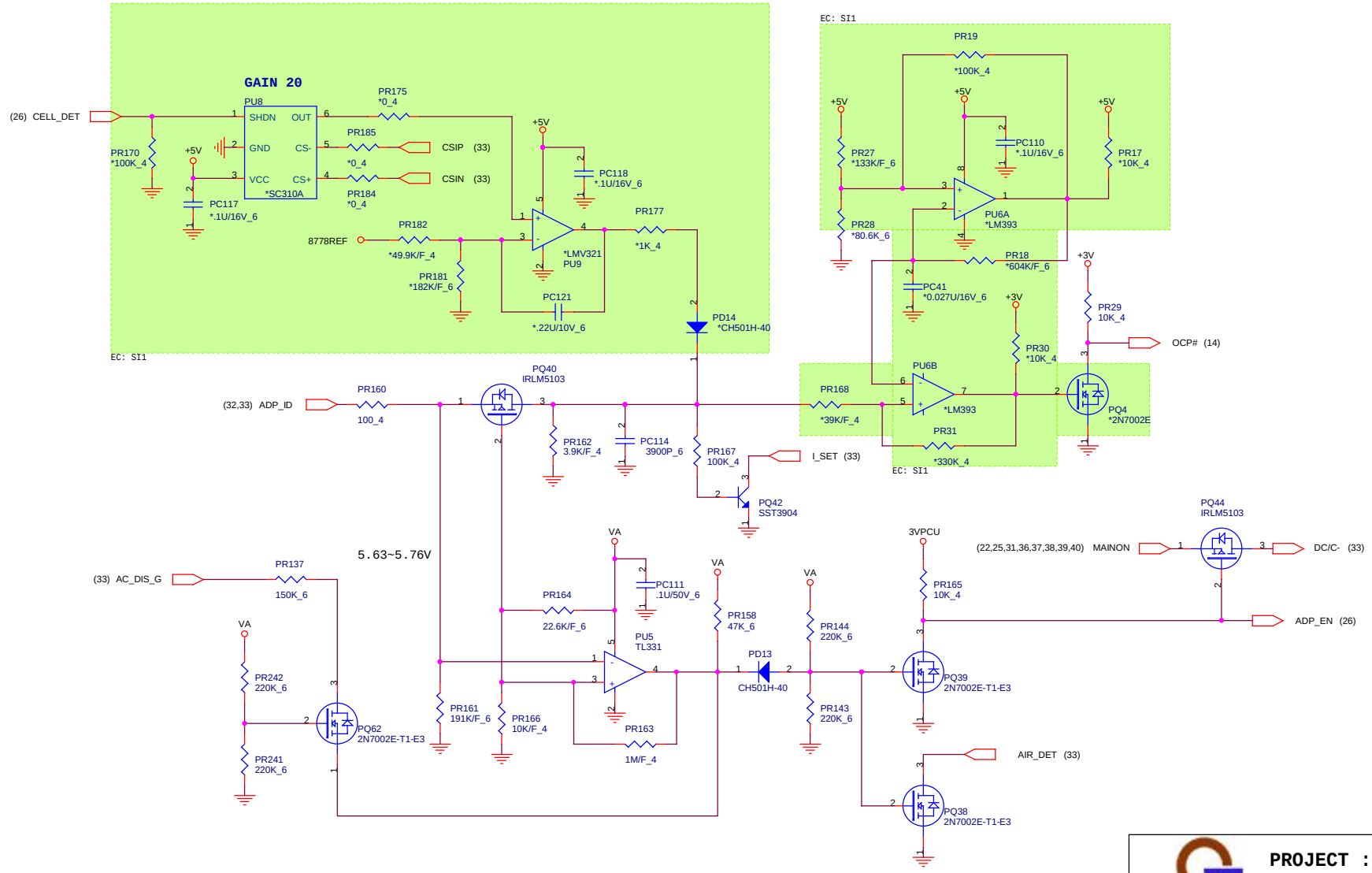


PROJECT : 0T2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	POWER SEQUENCE,BIOS	1A
Date: Thursday, March 22, 2007	Sheet 31 of 42	


DOCKING BOARD CONNECT
PV stage:for EMI request
VA
C673 .1U/50V_6
C674 .1U/50V_6
C675 .1U/50V_6
C676 .1U/50V_6
C677 .1U/50V_6
C678 .1U/50V_6
C360 0.1U
C361 0.1U
CN15
LAN
USB
TV
CRT
Line-out
Line-in
DB2 stage:modify due to no LAN S/W
XTX0P
XTX0N
XTX1P
XTX1N
XTX2P
XTX2N
XTX3P
XTX3N
5VSUS
+5V
USBP7+1
USBP7-1
TV_C/R
TV_Y/G
POWER_LED#
DOCK_CRT_B_1
DOCK_CRT_G_1
DOCK_CRT_R_1
DOCK_HP_OUT_L
DOCK_HP_OUT_R
AGND
LAN_LINKLED#
LOM_ACTLED#
ADP_ID
PWSWON#
PR_INSERT_DOCK#
DDCDAT2
DDCCLK2
PR_CRT_HSYNC
PR_CRT_VSYNC
LINE_IN_SENSE
DOCK_HP_SENSE
DOCK_LINE_IN_L
DOCK_LINE_IN_R
DOCK
Pin43 for Dock detect
(27) DOCK_CRT_B
(27) DOCK_CRT_G
(27) DOCK_CRT_R
L4 BK1608LL680
L5 BK1608LL680
L6 BK1608LL680
C60 *5.6P
C51 *5.6P
C38 *5.6P
C660 1000P
SI2 stage:add for EMI suggestion
3V_S5
R34 10K
C36 0.1U
PAD8 EMI spring
PAD2 EMIPAD-276X100
PAD3 EMIPAD-276X100
PAD7 EMI spring
PAD1 EMIPAD-276X100
PAD6 EMI spring
PAD5 EMI spring
PAD4 EMI spring
H22 h-c59d59n
H23 h-O91x59d91x59n
Area of Hole
H3 H-C313I160D110P2
H13 h-c197d47p2
H15 H-C315I160D110P2
H2 H-OT1-2-2P
H1 H-OT1-1-2P
H16 h-c157d47p2
H20 h-c157d47p2
H8 h-c313d118p2
H12 H-C313I160D110P2
H11 H-C313D110P2
H9 h-r313x165d118p2L
H19 H-C313D110P2
H18 h-c313d118p2
H17 h-c157d47p2
H21 h-c157d47p2
H10 h-c197d47p2
H7 h-c313d118p2
H6 H-C313D110P2
H5 H-C313D110P2
H14 h-c313d118p2
H4 H-C313D110P2
SI stage:for modem cble and mic cable
+1.05V
1.8VSUS
+5V
+1.5V
VA
VIN
EC4 470P
EC11 *0.1U
EC12 *0.1U
EC2 *0.1U
EC8 *0.1U
EC16 *0.1U
EC17 *0.1U
EC5 *0.1U
EC6 *0.1U
EC1 *0.1U
EC10 *0.1U
EC14 *0.1U
EC13 *0.1U
+3V
5VSUS
+1.5V
3VPCU
FOR EMI
PROJECT : 0T2
Quanta Computer Inc.
Size B
Document Number DOCKING
Rev 1A
Date: Thursday, March 22, 2007
Sheet 32 of 42

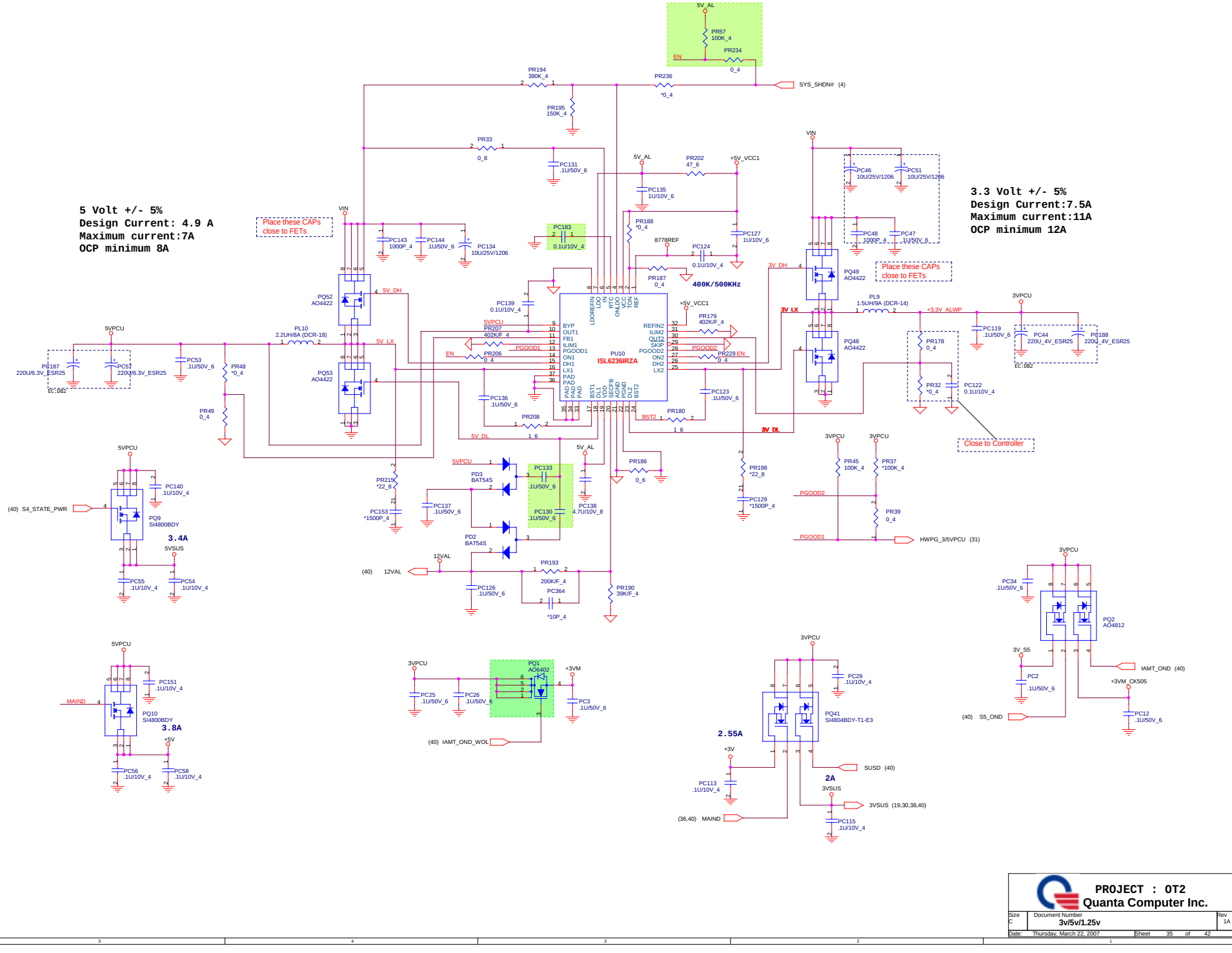

Normal:19.5 Volts
Airline:15.0 Volts
AC power from docking or system AC jack.Will not present at the same time.
ADAPTER 65W 19.5 Volts 3.33A
ADAPTER 90W 19.5 Volts 4.61A
If AC voltage lower then 16.3V will disable charger/charge LED/OS charge icon.
Float= 3 CELLS
REFIN=4CELLS
When system with AC and DC can support DC discharge for Battery learning.
Change PR196 from 30.1K change to 16.5K
Present AC:
When AC voltage level > 12.3 Volts.
DEL PR211-0ohm
CLS connect to REF
For Full-scale 75mV
Change PR110 from 10K to 100K
Remove
PR113,PR130,PC105,PC24,PR131,PR132,PQ25,PQ26
MAX8765
PROJECT : 0T2
Quanta Computer Inc.
CHARGE(MAX1908/8724)
Thursday, March 22, 2007

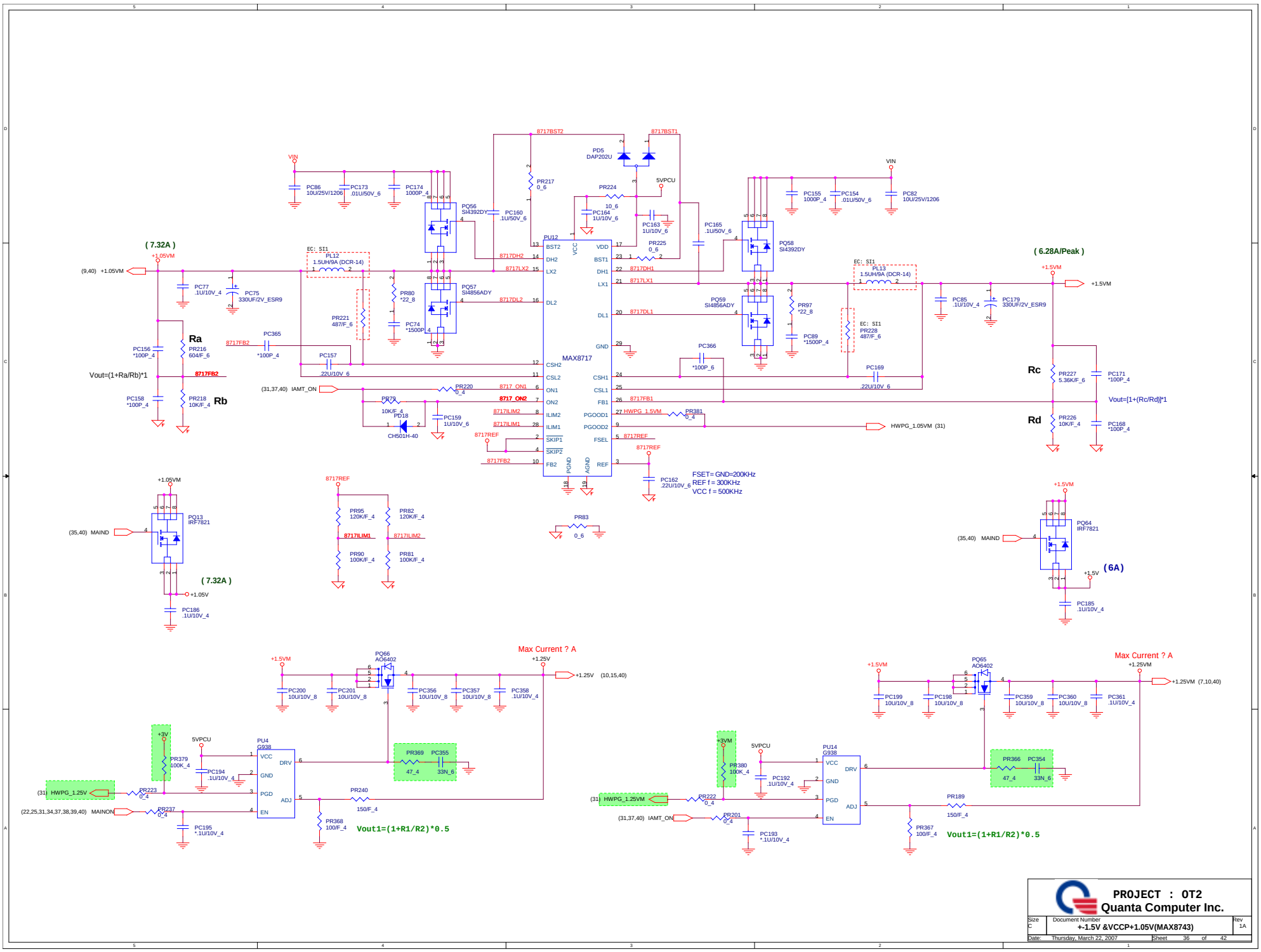


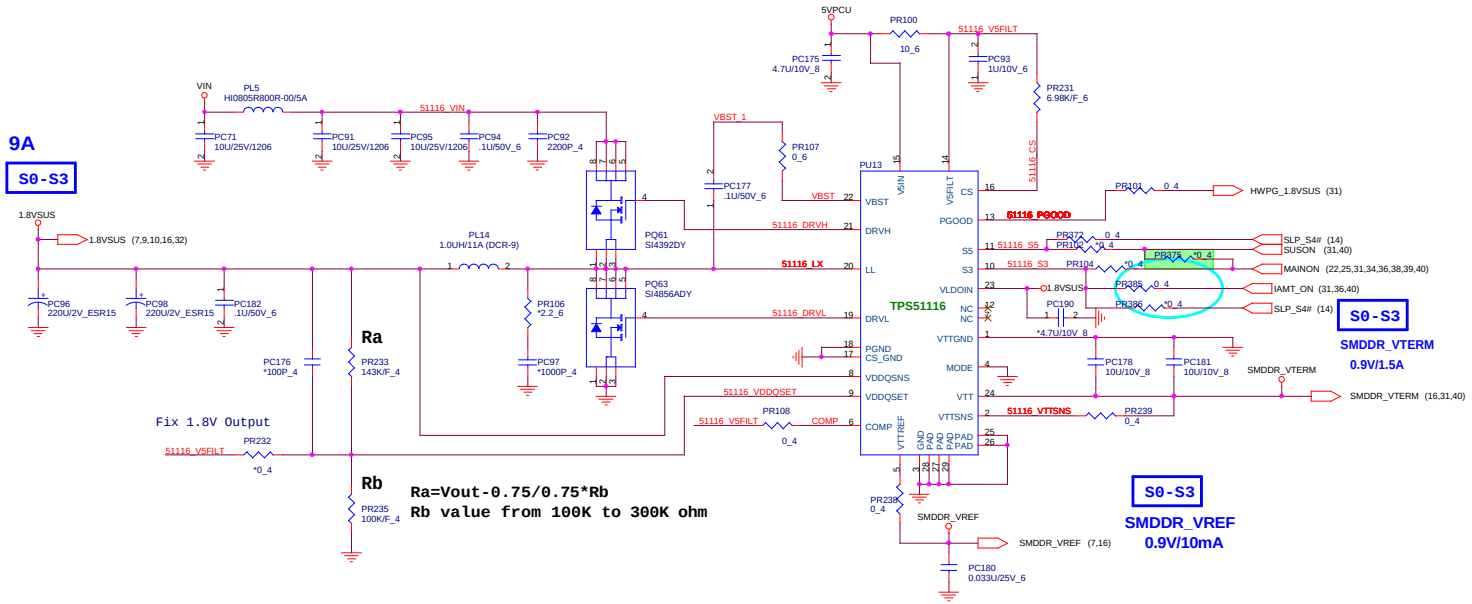
PROJECT : 0T2
Quanta Computer Inc.

Size	Document Number	Rev
B	CHARGER II	1A

Date: Thursday, March 22, 2007 Sheet 34 of 42


5 Volt +/- 5%
Design Current: 4.9 A
Maximum current:7A
OCP minimum 8A
3.3 Volt +/- 5%
Design Current:7.5A
Maximum current:11A
OCP minimum 12A
Place these CAPS close to FETs
Place these CAPs close to FETs
Close to Controller
400K/500KHz
ISL6236IRZA
3.4A
3.8A
2.55A
2A
PROJECT : 0T2
Quanta Computer Inc.
3v/5v/1.25v
Thursday, March 22, 2007


(7.32A)
(6.28A/Peak)
MAX8717
Ra
Rb
Rc
Rd
Vout=(1+Ra/Rb)*1
Vout=(1+Rc/Rd)*1
FSET= GND=200KHz
REF f = 300KHz
VCC f = 500KHz
(7.32A)
(6A)
Max Current ? A
Max Current ? A
Vout1=(1+R1/R2)*0.5
Vout1=(1+R1/R2)*0.5
PROJECT : 0T2
Quanta Computer Inc.
+-1.5V &VCCP+1.05V(MAX8743)
Thursday, March 22, 2007



V_TRIP(mV)=R_TRIP(Kohm)*10(uA)

I_OCP=V_trip/Rds_on+I_Ripple/2

VDDQSET	VDDQ(V)	VTTREF and Vtt	Note
GND	2.5	V_ vddqsns/2	DDR
V5IN	1.8	V _vddqsns/2	DDR2
FB	Adjustable	V_VDDQSNS/2	1.5V<VDDQ<3V

Mode	Discharge Mode
V5IN	No discharge
VDDQ	Tracking discharge
Gnd	Non-tracking discharge

PROJECT : 0T2
Quanta Computer Inc.

Size	Document Number	Rev
C	ti51116(1.8VSUS/DDR_VTERM)	1A

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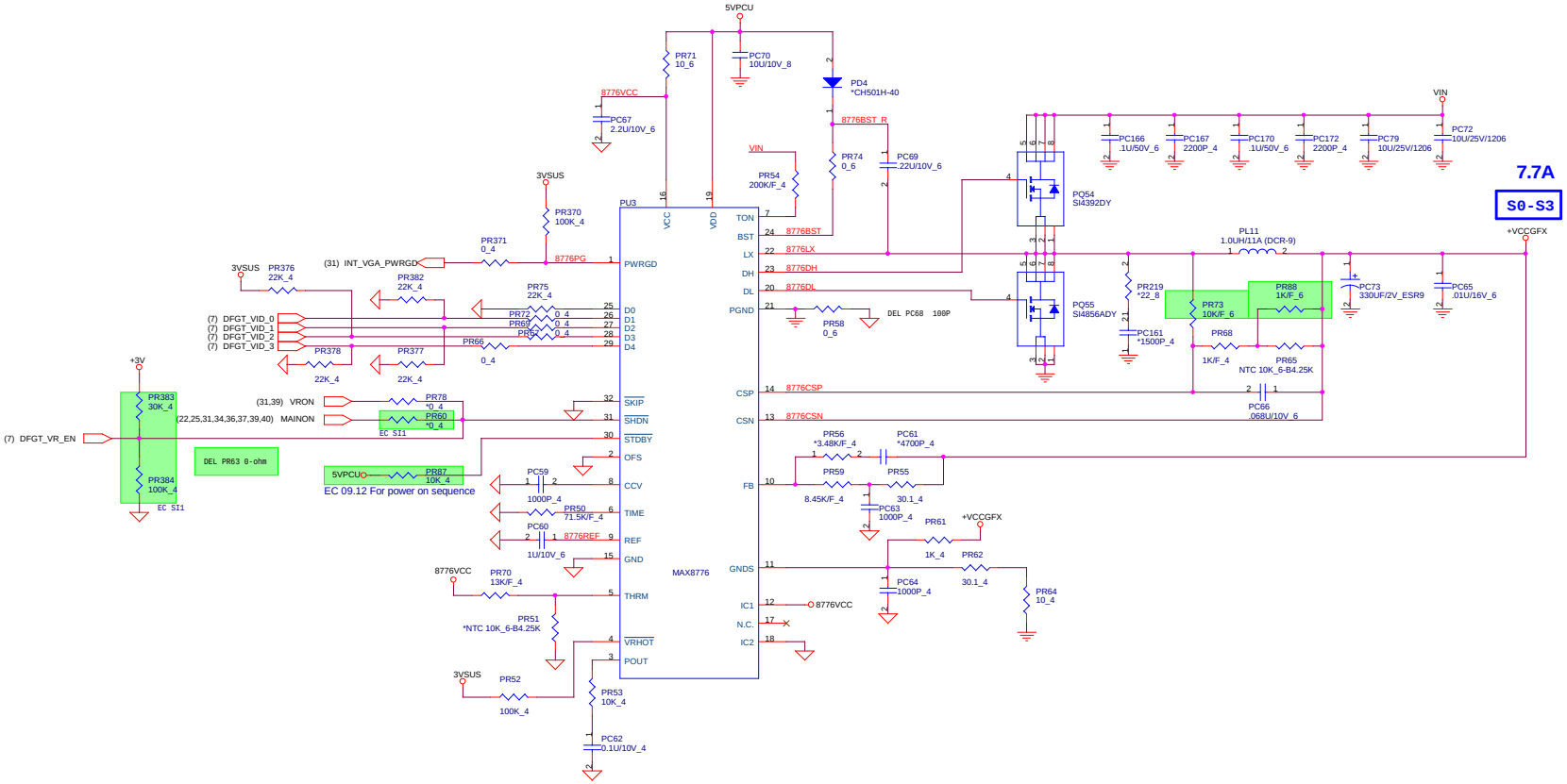
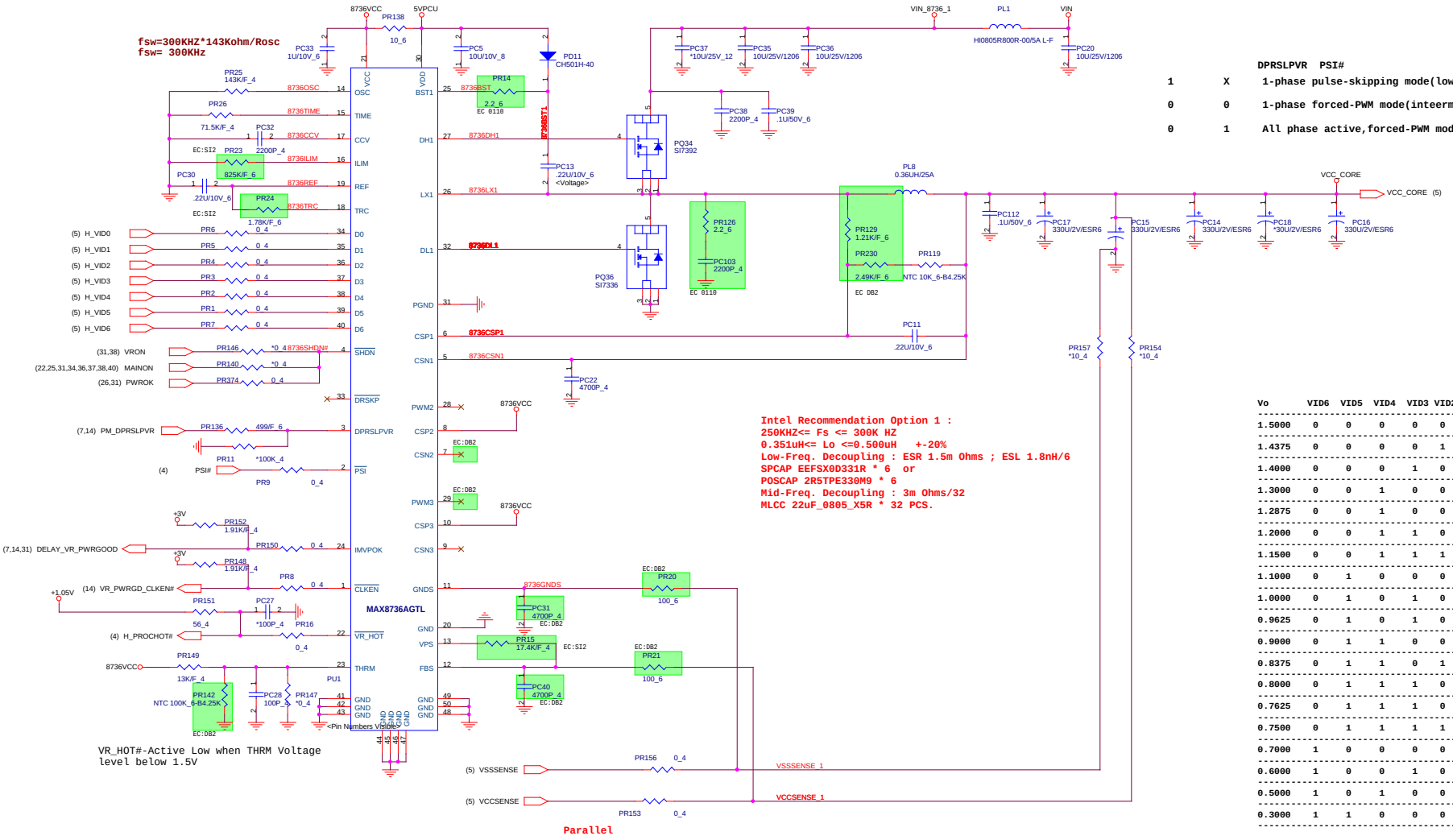


PROJECT : 0T2		
Quanta Computer Inc.		
Size: C	Document Number: GMCH (MAX8776)	Rev: 1A
Date: Thursday, March 22, 2007	Sheet 38 of 42	

DPRSLPVR	DPRSTP#	PSI#	State	CPU Current
1	0	0	Deeper Sleep	< 3A
1	0	1	Deeper Sleep	> 3A
0	1	0	Active Mode	< 18A
0	1	1	Active Mode	> 15A

RVPS = RDROOP / (RSENSE x GM) = 5.1mV/A / (0.001 x 200uS) =25.5K
RTRC = RSENSE x 5k / (RDROOP(AC) x # of Phases) = 0.001 x 5k / ((5.1mV/A x 80%) x 1phases) =1.24K
RILIMPK = Battery V x RTRC / (IPK x RSENSE) = 8V x 1.24K / (Ioutput peak x 0.001) OCP=17.7A
fsw=300kHZ*143kohm/Rosc
dV_Target/dt=12.5mV/us*71.5kohm/R_TIME

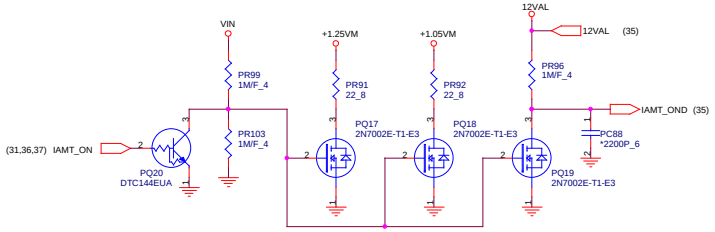


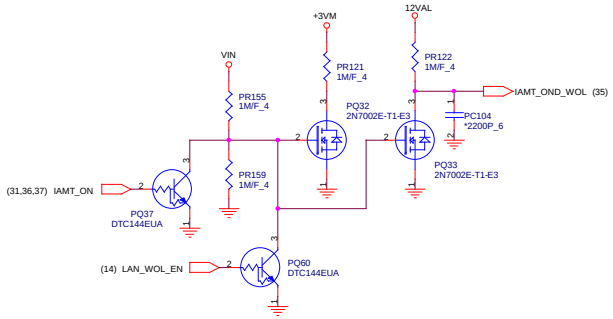
Vo	VID6	VID5	VID4	VID3	VID2	VID1	VID0
1.5000	0	0	0	0	0	0	0
1.4375	0	0	0	0	1	0	1
1.4000	0	0	0	1	0	0	0
1.3000	0	0	1	0	0	0	0
1.2875	0	0	1	0	0	0	1
1.2000	0	0	1	1	0	0	0
1.1500	0	0	1	1	1	0	0
1.1000	0	1	0	0	0	0	0
1.0000	0	1	0	1	0	0	0
0.9625	0	1	0	1	0	1	1
0.9000	0	1	1	0	0	0	0
0.8375	0	1	1	0	1	0	1
0.8000	0	1	1	1	0	0	0
0.7625	0	1	1	1	0	1	1
0.7500	0	1	1	1	1	0	0
0.7000	1	0	0	0	0	0	0
0.6000	1	0	0	1	0	0	0
0.5000	1	0	1	0	0	0	0
0.3000	1	1	0	0	0	0	0

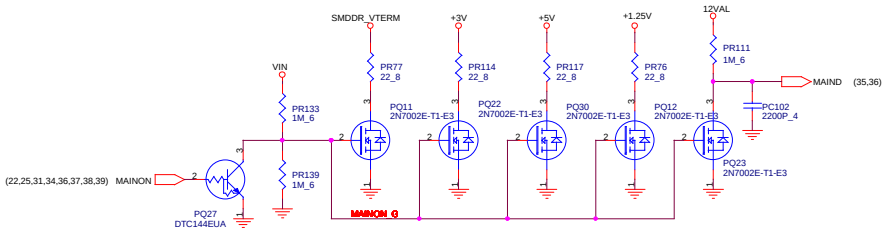
PROJECT : 0T2
Quanta Computer Inc.

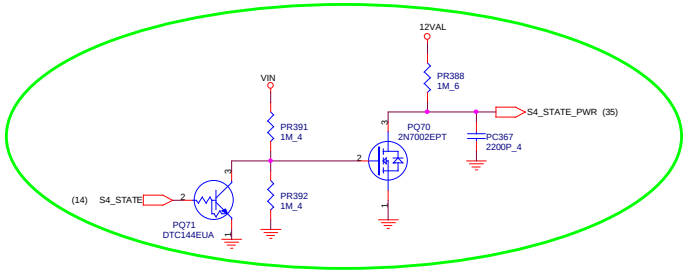
Size	Document Number	Rev
C	MAX8736	1A

Date: Thursday, March 22, 2007 Sheet 39 of 42

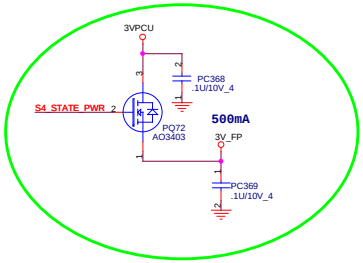




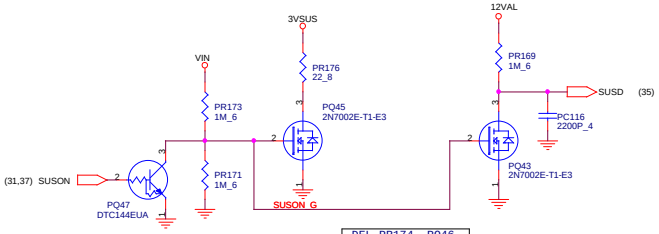




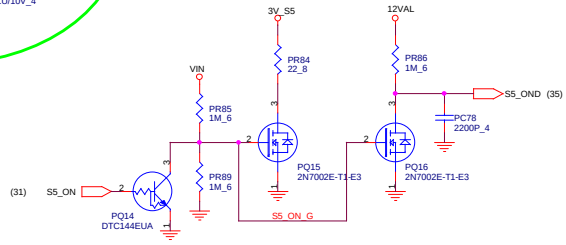
PV stager:add for HP request



PV stager:add for HP request



DEL PR174, PQ46
For S4-STATE



PROJECT : 0T2
Quanta Computer Inc.

Size	Document Number	Rev
C	DISCHARGE	1A
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MODEL

OT2 MB
31OT2MBXXXX

CHANGE LIST

DB2 --->SI

Date	Reason for change	Page	modify list
2006.11	change from 5VSUS to +5v due to not support wake up from suspend		change U35 pin13,15 to +5V
	change footprint to 0805 to easy prepare material		change U2, C577 footprint
	avoild leakage cruuent		change power plan from 3VSUS to 3V_S5 at RP31 , R241 , R448 , R538,change card bus switch poewr from 5VSUS to 5V R452 Install, R46 on instal;delete R496,Add D32 Add D33,D34 ;delete R293 ,and add Q60
	EC VCC2 pin is used in a comparator to sample when Vcc2 is going up or down. It will draw some current. Approx 300ua		R1005 install,R297 no install
	For auto boot issue		reserve R1029,add R1028 ,Q62 for auto power issue
	remove Kill switch function		remove Q37,R443,R426,CN1,R977
	add for EA team easy test		add R1031,R1032
	for internal mic issue		add C643, and modify pin 1 for U47 OP circuit and add C657
	modify footprint firm right angle tyoe to straight type		CN36
	change footprint for another vender for easy insert		change footprint for track point connector CN8
	move D31 close to ICH8 to solve battery LED issue ,else it will cause LED function abnormally		D31 close to ICH8 and pull up 10k(R1035) to +3V
	WWAN noise --- ICH improvement		reserve L53, L54,add R1033,R1034
	due to use 4MB flash part		delete CN24
	add strapping options for CPU_BSEL{0:2} so we can hardwire the clock to the FSB frequency if needed		R1036-R1044
	PU13.11, add IAMT_ON control signal option with 0-Ohm NO INSTALL to control power up of 0.9V This is to save system power in S3 when iAMT is disabled.		add PR385
	For ENERGY_DET, Change R18 to 1.4K, this is a change from Intel on LAN Energy Detect.		R18
DB2 --->SI2			
Date	schematic error and change to avoid leakage voltage		RP31 pin10 from 3V_S5 to 3VSUS
2007.1	change Lan crystal layout for intel suggestion		Lan crystal layout
	to avoid the ripple for signal CLK_PWRGD		add R1049 for intel suggestion
	tune Adp_Id signal for layout. to avoid overlay		for EMI suggestion
	for EMI suggestion		reseve C661,C662,C663
	for EMI suggestion(CRT)		L8,L10,L14 change to BK1608LL680
	for EMI suggestion(internal Mic)		reserve R664, R1050 for Mic
	for EMI suggestion(modem)		delete R280,R281 due to useless
	PWM signal(LCD)to avoid work abnormally		C5 no install
	change to 1.87K for Intel suggestion		change R18 to 1.87k
	Q61,D32 is for leakage voltage issue ,but will influence LAN function ,change to 0 ohm		delete Q61,add R1051;deleteD32,Add R1052

PROJECT : OT2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	change list-1	1A

Date: Thursday, March 22, 2007 Sheet 41 of 42

MODEL

DB2 --->SI2

OT2 MB
31OT2MBXXXX

CHANGE LIST

Date	Reason for change	Page	modify list
2007.1	For LCD rush current issue		change R30 to 82K,C32 to 0.1u ,and change R20 power source to 3VPCU
	due to no use		delete R341,R1025,L9,L13,L15,L8,L10,L14,R342,R95,R81
SI2--->PV 2007.1			

PROJECT : OT2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	change list-2	1A

Date: Thursday, March 22, 2007 Sheet 42 of 42