

Compal Confidential

ULC AMD M/B LA-A996P DIS Schematics Document

AMD APU Beema/Kabini FT3 + ATI SUN LE + DDR3

Project Code : ZSO51

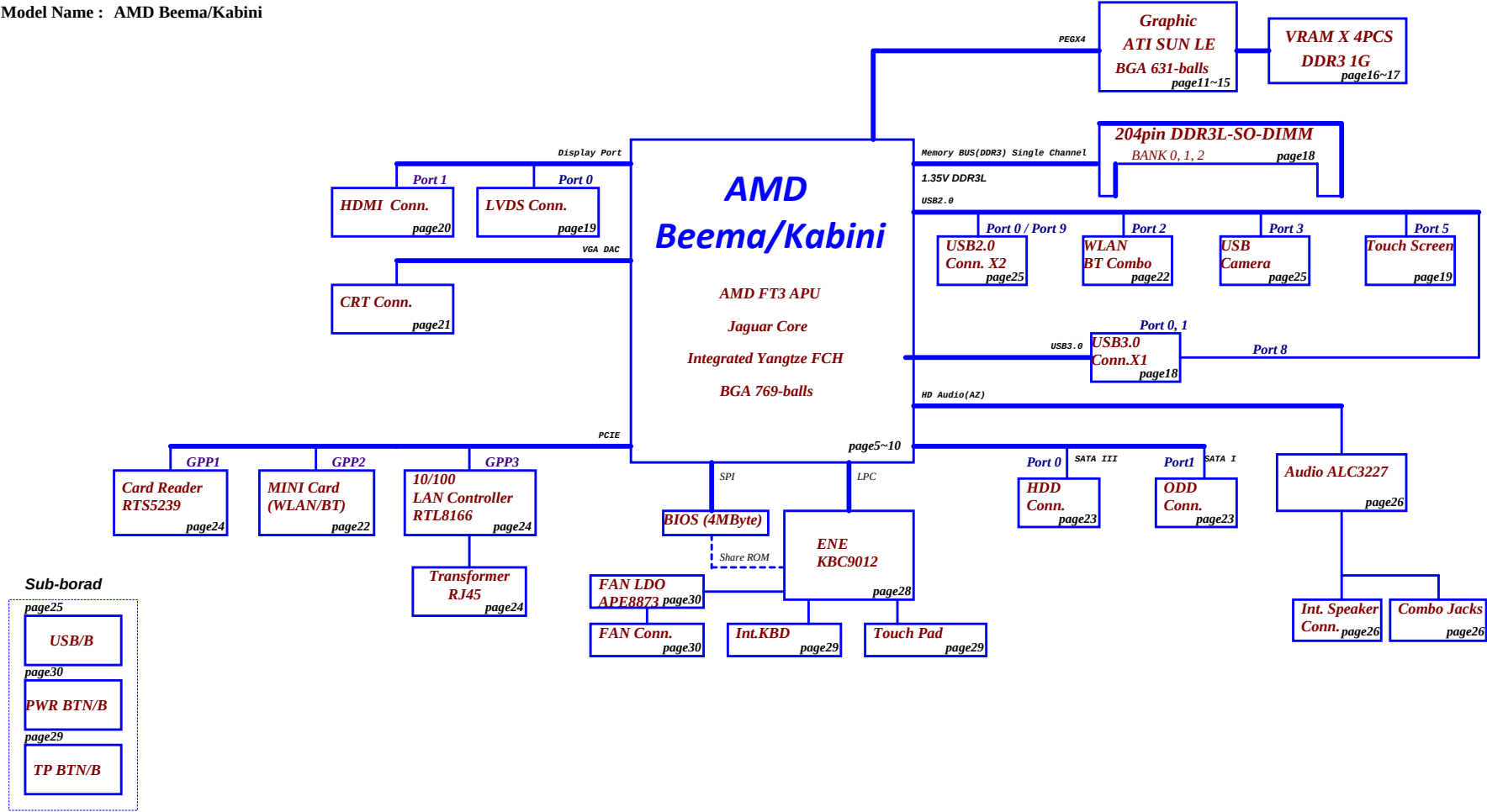
2014/02/08

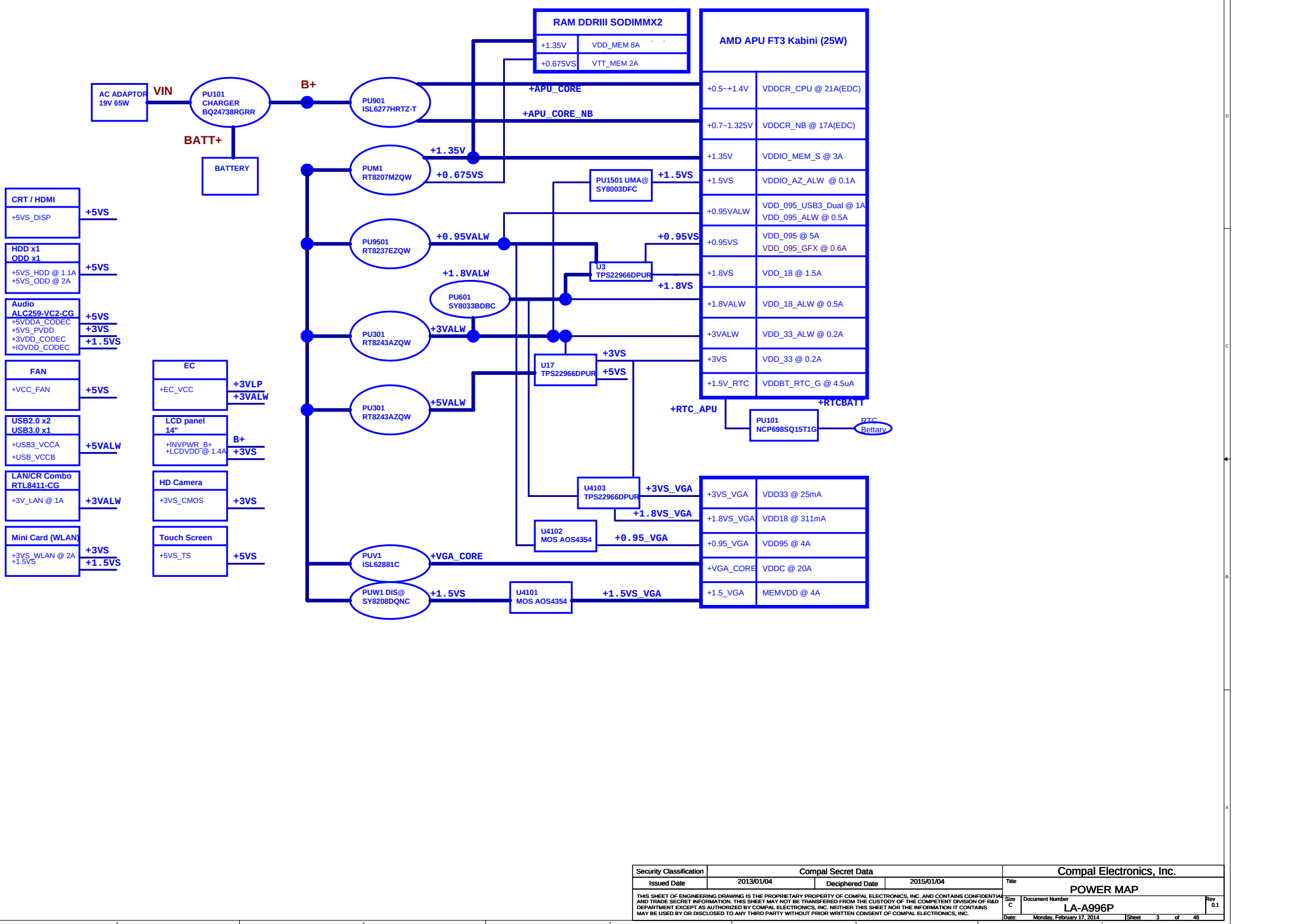
PV Rev. 4.0

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Model Name : AMD Beema/Kabini





Voltage Rails

Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+0.95VALW	0.95V always on power rail	ON	OFF	OFF
+0.95VS	0.95V switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON*
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for APU and DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+RTC_APU	RTC power			

STATE	SIGNAL		SLP_S#3	SLP_S#5	+VALW	+V	+VS	Clock
Full ON			HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)			HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)			HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)			LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)			LOW	LOW	ON	OFF	OFF	OFF



UAPU1 BA4@
A4-6300
Part Number = SA00007QP20
S IC A32 A4-6300 AM6300ITJ44JB



UAPU1 BE2@
E2-6200
Part Number = SA00007OQ20
S IC A32 E2-6200 EM6200ITJ44JB 1.5G BGA



UAPU1 BE1@
E1-6050
Part Number = SA00007IQ50
S IC A32 E1-6050 ZM1332M2J2370 1.35G BGA



UAPU1 R36410@
A8-6410 15W
Part Number = SA00007TQ20
AM6410ITJ44JB



UAPU1 R36210@
A4-6210 R3 15W
Part Number = SA00007RA60
AM6210ITJ44JB



UAPU1 R36110@
E2-6110 R2 15W
Part Number = SA00007RB60
EM6110ITJ44JB



UAPU1 R36010@
E1-6010 R2 10
Part Number = SA00007RC60
EM6010IUJ23JB



UAPU1 R16410@
A8-6410 15W
Part Number = SA00007TQ10
AM6410ITJ44JB



UAPU1 R16210@
A4-6210 R1 15W
Part Number = SA00007RA40
AM6210ITJ44JB



UAPU1 R16110@
E2-6110 R2 15W
Part Number = SA00007RB40
EM6110ITJ44JB



UAPU1 R16010@
E1-6010 R2 10
Part Number = SA00007RC40
EM6010IUJ23JB



DAX
PCB
Part Number = DAZ14D00203
PCB LA-A996P REV4.0 M/B



UAPU1 E1R1@
E1-2100
Part Number = SA00006QX10
S IC A32 KABINI EM2100ICJ23HM 1G BGA769P



UAPU1 A4R1@
A4-5000
Part Number = SA00006R410
S IC A4 SERIES AT1250IDJ23HM 1G BGA 769P



UAPU1 E2R1@
E2-3800
Part Number = SA00007BX20
S IC A32 KABINI EM2100ICJ23HM 1G BGA769P



UAPU1 A6R1@
A6-5200
Part Number = SA00006R350
S IC KABINI AM5200IAJ44HM 2G BGA769P APU



ZZZ H@
HDMI
Part Number = RO0000003HM
PCB 102 LA-A996P REV0 M/B 2



UAPU1 E1R3@
E1-2100
Part Number = SA00006QX60
S IC A32 KABINI EM2100ICJ23HM 1G BGA769P



UAPU1 A4R3@
A4-5000
Part Number = SA00006R460
S IC A4 SERIES AT1250IDJ23HM 1G BGA 769P



UAPU1 E2R3@
E2-3800
Part Number = SA00007BX60
S IC A32 KABINI EM2100ICJ23HM 1G BGA769P

SMBus List

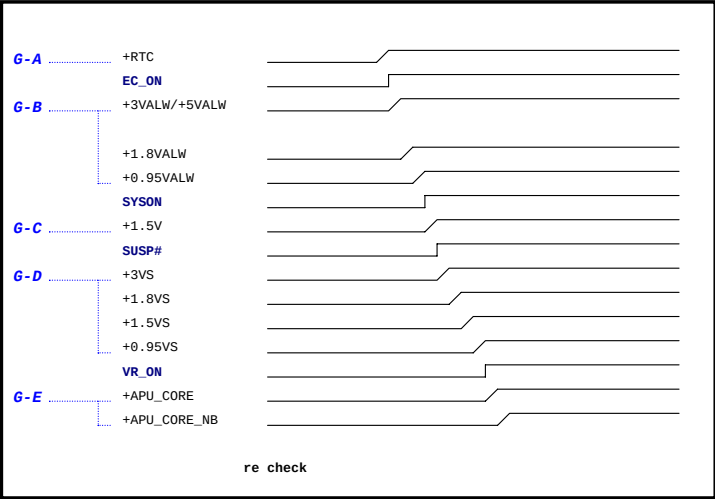
EC SMBus Port1 (+3VALW)			EC SMBus Port2 (+3VS)		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	SB-TSI (APU)	1001 100X b	98H

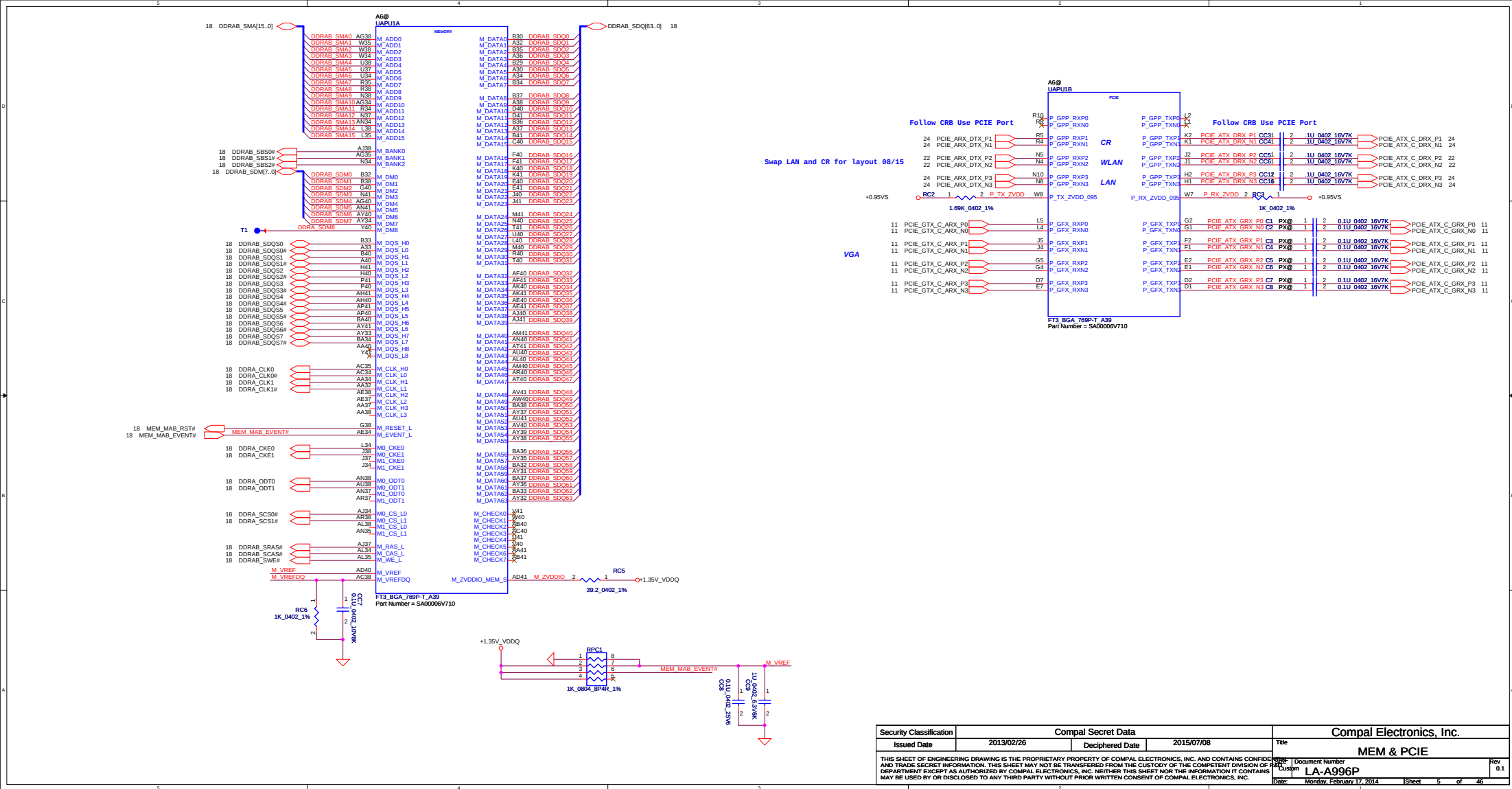
APU SMBus Port0 (+3VS)			APU SMBus Port1(+3VALW)		
Device	Address	HEX	Device	Address	HEX
DDR DIMM2	1010 000Xb	A0H			
DDR DIMM1	1010 001Xb	A2H			
Mini Card (DNI)					

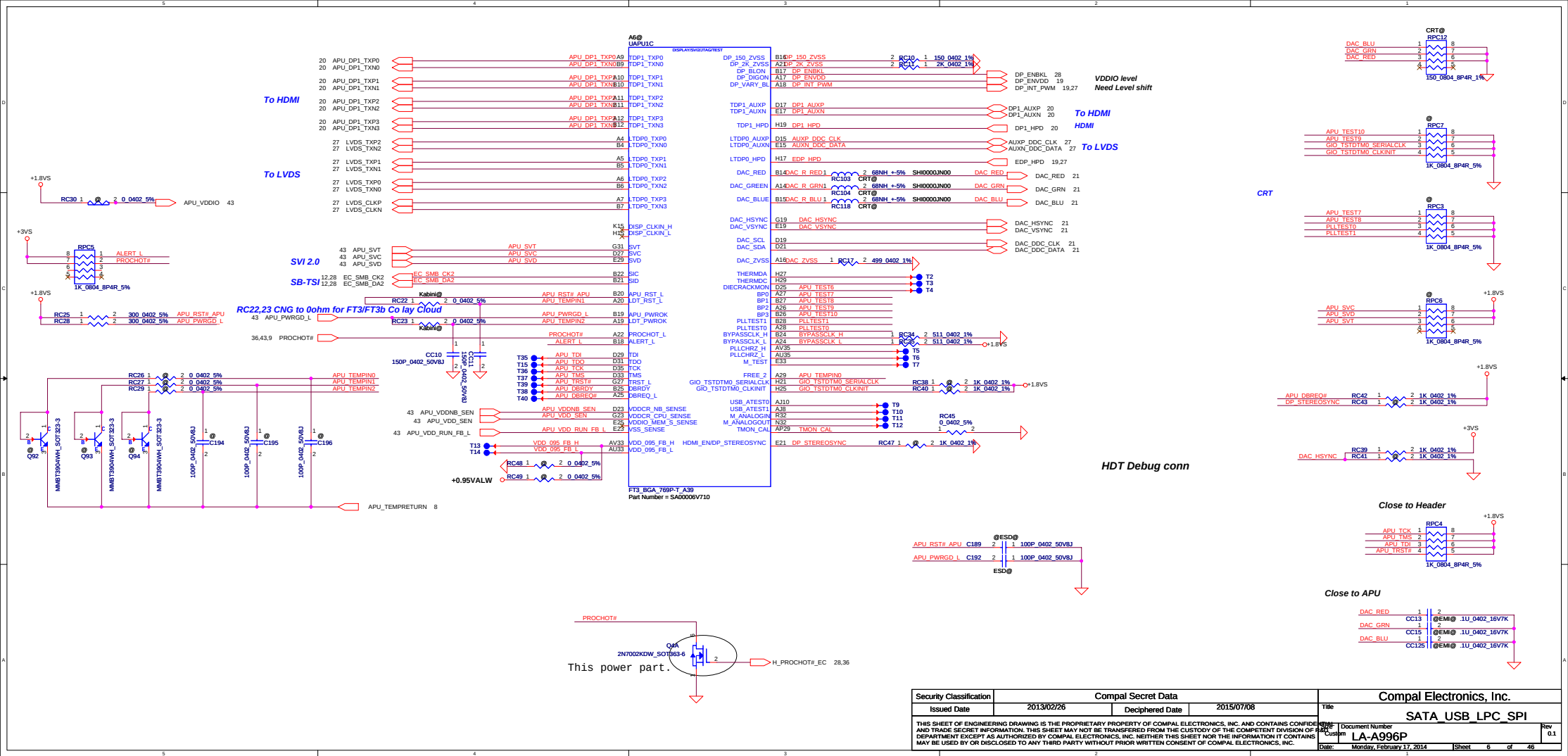
BOM Structure Table

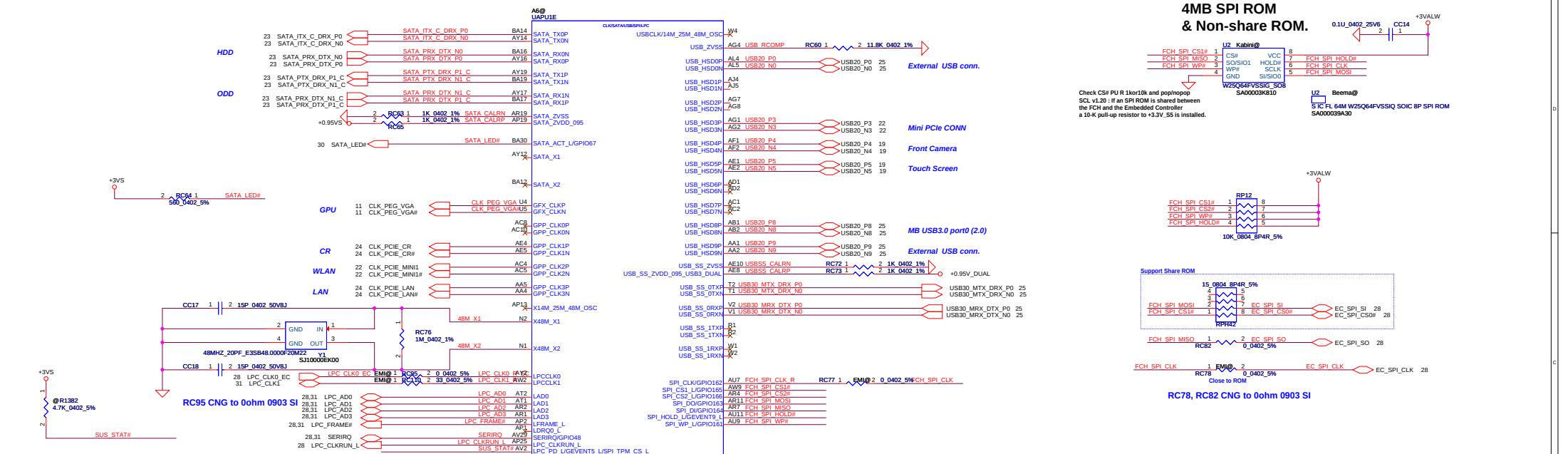
BOM Structure	BTO Item
@	Unpop
CONN@	Connector Part Control by ME
EMI@	EMI pop component
@EMI@	EMI unpop component
ESD@	ESD pop component
@ESD@	ESD Unpop component
PX@	GPU SUN LE Componet
8166@	10/100 LAN
8151@	Giga LAN
UMA@	UMA Componet
display@	display Componet
EDP@	EDP Componet
KLVDS@	Kabini LVDS Componet
BLVDS@	Beema LVDS Componet
Kabini@	Kabini Componet
Beema@	Beema Componet
LVDS@	LVDS Componet

APU POWER SEQUENCE



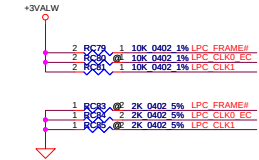






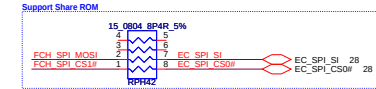
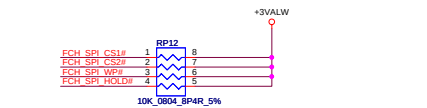
STRAPS OF APU

	LPC_FRAME#	LPC_CLK0_EC	LPC_CLK1	GEVENT2_L	RTC_CLK
H	SPI ROM (DEFAULT)	BOOT FAIL TIMER ENABLED	CLKGEN ENABLE (DEFAULT)	1.8V SPI ROM	NORMAL POWR UP/RESET TIMING (DEFAULT)
L	LPC ROM	BOOT FAIL TIMER DISABLED (DEFAULT)	CLKGEN DISABLED	3.3V SPI ROM (DEFAULT)	FAST POWER UP/RESET TIMING FOR SIMULATION



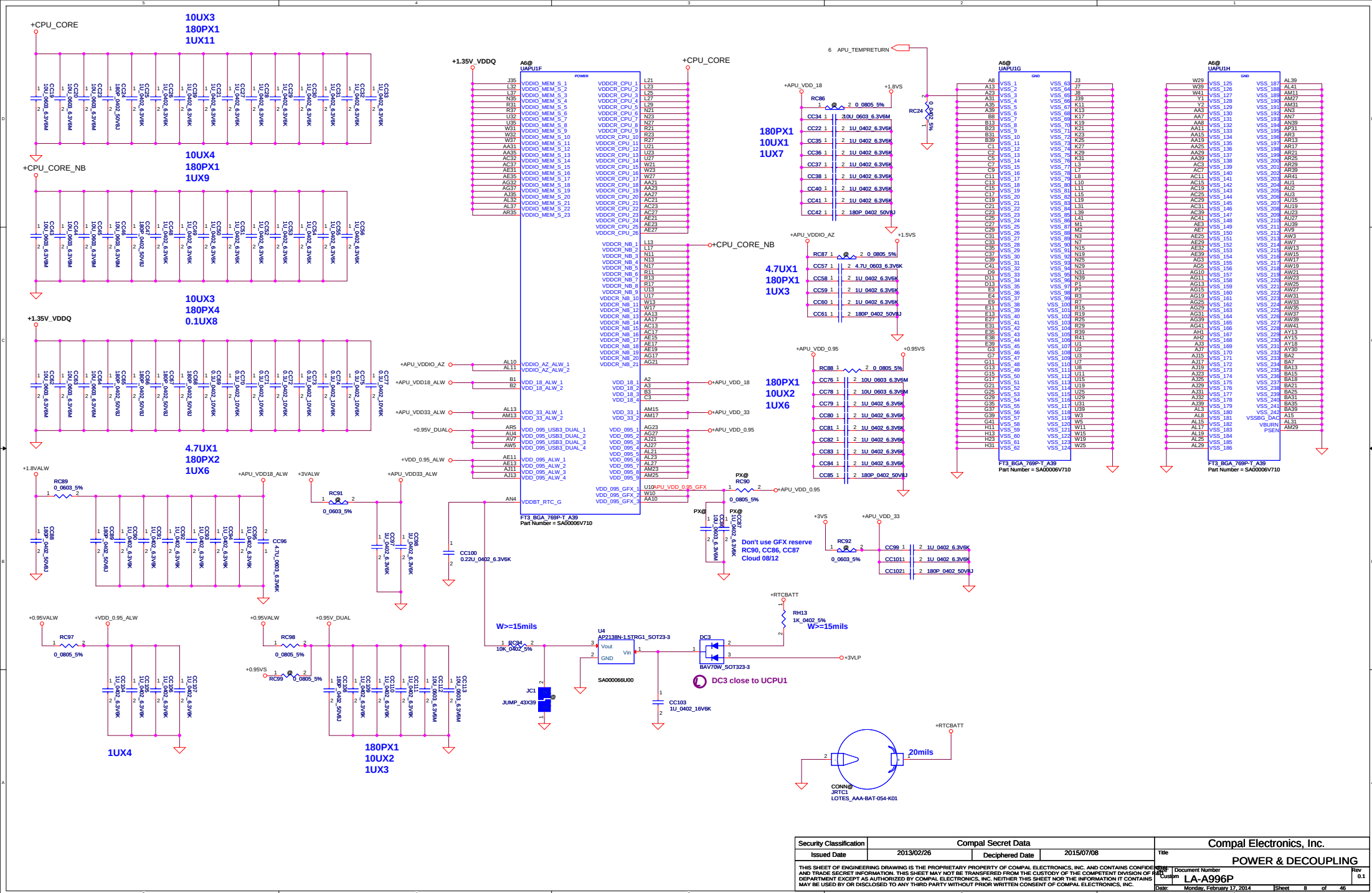
4MB SPI ROM & Non-share ROM.

Check CS# PU R 1k or 10k and popin popout SCL v1.20. If an SPI ROM is shared between the FCH and the Embedded Controller a 10-K pull-up resistor to +3.3V_SS is installed.

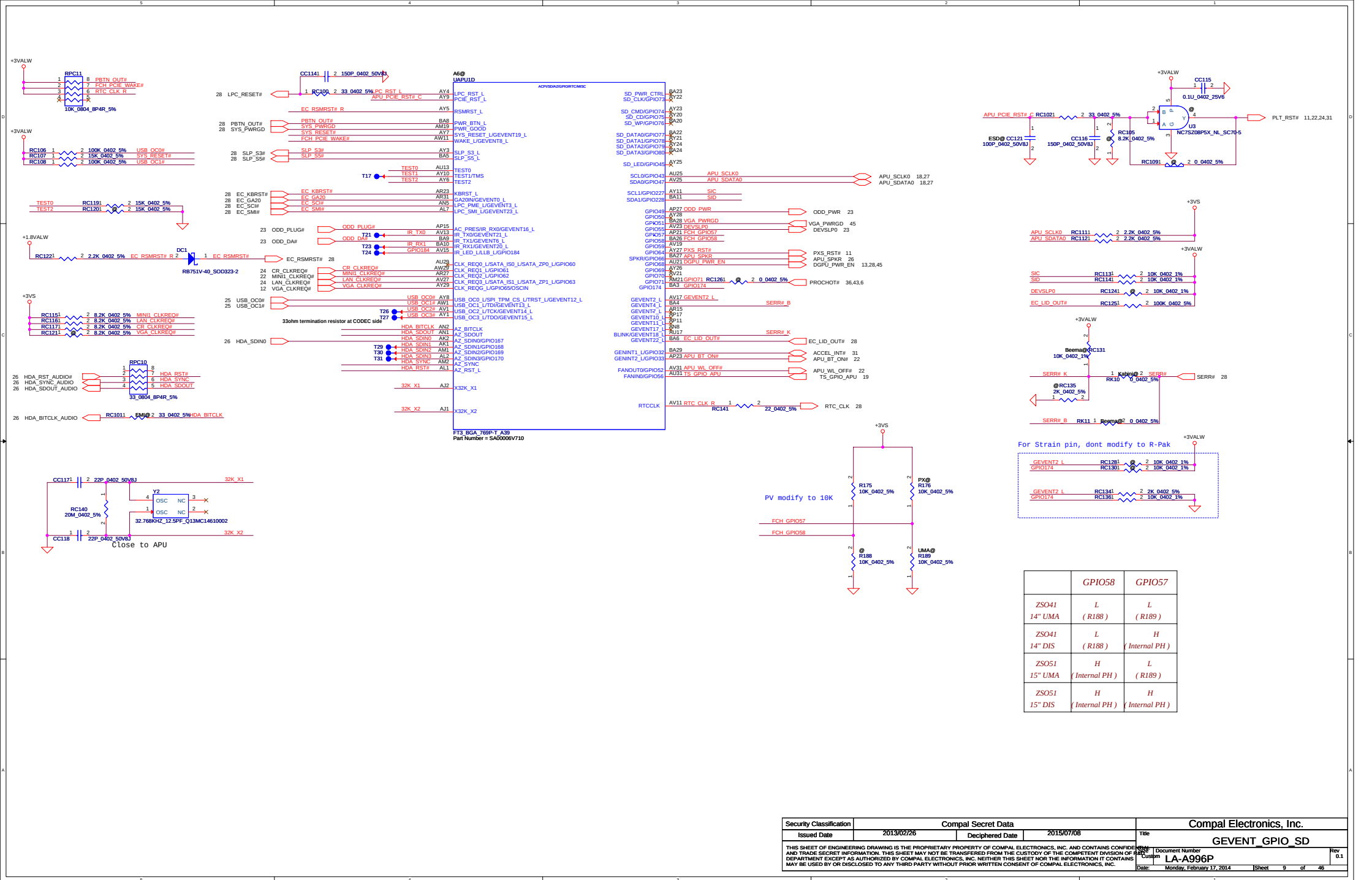


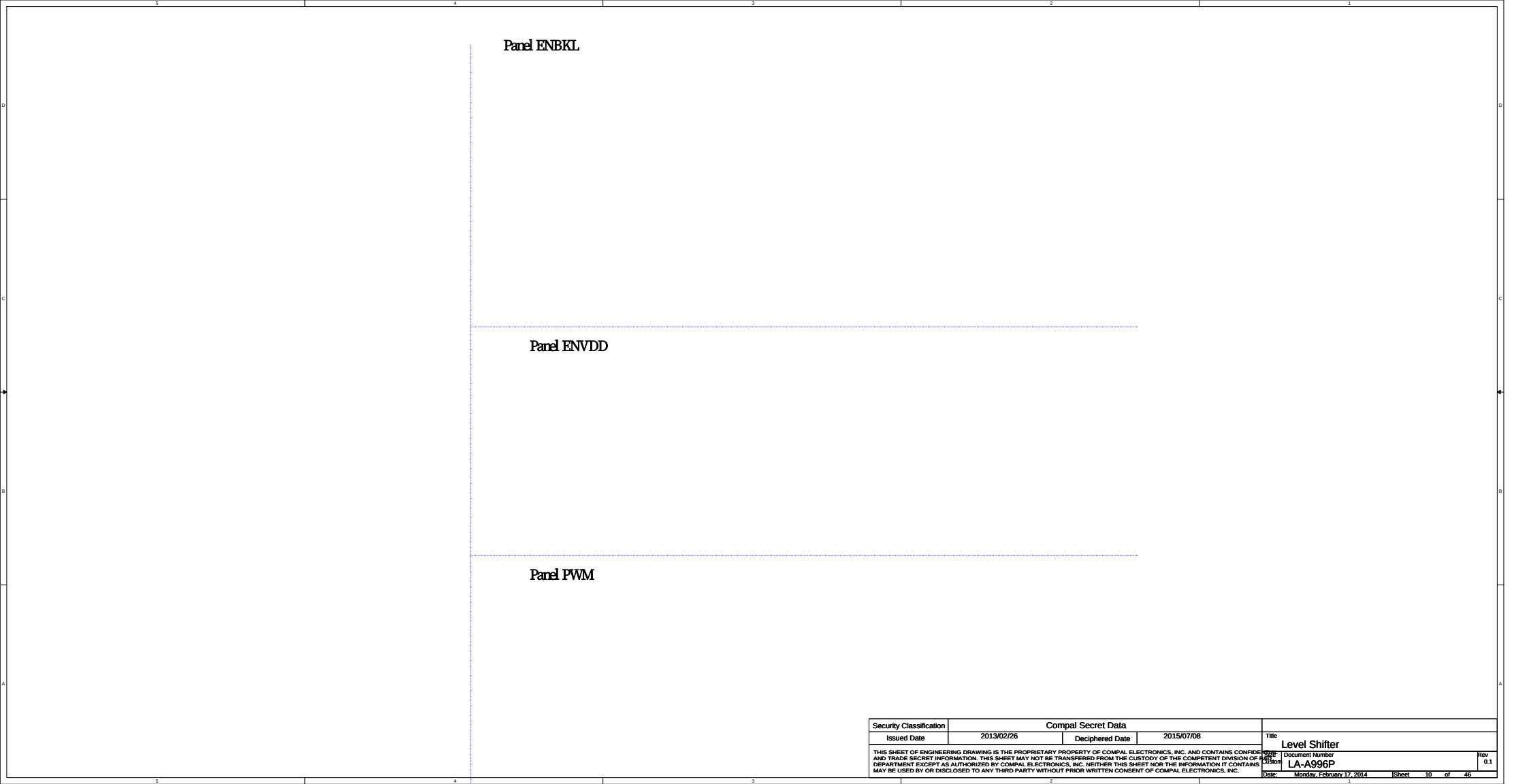
RC78, RC82 CNG to 0ohm 0903 SI

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				Drawing Number LA-A996P	
				Date Monday, February 17, 2014	
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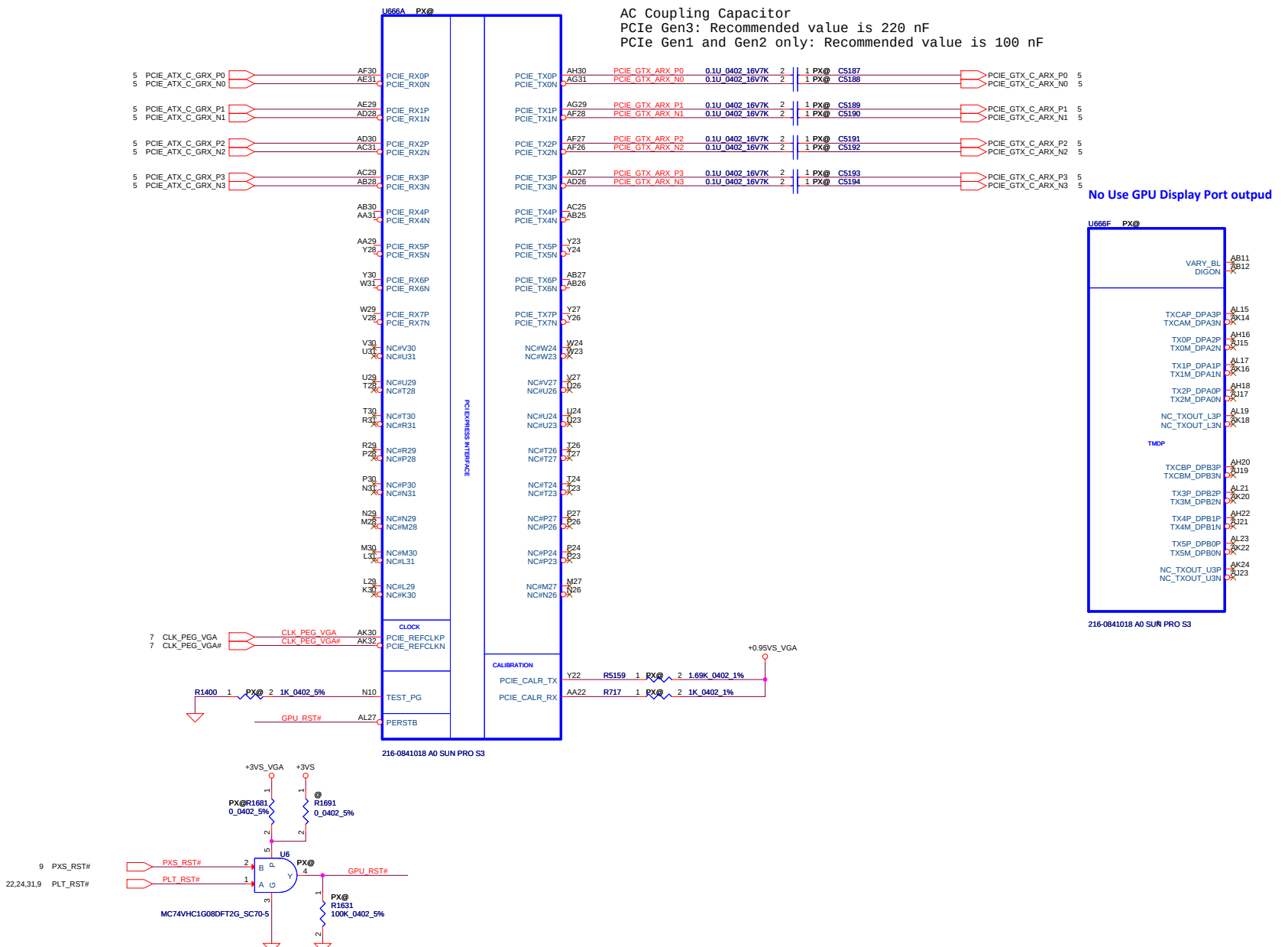


Panel ENBKL

Panel ENVDD

Panel PWM

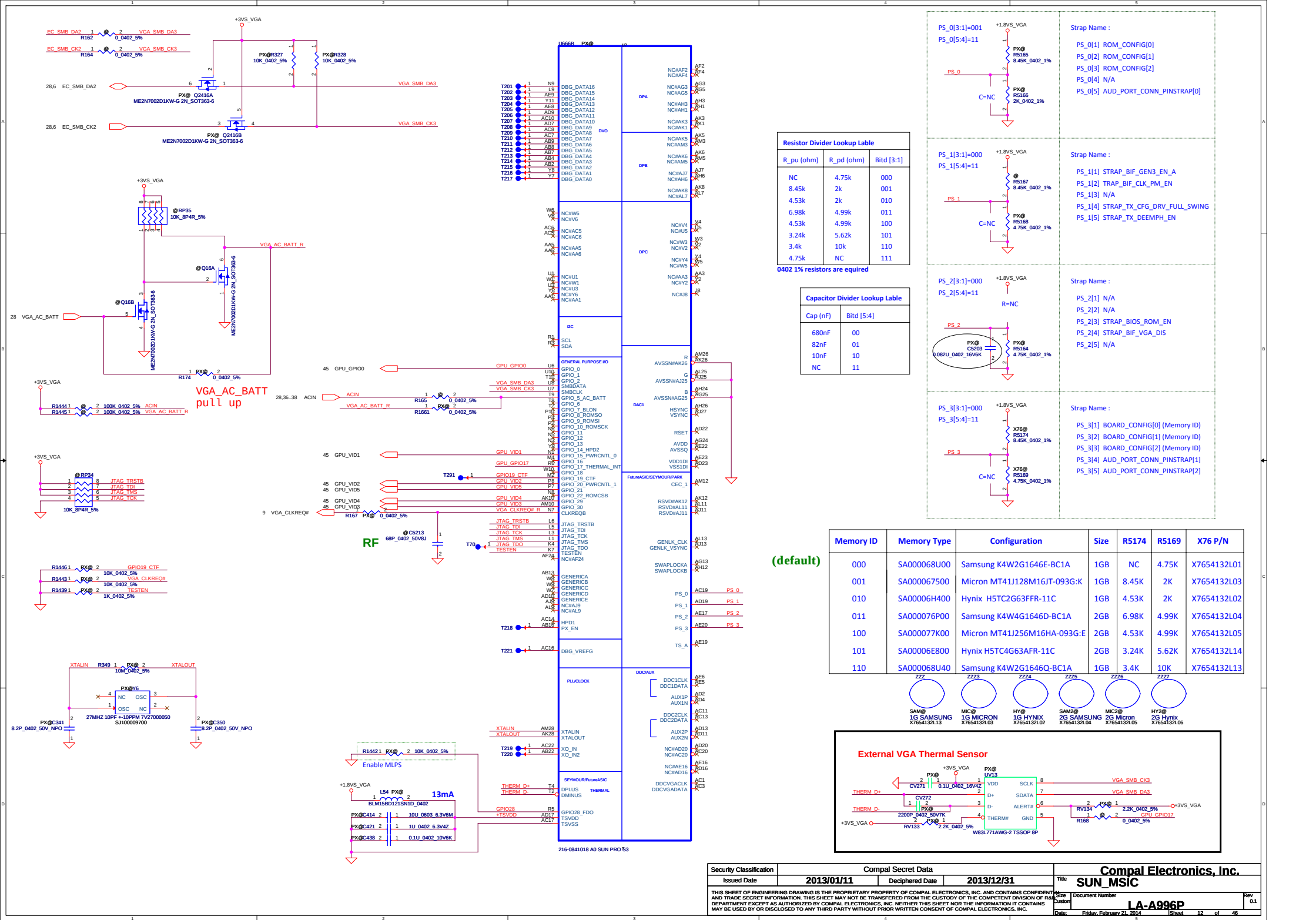
Security Classification	Compal Secret Data			Title	
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Level Shifter	
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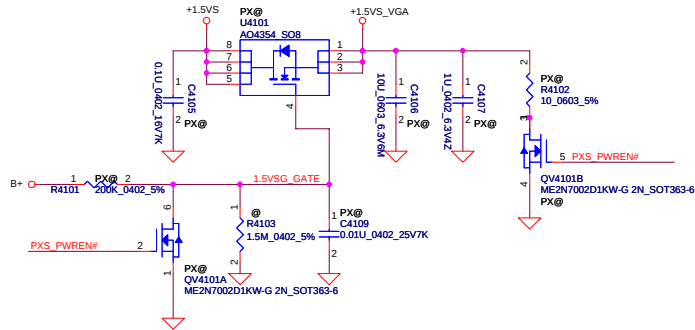
AC Coupling Capacitor
PCIe Gen3: Recommended value is 220 nF
PCIe Gen1 and Gen2 only: Recommended value is 100 nF

No Use GPU Display Port output

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2013/01/11		2013/12/31		2013/12/31	
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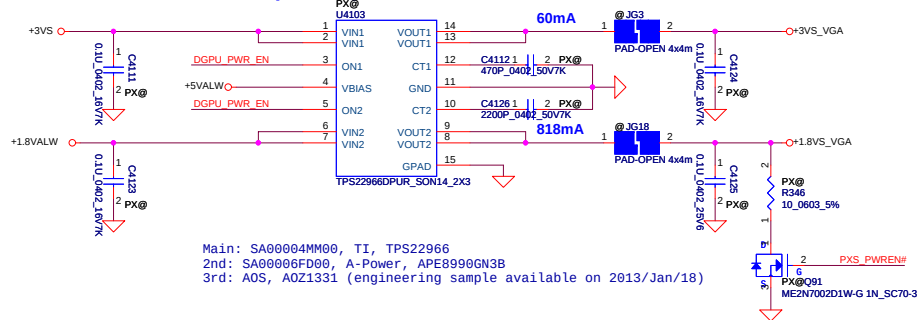
+1.5VS to +1.5VS_VGA (2.096A)



+3VS to +3VS_VGA (25mA)

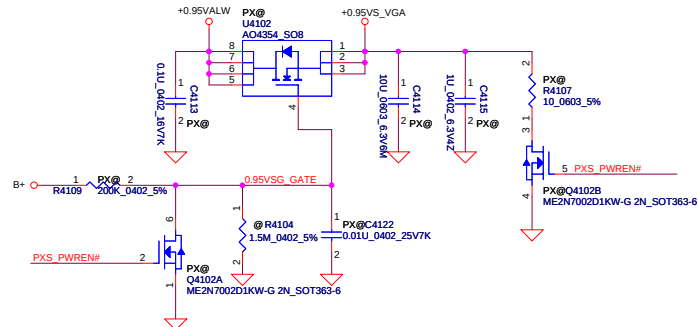
+1.8VALW to +1.8VS_VGA (311mA)

+1.8VS_VGA 必須比 +VGA_CORE晚起來



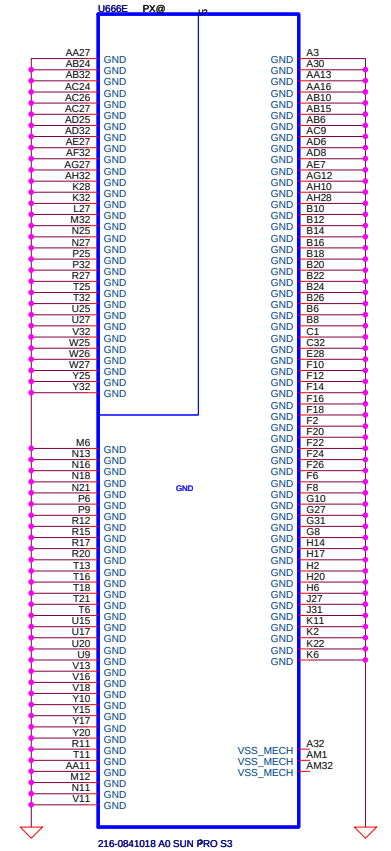
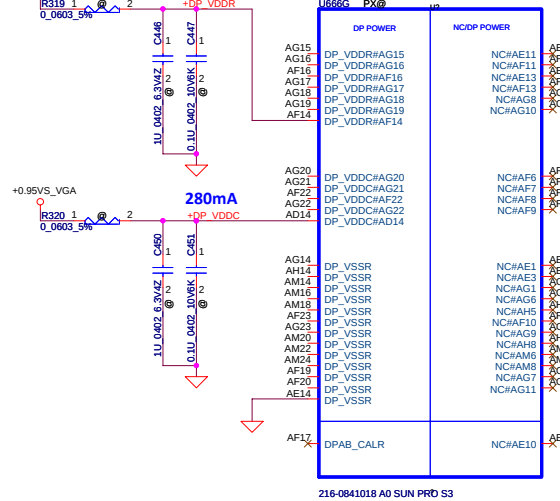
Main: SA00004MM00, TI, TPS22966
2nd: SA00006FD00, A-Power, APE8990GN3B
3rd: A0S, A0Z1331 (engineering sample available on 2013/Jan/18)

+0.95VALW to +0.95VSG (4.016A)



370mA (HDMI) 188mA (Display Port)

No Use GPU Display Port output



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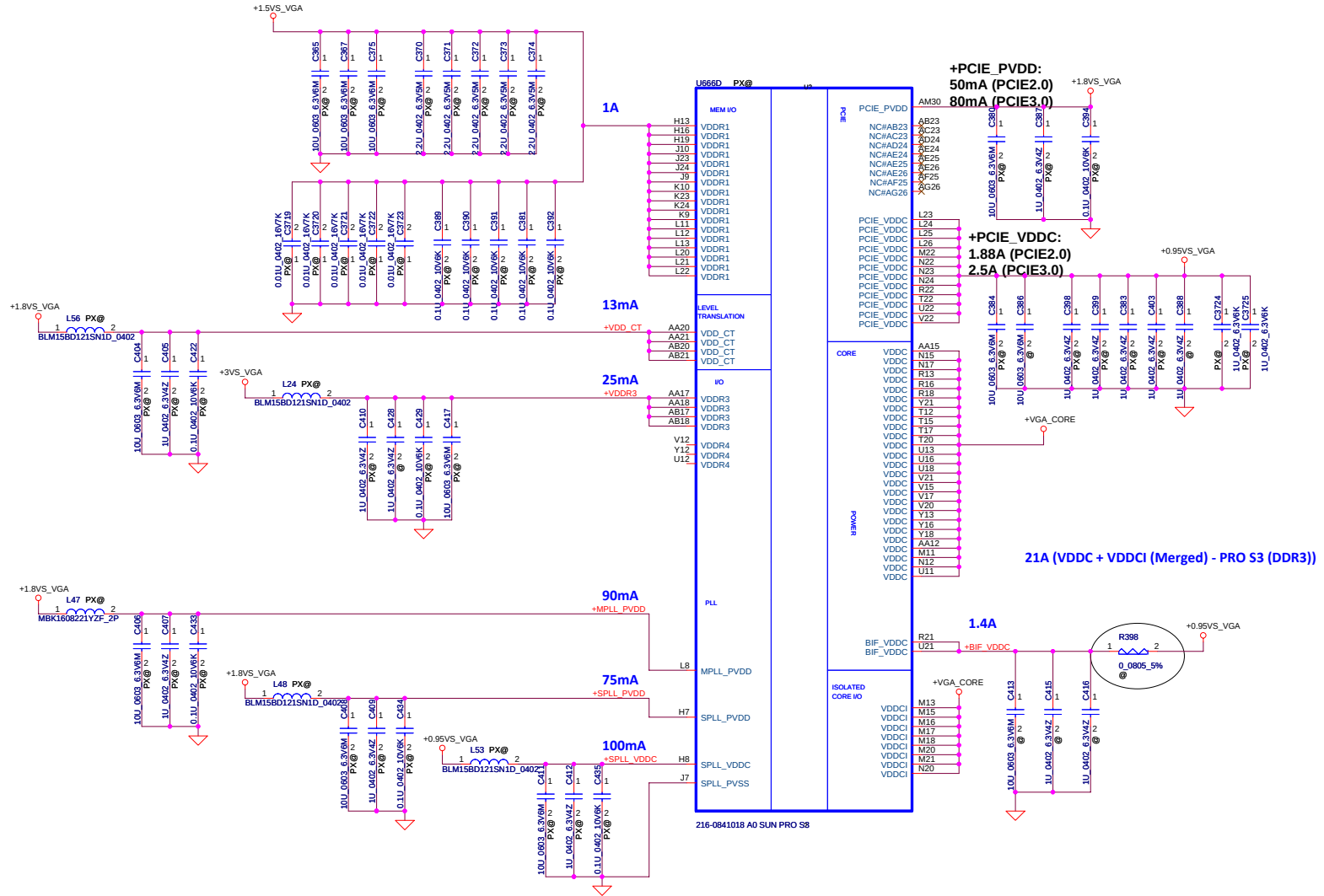
+VGA_CORE	10uF	1uF	0.1uF
VDDC	TBD	5 (1@)	10 (2@)
VDDCI	3.5A	1	3

+0.95VS_VGA	10uF	1uF	0.1uF
PCIE_VDDC	2.5A	2 (1@)	5 (1@)
BIF_VDDC	1.4A	0	0
SPLL_VDDC	100mA	1	1

+1.5VS_VGA	10uF	1uF	0.1uF
VDDR1	1.5A	3	5

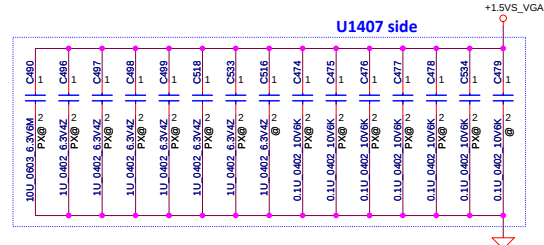
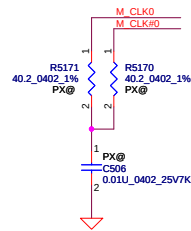
+1.8VS_VGA	10uF	1uF	0.1uF
PCIE_PVDD	100mA	1	1
MPLL_PVDD	130mA	1	1
SPLL_PVDD	75mA	1	1
VDDR4	(300mA)	0	0
VDD_CT	13mA	1	1
+TSVDD	13mA	1	1
+DP_VDDR	0	0	0
+DP_VDDC	0	0	0

+3VS_VGA	10uF	1uF	0.1uF
VDDR3	25mA	0	2 (1@)



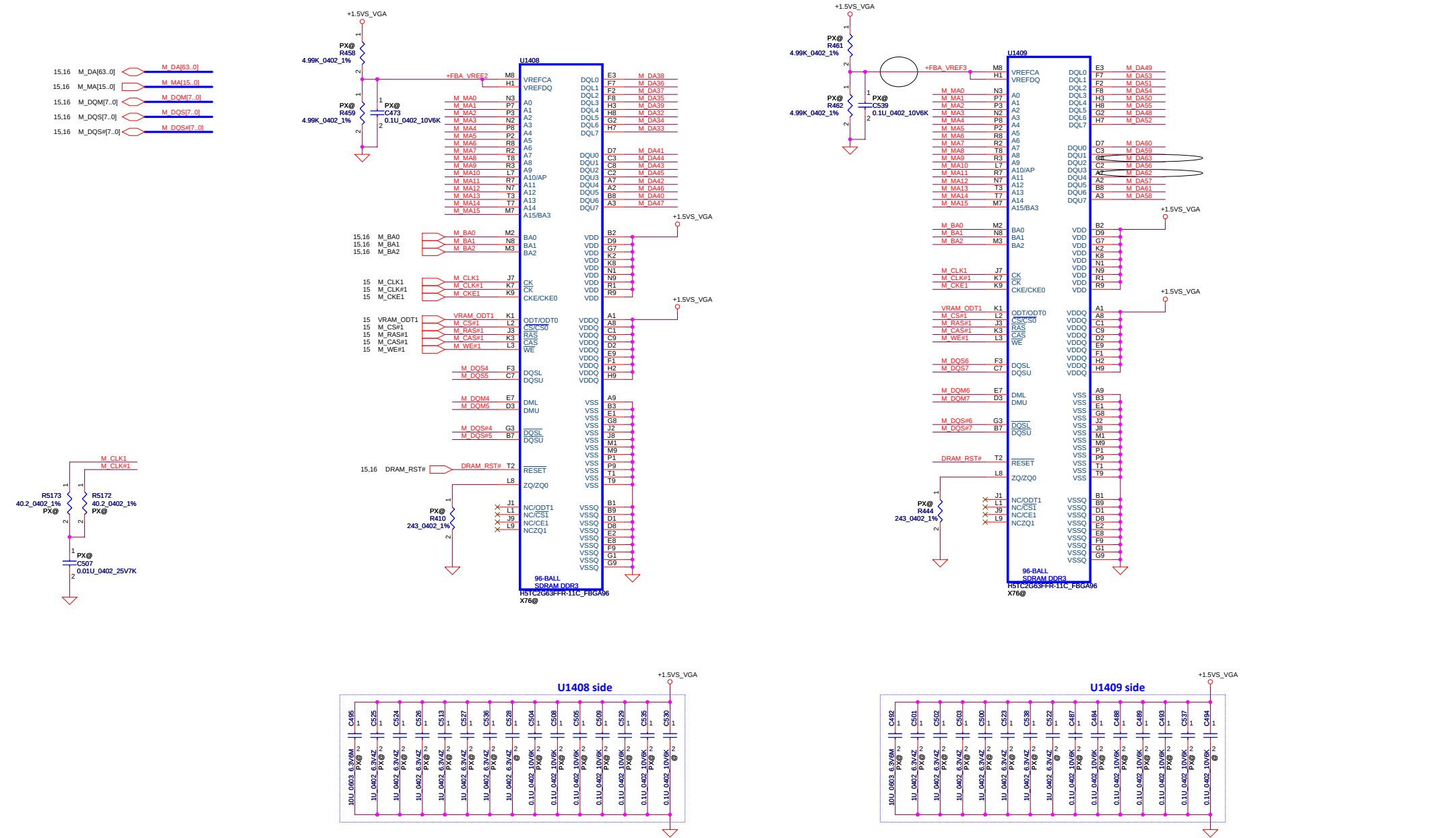
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15,17	M_DA[63..0]		M_DA[63..0]
15,17	M_MA[15..0]		M_MA[15..0]
15,17	M_DQM[7..0]		M_DQM[7..0]
15,17	M_DQS[7..0]		M_DQS[7..0]
15,17	M_DQS#[7..0]		M_DQS#[7..0]

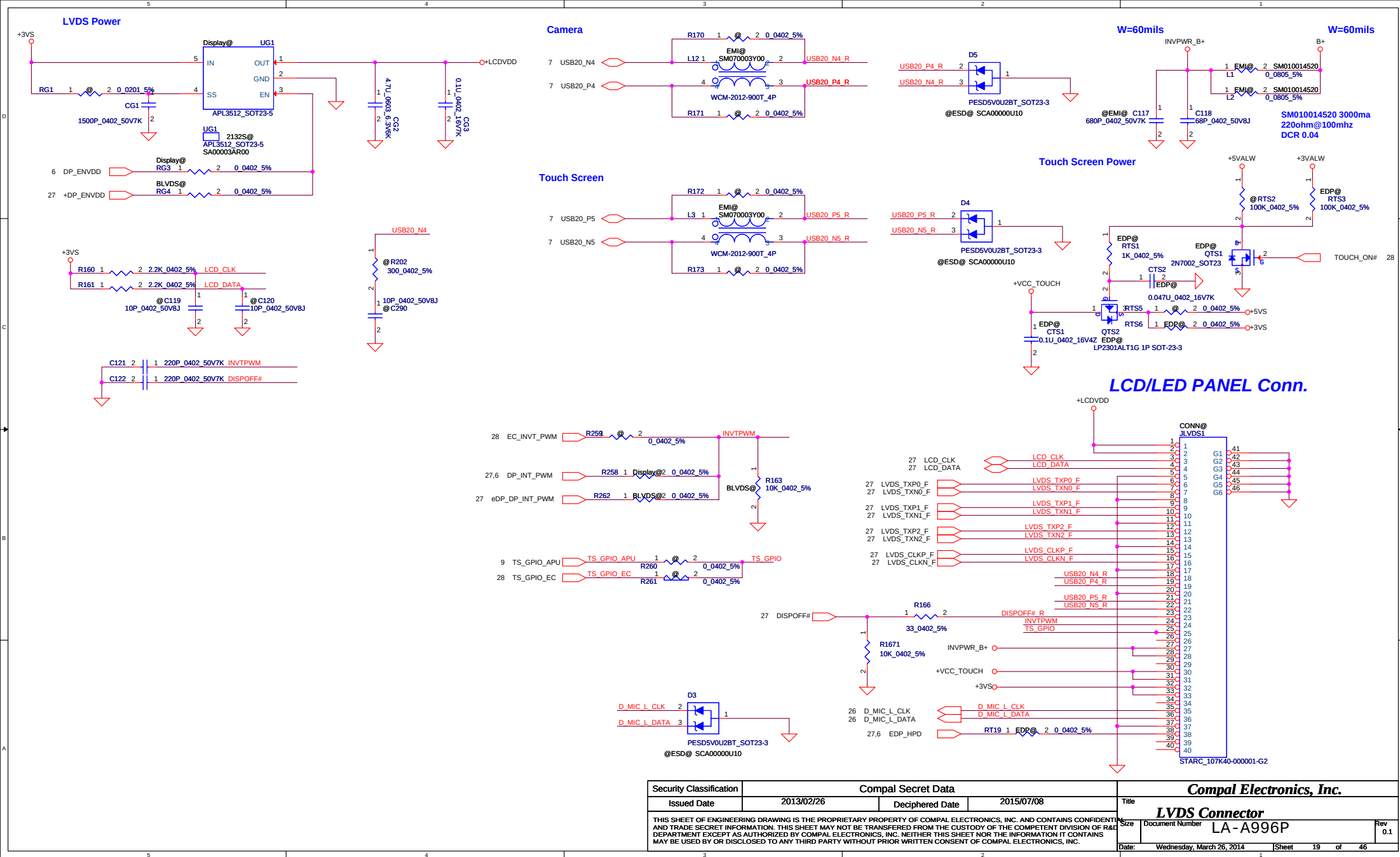


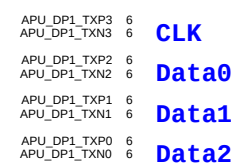
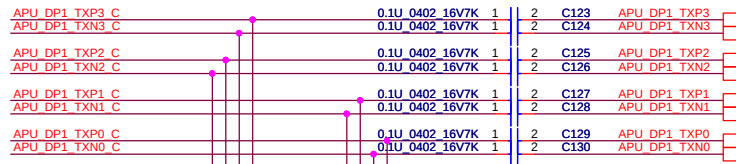
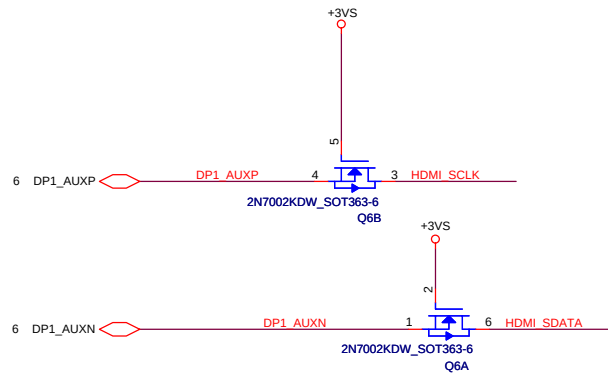
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				Custom	LA-A996P	0.1	
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Memory Partition A - Upper 32 bits

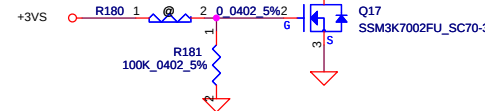


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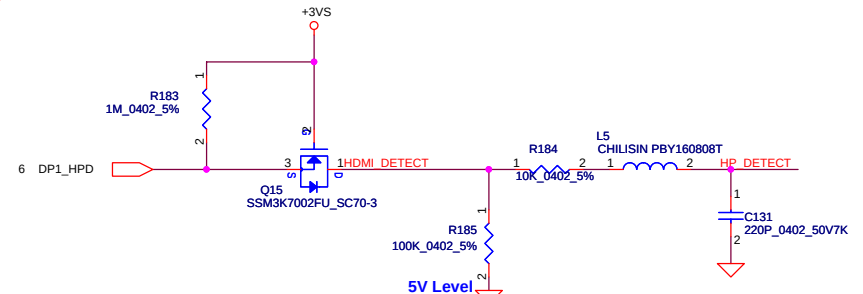
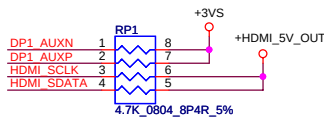
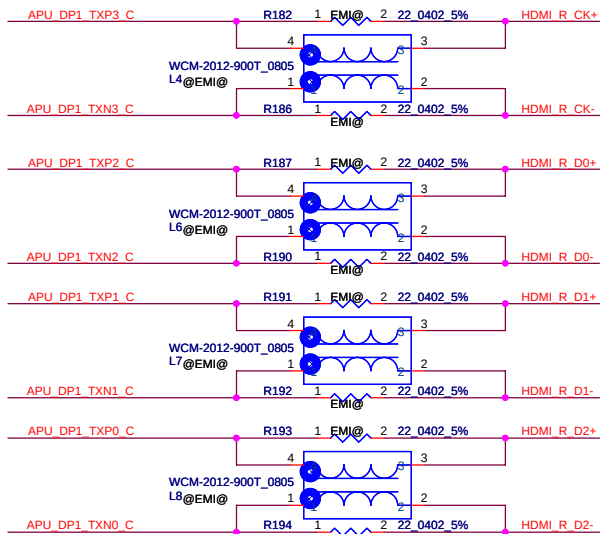




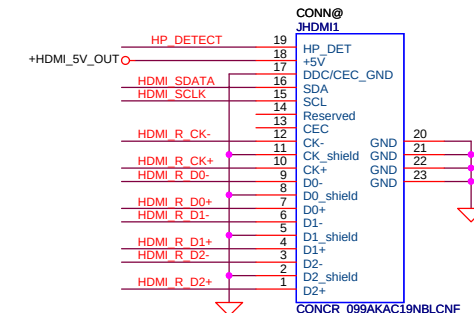
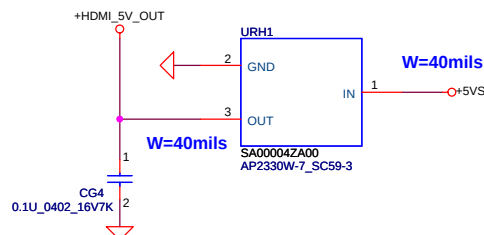
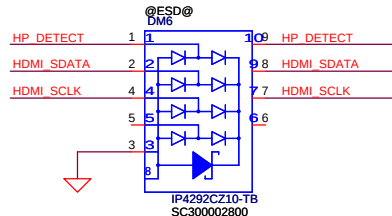
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SM070001310 400ma 90ohm@100mhz DCR 0.3

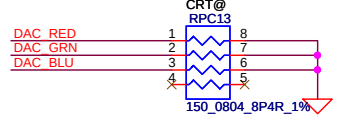
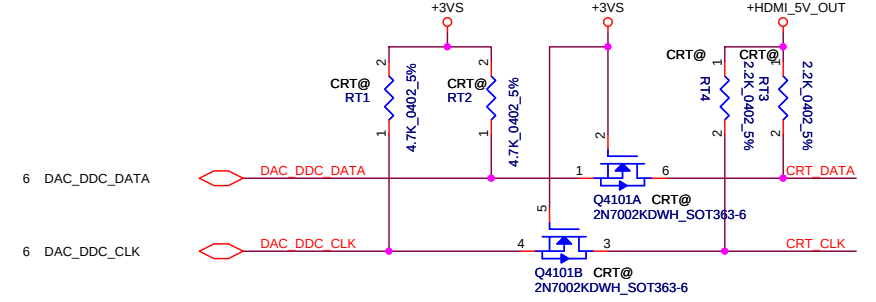
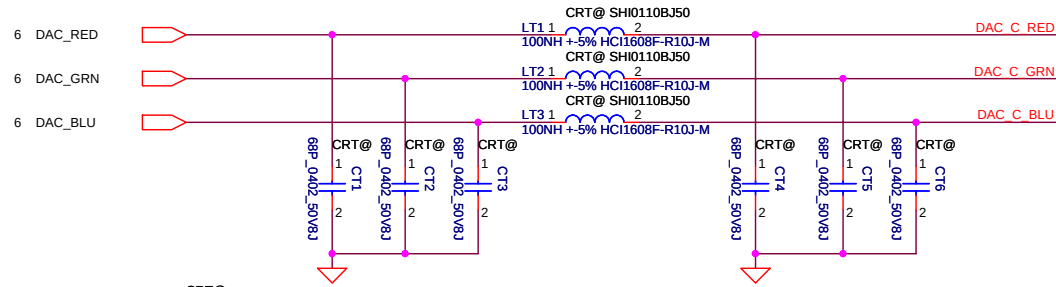
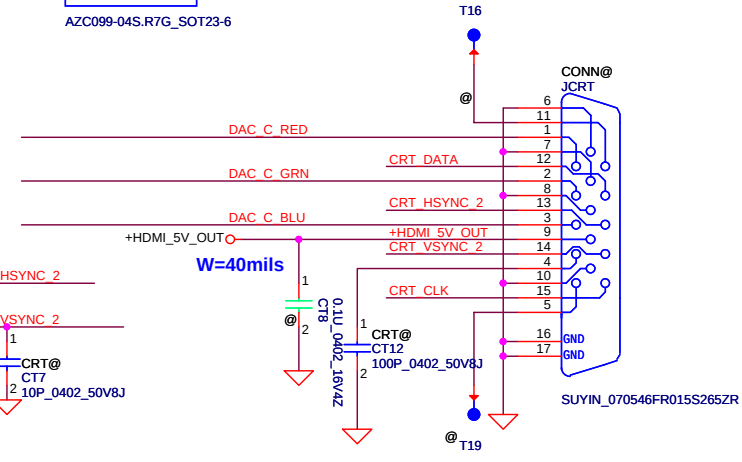
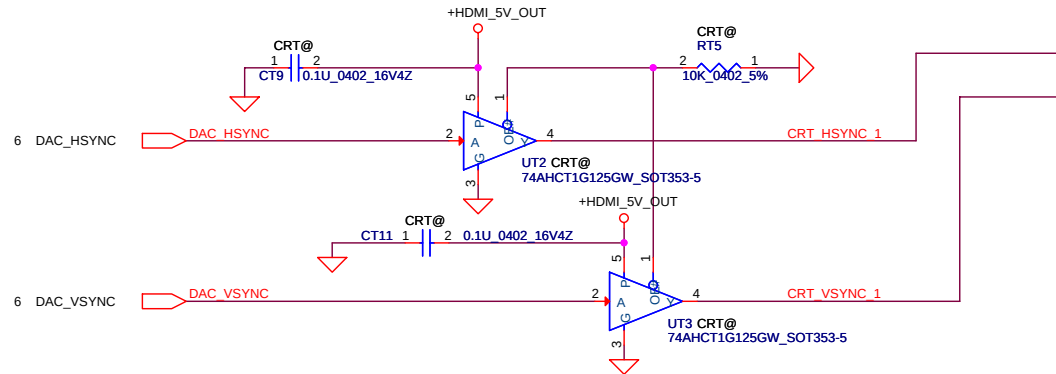
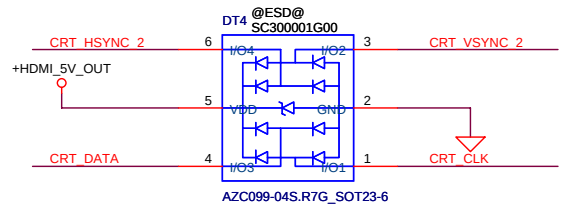
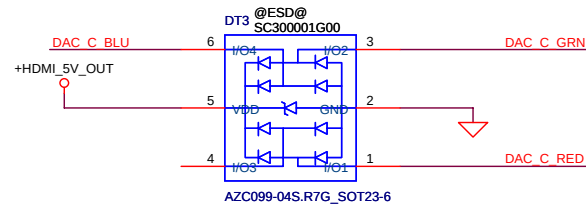


8/20 change HDMI Conn HDMI Conn.

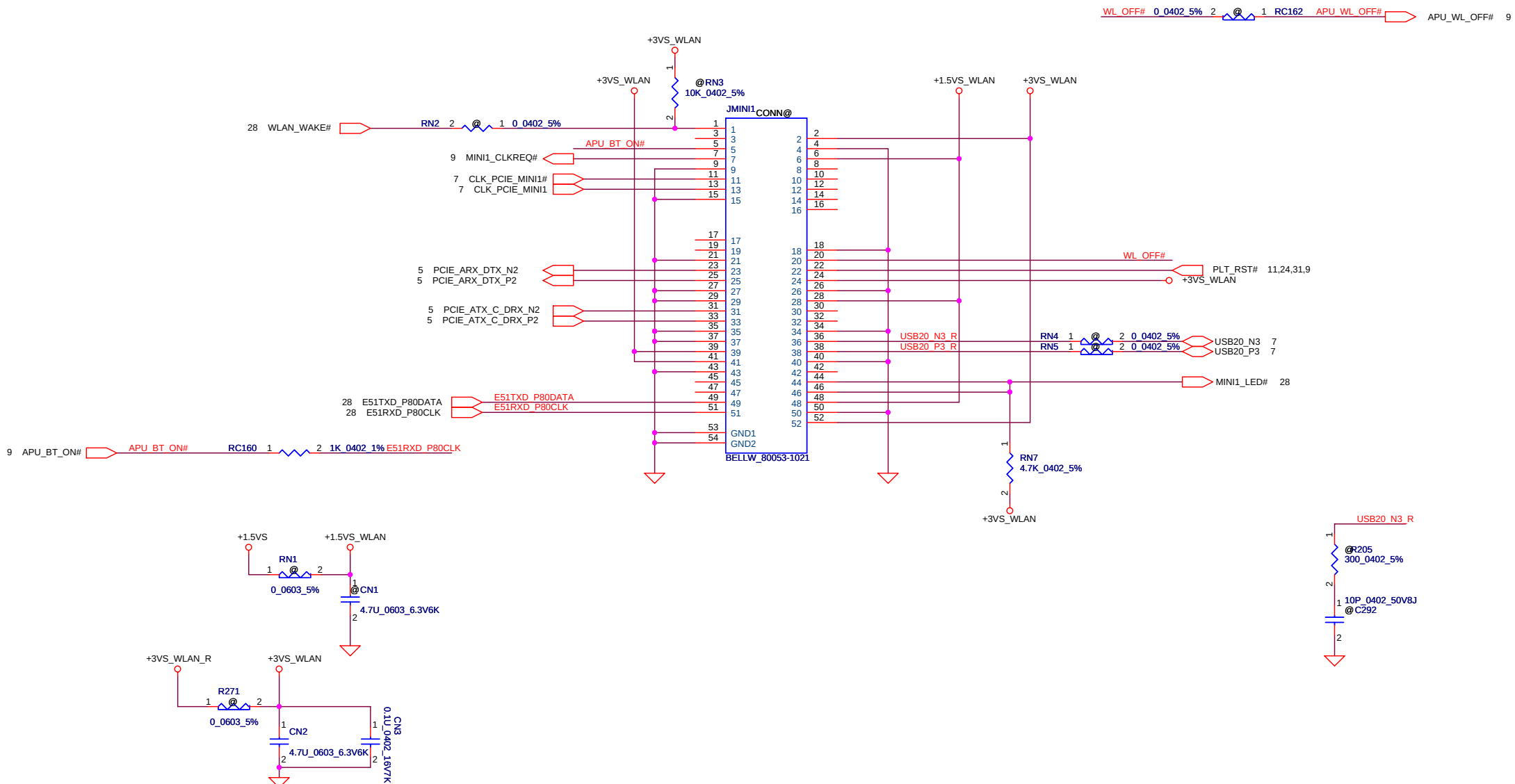


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				Size	Rev
				Custom	0.1
				Date	Monday, February 17, 2014
				Sheet	20 of 46

CRT share HDMI Power

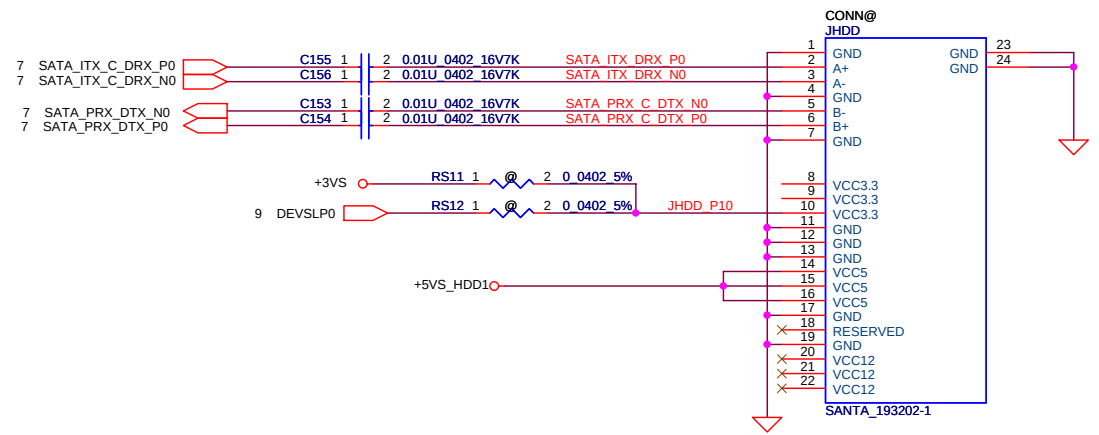
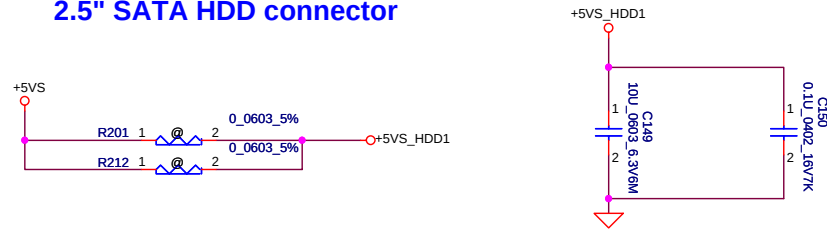


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				Date:	Friday, February 21, 2014
				Sheet	21 of 46

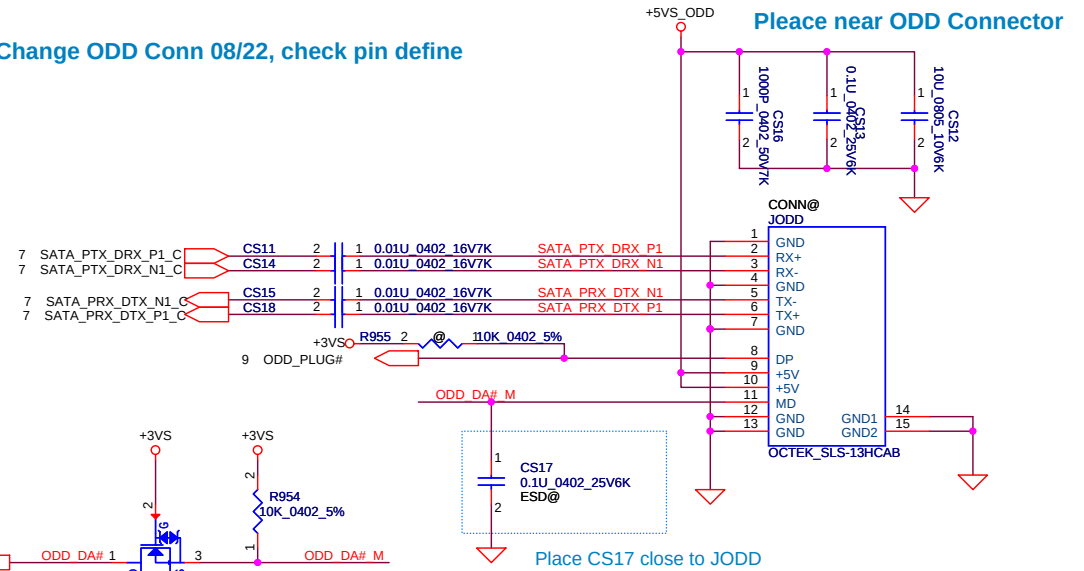
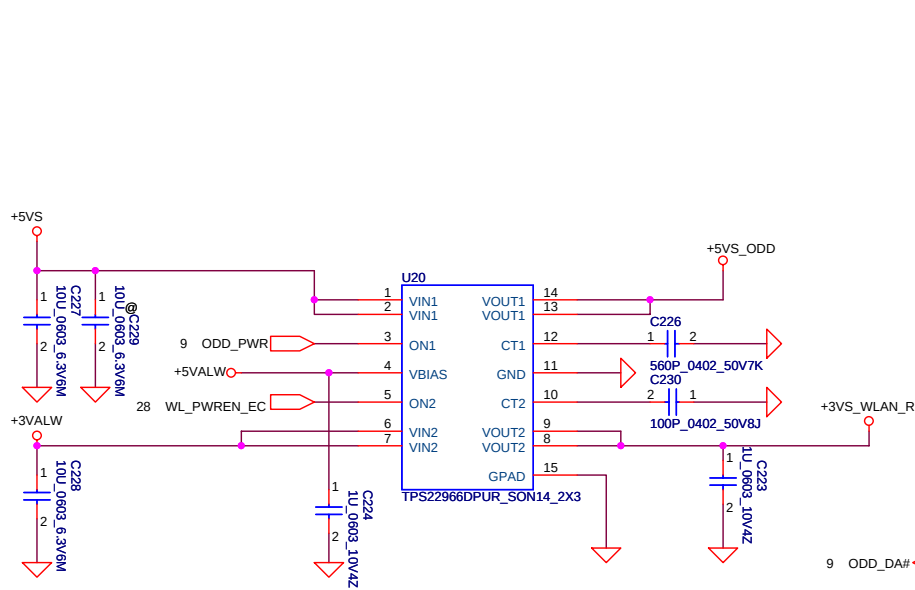


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Issued Date		2013/02/26		Deciphered Date		2015/07/08		Title		
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								Document Number		
								LA-A996P		
								Date: Monday, February 17, 2014		

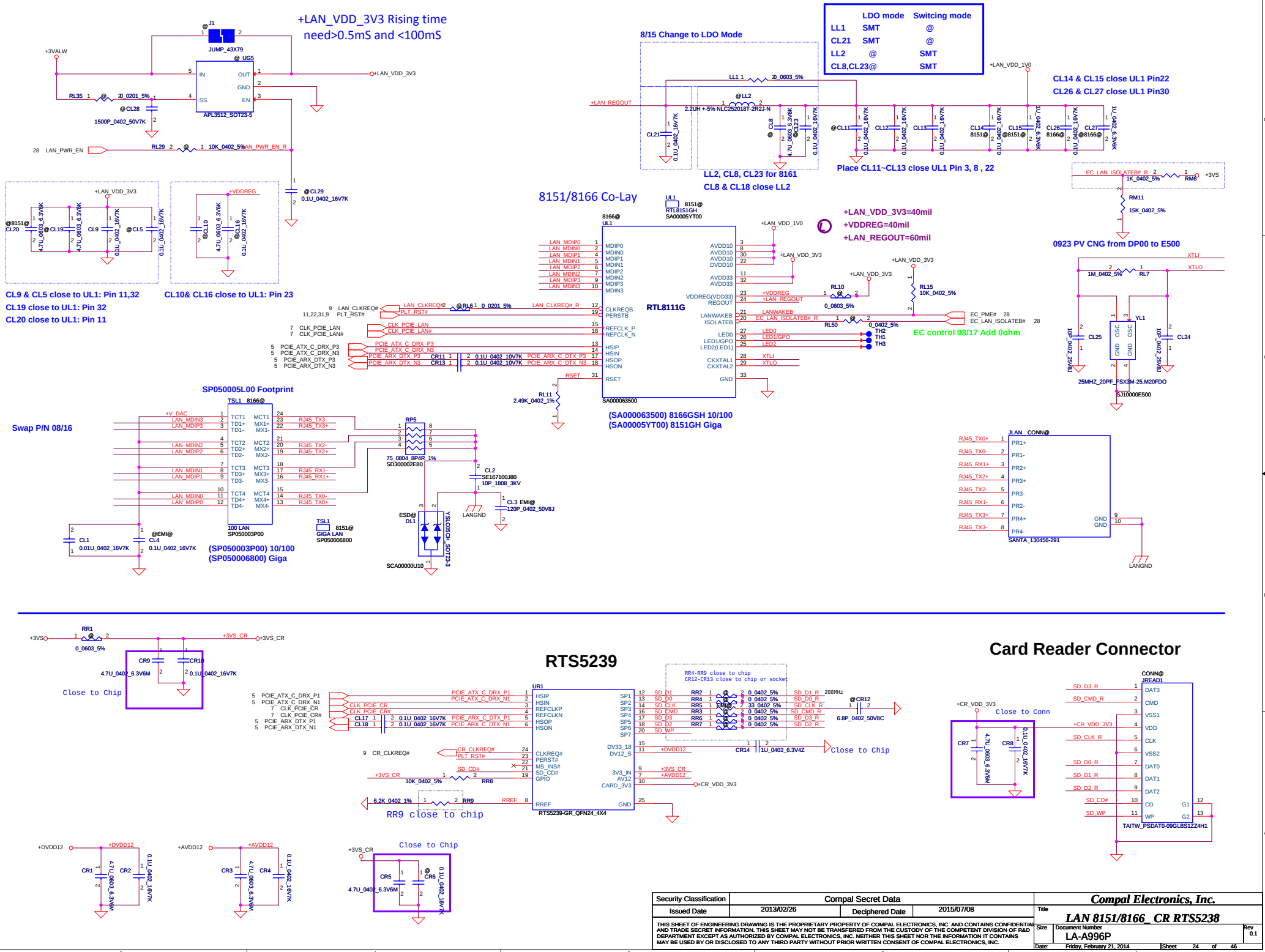
2.5" SATA HDD connector



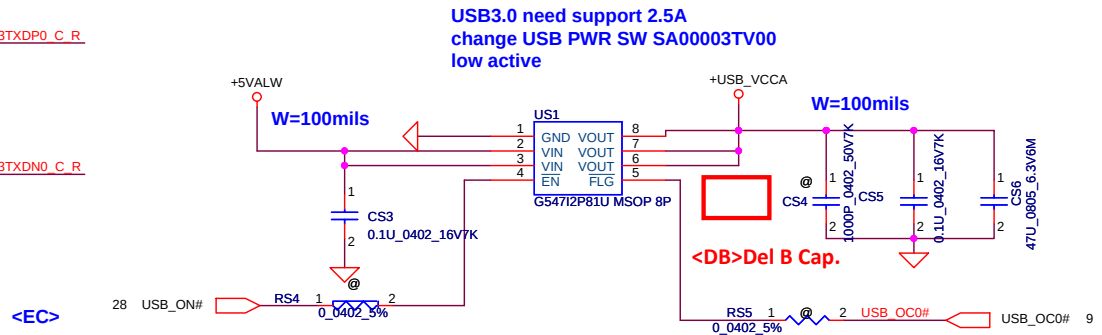
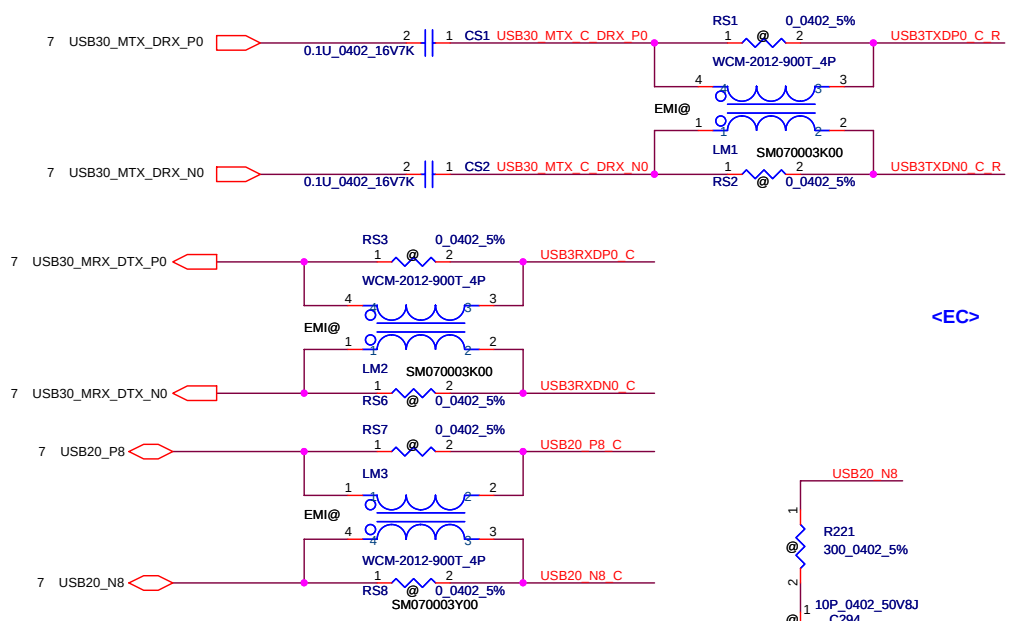
Change ODD Conn 08/22, check pin define



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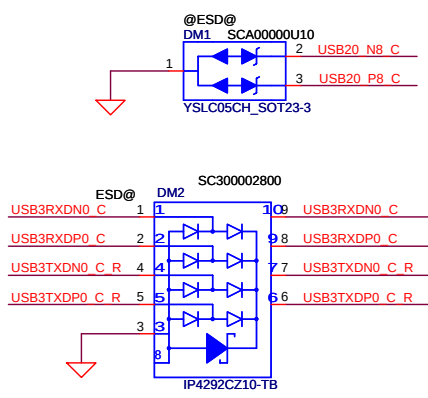


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Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	
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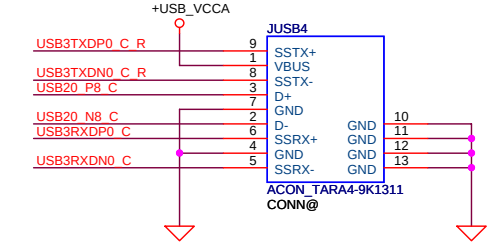


USB3.0 need support 2.5A
change USB PWR SW SA00003TV00
low active

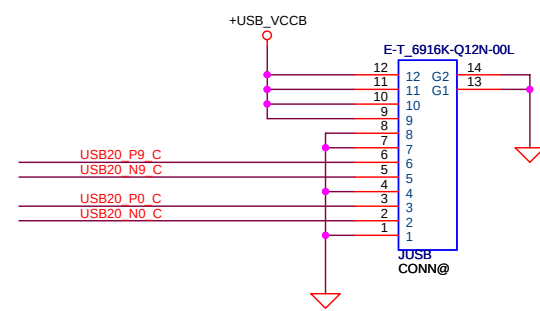
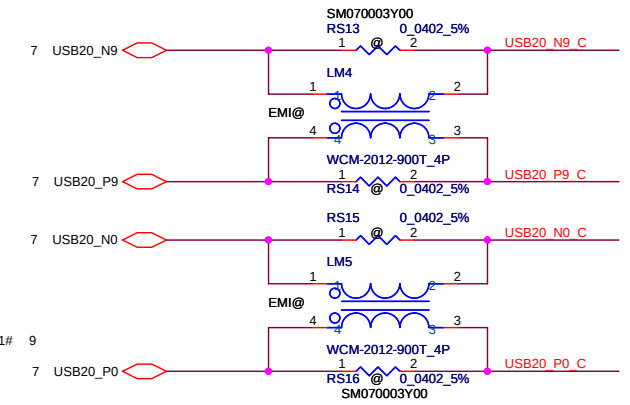
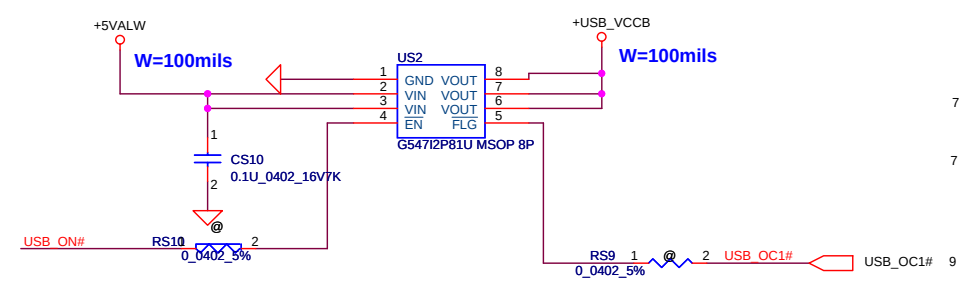
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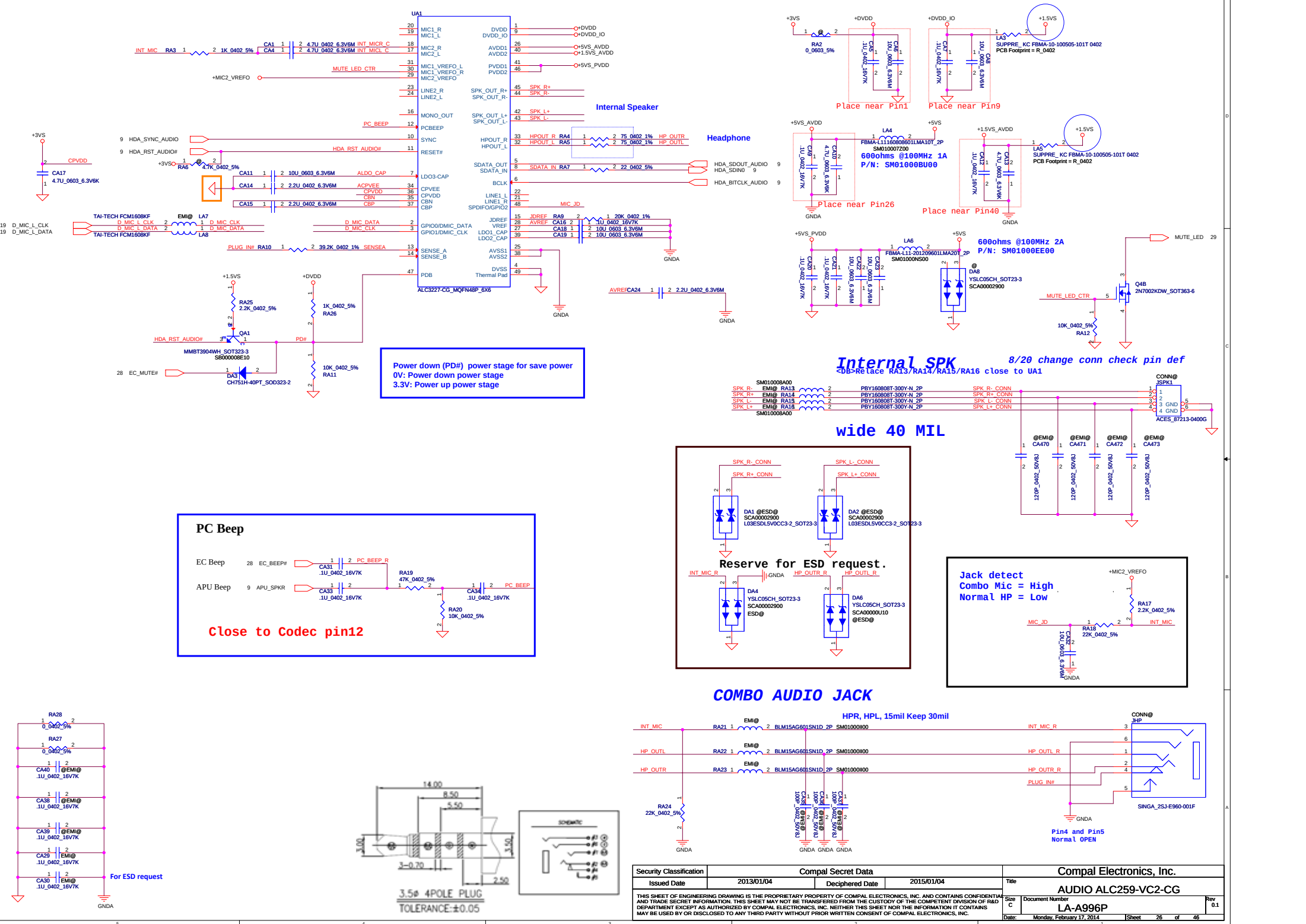
USB2.0/USB3.0 port 1



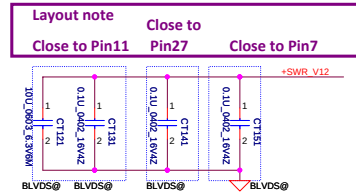
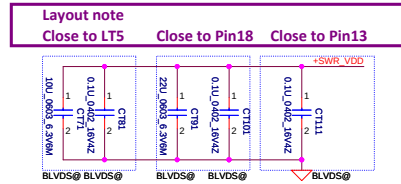
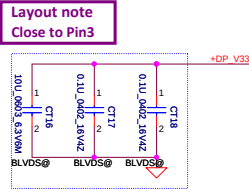
USB2.0 port x 2



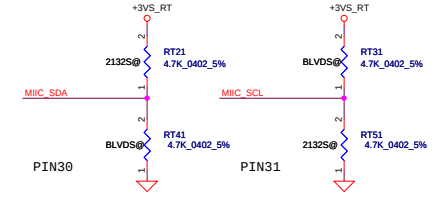
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Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	USB 3.0/2.0 conn
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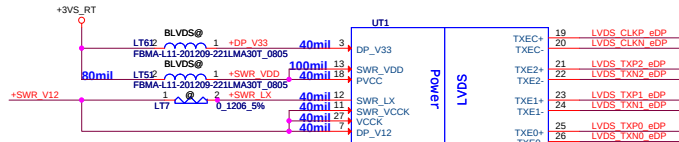


※ROM only mode : PIN 30 4.7k pull low, Pin 31 4.7k pull high.
EP mode : PIN 30 4.7k pull high, Pin 31 4.7k pull low.
EEPROM : PIN 30 4.7k pull high, Pin 31 4.7k pull high.
(※Default mode)

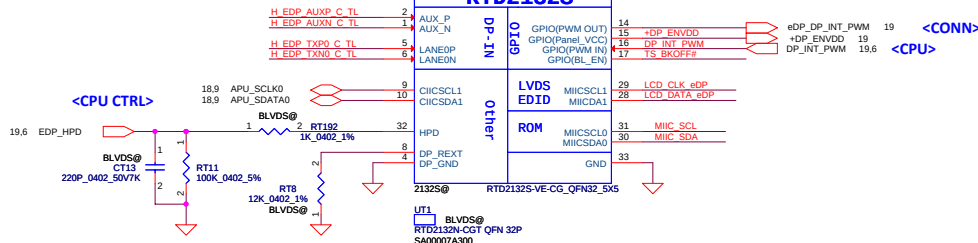


SWR / LDO Mode select		
	LDO	SWR
2132S	Do not support	mount LT7
2132N	Use 0 ohm	mount LT7

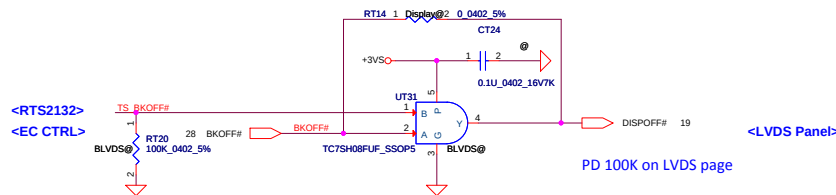
※ If use 2132N, please select LDO mode as default.



	display@	EDP@	KLVDS@	BLVDS@	Kabini@	Beema@
Kabini LVDS	V		V		V	
Kabini EDP	V	V			V	
Beema LVDS				V		V
Beema EDP	V	V				V



Layout note
Close to Pin8



PD 100k on LVDS page

<LVDS Panel>

LTDP0_TXP3
LTDP0_TXN3
LTDP0_TXP2
LTDP0_TXN2

LVDS_CLKN
LVDS_CLKP
LVDS_TXN0
LVDS_TXP0

LVDS_CLKP_eDP
LVDS_CLKN_eDP
LVDS_TXP0_eDP
LVDS_TXN0_eDP

<CPU>

LTDP0_TXP1
LTDP0_TXN1

LVDS_TXP1
LVDS_TXN1

LVDS_TXP1_eDP
LVDS_TXN1_eDP

LTDP0_TXP0
LTDP0_TXN0

LVDS_TXP2
LVDS_TXN2

LVDS_TXP0_eDP
LVDS_TXN0_eDP

LTDP0_AUXP
LTDP0_AUXN

AUXP_DDC_CLK
AUXN_DDC_DATA

LCD_DATA_eDP
LCD_CLK_eDP

RP40 Close CPU

RT24~27 Close JLVDS conn

LVDS_TXP2	RT33	1	Display@2	0.0402 5%	LVDS_TXP2_K	RT24	1	KLVDS@2	0.0402 5%	LVDS_TXP2_F
LVDS_TXN2	RT34	1	Display@2	0.0402 5%	LVDS_TXN2_K	RT25	1	KLVDS@2	0.0402 5%	LVDS_TXN2_F
AUXP_DDC_CLK	RT35	1	Display@2	0.0402 5%	AUXP_DDC_CLK_K	RT26	1	KLVDS@2	0.0402 5%	LCD_CLK
AUXN_DDC_DATA	RT36	1	Display@2	0.0402 5%	AUXN_DDC_DATA_K	RT27	1	KLVDS@2	0.0402 5%	LCD_DATA

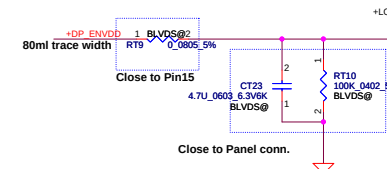
	PIN15
2132S	TL_ENVDD
BLVDS	+LCD_VDD *

* Version R internal Power Switch, can output 1A, Rds(on)=0.2 ohm

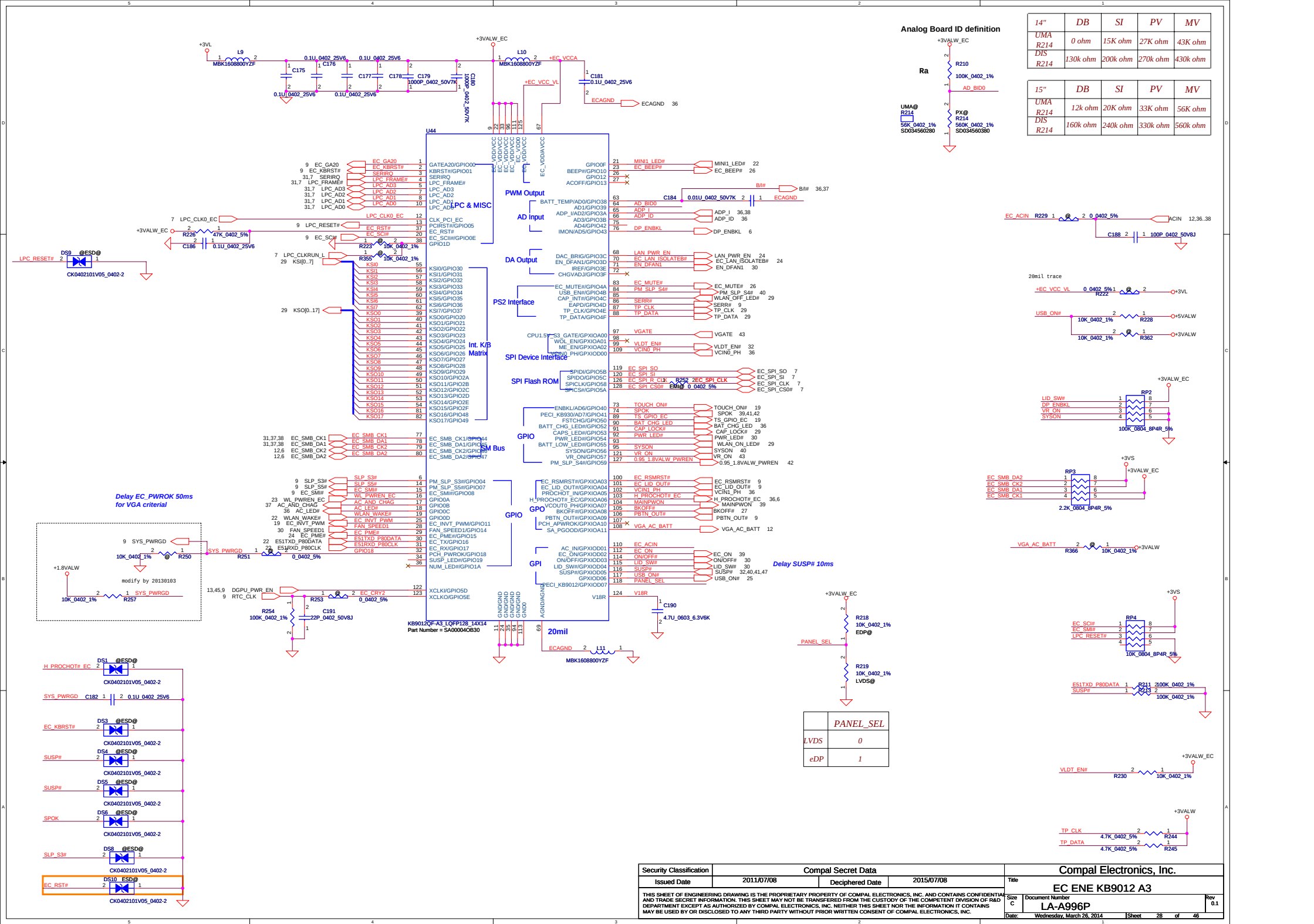
PIN16	Accept voltage input (high level)
2132S	3.3V
BLVDS	1.5~3.3V

* Version R has internal level shifter, remove level shifter circuit on AMD platform

Different between 2132S and 2132N(BLVDS)	
2132S	2132N
1. Support SWR mode	1. Support LDO mode and SWR mode 2. Internal ROM 3. Support LCD_VDD(internal Power switch) 4. Integrates Level shifter



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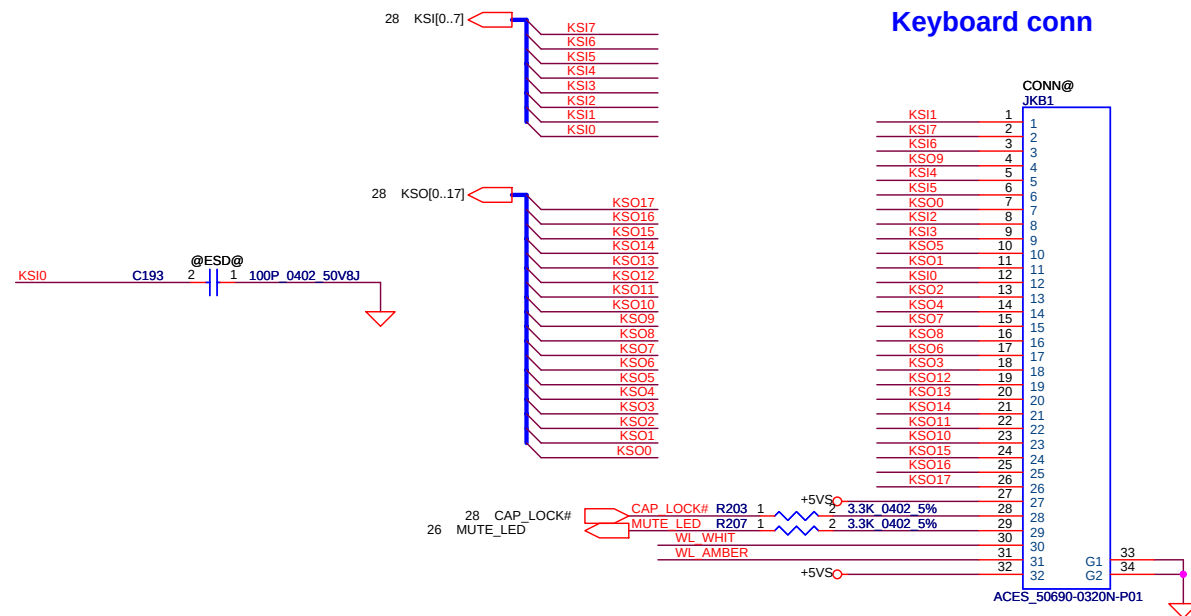


14"	DB	SI	PV	MV
UMA R214	0 ohm	15K ohm	27K ohm	43K ohm
DIS R214	130k ohm	200k ohm	270k ohm	430k ohm

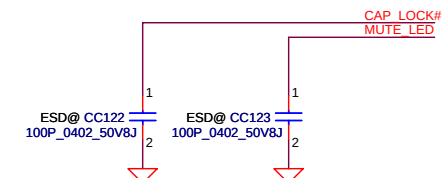
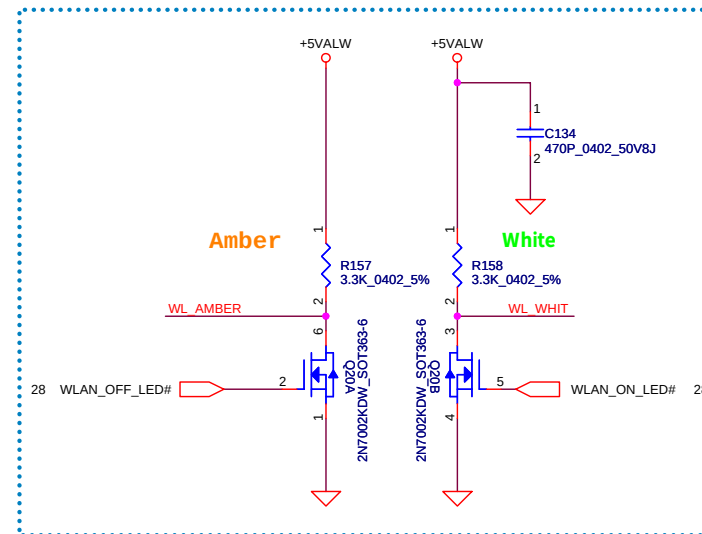
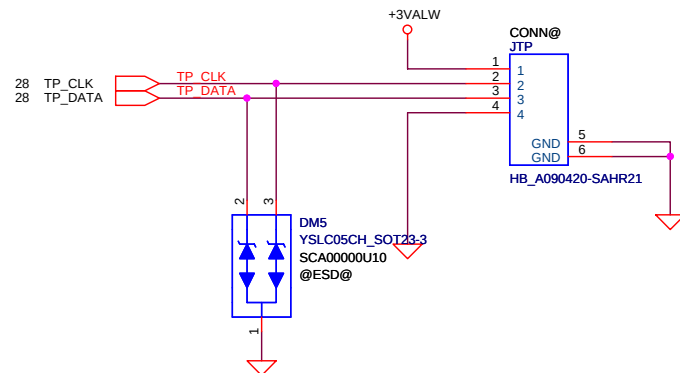
15"	DB	SI	PV	MV
UMA R214	12k ohm	20K ohm	33K ohm	56K ohm
DIS R214	160k ohm	240k ohm	330k ohm	560k ohm

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Keyboard conn

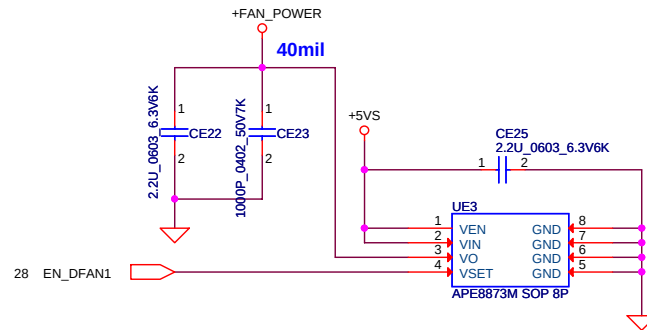
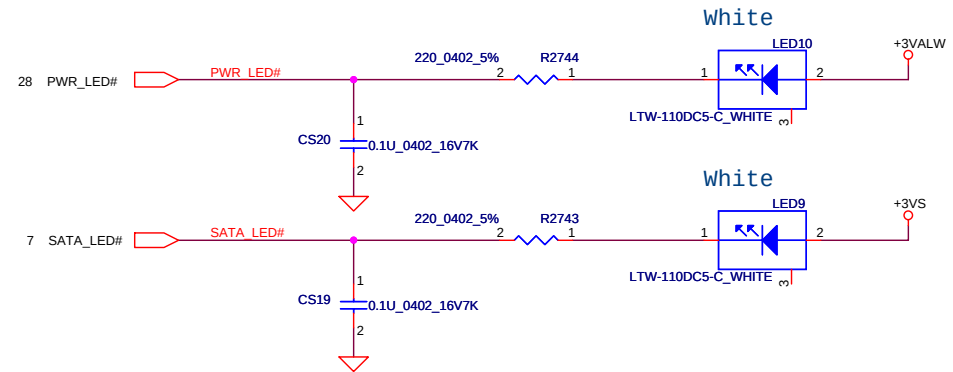
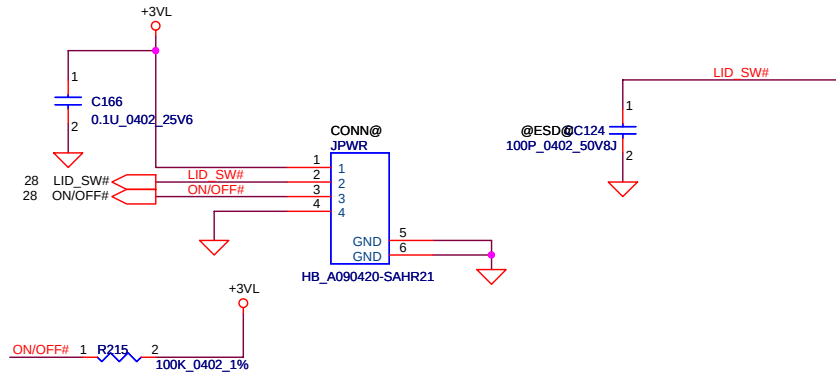


Touch pad conn

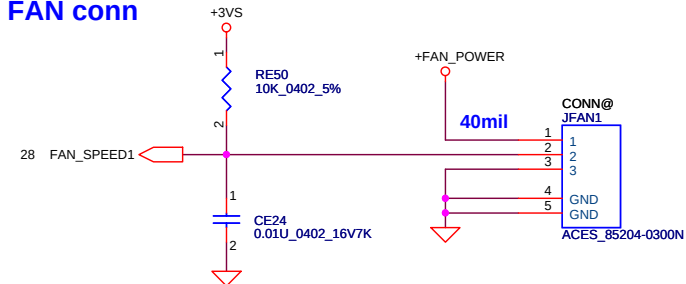


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								Document Number		Rev	
								LA-A996P		0.1	
								Date		Sheet	
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Power Button Connector

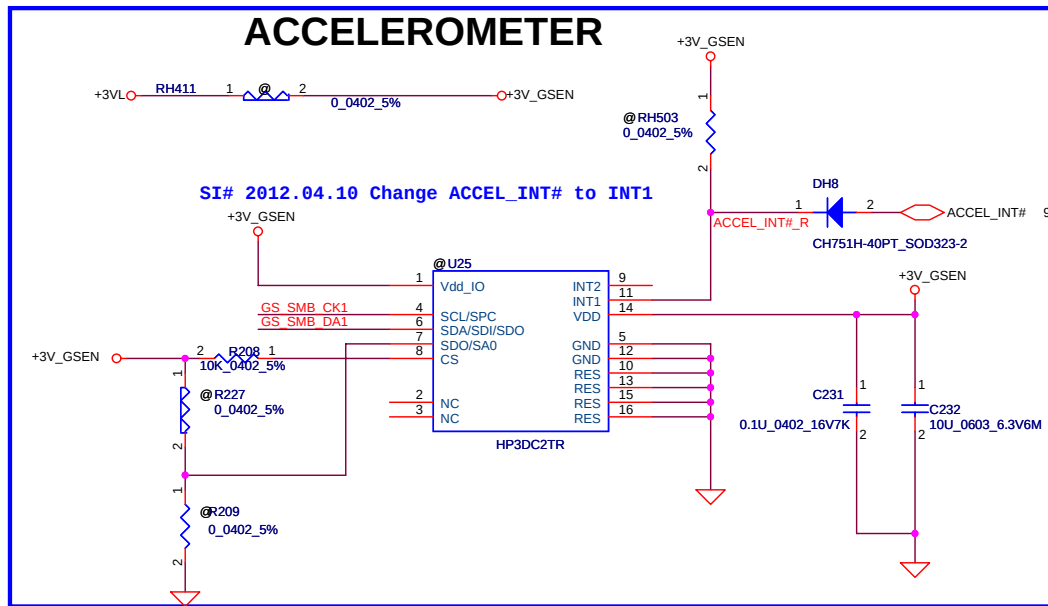


FAN conn



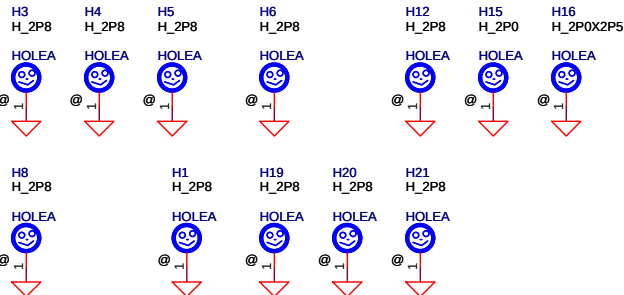
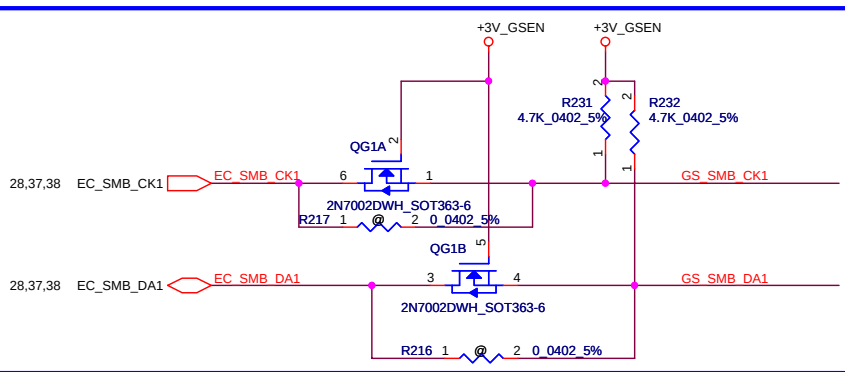
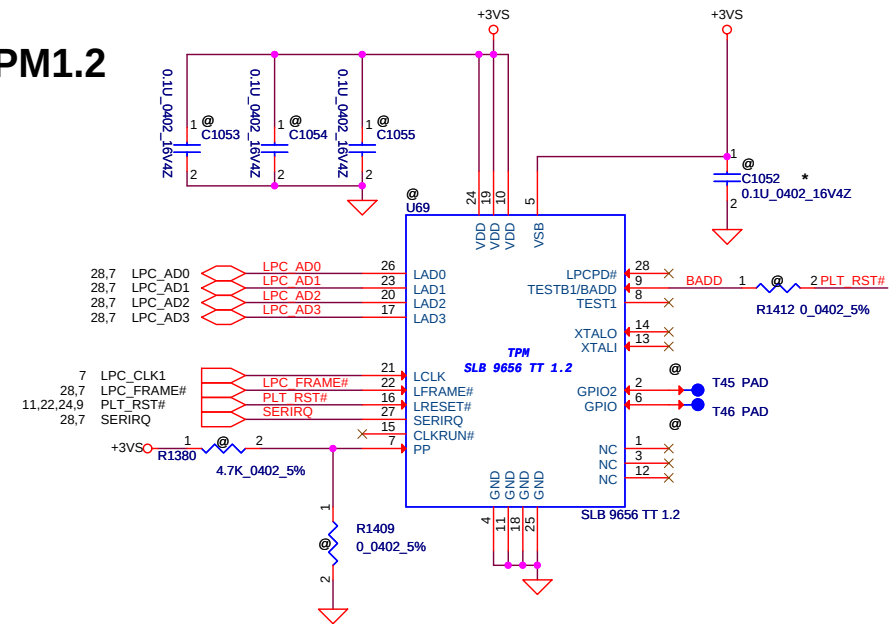
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Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	PWRBTN/FAN	
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ACCELEROMETER

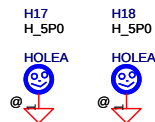


Add TPM Circuit in PV Phase

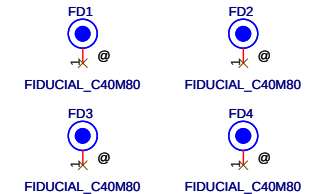
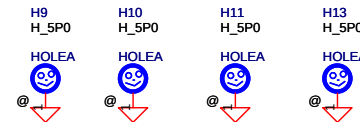
TPM1.2



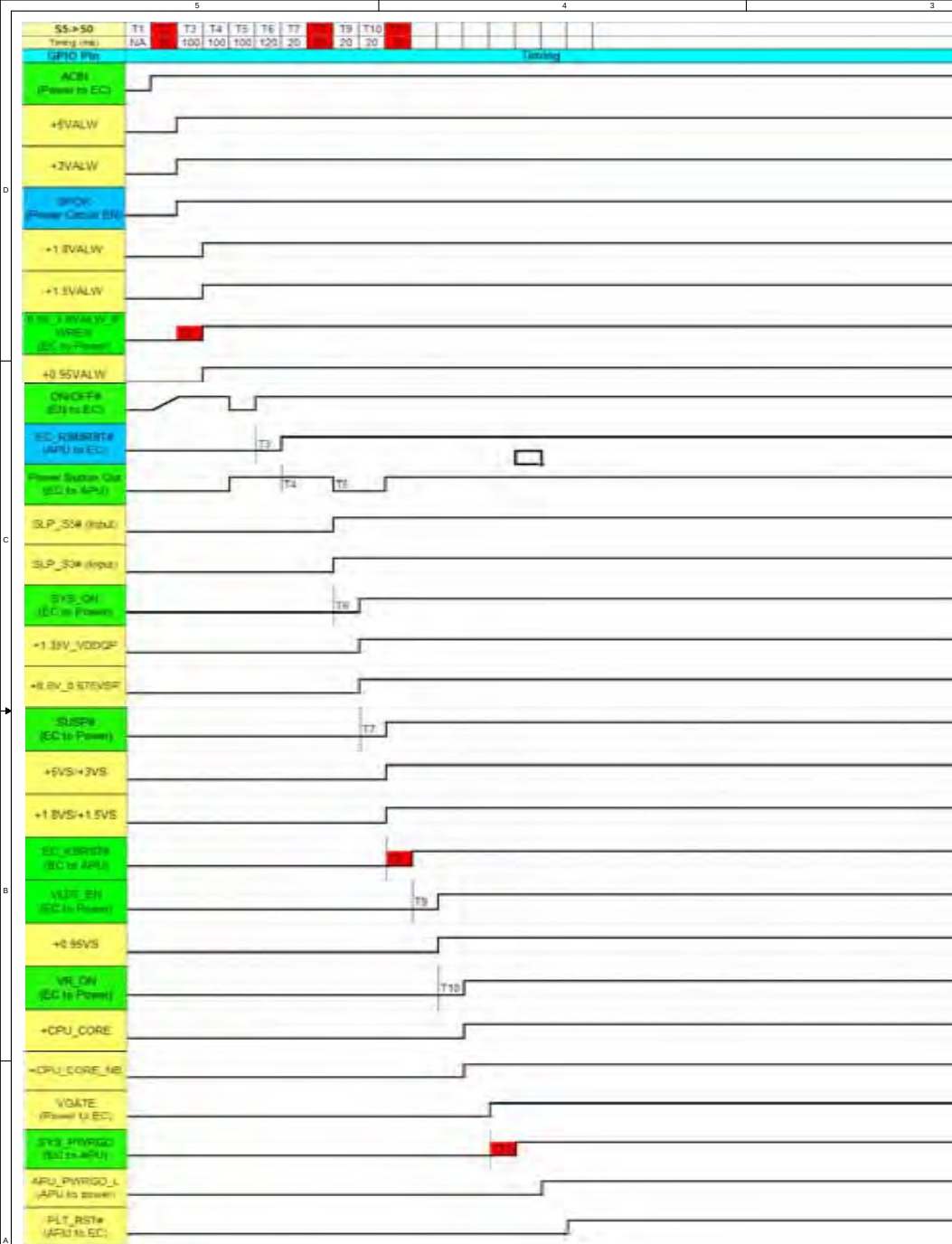
VGA



CPU



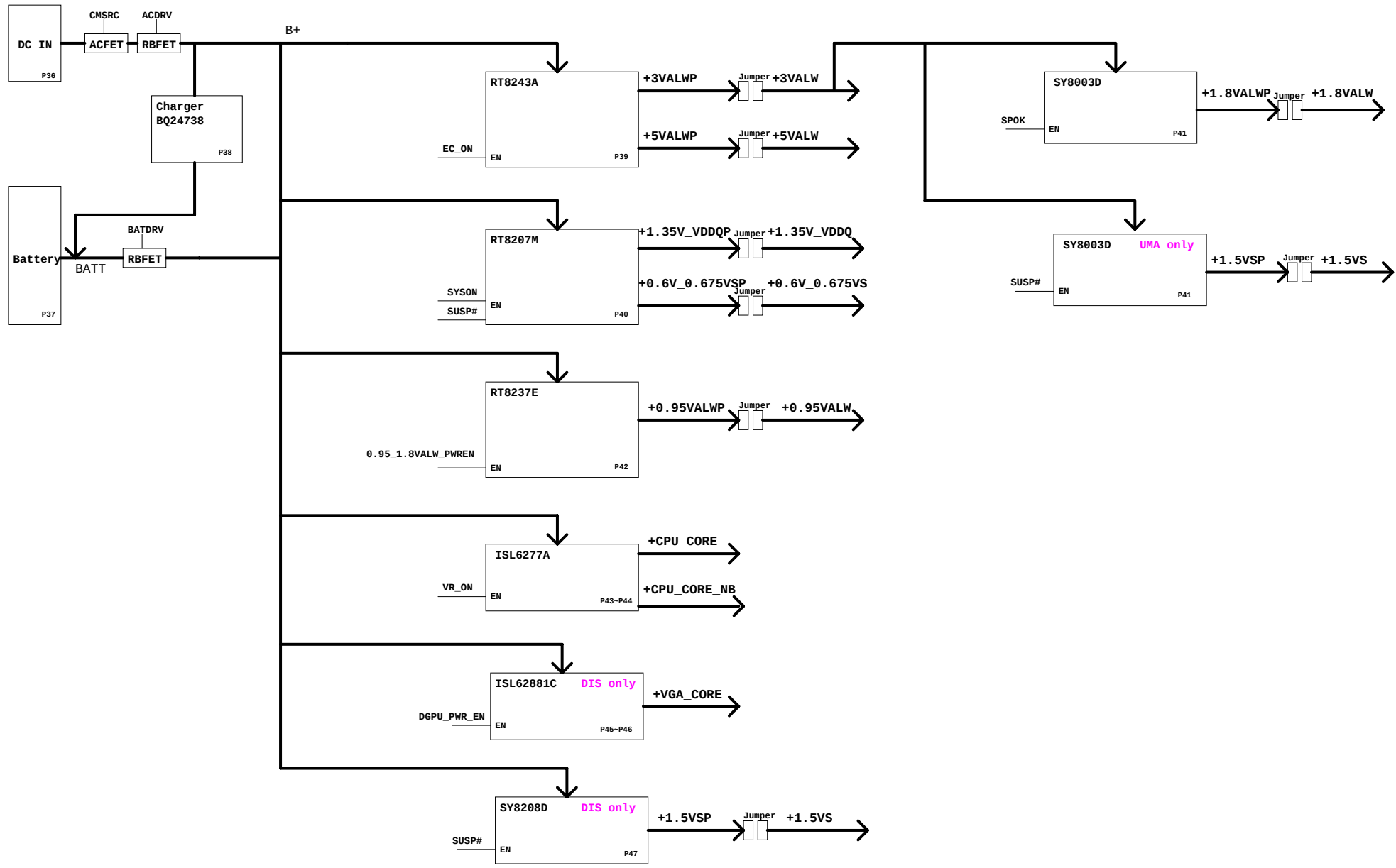
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	LED/Screw hole
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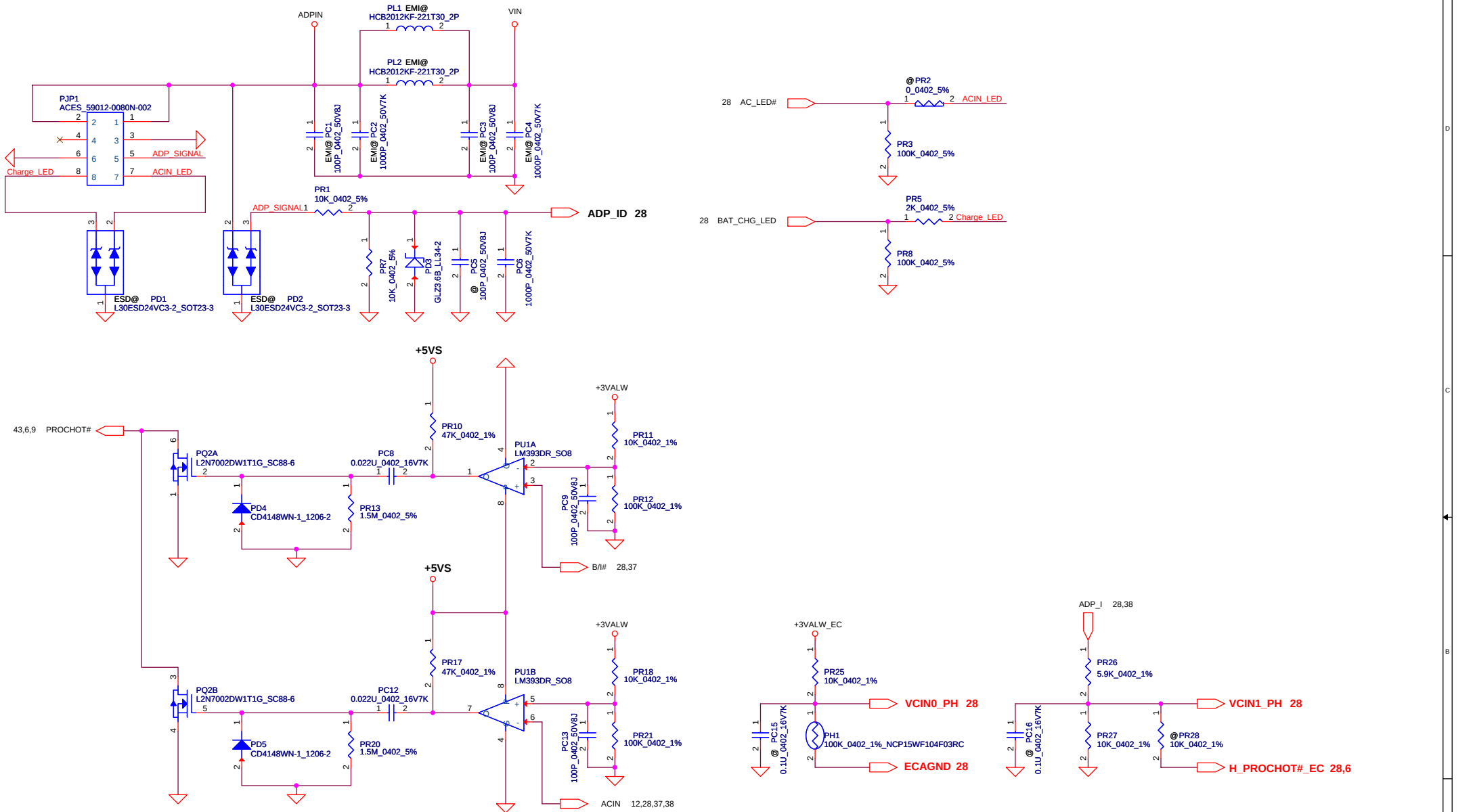
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5	4	3	2	1
D				D
C				C
B				B
A				A

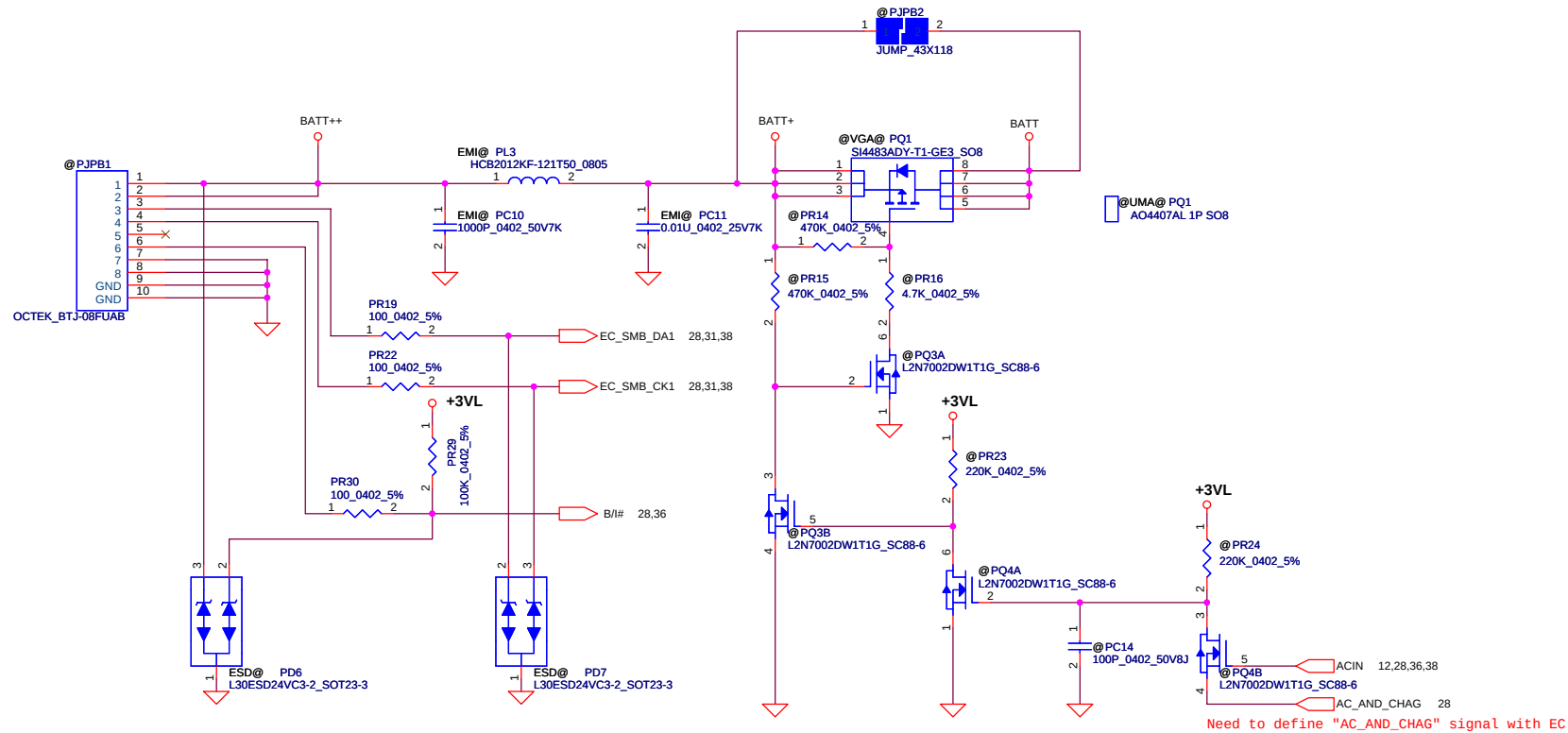
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	EE Change list
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				LA-A996P	0.1
Date	Monday, February 17, 2014			Sheet	34 of 46



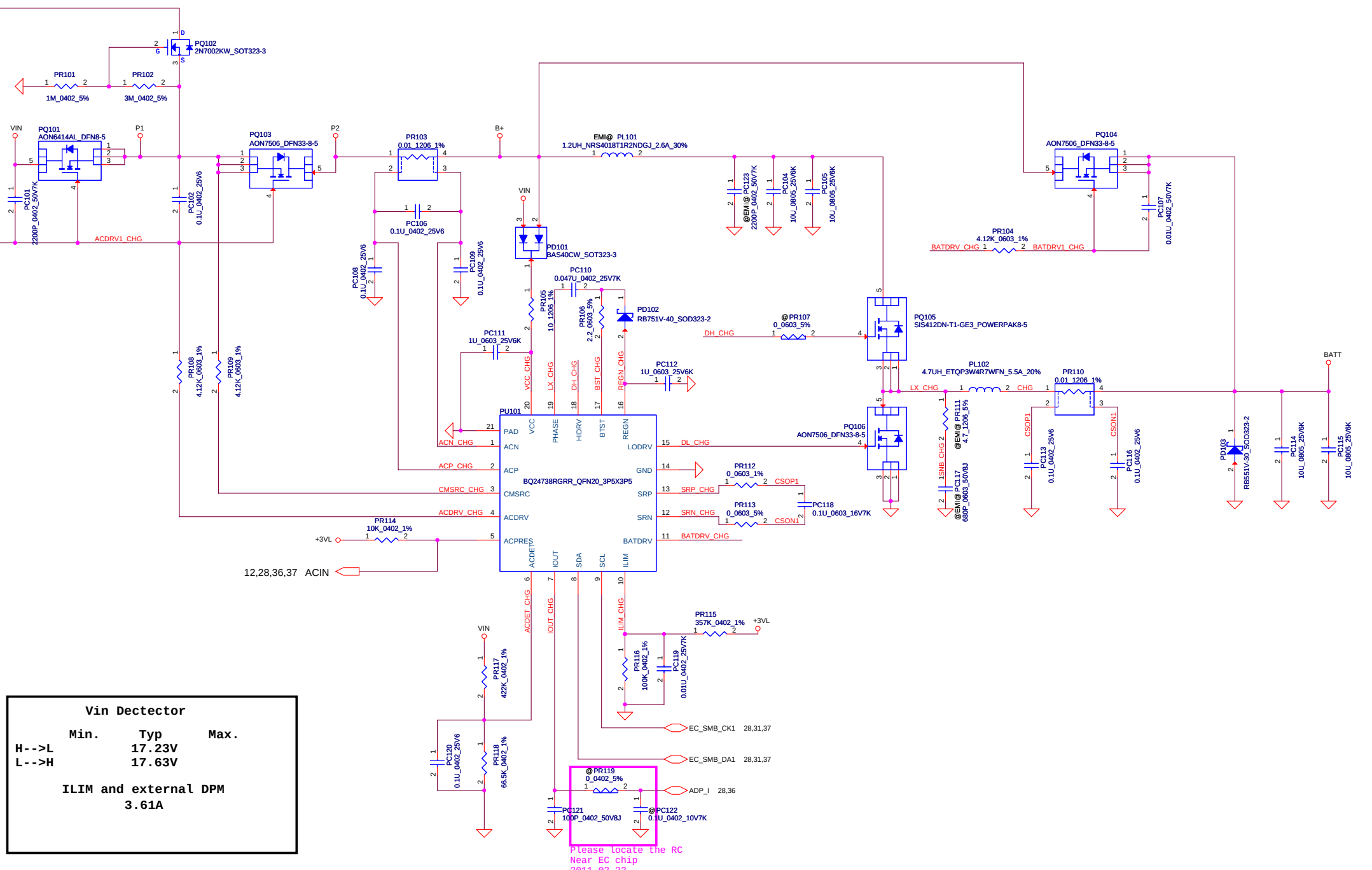
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Issued Date		2012/04/03	Deciphered Date	2014/12/31	Title	
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					Document Number	
					LA-A996P	
					Rev	
					0.1	
					Date: Tuesday, February 25, 2014	
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Issued Date	2013/08/07	Deciphered Date	2016/08/06	Title	DC Conn
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Date: Tuesday, February 25, 2014		Sheet 36 of 47			



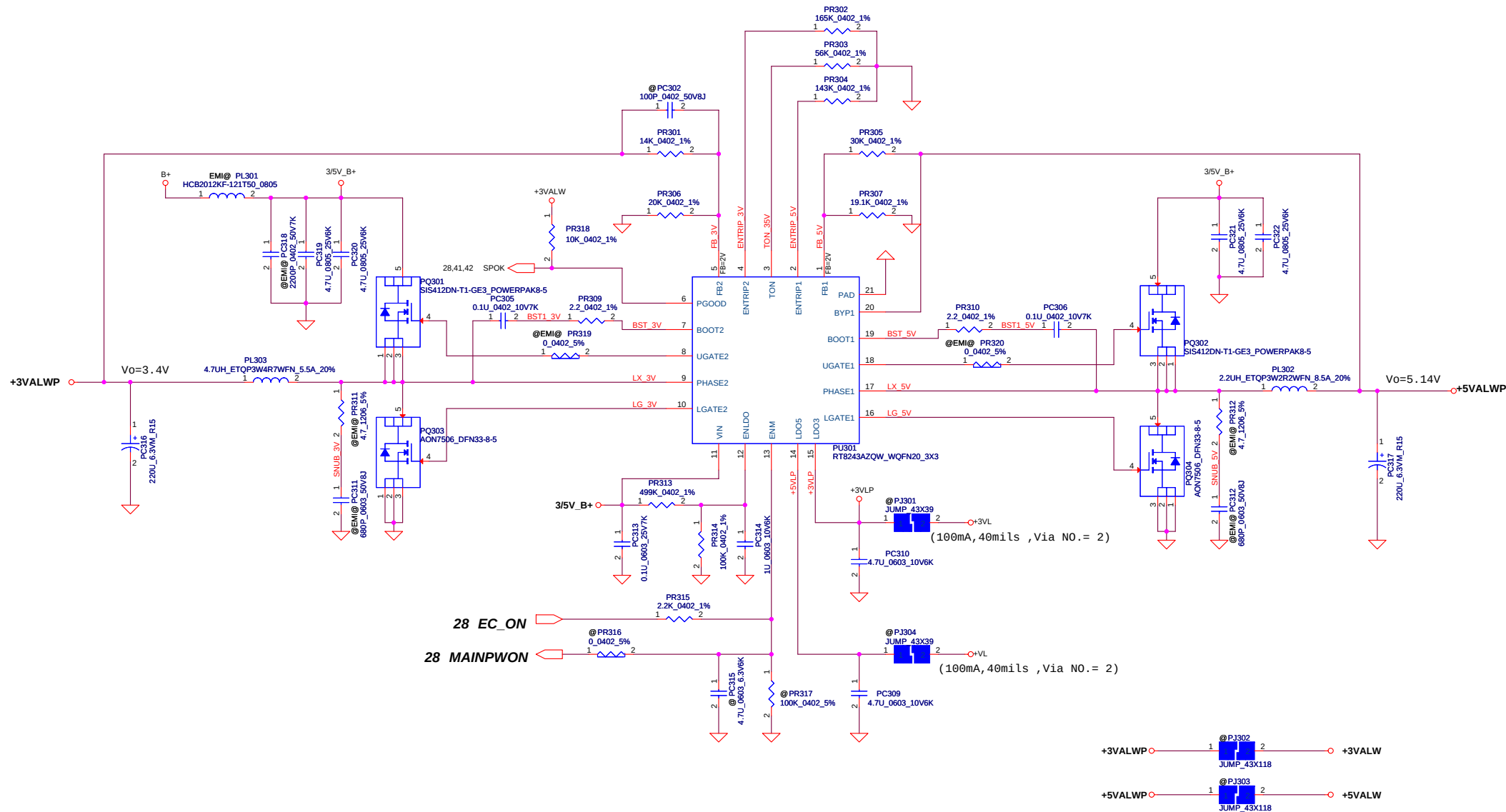
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Issued Date	2013/08/07	Deciphered Date	2016/08/06	Title	BATT Conn
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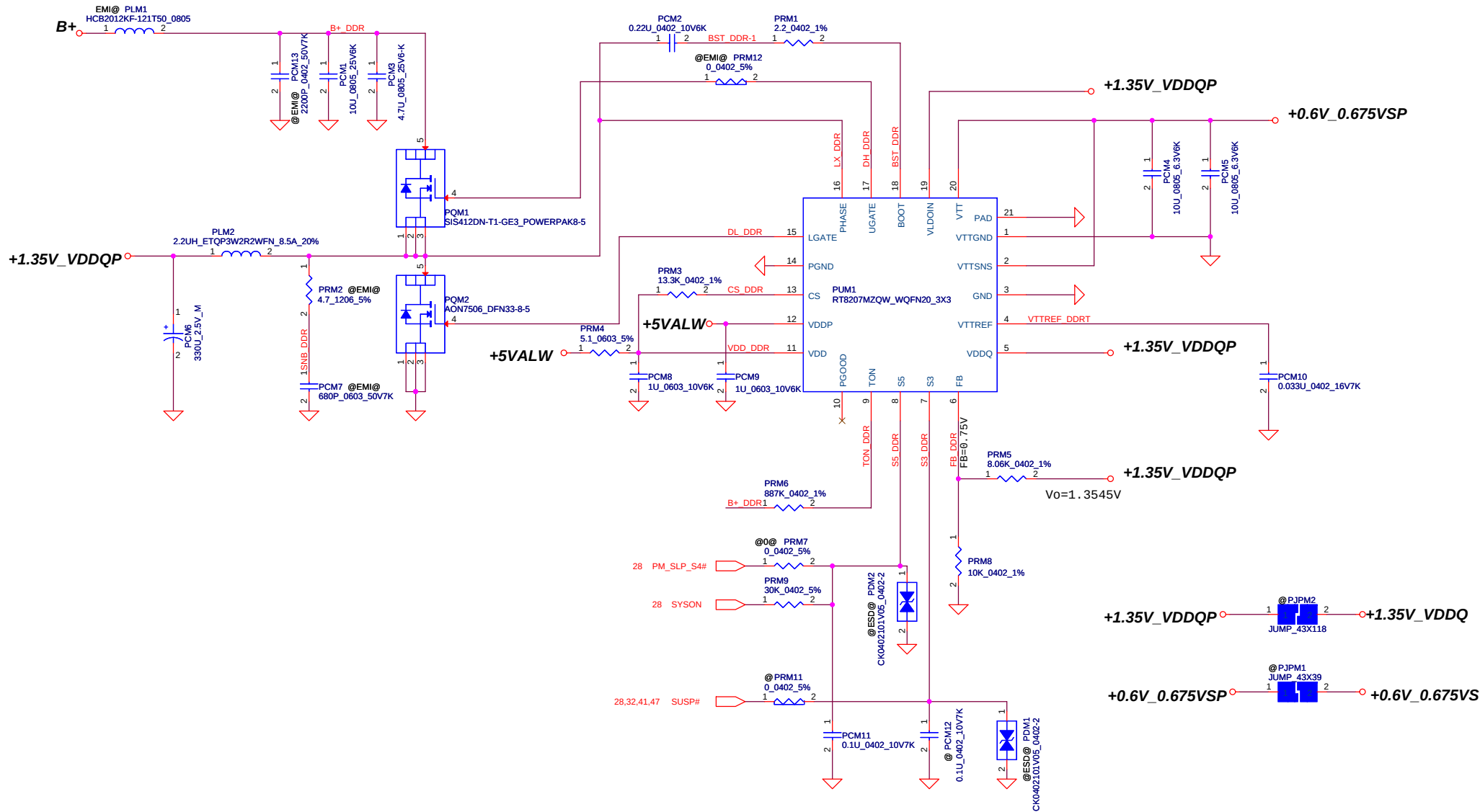
Vin Dectector

	Min.	Typ	Max.
H-->L		17.23V	
L-->H		17.63V	

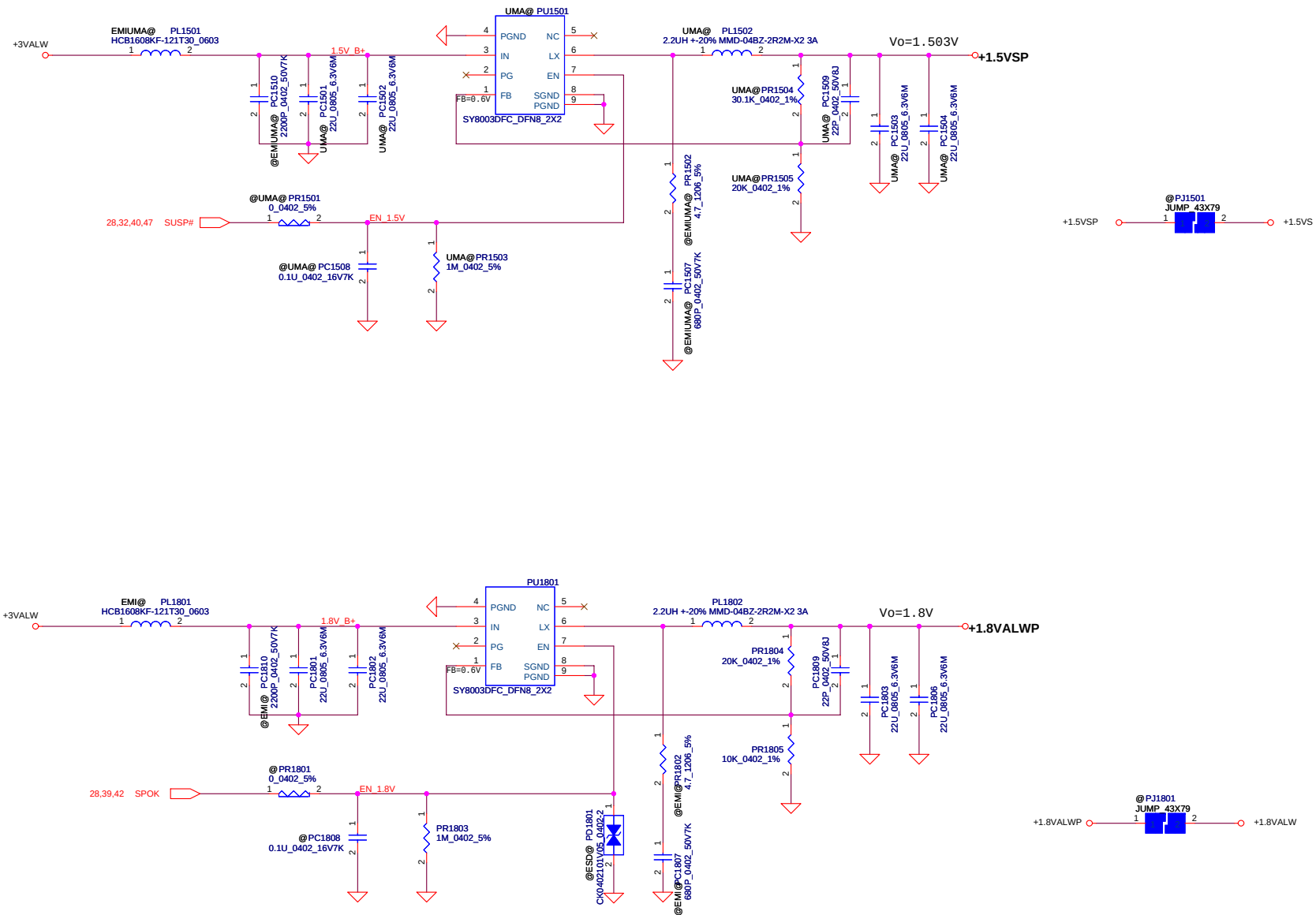
ILIM and external DPM
3.61A



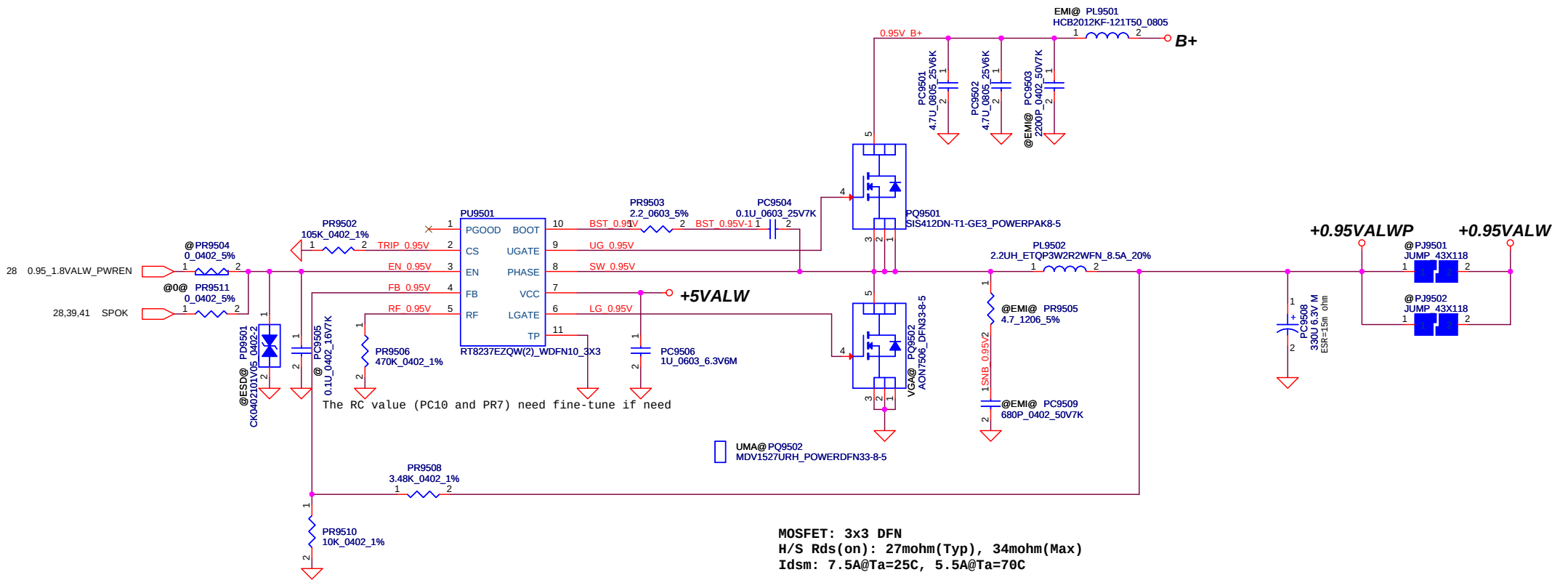
Security Classification	Compal Secret Data			Title		Compal Electronics, Inc.	
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Issued Date	2013/08/07	Deciphered Date	2016/08/06	Title	1.5VS/1.8VALW
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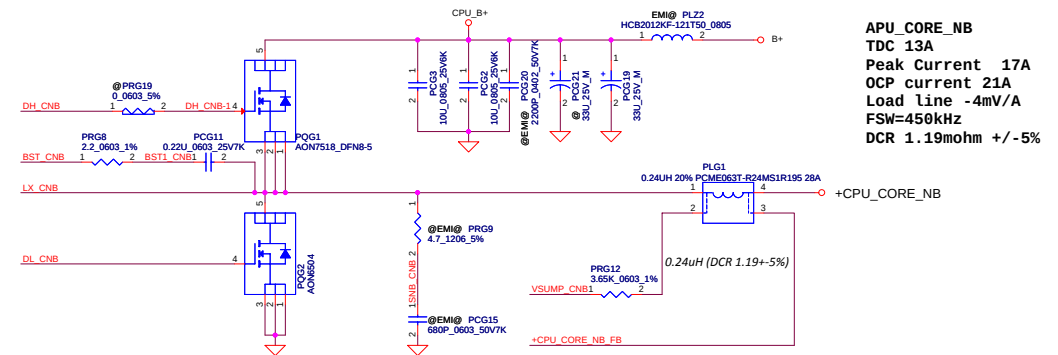
MOSFET: 3x3 DFN
H/S Rds(on): 27mohm(Typ), 34mohm(Max)
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

L/S Rds(on): 9.9mohm(Typ), 13mohm(Max)
Idsm: 13.5A@Ta=25C, 11A@Ta=70C

Choke: 7x7x3
Rdc=15.5mohm +/-15%

Switching Frequency: 290kHz
Imax=8A
OCP~10.977A
VFB=0.704V, Vout=0.949V
MOSFET footprint: SIS412DN

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[illegible]

24V@PC270 10V_0603_25V7K

25W@PQ23 AON7518_DFN8-S

25W@PRZ28 0_0603_5%

UGATE2 1 2

25W@PRZ50 0.22u_0603_25V7K

PC276 1 2

25W@PQ24 AON8504

PHASE2

25W@PRZ31 0.1K_0402_1%

ISEN2 1 2

25W@PRZ37 3.65K_0402_1%

VSUM+ 1 2

0.24uH 20% PCME063T-R24MS1R19S 28A

25W@PRZ30 1_0402_1%

VSUM- 1 2

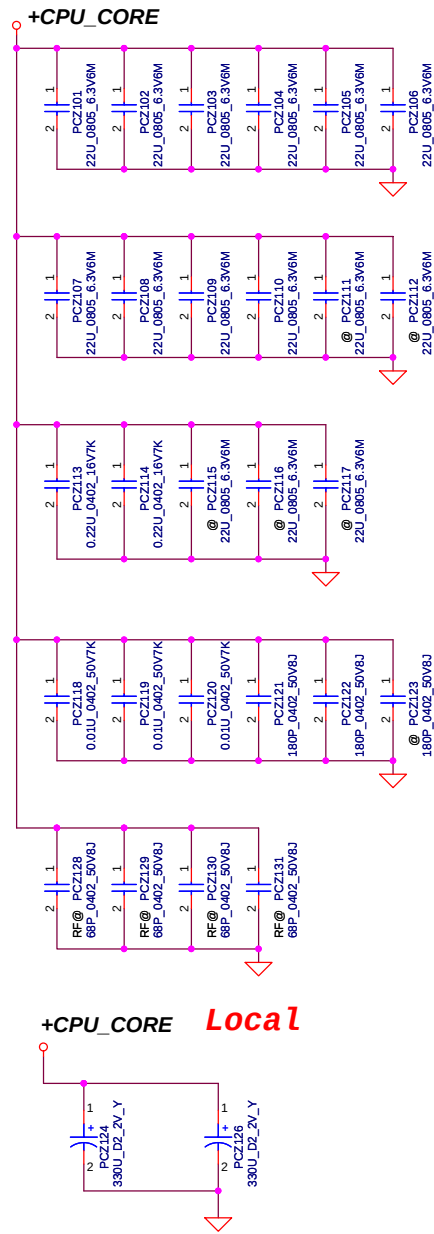
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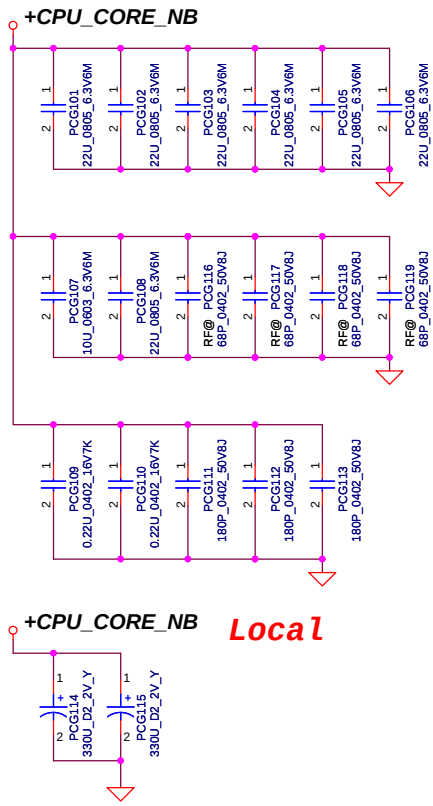
+CPU_CORE

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Issued Date	2012/11/07	Deciphered Date	2012/11/07	Title		
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				Custom	LA-A996P	0.1
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+CPU_CORE

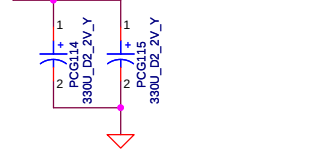


+CPU_CORE_NB

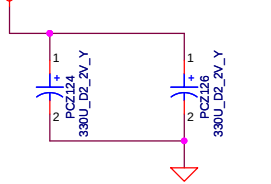


	330uF/9m	22uF/0805	0.22uF/0402	10uF/0603	0.01uF/0402	180pF/0402
+CPU_CORE	2	10	2		3	2
+CPU_CORE_NB	2	7	2	1		3

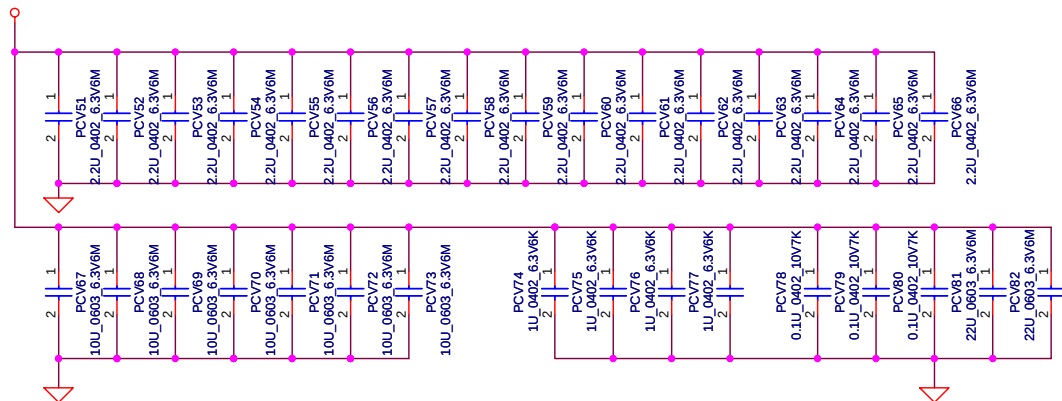
+CPU_CORE_NB Local



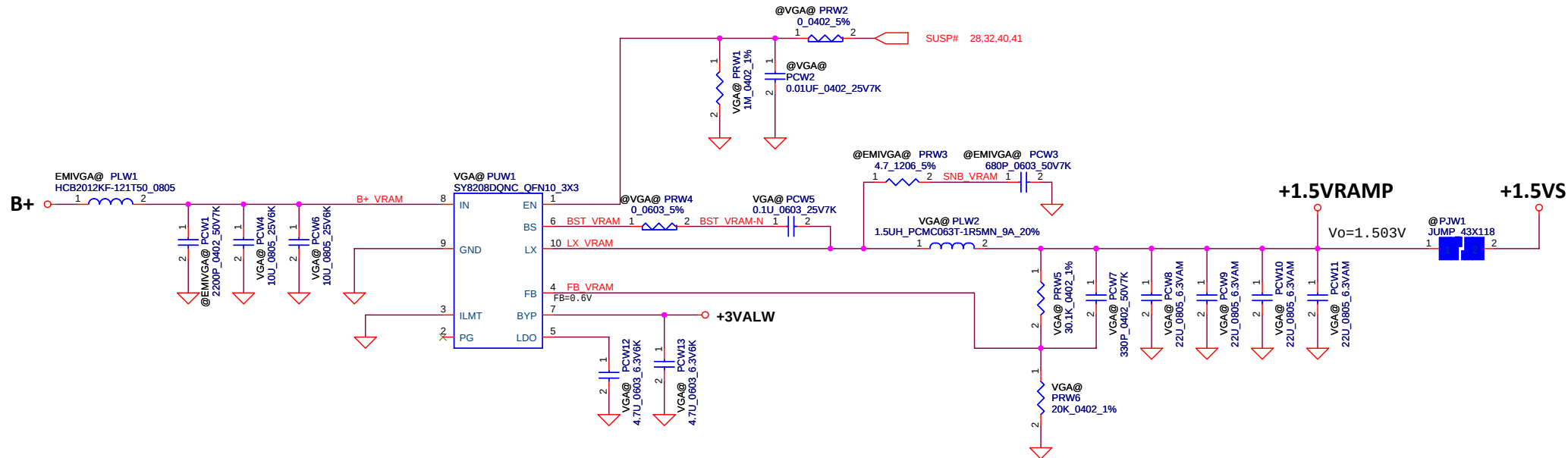
+CPU_CORE Local



+VGA_CORE



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				Date: Tuesday, February 25, 2014	Sheet 47 of 47