For DB build
SOUTH BRIDGE
HM75 QPEG Q0
BD82PPSM
P/N : 6019B0919101

HSF Property:ROHS or Halogen-Free(5L3?)

DB BUILD QUANTITY LIST :

1310A2493104	10 PCS	CR-SG + H-VRAM + GIGA LAN
1310A2493105	72 PCS	CR-SG + S-VRAM + 10/100 LAN
1310A2493106	55 PCS	CR-UMA + GIGA LAN
1310A2493201	137 PCS	POWER /B
1310A2493601	137 PCS	PICK BTN /B
1310A2493701	137 PCS	USB /B

MOTHER BOARD PCB
P/N：6050A2493101

POWER BOARD PCB
P/N：6050A2493201

USB BOARD PCB
P/N：6050A2493601

TOUCHPAD BOARD PCB
P/N：6050A2493701

HARVEY 14

CR / HR UMA / DIS

2011.09.27

HARVEY 14 ID LIST
HURON RIVER UMA : 0X1854
HURON RIVER DIS : 0X1855
CHIEF RIVER UMA : 0X1856
CHIEF RIVER DIS : 0X1857

SUB SYSTEM ID :
HP : 0X103C

BASE SCHEMATIC :
CR-SG + SAMSUNG VRAM + 10/100 LAN + 90W ADAPTER + SUPPORT 27MHZ GREEN CLK + USB2.0 CONN

PAD402	不開鋼板	RTC Rest
PAD4500	不開鋼板	SM_Vrer
PAD2	開	
PAD4		開
PAD400	開	
PAD4700		開
PAD500	開	
PAD508		開
PAD6015	開	
PAD6100		開
PAD6103	開	
PAD6105		開
PAD6110	開	
PAD6150		開
PAD6200	開	
PAD6210		開
PAD6220	開	
PAD6300		開
PAD6301	開	
PAD6310		開
PAD6510	開	
PAD8500		開
PAD6610	開	
PAD6710		開
PAD6750	開	
PAD6970		開
PAD9000	開	
PAD9001		開
PAD9200	開	

GPU VRAM TYPE:

U5 , U6 , U7 , U8

SAMSUNG 1GB C-DIE
PN : 6019B0818601
R2 : NA
R3 : NA
R33 : NA
R61 : NA

HYNIX 1GB D-DIE
PN : 6019B0938301
R2 : MOUNT 0R : 60130B0000ZT
R3 : NA
R33 : NA
R61 : NA

SAMSUNG 512KB
R2 : NA
R3 : MOUNT
R33 : NA
R61 : NA

HYNIX 512MB
R2 : MOUNT
R3 : MOUNT
R33 : NA
R61 : NA

DIS GREEN CLK SUPPORT 27MHZ

U9	SLG3NB300V	P/N : 6019B0941101
C188	MOUNT	0.1UF : 6010A0036403
R126	MOUNT	10R : 60130B10000X
D4400	NA	P/N : 6011A0026803

UMA GREEN CLK

U9	SLG3NB250V	6019B0934701
C188	NA	
R126	NA	
D4400	NA	

DIS ADAPTER 90W

R802	MOUNT 100K : 60130B1040ZT
R769	NA

UMA ADAPTER 65W

R802	NA
R769	MOUNT 100K : 60130B1040ZT

USB 3.0 CONN

CN518 6012B0370301

C2405	MOUNT	0.1UF : 6010A0036403
C2406	MOUNT	0.1UF : 6010A0036403
D2400	NA >> ESD	
L470	MOUNT	P/N : 6014B0177901
L471	MOUNT	P/N : 6014B0177901

USB 2.0 CONN

CN518 6012B0370102

C2405	NA
C2406	NA
D2400	NA >> ESD
L470	NA
L471	NA

BOARD ID	CR-UMA HR-UMA INTEL	CR-SG HR-SG SEYMOUR	CR-SG HR-SG THAMES
ID0-HI R960	0	1	0
ID1-HI R905	0	0	1
ID2-HI R902	0	0	0
ID3-HI R967	0	0	0
ID4-HI R899	0	0	0
ID5-HI R914	1	1	1
ID0-LO R961	1	0	1
ID1-LO R903	1	1	0
ID2-LO R904	1	1	1
ID3-LO R968	1	1	1
ID4-LO R900	1	1	1
ID5-LO R920	0	0	0

ID0 = GPIO40 RXXX = 10K : 60130B1030ZT
ID1 = GPIO41 0 : RXXX NA 1 : RXXX MOUNT
ID2 = GPIO42
ID3 = GPIO43 BOARD_ID5 ONLY FOR WEBCAN USE
ID4 = GPIO9 FOR HD WEB CAM BOARD_ID5 PULL P3V3A
ID5 = GPIO10 FOR VGA WEB CAM BOARD_ID5 PULL GND

M/B ID	DB	SI	PV	MV
R844	MOUNT	NA	MOUNT	NA
R824	MOUNT	MOUNT	NA	NA
R845	NA	MOUNT	NA	MOUNT
R828	NA	NA	MOUNT	MOUNT

RXXX = 10K : 60130B1030ZT NOV JAN MAR

RTL8161FH = 6019B0928101(10/100/1000)
RTL8165EH = 6019B0928301(10/100)

RTL8165EH(10/100) LDO MODE

R408 : MOUNT ----> CHOOSE LDO MODE 0R : 60130B0000ZT
R407 : NA ----> CHOOSE SWITCHING MODE
R413 : NA
C404 : NA
C405 : NA
C406 : NA
C409 : NA
C411 : NA
C415 : NA
C417 : NA
C420 : NA
L400 : NA
U470 : NA
U502 : MOUNT 6016B0008101
U400 : MOUNT 6019B0928301 (10/100 LAN)

RTL8161FH(GIGA-LAN) SWITCHING MODE

R408 : NA ----> CHOOSE LDO MODE
R407 : MOUNT ----> CHOOSE SWITCHING MODE 0R : 60130B1030ZT
R413 : MOUNT 0R_0603 : 60130B00000Z
C404 : MOUNT 4.7UF : 6010B0009904
C405 : MOUNT 0.1UF : 6010A0036403
C406 : MOUNT 0.1UF : 6010A0036403
C409 : MOUNT 0.1UF : 6010A0036403
C411 : MOUNT 0.1UF : 6010A0036403
C415 : MOUNT 0.1UF : 6010A0036403
C417 : MOUNT 4.7UF : 6010B0009904
C420 : MOUNT 0.1UF : 6010A0036403
L400 : MOUNT P/N : 6014B0200401
U470 : MOUNT 6016B0010401
U502 : NA
U400 : MOUNT 6019B0928101 (GIGALAN)

DRAWER		EE		
DESIGN		DATE		
CHECK		POWER		
RESPONSIBLE		DATE		

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
HARVEY 14

SIZE= VER:
FILE NAME:
P/N 6050A2493101 REV

SIZE	CODE	DOC.NUMBER	REV
C	CS	1310xxxxx-0-0	X01

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DATE	CHANGE NO.	REV
AUGUST 2012		X01

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34 PCH-9
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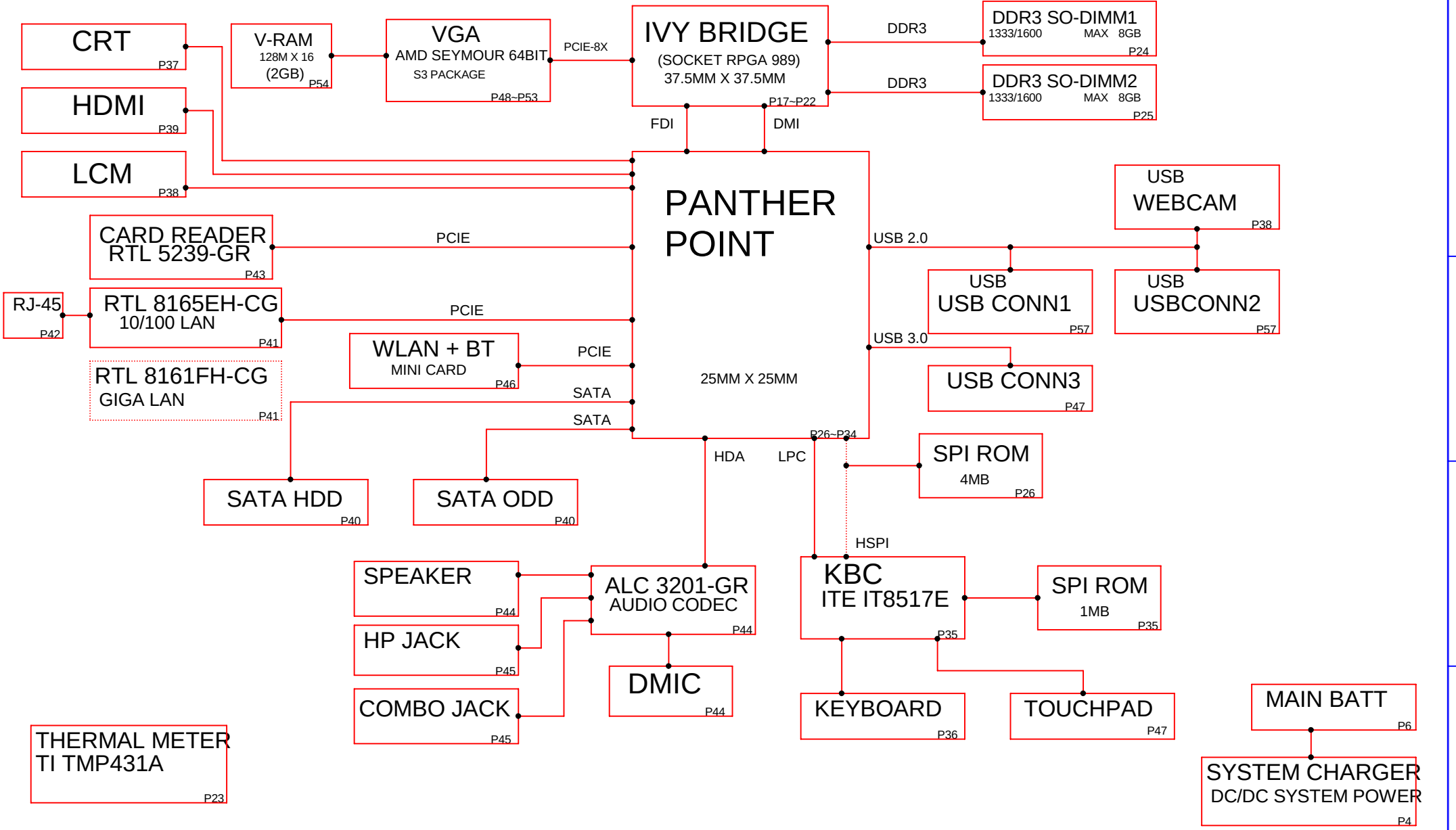
36 KB & LED
37 CRT
38 LCD & WEBCAN
39 HDMI
40 SATA HDD& ODD
41 LAN
42 RJ-45 CONN
43 CARD READER
44 AUDIO CODEC
45 HP & MIC JACK
46 WLAN
47 USB 3.0 CONN
48 SEYMOUR PCI-E INTERFACE
49 SEYMOUR CRT CLK THERMAL
50 SEYMOUR THERMAL SENSOR
51 SEYMOUR POWER
52 SEYMOUR DP-POWER & LVDS
53 SEYMOUR MEMORY INTERFACE
54 VRAM DDR3
55 DGPU POWER EE
56 DGPU POWER
57 USB, POWERBUTTON ,TP DB

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
INDEX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

CHANGE by XXX | DATE 21-OCT-2002 | SHEET 2 of 57

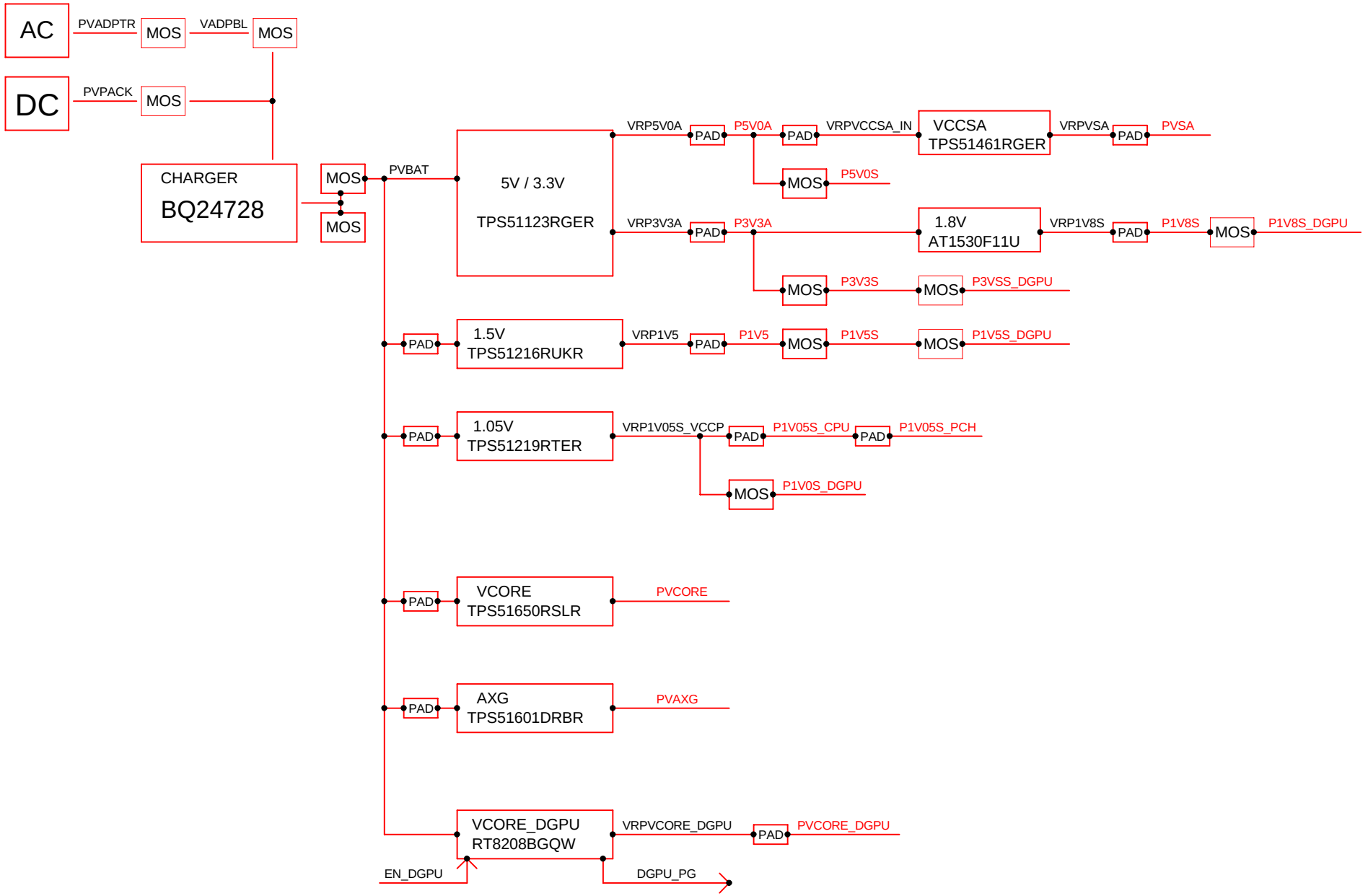


INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

CHANGE by XXX | DATE 21-OCT-2002 | SHEET 3 of 57

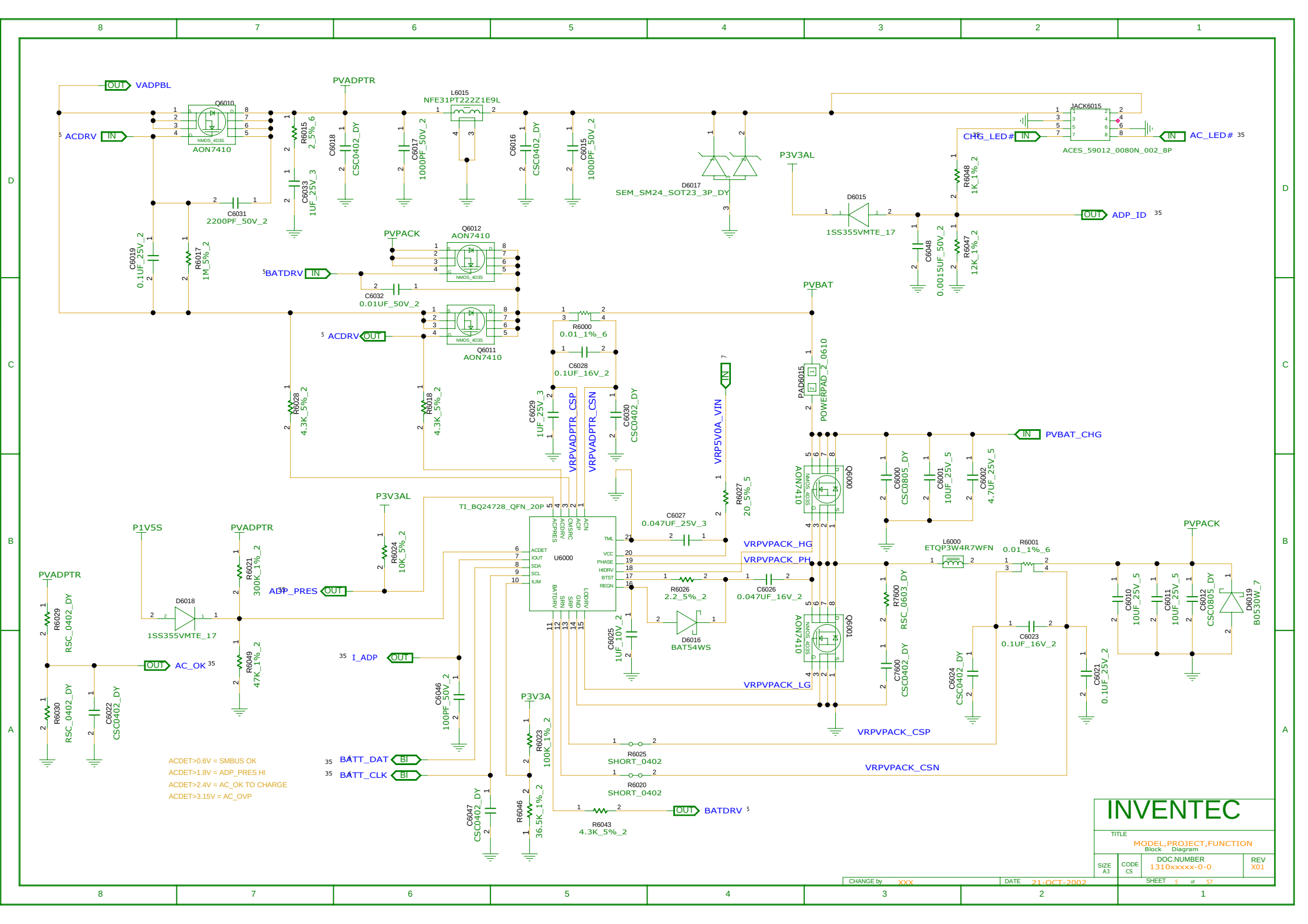


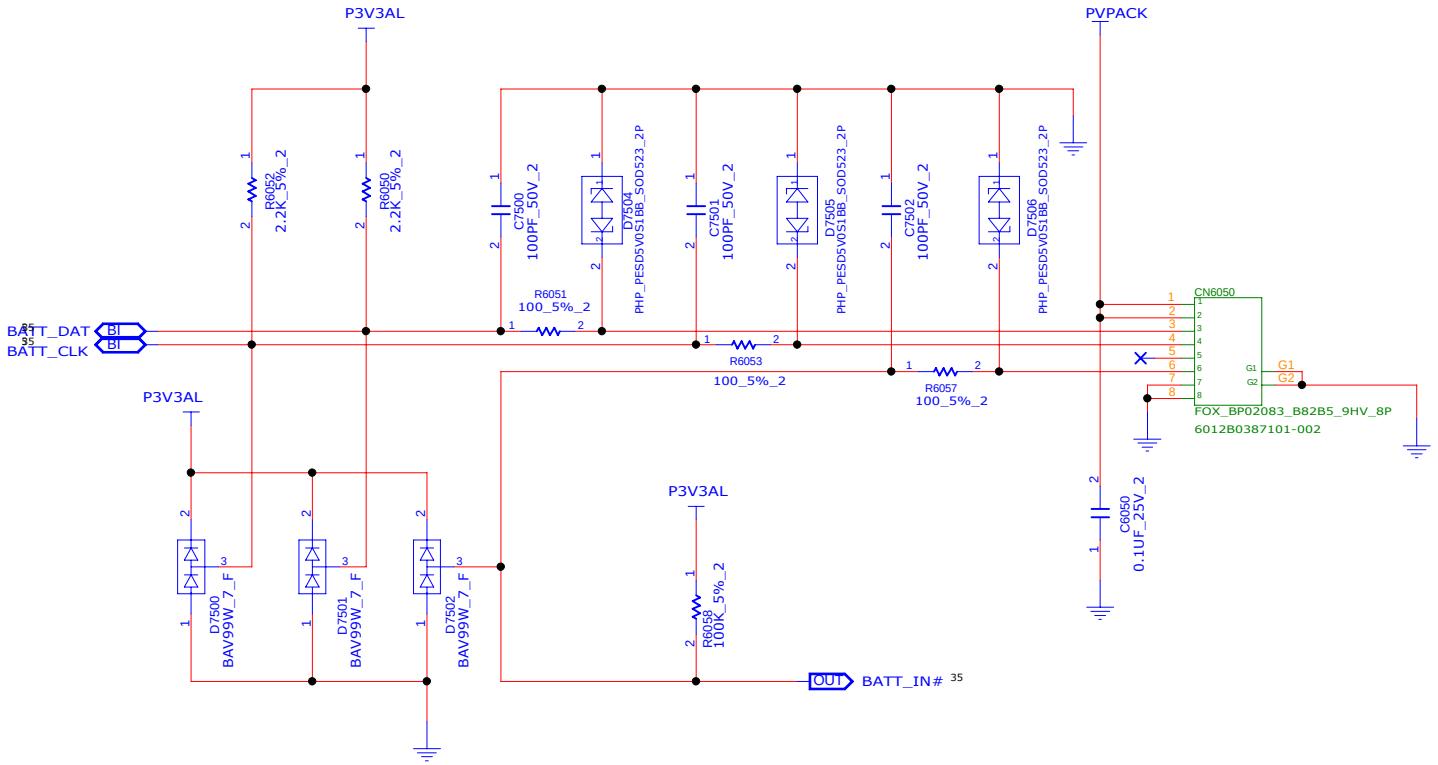
INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
POWER PROCEDURE

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

CHANGE by XXX | DATE 21-OCT-2002 | SHEET 4 of 57


VADPBL
ACDRV
Q6010
AON7410
PVADPTR
L6015
NFE31PT222Z1E9L
R6015 2.5%_6
C6033 1UF_25V_3
C6031 2200PF_50V_2
C6018 CSC0402_DY
C6017 1000PF_50V_2
C6016 CSC0402_DY
C6015 1000PF_50V_2
D6017
SEM_SM24_SOT23_3P_DY
P3V3AL
D6015
1SS355VMTE_17
JACK6015
ACES_59012_0080N_002_8P
CHG_LED#
AC_LED#
R6048 1K_1%_2
R6047 12K_1%_2
C6048 0.0015UF_50V_2
ADP_ID
C6019 0.1UF_25V_2
R6017 1M_5%_2
PVPACK
Q6012
AON7410
BATDRV
C6032 0.01UF_50V_2
Q6011
AON7410
ACDRV
PVBAT
R6000 0.01_1%_6
C6028 0.1UF_16V_2
R6028 4.3K_5%_2
R6018 4.3K_5%_2
C6029 1UF_25V_3
C6030 CSC0402_DY
VRPVADPTR_CSP
VRPVADPTR_CSN
VRP5V0A_VIN
PAD6015
POWERPAD_2_0610
PVBAT_CHG
Q6000
AON7410
C6000 CSC0805_DY
C6001 10UF_25V_5
C6002 4.7UF_25V_5
R6027 20_5%_5
C6027 0.047UF_25V_3
TI_BQ24728_QFN_20P
U6000
VRPVPACK_HG
VRPVPACK_PH
VRPVPACK_LG
VRPVPACK_CSP
VRPVPACK_CSN
R6026 2.2_5%_2
C6026 0.047UF_16V_2
C6025 1UF_10V_2
D6016 BAT54WS
Q6001
AON7410
R7600 RSC_0603_DY
C7600 CSC0402_DY
L6000 ETQP3W4R7WFN
R6001 0.01_1%_6
C6023 0.1UF_16V_2
C6024 CSC0402_DY
C6021 0.1UF_25V_2
C6010 10UF_25V_5
C6011 10UF_25V_5
C6012 CSC0805_DY
D6019 B0530W_7
P1V5S
PVADPTR
R6021 300K_1%_2
R6024 10K_5%_2
ADP_PRES
D6018
1SS355VMTE_17
R6049 47K_1%_2
I_ADP
C6046 100PF_50V_2
P3V3A
R6023 100K_1%_2
R6025 SHORT_0402
R6020 SHORT_0402
R6046 36.5K_1%_2
R6043 4.3K_5%_2
C6047 CSC0402_DY
BATT_DAT
BATT_CLK
BATDRV
PVADPTR
R6029 RSC_0402_DY
R6030 RSC_0402_DY
C6022 CSC0402_DY
AC_OK
ACDET>0.6V = SMBUS OK
ACDET>1.8V = ADP_PRES HI
ACDET>2.4V = AC_OK TO CHARGE
ACDET>3.15V = AC_OVP
INVENTEC
TITLE
MODEL,PROJECT,FUNCTION
Block Diagram
SIZE A3
CODE CS
DOC.NUMBER 1310xxxxx-0-0
REV X01
CHANGE by XXX
DATE 21-OCT-2002
SHEET 5 of 57

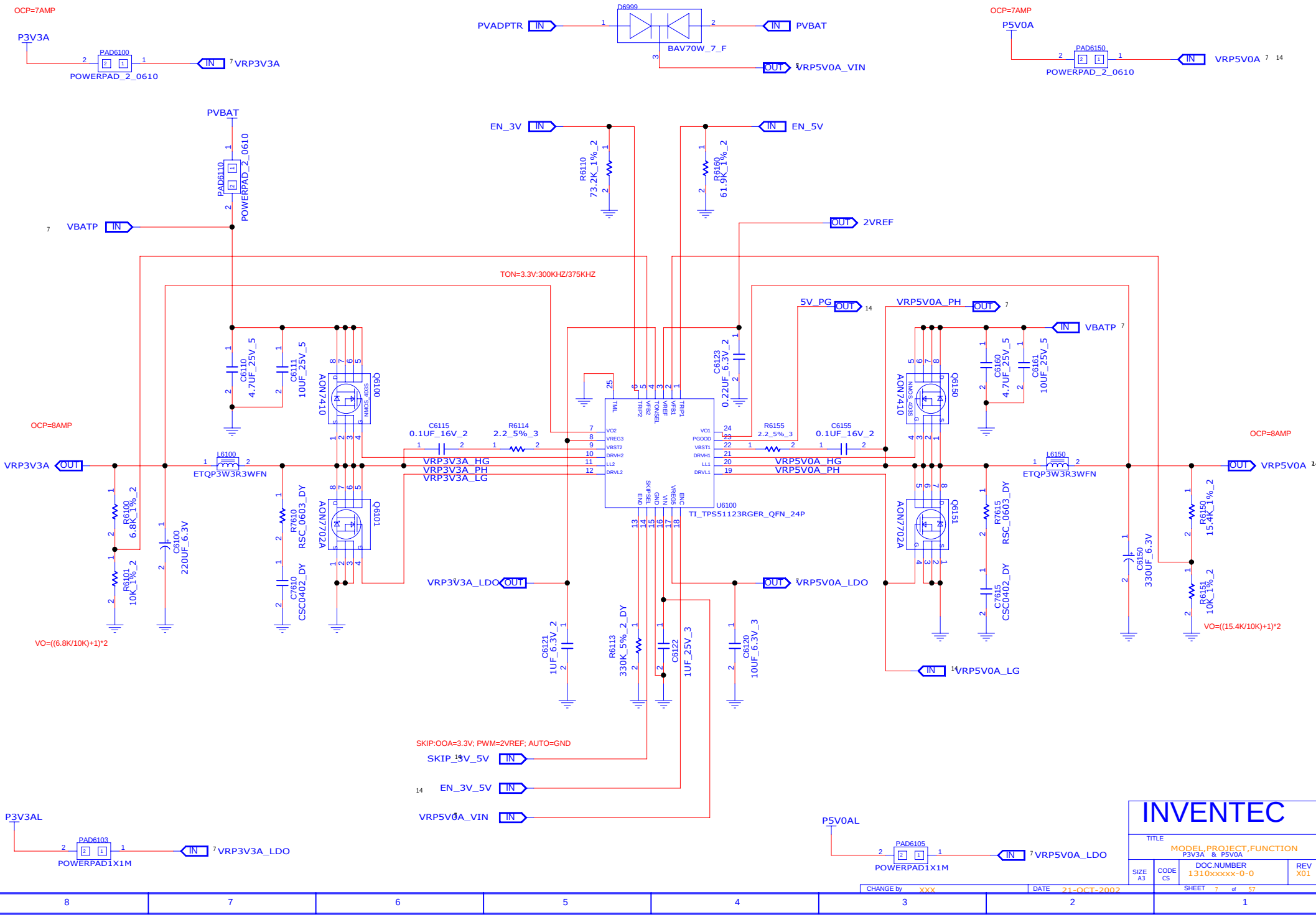


INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
SELETOR

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

CHANGE by XXX | DATE 21-OCT-2002 | SHEET 6 of 57


OCP=7AMP
P3V3A
PAD6100
POWERPAD_2_0610
VRP3V3A
PVADPTR
D6999
BAV70W_7_F
PVBAT
VRP5V0A_VIN
OCP=7AMP
P5V0A
PAD6150
VRP5V0A
PVBAT
PAD6110
POWERPAD_2_0610
EN_3V
EN_5V
R6110
73.2K_1%_2
R6160
61.9K_1%_2
2VREF
VBATP
TON=3.3V:300KHZ/375KHZ
5V_PG
VRP5V0A_PH
C6110
4.7UF_25V_5
C6111
10UF_25V_5
Q6100
AON7410
C6115
0.1UF_16V_2
R6114
2.2_5%_3
C6123
0.22UF_6.3V_2
R6155
2.2_5%_3
C6155
0.1UF_16V_2
Q6150
C6160
4.7UF_25V_5
C6161
10UF_25V_5
OCP=8AMP
VRP3V3A
L6100
ETQP3W3R3WFN
VRP3V3A_HG
VRP3V3A_PH
VRP3V3A_LG
U6100
TI_TPS51123RGER_QFN_24P
VRP5V0A_HG
VRP5V0A_PH
L6150
ETQP3W3R3WFN
OCP=8AMP
VRP5V0A
R6100
6.8K_1%_2
C6100
220UF_6.3V
R6101
10K_1%_2
Q6101
AON7702A
R7610
RSC_0603_DY
C7610
CSC0402_DY
Q6151
AON7702A
R7615
RSC_0603_DY
C7615
CSC0402_DY
C6150
330UF_6.3V
R6150
15.4K_1%_2
R6151
10K_1%_2
VO=((6.8K/10K)+1)*2
VO=((15.4K/10K)+1)*2
VRP3V3A_LDO
VRP5V0A_LDO
C6121
1UF_6.3V_2
R6113
330K_5%_2_DY
C6122
1UF_25V_3
C6120
10UF_6.3V_3
VRP5V0A_LG
SKIP:OOA=3.3V; PWM=2VREF; AUTO=GND
SKIP_3V_5V
EN_3V_5V
VRP5V0A_VIN
P3V3AL
PAD6103
POWERPAD1X1M
VRP3V3A_LDO
P5V0AL
PAD6105
POWERPAD1X1M
VRP5V0A_LDO
INVENTEC
TITLE
MODEL,PROJECT,FUNCTION
P3V3A & P5V0A
SIZE A3
CODE CS
DOC.NUMBER 1310xxxxx-0-0
REV X01
CHANGE by XXX
DATE 21-OCT-2002
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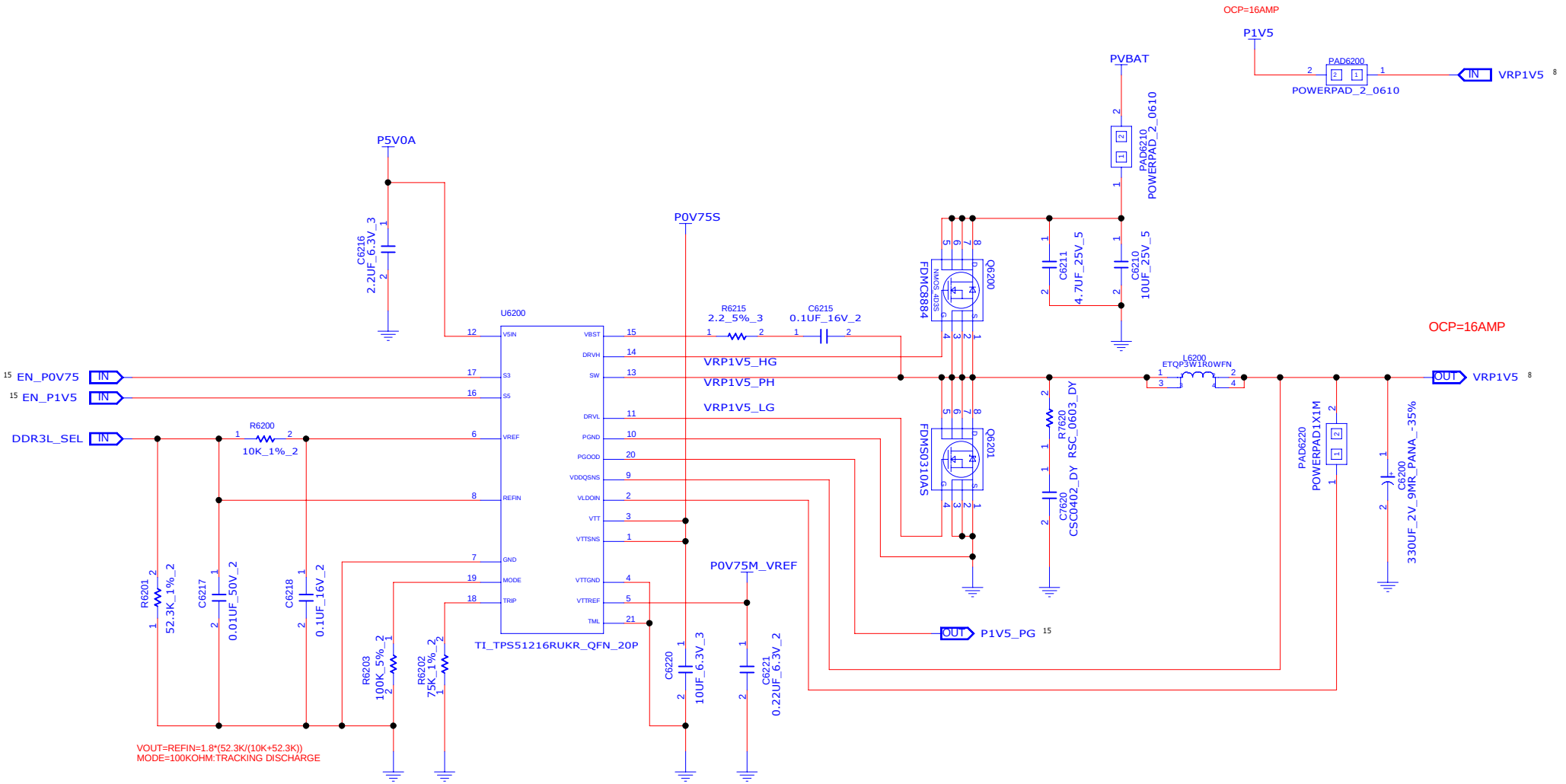


Table 1. S3/S5 Power State Control

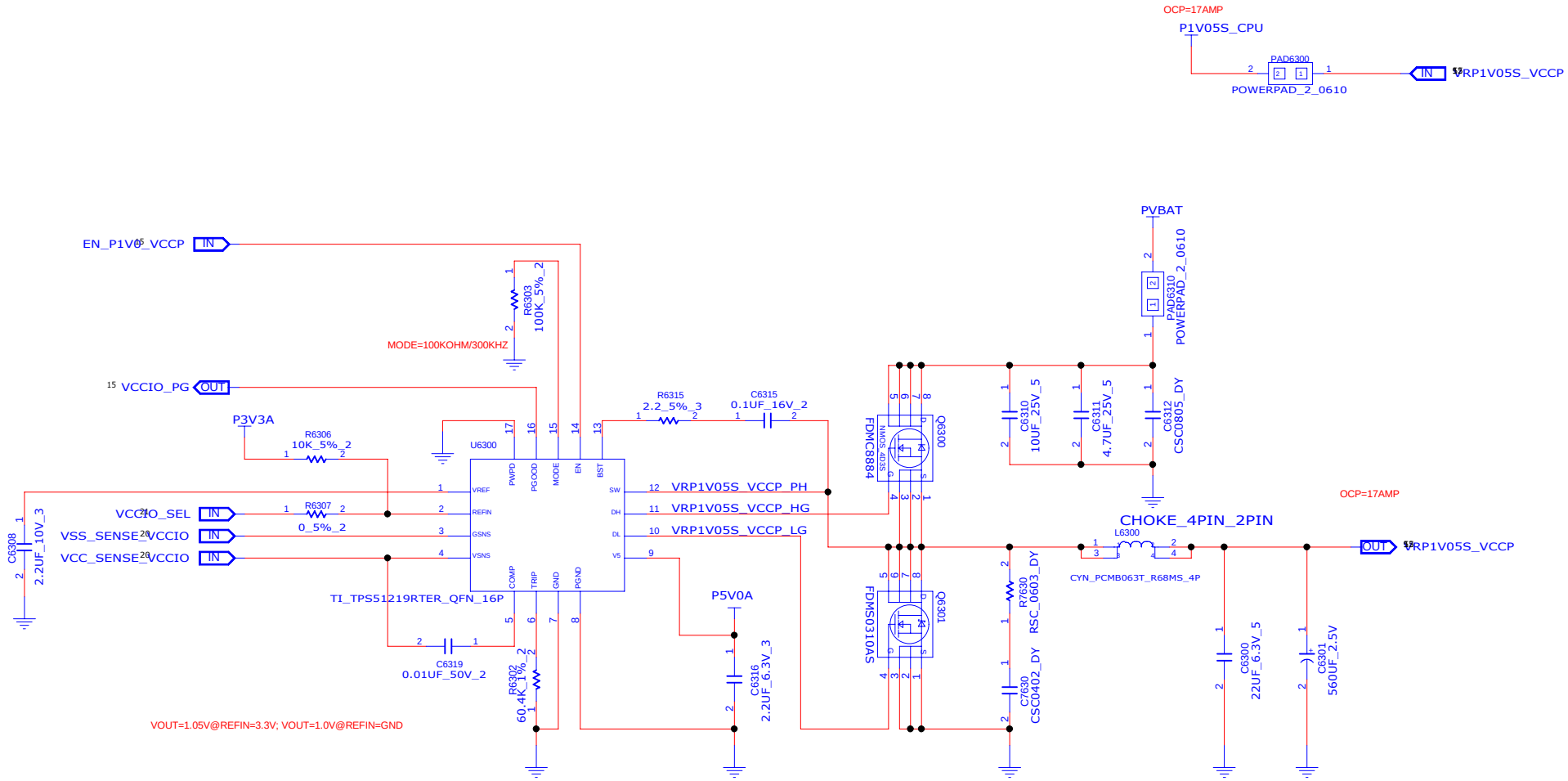
STATE	S3	S5	VREF	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF(High-Z)
S4/S5	LO	LO	OFF	OFF(Discharge)	OFF(Discharge)	OFF(Discharge)

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
P1V5

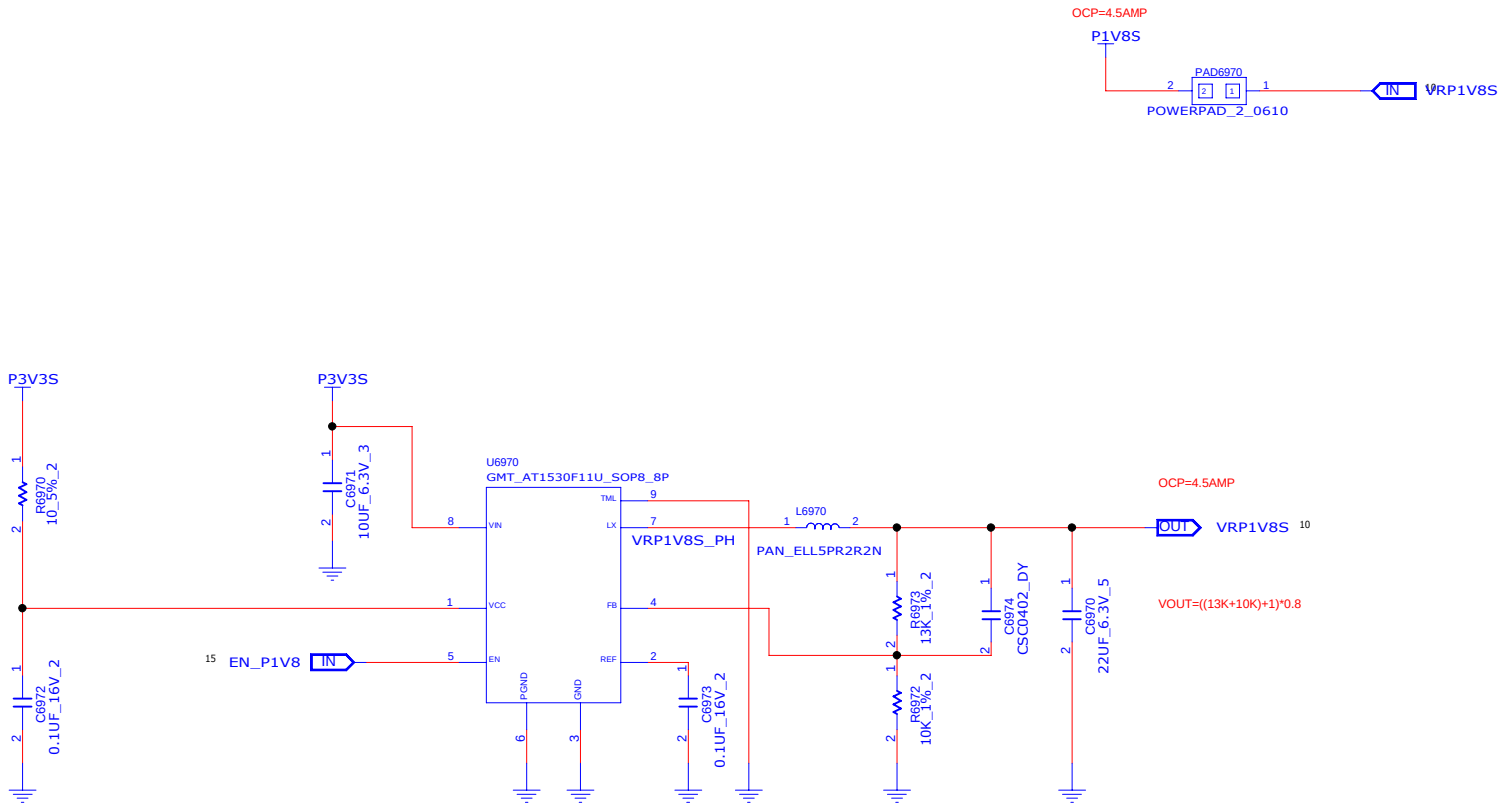
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

CHANGE by XXX | DATE 21-OCT-2002 | SHEET 8 of 57

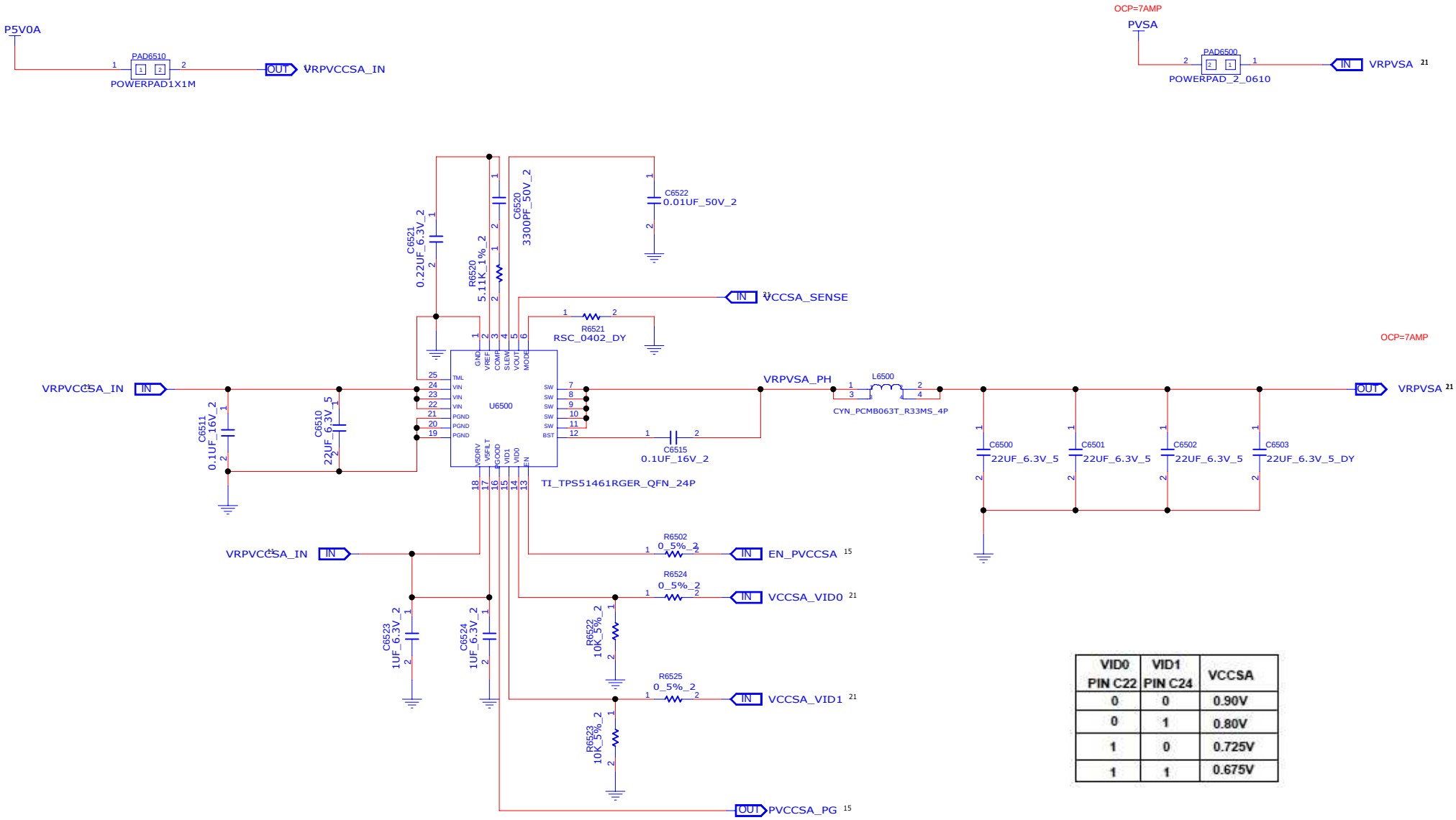


INVENTEC

TITLE: MODEL,PROJECT,FUNCTION — P1V05S_CPU			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX	DATE 21-OCT-2002	SHEET 9 of 57	



INVENTEC			
TITLE: MODEL,PROJECT,FUNCTION P1V8S			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX	DATE 21-OCT-2002	SHEET 10 of 57	



VID0 PIN C22	VID1 PIN C24	VCCSA
0	0	0.90V
0	1	0.80V
1	0	0.725V
1	1	0.675V

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
PVSA

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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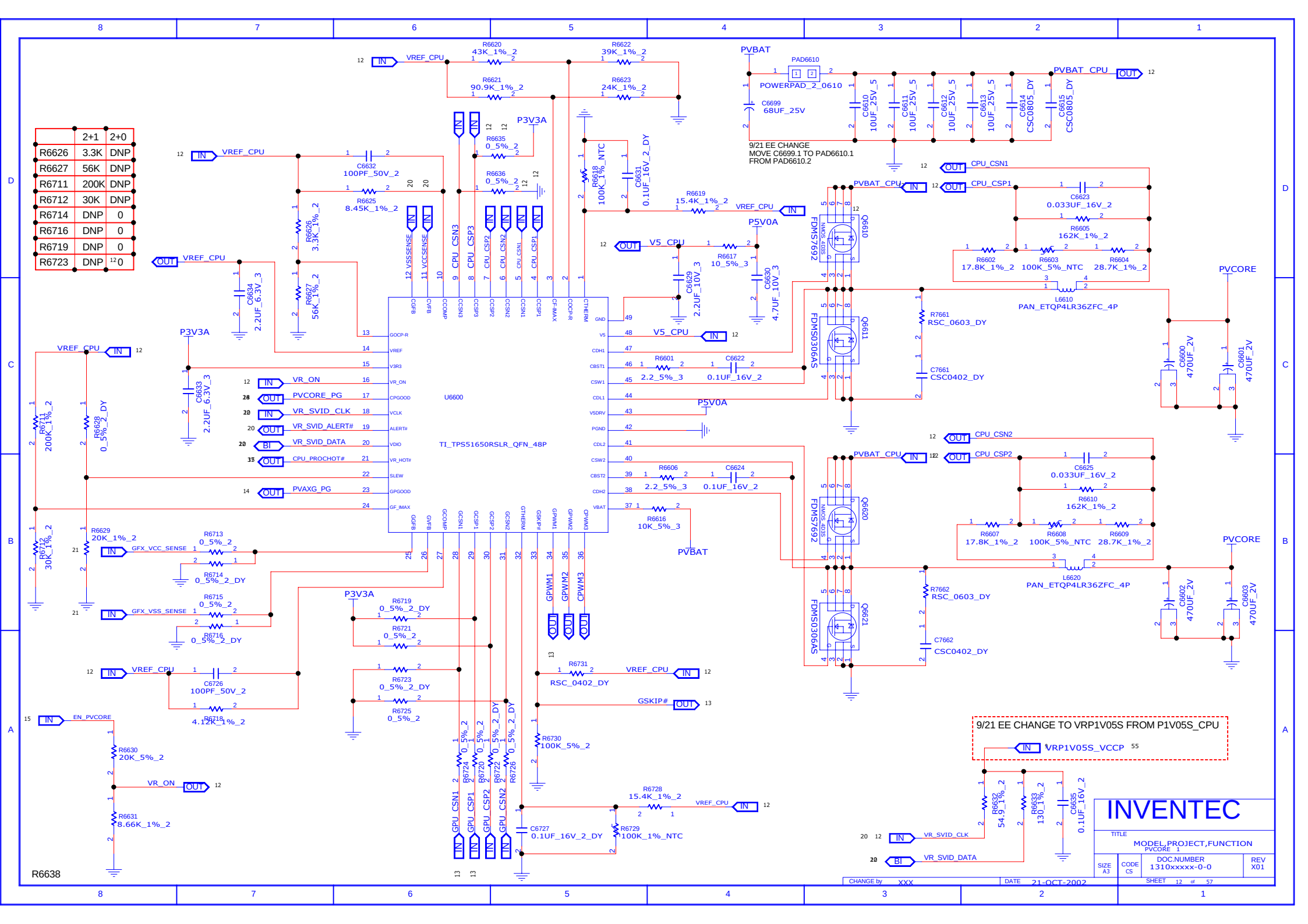
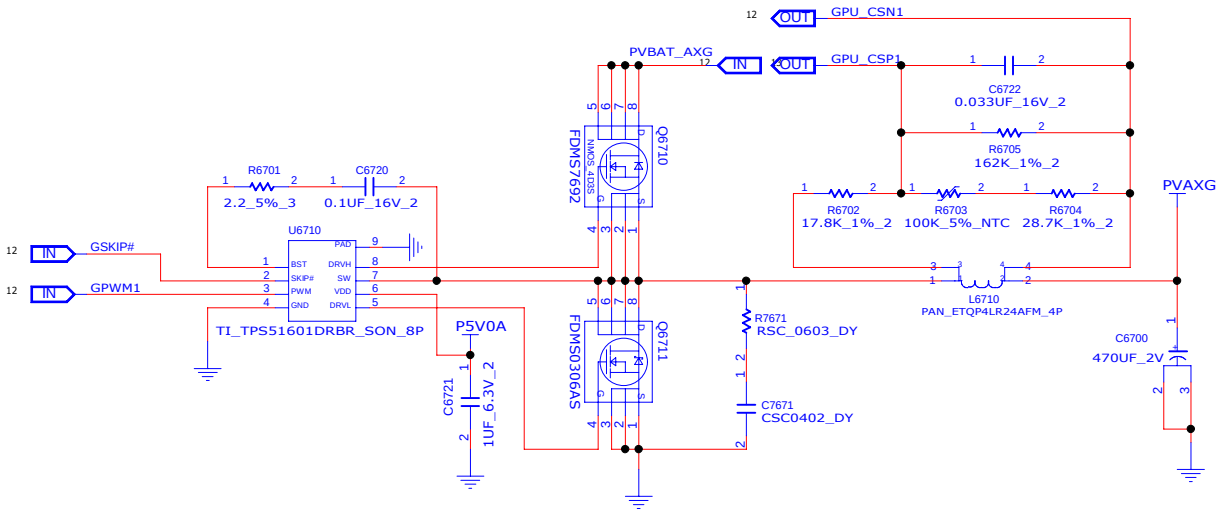
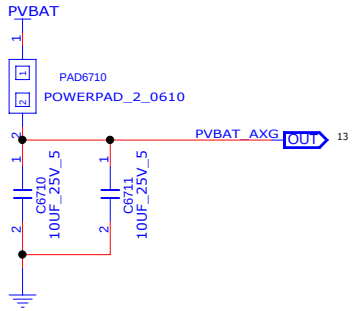


	2+1	2+0
R6626	3.3K	DNP
R6627	56K	DNP
R6711	200K	DNP
R6712	30K	DNP
R6714	DNP	0
R6716	DNP	0
R6719	DNP	0
R6723	DNP	0



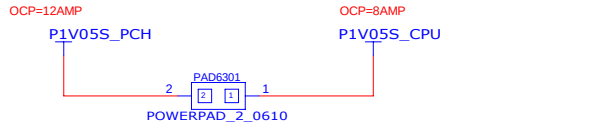


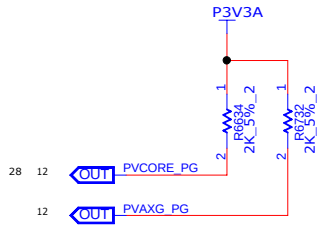
INVENTEC

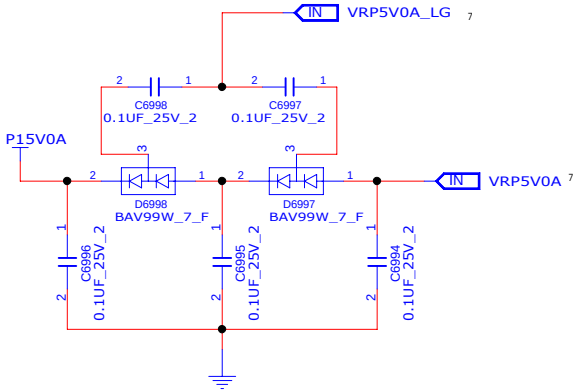
TITLE
MODEL,PROJECT,FUNCTION
PVCORE 2

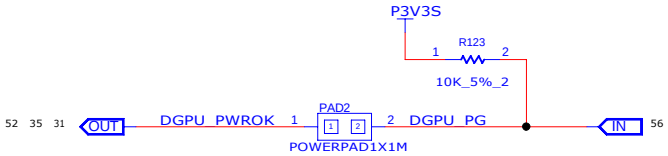
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

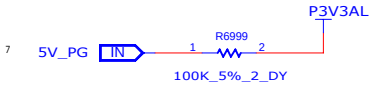
CHANGE by XXX | DATE 21-OCT-2002 | SHEET 13 of 57

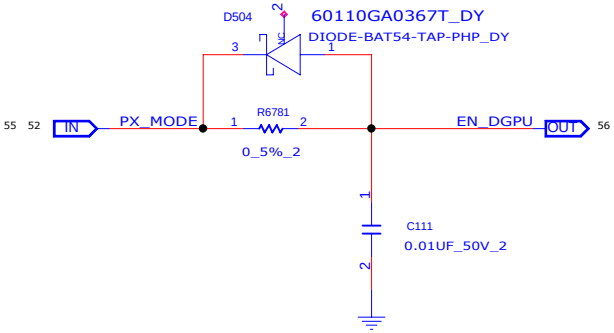




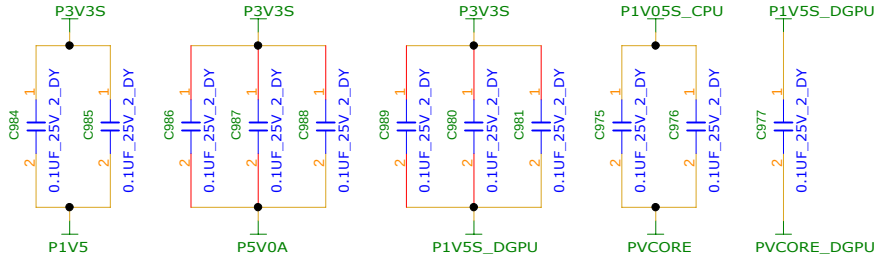


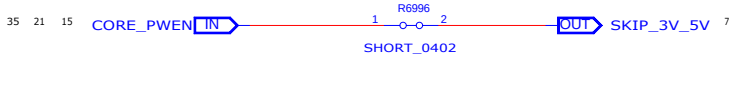


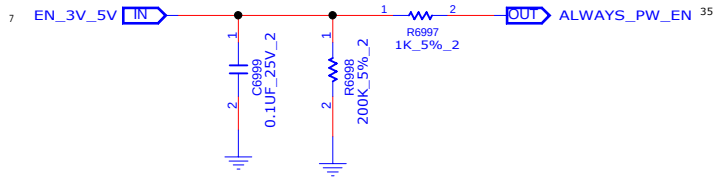


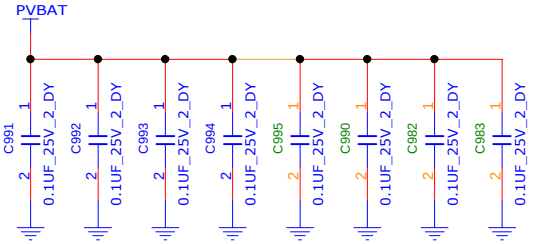


EMI Part



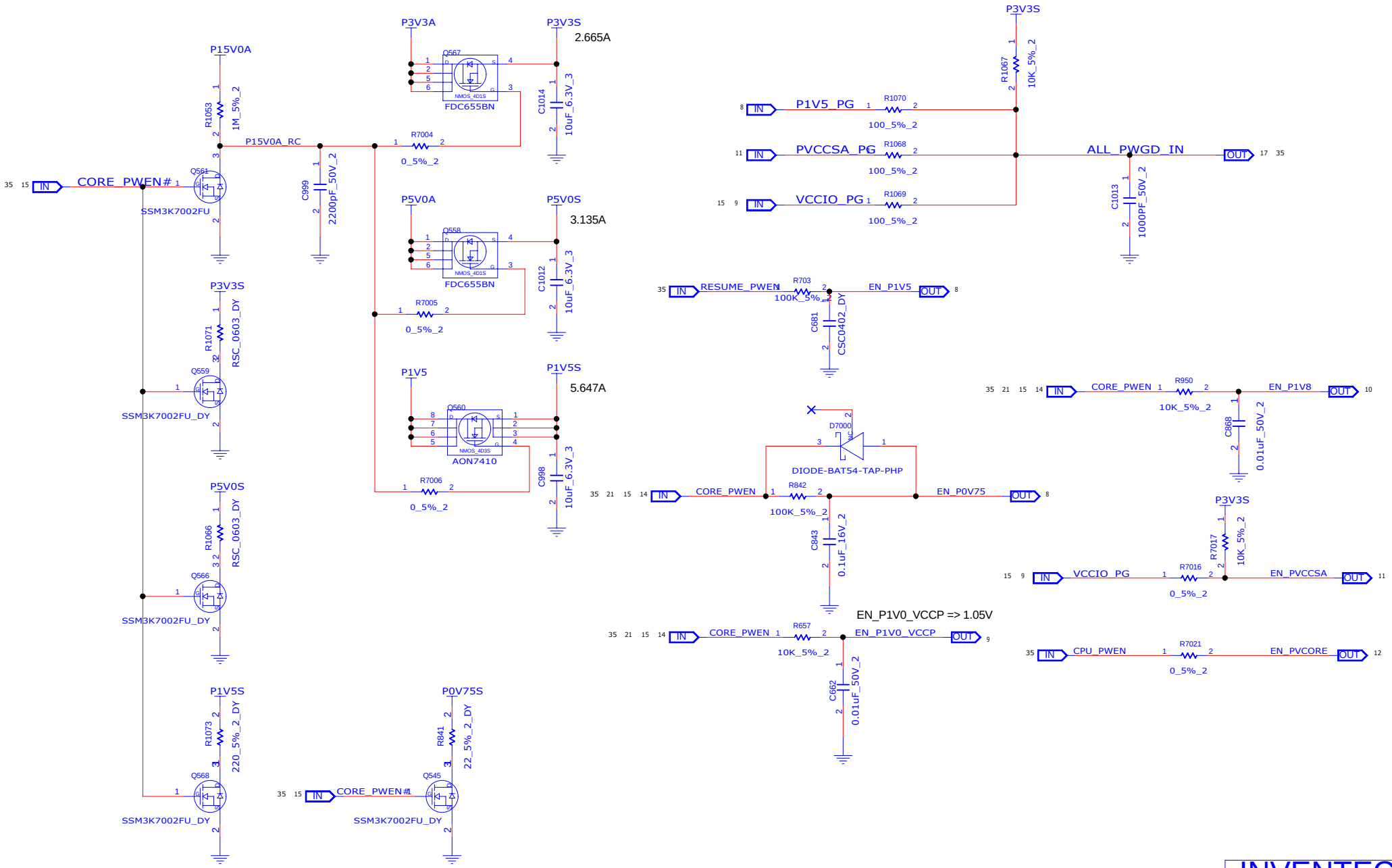






INVENTEC

TITLE: MODEL,PROJECT,FUNCTION POWER TO EE PORT & EMI PART			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX	DATE 21-OCT-2002	SHEET 14 of 57	



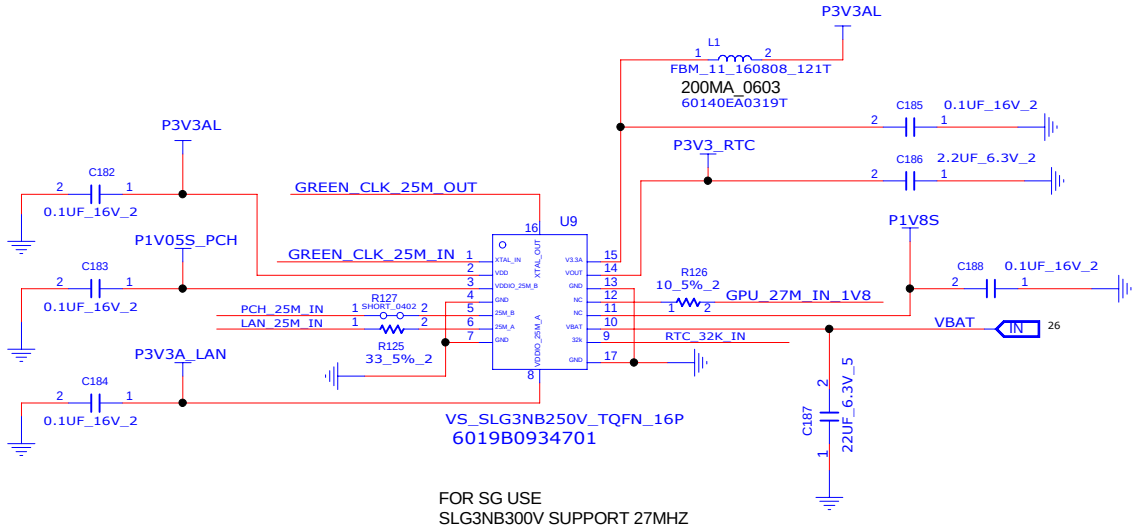
INVENTEC

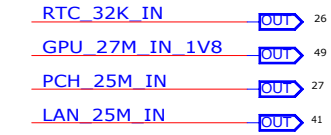
TITLE: MODEL,PROJECT,FUNCTION
P5V0S & P3V3S

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

CHANGE by XXX | DATE 21-OCT-2002 | SHEET 15 of 57

Green CLK





TYPICAL RTC_32K_IN TRACE <= 6
MAX. LENGTH <= 24

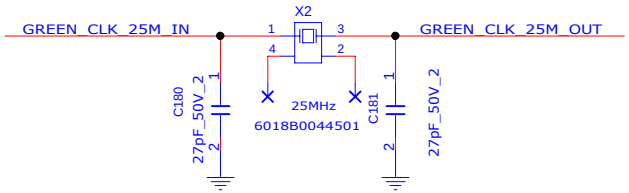
TYPICAL GPU_27M_IN TRACE <= 8
MAX. LENGTH <= 12

TYPICAL LAN_25M_IN TRACE <= 8
MAX. LENGTH <= 12

TYPICAL LAN_25M_IN TRACE <= 8
MAX. LENGTH <= 12

FOR SG USE
SLG3NB300V SUPPORT 27MHZ
P/N : 6019B0941101

FOR UMA USE
SLG3NB250V
P/N : 6019B0934701



FOR UMA
U9 : 6019B0934701
R126 : NA
C188 : NA

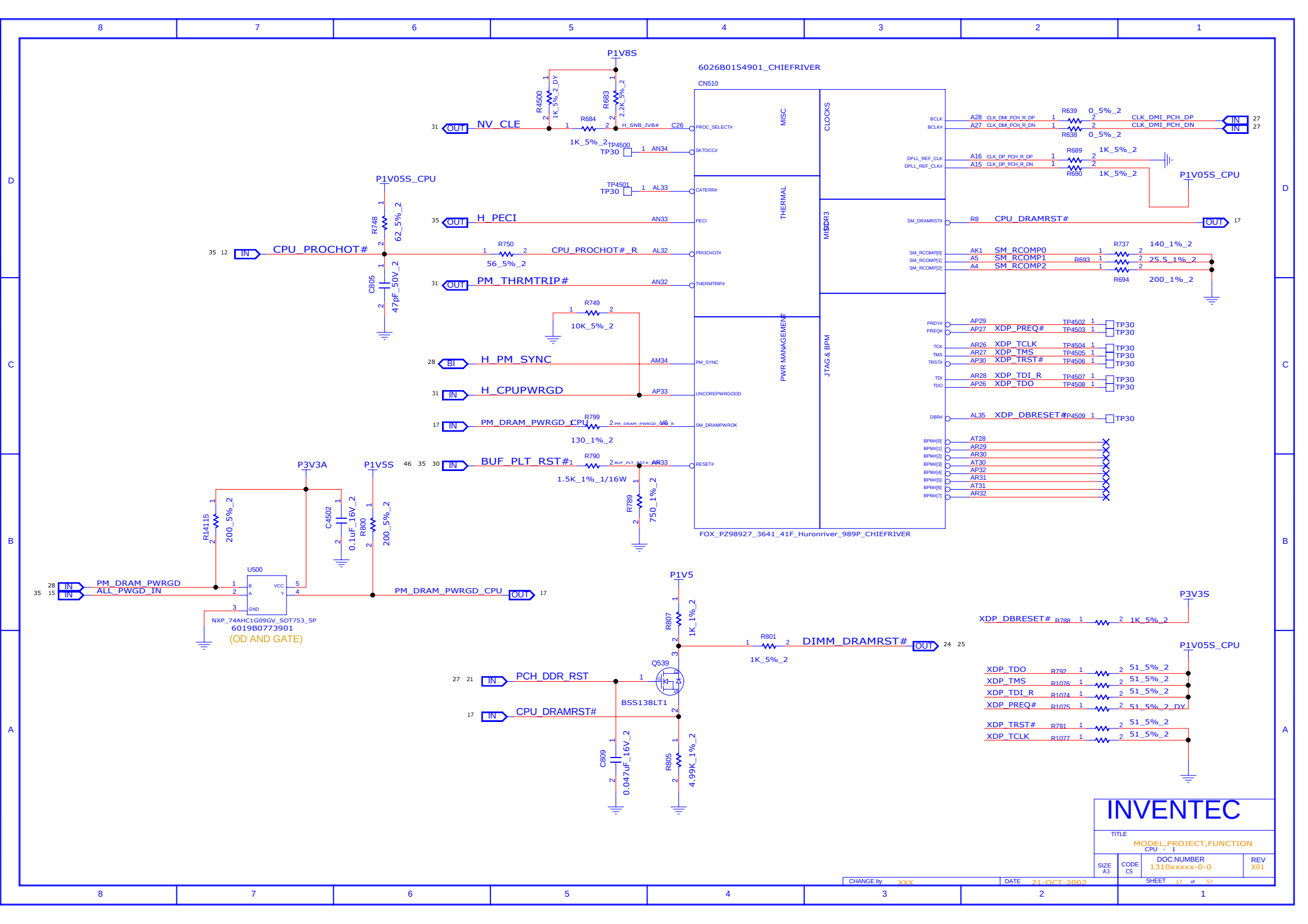
FOR SG
U9 : SLG3NB300V P/N APPLY
R126 : MOUNT
C188 : MOUNT

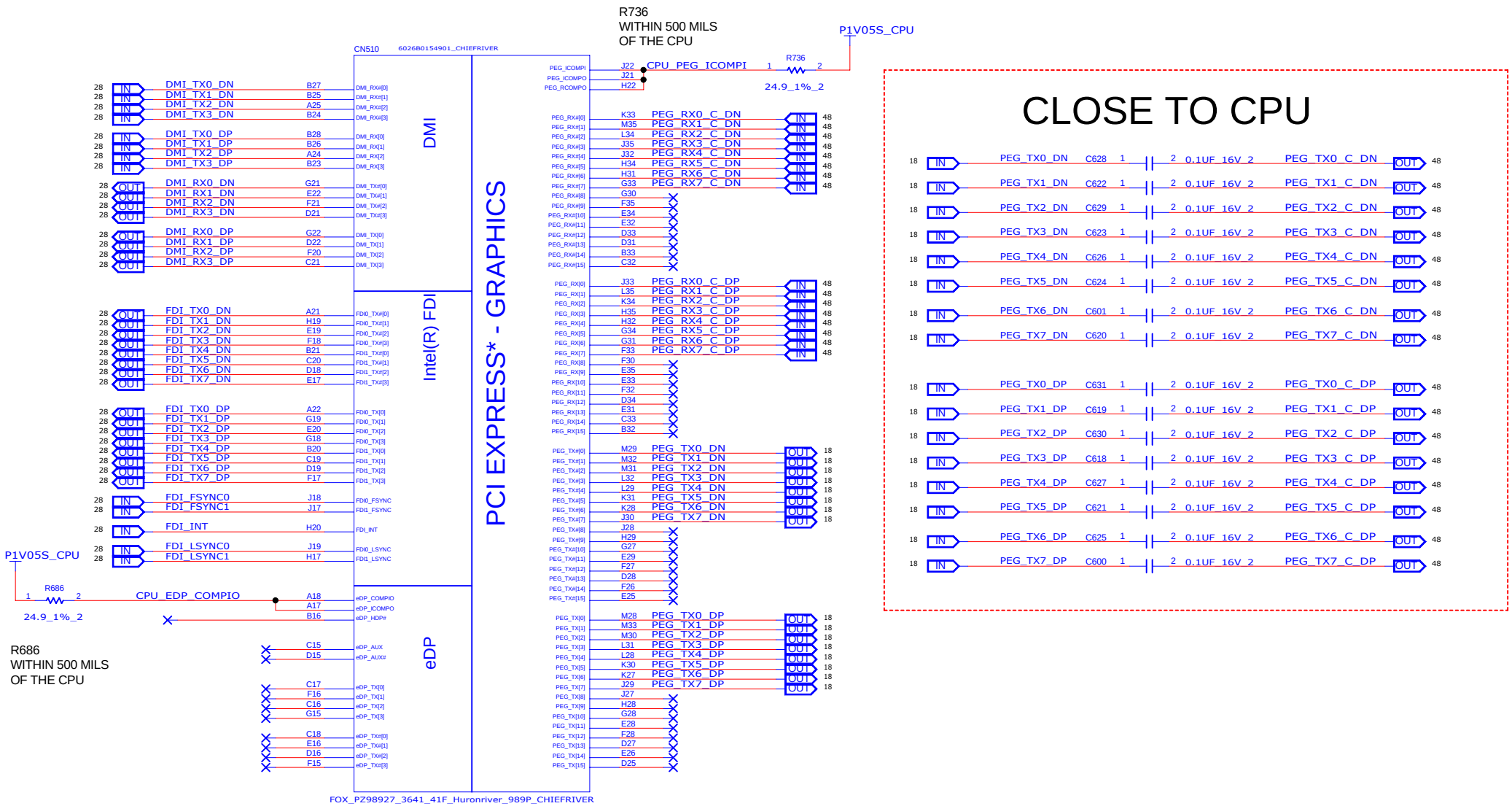
IF USE U9 (SLG3NB250V)

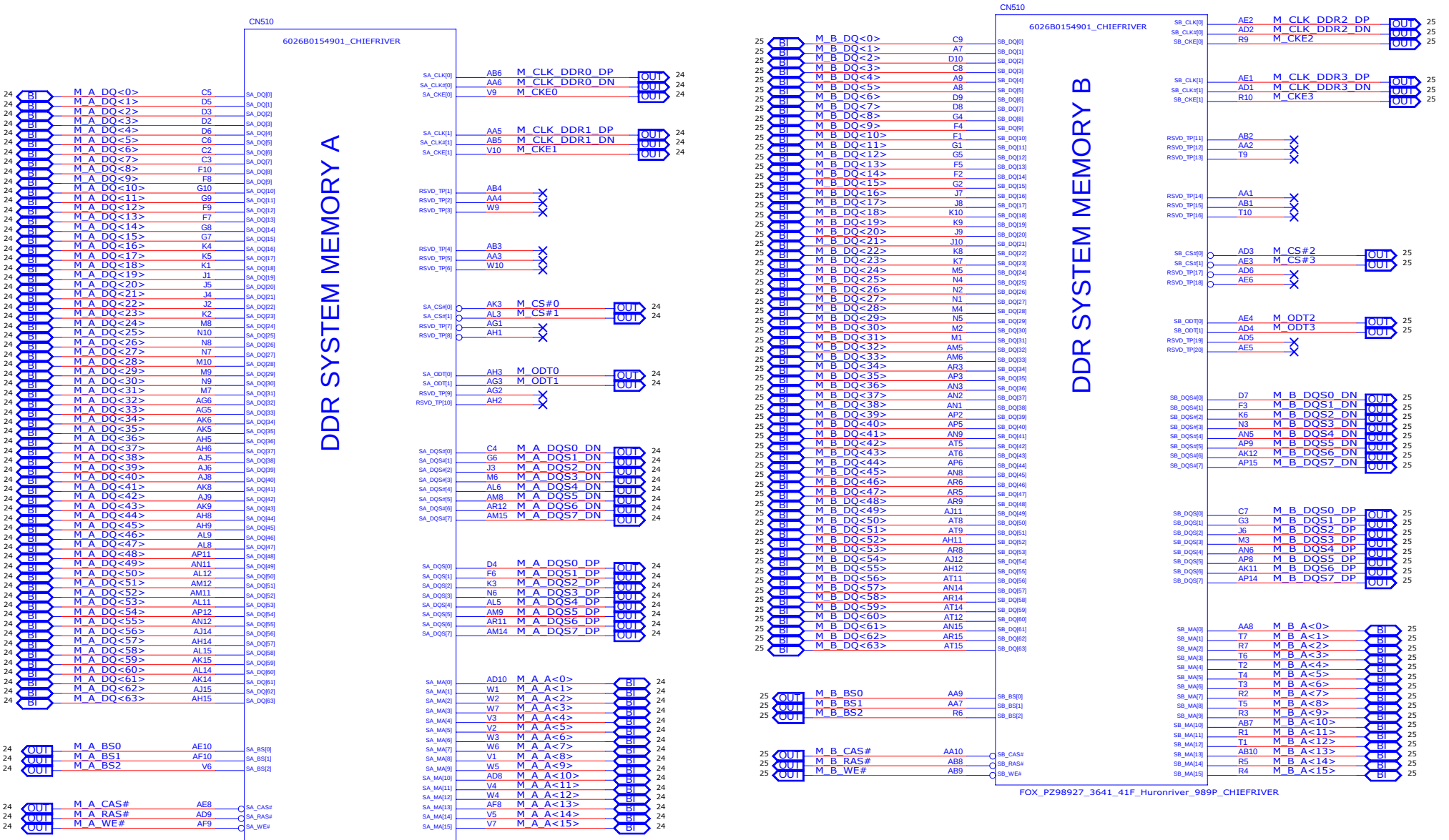
MOUNT	OPEN (PAGE26)	OPEN (PAGE41)
X2	D4400	X400
R1	X501	C402
L1	R958	C403
C180	C874	
C181	C875	
C182		
C183	OPEN (PAGE27)	OPEN (PAGE49)
C184	X503	X1
C185	R1041	R29
C186	C962	C35
C187	C965	C36
R906 (PAGE26)		
R912 (PAGE27)		
R414 (PAGE41)		
R120 (PAGE49)		

INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION GREEN_CLK_SLG3NB250			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX	DATE 21-OCT-2002	SHEET 16 of 57	


P1V8S
6026B0154901_CHIEFRIVER
CN510
R4500 1K_5%_2_DY
R683 2.2K_5%_2
R684 1K_5%_2
31 OUT NV_CLE
H_SNB_IVB# C26
PROC_SELECT#
TP4500
TP30
AN34
SKTOCC#
MISC
CLOCKS
P1V05S_CPU
TP4501
TP30
AL33
CATERR#
THERMAL
R748 62_5%_2
35 OUT H_PECI
AN33
PECI
35 12 IN CPU_PROCHOT#
R750 56_5%_2
CPU_PROCHOT#_R AL32
PROCHOT#
C805 47pF_50V_2
31 OUT PM_THRMTRIP#
AN32
THERMTRIP#
MISC
DDR3
R749 10K_5%_2
PWR MANAGEMENT
28 BI H_PM_SYNC
AM34
PM_SYNC
31 IN H_CPUPWRGD
AP33
UNCOREPWRGOOD
17 IN PM_DRAM_PWRGD_CPU
R799 130_1%_2
PM_DRAM_PWRGD_V8_R
SM_DRAMPWROK
46 35 30 IN BUF_PLT_RST#1
R790 1.5K_1%_1/16W
BUF_PLT_RST#_R AR33
RESET#
R789 750_1%_2
FOX_PZ98927_3641_41F_Huronriver_989P_CHIEFRIVER
JTAG & BPM
BCLK
BCLK#
A28 CLK_DMI_PCH_R_DP
A27 CLK_DMI_PCH_R_DN
R639 0_5%_2
R638 0_5%_2
CLK_DMI_PCH_DP
CLK_DMI_PCH_DN
IN 27
IN 27
DPLL_REF_CLK
DPLL_REF_CLK#
A16 CLK_DP_PCH_R_DP
A15 CLK_DP_PCH_R_DN
R689 1K_5%_2
R690 1K_5%_2
P1V05S_CPU
SM_DRAMRST#
R8 CPU_DRAMRST#
OUT 17
SM_RCOMP[0]
SM_RCOMP[1]
SM_RCOMP[2]
AK1 SM_RCOMP0
A5 SM_RCOMP1
A4 SM_RCOMP2
R693
R737 140_1%_2
25.5_1%_2
R694 200_1%_2
PRDY#
PREQ#
AP29
AP27 XDP_PREQ#
TP4502
TP4503
TP30
TP30
TCK
TMS
TRST#
AR26 XDP_TCLK
AP27 XDP_TMS
AP30 XDP_TRST#
TP4504
TP4505
TP4506
TP30
TP30
TP30
TDI
TDO
AR28 XDP_TDI_R
AP26 XDP_TDO
TP4507
TP4508
TP30
TP30
DBR#
AL35 XDP_DBRESET#
TP4509
TP30
BPM#[0]
BPM#[1]
BPM#[2]
BPM#[3]
BPM#[4]
BPM#[5]
BPM#[6]
BPM#[7]
AT28
AR29
AR30
AT30
AP32
AR31
AT31
AR32
P3V3A
P1V5S
R14115 200_5%_2
C4502 0.1uF_16V_2
R800 200_5%_2
28 IN PM_DRAM_PWRGD
35 15 IN ALL_PWGD_IN
U500
NXP_74AHC1G09GV_SOT753_5P
6019B0773901
(OD AND GATE)
PM_DRAM_PWRGD_CPU OUT 17
P1V5
R807 1K_1%_2
R801 1K_5%_2
DIMM_DRAMRST# OUT 24 25
Q539
BSS138LT1
27 21 IN PCH_DDR_RST
17 IN CPU_DRAMRST#
C809 0.047uF_16V_2
R805 4.99K_1%_2
P3V3S
XDP_DBRESET# R788 1K_5%_2
P1V05S_CPU
XDP_TDO R792 51_5%_2
XDP_TMS R1076 51_5%_2
XDP_TDI_R R1074 51_5%_2
XDP_PREQ# R1075 51_5%_2_DY
XDP_TRST# R791 51_5%_2
XDP_TCLK R1077 51_5%_2
INVENTEC
TITLE
MODEL,PROJECT,FUNCTION
CPU - 1
SIZE A3
CODE CS
DOC.NUMBER 1310xxxxx-0-0
REV X01
CHANGE by XXX
DATE 21-OCT-2002
SHEET 17 of 57


R736
WITHIN 500 MILS
OF THE CPU
P1V05S_CPU
CN510
6026B0154901_CHIEFRIVER
CPU_PEG_ICOMPI
R736
24.9_1%_2
DMI_TX0_DN
DMI_TX1_DN
DMI_TX2_DN
DMI_TX3_DN
DMI_TX0_DP
DMI_TX1_DP
DMI_TX2_DP
DMI_TX3_DP
DMI_RX0_DN
DMI_RX1_DN
DMI_RX2_DN
DMI_RX3_DN
DMI_RX0_DP
DMI_RX1_DP
DMI_RX2_DP
DMI_RX3_DP
DMI
FDI_TX0_DN
FDI_TX1_DN
FDI_TX2_DN
FDI_TX3_DN
FDI_TX4_DN
FDI_TX5_DN
FDI_TX6_DN
FDI_TX7_DN
FDI_TX0_DP
FDI_TX1_DP
FDI_TX2_DP
FDI_TX3_DP
FDI_TX4_DP
FDI_TX5_DP
FDI_TX6_DP
FDI_TX7_DP
FDI_FSYNC0
FDI_FSYNC1
FDI_INT
FDI_LSYNC0
FDI_LSYNC1
Intel(R) FDI
PCI EXPRESS* - GRAPHICS
P1V05S_CPU
R686
24.9_1%_2
CPU_EDP_COMPIO
R686
WITHIN 500 MILS
OF THE CPU
eDP
PEG_RX0_C_DN
PEG_RX1_C_DN
PEG_RX2_C_DN
PEG_RX3_C_DN
PEG_RX4_C_DN
PEG_RX5_C_DN
PEG_RX6_C_DN
PEG_RX7_C_DN
PEG_RX0_C_DP
PEG_RX1_C_DP
PEG_RX2_C_DP
PEG_RX3_C_DP
PEG_RX4_C_DP
PEG_RX5_C_DP
PEG_RX6_C_DP
PEG_RX7_C_DP
PEG_TX0_DN
PEG_TX1_DN
PEG_TX2_DN
PEG_TX3_DN
PEG_TX4_DN
PEG_TX5_DN
PEG_TX6_DN
PEG_TX7_DN
PEG_TX0_DP
PEG_TX1_DP
PEG_TX2_DP
PEG_TX3_DP
PEG_TX4_DP
PEG_TX5_DP
PEG_TX6_DP
PEG_TX7_DP
FOX_PZ98927_3641_41F_Huronriver_989P_CHIEFRIVER
CLOSE TO CPU
PEG_TX0_DN C628 0.1UF_16V_2 PEG_TX0_C_DN
PEG_TX1_DN C622 0.1UF_16V_2 PEG_TX1_C_DN
PEG_TX2_DN C629 0.1UF_16V_2 PEG_TX2_C_DN
PEG_TX3_DN C623 0.1UF_16V_2 PEG_TX3_C_DN
PEG_TX4_DN C626 0.1UF_16V_2 PEG_TX4_C_DN
PEG_TX5_DN C624 0.1UF_16V_2 PEG_TX5_C_DN
PEG_TX6_DN C601 0.1UF_16V_2 PEG_TX6_C_DN
PEG_TX7_DN C620 0.1UF_16V_2 PEG_TX7_C_DN
PEG_TX0_DP C631 0.1UF_16V_2 PEG_TX0_C_DP
PEG_TX1_DP C619 0.1UF_16V_2 PEG_TX1_C_DP
PEG_TX2_DP C630 0.1UF_16V_2 PEG_TX2_C_DP
PEG_TX3_DP C618 0.1UF_16V_2 PEG_TX3_C_DP
PEG_TX4_DP C627 0.1UF_16V_2 PEG_TX4_C_DP
PEG_TX5_DP C621 0.1UF_16V_2 PEG_TX5_C_DP
PEG_TX6_DP C625 0.1UF_16V_2 PEG_TX6_C_DP
PEG_TX7_DP C600 0.1UF_16V_2 PEG_TX7_C_DP
INVENTEC
TITLE
MODEL,PROJECT,FUNCTION
CPU - 2
SIZE A3
CODE CS
DOC.NUMBER 1310xxxxx-0-0
REV X01
CHANGE by XXX
DATE 21-OCT-2002
SHEET 18 of 57


CN510
6026B0154901_CHIEFRIVER
DDR SYSTEM MEMORY A
M_A_DQ<0> C5
M_A_DQ<1> D5
M_A_DQ<2> D3
M_A_DQ<3> D2
M_A_DQ<4> D6
M_A_DQ<5> C6
M_A_DQ<6> C2
M_A_DQ<7> C3
M_A_DQ<8> F10
M_A_DQ<9> F8
M_A_DQ<10> G10
M_A_DQ<11> G9
M_A_DQ<12> F9
M_A_DQ<13> F7
M_A_DQ<14> G8
M_A_DQ<15> G7
M_A_DQ<16> K4
M_A_DQ<17> K5
M_A_DQ<18> K1
M_A_DQ<19> J1
M_A_DQ<20> J5
M_A_DQ<21> J4
M_A_DQ<22> J2
M_A_DQ<23> K2
M_A_DQ<24> M8
M_A_DQ<25> N10
M_A_DQ<26> N8
M_A_DQ<27> N7
M_A_DQ<28> M10
M_A_DQ<29> M9
M_A_DQ<30> N9
M_A_DQ<31> M7
M_A_DQ<32> AG6
M_A_DQ<33> AG5
M_A_DQ<34> AK6
M_A_DQ<35> AK5
M_A_DQ<36> AH5
M_A_DQ<37> AH6
M_A_DQ<38> AJ5
M_A_DQ<39> AJ6
M_A_DQ<40> AJ8
M_A_DQ<41> AK8
M_A_DQ<42> AJ9
M_A_DQ<43> AK9
M_A_DQ<44> AH8
M_A_DQ<45> AH9
M_A_DQ<46> AL9
M_A_DQ<47> AL8
M_A_DQ<48> AP11
M_A_DQ<49> AN11
M_A_DQ<50> AL12
M_A_DQ<51> AM12
M_A_DQ<52> AM11
M_A_DQ<53> AL11
M_A_DQ<54> AP12
M_A_DQ<55> AN12
M_A_DQ<56> AJ14
M_A_DQ<57> AH14
M_A_DQ<58> AL15
M_A_DQ<59> AK15
M_A_DQ<60> AL14
M_A_DQ<61> AK14
M_A_DQ<62> AJ15
M_A_DQ<63> AH15
M_A_BS0 AE10
M_A_BS1 AF10
M_A_BS2 V6
M_A_CAS# AE8
M_A_RAS# AD9
M_A_WE# AF9
M_CLK_DDR0_DP AB6
M_CLK_DDR0_DN AA6
M_CKE0 V9
M_CLK_DDR1_DP AA5
M_CLK_DDR1_DN AB5
M_CKE1 V10
AB4
AA4
W9
AB3
AA3
W10
M_CS#0 AK3
M_CS#1 AL3
AG1
AH1
M_ODT0 AH3
M_ODT1 AG3
AG2
AH2
M_A_DQS0_DN C4
M_A_DQS1_DN G6
M_A_DQS2_DN J3
M_A_DQS3_DN M6
M_A_DQS4_DN AL6
M_A_DQS5_DN AM8
M_A_DQS6_DN AR12
M_A_DQS7_DN AM15
M_A_DQS0_DP D4
M_A_DQS1_DP F6
M_A_DQS2_DP K3
M_A_DQS3_DP N6
M_A_DQS4_DP AL5
M_A_DQS5_DP AM9
M_A_DQS6_DP AR11
M_A_DQS7_DP AM14
M_A_A<0> AD10
M_A_A<1> W1
M_A_A<2> W2
M_A_A<3> W7
M_A_A<4> V3
M_A_A<5> V2
M_A_A<6> W3
M_A_A<7> W6
M_A_A<8> V1
M_A_A<9> W5
M_A_A<10> AD8
M_A_A<11> V4
M_A_A<12> W4
M_A_A<13> AF8
M_A_A<14> V5
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FOX_PZ98927_3641_41F_Huronriver_989P_CHIEFRIVER
CN510
6026B0154901_CHIEFRIVER
DDR SYSTEM MEMORY B
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M_B_DQ<2> D10
M_B_DQ<3> C8
M_B_DQ<4> A9
M_B_DQ<5> A8
M_B_DQ<6> D9
M_B_DQ<7> D8
M_B_DQ<8> G4
M_B_DQ<9> F4
M_B_DQ<10> F1
M_B_DQ<11> G1
M_B_DQ<12> G5
M_B_DQ<13> F5
M_B_DQ<14> F2
M_B_DQ<15> G2
M_B_DQ<16> J7
M_B_DQ<17> J8
M_B_DQ<18> K10
M_B_DQ<19> K9
M_B_DQ<20> J9
M_B_DQ<21> J10
M_B_DQ<22> K8
M_B_DQ<23> K7
M_B_DQ<24> M5
M_B_DQ<25> N4
M_B_DQ<26> N2
M_B_DQ<27> N1
M_B_DQ<28> M4
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M_B_DQ<32> AM5
M_B_DQ<33> AM6
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M_B_DQ<35> AP3
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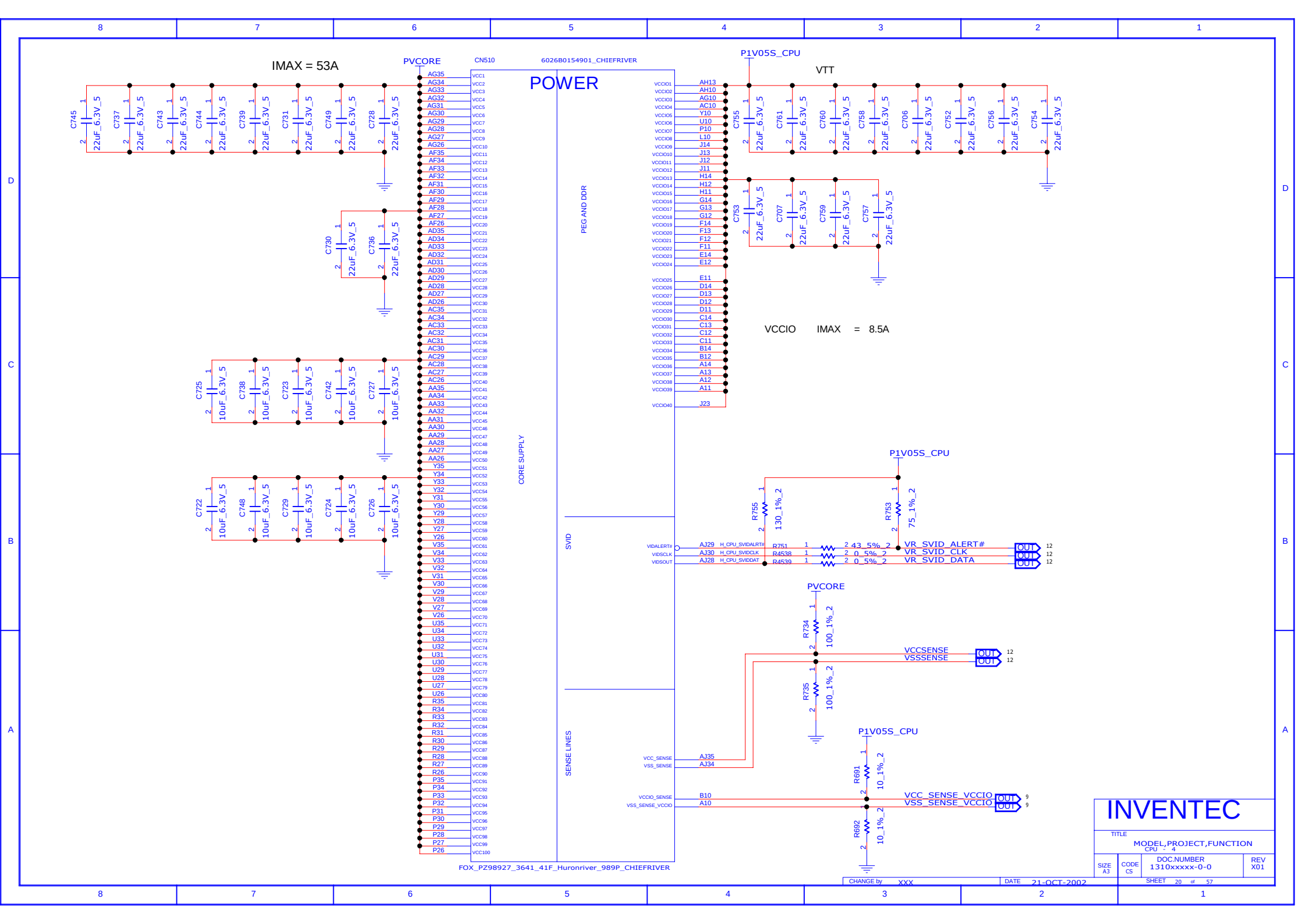
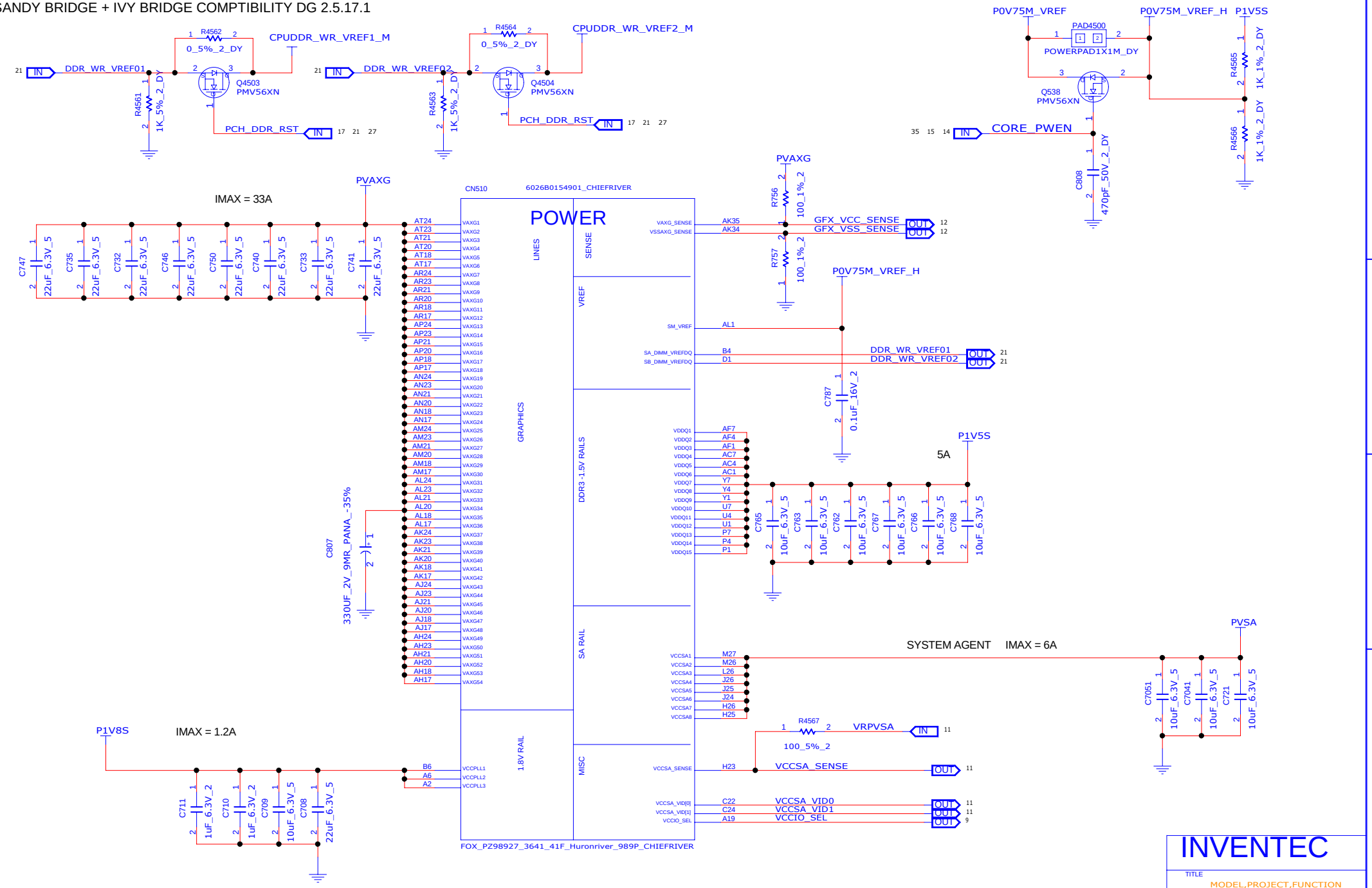
M_B_DQ<43> AT6
M_B_DQ<44> AP6
M_B_DQ<45> AN8
M_B_DQ<46> AR6
M_B_DQ<47> AR5
M_B_DQ<48> AR9
M_B_DQ<49> AJ11
M_B_DQ<50> AT8
M_B_DQ<51> AT9
M_B_DQ<52> AH11
M_B_DQ<53> AR8
M_B_DQ<54> AJ12
M_B_DQ<55> AH12
M_B_DQ<56> AT11
M_B_DQ<57> AN14
M_B_DQ<58> AR14
M_B_DQ<59> AT14
M_B_DQ<60> AT12
M_B_DQ<61> AN15
M_B_DQ<62> AR15
M_B_DQ<63> AT15
M_B_BS0 AA9
M_B_BS1 AA7
M_B_BS2 R6
M_B_CAS# AA10
M_B_RAS# AB8
M_B_WE# AB9
M_CLK_DDR2_DP AE2
M_CLK_DDR2_DN AD2
M_CKE2 R9
M_CLK_DDR3_DP AE1
M_CLK_DDR3_DN AD1
M_CKE3 R10
AB2
AA2
T9
AA1
AB1
T10
M_CS#2 AD3
M_CS#3 AE3
AD6
AE6
M_ODT2 AE4
M_ODT3 AD4
AD5
AE5
M_B_DQS0_DN D7
M_B_DQS1_DN F3
M_B_DQS2_DN K6
M_B_DQS3_DN N3
M_B_DQS4_DN AN5
M_B_DQS5_DN AP9
M_B_DQS6_DN AK12
M_B_DQS7_DN AP15
M_B_DQS0_DP C7
M_B_DQS1_DP G3
M_B_DQS2_DP J6
M_B_DQS3_DP M3
M_B_DQS4_DP AN6
M_B_DQS5_DP AP8
M_B_DQS6_DP AK11
M_B_DQS7_DP AP14
M_B_A<0> AA8
M_B_A<1> T7
M_B_A<2> R7
M_B_A<3> T6
M_B_A<4> T2
M_B_A<5> T4
M_B_A<6> T3
M_B_A<7> R2
M_B_A<8> T5
M_B_A<9> R3
M_B_A<10> AB7
M_B_A<11> R1
M_B_A<12> T1
M_B_A<13> AB10
M_B_A<14> R5
M_B_A<15> R4
FOX_PZ98927_3641_41F_Huronriver_989P_CHIEFRIVER
INVENTEC
TITLE
MODEL,PROJECT,FUNCTION
CPU - 3
SIZE A3
CODE CS
DOC.NUMBER 1310xxxxx-0-0
REV X01
CHANGE by XXX
DATE 21-OCT-2002
SHEET 19 of 57


IMAX = 53A
PVCORE
CN510
6026B0154901_CHIEFRIVER
POWER
P1V05S_CPU
VTT
VCCIO IMAX = 8.5A
PEG AND DDR
CORE SUPPLY
SVID
SENSE LINES
VR_SVID_ALERT#
VR_SVID_CLK
VR_SVID_DATA
VCCSENSE
VSSSENSE
VCC_SENSE_VCCIO
VSS_SENSE_VCCIO
FOX_PZ98927_3641_41F_Huronriver_989P_CHIEFRIVER
INVENTEC
MODEL,PROJECT,FUNCTION
CPU - 4
DOC.NUMBER
1310xxxxx-0-0
REV
X01
SIZE
A3
CODE
CS
CHANGE by
XXX
DATE
21-OCT-2002
SHEET
20 of 57

SANDY BRIDGE + IVY BRIDGE COMPTIBILITY DG 2.5.17.1



INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION CPU - 5			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01

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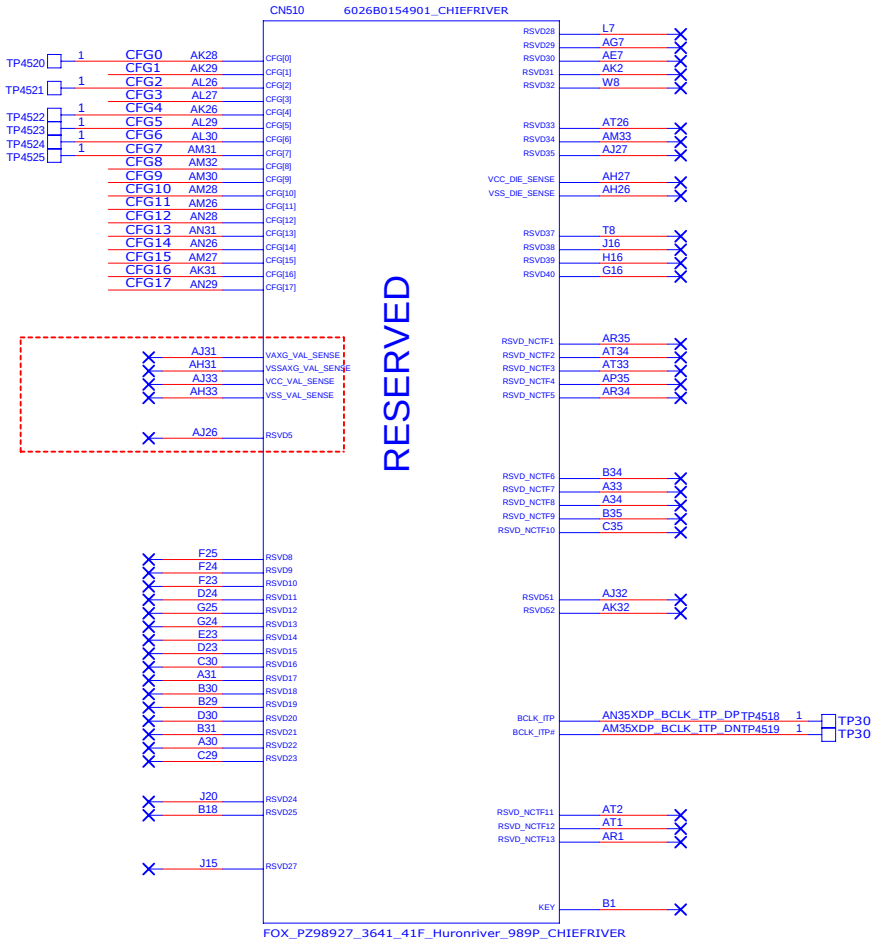
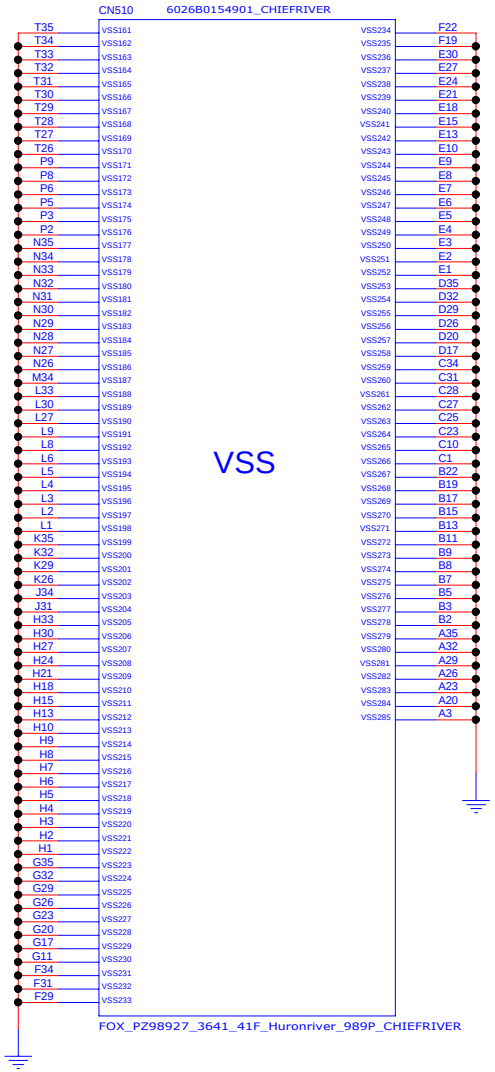
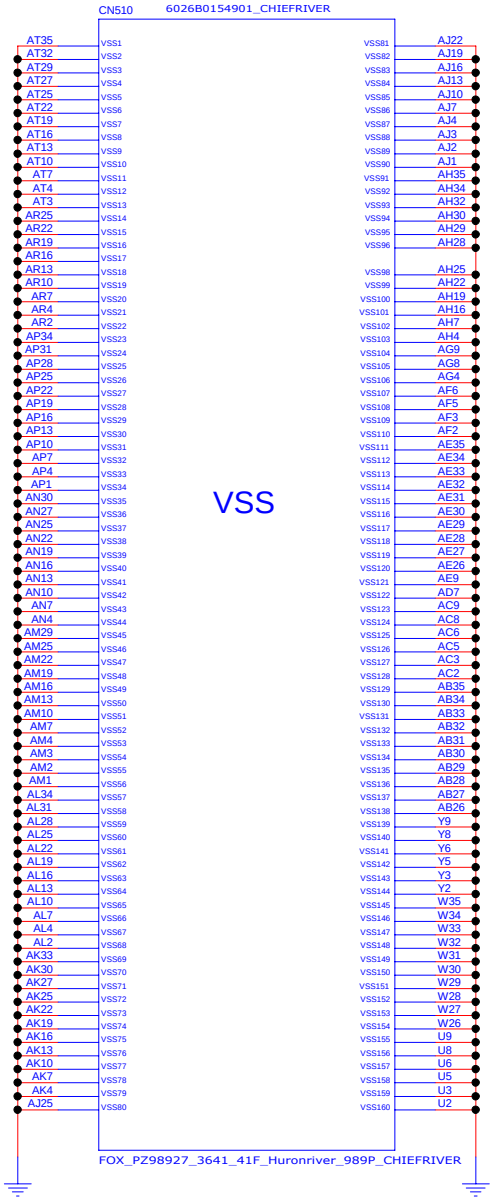
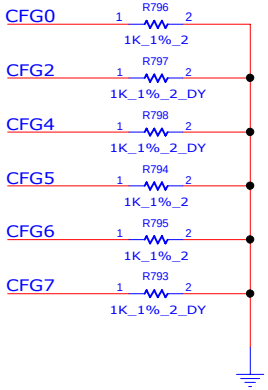








CFG[2] : PCI Express* Static x16 Lane Numbering Reversal.
1 = Normal operation
0 = Lane numbers reversed

CFG[4] : eDP enable
1 = Disabled
0 = Enabled

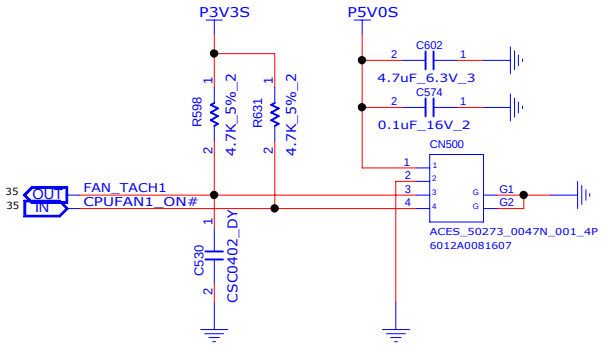
CFG[6:5] : PCI Express Bifurcation:
00 = 1 x8, 2 x4 PCI Expres
01 = reserved
10 = 2 x8 PCI Express
11 = 1 x16 PCI Express

CFG[7] :PEG DEFER TRAINING
1: (Default) PEG Train immediately following RESETB deassertion
0: PEG Wait for BIOS for training

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION CPU - 6			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX	DATE 21-OCT-2002	SHEET 22 of 57	

FAN CONN



7.2.5 Register : Local Diode Temperature Alert Temperature

Location : Read = Address 05h Write = Address 0Bh
Type : Read/Write
Power on default value : Hardware strapping.

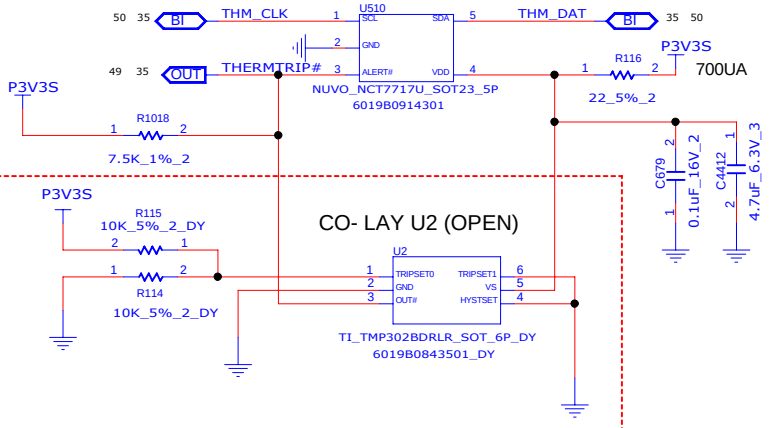
BIT	7	6	5	4	3	2	1	0
NAME	LDT Alert Temperature							
VALUE	SIGN	64	32	16	8	4	2	1
DEFAULT	Hardware strapping							

6.6 ALERT# point hardware power-on setting

The default value could be set after power up 100ms by different pull-up resistor of ALERT# pin:

PULL-UP RESISTOR		TEMPERATURE (℃)
ALERT	2KΩ	75
	7.5KΩ	90
	10.5KΩ	100
	14KΩ	105
	18.7KΩ	110

THERMAL SENSOR(LOCAL)
NCT7717U I2C / SMBus address is 1001000xb (x is R/W bit).



TMP302 Available Versions(1)

DEVICE	SELECTABLE TRIP POINTS (℃)
TMP302A	50, 55, 60, 65
TMP302B	70, 75, 80, 85
TMP302C	90, 95, 100, 105
TMP302D	110, 115, 120, 125

(1) For other available trip points, please contact a TI representative.

Table 1. Trip Point vs $TRIP_{SET1}$ and $TRIP_{SET0}$

$TRIP_{SET1}$	$TRIP_{SET0}$	TMP302A	TMP302B	TMP302C	TMP302D
GND	GND	+50°C	+70°C	+90°C	+110°C
GND	V_S	+55°C	+75°C	+95°C	+115°C
V_S	GND	+60°C	+80°C	+100°C	+120°C
V_S	V_S	+65°C	+85°C	+105°C	+125°C

Table 2. $HYST_{SET}$ Window

$HYST_{SET}$	THRESHOLD HYSTERESIS
GND	+5°C
V_S	+10°C

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
THERMAL & FAN

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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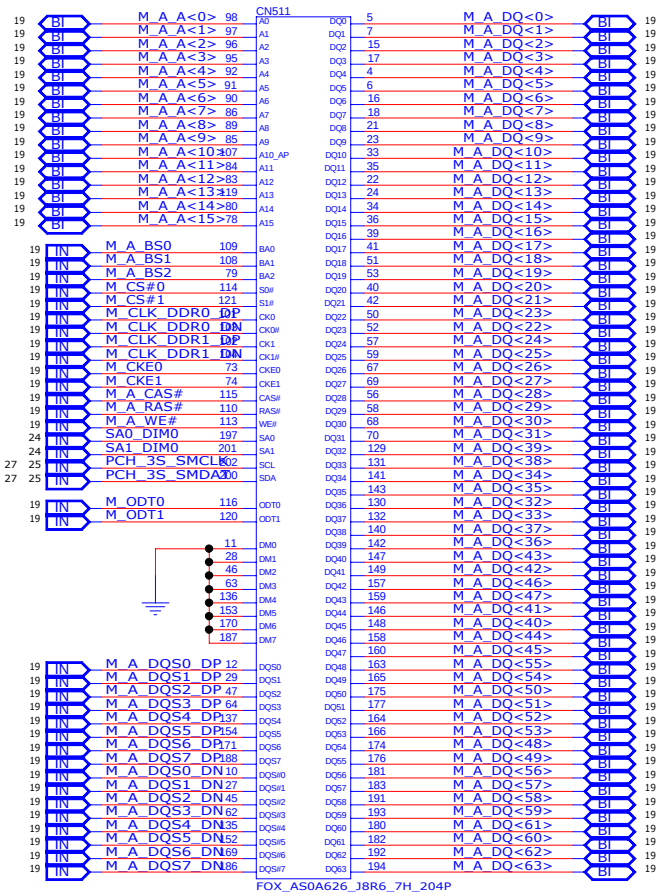
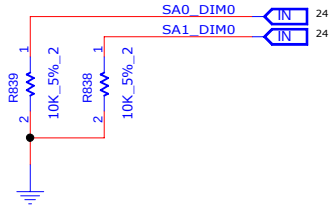
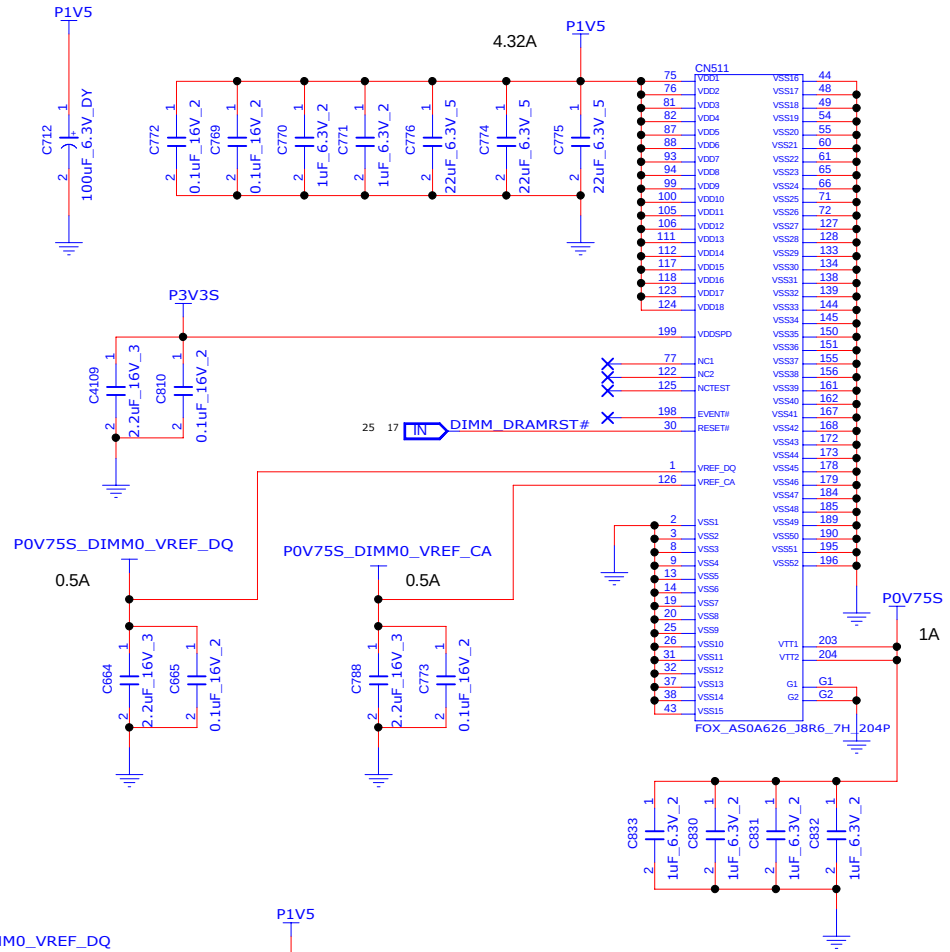
DDR3 (8mm) P/N : 6026B0221101

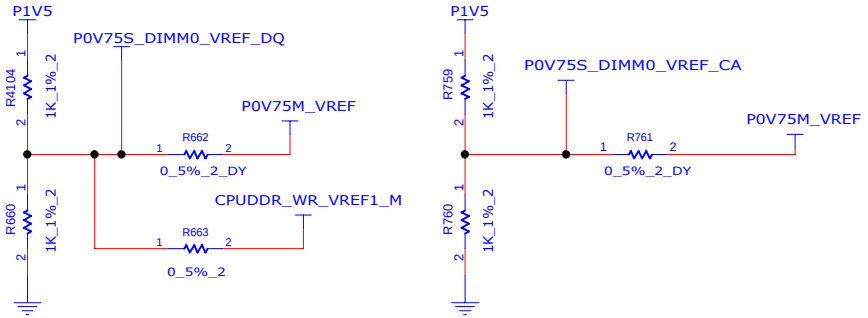


Note :

SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30





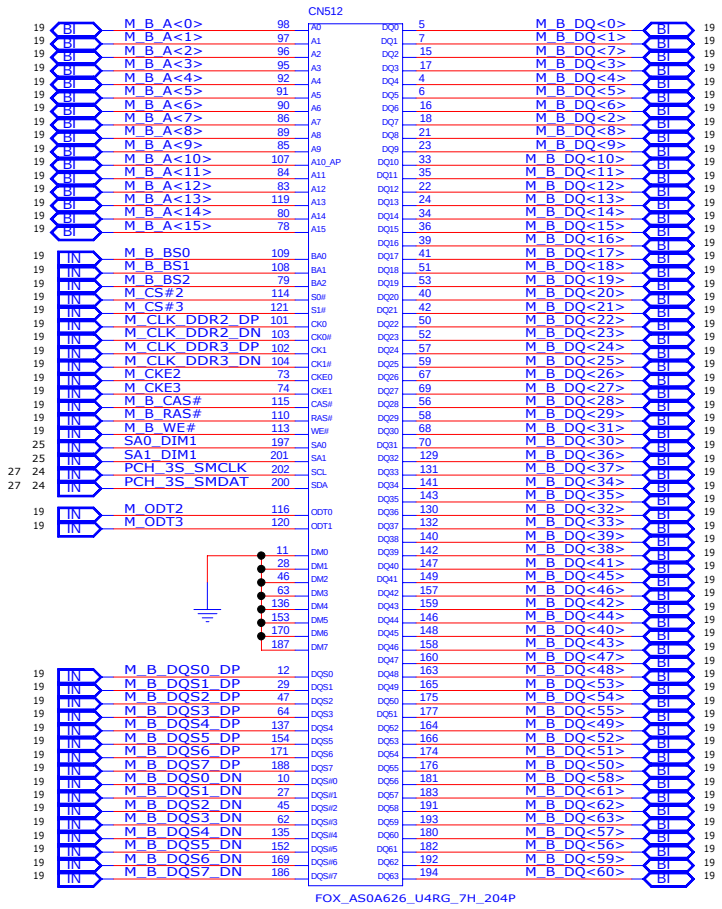


SANDY BRIDGE + IVY BRIDGE DG4.14

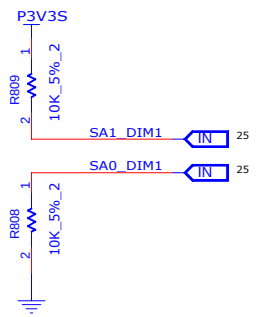
INVENTEC

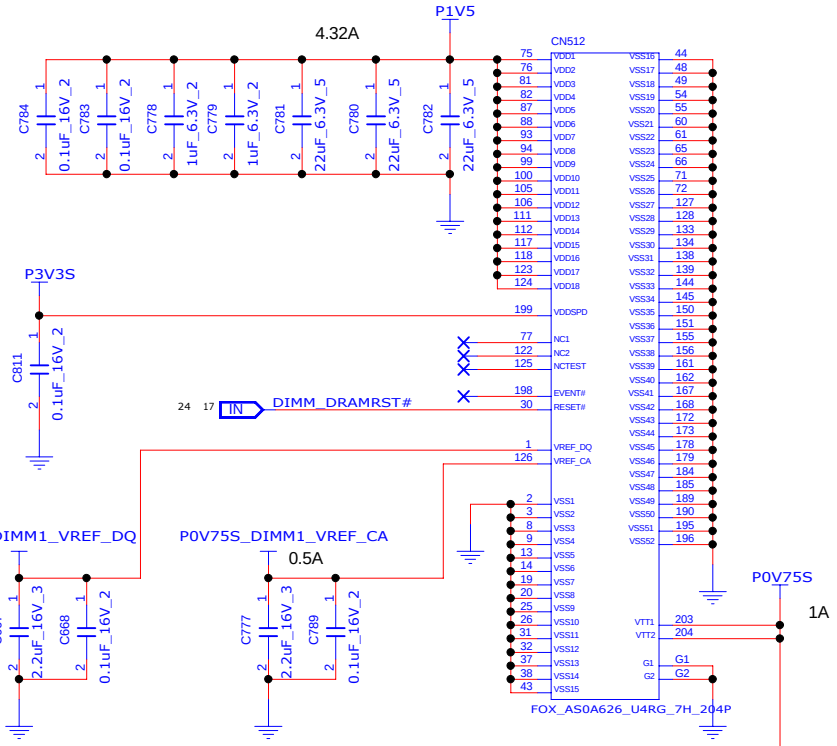
TITLE: MODEL,PROJECT,FUNCTION DDR3 - 1			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX	DATE 21-OCT-2002	SHEET 24 of 57	

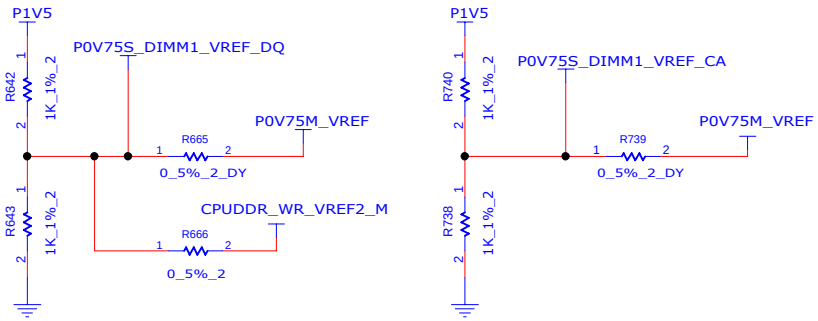
DDR3 (4mm) P/N : 6026B0221601



Note :
SO-DIMMA SPD Address is 0xA4
SO-DIMMA TS Address is 0x34







SANDY BRIDGE + IVY BRIDGE DG4.14

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
DDR3 - 2

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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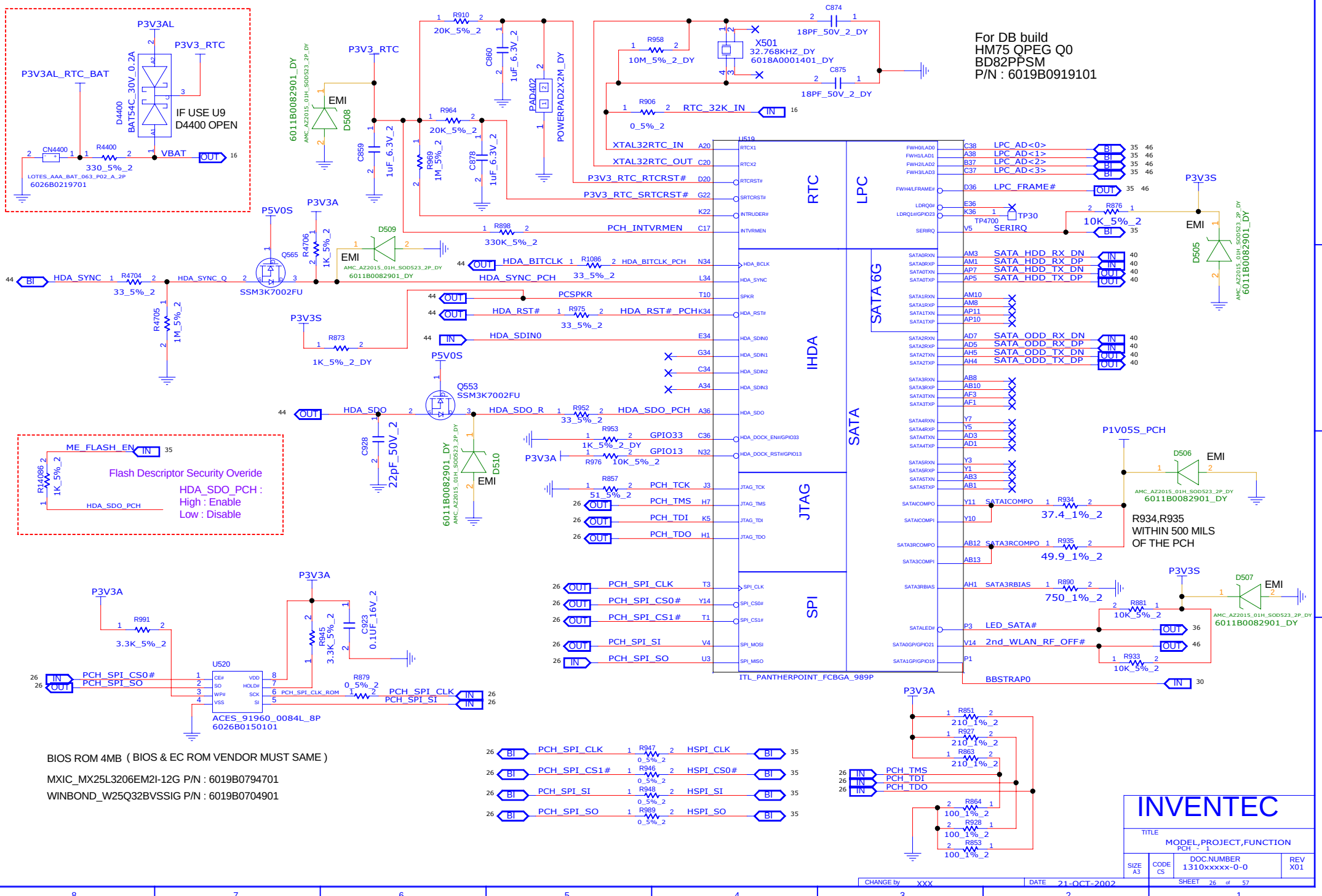
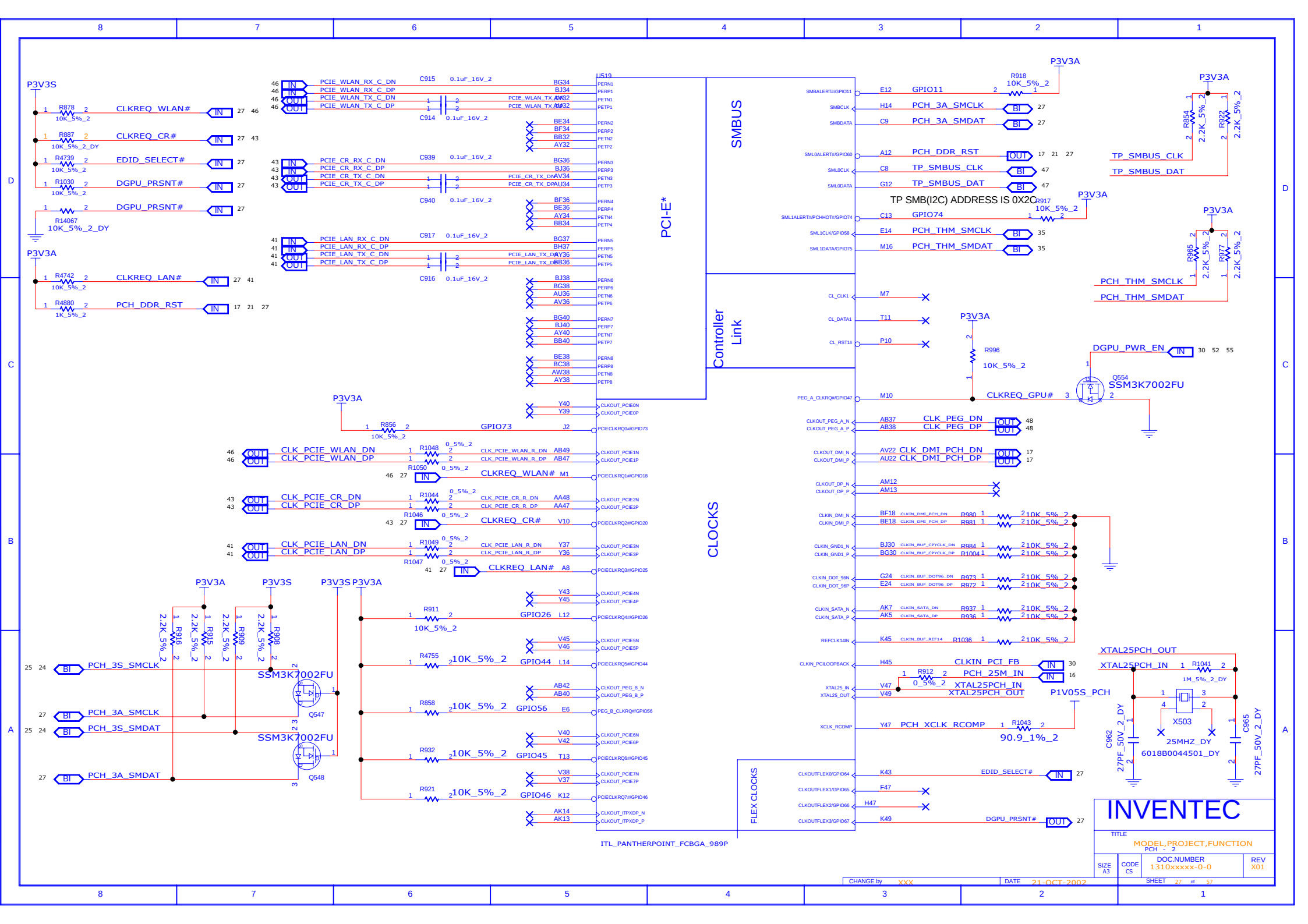
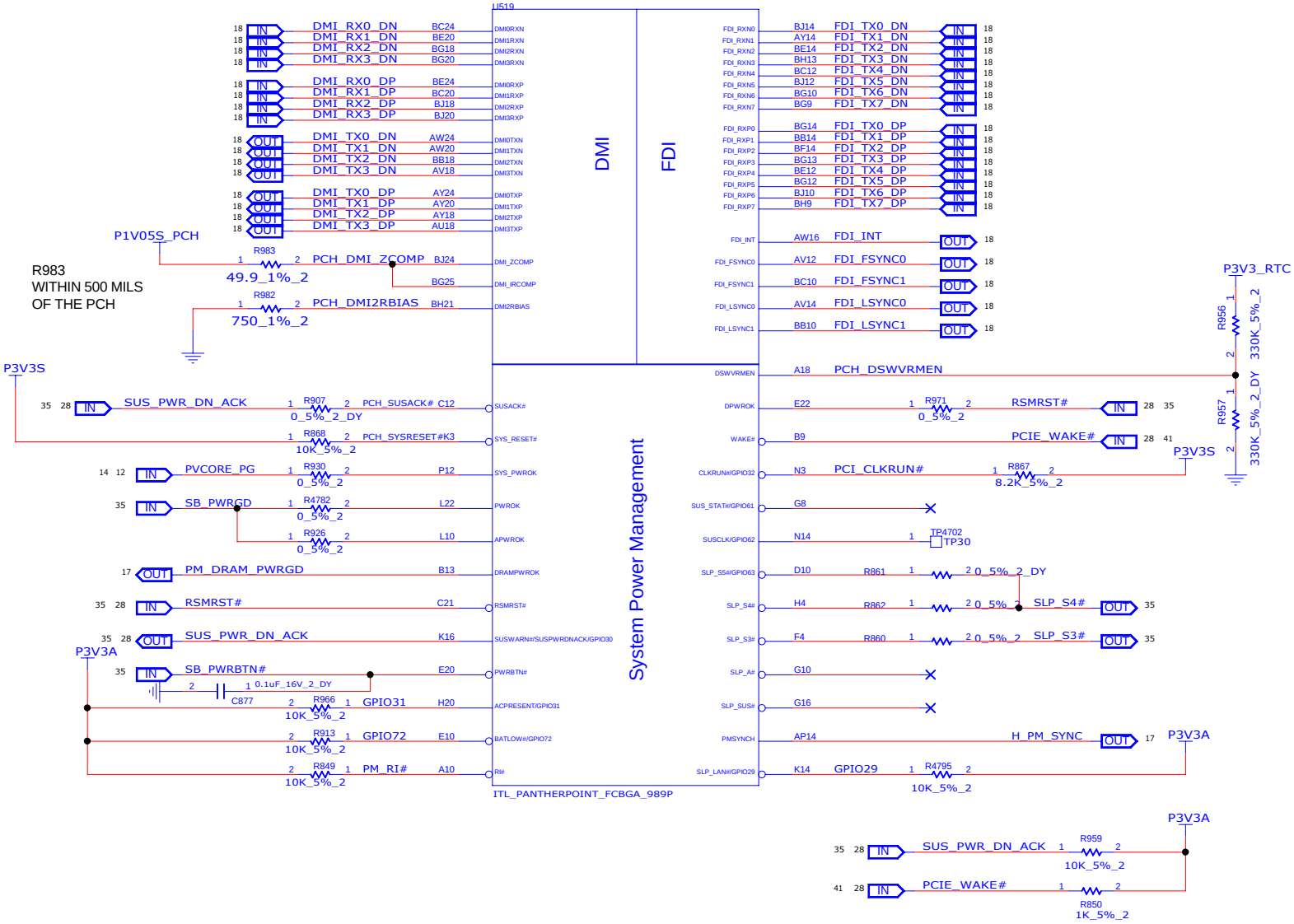
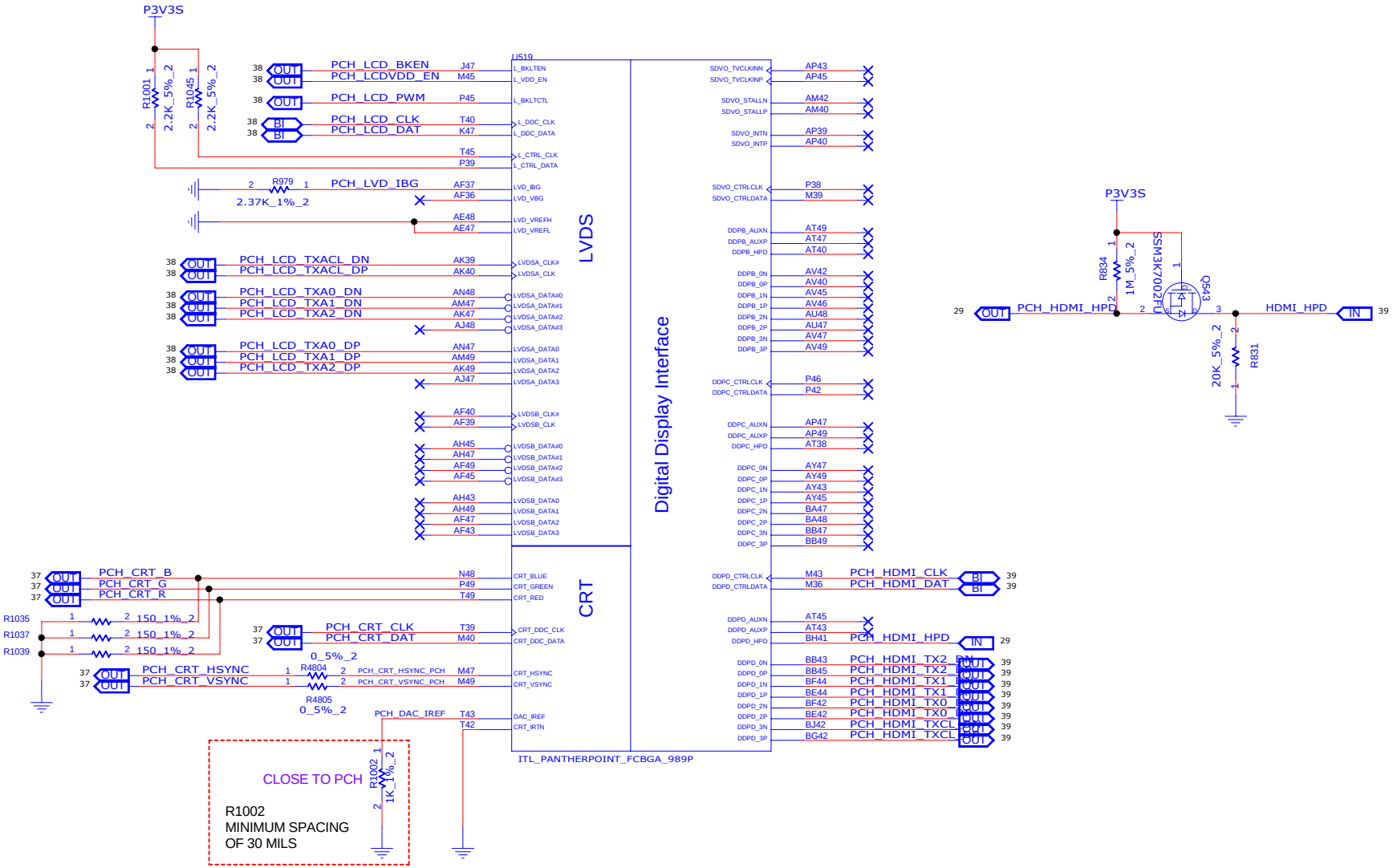

For DB build
HM75 QPEG Q0
BD82PPSM
P/N : 6019B0919101
P3V3AL
P3V3_RTC
P3V3AL_RTC_BAT
IF USE U9
D4400 OPEN
6026B0219701
RTC
LPC
IHDA
SATA
JTAG
SPI
SATA 6G
ITL_PANTHERPOINT_FCBGA_989P
HDA_SYNC
HDA_SYNC_Q
SSM3K7002FU
HDA_BITCLK
HDA_SYNC_PCH
PCSPKR
HDA_RST#
HDA_SDIN0
HDA_SDO
HDA_SDO_R
HDA_SDO_PCH
Flash Descriptor Security Overide
HDA_SDO_PCH :
High : Enable
Low : Disable
ME_FLASH_EN
PCH_SPI_CS0#
PCH_SPI_SO
PCH_SPI_CLK
PCH_SPI_SI
ACES_91960_0084L_8P
6026B0150101
BIOS ROM 4MB (BIOS & EC ROM VENDOR MUST SAME)
MXIC_MX25L3206EM2I-12G P/N : 6019B0794701
WINBOND_W25Q32BVSSIG P/N : 6019B0704901
R934,R935
WITHIN 500 MILS
OF THE PCH
INVENTEC
MODEL,PROJECT,FUNCTION
DOC.NUMBER
1310xxxxx-0-0
CHANGE by XXX
DATE 21-OCT-2002
SHEET 26 of 57

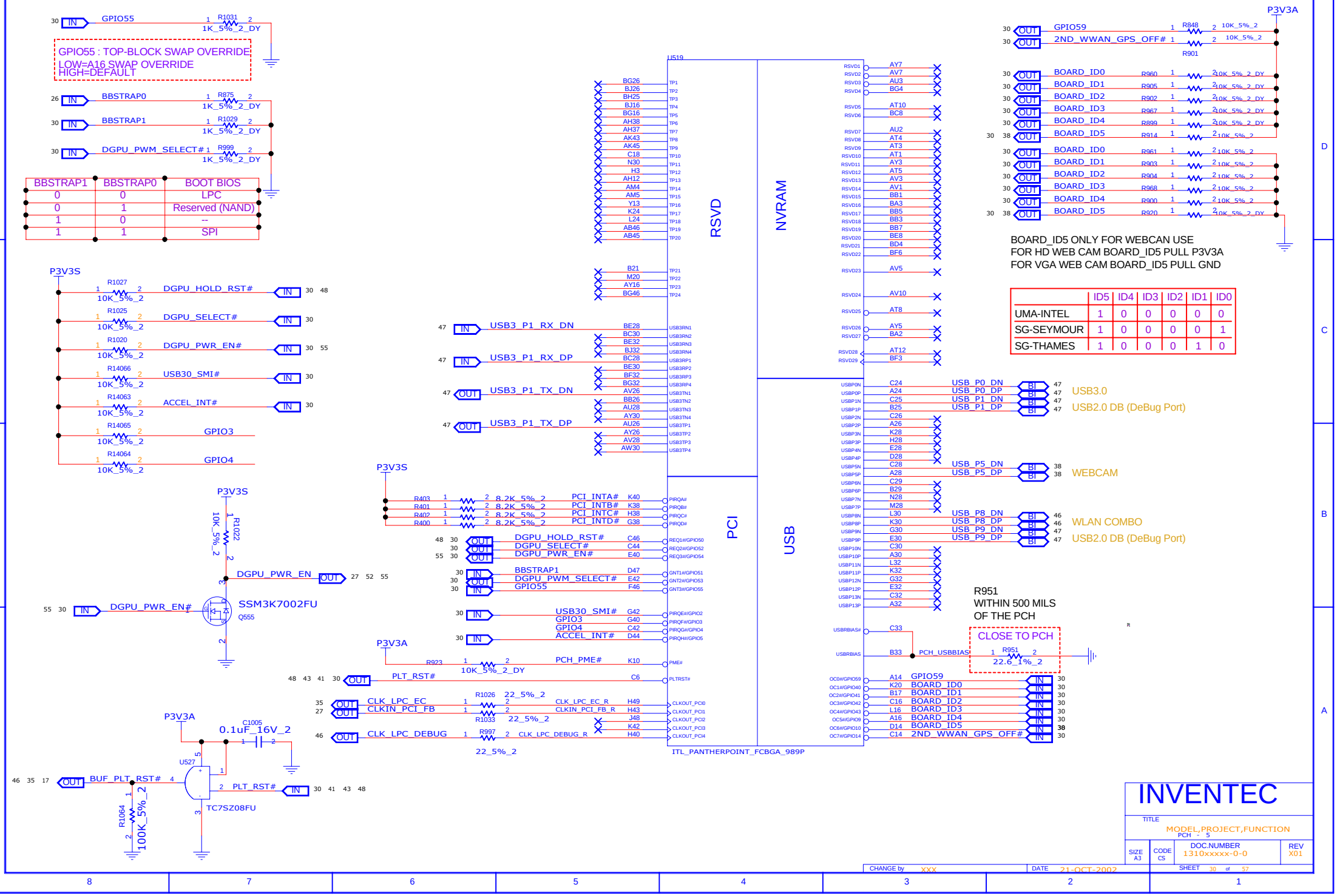

P3V3S
R878 2 CLKREQ_WLAN# IN 27 46
10K_5%_2
R887 2 CLKREQ_CR# IN 27 43
10K_5%_2_DY
R4739 2 EDID_SELECT# IN 27
10K_5%_2
R1030 2 DGPU_PRSNT# IN 27
10K_5%_2
DGPU_PRSNT# IN 27
R14067
10K_5%_2_DY
P3V3A
R4742 2 CLKREQ_LAN# IN 27 41
10K_5%_2
R4880 2 PCH_DDR_RST IN 17 21 27
1K_5%_2
PCIE_WLAN_RX_C_DN
PCIE_WLAN_RX_C_DP
PCIE_WLAN_TX_C_DN
PCIE_WLAN_TX_C_DP
C915 0.1uF_16V_2
C914 0.1uF_16V_2
PCIE_CR_RX_C_DN
PCIE_CR_RX_C_DP
PCIE_CR_TX_C_DN
PCIE_CR_TX_C_DP
C939 0.1uF_16V_2
C940 0.1uF_16V_2
PCIE_LAN_RX_C_DN
PCIE_LAN_RX_C_DP
PCIE_LAN_TX_C_DN
PCIE_LAN_TX_C_DP
C917 0.1uF_16V_2
C916 0.1uF_16V_2
U519
PCI-E*
SMBUS
Controller Link
CLOCKS
FLEX CLOCKS
ITL_PANTHERPOINT_FCBGA_989P
SMBALERT#/GPIO11
SMBCLK
SMBDATA
SML0ALERT#/GPIO60
SML0CLK
SML0DATA
SML1ALERT#/PCHHOT#/GPIO74
SML1CLK/GPIO58
SML1DATA/GPIO75
GPIO11
PCH_3A_SMCLK
PCH_3A_SMDAT
PCH_DDR_RST
TP_SMBUS_CLK
TP_SMBUS_DAT
GPIO74
PCH_THM_SMCLK
PCH_THM_SMDAT
TP SMB(I2C) ADDRESS IS 0X2C
R918 10K_5%_2
R917 10K_5%_2
R854 2.2K_5%_2
R922 2.2K_5%_2
R965 2.2K_5%_2
R977 2.2K_5%_2
CL_CLK1
CL_DATA1
CL_RST1#
R996 10K_5%_2
DGPU_PWR_EN
Q554 SSM3K7002FU
PEG_A_CLKRQ#/GPIO47
CLKREQ_GPU#
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLK_PEG_DN
CLK_PEG_DP
CLKOUT_DMI_N
CLKOUT_DMI_P
CLK_DMI_PCH_DN
CLK_DMI_PCH_DP
CLKOUT_DP_N
CLKOUT_DP_P
CLKIN_DMI_N
CLKIN_DMI_P
CLKIN_GND1_N
CLKIN_GND1_P
CLKIN_DOT_96N
CLKIN_DOT_96P
CLKIN_SATA_N
CLKIN_SATA_P
REFCLK14IN
CLKIN_PCILOOPBACK
CLKIN_PCI_FB
PCH_25M_IN
XTAL25_IN
XTAL25_OUT
XTAL25PCH_IN
XTAL25PCH_OUT
P1V05S_PCH
XCLK_RCOMP
PCH_XCLK_RCOMP
90.9_1%_2
X503 25MHZ_DY 6018B0044501_DY
C962 27PF_50V_2_DY
C965 27PF_50V_2_DY
CLKOUTFLEX0/GPIO64
CLKOUTFLEX1/GPIO65
CLKOUTFLEX2/GPIO66
CLKOUTFLEX3/GPIO67
EDID_SELECT#
DGPU_PRSNT#
CLK_PCIE_WLAN_DN
CLK_PCIE_WLAN_DP
CLK_PCIE_CR_DN
CLK_PCIE_CR_DP
CLK_PCIE_LAN_DN
CLK_PCIE_LAN_DP
CLKREQ_WLAN#
CLKREQ_CR#
CLKREQ_LAN#
GPIO73
GPIO26
GPIO44
GPIO56
GPIO45
GPIO46
R1048 0_5%_2
R1050 0_5%_2
R1044 0_5%_2
R1046 0_5%_2
R1049 0_5%_2
R1047 0_5%_2
R856 10K_5%_2
R911 10K_5%_2
R4755 10K_5%_2
R858 10K_5%_2
R932 10K_5%_2
R921 10K_5%_2
PCH_3S_SMCLK
PCH_3A_SMCLK
PCH_3S_SMDAT
PCH_3A_SMDAT
SSM3K7002FU Q547
SSM3K7002FU Q548
R916 2.2K_5%_2
R915 2.2K_5%_2
R909 2.2K_5%_2
R908 2.2K_5%_2
INVENTEC
TITLE
MODEL,PROJECT,FUNCTION
PCH - 2
SIZE A3
CODE CS
DOC.NUMBER 1310xxxxx-0-0
REV X01
CHANGE by XXX
DATE 21-OCT-2002
SHEET 27 of 57

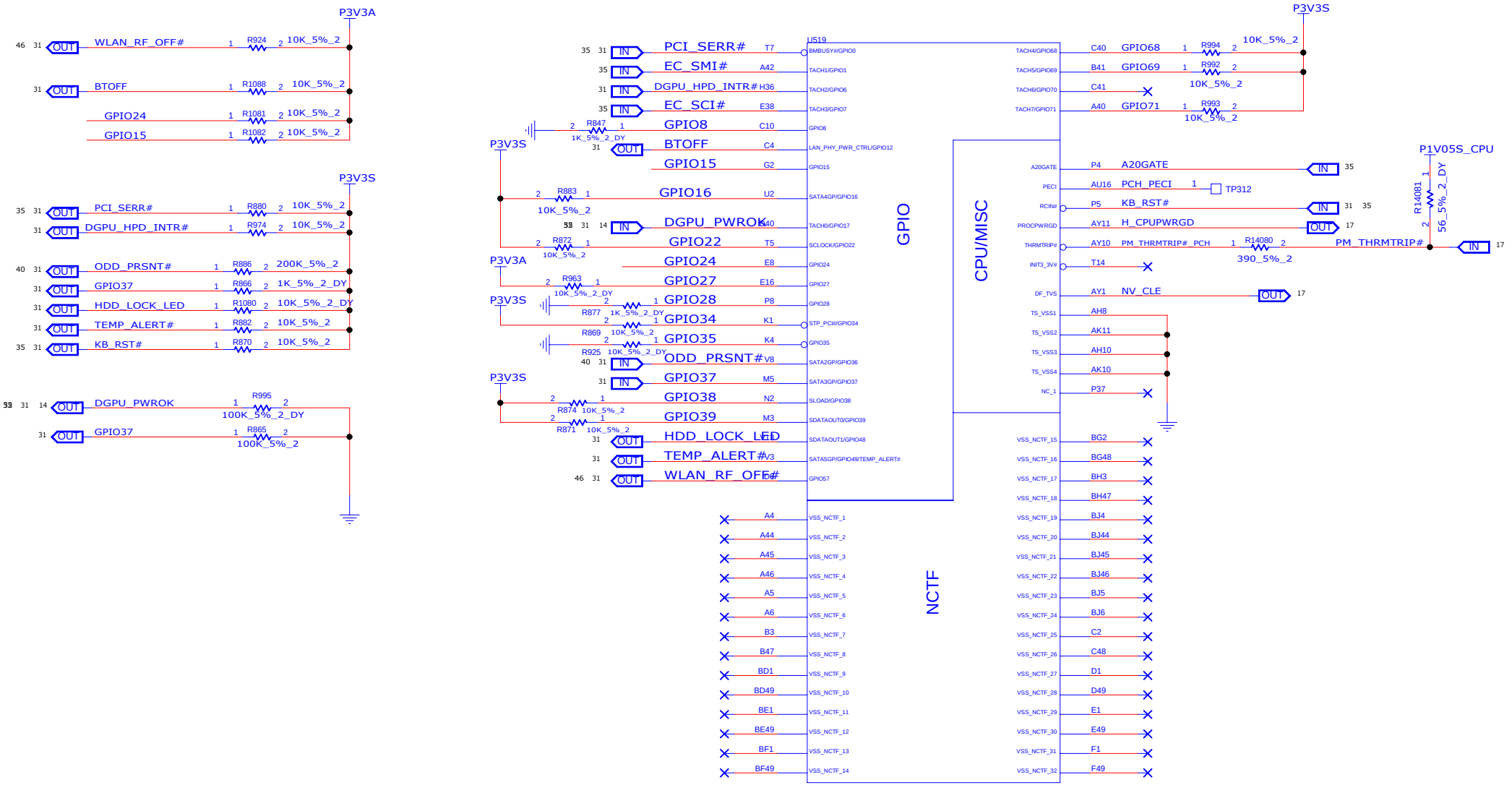


INVENTEC			
TITLE: MODEL,PROJECT,FUNCTION PCH - 3			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX	DATE 21-OCT-2002	SHEET 28 of 57	

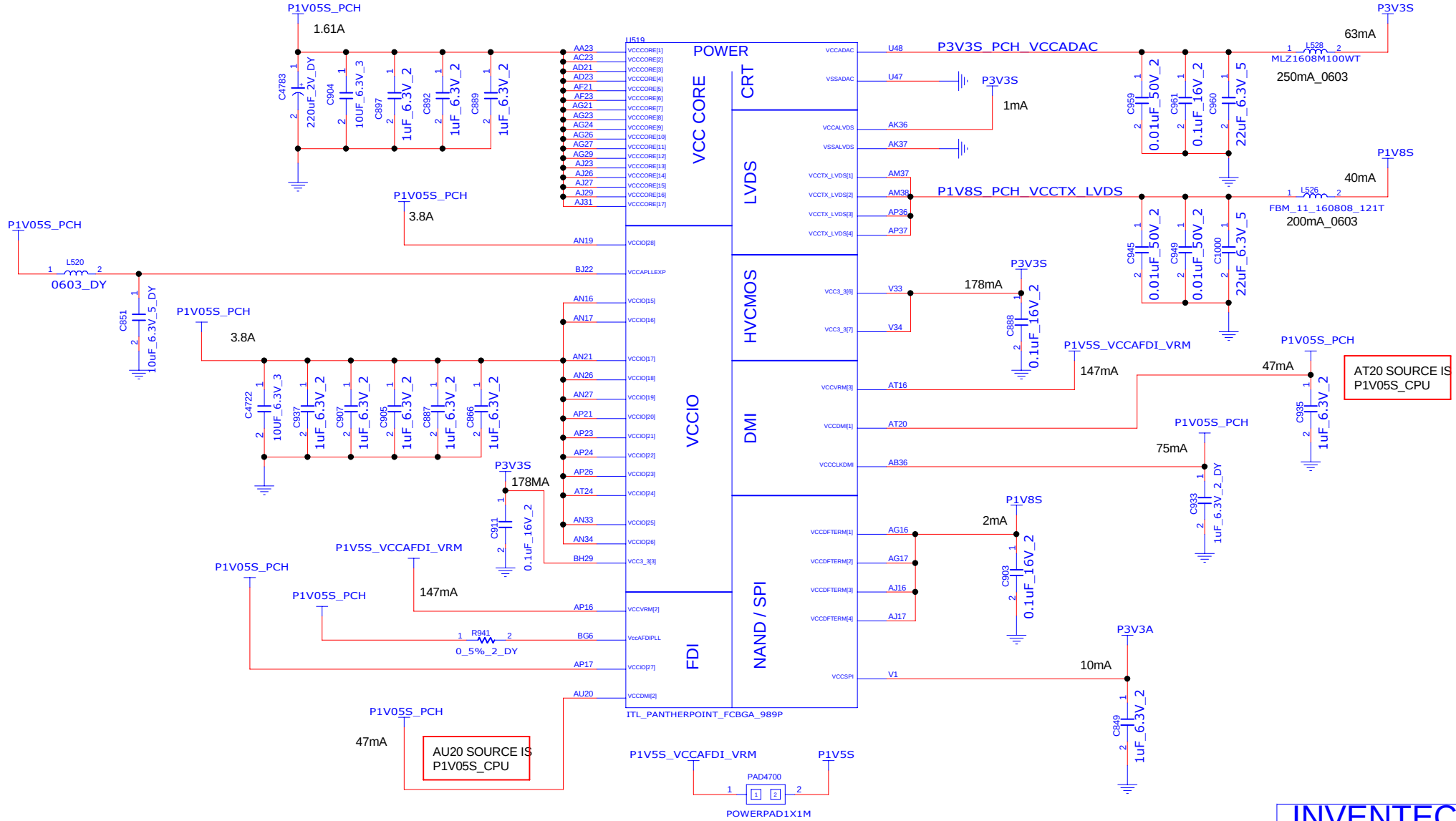


INVENTEC	
TITLE	MODEL,PROJECT,FUNCTION PCH - 4
SIZE A3	CODE CS
DOC.NUMBER	1310xxxxx-0-0
REV	X01
CHANGE by	XXX
DATE	21-OCT-2002
SHEET	29 of 57


GPIO55
R1031 1K_5%_2_DY
GPIO55 : TOP-BLOCK SWAP OVERRIDE
LOW=A16 SWAP OVERRIDE
HIGH=DEFAULT
BBSTRAP0
R875 1K_5%_2_DY
BBSTRAP1
R1029 1K_5%_2_DY
DGPU_PWM_SELECT#
R999 1K_5%_2_DY
BBSTRAP1 BBSTRAP0 BOOT BIOS
0 0 LPC
0 1 Reserved (NAND)
1 0 --
1 1 SPI
P3V3S
DGPU_HOLD_RST#
DGPU_SELECT#
DGPU_PWR_EN#
USB30_SMI#
ACCEL_INT#
GPIO3
GPIO4
P3V3A
GPIO59
2ND_WWAN_GPS_OFF#
BOARD_ID0
BOARD_ID1
BOARD_ID2
BOARD_ID3
BOARD_ID4
BOARD_ID5
BOARD_ID5 ONLY FOR WEBCAN USE
FOR HD WEB CAM BOARD_ID5 PULL P3V3A
FOR VGA WEB CAM BOARD_ID5 PULL GND
ID5 ID4 ID3 ID2 ID1 ID0
UMA-INTEL 1 0 0 0 0 0
SG-SEYMOUR 1 0 0 0 1 0
SG-THAMES 1 0 0 0 1 0
U519
RSVD
NVRAM
PCI
USB
ITL_PANTHERPOINT_FCBGA_989P
USB3_P1_RX_DN
USB3_P1_RX_DP
USB3_P1_TX_DN
USB3_P1_TX_DP
USB_P0_DN
USB_P0_DP
USB_P1_DN
USB_P1_DP
USB3.0
USB2.0 DB (DeBug Port)
USB_P5_DN
USB_P5_DP
WEBCAM
USB_P8_DN
USB_P8_DP
USB_P9_DN
USB_P9_DP
WLAN COMBO
USB2.0 DB (DeBug Port)
R951
WITHIN 500 MILS
OF THE PCH
CLOSE TO PCH
R951 22.6_1%_2
PCH_USBBIAS
PCI_INTA#
PCI_INTB#
PCI_INTC#
PCI_INTD#
PCH_PME#
PLT_RST#
CLK_LPC_EC
CLKIN_PCI_FB
CLK_LPC_DEBUG
SSM3K7002FU
Q555
DGPU_PWR_EN
C1005 0.1uF_16V_2
U527
BUF_PLT_RST#
TC7SZ08FU
R1064 100K_5%_2
INVENTEC
TITLE
MODEL,PROJECT,FUNCTION
PCH - 5
SIZE A3
CODE CS
DOC.NUMBER 1310xxxxx-0-0
REV X01
CHANGE by XXX
DATE 21-OCT-2002
SHEET 30 of 57



INVENTEC	
TITLE	MODEL,PROJECT,FUNCTION PCH - 6
SIZE A3	CODE CS
DOC.NUMBER	1310xxxxx-0-0
REV	X01
CHANGE by	XXX
DATE	21-OCT-2002
SHEET	31 of 57

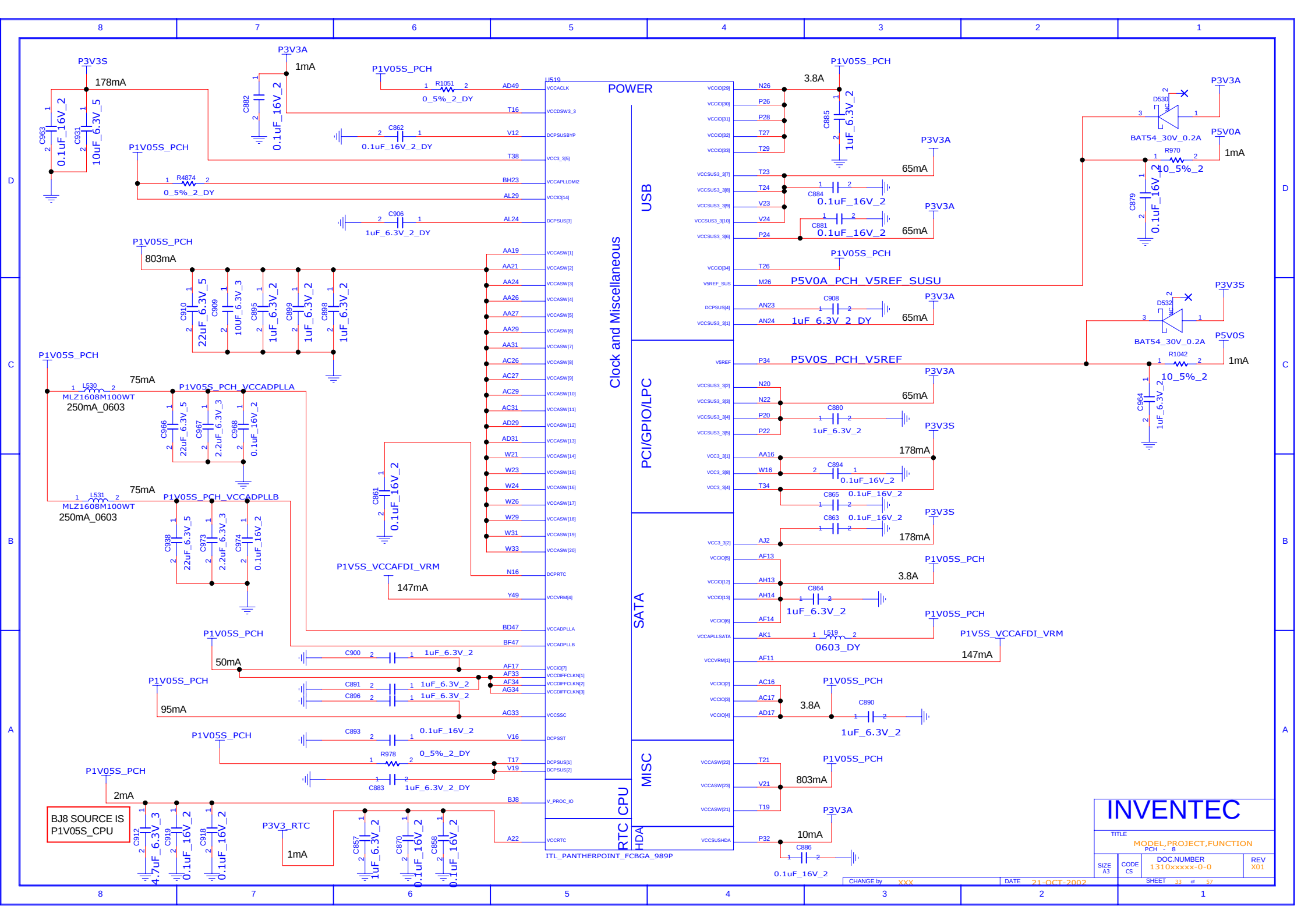


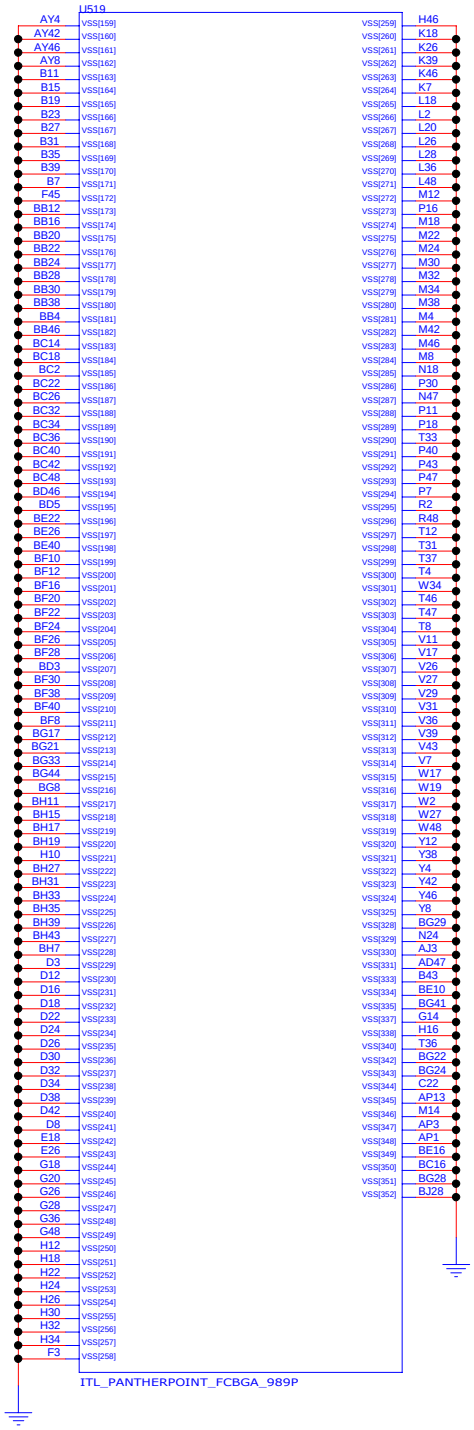
INVENTEC

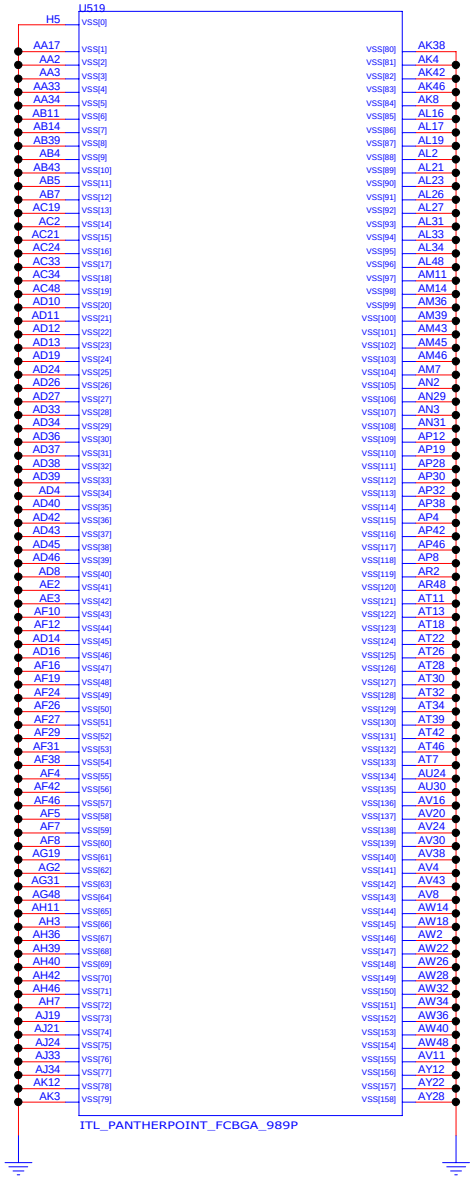
TITLE: MODEL,PROJECT,FUNCTION
PCH - 7

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

CHANGE by XXX | DATE 21-OCT-2002 | SHEET 32 of 57


P3V3S
178mA
P3V3A
1mA
P1V05S_PCH
P1V05S_PCH
803mA
P1V05S_PCH
75mA
P1V05S_PCH_VCCADPLLA
P1V05S_PCH
75mA
P1V05S_PCH_VCCADPLLB
P1V05S_PCH
50mA
P1V05S_PCH
95mA
P1V05S_PCH
P1V05S_PCH
2mA
BJ8 SOURCE IS
P1V05S_CPU
P3V3_RTC
1mA
P1V5S_VCCAFDI_VRM
147mA
POWER
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
MISC
CPU
RTC
HDA
ITL_PANTHERPOINT_FCBGA_989P
P1V05S_PCH
3.8A
P3V3A
65mA
P1V05S_PCH
P5V0A_PCH_V5REF_SUSU
P3V3A
65mA
P1V05S_PCH
P5V0A_PCH_V5REF
P3V3A
65mA
P3V3S
178mA
P3V3S
178mA
P1V05S_PCH
3.8A
P1V05S_PCH
P1V5S_VCCAFDI_VRM
147mA
P1V05S_PCH
3.8A
P1V05S_PCH
803mA
P3V3A
10mA
P3V3A
P5V0A
1mA
P3V3S
P5V0S
1mA
BAT54_30V_0.2A
BAT54_30V_0.2A
INVENTEC
TITLE
MODEL,PROJECT,FUNCTION
PCH - 8
SIZE A3
CODE CS
DOC.NUMBER 1310xxxxx-0-0
REV X01
CHANGE by XXX
DATE 21-OCT-2002
SHEET 33 of 57





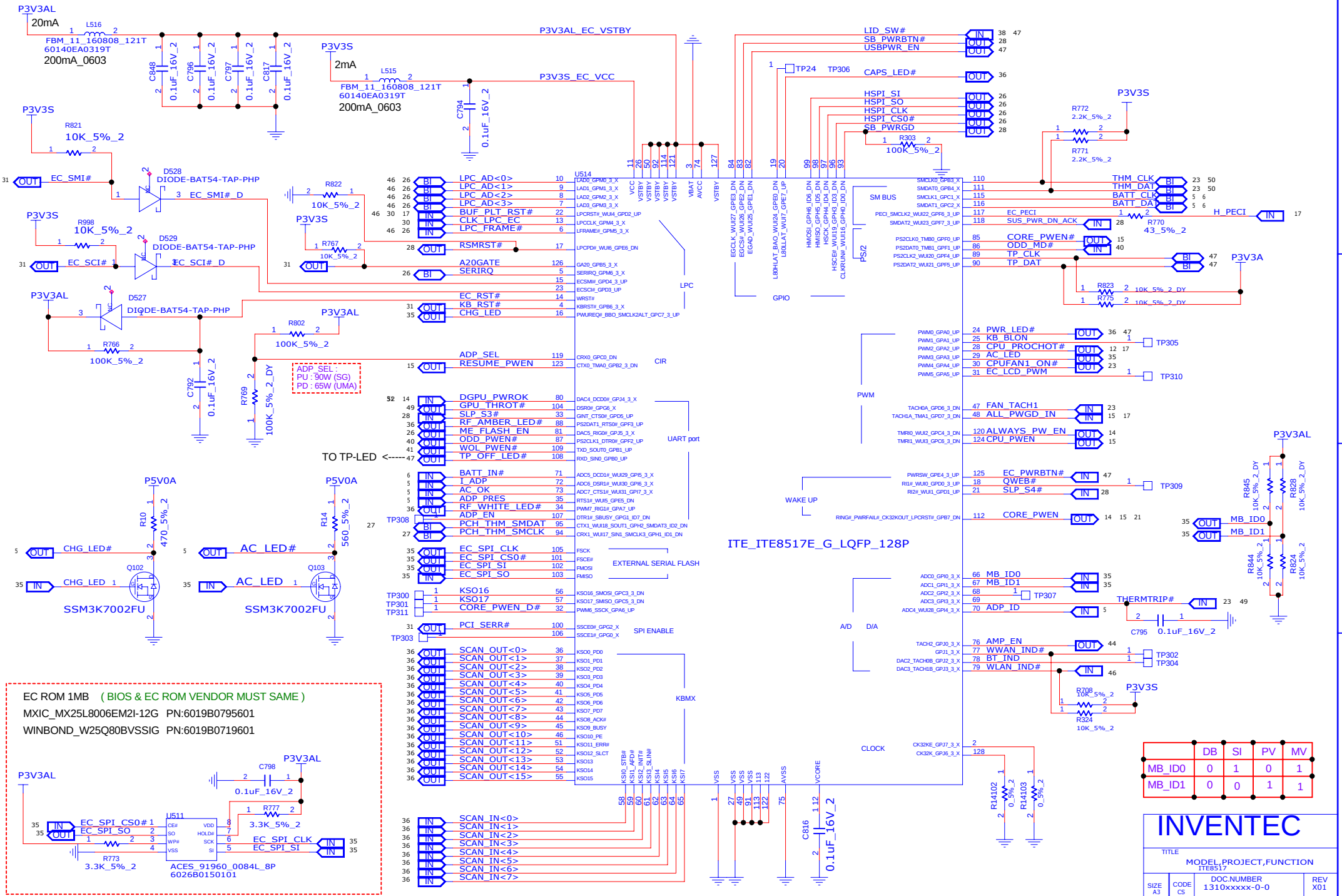
INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
PCH - 9

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 34 of 57

CHANGE by XXX DATE 21-OCT-2002


P3V3AL
20mA
L516
FBM_11_160808_121T
60140EA0319T
200mA_0603
P3V3AL_EC_VSTBY
P3V3S
2mA
L515
FBM_11_160808_121T
60140EA0319T
200mA_0603
P3V3S_EC_VCC
C848 0.1uF_16V_2
C796 0.1uF_16V_2
C797 0.1uF_16V_2
C817 0.1uF_16V_2
C794 0.1uF_16V_2
R821 10K_5%_2
D528 DIODE-BAT54-TAP-PHP
EC_SMI#
EC_SMI#_D
R998 10K_5%_2
D529 DIODE-BAT54-TAP-PHP
EC_SCI#
EC_SCI#_D
D527 DIODE-BAT54-TAP-PHP
R766 100K_5%_2
C792 0.1uF_16V_2
R822 10K_5%_2
R767 10K_5%_2
R802 100K_5%_2
R769 100K_5%_2_DY
ADP_SEL :
PU : 90W (SG)
PD : 65W (UMA)
U514
LPC_AD<0>
LPC_AD<1>
LPC_AD<2>
LPC_AD<3>
BUF_PLT_RST#
CLK_LPC_EC
LPC_FRAME#
RSMRST#
A20GATE
SERIRQ
EC_RST#
KB_RST#
CHG_LED
ADP_SEL
RESUME_PWEN
LPC
CIR
DGPU_PWROK
GPU_THROT#
SLP_S3#
RF_AMBER_LED#
ME_FLASH_EN
ODD_PWEN#
WOL_PWEN#
TP_OFF_LED#
UART port
TO TP-LED <-----
BATT_IN#
I_ADP
AC_OK
ADP_PRES
RF_WHITE_LED#
ADP_EN
PCH_THM_SMDAT
PCH_THM_SMCLK
EXTERNAL SERIAL FLASH
EC_SPI_CLK
EC_SPI_CS0#
EC_SPI_SI
EC_SPI_SO
KSO16
KSO17
CORE_PWEN_D#
SPI ENABLE
PCI_SERR#
KBMX
SCAN_OUT<0>
SCAN_OUT<1>
SCAN_OUT<2>
SCAN_OUT<3>
SCAN_OUT<4>
SCAN_OUT<5>
SCAN_OUT<6>
SCAN_OUT<7>
SCAN_OUT<8>
SCAN_OUT<9>
SCAN_OUT<10>
SCAN_OUT<11>
SCAN_OUT<12>
SCAN_OUT<13>
SCAN_OUT<14>
SCAN_OUT<15>
SCAN_IN<0>
SCAN_IN<1>
SCAN_IN<2>
SCAN_IN<3>
SCAN_IN<4>
SCAN_IN<5>
SCAN_IN<6>
SCAN_IN<7>
P5V0A
R10 470_5%_2
R14 560_5%_2
CHG_LED#
CHG_LED
AC_LED#
AC_LED
Q102 SSM3K7002FU
Q103 SSM3K7002FU
EC ROM 1MB (BIOS & EC ROM VENDOR MUST SAME)
MXIC_MX25L8006EM2I-12G PN:6019B0795601
WINBOND_W25Q80BVSSIG PN:6019B0719601
U511
ACES_91960_0084L_8P
6026B0150101
C798 0.1uF_16V_2
R777 3.3K_5%_2
R773 3.3K_5%_2
LID_SW#
SB_PWRBTN#
USBPWR_EN
CAPS_LED#
HSPI_SI
HSPI_SO
HSPI_CLK
HSPI_CS0#
SB_PWRGD
R303 100K_5%_2
TP24
TP306
SM BUS
PS/2
GPIO
R772 2.2K_5%_2
R771 2.2K_5%_2
THM_CLK
THM_DAT
BATT_CLK
BATT_DAT
H_PECI
R770 43_5%_2
EC_PECI
SUS_PWR_DN_ACK
CORE_PWEN#
ODD_MD#
TP_CLK
TP_DAT
R823 10K_5%_2_DY
R775 10K_5%_2_DY
PWM
PWR_LED#
KB_BLON
CPU_PROCHOT#
AC_LED
CPUFAN1_ON#
EC_LCD_PWM
TP305
TP310
FAN_TACH1
ALL_PWGD_IN
ALWAYS_PW_EN
CPU_PWEN
WAKE UP
EC_PWRBTN#
QWEB#
SLP_S4#
TP309
CORE_PWEN
ITE_ITE8517E_G_LQFP_128P
A/D
D/A
MB_ID0
MB_ID1
THERMTRIP#
ADP_ID
TP307
C795 0.1uF_16V_2
AMP_EN
WWAN_IND#
BT_IND
WLAN_IND#
TP302
TP304
R708 10K_5%_2
R324 10K_5%_2
CLOCK
R14102 0_5%_2
R14103 0_5%_2
C816 0.1uF_16V_2
R845 10K_5%_2_DY
R828 10K_5%_2_DY
R844 10K_5%_2
R824 10K_5%_2
DB SI PV MV
MB_ID0 0 1 0 1
MB_ID1 0 0 1 1
INVENTEC
TITLE
MODEL,PROJECT,FUNCTION
ITE8517
SIZE A3
CODE CS
DOC.NUMBER 1310xxxxx-0-0
REV X01
CHANGE by XXX
DATE 21-OCT-2002
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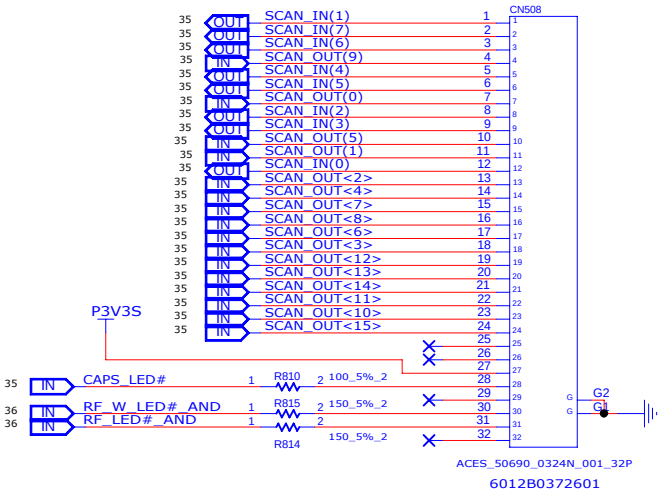
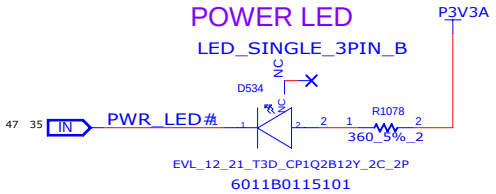
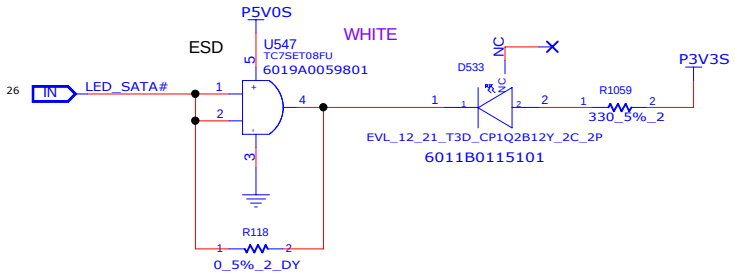
KeyBoard CONN(30 pin)



POWER LED

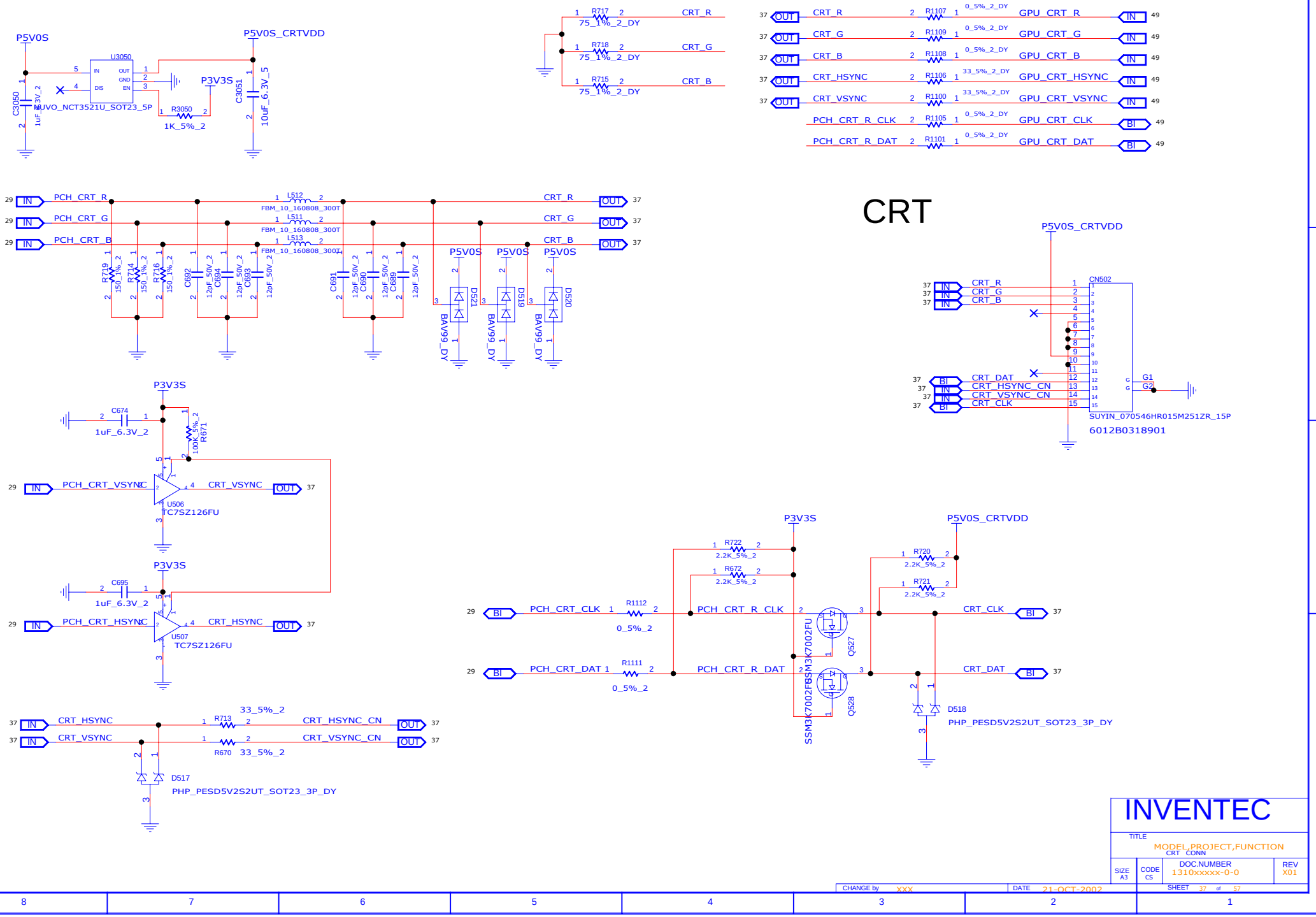


SATA LED & HDD HALTED LED



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION — KB CONN & LED			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX	DATE 21-OCT-2002	SHEET 36 of 57	


P5V0S
P5V0S_CRTVDD
U3050
SUYO_NCT3521U_SOT23_5P
C3050
1uF_3V_2
R3050
1K_5%_2
P3V3S
C3051
10uF_6.3V_5
CRT_R
CRT_G
CRT_B
R717
R718
R715
75_1%_2_DY
GPU_CRT_R
GPU_CRT_G
GPU_CRT_B
GPU_CRT_HSYNC
GPU_CRT_VSYNC
GPU_CRT_CLK
GPU_CRT_DAT
R1107
R1109
R1108
R1106
R1100
R1105
R1101
0_5%_2_DY
33_5%_2_DY
PCH_CRT_R_CLK
PCH_CRT_R_DAT
PCH_CRT_R
PCH_CRT_G
PCH_CRT_B
L512
L511
L513
FBM_10_160808_300T
R719
R714
R716
150_1%_2
C692
C694
C693
C691
C690
C689
12pF_50V_2
D521
D519
D520
BAV99_DY
CRT
CN502
SUYIN_070546HR015M251ZR_15P
6012B0318901
CRT_DAT
CRT_HSYNC_CN
CRT_VSYNC_CN
CRT_CLK
G1
G2
C674
C695
1uF_6.3V_2
R671
100K_5%_2
PCH_CRT_VSYNC
CRT_VSYNC
U506
TC7SZ126FU
PCH_CRT_HSYNC
CRT_HSYNC
U507
R713
R670
33_5%_2
CRT_HSYNC_CN
CRT_VSYNC_CN
D517
PHP_PESD5V2S2UT_SOT23_3P_DY
R722
R672
2.2K_5%_2
R720
R721
R1112
R1111
0_5%_2
PCH_CRT_CLK
PCH_CRT_DAT
PCH_CRT_R_CLK
PCH_CRT_R_DAT
SSM3K7002FU
Q527
Q528
D518
PHP_PESD5V2S2UT_SOT23_3P_DY
INVENTEC
TITLE
MODEL,PROJECT,FUNCTION
CRT_CONN
SIZE
A3
CODE
CS
DOC.NUMBER
1310xxxxx-0-0
REV
X01
CHANGE by
XXX
DATE
21-OCT-2002
SHEET
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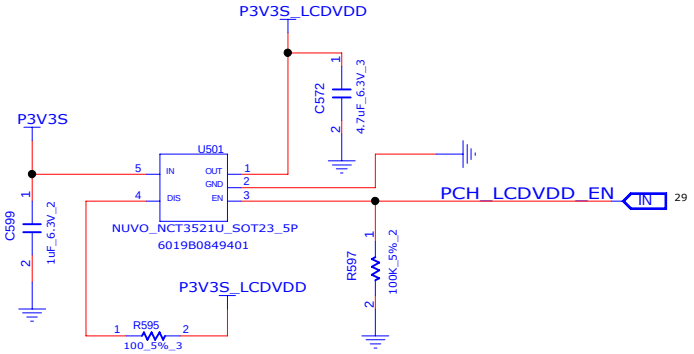
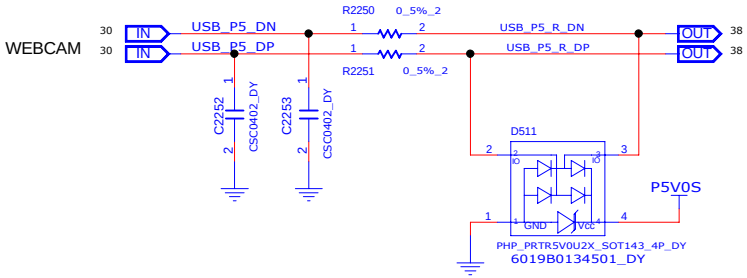
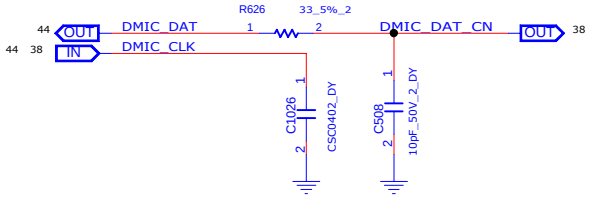
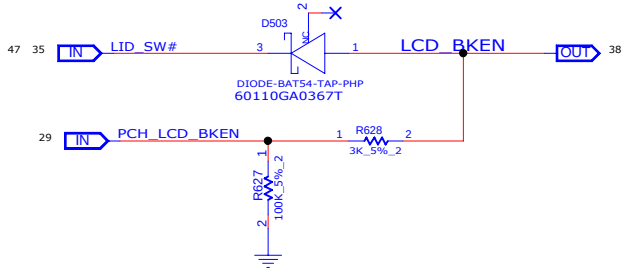
LCM

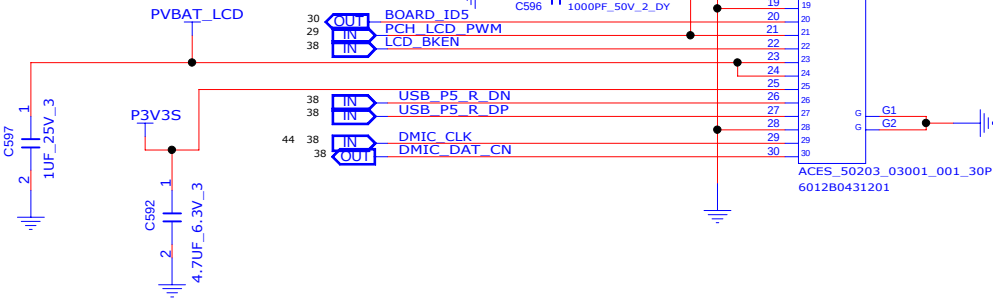


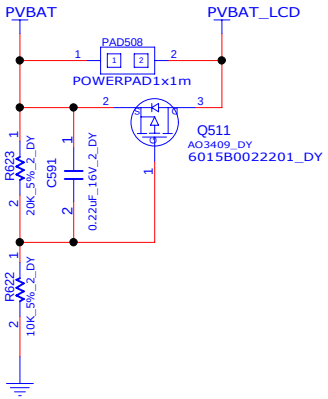






BOARD_ID5 ONLY FOR WEBCAN USE
FOR HD WEB CAM BOARD_ID5 PULL P3V3A
FOR VGA WEB CAM BOARD_ID5 PULL GND





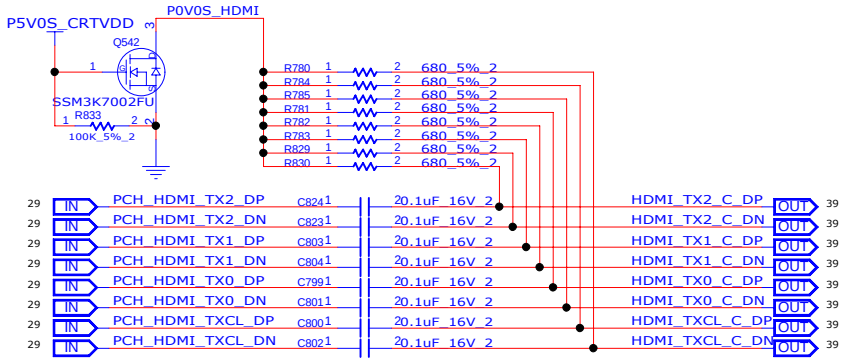
INVENTEC

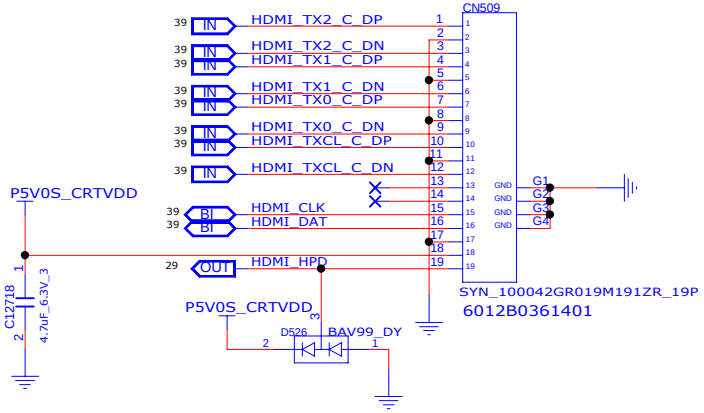
TITLE
MODEL_PROJECT,FUNCTION
LCD_CONN

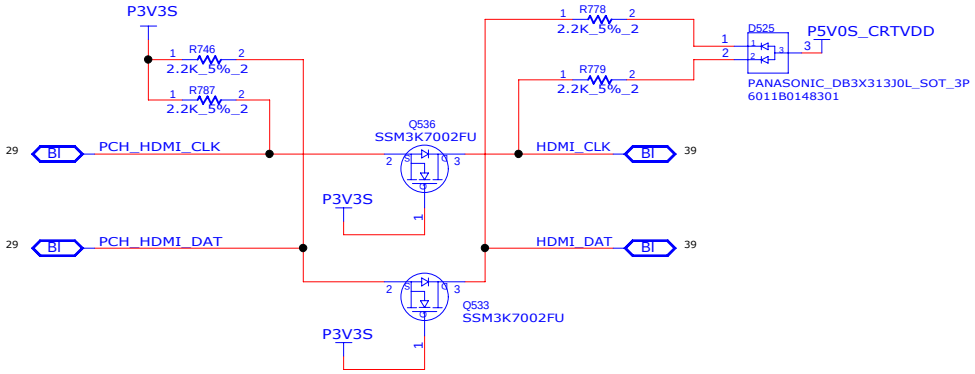
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

CHANGE by XXX | DATE 21-OCT-2002 | SHEET 38 of 57

HDMI







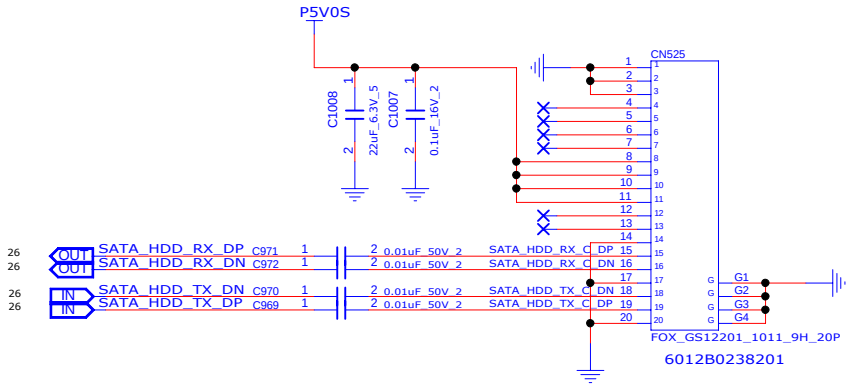
INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
HDMI_CONN

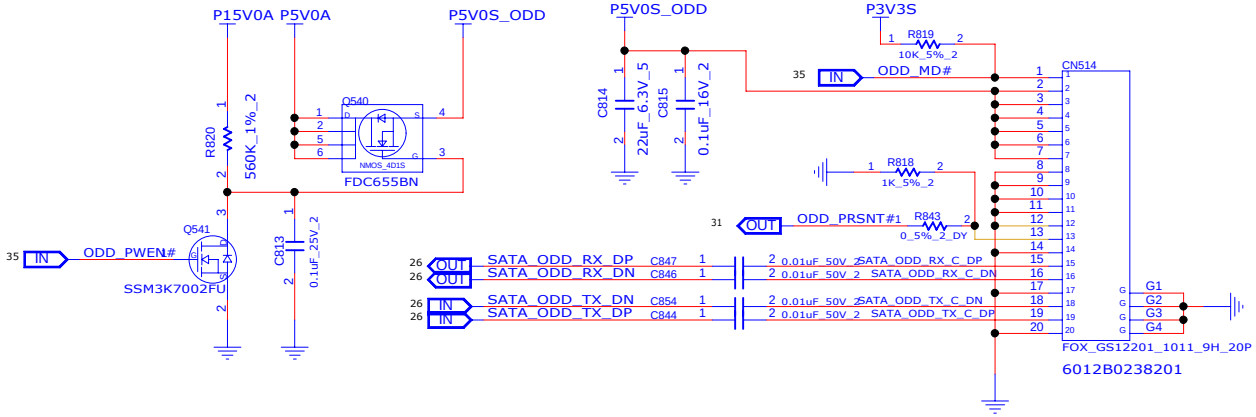
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

CHANGE by XXX DATE 21-OCT-2002 SHEET 39 of 57

SATA HDD CABLE CONN on MB



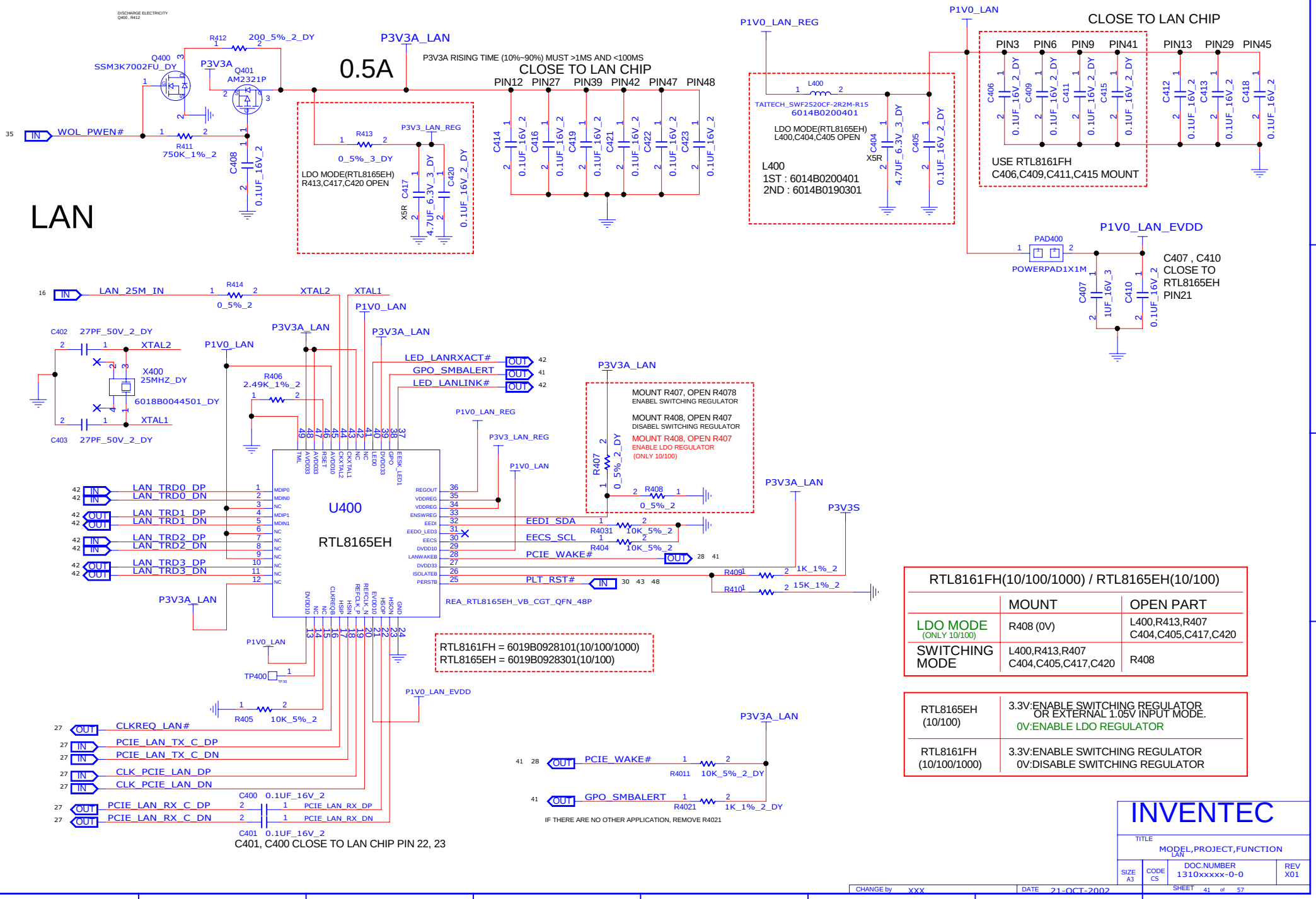
SATA ODD CABLE CONN on MB



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION — SATA_HDD & SATA_ODD			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX	DATE 21-OCT-2002	SHEET 40 of 57	

LAN



RTL8161FH(10/100/1000) / RTL8165EH(10/100)		
	MOUNT	OPEN PART
LDO MODE (ONLY 10/100)	R408 (0V)	L400,R413,R407 C404,C405,C417,C420
SWITCHING MODE	L400,R413,R407 C404,C405,C417,C420	R408

RTL8165EH (10/100)	3.3V:ENABLE SWITCHING REGULATOR OR EXTERNAL 1.05V INPUT MODE. 0V:ENABLE LDO REGULATOR
RTL8161FH (10/100/1000)	3.3V:ENABLE SWITCHING REGULATOR 0V:DISABLE SWITCHING REGULATOR

INVENTEC

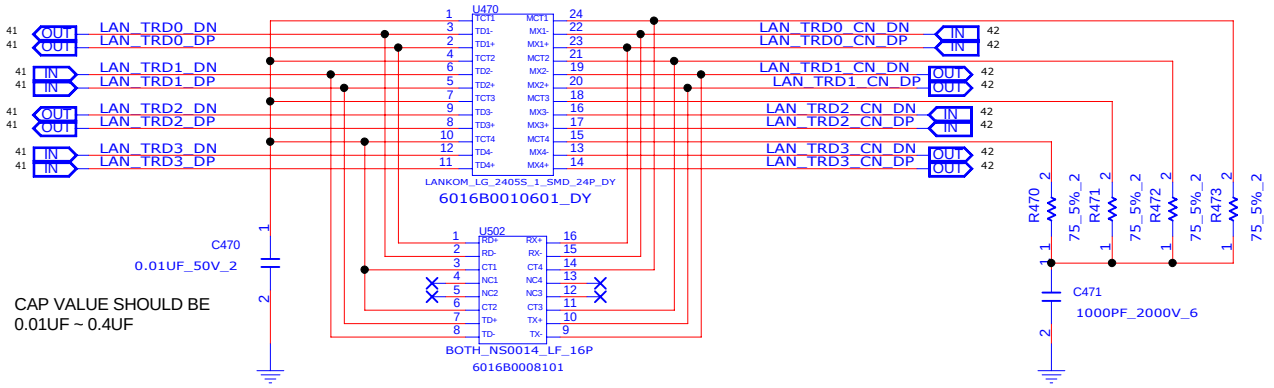
TITLE: MODEL,PROJECT,FUNCTION
LAN

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

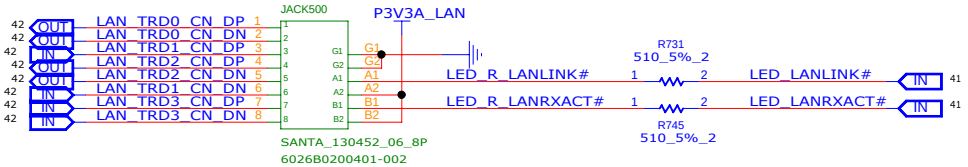
CHANGE by XXX DATE 21-OCT-2002 SHEET 41 of 57

TRANSFORMER

U470 FOR GIGALAN
U502 FOR 10/100 LAN



CAP VALUE SHOULD BE
0.01UF ~ 0.4UF

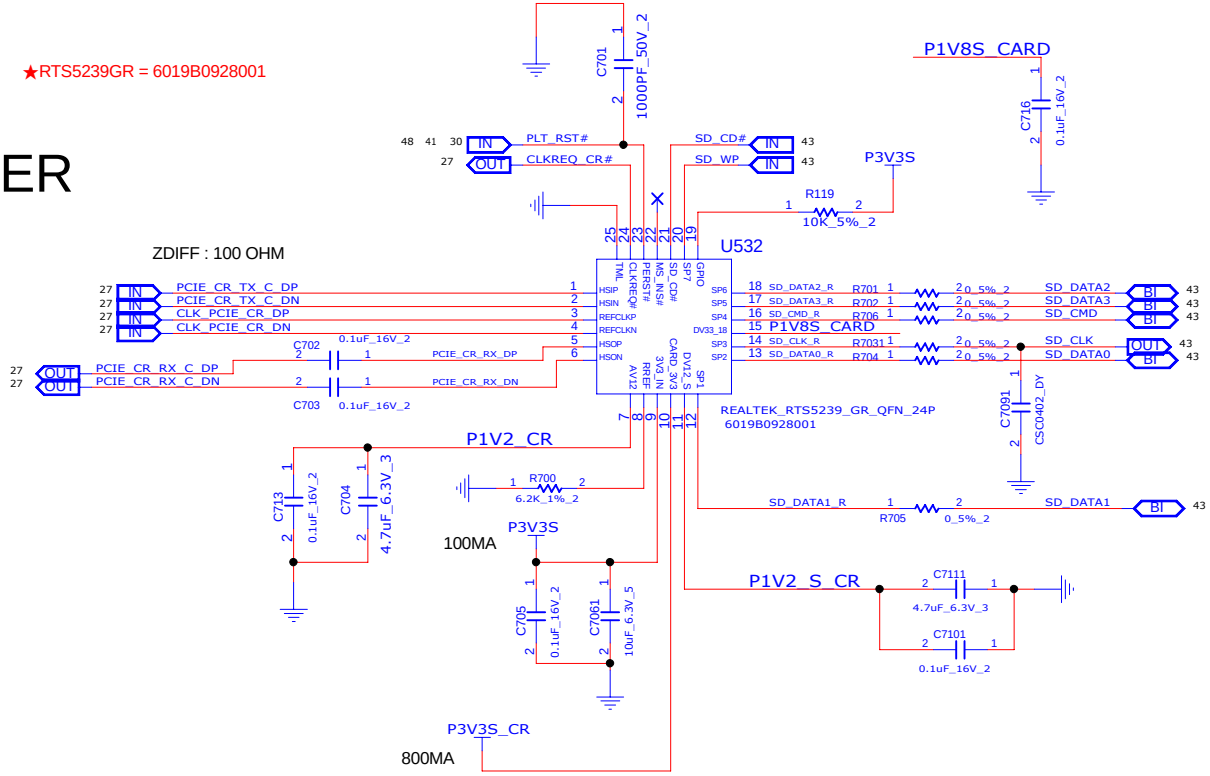


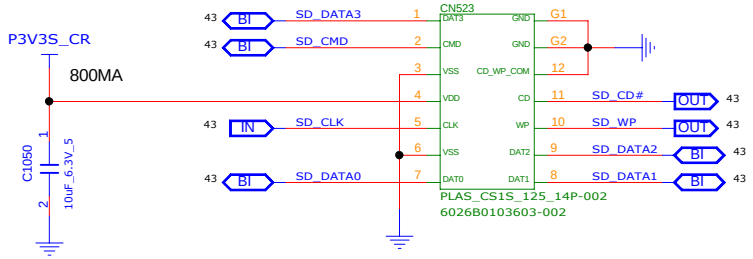
INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION RJ45 & TRANSFORMER			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX	DATE 21-OCT-2002	SHEET 42 of 57	

CARE READER

★RTS5239GR = 6019B0928001



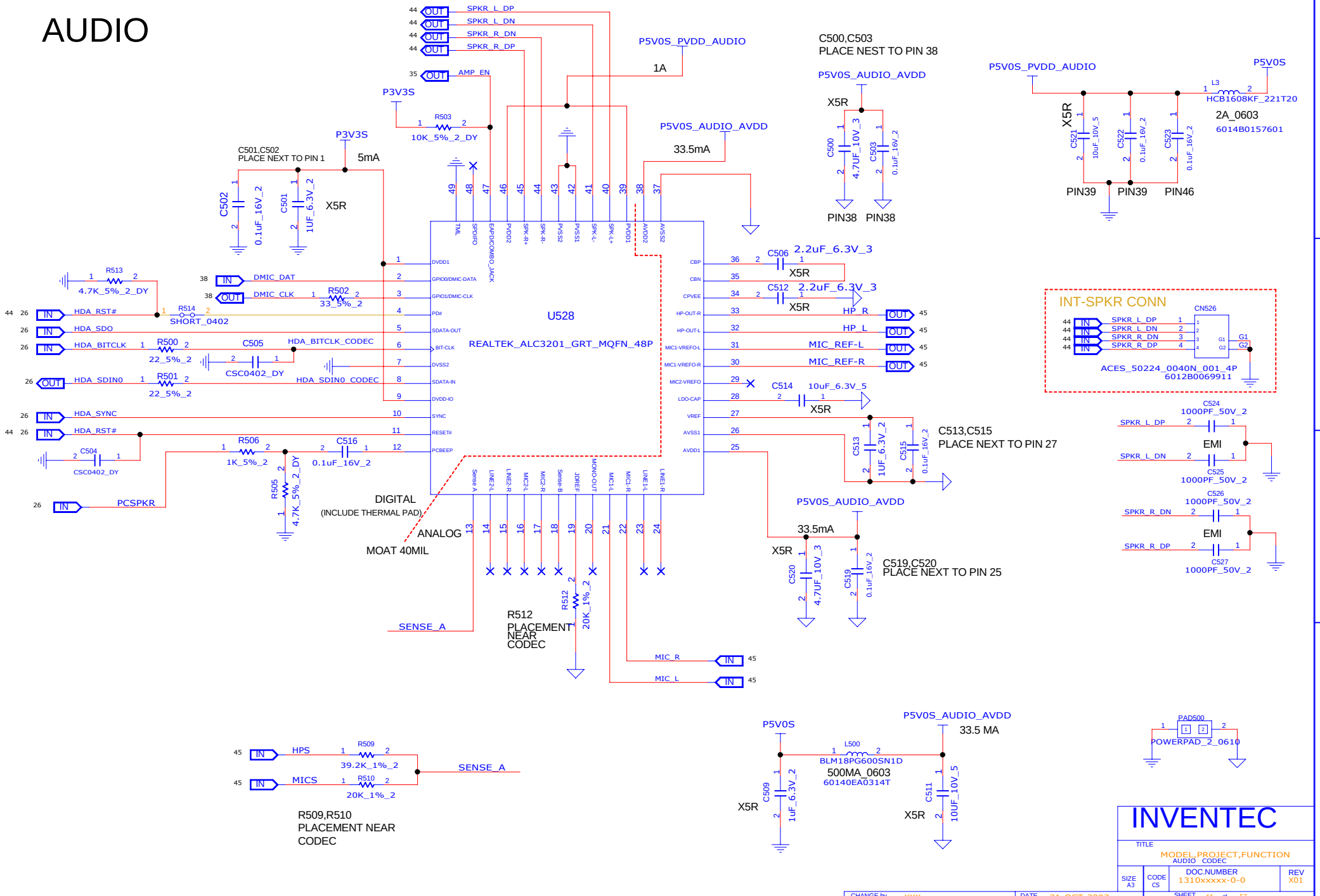


■ On chip 800ma MOSFET for direct power control of all types memory cards

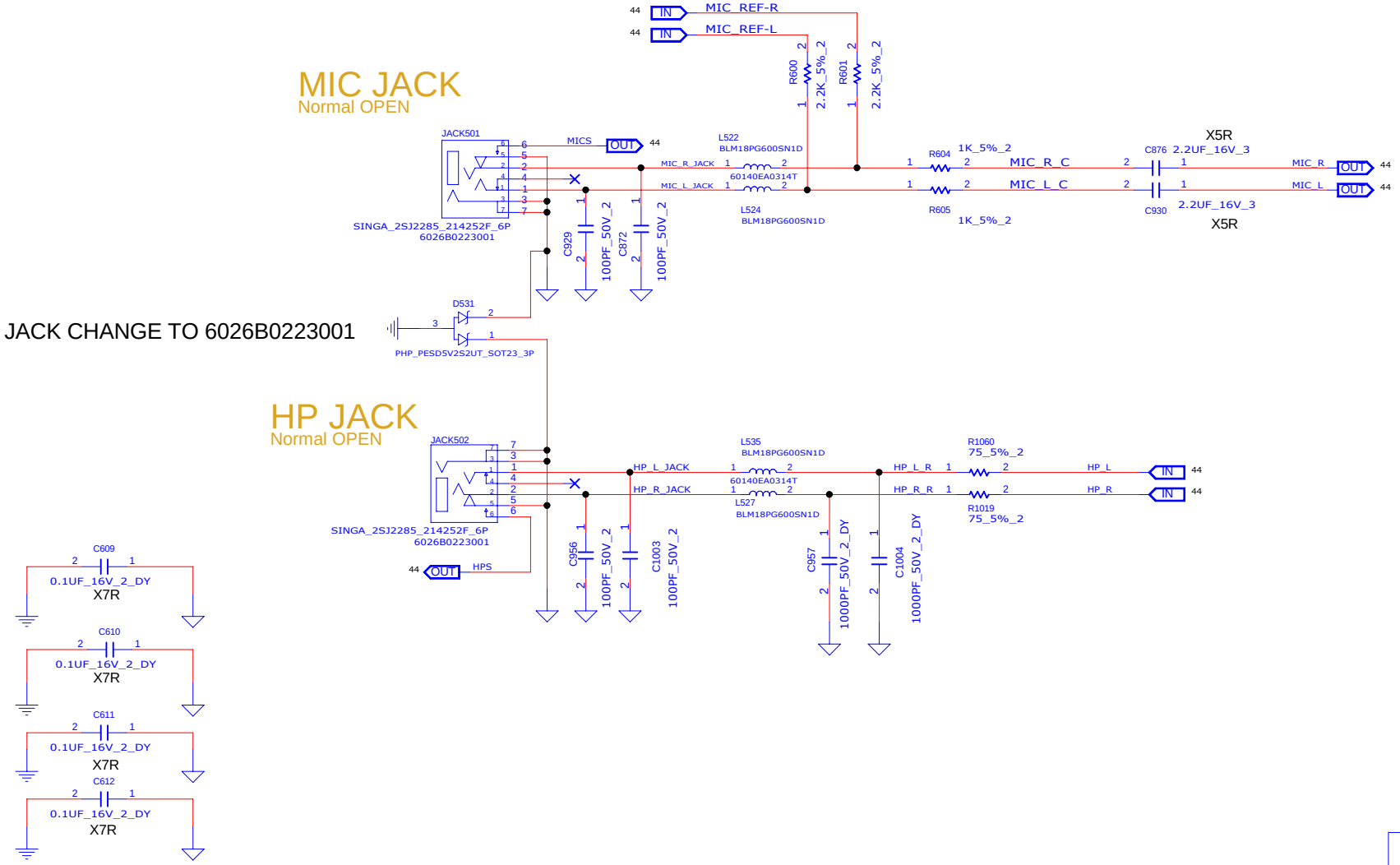
INVENTEC

TITLE: MODEL,PROJECT,FUNCTION CARD_READER			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX	DATE 21-OCT-2002	SHEET 43 of 57	

AUDIO



INVENTEC				
TITLE: MODEL,PROJECT,FUNCTION AUDIO CODEC				
SIZE: A3	CODE: CS	DOC.NUMBER: 1310xxxxx-0-0	REV: X01	
CHANGE by: XXX	DATE: 21-OCT-2002	SHEET: 44 of 57		



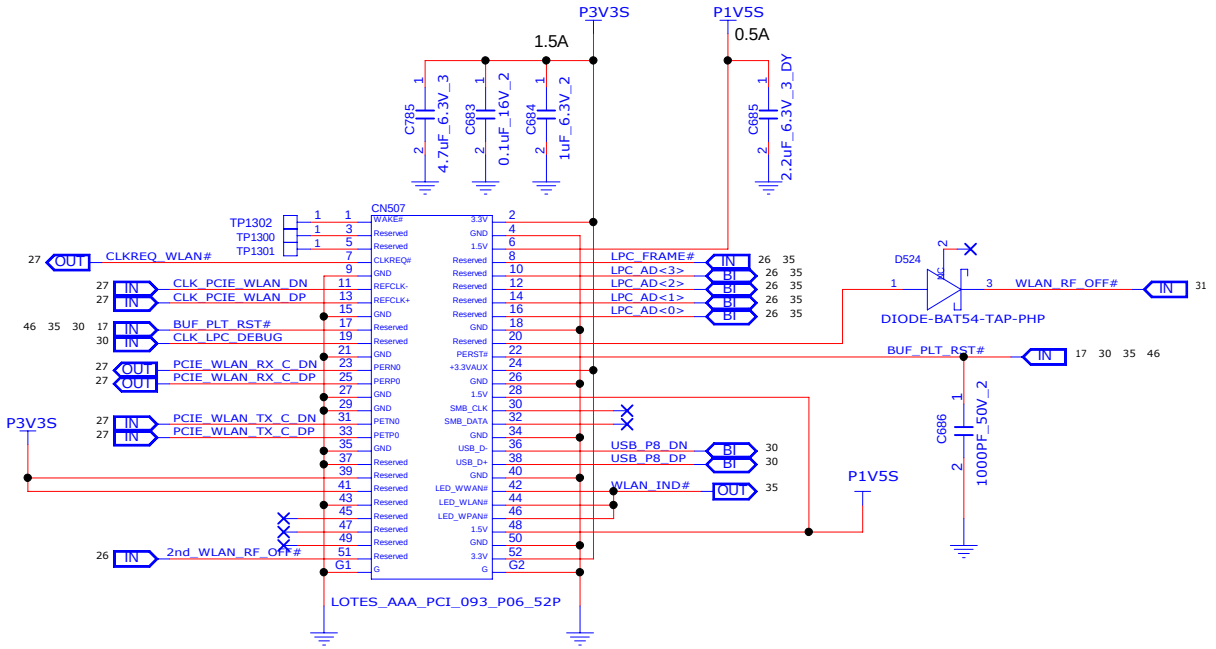
INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
HP JACK & MIC JACK

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

CHANGE by XXX | DATE 21-OCT-2002 | SHEET 45 of 57

WLAN CONN (MINICARD)



SI build change to 6026B0221502

	MARILYN	RIPPLE3
	ATHEROS	FOXCONN
	AR5B125	RALINK RT5390
VENDOR ID :	0X168C	0X1814
DEVICE ID :	0X0032	0X539A
(SSID) SUBSYSTEM ID :	0X1838	0X1839
SUBSYSTEM VENDOR ID :	0X103C	0X103C
HP P/N :	670036-001	670285-001

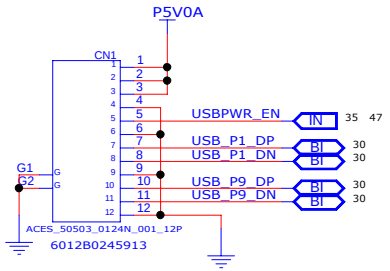
INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
WLAN & BT

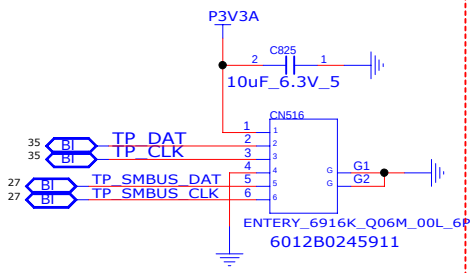
SIZE A3 | CODE CS | DOC.NUMBER 1310xxxxx-0-0 | REV X01

CHANGE by XXX | DATE 21-OCT-2002 | SHEET 46 of 57

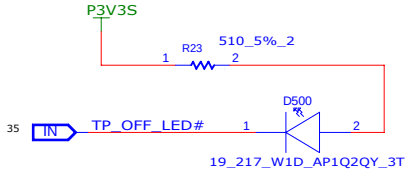
USB 2.0 BOARD Cable CONN on MB



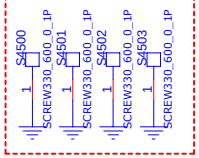
TouchPad Module CONN



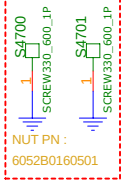
TOUCHPAD LED ON MB

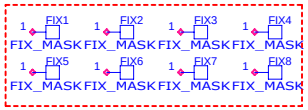


for CPU

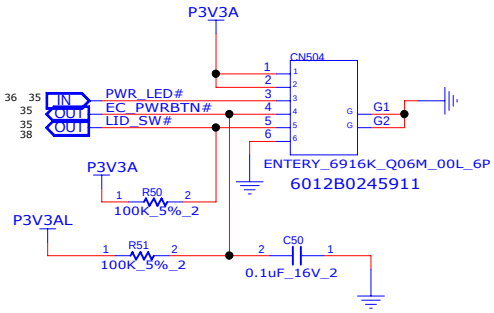


for GPU

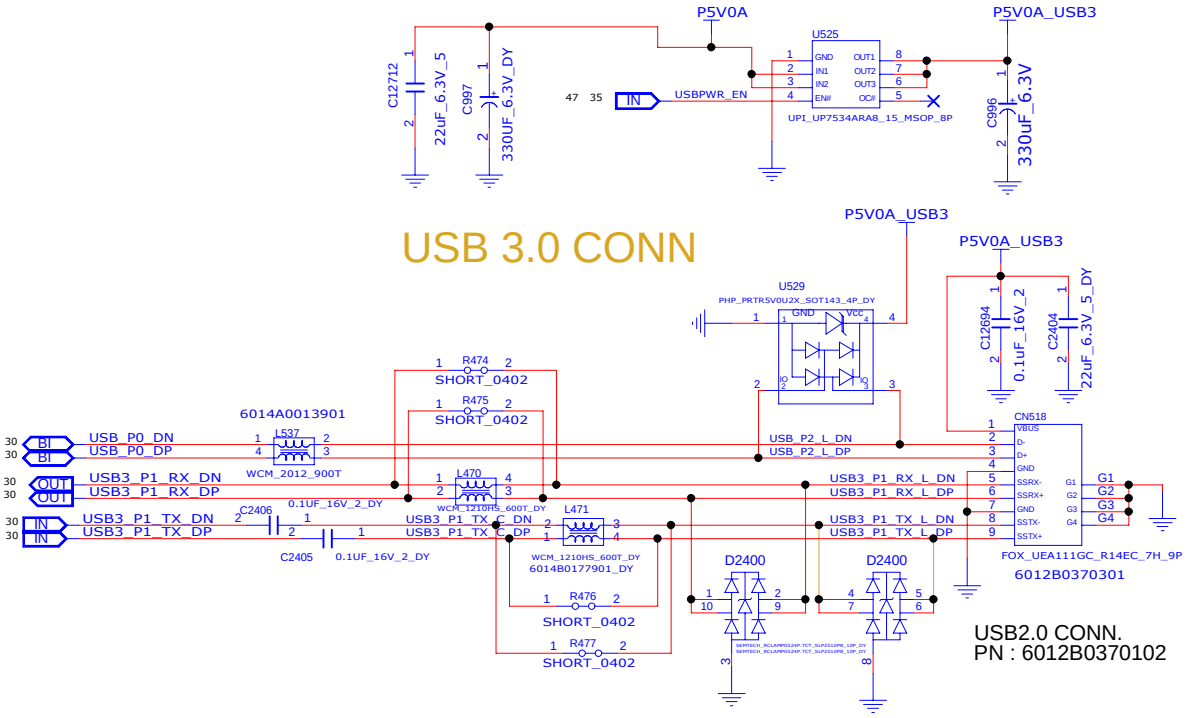




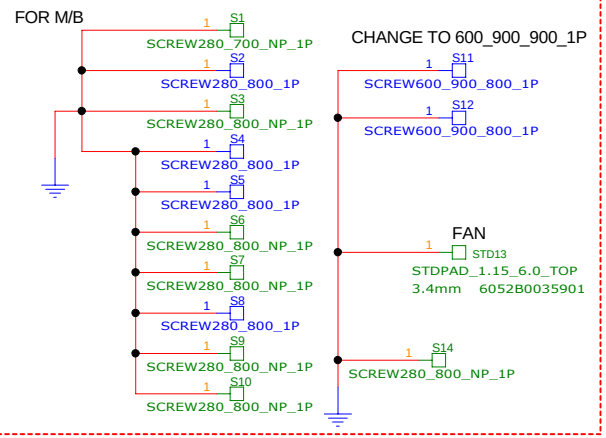
POWER BUTTON CONN ON MB



USB 3.0 CONN

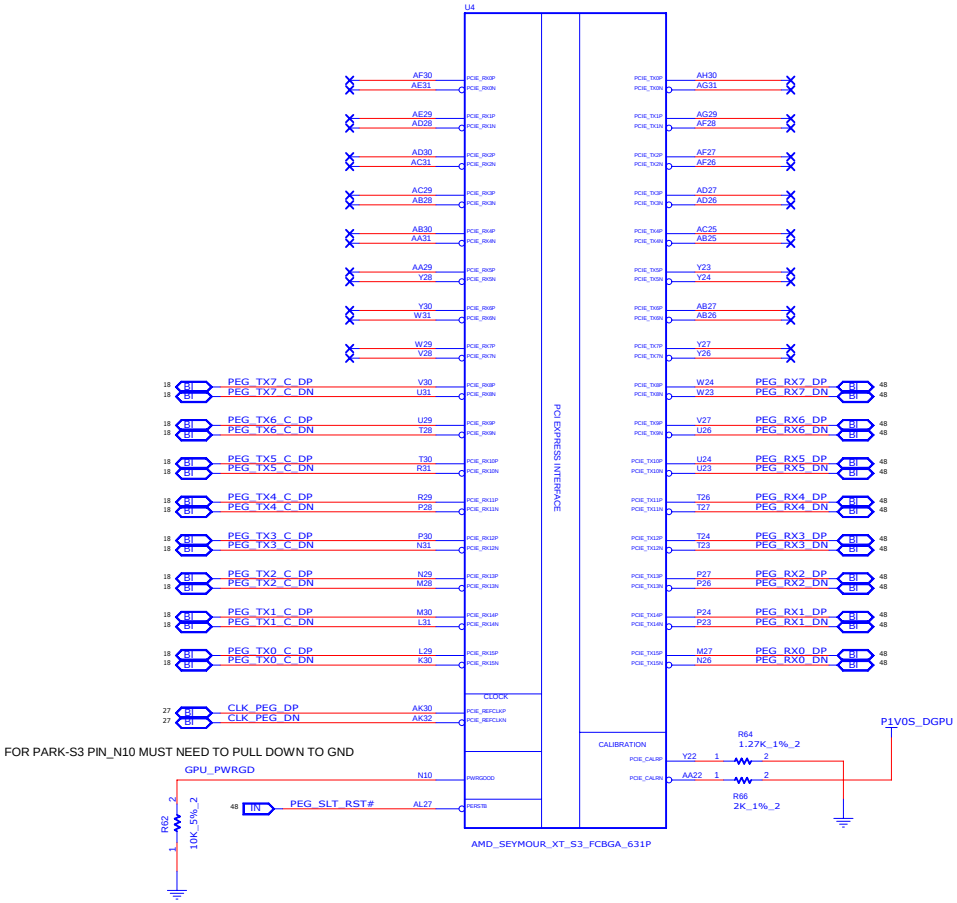


FOR M/B



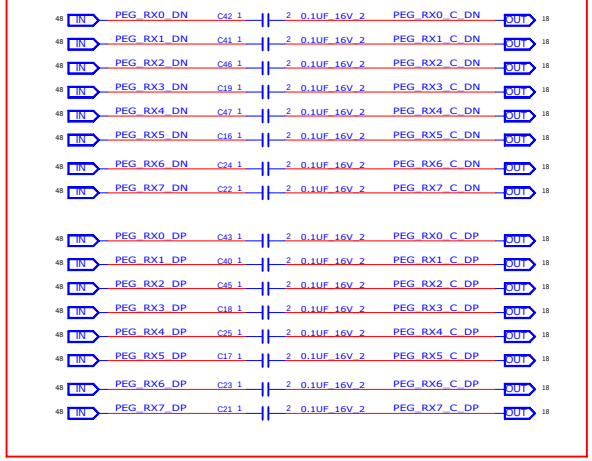
CHANGE TO 600_900_900_1P

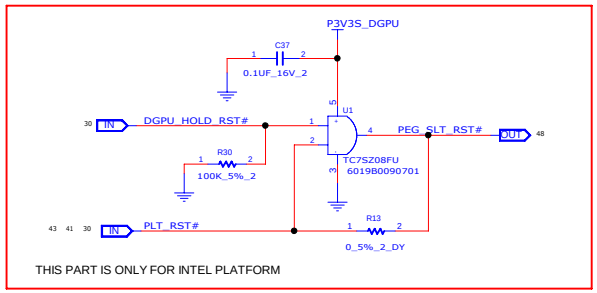
INVENTEC			
TITLE: MODEL,PROJECT,FUNCTION USB 3.0 CONN & M/B TO D/B CONN			
SIZE: A3	CODE: CS	DOC.NUMBER: 1310xxxxx-0-0	REV: X01
CHANGE by: XXX	DATE: 21-OCT-2002	SHEET 47 of 57	



FOR PARK-S3 PIN_N10 MUST NEED TO PULL DOWN TO GND

CLOSE TO GPU





THIS PART IS ONLY FOR INTEL PLATFORM

INVENTEC

MODEL,PROJECT,FUNCTION
SEYMOUR XT-S3

SIZE	CODE	DOC NUMBER	REV
C	CS	1310xxxxx-D-D	X01

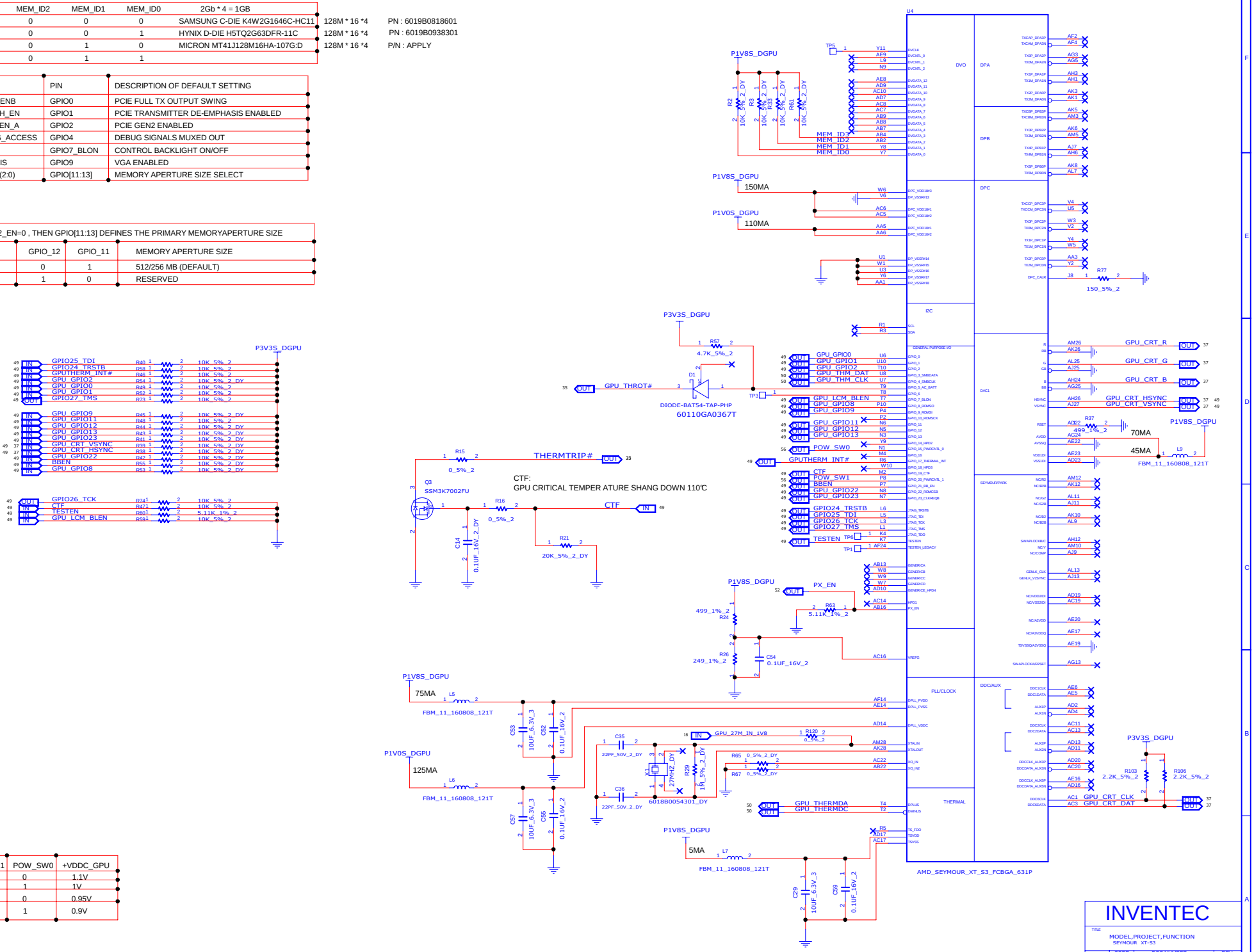
CHANGE by YXX DATE 21-OCT-2002 SHEET 48 of 57

MEM_ID3	MEM_ID2	MEM_ID1	MEM_ID0	2Gb * 4 = 1GB		
0	0	0	0	SAMSUNG C-DIE K4W2G1646C-HC11	128M * 16 *4	PN : 6019B0818601
0	0	0	1	HYNIX D-DIE H5TQ2G63DFR-11C	128M * 16 *4	PN : 6019B0938301
0	0	1	0	MICRON MT41J128M16HA-107G:D	128M * 16 *4	P/N : APPLY
0	0	1	1			

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTING
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED
BIF_GEN2_EN_A	GPIO2	PCIE GEN2 ENABLED
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS MUXED OUT
	GPIO7_BLON	CONTROL BACKLIGHT ON/OFF
BIF_VGA_DIS	GPIO9	VGA ENABLED
ROMIDCFG(2:0)	GPIO[11:13]	MEMORY APERTURE SIZE SELECT

IF GPIO_22_EN=0 , THEN GPIO[11:13] DEFINES THE PRIMARY MEMORYAPERTURE SIZE			
GPIO_13	GPIO_12	GPIO_11	MEMORY APERTURE SIZE
0	0	1	512/256 MB (DEFAULT)
1	1	0	RESERVED

POW_SW1	POW_SW0	+VDDC_GPU
0	0	1.1V
0	1	1V
1	0	0.95V
1	1	0.9V



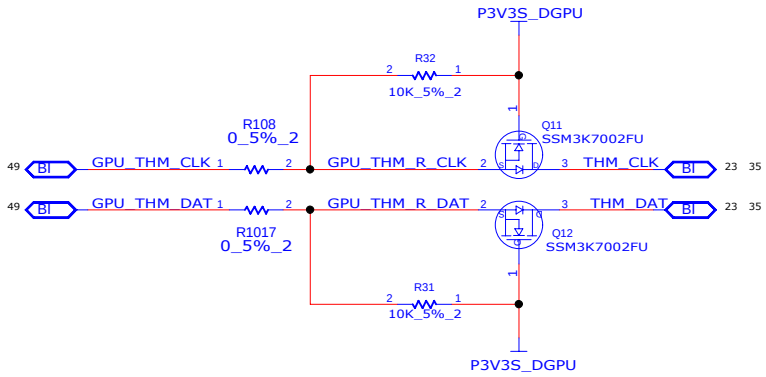
CHANGE by	XXX	DATE	21-OCT-2002		

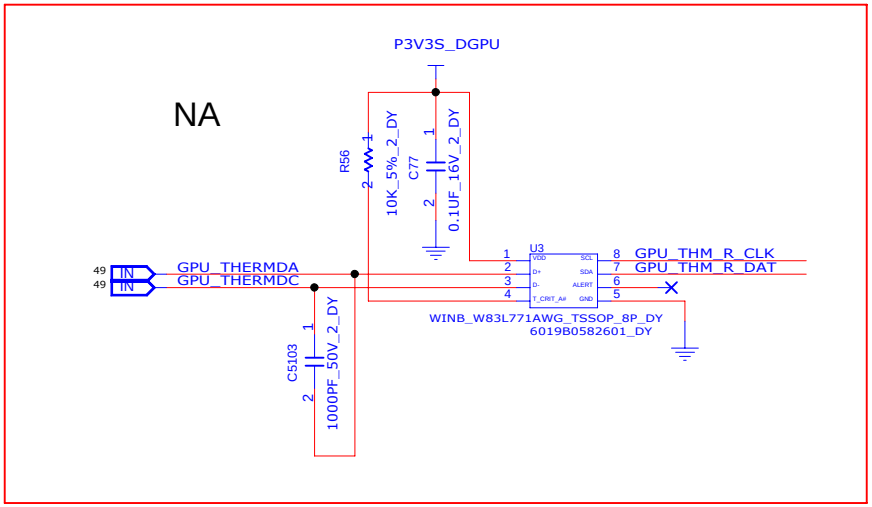
INVENTEC

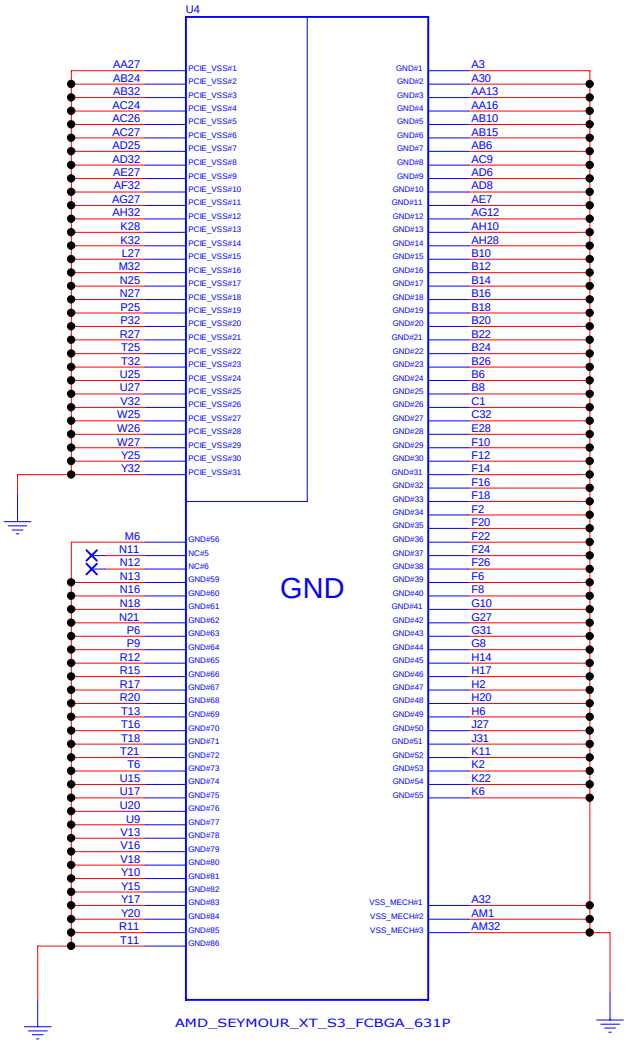
TITLE: MODEL,PROJECT,FUNCTION
SEYMOUR XT-S3

SIZE	CODE	DOC NUMBER	REV
C	CS	1310xxxxx-0-0	X01

SHEET 49 of 57

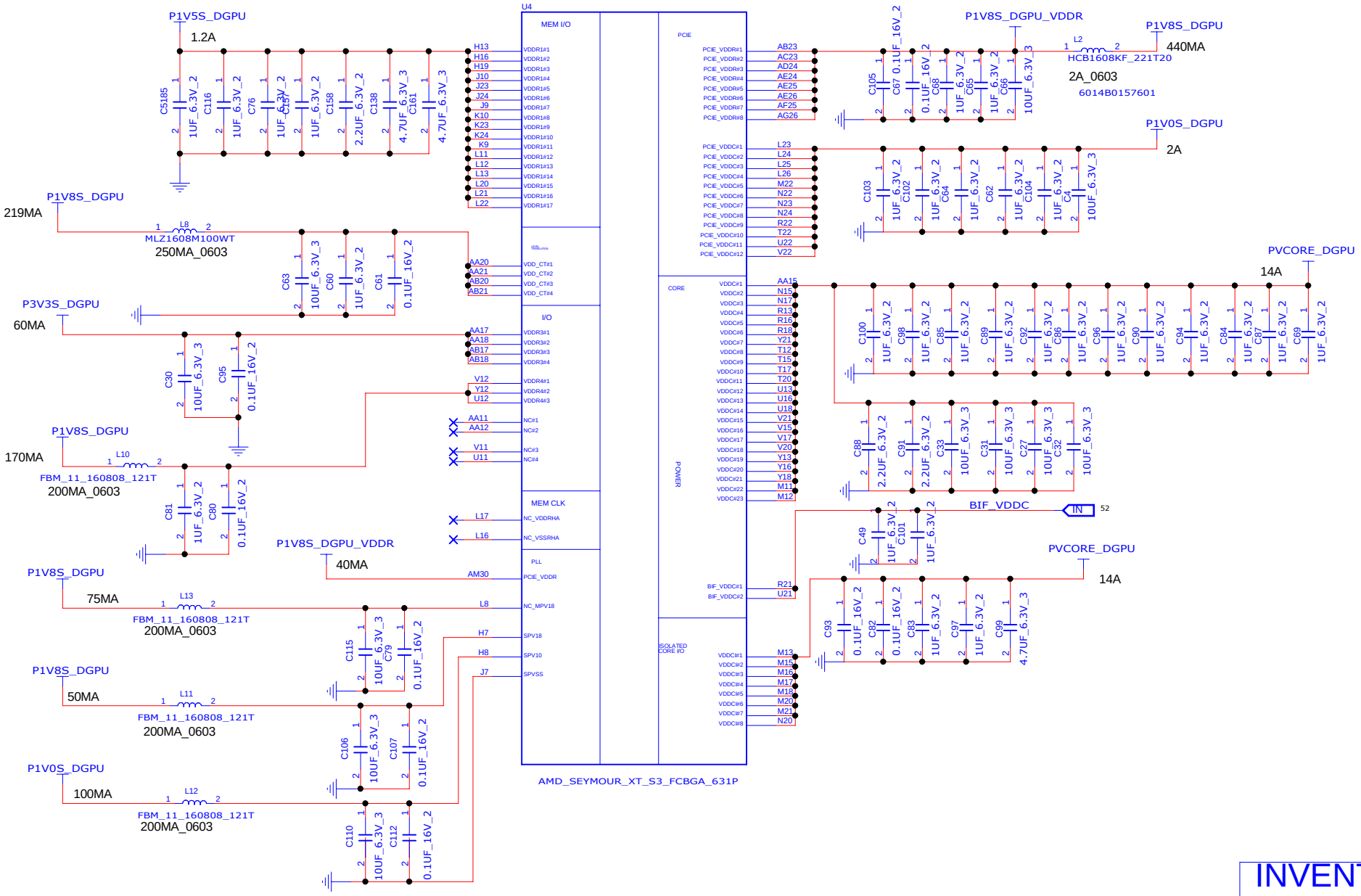






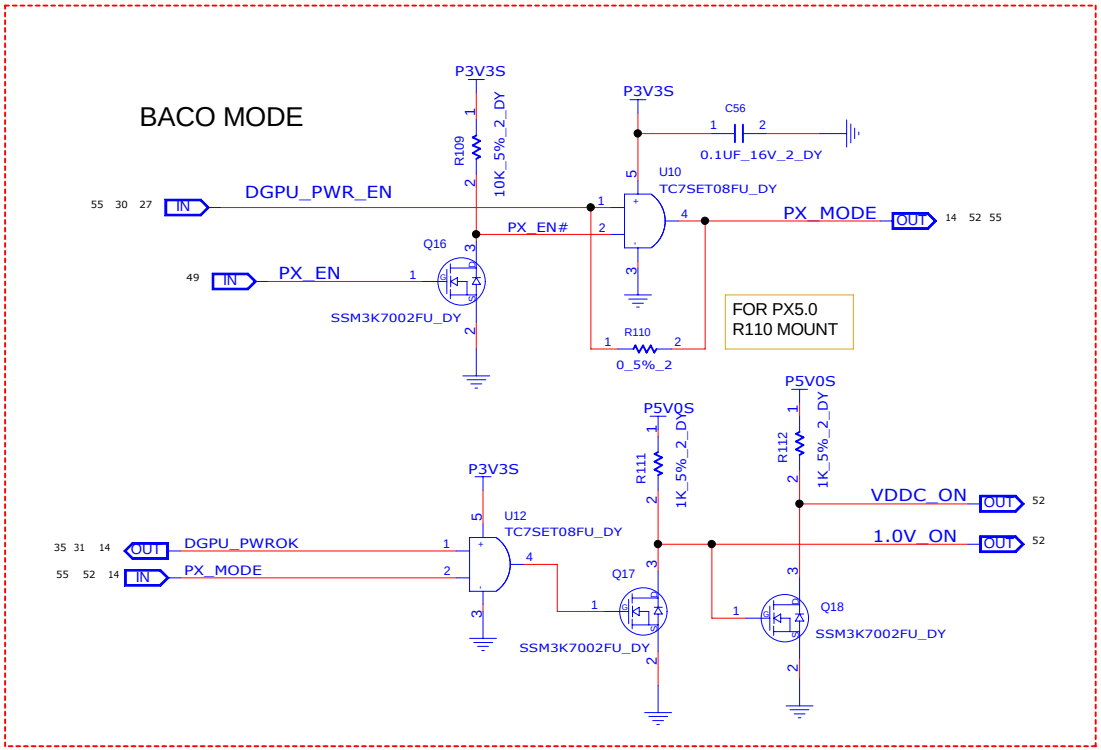
INVENTEC

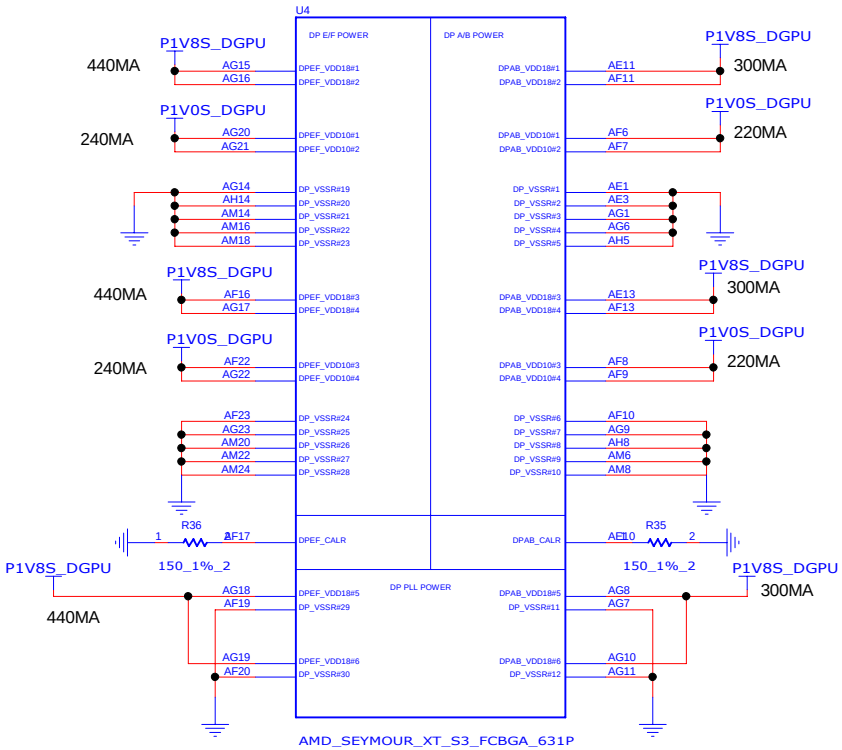
TITLE: MODEL,PROJECT,FUNCTION — SEYMOUR XT-S3			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX	DATE 21-OCT-2002	SHEET 50 of 57	



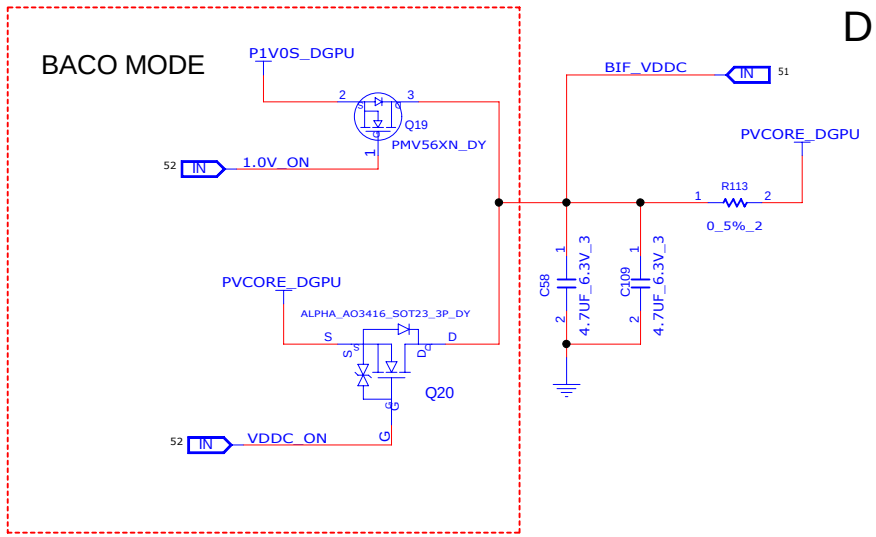
INVENTEC

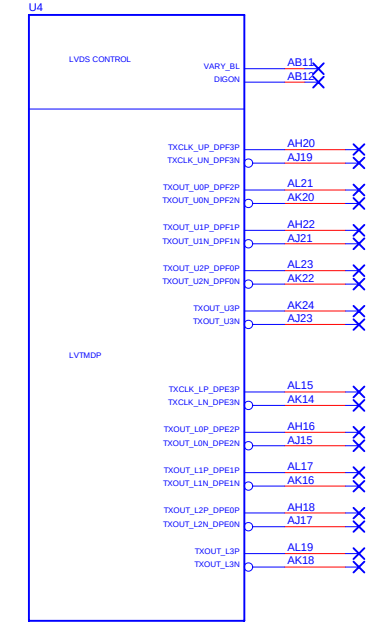
TITLE			
MODEL,PROJECT,FUNCTION SEYMOUR XT-S3			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX	DATE 21-OCT-2002	SHEET 51 of 57	





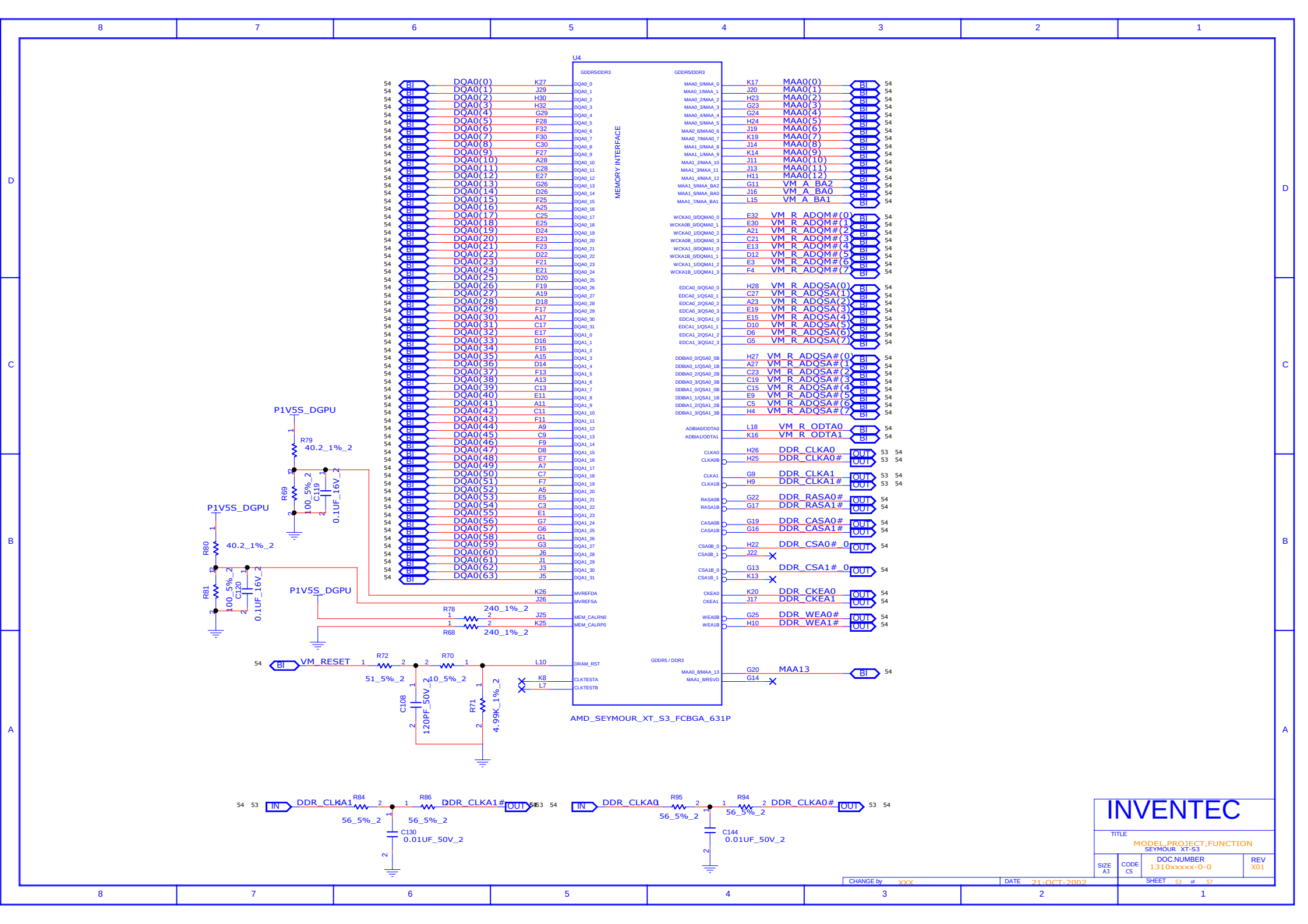
DEFULT IS PX5.0

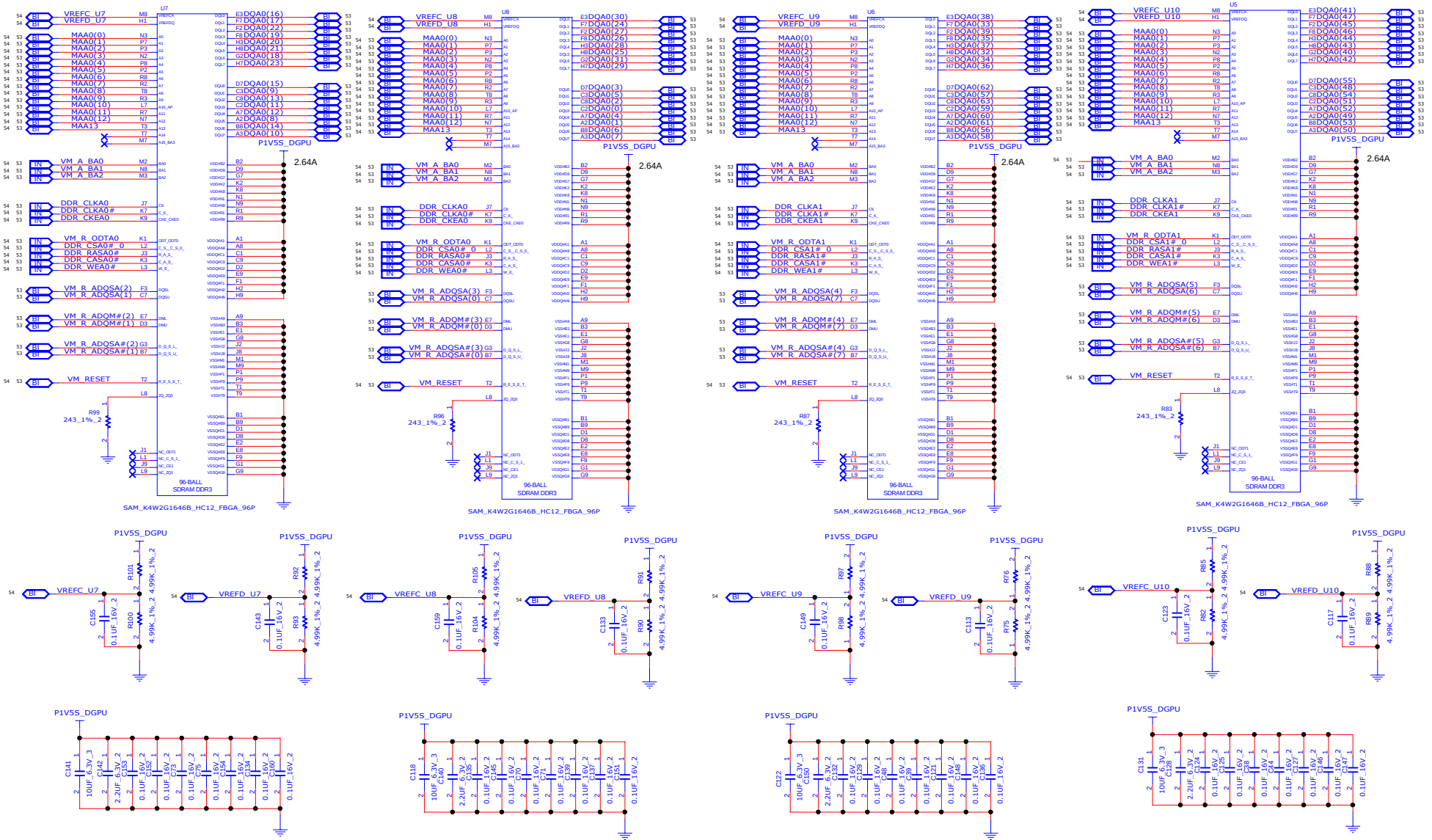




INVENTEC

TITLE: MODEL,PROJECT,FUNCTION SEYMOUR XT-S3			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX	DATE 21-OCT-2002	SHEET 52 of 57	

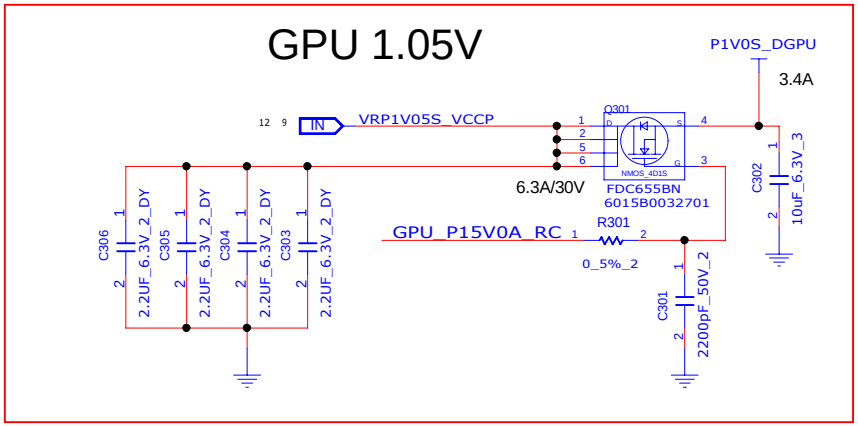

U4
GDDR5/DDR3
MEMORY INTERFACE
AMD_SEYMOUR_XT_S3_FCBGA_631P
P1V5S_DGPU
R79 40.2_1%_2
R69 100_5%_2
C119 0.1UF_16V_2
R80 40.2_1%_2
R81 100_5%_2
C120 0.1UF_16V_2
R78 240_1%_2
R68 240_1%_2
VM_RESET
R72 51_5%_2
R70 10_5%_2
C108 120PF_50V_2
R71 4.99K_1%_2
DDR_CLKA1
DDR_CLKA1#
R84 56_5%_2
R86 56_5%_2
C130 0.01UF_50V_2
DDR_CLKA0
DDR_CLKA0#
R95 56_5%_2
R94 56_5%_2
C144 0.01UF_50V_2
INVENTEC
TITLE
MODEL,PROJECT,FUNCTION
SEYMOUR XT-S3
SIZE A3
CODE CS
DOC.NUMBER 1310xxxxx-0-0
REV X01
CHANGE by XXX
DATE 21-OCT-2002
SHEET 53 of 57



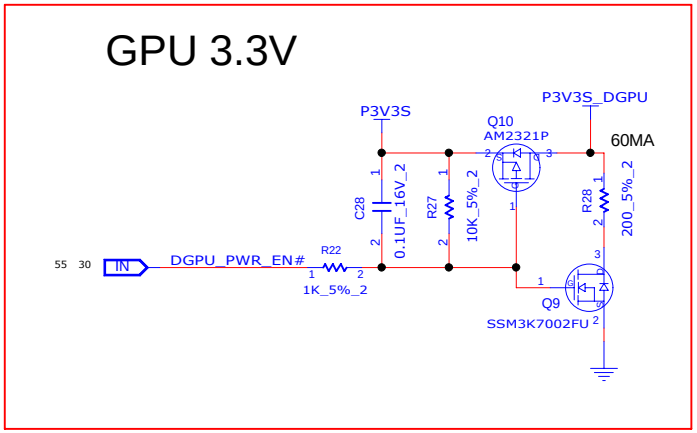
HYNIX 1GB D-DIE PN : 6019B0938301

SAMSUNG 1GB C-DIE PN : 6019B0818601

GPU 1.05V

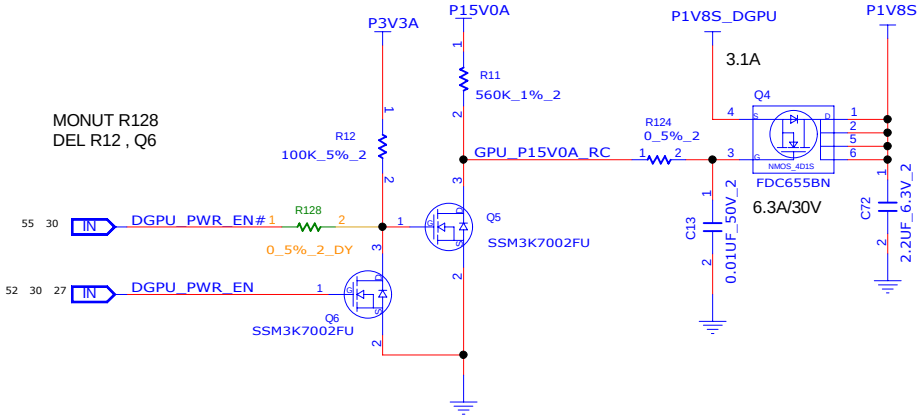


GPU 3.3V

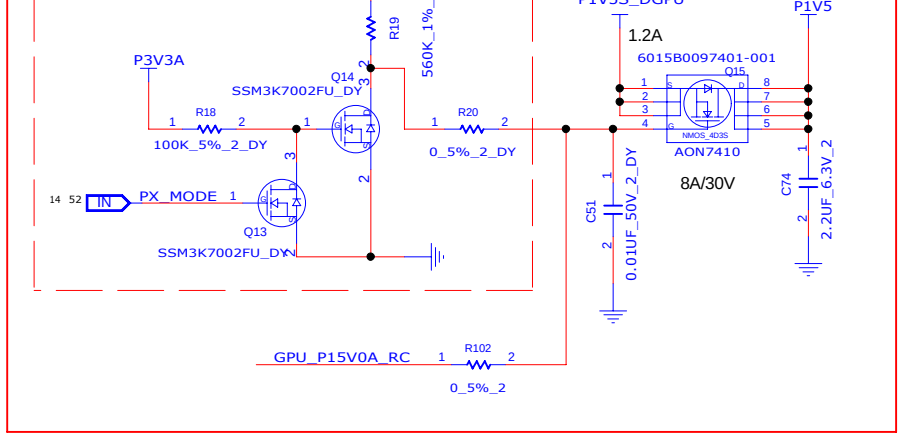


DEFULT IS PX5.0

GPU 1.8V



GPU 1.5V

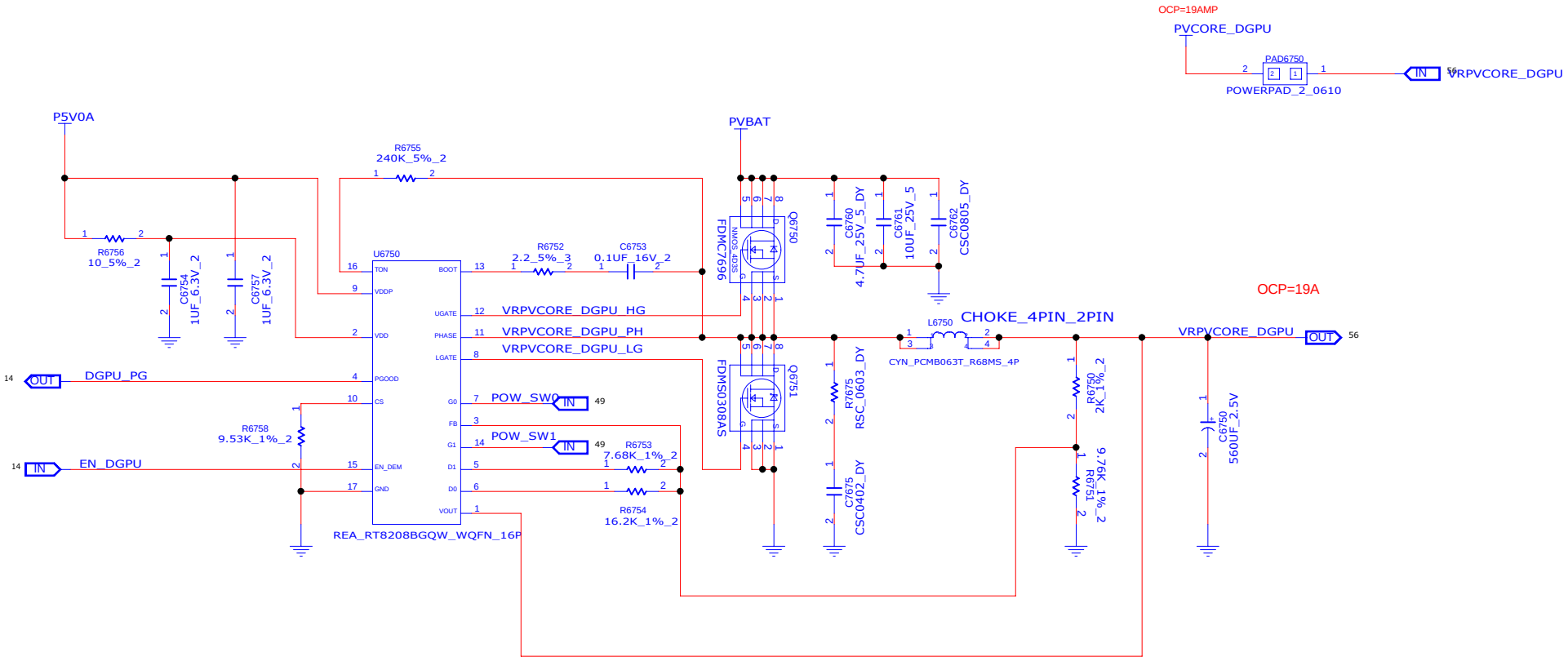


INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
DGPU POWER EE

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

CHANGE by XXX | DATE 21-OCT-2002 | SHEET 55 of 57



P.S. R6750(R1)R6751(R2)R6753(R3)R6754(R4)

RT8208A		RT8208B		Output Voltage Equation
G0	G1	G0	G1	
0	0	1	1	$V_{OUT} = \frac{R1+R2}{R2} \times 0.75$
1	0	0	1	$V_{OUT} = \frac{R1+(R2//R3)}{(R2//R3)} \times 0.75$
0	1	1	0	$V_{OUT} = \frac{R1+(R2//R4)}{(R2//R4)} \times 0.75$
1	1	0	0	$V_{OUT} = \frac{R1+(R2//R3//R4)}{(R2//R3//R4)} \times 0.75$

INVENTEC

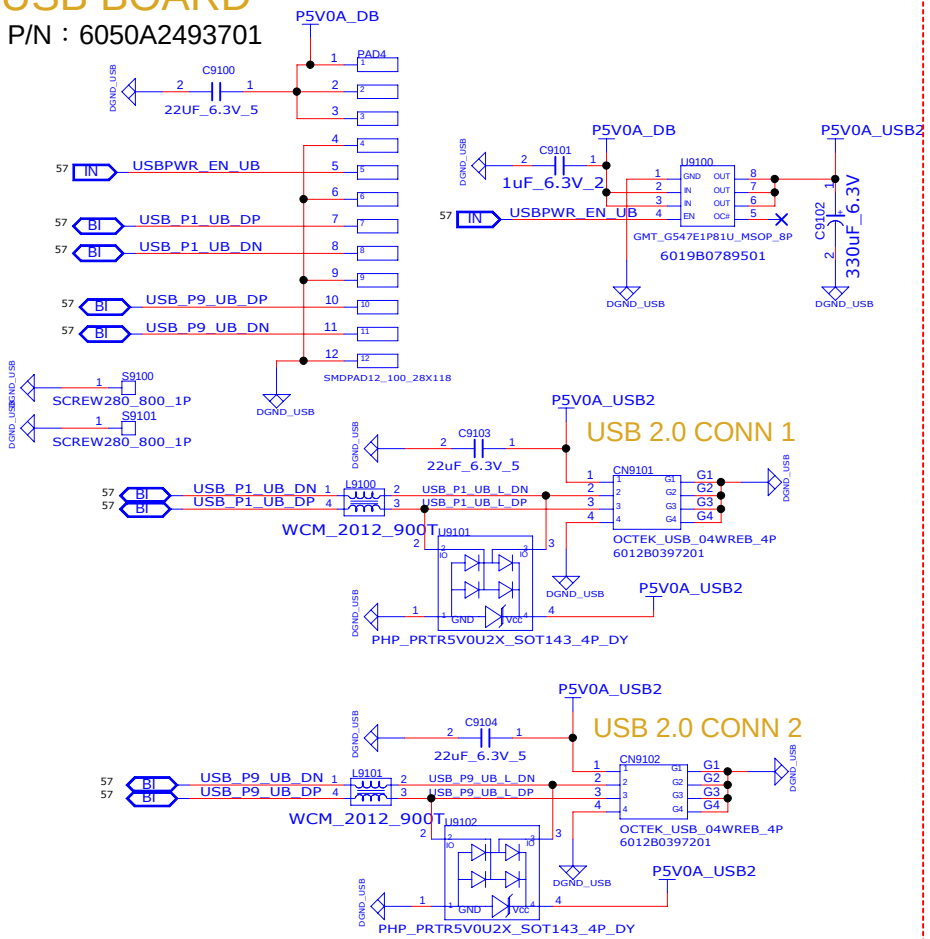
TITLE: MODEL,PROJECT,FUNCTION
DGPU POWER

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

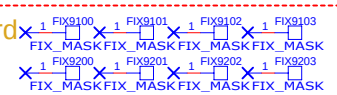
CHANGE by XXX | DATE 21-OCT-2002 | SHEET 56 of 57

USB BOARD

P/N：6050A2493701

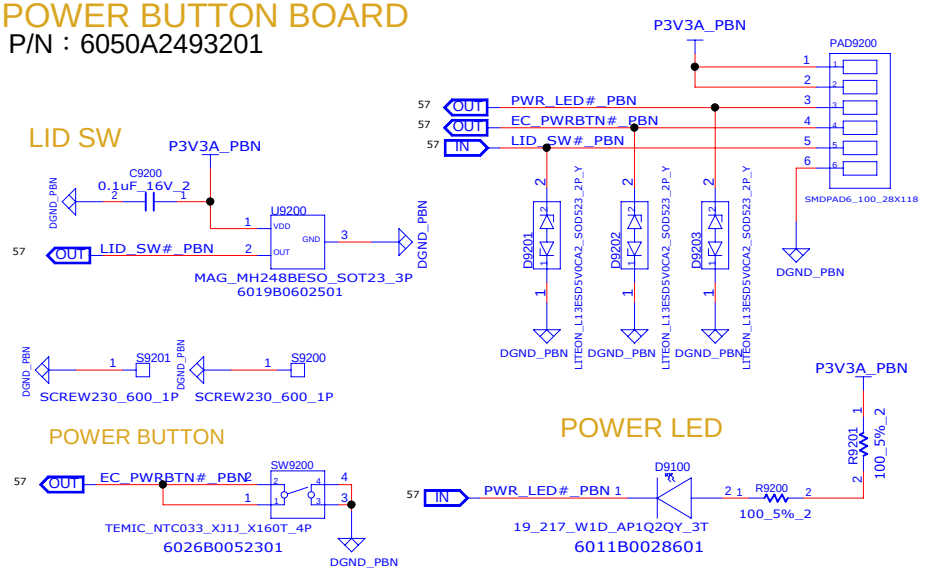


for Dauther Board



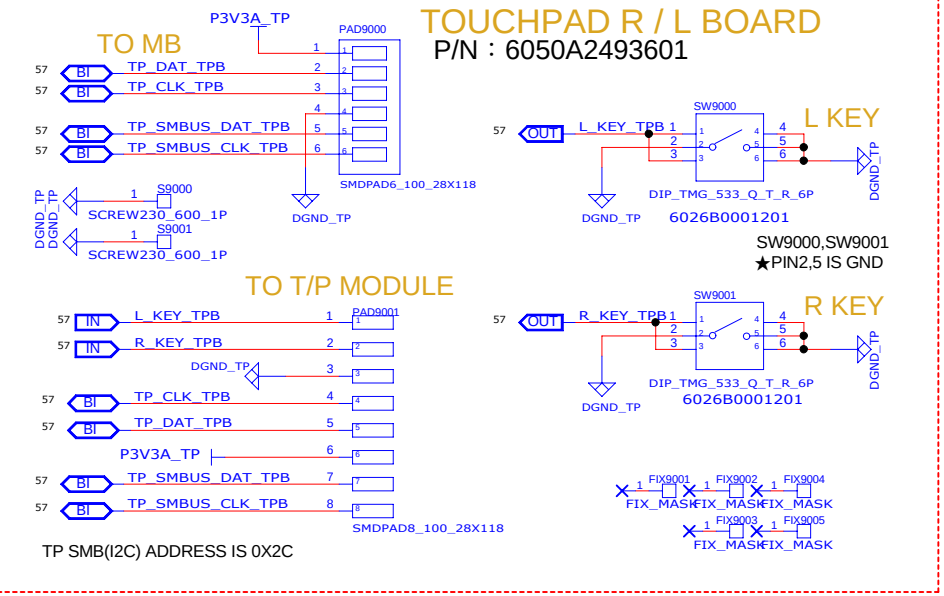
POWER BUTTON BOARD

P/N：6050A2493201



TOUCHPAD R / L BOARD

P/N：6050A2493601



TP SMB(I2C) ADDRESS IS 0X2C

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION USB, POWER BUTTON_DB			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX	DATE 21-OCT-2002	SHEET 57 of 57	