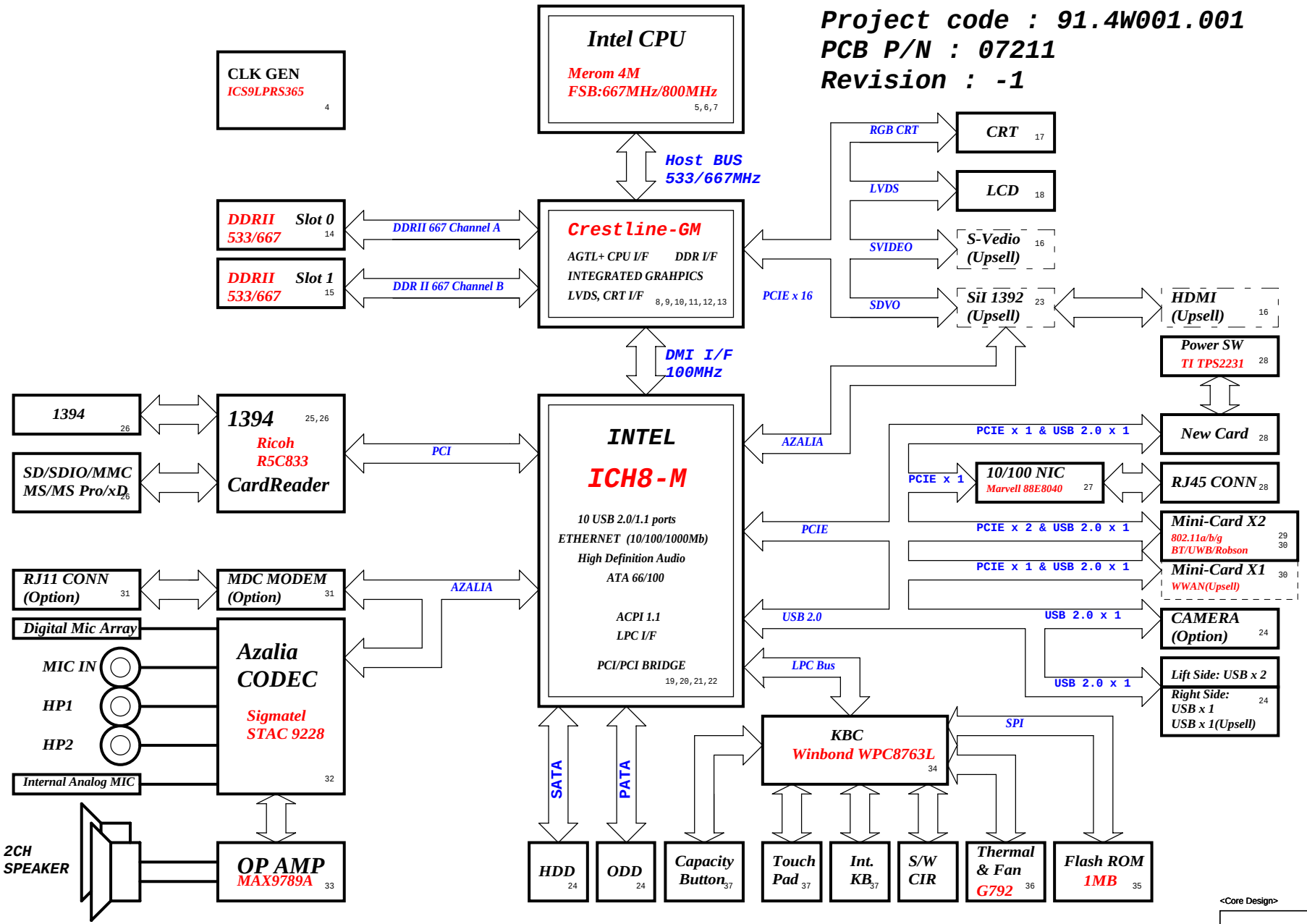
Spears Intel UMA Block Diagram 2007/08/29

Project code : 91.4W001.001
PCB P/N : 07211
Revision : -1



CPU DC/DC ISL6262A	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS5117	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

SYSTEM DC/DC TPS51120	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC TPS51100	
INPUTS	OUTPUTS
1D8V_S3	0D9V_S3

SYSTEM DC/DC LDO	
INPUTS	OUTPUTS
3D3V	2D5V
1D8V	1D5V_S0

SYSTEM DC/DC LDO	
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 1D5V_S0

MAXIM CHARGER MAX8731A	
INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

<Core Design>

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Title: DS2 System Block Diagram

Size	Document Number	Rev
A3	Spears-Intel	-1

Date: Wednesday, September 12, 2007 Sheet 1 of 47

CPU_CORE
ISL6262A

VID0
VID1
VID2
VID3
VID4
VID5

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)

Output Signal
VROK()

VRPWRGD

Output Power
VCC_CORE_PWR(O)

VCC_CORE_S0(Imax=35A)

CPUCORE_ON

Input Signal
EN (I / 3.3V)

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

VCC_SENSE
VSS_SENSE

Input Power
VCC(I)
VCC(I)
VCC(I)

DCBATOUT
5V_S0
3D3V_S0

TI TPS51120
3D3V/5V

3V/5V_EN

Input Signal
51120_EN2 FOR 3.3V
51120_EN1 FOR 5.0V

Output Signal
PGOUT1(OD / 5V)
PGOUT2(OD / 3D3V)

CPUCORE_ON(Pull High 3D3V)

DCBATOUT

Input Power
VIN
V5FILT(I / 5V)

Output Power
5V(O)
3D3V(O)

5V_AUX_S5
3D3V_AUX_S5
5V_S5 (6A)
3D3V_S5 (5A)

1D5V_S0

5V_S5
1D8V_S3
PM_SLP_S3#

VCNTL
VIN
EN

VOUT(O)
POK

1D5V_S0
CPUCORE_ON

APL5915

2D5V_S0

3D3V_S0

INPUT
OUT

2D5V_S0

G9131

1D25V_S0

5V_S5
1D8V_S3
PM_SLP_S3#

VCNTL
VIN
EN

VOUT(O)
POK

1D5V_S0
CPUCORE_ON

G971

Adapter

AD_OFF
AD_JK
5V_AUX_S5

Input Signal
(I)

Output Signal
(O)

Input Power
VCC(I)
VCC(I)

Output Power
VCC(O)

AD_IN
AD+

Charger_MAX8731A

CHARGE_OFF
BAT+SENSE
BT_SCL
BT_SDA
AC_IN

Input Signal
CLS (I / 3.3V)
BATT (I / 3.3V)
SCL (IO / 5V)
SDA (IO / 5V)
PB0/MOSI/AIN0

Output Signal
LDO (O / 5.4V)
XTAL2/PB4 (O/5V)
XTAL1/PB3 (O/5V)

Output Power
VCC (O)
VCC (O)

MAX8731_LDO
DCBATOUT
BT+

Input Power
DCIN (I)

AD+

TI TPS51100
0.9V/DDR_VREF_S3

PM_SLP_S4#
PM_SLP_S3#

Input Signal
S5
S3

Input Power
VCC(I)
VCC(I)

DCBATOUT
5V_S5

Output Power
VCC(O)
VCC(O)

0D9V_DDR_VTT
DDR_VREF_S3

TPS51117_1D8V_S3

PM_SLP_S4#
5V_S5
DCBATOUT

Input Signal
EN_PSV(I / 5V)

Output Signal
PGOUT(OD / 5V)

Input Power
VCC
VIN

Output Power
1D8V_PWR

CPUCORE_ON
1D8V_S3

TPS51117_1D05V

PM_SLP_S3#
5V_S5
DCBATOUT

Input Signal
EN_PSV(I / 5V)

Output Signal
PGOUT(OD / 5V)

Input Power
VCC
VIN

Output Power
1D05V_PWR

CPUCORE_ON
1D05V_S0 (15A)

<Core Design>

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Title: **Power Block Diagram**

Size	Document Number	Rev
A3	DS2-Intel	-1

Date: Wednesday, September 12, 2007 Sheet 2 of 47

INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overidden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap

ICH_RSVD	Tp3	AZ_DOUT_ICH	Description
0		0	RSVD
0		1	Enter XOR Chain
1		0	Normal Operation(default)
1		1	Set PCIE port cofig bit1

A16 swap override strap

PCI_GNT#3	low = A16 swap override enable high = default

BOOT BIOS Strap

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

integrated VccSus1_05,VccSus1_5,VccCL1_5

SM_INTVRMEN	High=Enable	Low=Disable

integrated VccLan1_05VccCL1_05

LAN100_SLP	High=Enable	Low=Disable

DEFAULE HIGH

No Reboot Strap

SPKR	LOW = Defaule High=No Reboot

8.2K PULL HIGH

INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4 ★
CFG 8 Low Power PCI Express	Normal★	Low Power mode
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode(Lanes number in order)★
CFG 16 FSB Dynamic ODT	Disabled	Enabled ★
CFG 19 DMI Lane Reversed	Normal Operation ★	Reserved Lane
CFG 20 Concurrent SDVO/PCIE	Only PCIE or SDVO is operation★	PCIE and SDVO are operation simultaneous
SDVO_CTRL_DATA SDVO Present	NO SDVO Card Present ★	SDVO Card Present

CFG 12 CFG 13	XOR/ALL-Z
LL(00)	Reserved
LH(01)	XOR Mode Enabled
HL(10)	All Z Mode Enabled
HH(11)	Normal Operation

INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD

20,22 +RTCVCC → +RTCVCC
5,6,7,8,10,11,12,20,22,34,43,47 1D05V_S0 → 1D05V_S0
8,11,22,45 1D25V_S0 → 1D25V_S0
27 1D2V_LAN_S5 → 1D2V_LAN_S5
28 1D5V_NEW_S0 → 1D5V_NEW_S0
6,11,20,21,22,28,29,30,45 1D5V_S0 → 1D5V_S0
8,11,12,14,15,44,45,46,47 1D8V_S3 → 1D8V_S3
27,28 2D5V_LAN_S5 → 2D5V_LAN_S5

20,31,34,35,36,38,39,40,47 3D3V_AUX_S5 → 3D3V_AUX_S5
27,28 3D3V_LAN_S5 → 3D3V_LAN_S5
4,8,10,11,14,15,16,17,18,19,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,40,41,43,45,46,47 3D3V_S0 → 3D3V_S0
19,21,22,27,28,31,35,38,40,46,47 3D3V_S5 → 3D3V_S5
18,39,40,47 5V_AUX_S5 → 5V_AUX_S5

16,17,18,22,24,33,35,36,37,41,45,46,47 5V_S0 → 5V_S0
22,24,29,30,31,35,38,40,43,44,45,46,47 5V_S5 → 5V_S5
38,39,47 AD+ → AD+
18,39,40,41,42,43,44,46,47 DCBATOUT → DCBATOUT
14,15,45,47 DDR_VREF_S0 → DDR_VREF_S0
8,14,15,45 DDR_VREF_S3 → DDR_VREF_S3

18 +LCDVDD → +LCDVDD
6,7,42 VCC_CORE_S0 → VCC_CORE_S0

<Core Design>

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Title: Table of Content

Size: A3 | Document Number: DS2-Intel | Rev: -1

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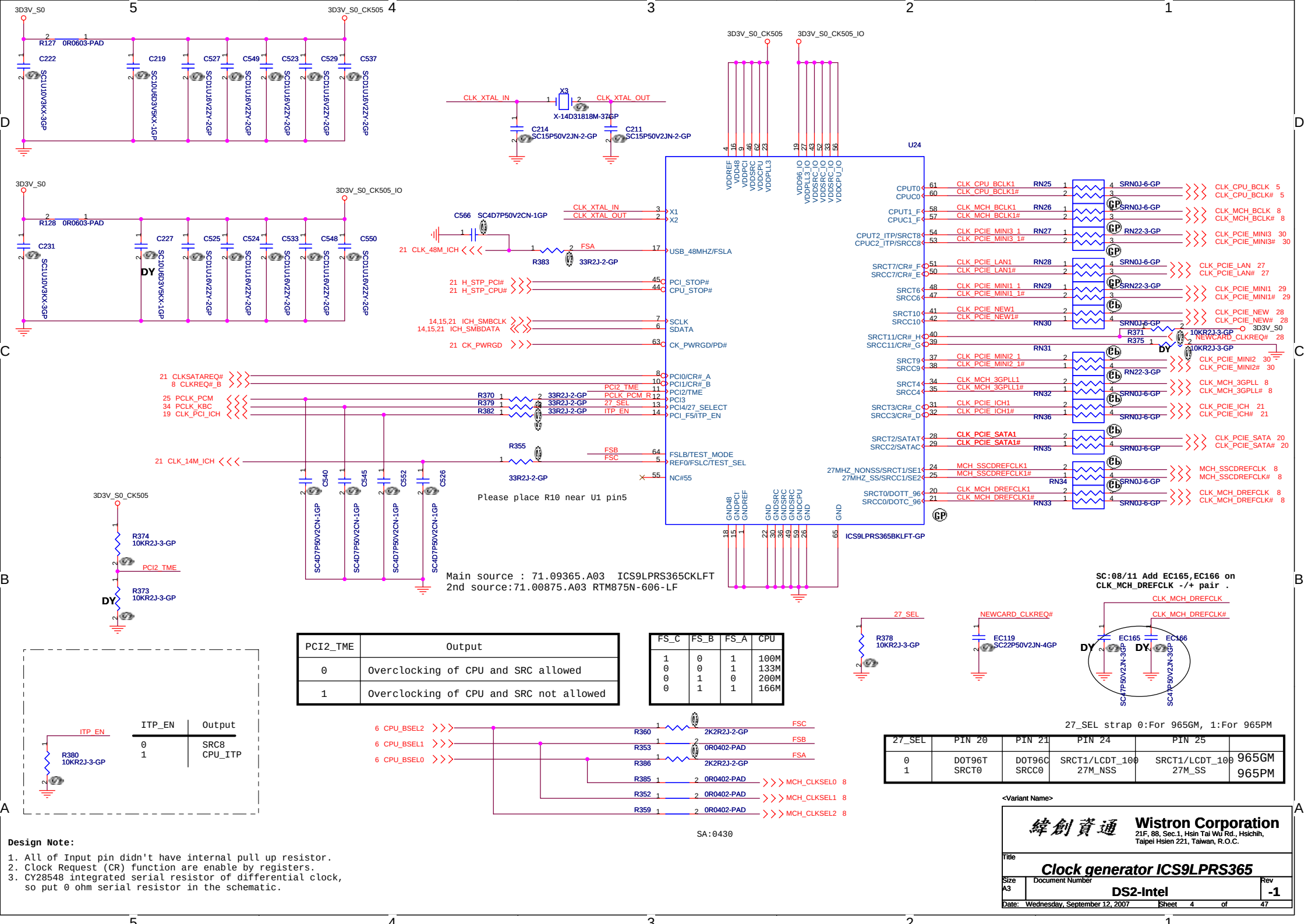
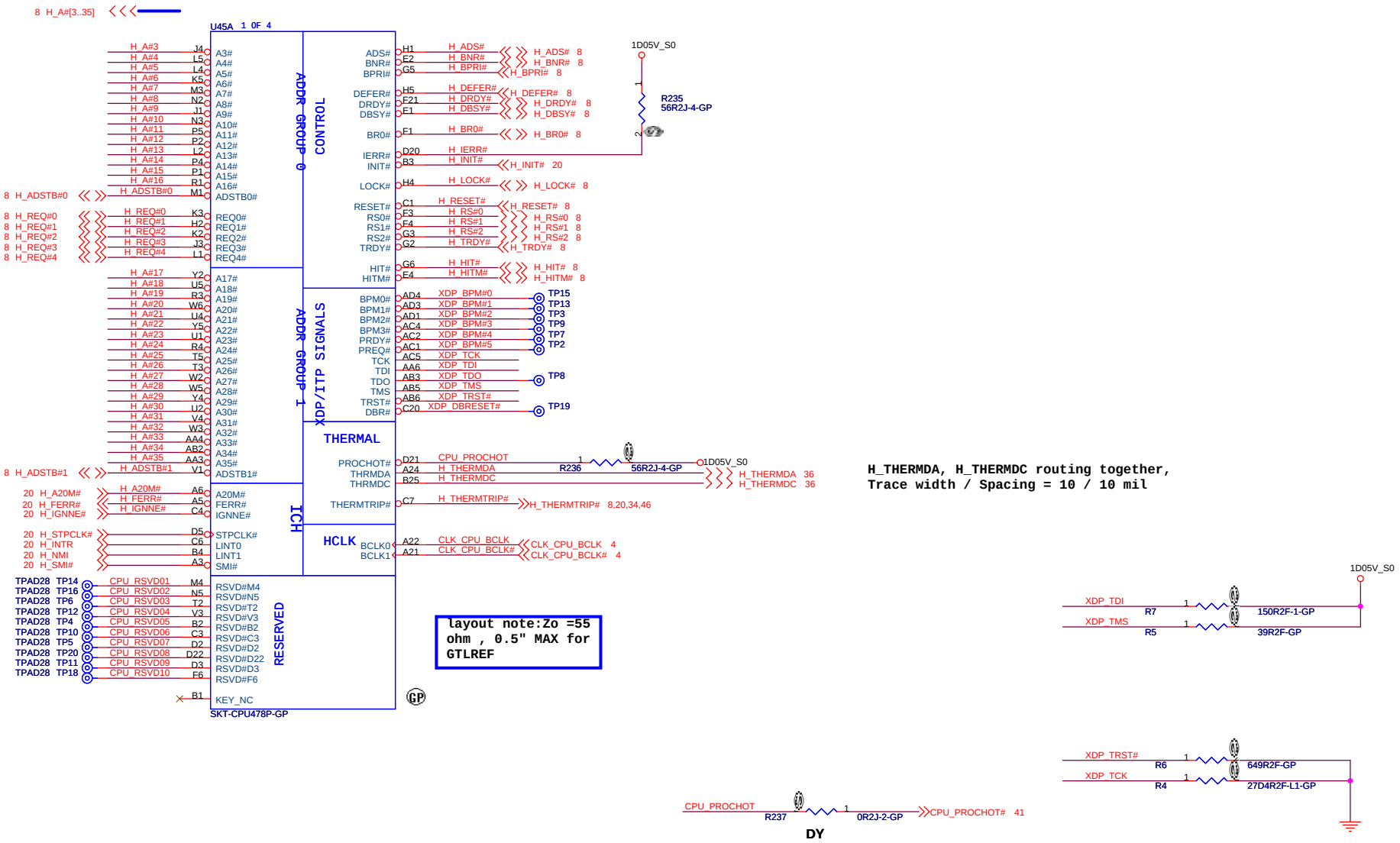


PCI2_TME	Output
0	Overclocking of CPU and SRC allowed
1	Overclocking of CPU and SRC not allowed

FS_C	FS_B	FS_A	CPU
1	0	1	100M
0	0	1	133M
0	1	0	200M
0	1	1	166M

ITP_EN	Output
0	SRC8
1	CPU_ITP

27_SEL	PIN 20	PIN 21	PIN 24	PIN 25	
0	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100	965GM
1	SRCT0	SRCC0	27M_NSS	27M_SS	965PM



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Title: ***Meron(1/3)-AGTL+/XDP***

Size	Document Number	Rev
A3	DS2-Intel	-1

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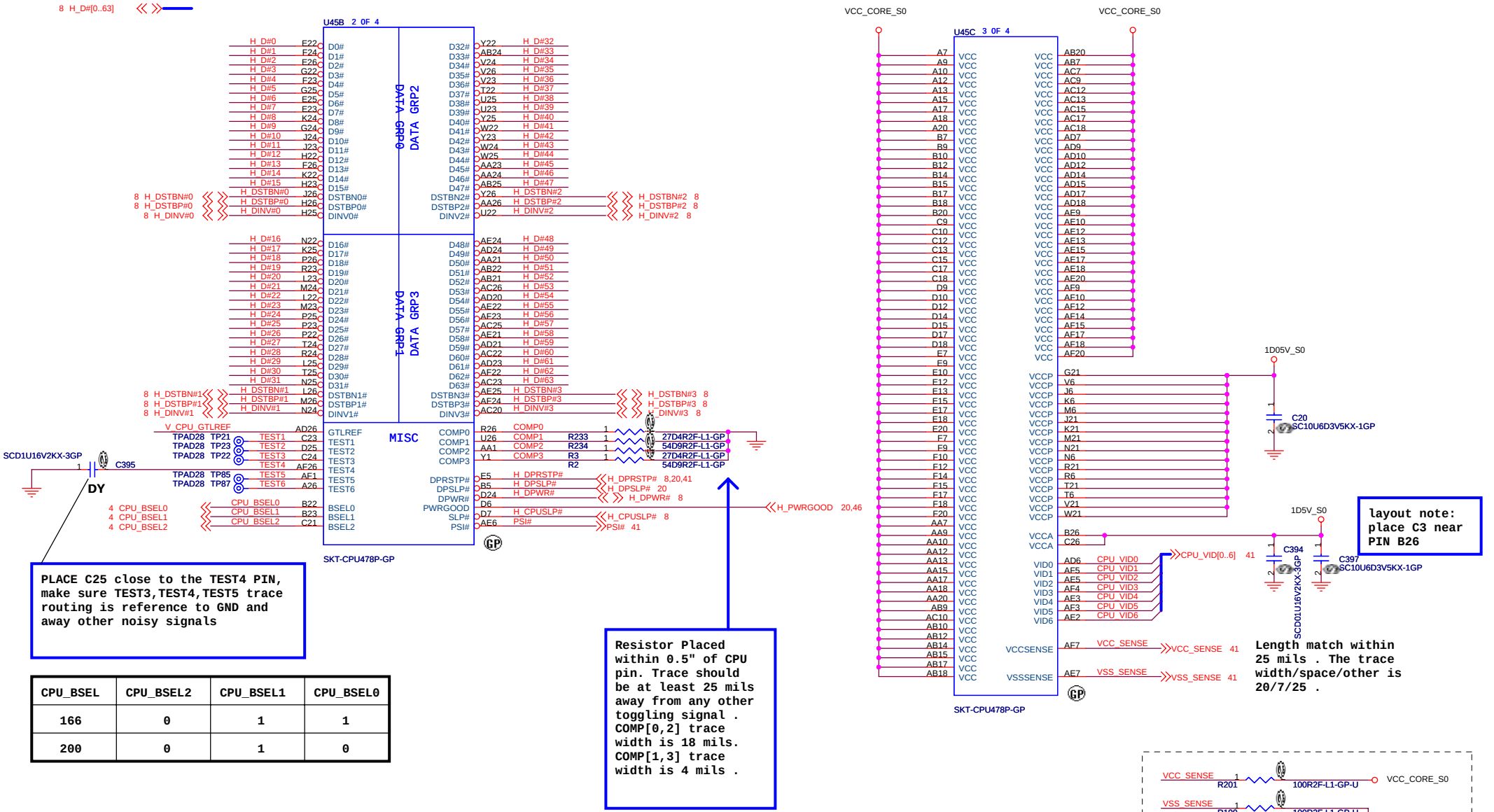

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

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Title: Meron(2/3)-AGTL+/PWR

Size	Document Number	Rev
A3	DS2-Intel	-1

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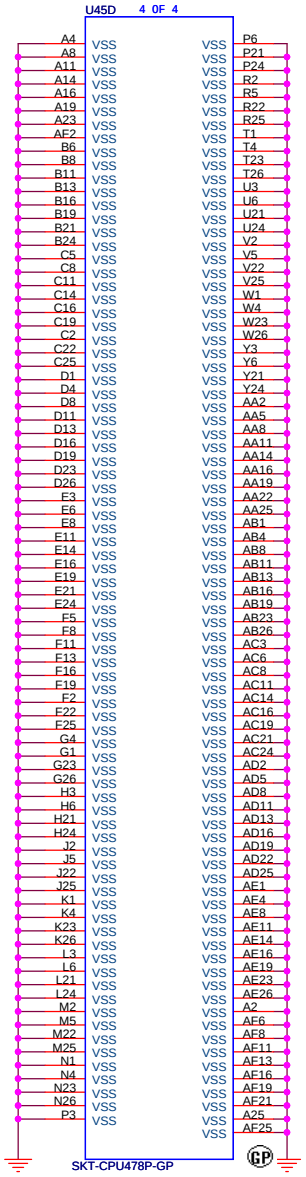

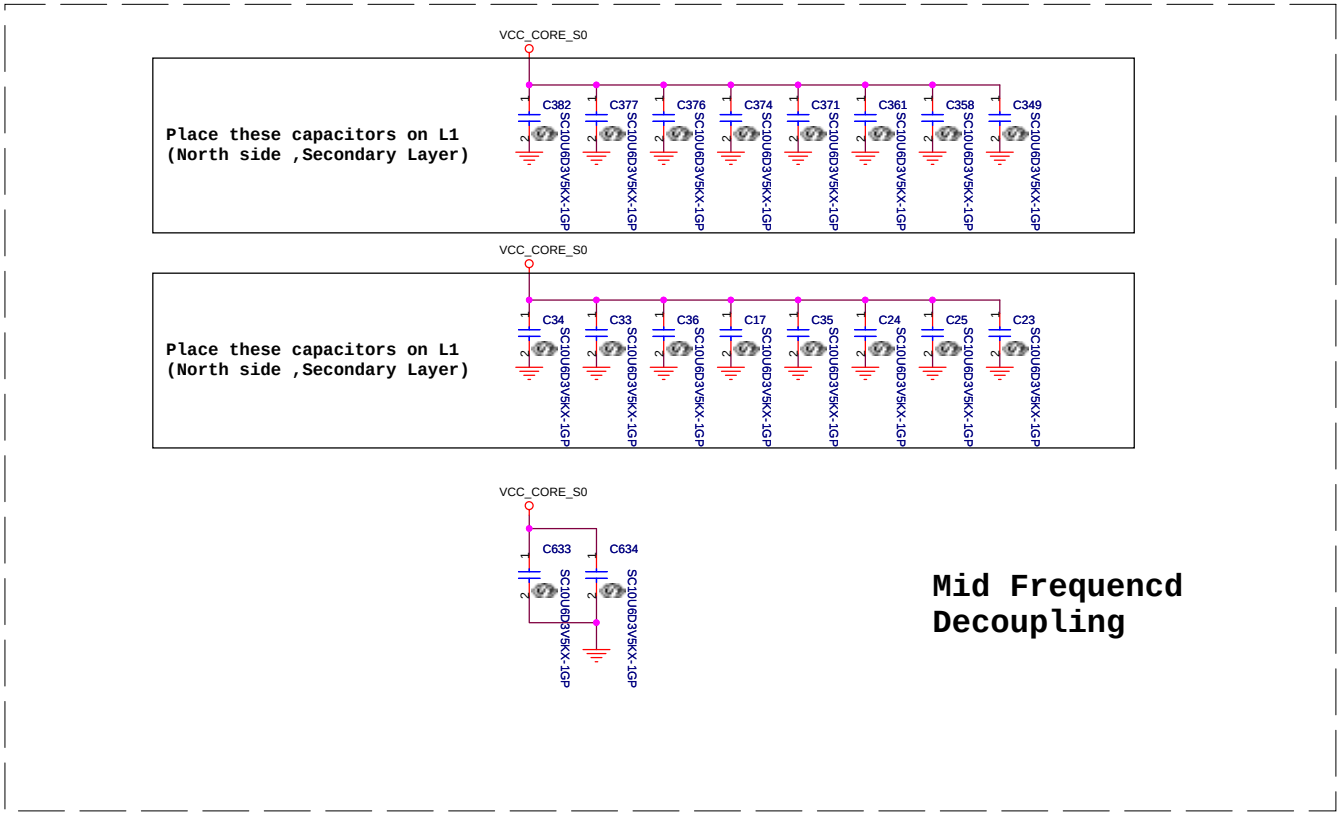

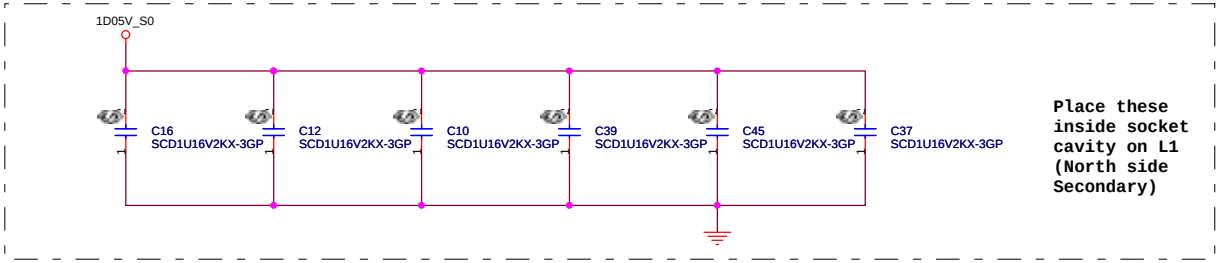

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Title: Meron(3/3)-GND&Bypass

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FOR Calero: 80.6 ohm
Crestline: 20 ohm

CFG[17:3] have internal pull up
CFG[19:18] have internal pull down

NB:71.GM965.A0U

layout note :
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

Layout Note :
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20

Spec: H_SWING=0.3125 X
VTT +/- 1%

Layout Note :
Place C32 within 100 mils of NB

Layout Note :
Place C33 near
pin B3 of NB

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Title: CRESTLINE(1/6)-AGTL+/DMI/DDR2

Size: Custom | Document Number: DS2-Intel | Rev: -1

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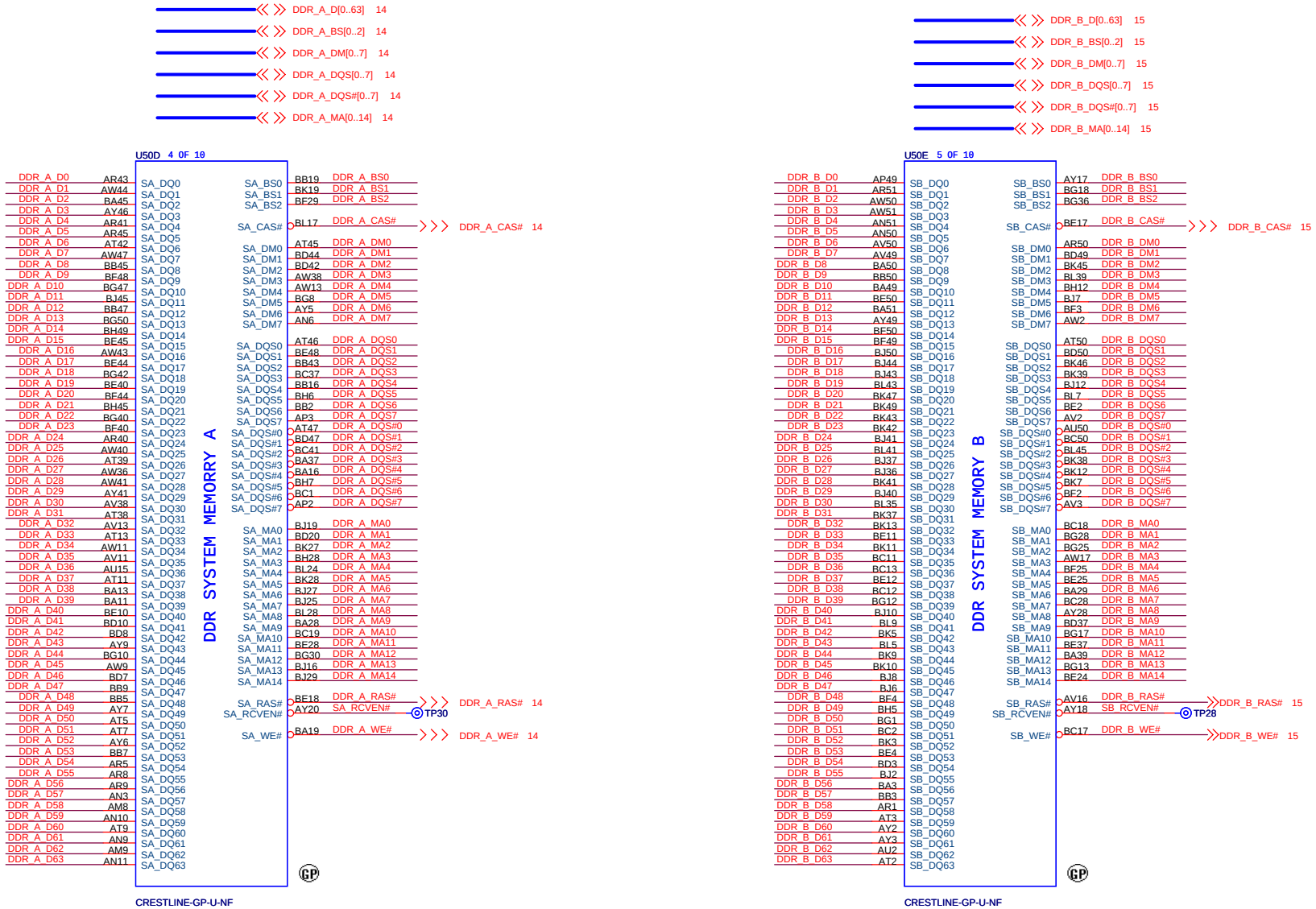

<Core Design>

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Title: CRESTLINE(2/6)-DDR2 A/B CH

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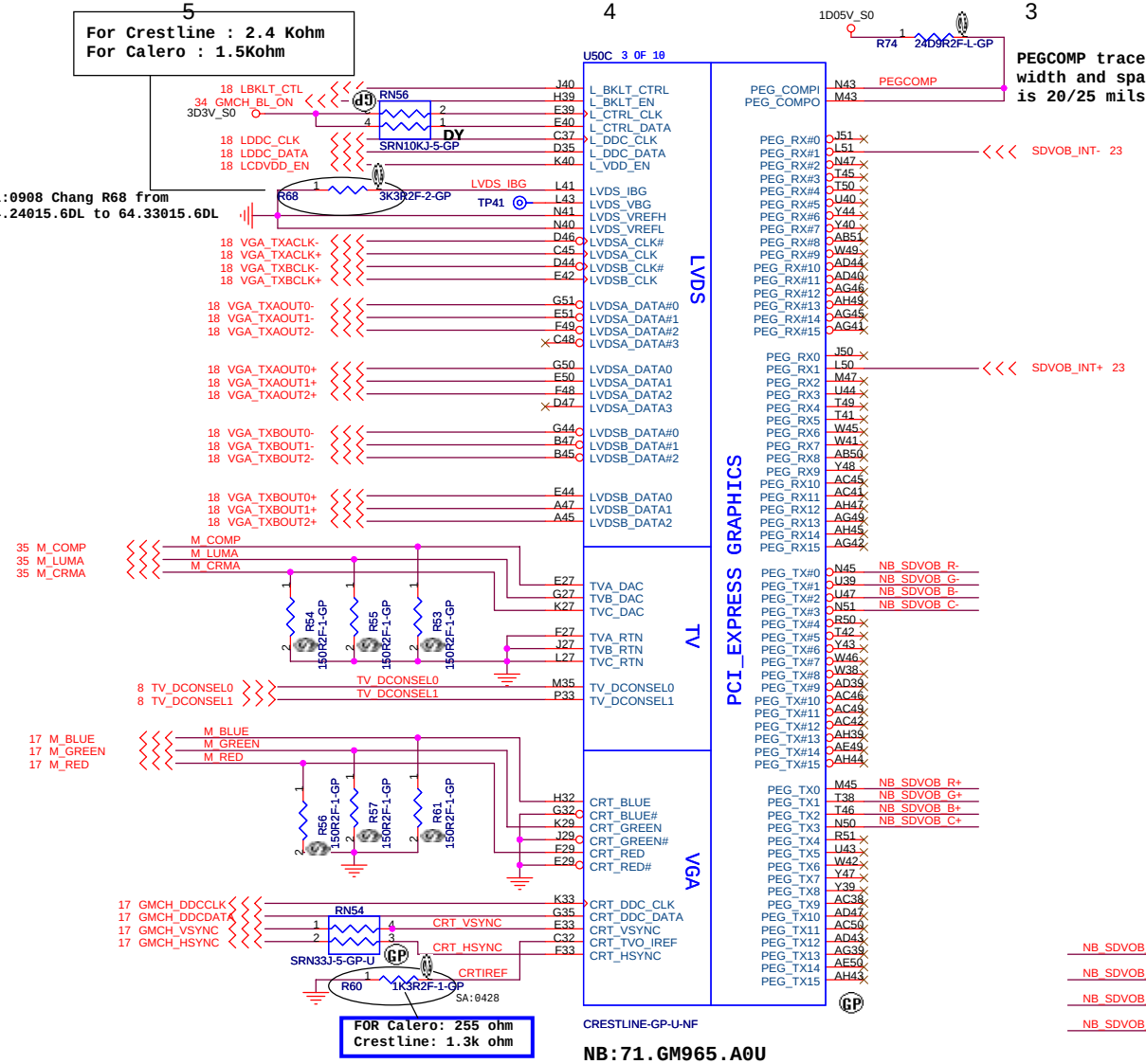
For Crestline : 2.4 Kohm
For Calero : 1.5Kohm

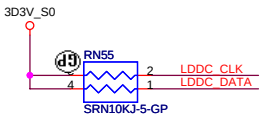
D 1:0908 Chang R68 from 64.24015.6DL to 64.33015.6DL

PEGCOMP trace width and spacing is 20/25 mils.



FOR Calero: 255 ohm
Crestline: 1.3k ohm

NB:71.GM965.A0U



Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB_667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default)*
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disable 1 = Enable *
CFG[18:17]	Reversed
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19(DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse lane
CFG20(PCIE/SDVO consurrent)	0 = Only PCIE or SDVO is operational * 1 = PCIE/SDVO are operating simu.

<Core Design>

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Title: CRESTLINE(3/6)-VGA/LVDS/TV

Size: A3 | Document Number: DS2-Intel | Rev: -1

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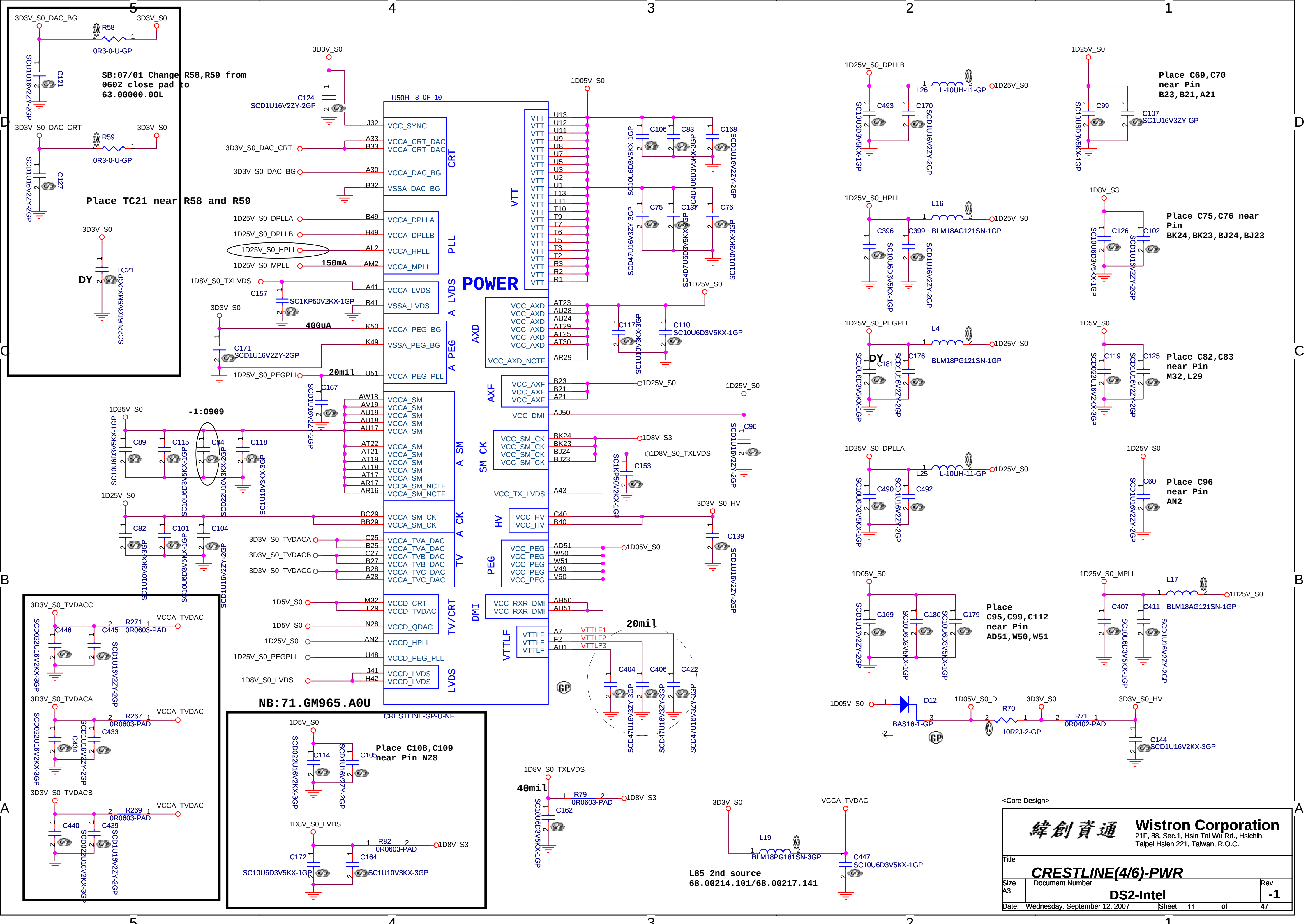
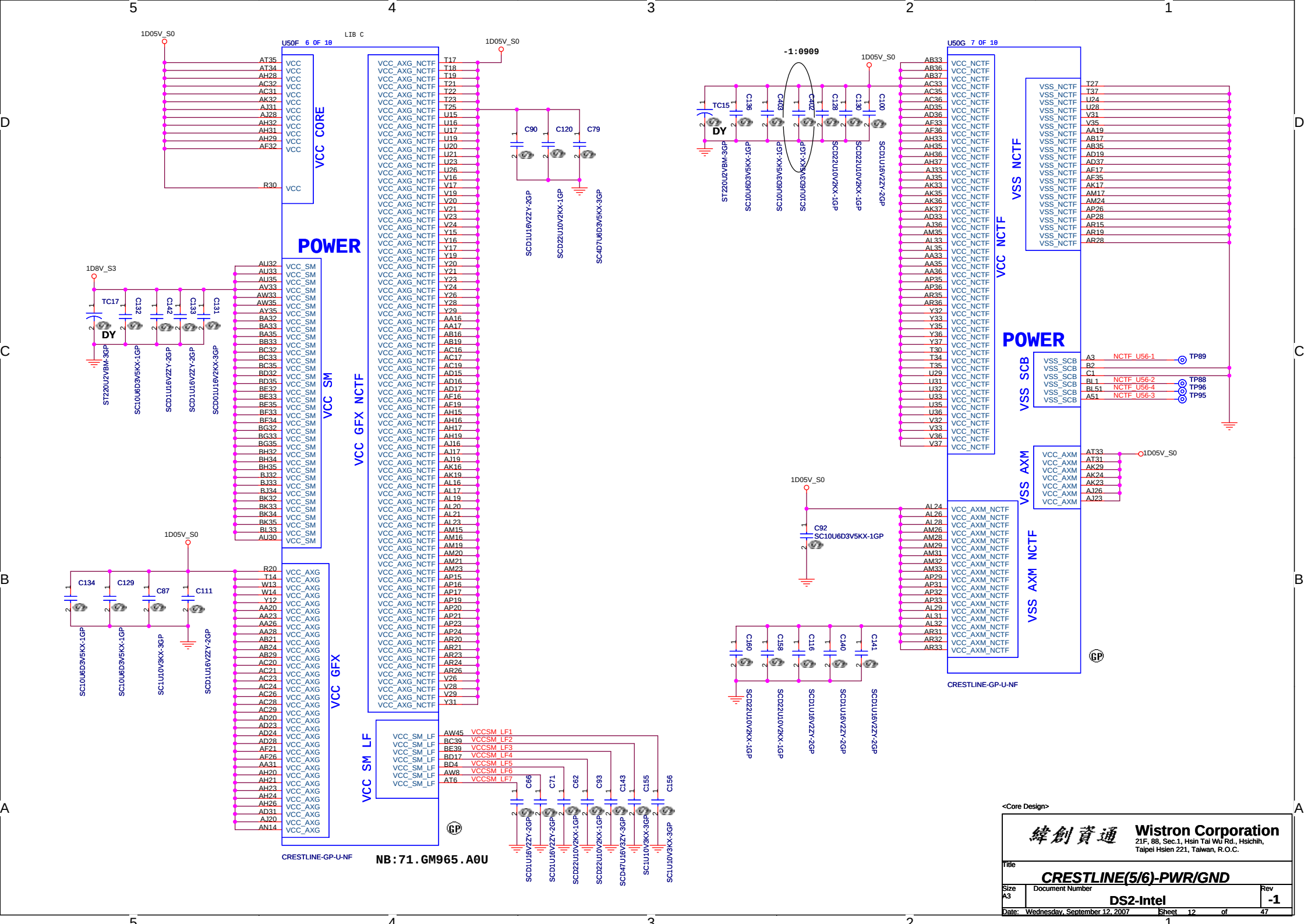
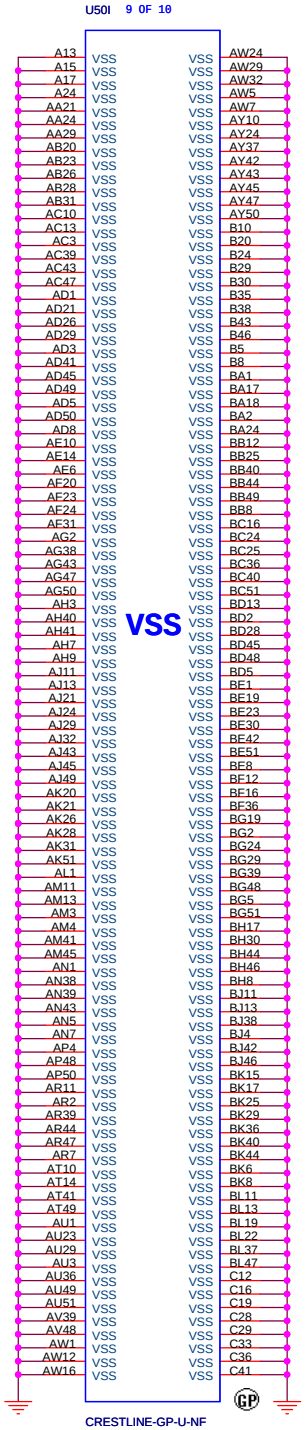
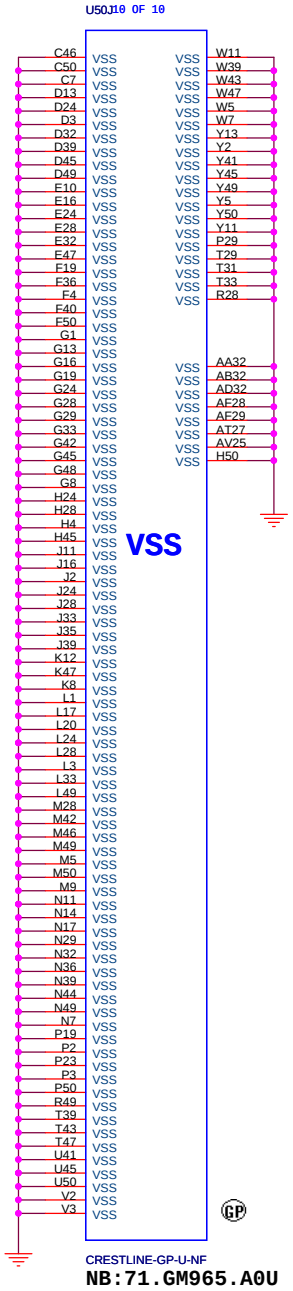

3D3V_S0_DAC_BG
R58
0R3-0-U-GP
C121
SCD1U16V2ZY-2GP
SB:07/01 Change R58,R59 from
0602 close pad to
63.00000.00L
3D3V_S0_DAC_CRT
R59
0R3-0-U-GP
C127
SCD1U16V2ZY-2GP
Place TC21 near R58 and R59
3D3V_S0
TC21
DY
SC22U6D3V5MX-2GP
C124
SCD1U16V2ZY-2GP
U50H 8 OF 10
VCC_SYNC
VCCA_CRT_DAC
VCCA_DAC_BG
VSSA_DAC_BG
CRT
VCCA_DPLLA
VCCA_DPLLB
VCCA_HPLL
VCCA_MPLL
PLL
1D25V_S0_DPLLA
1D25V_S0_DPLLB
1D25V_S0_HPLL
1D25V_S0_MPLL
150mA
1D8V_S0_TXLVDS
C157
SC1KP50V2KX-1GP
VCCA_LVDS
VSSA_LVDS
A LVDS
POWER
400uA
C171
SCD1U16V2ZY-2GP
VCCA_PEG_BG
VSSA_PEG_BG
VCCA_PEG_PLL
A PEG
20mil
1D25V_S0_PEGPLL
C167
-1:0909
C89
C115
C94
C118
SC10U6D3V5KX-1GP
SCD22U10V3KX-2GP
SC1U10V3KX-3GP
VCCA_SM
VCCA_SM_NCTF
A SM
C82
C101
C104
VCCA_SM_CK
A CK
3D3V_S0_TVDACA
3D3V_S0_TVDACB
3D3V_S0_TVDACC
VCCA_TVA_DAC
VCCA_TVB_DAC
VCCA_TVC_DAC
TV
1D5V_S0
VCCD_CRT
VCCD_TVDAC
VCCD_QDAC
VCCD_HPLL
VCCD_PEG_PLL
VCCD_LVDS
TV/CRT
LVDS
1D8V_S0_LVDS
NB:71.GM965.A0U
CRESTLINE-GP-U-NF
R271
R267
R269
0R0603-PAD
VCCA_TVDAC
C446
C445
C434
C433
C440
C439
SCD022U16V2KX-3GP
1D05V_S0
VTT
C106
C83
C168
C75
C197
C76
SC10U6D3V5KX-1GP
SC4D7U6D3V5KX-3GP
SCD47U16V2ZY-3GP
SC1U10V3KX-3GP
VCC_AXD
VCC_AXD_NCTF
AXD
C117
C110
SC10U6D3V5KX-1GP
VCC_AXF
AXF
VCC_DMI
C96
VCC_SM_CK
SM CK
1D8V_S3
C153
SC1KP50V2KX-1GP
VCC_TX_LVDS
VCC_HV
HV
3D3V_S0_HV
C139
VCC_PEG
PEG
VCC_RXR_DMI
DMI
VTTLF
VTTLF1
VTTLF2
VTTLF3
20mil
C404
C406
C422
SCD47U16V2ZY-3GP
GP
Place C108,C109
near Pin N28
C114
C105
C172
C164
R82
0R0603-PAD
SC10U6D3V5KX-1GP
SC1U10V3KX-3GP
1D8V_S0_TXLVDS
40mil
R79
C162
L19
BLM18PG181SN-3GP
C447
SC10U6D3V5KX-1GP
VCCA_TVDAC
L85 2nd source
68.00214.101/68.00217.141
1D25V_S0_DPLLB
L26
L-10UH-11-GP
C493
C170
1D25V_S0
C99
C107
SC1U16V3ZY-GP
Place C69,C70
near Pin
B23,B21,A21
1D25V_S0_HPLL
L16
BLM18AG121SN-1GP
C396
C399
1D8V_S3
C126
C102
Place C75,C76 near
Pin
BK24,BK23,BJ24,BJ23
1D25V_S0_PEGPLL
L4
BLM18PG121SN-1GP
C181
C176
1D5V_S0
C119
C125
Place C82,C83
near Pin
M32,L29
1D25V_S0_DPLLA
L25
C490
C492
C60
Place C96
near Pin
AN2
C169
C180
C179
Place
C95,C99,C112
near Pin
AD51,W50,W51
1D25V_S0_MPLL
L17
C407
C411
D12
BAS16-1-GP
1D05V_S0_D
R70
10R2J-2-GP
R71
0R0402-PAD
C144
SCD1U16V2KX-3GP
<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CRESTLINE(4/6)-PWR
Size A3
Document Number
DS2-Intel
Rev -1
Date: Wednesday, September 12, 2007
Sheet 11 of 47


POWER
VCC CORE
VCC GFX
VCC SM
VCC GFX NCTF
VCC SM LF
VCC AXG NCTF
VCC SM NCTF
VCC AXM NCTF
VSS NCTF
VSS SCB
VSS AXM
VSS AXM NCTF
U50F 6 OF 10
U50G 7 OF 10
LIB C
CRESTLINE-GP-U-NF
NB:71.GM965.A0U
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CRESTLINE(5/6)-PWR/GND
DS2-Intel
-1
Wednesday, September 12, 2007
Sheet 12 of 47





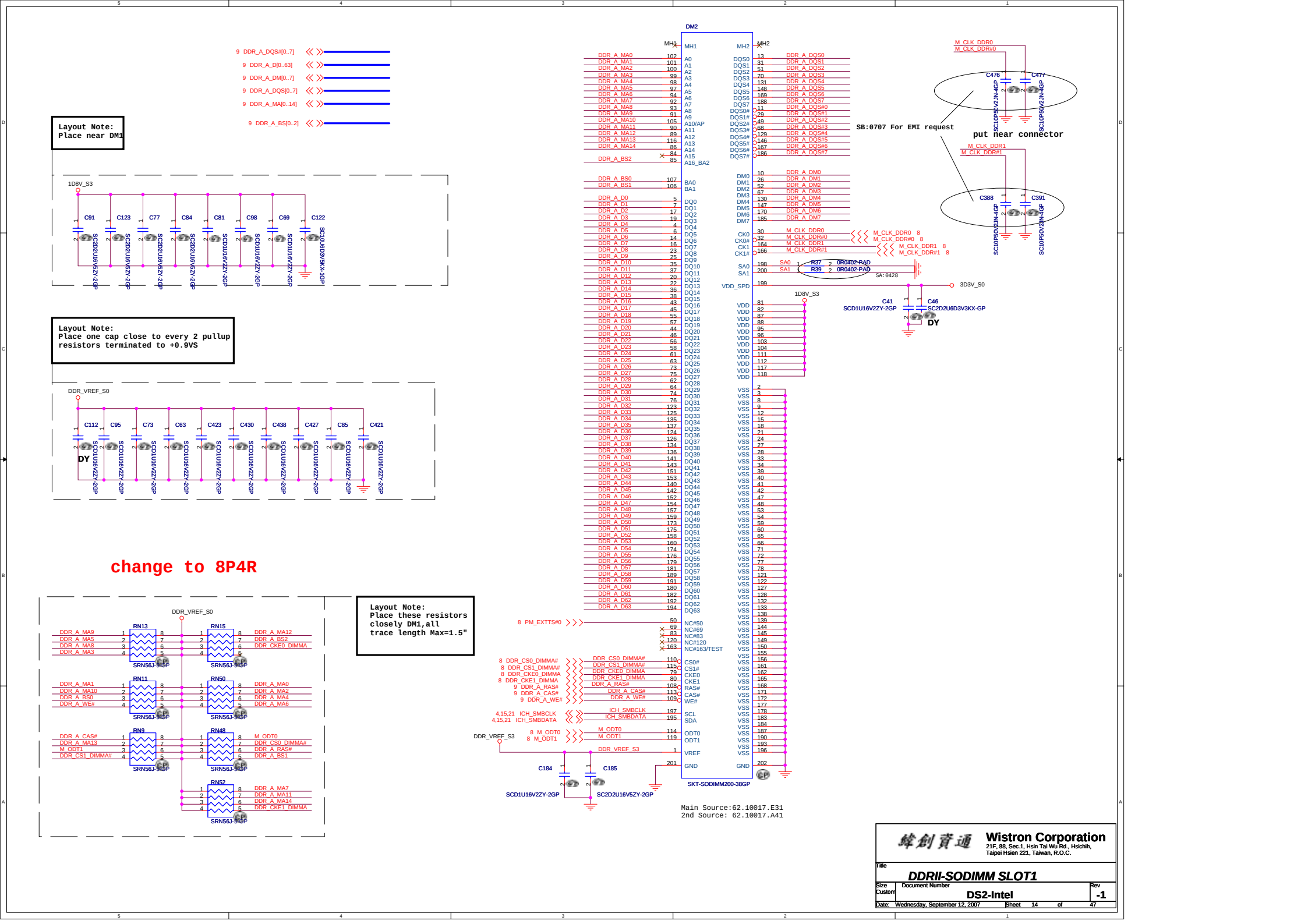
<Core Design>

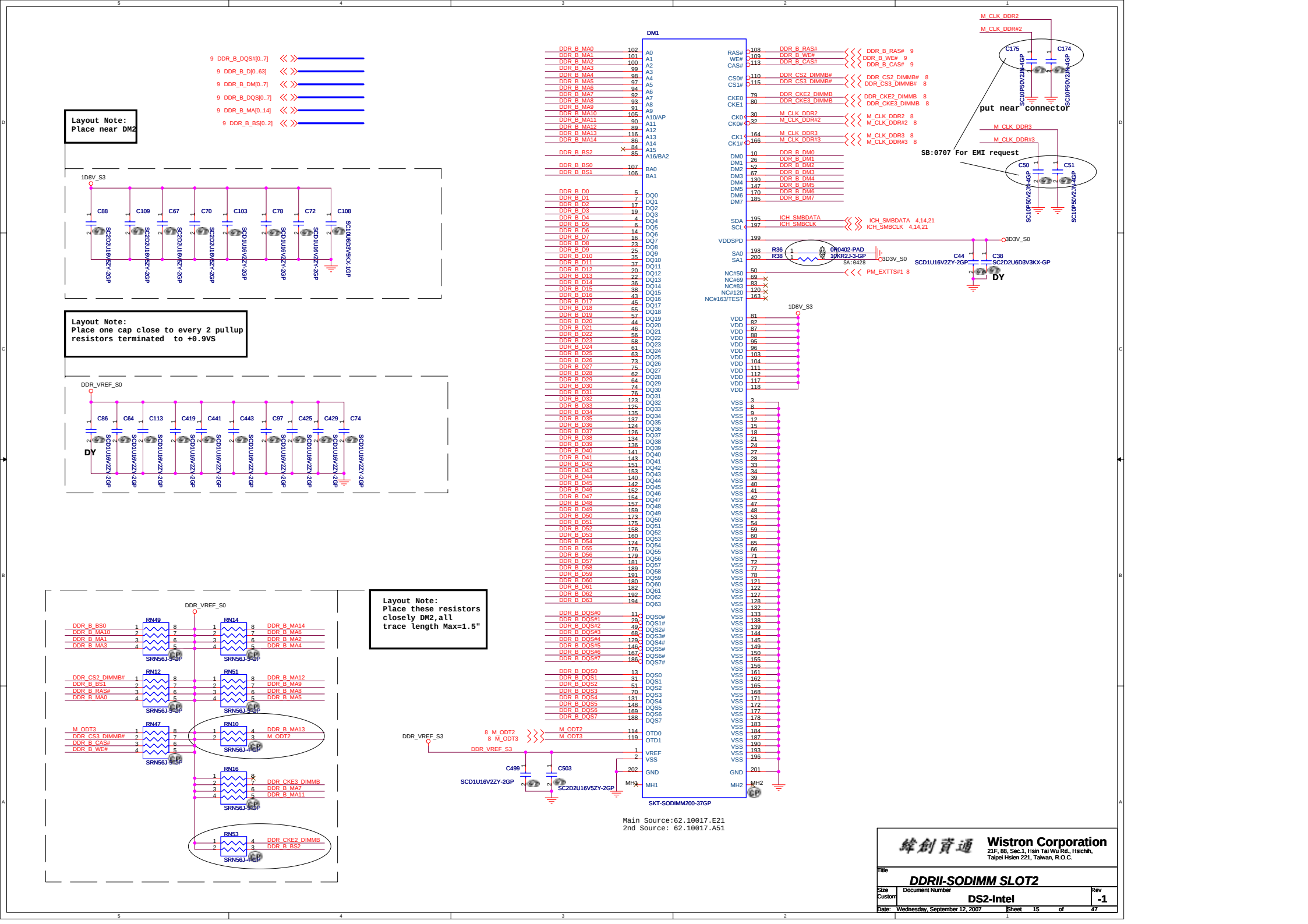
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRESTLINE(6/6)-PWR/GND

Size	Document Number	Rev
A3	DS2-Intel	-1

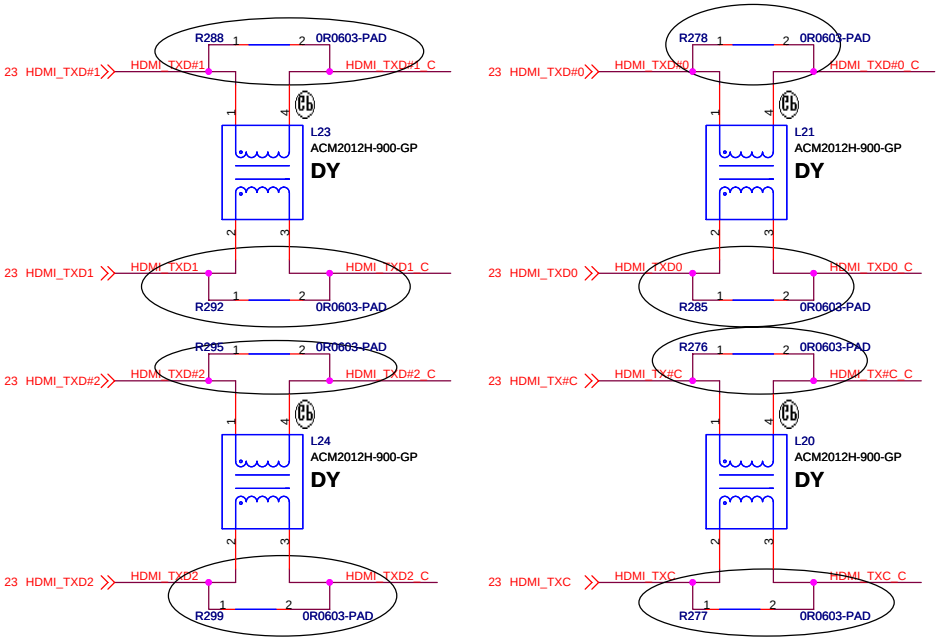
Date: Wednesday, September 12, 2007 Sheet 13 of 47

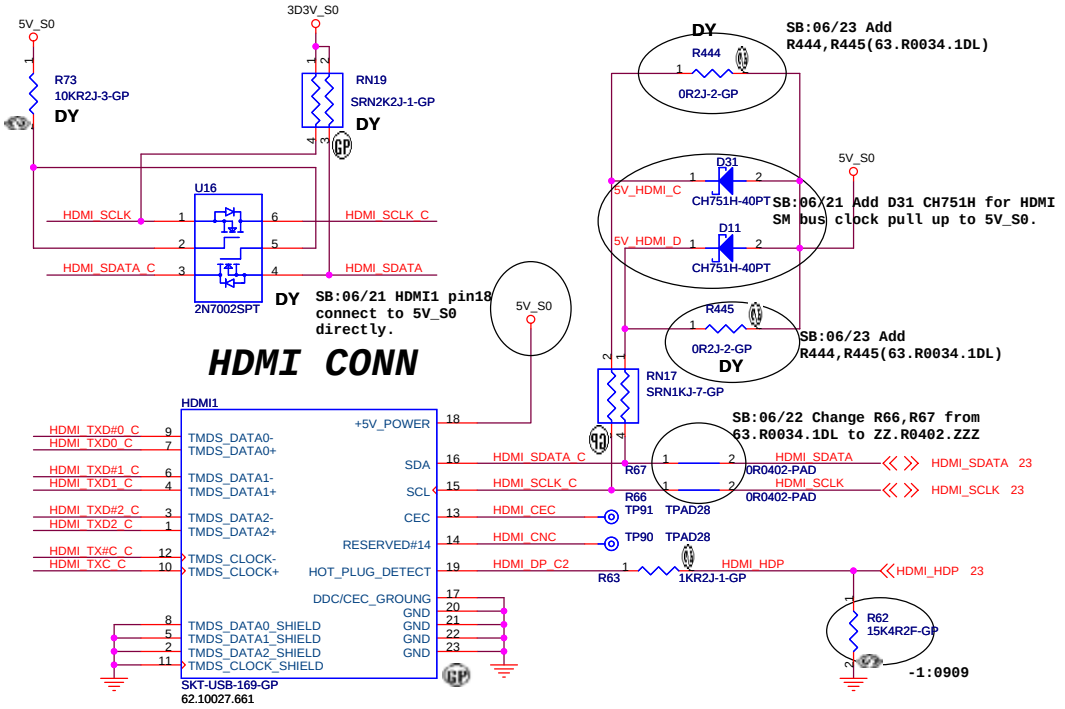

9 DDR_A_DQS#[0..7]
9 DDR_A_D[0..63]
9 DDR_A_DM[0..7]
9 DDR_A_DQS[0..7]
9 DDR_A_MA[0..14]
9 DDR_A_BS[0..2]
Layout Note:
Place near DM1
1D8V_S3
C91
C123
C77
C84
C81
C98
C69
C122
SC20U6D3V5KX-1GP
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS
DDR_VREF_S0
C112
C95
C73
C63
C423
C430
C438
C427
C85
C421
DY
SCD1U16V2ZY-2GP
change to 8P4R
DDR_VREF_S0
RN13
RN15
RN11
RN50
RN9
RN48
RN52
SRN56J-8GP
DDR_A_MA9
DDR_A_MA5
DDR_A_MA8
DDR_A_MA3
DDR_A_MA12
DDR_A_BS2
DDR_CKE0_DIMMA
DDR_A_MA1
DDR_A_MA10
DDR_A_BS0
DDR_A_WE#
DDR_A_MA0
DDR_A_MA2
DDR_A_MA4
DDR_A_MA6
DDR_A_CAS#
DDR_A_MA13
M_ODT1
DDR_CS1_DIMMA#
M_ODT0
DDR_CS0_DIMMA#
DDR_A_RAS#
DDR_A_BS1
DDR_A_MA7
DDR_A_MA11
DDR_A_MA14
DDR_CKE1_DIMMA
Layout Note:
Place these resistors
closely DM1,all
trace length Max=1.5"
DM2
MH1
MH2
SKT-SODIMM200-38GP
DDR_A_MA0
DDR_A_MA1
DDR_A_MA2
DDR_A_MA3
DDR_A_MA4
DDR_A_MA5
DDR_A_MA6
DDR_A_MA7
DDR_A_MA8
DDR_A_MA9
DDR_A_MA10
DDR_A_MA11
DDR_A_MA12
DDR_A_MA13
DDR_A_MA14
DDR_A_BS2
DDR_A_BS0
DDR_A_BS1
DDR_A_D0
DDR_A_D1
DDR_A_D2
DDR_A_D3
DDR_A_D4
DDR_A_D5
DDR_A_D6
DDR_A_D7
DDR_A_D8
DDR_A_D9
DDR_A_D10
DDR_A_D11
DDR_A_D12
DDR_A_D13
DDR_A_D14
DDR_A_D15
DDR_A_D16
DDR_A_D17
DDR_A_D18
DDR_A_D19
DDR_A_D20
DDR_A_D21
DDR_A_D22
DDR_A_D23
DDR_A_D24
DDR_A_D25
DDR_A_D26
DDR_A_D27
DDR_A_D28
DDR_A_D29
DDR_A_D30
DDR_A_D31
DDR_A_D32
DDR_A_D33
DDR_A_D34
DDR_A_D35
DDR_A_D36
DDR_A_D37
DDR_A_D38
DDR_A_D39
DDR_A_D40
DDR_A_D41
DDR_A_D42
DDR_A_D43
DDR_A_D44
DDR_A_D45
DDR_A_D46
DDR_A_D47
DDR_A_D48
DDR_A_D49
DDR_A_D50
DDR_A_D51
DDR_A_D52
DDR_A_D53
DDR_A_D54
DDR_A_D55
DDR_A_D56
DDR_A_D57
DDR_A_D58
DDR_A_D59
DDR_A_D60
DDR_A_D61
DDR_A_D62
DDR_A_D63
DDR_A_DQS0
DDR_A_DQS1
DDR_A_DQS2
DDR_A_DQS3
DDR_A_DQS4
DDR_A_DQS5
DDR_A_DQS6
DDR_A_DQS7
DDR_A_DQS#0
DDR_A_DQS#1
DDR_A_DQS#2
DDR_A_DQS#3
DDR_A_DQS#4
DDR_A_DQS#5
DDR_A_DQS#6
DDR_A_DQS#7
DDR_A_DM0
DDR_A_DM1
DDR_A_DM2
DDR_A_DM3
DDR_A_DM4
DDR_A_DM5
DDR_A_DM6
DDR_A_DM7
M_CLK_DDR0
M_CLK_DDR#0
M_CLK_DDR1
M_CLK_DDR#1
SA0
SA1
R37
R39
0R0402-PAD
SA:8428
VDD_SPD
3D3V_S0
1D8V_S3
C41
C46
SCD1U16V2ZY-2GP
SC2D2U6D3V3KX-GP
DY
8 PM_EXTTS#0
8 DDR_CS0_DIMMA#
8 DDR_CS1_DIMMA#
8 DDR_CKE0_DIMMA
8 DDR_CKE1_DIMMA
9 DDR_A_RAS#
9 DDR_A_CAS#
9 DDR_A_WE#
4,15,21 ICH_SMBCLK
4,15,21 ICH_SMBDATA
8 M_ODT0
8 M_ODT1
DDR_VREF_S3
C184
C185
SCD1U16V2ZY-2GP
SC2D2U16V5ZY-2GP
SB:0707 For EMI request
put near connector
C476
C477
C388
C391
SC10P50V2JN-4GP
Main Source:62.10017.E31
2nd Source: 62.10017.A41
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDRII-SODIMM SLOT1
Size
Custom
Document Number
DS2-Intel
Rev
-1
Date: Wednesday, September 12, 2007
Sheet 14 of 47



Wistron Corporation	蜂創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: DDRII-SODIMM SLOT2	
Size: Custom	Document Number: DS2-Intel
Rev: -1	
Date: Wednesday, September 12, 2007	Sheet 15 of 47

HDMI I/F & CONNECTOR





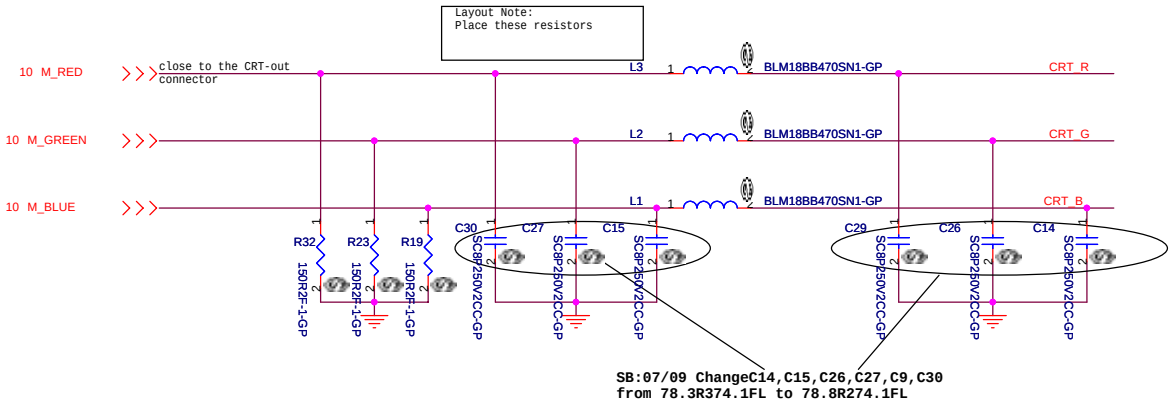
TV OUT CONN (Optional) Move to Right I/O Board

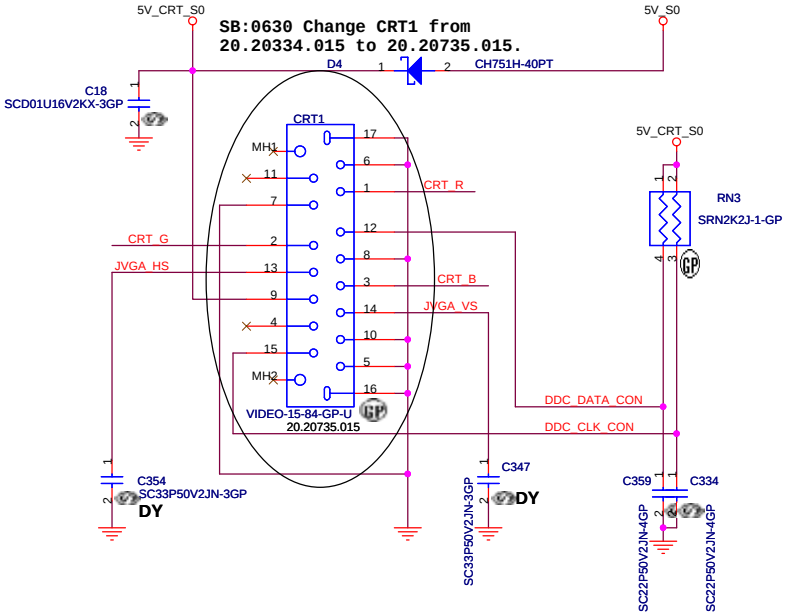
<Core Design>

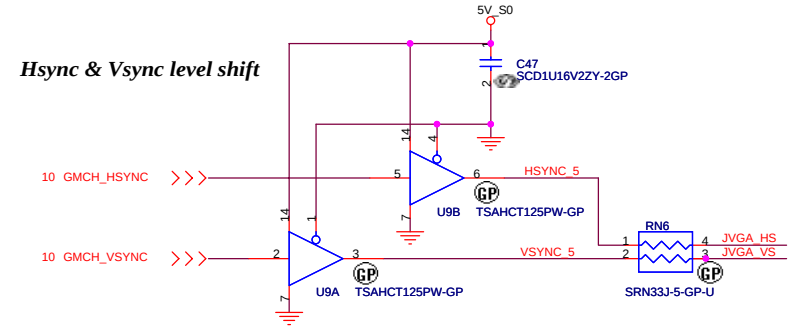
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

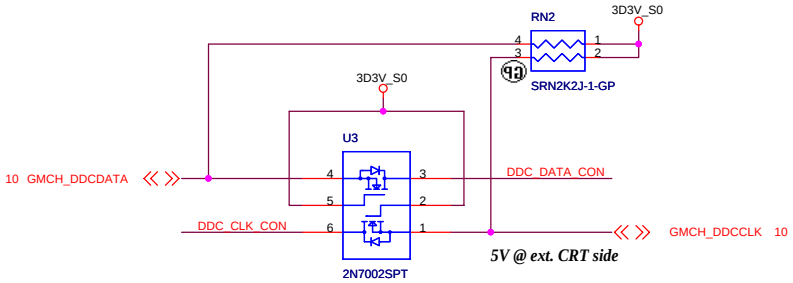
Title	HDMI/TV Connector	
Size A3	Document Number DS2-Intel	Rev -1
Date: Wednesday, September 12, 2007	Sheet 16 of 47	

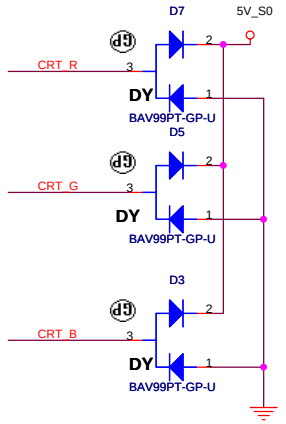
CRT I/F & CONNECTOR











<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Connector

Size	Document Number	Rev
A3	DS2-Intel	-1

Date: Wednesday, September 12, 2007 Sheet 17 of 47

SC:08/09 Add LCD2 (20.F1093.040) ,please check LCD1 and LCD 2 layout overlap possibility.

SC:08/15 Rename "LCD2" to "LCD1"

SC:08/05 Change C57 from 78.10423.5FL to 78.10523.5BL

-1:08/29 Change LCD1 pin 31 from GND to NC

-1:09/02 Add R460 to prevent power short to GND via "LCD_CBL_DET#"

SC:08/09 Add EC161(78.10491.4FL) for EMI request .Default is DUMMY

SC:08/13 Add EC167,EC168(78.10034.1FL), R460,R461(63.R0034.1DL) place cross LVDS CLK A,Bpair. Default is DY.This is for RF request.

-1:08/29 Change LVDS channel A and channel B EMI solution. this is for antena team request.

SC:08/13 Add EC169,EC170,EC171, R462,R463,R464 on LVDS channel A each data pairs. This is for RF request .Default is DY.

INVERTER POWER

Mic Power

600ohm 100MHz
200mA 0.5ohm DC

SC:08/09 Add EC154(78.10491.4FL) for EMI request .Default is DUMMY

CAMERA Power

SC:08/09 Add EC153(78.10491.4FL) for EMI request .Default is DUMMY

SC:08/09 Add EC151(78.22124.2FL) for EMI request .Default is DUMMY

SC:08/09 Add EC152(78.22124.2FL) for EMI request .Default is DUMMY

SC:08/03 Add D32 ,R456 connect to U49 pin3 and delete R46 that are for LCD test function.

LCD POWER

SC:08/09 Add EC157(78.33034.1FL) for EMI request .Default is DUMMY

SC:08/09 Add EC156(78.33034.1FL) for EMI request .Default is DUMMY

SC:08/09 Add EC155(78.33034.1EL) for EMI request .Default is DUMMY

-1:09/11

SC:08/13 Change L12 pin connection.pin 1 connect to "USB_PN6", pin4 connect to "USB_PP6" . This change is for layout request.

-1:09/11

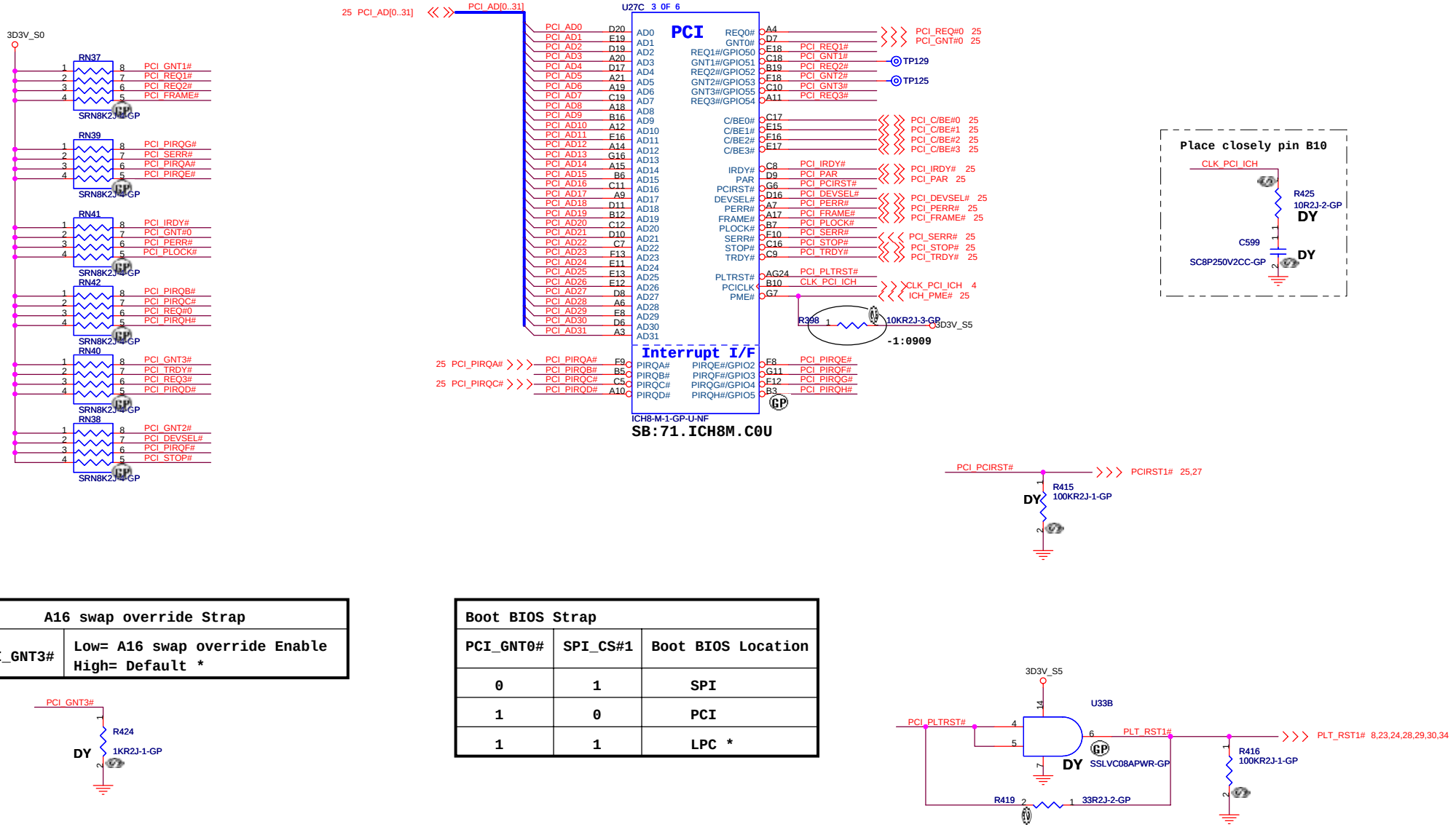
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD/Inverter Connector

Size: Custom | Document Number: DS2-Intel | Rev: -1

Date: Wednesday, September 12, 2007 | Sheet 18 of 47



A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *

Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

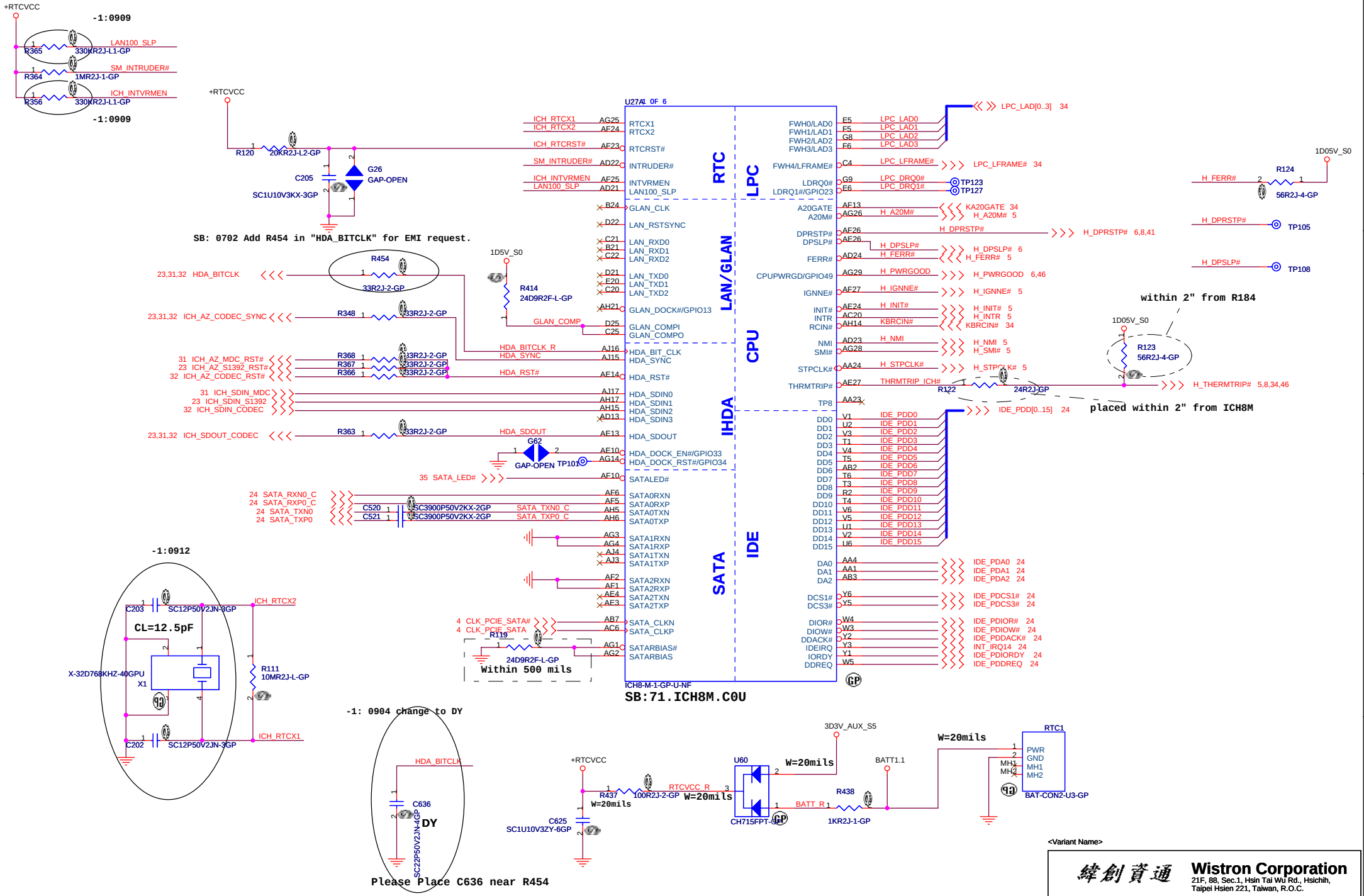
<Variant Name>

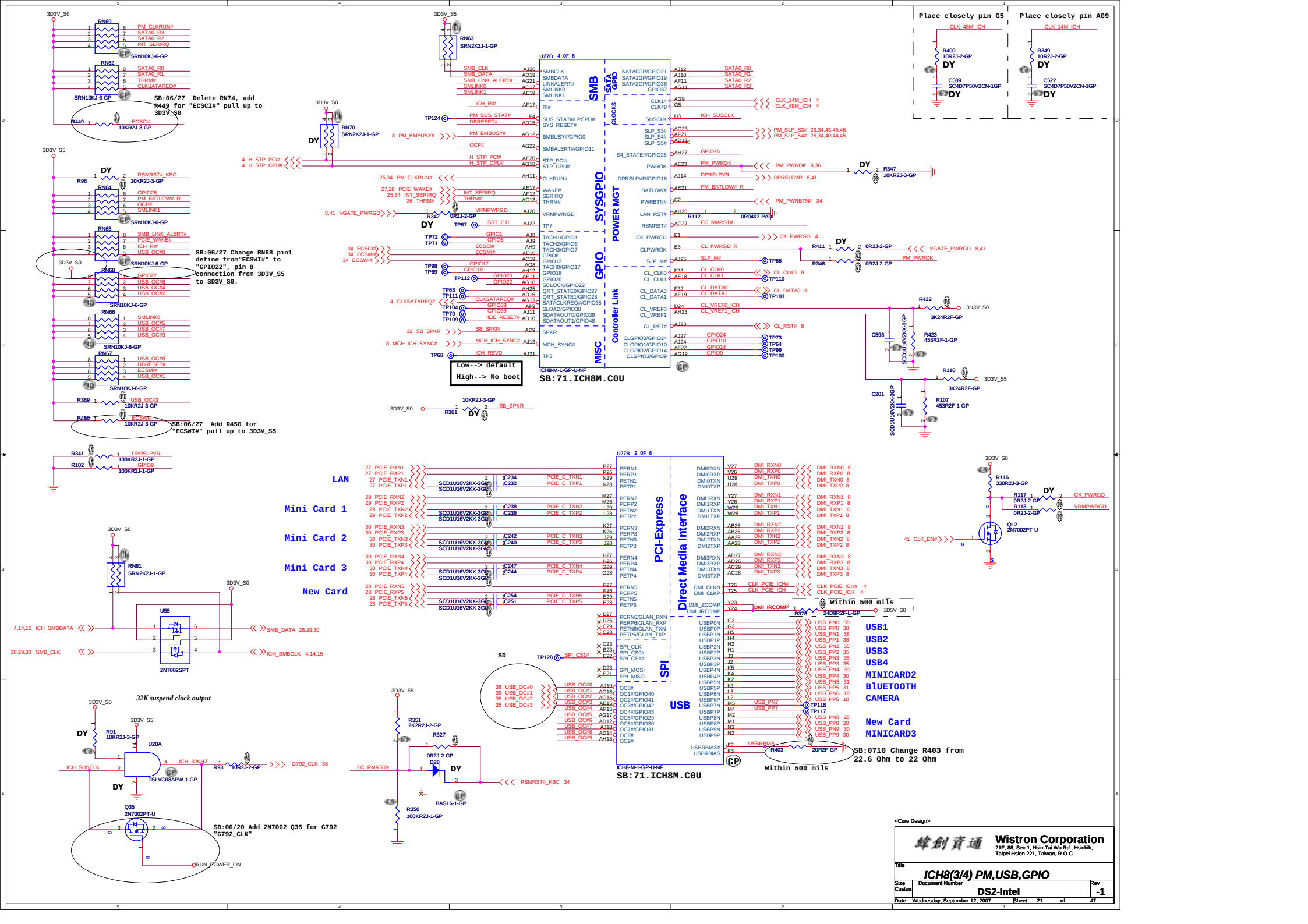
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

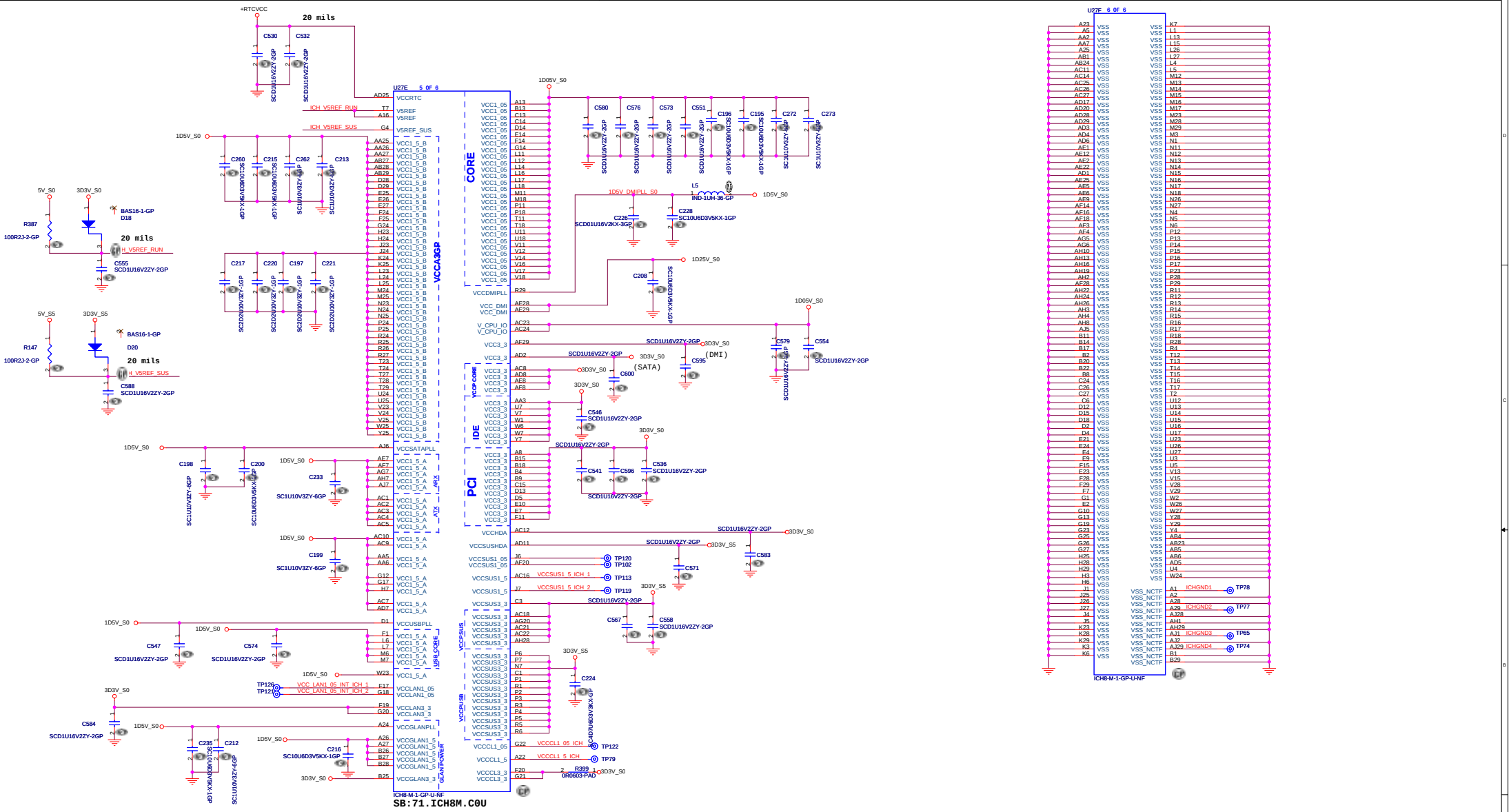
Title: ICH8(1/4)-PCI/INT

Size: A3 | Document Number: DS2-Intel | Rev: -1

Date: Wednesday, September 12, 2007 | Sheet 19 of 47


+RTCVCC
-1:0909
LAN100_SLP
R365
330KR2J-L1-GP
SM_INTRUDER#
R364
1MR2J-1-GP
ICH_INTVRMEN
R356
330KR2J-L1-GP
-1:0909
+RTCVCC
R120
20KR2J-L2-GP
C205
SC1U10V3KX-3GP
G26
GAP-OPEN
SB: 0702 Add R454 in "HDA_BITCLK" for EMI request.
R454
33R2J-2-GP
23,31,32 HDA_BITCLK
R348
33R2J-2-GP
23,31,32 ICH_AZ_CODEC_SYNC
R368
R367
R366
33R2J-2-GP
31 ICH_AZ_MDC_RST#
23 ICH_AZ_S1392_RST#
32 ICH_AZ_CODEC_RST#
31 ICH_SDIN_MDC
23 ICH_SDIN_S1392
32 ICH_SDIN_CODEC
R363
23,31,32 ICH_SDOUT_CODEC
1D5V_S0
R414
24D9R2F-L-GP
G62
GAP-OPEN
TP101
35 SATA_LED#
24 SATA_RXN0_C
24 SATA_RXP0_C
24 SATA_TXN0
24 SATA_TXP0
C520
C521
SC3900P50V2KX-2GP
SATA_TXN0_C
SATA_TXP0_C
4 CLK_PCIE_SATA#
4 CLK_PCIE_SATA
R119
24D9R2F-L-GP
Within 500 mils
U27A1 OF 6
ICH_RTCX1
ICH_RTCX2
ICH_RTCRST#
SM_INTRUDER#
ICH_INTVRMEN
LAN100_SLP
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#/GPIO13
GLAN_COMP
GLAN_COMPI
GLAN_COMPO
HDA_BITCLK_R
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
RTC
LAN/GLAN
CPU
IHDA
SATA
LPC
IDE
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD/GPIO49
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
TP8
DD0
DD1
DD2
DD3
DD4
DD5
DD6
DD7
DD8
DD9
DD10
DD11
DD12
DD13
DD14
DD15
DA0
DA1
DA2
DCS1#
DCS3#
DIOR#
DIOW#
DDACK#
IDEIRQ
IORDY
DDREQ
ICH8-M-1-GP-U-NF
LPC_LAD[0..3] 34
LPC_LAD0
LPC_LAD1
LPC_LAD2
LPC_LAD3
LPC_LFRAME# 34
LPC_DRQ0#
LPC_DRQ1#
TP123
TP127
KA20GATE 34
H_A20M# 5
H_DPRSTP# 6,8,41
H_DPSLP# 6
H_FERR# 5
H_PWRGOOD 6,46
H_IGNNE# 5
H_INIT# 5
H_INTR 5
KBRCIN# 34
H_NMI 5
H_SMI# 5
H_STPCLK# 5
H_THERMTRIP# 5,8,34,46
IDE_PDD[0..15] 24
IDE_PDA0 24
IDE_PDA1 24
IDE_PDA2 24
IDE_PDCS1# 24
IDE_PDCS3# 24
IDE_PDIOR# 24
IDE_PDIOW# 24
IDE_PDDACK# 24
INT_IRQ14 24
IDE_PDIORDY 24
IDE_PDDREQ 24
SB:71.ICH8M.C0U
1D05V_S0
R124
56R2J-4-GP
H_FERR#
H_DPRSTP#
TP105
H_DPSLP#
TP108
within 2" from R184
R123
56R2J-4-GP
R122
24R2J-GP
placed within 2" from ICH8M
-1:0912
C203
SC12P50V2JN-3GP
CL=12.5pF
X-32D768KHZ-40GPU
X1
R111
10MR2J-L-GP
C202
SC12P50V2JN-3GP
ICH_RTCX2
ICH_RTCX1
-1: 0904 change to DY
HDA_BITCLK
C636
SC22P50V2JN-4GP
DY
Please Place C636 near R454
+RTCVCC
R437
100R2J-2-GP
W=20mils
RTCVCC_R
C625
SC1U10V3ZY-6GP
U60
CH715FPT-GP
3D3V_AUX_S5
W=20mils
BATT1.1
R438
1KR2J-1-GP
BATT_R
RTC1
BAT-CON2-U3-GP
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8(2/4) LAN,HD,IDE,LPC
Size
A3
Document Number
DS2-Intel
Rev
-1
Date: Wednesday, September 12, 2007
Sheet 20 of 47


Place closely pin G5
Place closely pin AG9
SB:06/27 Delete RN74, add R449 for "ECSCI#" pull up to 3D3V_S0
SB:06/27 Change RN68 pin1 define from"ECSWI#" to "GPIO22", pin 8 connection from 3D3V_S5 to 3D3V_S0.
SB:06/27 Add R450 for "ECSWI#" pull up to 3D3V_S5
Low--> default
High--> No boot
SB:71.ICH8M.C0U
LAN
Mini Card 1
Mini Card 2
Mini Card 3
New Card
SD
USB1
USB2
USB3
USB4
MINICARD2
BlUETOOTH
CAMERA
New Card
MINICARD3
Within 500 mils
SB:0710 Change R403 from 22.6 Ohm to 22 Ohm
32K suspend clock output
SB:06/20 Add 2N7002 Q35 for G792 "G792_CLK"
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ICH8(3/4) PM,USB,GPIO
DS2-Intel
-1
Wednesday, September 12, 2007
21
47



<variant_name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH8(4/4) POWER&GND

Size: A2 | Document Number: DS2-Intel | Rev: -1

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SB:06/22 Change R279,R280,R281,R282 from 63.30134.1DL
to 63.12134.1DL

SB:06/22 Change R291 from 64.75005.6DL to
64.56005.6DL

SB: 0710 Change R345 from 33 Ohm to 0
Ohm

-1:09/06 Change EC83 from ASM to DUMMY.

LAYOUT must support
connectors from JAE,
Molex, and Acon

550mA

30mA

<Core Design>

Wistron Corporation
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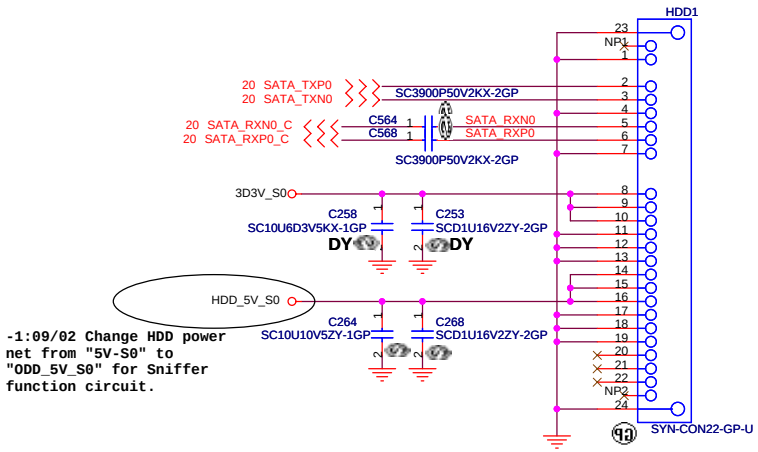
Taipei Hsien 221, Taiwan, R.O.C.

Title: Sil 1392 HDMI

Size: A3 | Document Number: DS2-Intel | Rev: -1

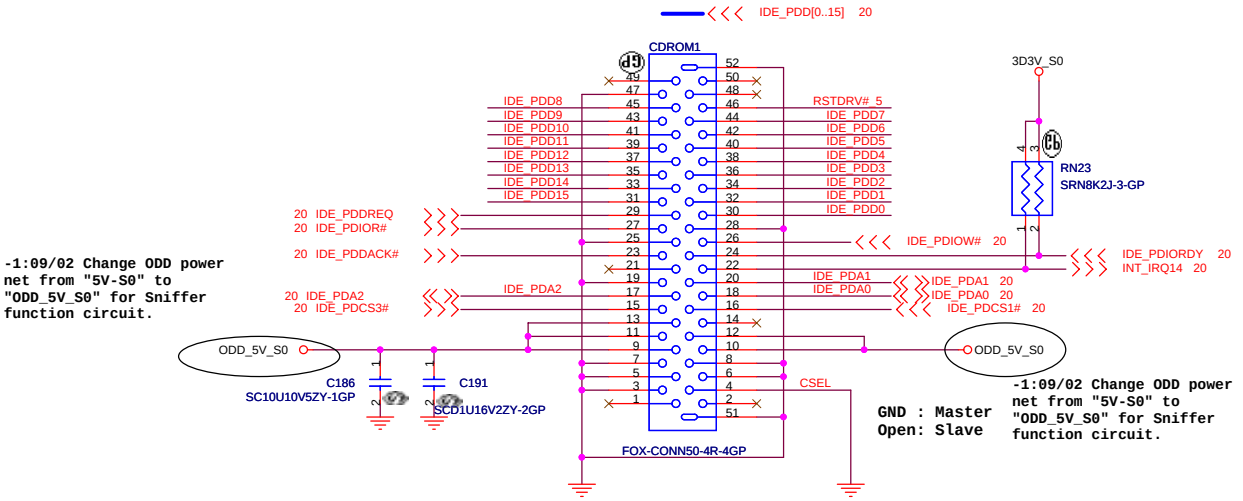
Date: Wednesday, September 12, 2007 | Sheet 23 of 47

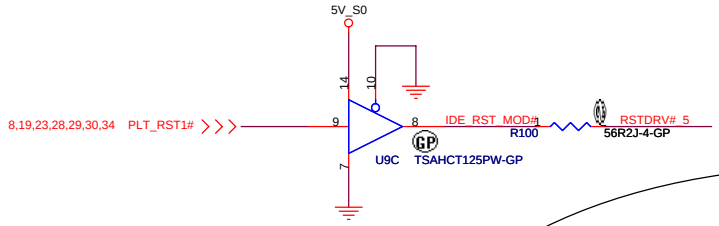
SATA HD Connector

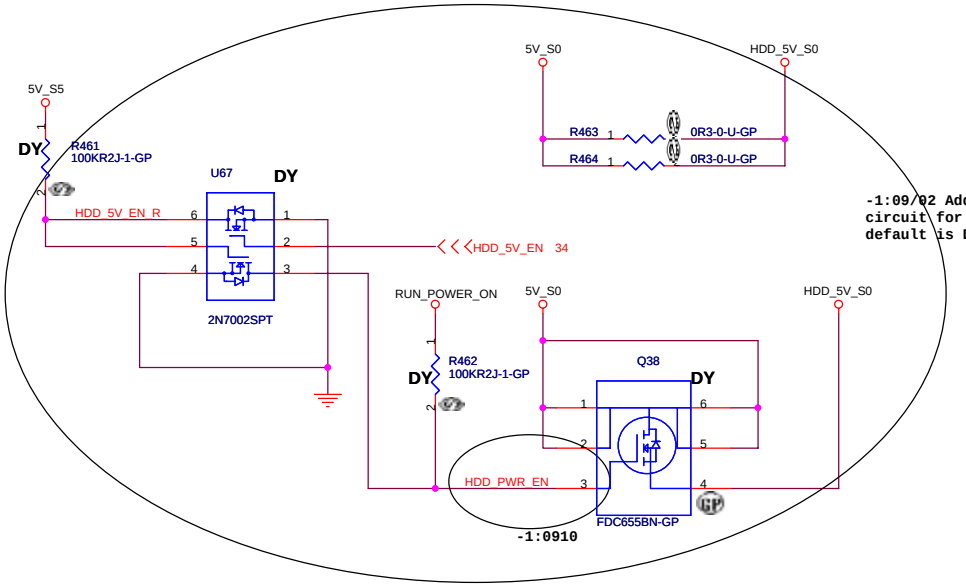


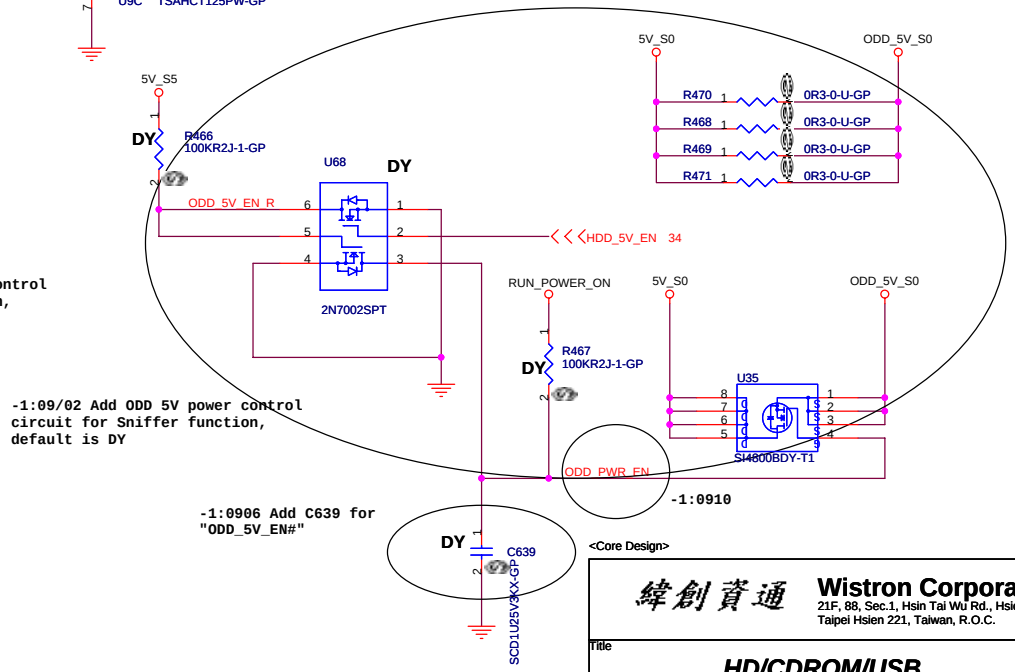
Main Source:20.80919.022

CD-ROM Connector









<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **HD/CDROM/USB**

Size	Document Number	Rev
A3	DS2-Intel	-1

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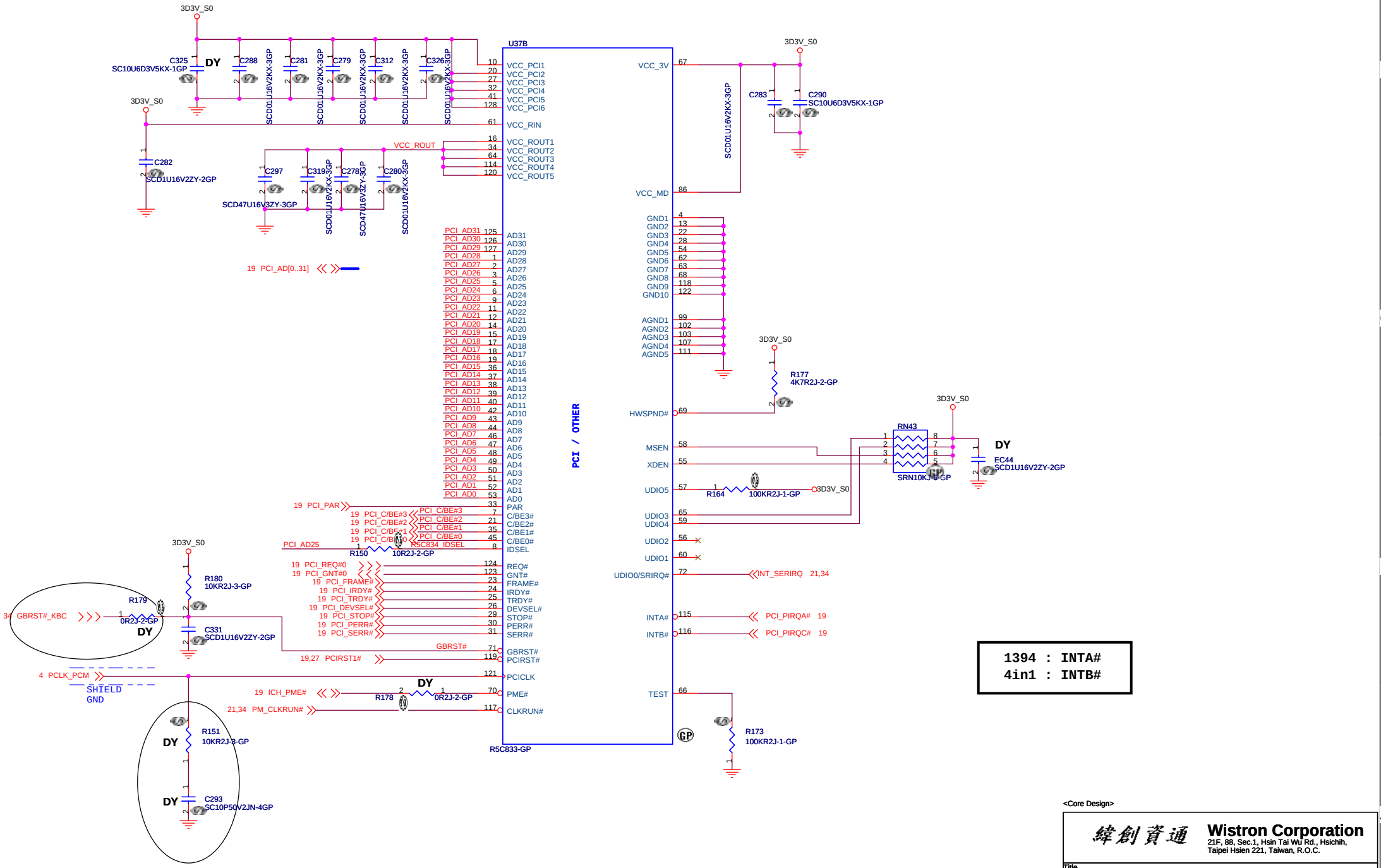
U37B
R5C833-GP
PCI / OTHER
3D3V_S0
C325
SC10U6D3V5KX-1GP
DY
C288
C281
C279
C312
C326
SCD01U16V2KX-3GP
C282
SCD1U16V2ZY-2GP
C297
SCD47U16V3ZY-3GP
C319
C278
C280
VCC_ROUT
VCC_PCI1
VCC_PCI2
VCC_PCI3
VCC_PCI4
VCC_PCI5
VCC_PCI6
VCC_RIN
VCC_ROUT1
VCC_ROUT2
VCC_ROUT3
VCC_ROUT4
VCC_ROUT5
VCC_3V
VCC_MD
C283
C290
SC10U6D3V5KX-1GP
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
GND10
AGND1
AGND2
AGND3
AGND4
AGND5
R177
4K7R2J-2-GP
HWSPND#
MSEN
XDEN
UDIO5
UDIO3
UDIO4
UDIO2
UDIO1
UDIO0/SRIRQ#
INTA#
INTB#
TEST
RN43
SRN10KJ-GP
EC44
SCD1U16V2ZY-2GP
R164
100KR2J-1-GP
INT_SERIRQ 21,34
PCI_PIRQA# 19
PCI_PIRQC# 19
R173
100KR2J-1-GP
19 PCI_AD[0..31]
PCI_AD31
PCI_AD30
PCI_AD29
PCI_AD28
PCI_AD27
PCI_AD26
PCI_AD25
PCI_AD24
PCI_AD23
PCI_AD22
PCI_AD21
PCI_AD20
PCI_AD19
PCI_AD18
PCI_AD17
PCI_AD16
PCI_AD15
PCI_AD14
PCI_AD13
PCI_AD12
PCI_AD11
PCI_AD10
PCI_AD9
PCI_AD8
PCI_AD7
PCI_AD6
PCI_AD5
PCI_AD4
PCI_AD3
PCI_AD2
PCI_AD1
PCI_AD0
AD31
AD30
AD29
AD28
AD27
AD26
AD25
AD24
AD23
AD22
AD21
AD20
AD19
AD18
AD17
AD16
AD15
AD14
AD13
AD12
AD11
AD10
AD9
AD8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
19 PCI_PAR
PAR
19 PCI_C/BE#3
19 PCI_C/BE#2
19 PCI_C/BE#1
19 PCI_C/BE#0
C/BE3#
C/BE2#
C/BE1#
C/BE0#
PCI_AD25
R150
10R2J-2-GP
R5C834_IDSEL
IDSEL
19 PCI_REQ#0
19 PCI_GNT#0
19 PCI_FRAME#
19 PCI_IRDY#
19 PCI_TRDY#
19 PCI_DEVSEL#
19 PCI_STOP#
19 PCI_PERR#
19 PCI_SERR#
REQ#
GNT#
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
PERR#
SERR#
R180
10KR2J-3-GP
R179
0R2J-2-GP
34 GBRST#_KBC
C331
SCD1U16V2ZY-2GP
GBRST#
19,27 PCIRST1#
GBRST#
PCIRST#
4 PCLK_PCM
SHIELD
GND
PCICLK
19 ICH_PME#
R178
0R2J-2-GP
PME#
21,34 PM_CLKRUN#
CLKRUN#
R151
10KR2J-3-GP
C293
SC10P50V2JN-4GP
1394 : INTA#
4in1 : INTB#
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
R5C833/PCI
Size
A3
Document Number
DS2-Intel
Rev
-1
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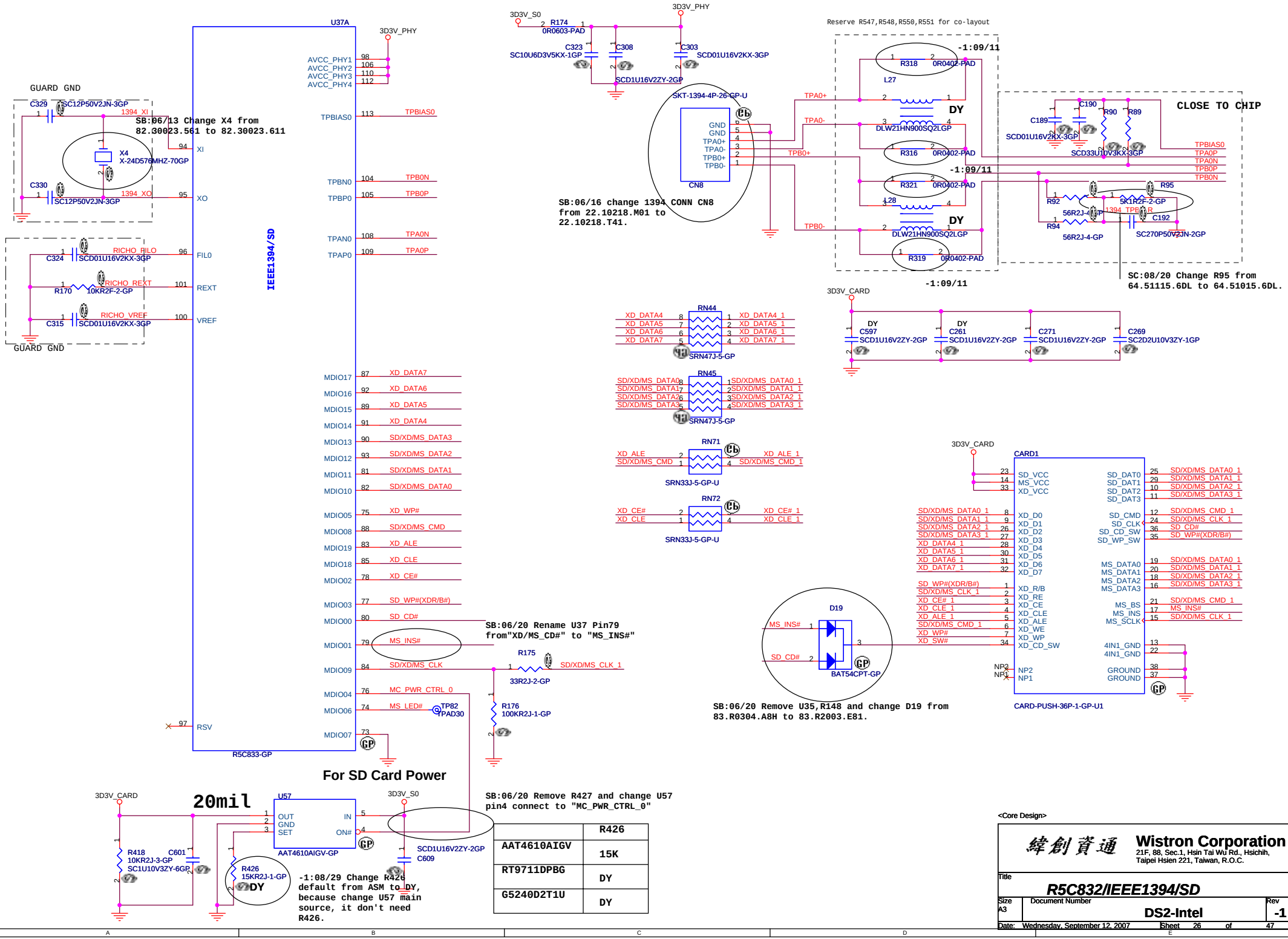

	R426
AAT4610AIGV	15K
RT9711DPBG	DY
G5240D2T1U	DY

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: R5C832/IEEE1394/SD

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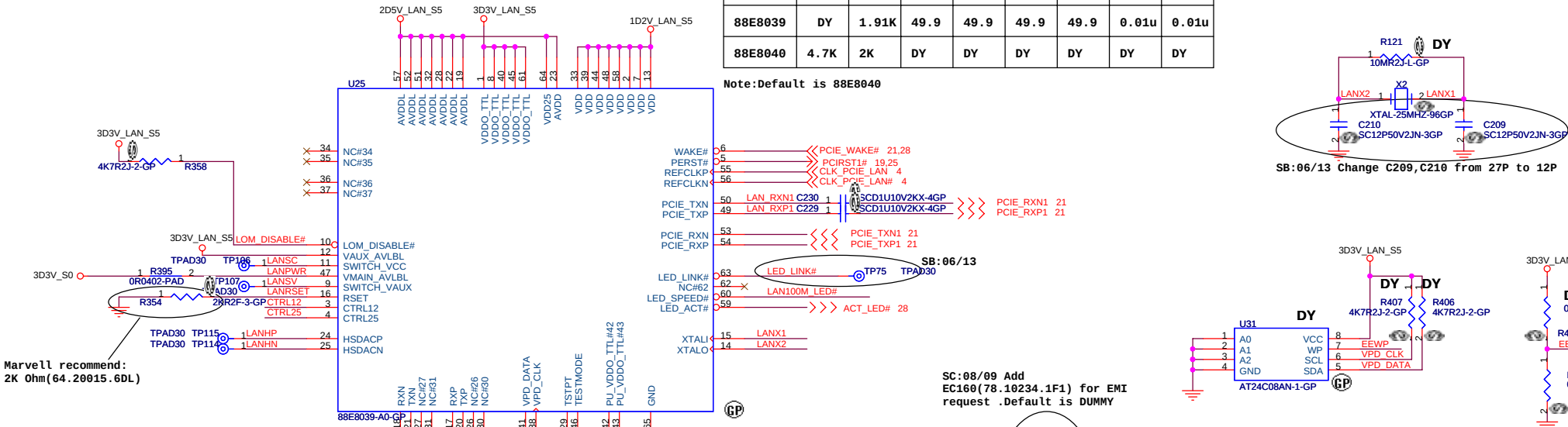
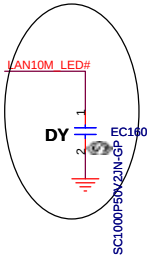
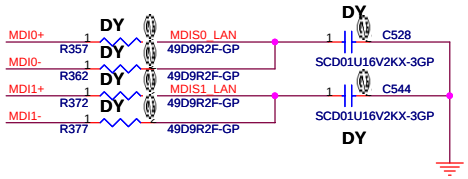
	R394	R354	R357	R362	R372	R377	C528	C544
88E8039	DY	1.91K	49.9	49.9	49.9	49.9	0.01u	0.01u
88E8040	4.7K	2K	DY	DY	DY	DY	DY	DY

Note:Default is 88E8040

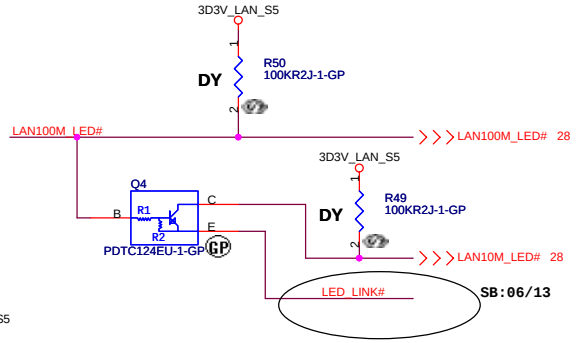


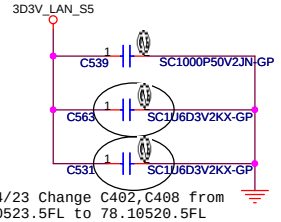
SC:08/09 Add EC160(78.10234.1F1) for EMI request .Default is DUMMY



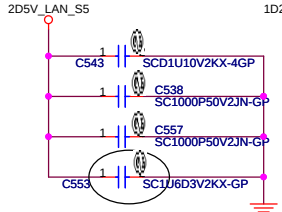


	R397	Q15	R417	Q17
88E8039	4K7	2SB772PT	4K7	2SB772PT
88E8040	DY	DY	DY	DY

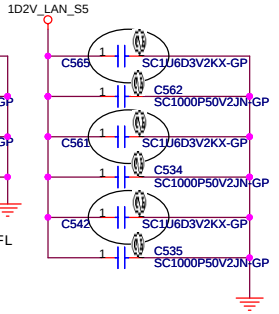


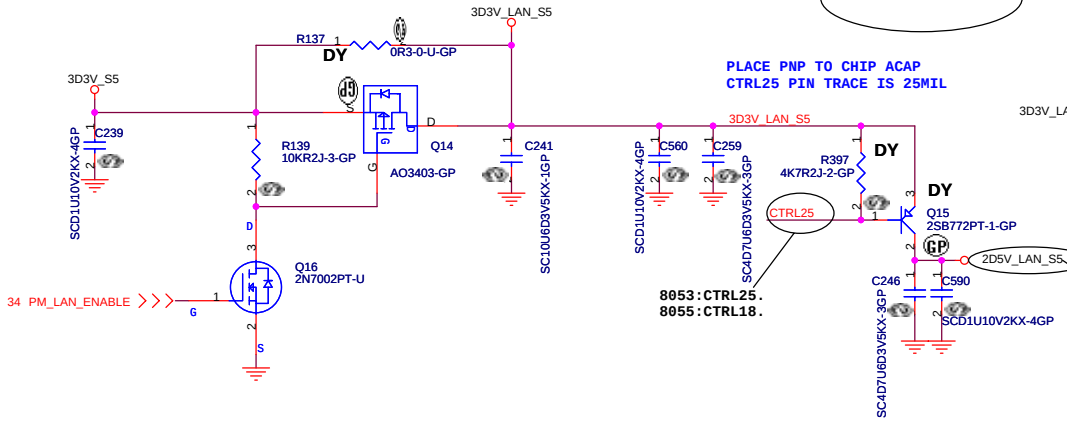


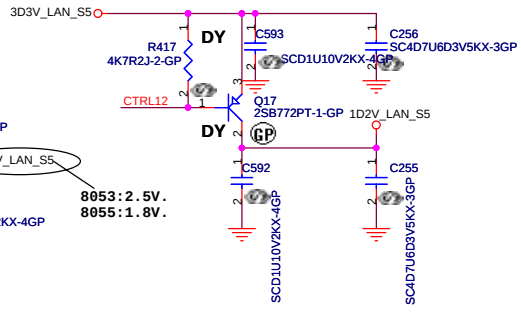
SA:04/23 Change C402,C408 from 78.10523.5FL to 78.10520.5FL



SA:04/23 Change C411 from 78.10523.5FL to 78.10520.5FL







<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN MARVELL

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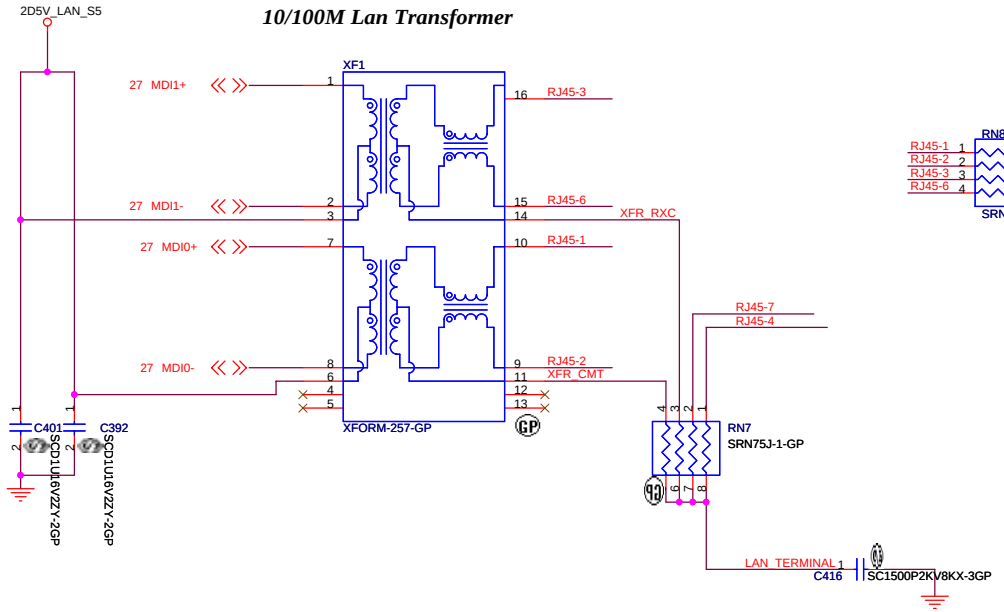
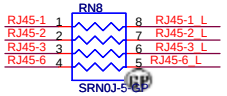
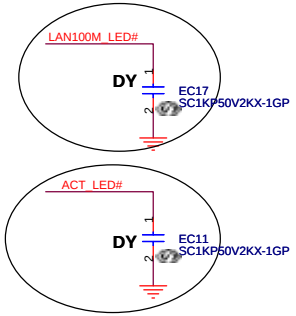
RJ45 Connector

10/100M Lan Transformer

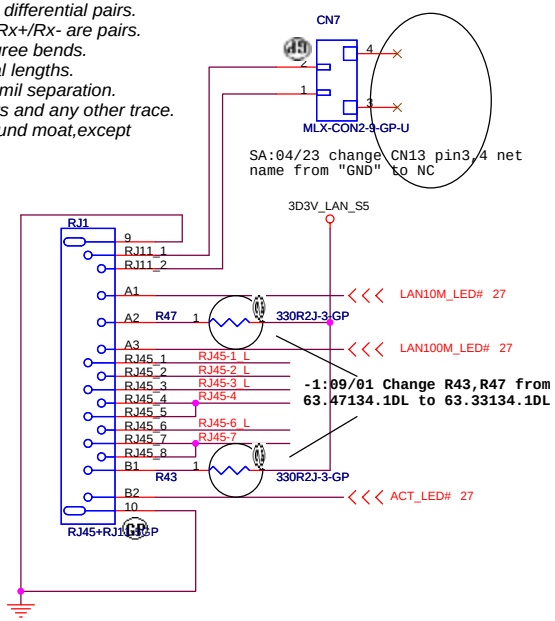




1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

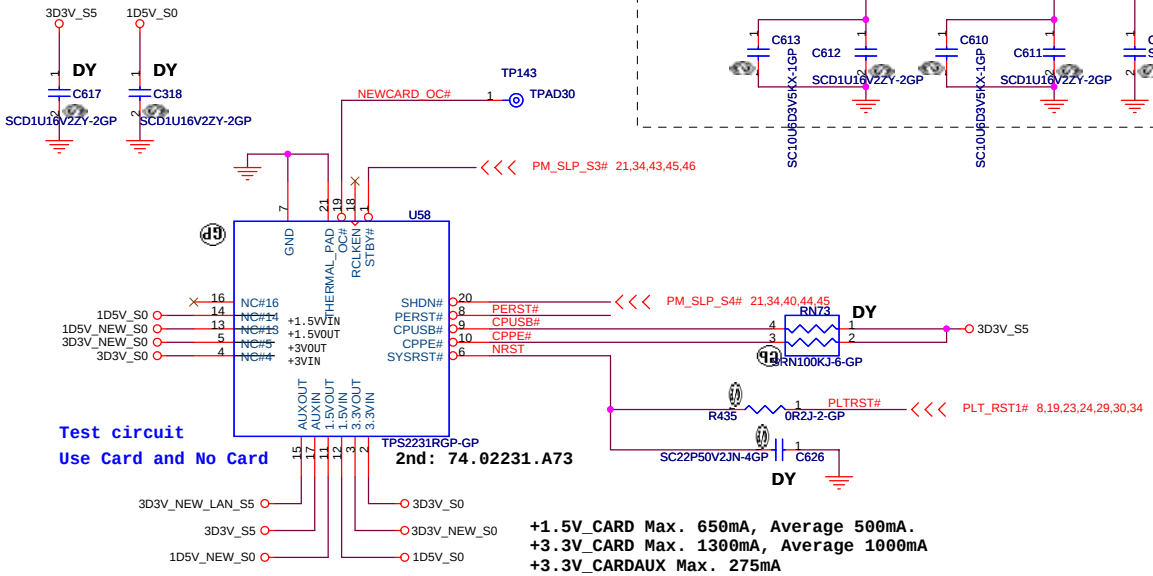


Green : Link up
Blinking : TX/RX activity

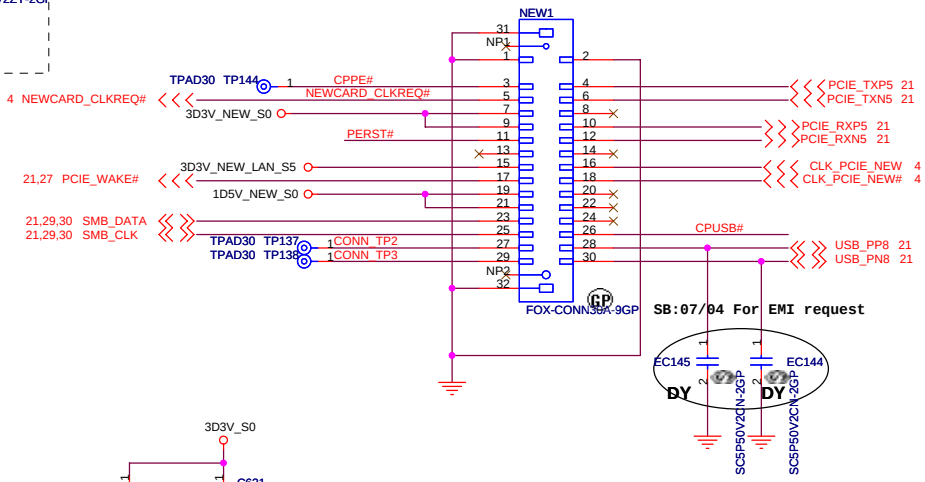


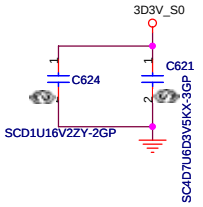
NEWCARD Connector

Place them Near to Chip



Place them Near to Connector





+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

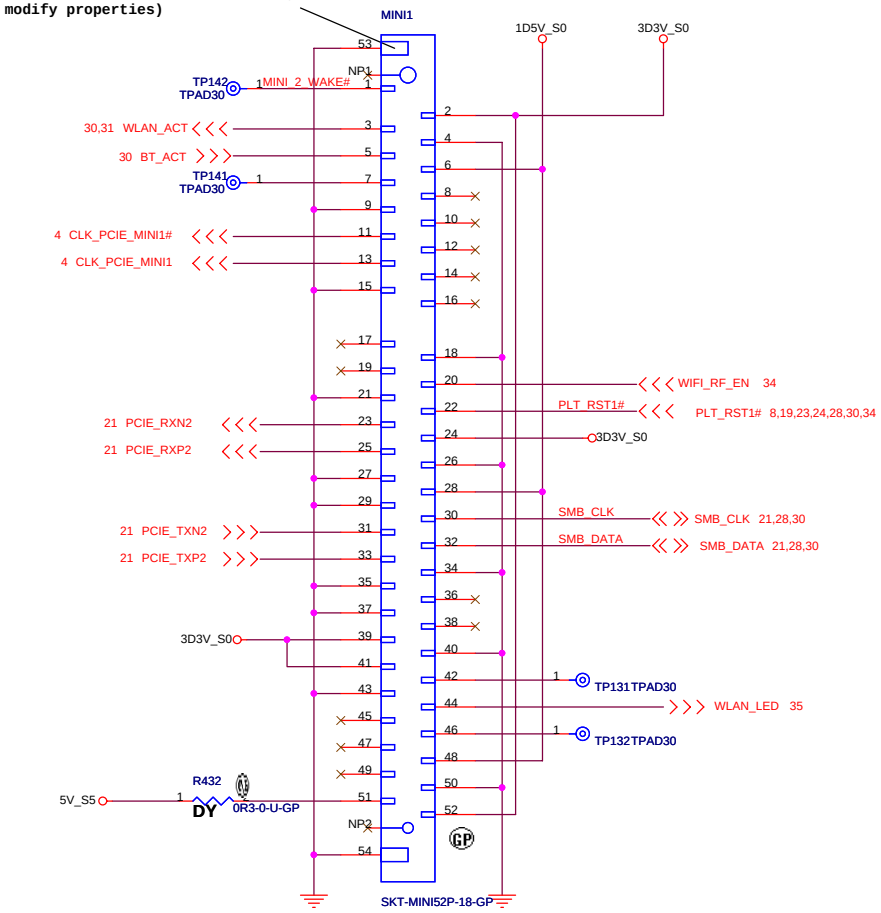
Title: LAN connector/NEW CARD/SIM

Size	Document Number	Rev
A3	DS2-Intel	-1

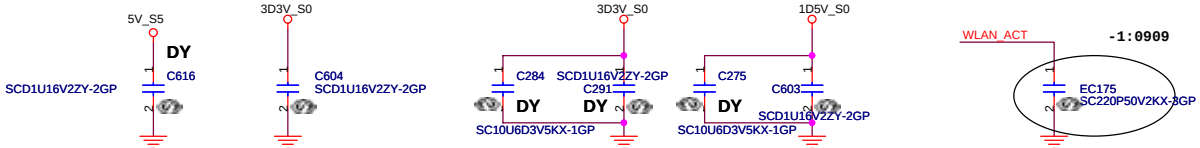
Date: Wednesday, September 12, 2007 Sheet 28 of 47

Mini Card Connector 1(802.11a/b/g)

SB:06/22 Change MINI1,2,3 slot from 62.10043.431 to 62.10043.551(only modify properties)



Main Source:62.10043.431
2nd Source: 20.F0992.052



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI CARD CONN 1

Size	Document Number	Rev
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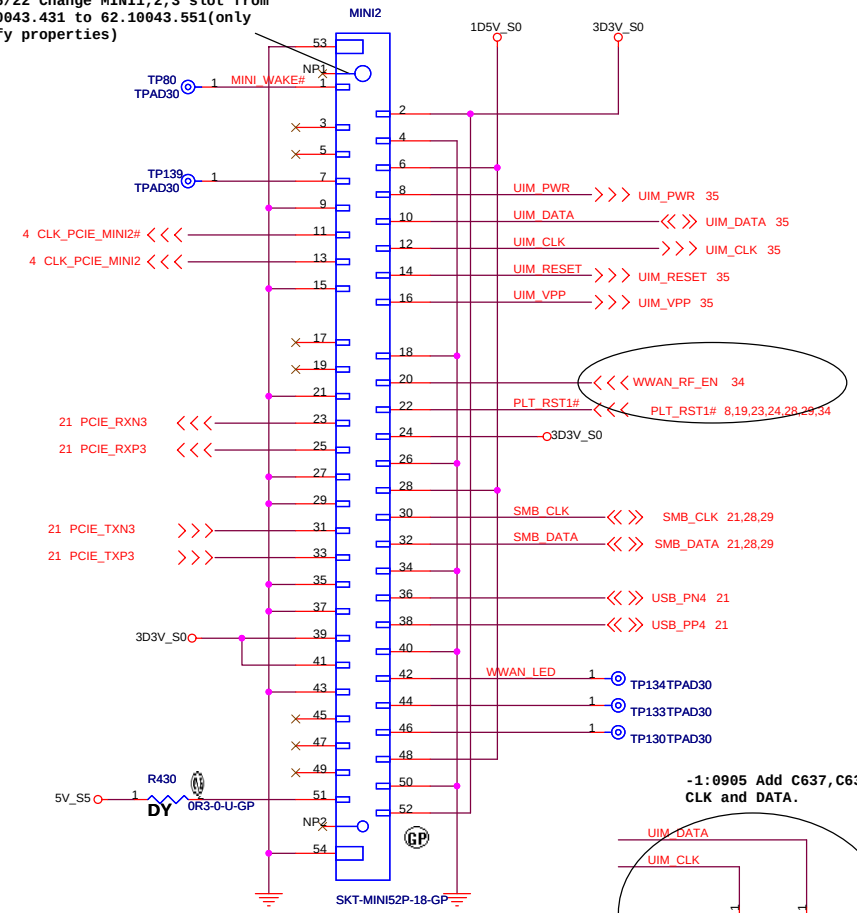
Date: Wednesday, September 12, 2007 Sheet 29 of 47

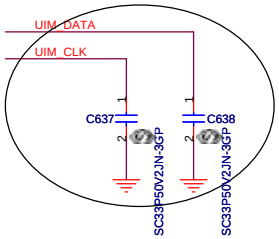
Mini Card Connector
Mini Card Connector 2(WWAN)

SB:06/22 Change MINI1,2,3 slot from 62.10043.431 to 62.10043.551(only modify properties)

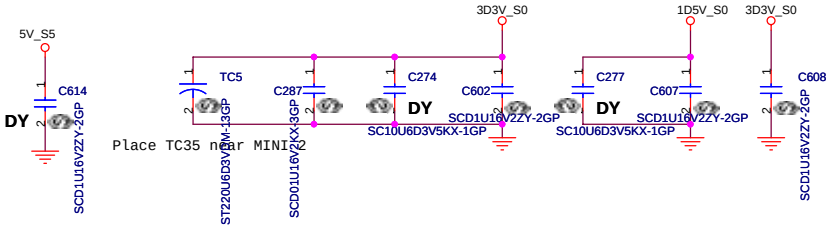


SC:07/30 Add "WWAN_RF_EN" GPIO pin connect to MINI2 pin20

-1:0905 Add C637,C638 for SIM CLK and DATA.



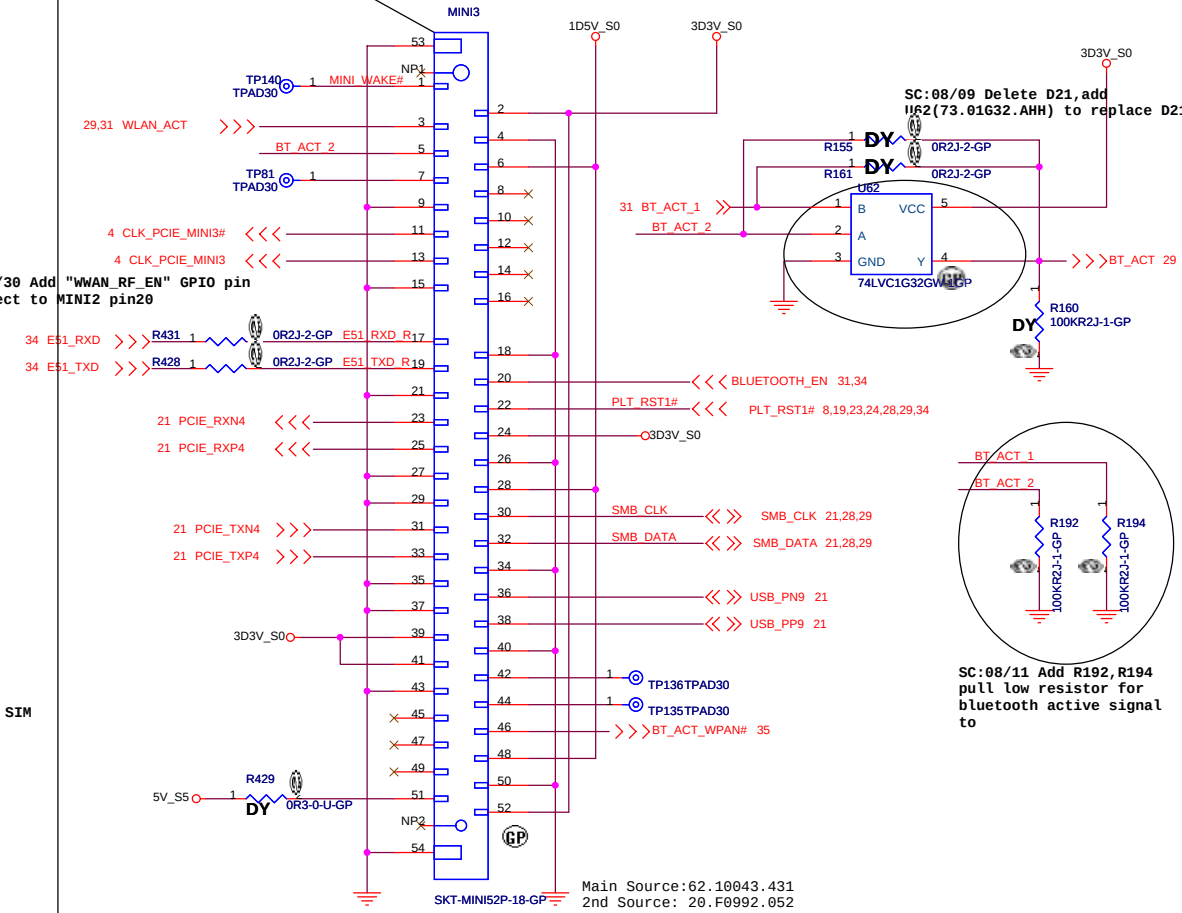
Main Source:62.10043.431
2nd Source: 20.F0992.052



Place TC35 near MINI2

Mini Card Connector 3(Robson)

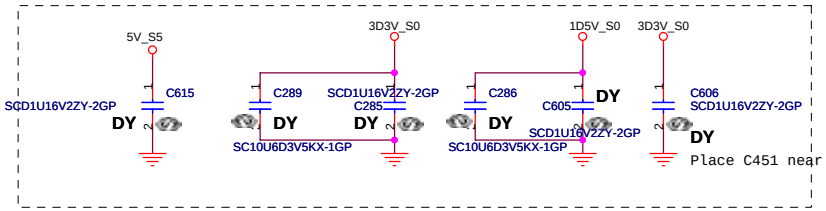
SB:06/22 Change MINI1,2,3 slot from 62.10043.431 to 62.10043.551(only modify properties)



SC:08/09 Delete D21,add U62(73.01G32.AHH) to replace D21

SC:08/11 Add R192,R194 pull low resistor for bluetooth active signal to

Main Source:62.10043.431
2nd Source: 20.F0992.052



Place C451 near MINI 3 pin24

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI CARD CONN 2 & 3

Size	Document Number	Rev
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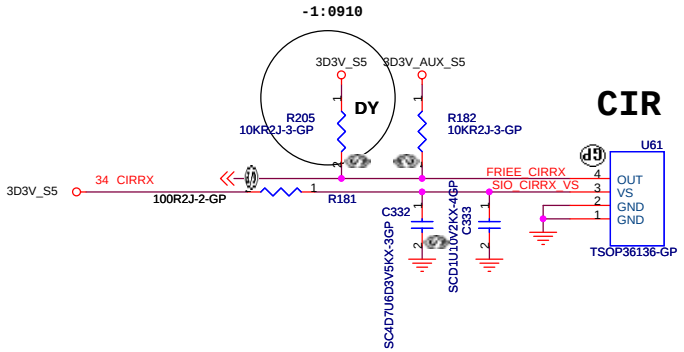
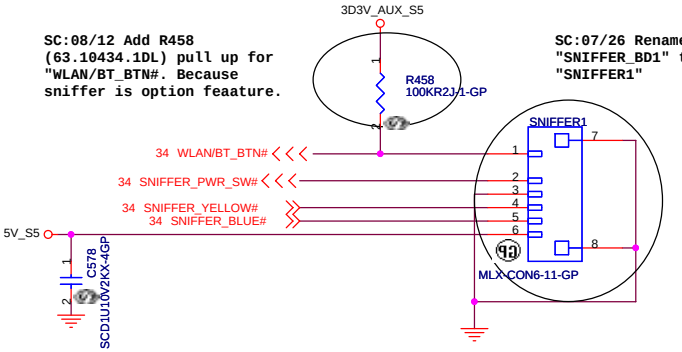
-1:0910

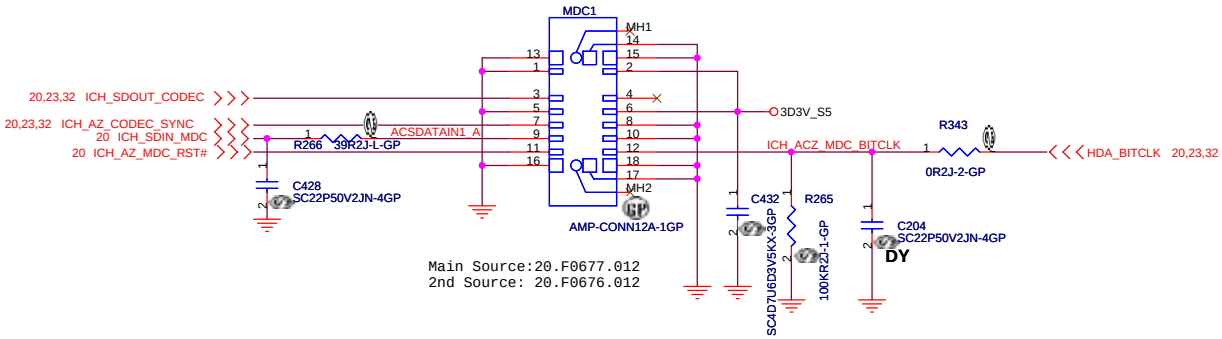
CIR



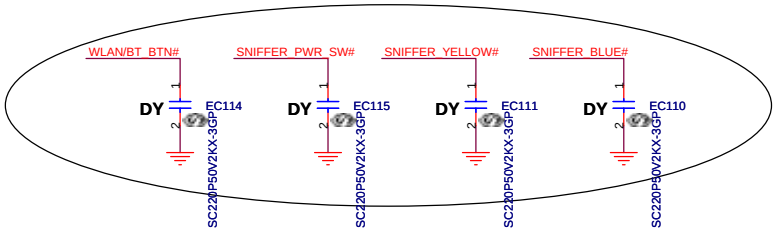
SC:08/12 Add R458 (63.10434.1DL) pull up for "WLAN/BT_BTN#. Because sniffer is option feaature.

SC:07/26 Rename "SNIFFER_BD1" to "SNIFFER1"

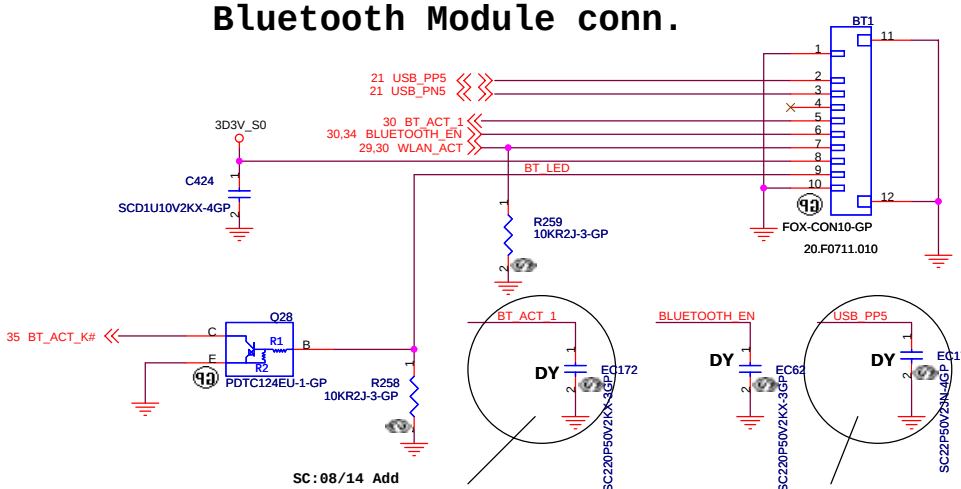




Main Source:20.F0677.012
2nd Source: 20.F0676.012



Bluetooth Module conn.



SC:08/14 Add EC172(78.22124.2FL) on "BT_ACT1" for EMI team request.

SC:08/14 Add EC173(78.22034.1FL) on "USB_PP5" for EMI team request.

SC:08/14 Add EC174(78.22034.1FL) on "USB_PN5" for EMI team request.

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MDC&RJ11 CONN

Size	Document Number	Rev
A3	DS2-Intel	-1

Date: Wednesday, September 12, 2007 Sheet 31 of 47

60ohm 100MHz
3000mA 0.05ohm DC

3D3V_S0

C266 SCD1U10V2KX-4GP
C276 SCD1U10V2KX-4GP
C270 SC1U6D3V2KX-GP

+VDDA

C320 SCD1U10V2KX-4GP
C296 SC1U10V3KX-3GP

R421 5K1R2F-2-GP
R420 39K2R2F-L-GP
AUD_HP1_JD# 33

R154 5K1R2F-2-GP
R158 20KR2J-L2-GP
AUD_HP2_JD# 33
R157 39K2R2F-L-GP
EXT_MIC_JD#

U36

R152 1+3V_RUN_DVDD_CORE3 100KR2J-1-GP
C298 SC1KP50V2KX-1GP

SB:07/10 Change R344 from 33 Ohm to 0 Ohm

20,23,31 HDA_BITCLK
20 ICH_SDIN_CODEC
20,23,31 ICH_SDOUT_CODEC
20,23,31 ICH_AZ_CODEC_SYNC
20 ICH_AZ_CODEC_RST#

R344 0R2J-2-GP
R146 33R2J-2-GP
ICH_AZ_CODEC_BITCLK
SB_AZ_CODEC_SDIN0_R

DVDD_CORE
DVDD_CORE
DVDD
BIT_CLK
SDATA_IN
SDATA_OUT
SYNC
RESET#

AVDD1
AVDD2
SENSE_A
SENSE_B
PORT_A_L
PORT_A_R
VREFOUT_A
PORT_B_L
PORT_B_R
VREFOUT_B
PORT_C_L
PORT_C_R
VREFOUT_C
PORT_D_L
PORT_D_R
VREFOUT_D
PORTE_L
PORTE_R
VREFOUT_E
PORTF_L
PORTF_R
VREFOUT_F
PORTG_L
PORTG_R
PORTH_L
PORTH_R
CD_L
CD_GND
CD_R
PC_BEEP
CAP2
VREFFILT
AVSS1
AVSS2

AUD_SENSE_A
AUD_SENSE_B

TO Audio OP
AUD_HP1_OUT_L
AUD_HP1_OUT_R
AUD_HP1_OUT_L 33
AUD_HP1_OUT_R 33

C292 SC1U10V3KX-3GP
C294 SC1U10V3KX-3GP
INT_MIC
AUD_INT_MIC_L
AUD_INT_MIC_R
AUD_VREFOUT_B
R153 4K7R2J-2-GP

AUD_LINE_OUT_L
AUD_LINE_OUT_R
AUD_LINE_OUT_L 33
AUD_LINE_OUT_R 33

TO Audio OP

AUD_EXT_MIC_L
AUD_EXT_MIC_R
AUD_VREFOUT_E

AUD_HP2_OUT_L 33
AUD_HP2_OUT_R 33

Port A---> HP1
Port E---> Ext Mic
Port D---> Speaker
Port F---> HP2
Port C--->Int Mic

3D3V_S0
U34 DY
VCC OE# A Y GND
74LVC1G125DC-GP
18 AUD_DMIC_CLK_G
AUD_DMIC_CLK
R149 33R2J-2-GP

SB: Change R149 from 63.R0034.1DL to 63.33034.1DL

18 AUD_DMIC_IN0
AUD_DMIC_IN0
R455 200R2F-L-GP
35 SPDIF_D
23 AUD_SPDIF_OUT
AUD_SPDIF_OUT
AUD_DMIC_CLK

VOLUME UP/DMIC_0/GPIO1
VOLUME DN/DMIC_1/GPIO2
SPDIF_IN/GPIO0/DMIC_CLK
SPDIF_OUT
DVSS1
DVSS2

PC BEEP

AUD_PC_BEEP
AUD_BEEP
C267 SCD1U10V2KX-4GP
AUD_CAP2
AUD_VREFFLT
C299 SC1U10V5KX-2GP
C300 SC1U10V5KX-2GP
R412 10KR2J-3-GP

R141 47KR2F-GP
From SB
SB_SPKR 21
R413 47KR2F-GP
KBC_BEEP 34
From EC

SA:0428

STAC9228X5TAEA2-GP 71.09228.00G

AUD_DMIC_CLK_G
EC129 SC22P50V2JN-4GP

ICH_AZ_CODEC_BITCLK
DY EC36 SC22P50V2JN-4GP

SB:06/26 Add EC129(78.22034.1FL) by EMI request

SB:07/02 Change EC36 from ASM to DUMMY

Internal Microphone

-1:09/06 Change Int. MIC from 23.42132.001 to 23.42143.001

INT_MIC
CN4 MICROPHONE-40-GP-U
EC52 SC1KP50V2KX-1GP

Azalia I/F EMI

ICH_SDOUT_CODEC
R145 47R2J-2-GP
DY
ICH_AZ_CODEC_SDOUT1
C263 SCD1U10V2KX-4GP
DY

Azalia I/F EMI

ICH_AZ_CODEC_BITCLK
R144 47R2J-2-GP
DY
ICH_AZ_CODEC_BITCLK1
C265 SCD1U10V2KX-4GP
DY

MIC IN

AUD_VREFOUT_E
R162 4K7R2J-2-GP
R163 4K7R2J-2-GP
C302 SC1U10V3KX-3GP

AUD_EXT_MIC_L
C306 SC1U10V3KX-3GP
MIC_IN_L_2
AUD_EXT_MIC_R
C307 SC1U10V3KX-3GP
MIC_IN_R_2
R169 0R3-0-U-GP
R168 0R3-0-U-GP
MIC_IN_L_C
MIC_IN_R_C

SB:07/02 Change R168 from 63.R0034.1DL to 63.00000.00L

600ohm 100MHz
200mA 0.5ohm DC

EXT_MIC_JD#
MIC1
EC48 SC100P50V2JN-3GP
EC49 SC100P50V2JN-3GP
AUDIO-JK89-GP-U

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

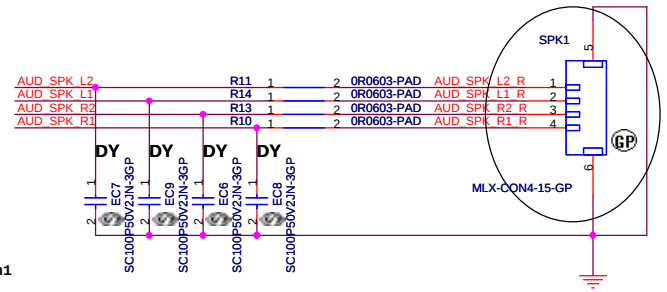
Title: AUDIO CODEC STAC9228

Size	Document Number	Rev
A3	DS2-Intel	-1

Date: Wednesday, September 12, 2007 Sheet 32 of 47

Speaker

SC:08/11 Change SPK1 pin define that follow ME request

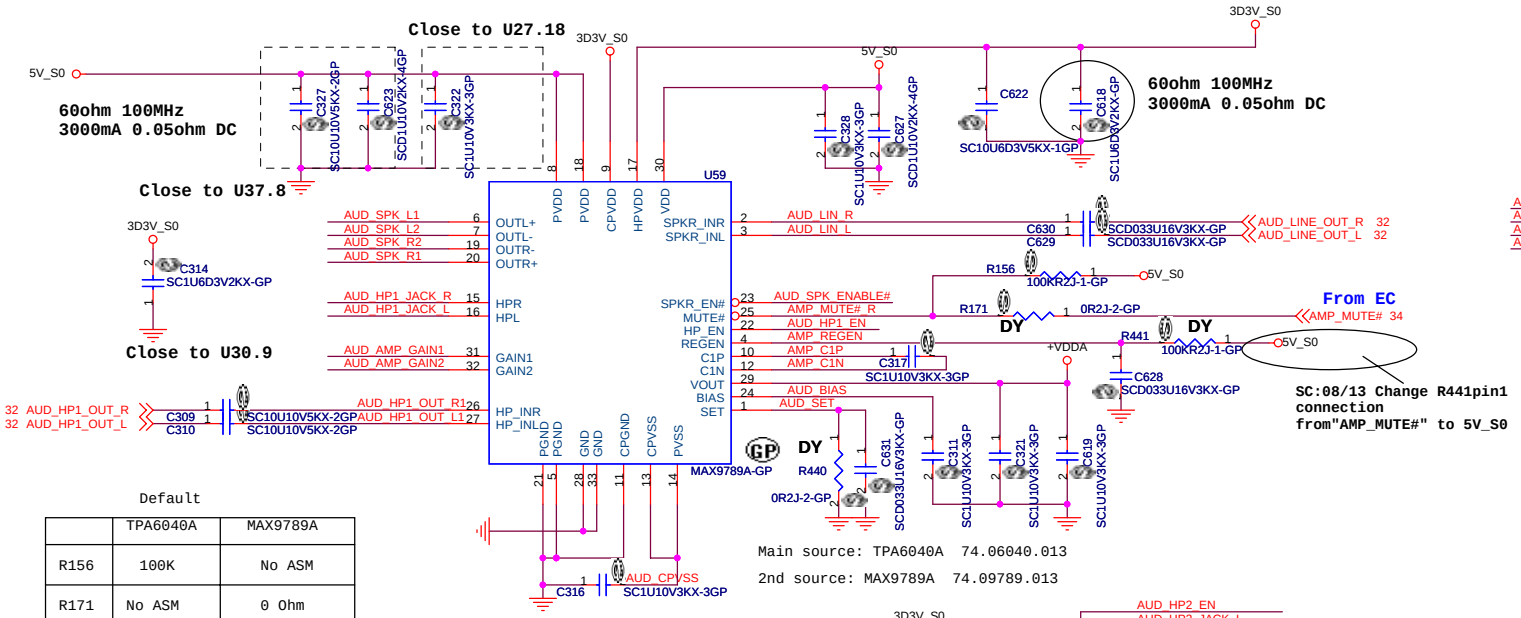


Close to U27.18

60ohm 100MHz
3000mA 0.05ohm DC

Close to U37.8

Close to U30.9



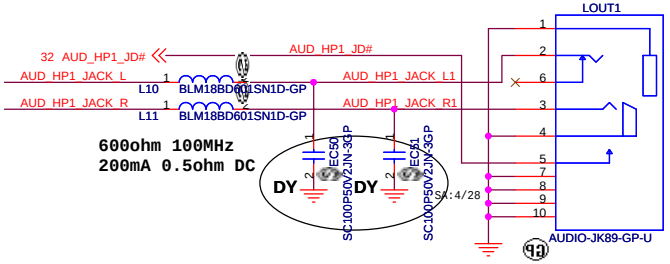
Default

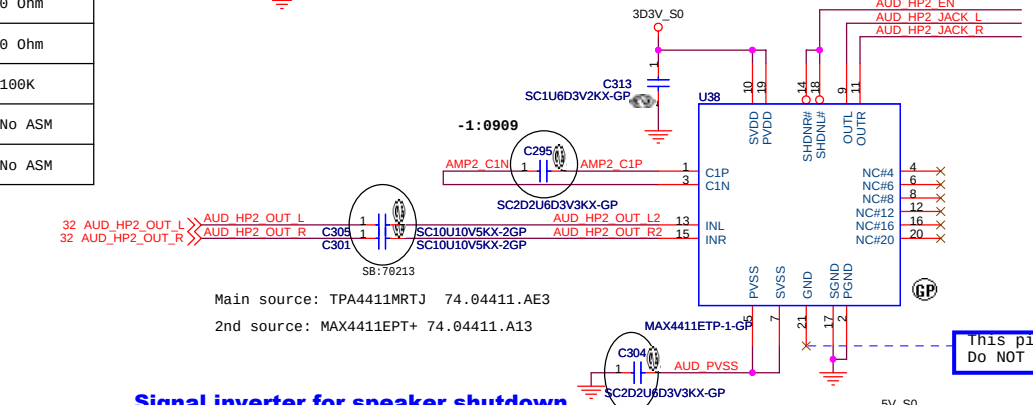
	TPA6040A	MAX9789A
R156	100K	No ASM
R171	No ASM	0 Ohm
R440	No ASM	0 Ohm
R441	No ASM	100K
C631	0.33uF	No ASM
C628	0.33uF	No ASM

Main source: TPA6040A 74.06040.013

2nd source: MAX9789A 74.09789.013

LINE1 OUT



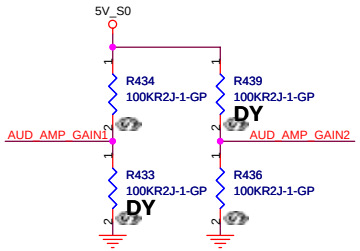


Main source: TPA4411MRTJ 74.04411.AE3

2nd source: MAX4411EPT+ 74.04411.A13

LINE2 OUT

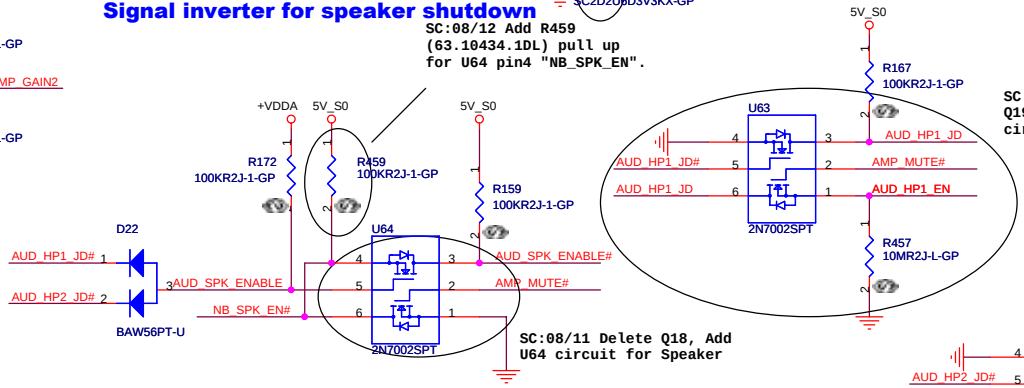
GAIN SETTING

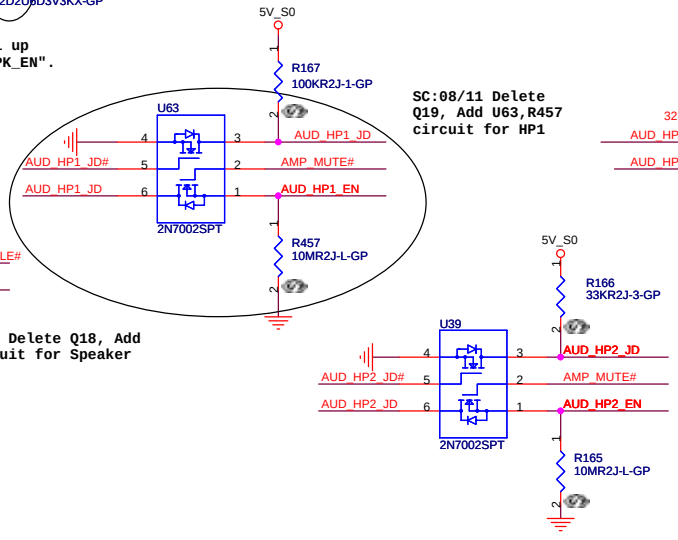


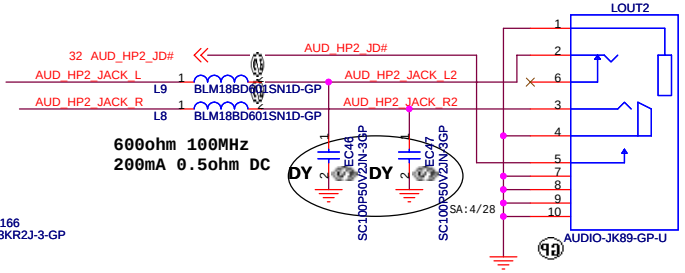
GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

Signal inverter for speaker shutdown

SC:08/12 Add R459 (63.10434.1DL) pull up for U64 pin4 "NB_SPK_EN".







<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO AMP/SPEAKER

Size: A3 | Document Number: DS2-Intel | Rev: -1

Date: Wednesday, September 12, 2007 | Sheet 33 of 47

WPC8763L STRAP PIN

JEN0 (Pin 24)	JENK (Pin 53)	Functionality of Pins 17, 20, 21, 23 25, 27	Functionality of Pins 47, 48, 50, 51, 52
NO PD RES		GPIO Port	Keyboard Scan
10K PD	NO PD	JTAG signals	Keyboard Scan
NO PD	10K PD	GPIO Port	JTAG signals

TRIS#(Pin 110) TRI-STATE

Forces the device to float all its output and I/O pins,if an external 10 KΩ pull-down resistor is conected.

BADDR1-0 (PIN 111, 112) I/O Base Address.
10KΩ external pull-down resistor on BADDR1: Core defined

SB:06/24 Change R104 from 63.10334.1DL to 63.47234.1DL.Base on Winbond FAE recommend to fix system will hang up after Thermal T8 shutdown

SHBM PIPN83 Shared Host BIOS Memory.
HIGH:NO SHARED(internal resistor)
LOW:SHARED BIOS memory.

SB:06/27 Change R98 from 63.10334.1DL to 63.47234.1DL

PLACE CAP NEAR PIN80 AND PIN102

PLACE CAP NEAR PIN46,19,115,76,88,104

-1:08/30 Change Pin10 from NC to be"WWAN_RF_EN"

-1:08/30 Change Pin11 from NC to be"HDD_5V_EN"

-1: 08/29 change Pin24 from "WWAN_RF_EN" to NC, because pin24 is H/W straping pin. it has H/W concern.

SC:08/03 Change Pin27 from"BLON_OUT" to" LCD_TST_EN", delete TP45 test pad.

-1:08/29 Change U22 pin110 define from NC to"USB_PWR_EN" or USB power control.

KBC DEBUG POINT

<-----BATTERY

FOR Thermal AND Capacity Button Module

MB VERSION ID

	VER0	VER1
SA	0	0
SB	0	1
SC	1	0
-1	1	1

WPC8763L XTAL

-1:0912

KBC CLK EMI

ADIA:to Charger
ACDC_ID:from Adapter Conn
KBC_PWRBTN#:from power button
BAT_IN#:from Battery Conn
DC_BATFULL#:for Battery charge LED 1
WLAN_TEST:for WKS test WLAN LED
AD_OFF:enable AC adapter power source
CHARGE_LED#:for Battery charge LED 2
WLAN/BT_BTN#:from Wlan on/off button
GMCH_BL_ON:Sense The Backlight On/Off Status from VGA Chip
WIRELESS_EN:Disable/Enable Wireless Module
BLUETOOTH_EN:Disable/Enable Bluetooth
USB_PWR_EN#:to on/off USB power switch
CCD_ON:Webcam power on/off
AC_IN#:From Charge

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC_Winbond WPC8763L
Size: A2 | Document Number: DS2-Intel | Rev: -1
Date: Wednesday, September 12, 2007 | Sheet 34 of 47

SPI

SA:04/22 change C532,C533,C534 connection power from "3D3V_S0" to "3D3V_AUX_S5"

SPI FLASH ROM

8M Bits

EMI REQUEST

Power Dash Board to Board CONN

-1:09/02 Change CN2(Power Dash Board) pin assignment.

Main Source:20.K0227.008
2nd Source: 20.K0237.008

LED Board to Board CONN

-1:09/02 Change CN3(LED Board) pin assignment.

SC:08/09 Add EC148(78.22124.2FL) for EMI request, deault is dummy.

SC:08/11 Add EC163 on "LID_CLOSE" for RF team Request.

SC:08/09 Add EC149(78.22124.2FL) for EMI request, deault is dummy.

SC:08/09 Add EC150(78.22124.2FL) for EMI request, deault is dummy.

Right I/O Board to Board CONN

CONN 28PIN

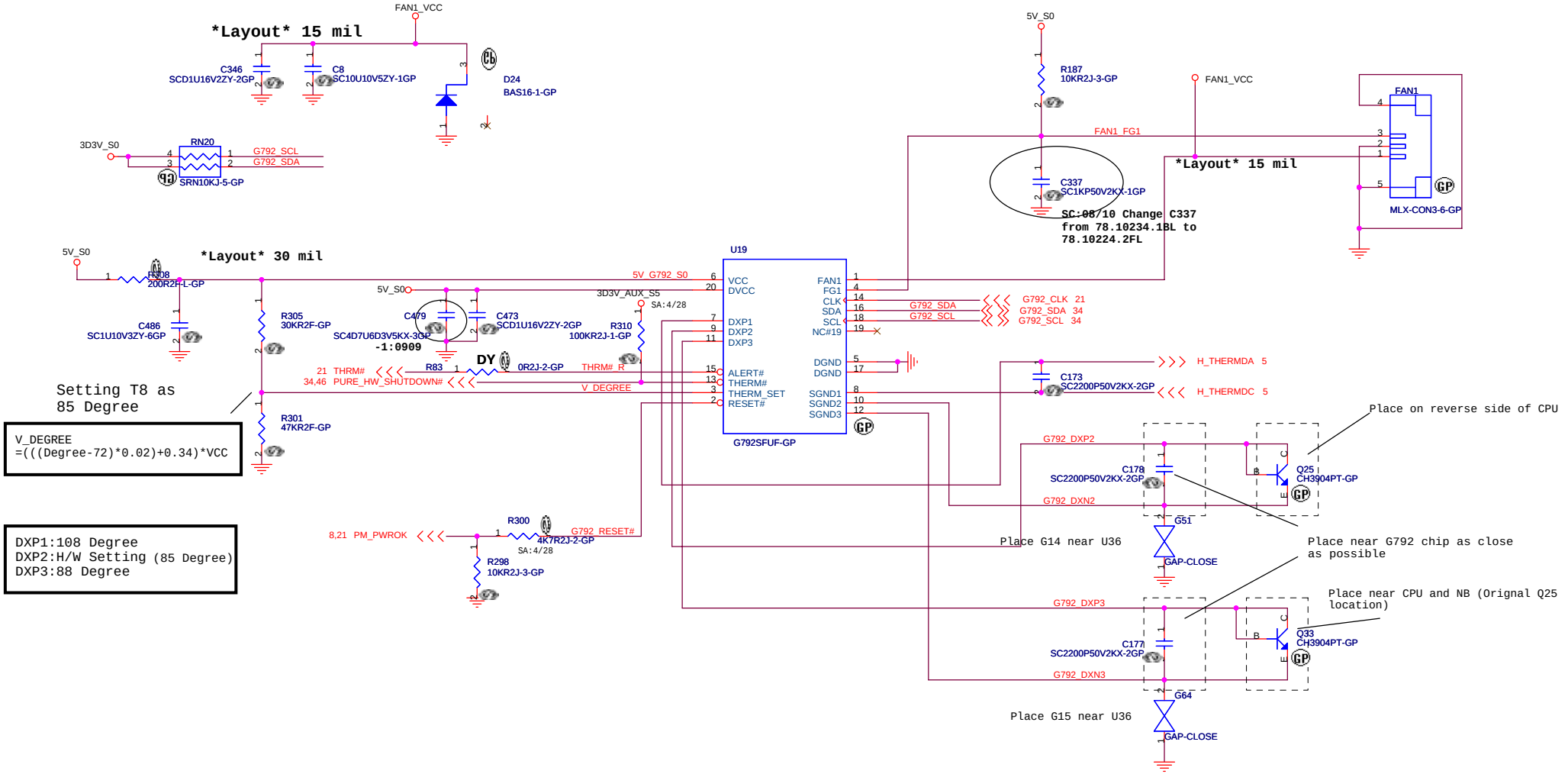
-1:08/29 Rename CN6 pin2,pin4 power net become "5V_USB2_S5".

-1:08/31 Change CN6 pin26 from "5V_S5" to "5V_USB2_S5"

-1:08/29 Add U65 power switch to controll "5V_USB2_S5".

<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: FWH and Board to Board CONN		
Size: A3	Document Number: DS2-Intel	Rev: -1
Date: Wednesday, September 12, 2007	Sheet 35 of 47	



<Core Design>

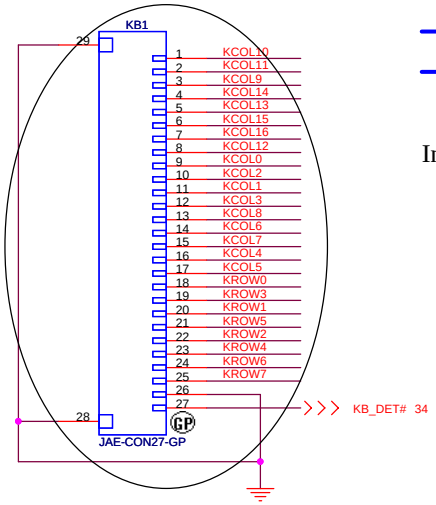
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Thermal/Fan Controllor G792***

Size	Document Number	Rev
A3	DS2-Intel	-1

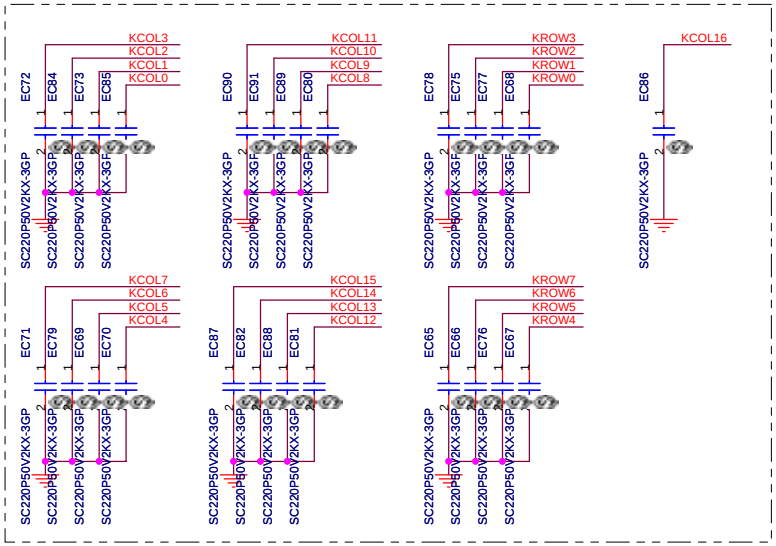
Date: Wednesday, September 12, 2007 Sheet 36 of 47

SB:06/27 Change K/B connector from 20.F0694.025
to 20.K0291.027 .

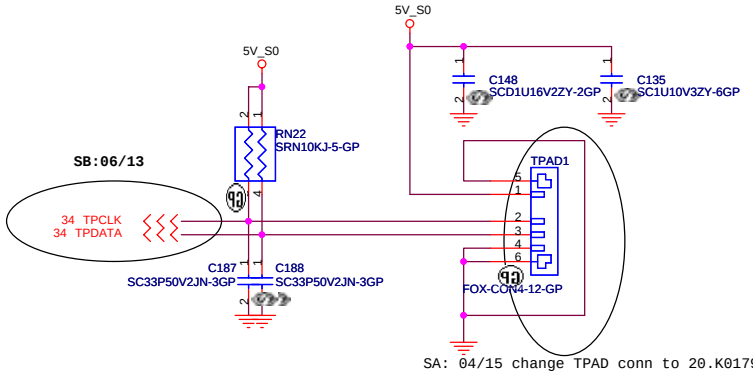


Internal KeyBoard Connector

for EMI

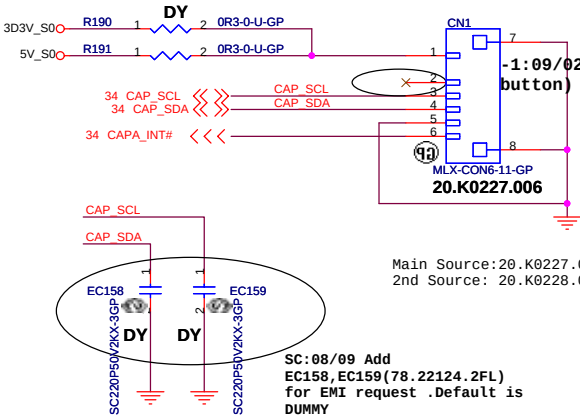


TouchPad Connector



SA: 04/15 change TPAD conn to 20.K0179.004

CAPACITY BUTTON



-1:09/02 Change CN1(Capacity button) pin2 from GND to NC

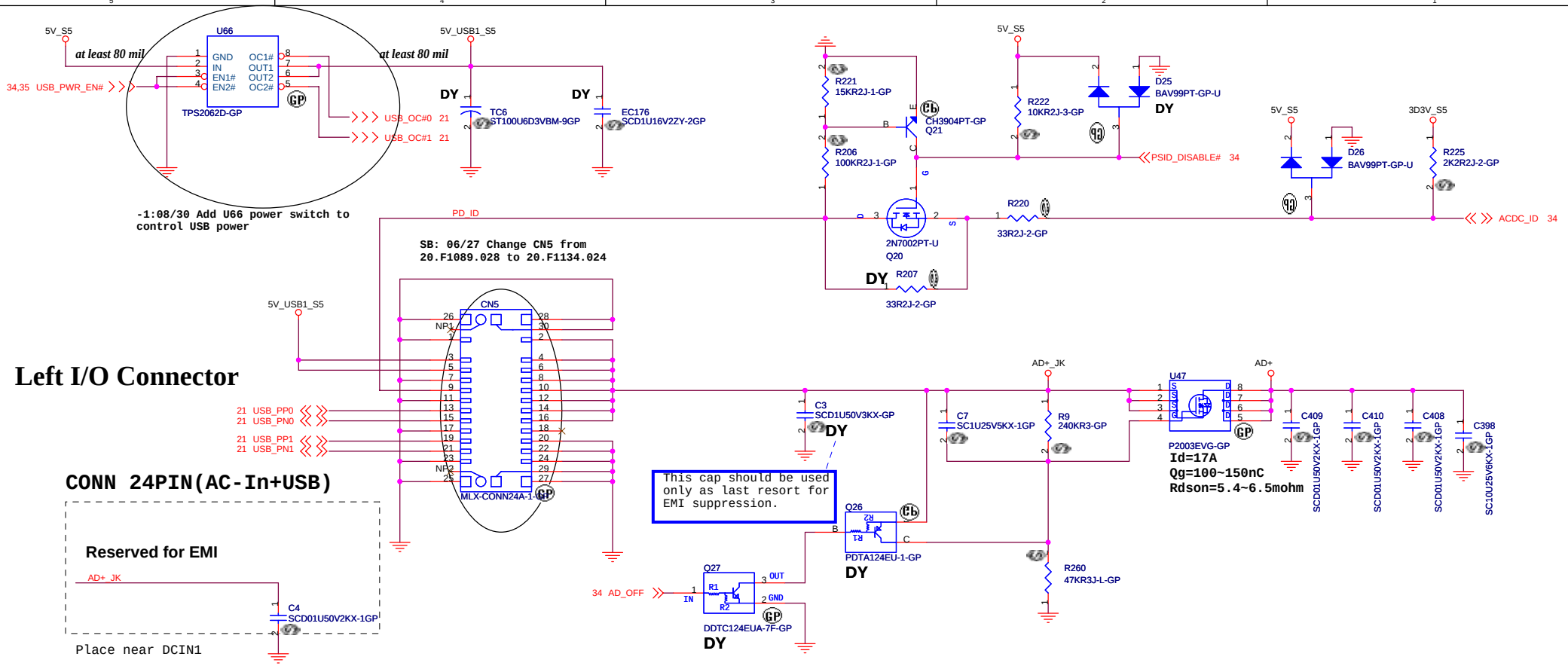
Main Source:20.K0227.006
2nd Source: 20.K0228.006

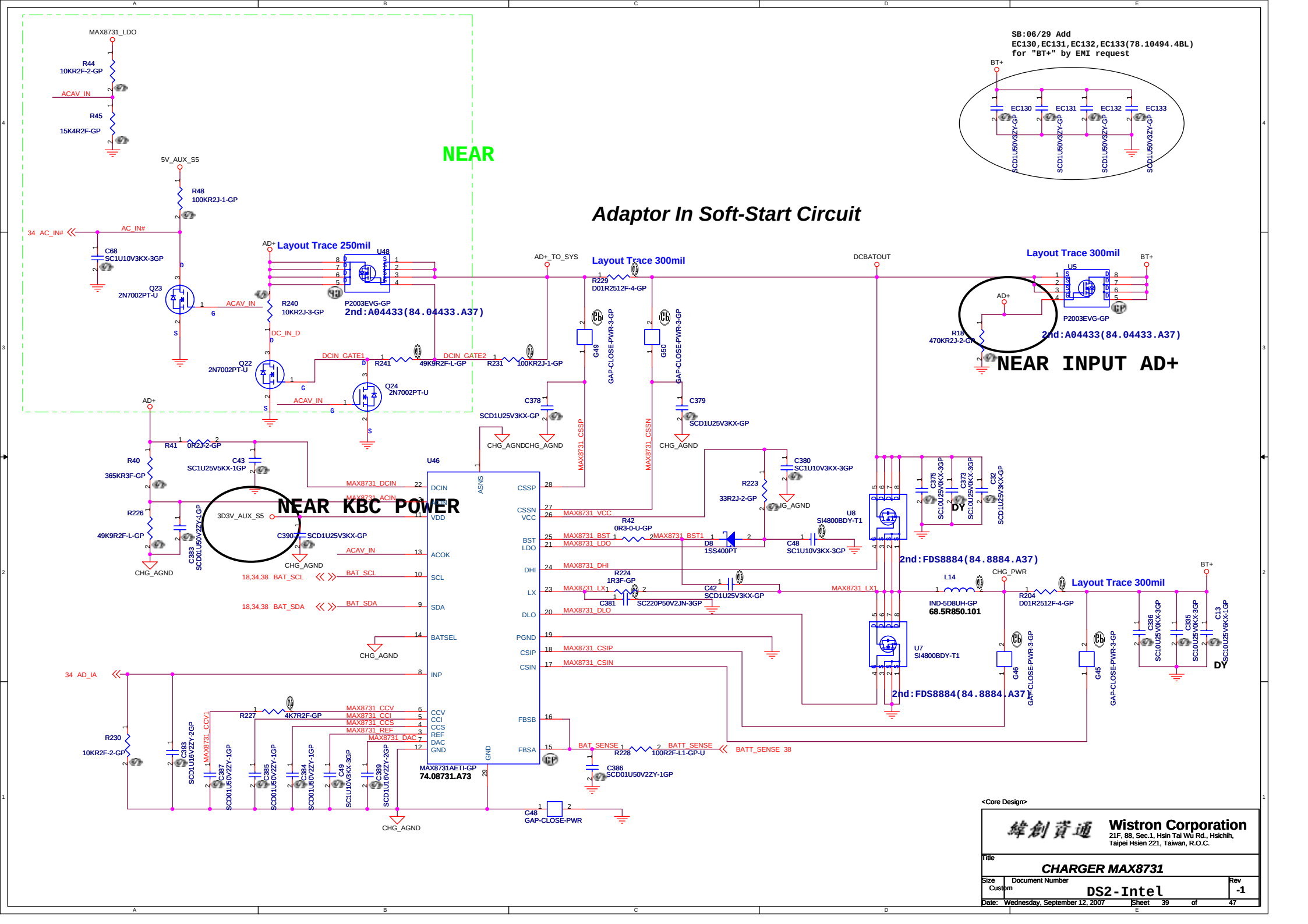
SC:08/09 Add
EC158,EC159(78.22124.2FL)
for EMI request .Default is
DUMMY

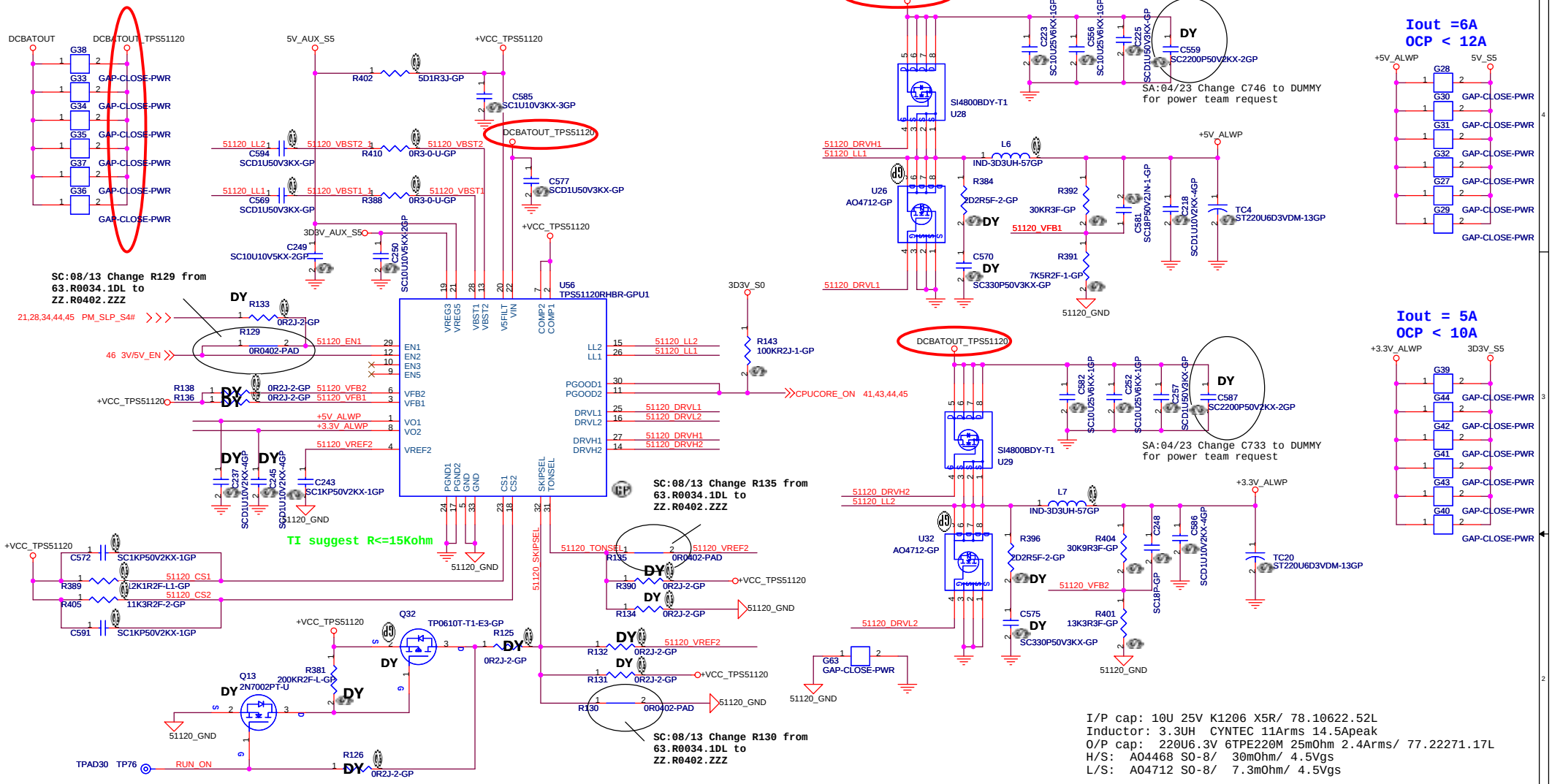
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	KeyBoard-CONN	
Size A3	Document Number DS2-Intel	Rev -1
Date: Wednesday, September 12, 2007	Sheet 37 of 47	


5V_S5
at least 80 mil
U66
GND
IN
EN1#
EN2#
OC1#
OUT1
OUT2
OC2#
TPS2062D-GP
34,35 USB_PWR_EN#
5V_USB1_S5
at least 80 mil
USB_OC#0 21
USB_OC#1 21
DY
TC6
ST100U6D3VBM-9GP
EC176
SCD1U16V2ZY-2GP
-1:08/30 Add U66 power switch to control USB power
PD_ID
R221
15KR2J-1-GP
R206
100KR2J-1-GP
CH3904PT-GP
Q21
R222
10KR2J-3-GP
D25
BAV99PT-GP-U
PSID_DISABLE# 34
D26
BAV99PT-GP-U
R225
2K2R2J-2-GP
ACDC_ID 34
2N7002PT-U
Q20
R220
33R2J-2-GP
R207
33R2J-2-GP
SB: 06/27 Change CN5 from 20.F1089.028 to 20.F1134.024
CN5
MLX-CONN24A-1-GP
21 USB_PP0
21 USB_PN0
21 USB_PP1
21 USB_PN1
Left I/O Connector
CONN 24PIN(AC-In+USB)
Reserved for EMI
AD+_JK
C4
SCD01U50V2KX-1GP
Place near DCIN1
C3
SCD1U50V3KX-GP
This cap should be used only as last resort for EMI suppression.
Q26
PDTA124EU-1-GP
Q27
DDTC124EUA-7F-GP
34 AD_OFF
C7
SC1U25V5KX-1GP
R9
240KR3-GP
R260
47KR3J-L-GP
U47
P2003EVG-GP
Id=17A
Qg=100~150nC
Rdson=5.4~6.5mohm
AD+
C409
C410
C408
C398
SCD01U50V2KX-1GP
SC10U25V6KX-1GP
Left I/O Board to Board CONN
Batt Connecter
BATT1
SYN-CON9-1-GP-U1
PBAT_ALARM#
PBAT_PRES1#
PBAT_SMBDAT1
PBAT_SMBCLK1
TP17
R22
100R2J-2-GP
RN1
SRN100J-3-GP
SB:07/09 Change R21 from 100K to 470K for power team request
R21
470KR2J-2-GP
3D3V_AUX_S5
BAT_IN# 34
BAT_SDA 18,34,39
BAT_SCL 18,34,39
BT+
R1
0R0603-PAD
BATT_SENSE 39
C2
SCD1U50V3KX-GP
C1
SC2200P50V2KX-2GP
Battery CONN. Main source:20.80953.009
2nd source:20.80626.009
D23
D1
D6
D2
BAT_SCL
BAT_SDA
BAT_IN#
PBAT_ALARM#
BAV99PT-GP-U
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AD/BATT CONN
Size A3
Document Number
DS2-Intel
Rev -1
Date: Wednesday, September 12, 2007
Sheet 38 of 47


SB:06/29 Add
EC130,EC131,EC132,EC133(78.10494.4BL)
for "BT+" by EMI request
NEAR
Adaptor In Soft-Start Circuit
NEAR INPUT AD+
NEAR KBC POWER
Layout Trace 250mil
Layout Trace 300mil
2nd:A04433(84.04433.A37)
2nd:FDS8884(84.8884.A37)
MAX8731_LDO
5V_AUX_S5
3D3V_AUX_S5
AD+
BT+
DCBATOUT
AD+_TO_SYS
CHG_AGND
CHG_PWR
MAX8731AETI-GP
74.08731.A73
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CHARGER MAX8731
DS2-Intel
Wednesday, September 12, 2007
Sheet 39 of 47



Vout=1V*(R1+R2)/R2

	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 580k/CH2	280k/CH1 430k/CH2	220k/CH1 330k/CH2	180k/CH1 2870k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1,EN2	Switcher OFF	not use	Switchr ON	Switcher ON
EN3,EN5	LDO OFF	not use	LDO ON	VREG3 on

<Core Design>

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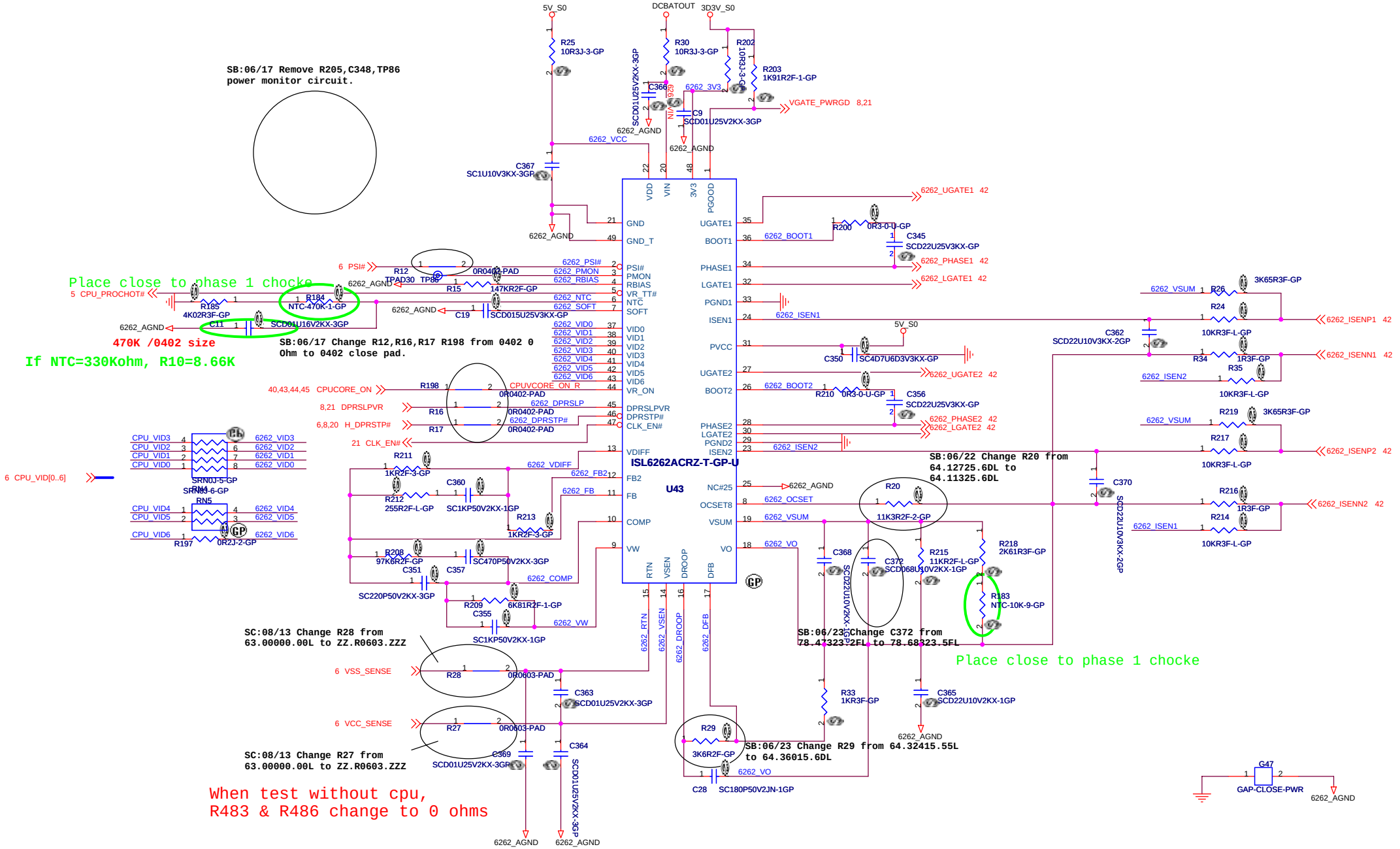
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC 3.3V & 5V

Size: Custom | Document Number: DS2-Intel | Rev: -1

Date: Wednesday, September 12, 2007 | Sheet 40 of 47



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: DC-DC VCCCPUCORE 1/2

Size: A3 | Document Number: DS2-Intel | Rev: -1

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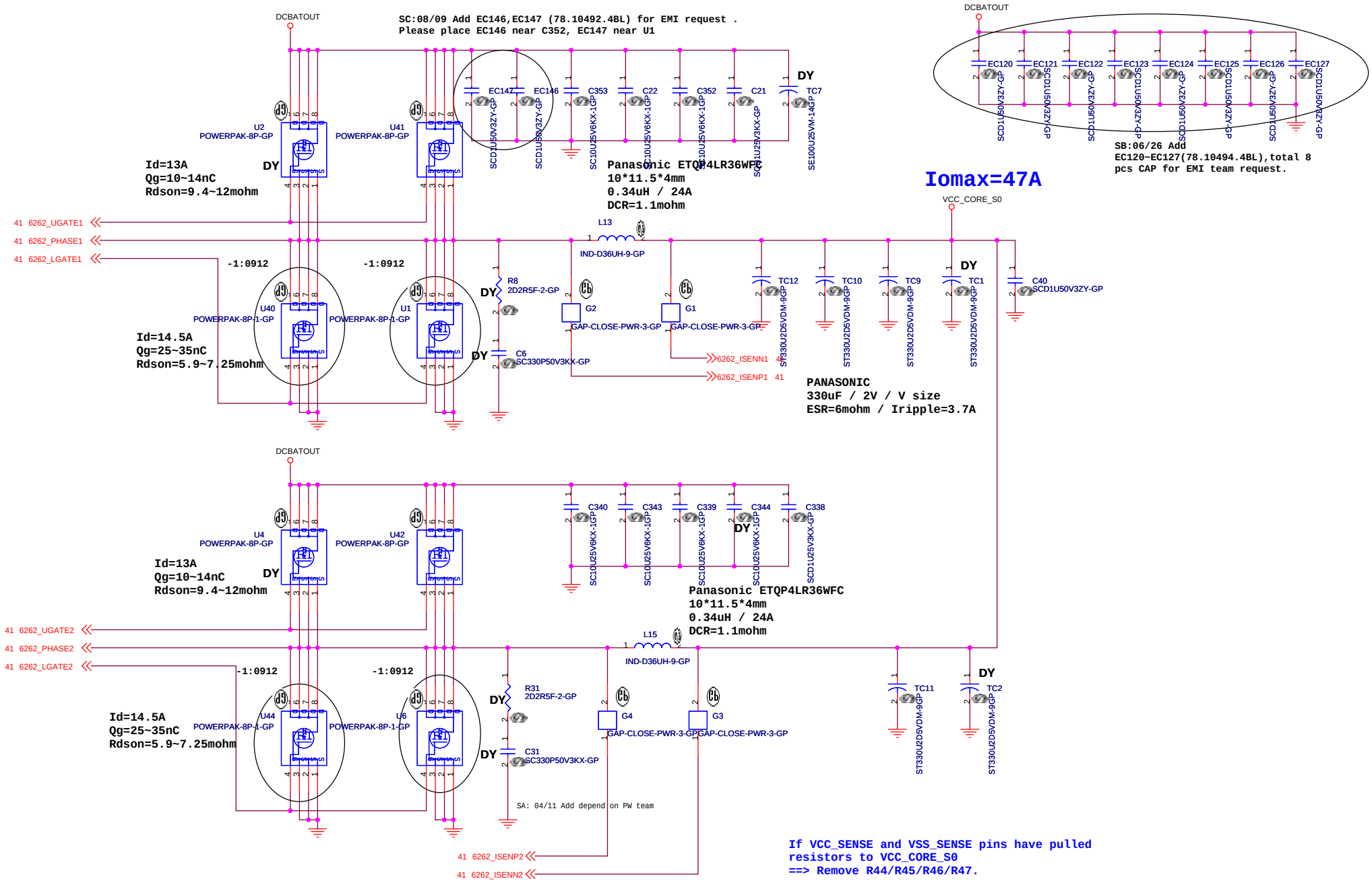

<Core Design>

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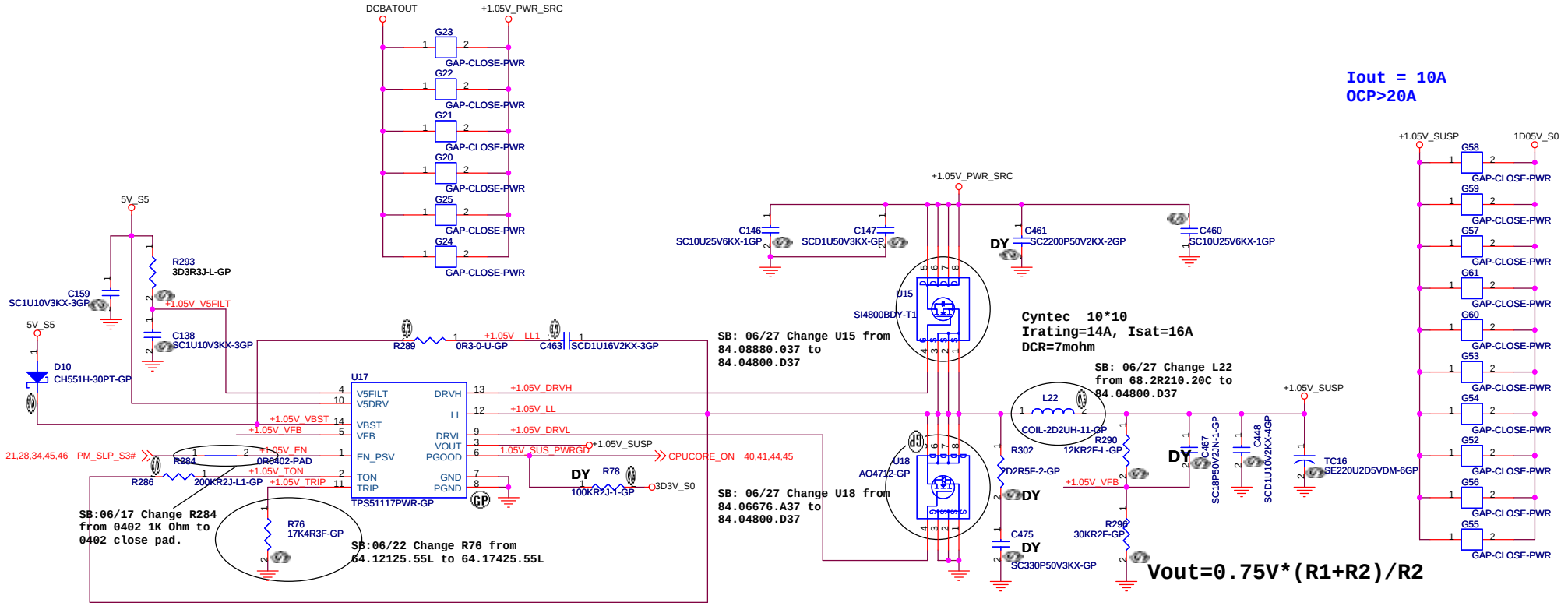
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC-DC VCCCPUCORE 2/2

Size	Document Number	Rev
A3	DS2-Intel	-1

Date: Wednesday, September 12, 2007 Sheet 42 of 47



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH M MPL73-1R5 Delta 9Arms 18Apeak / 68.1R510.10I
O/P cap: 220U 4V 4TPE220MF 15mOhm 3.1Arms/ 77.22271.161
H/S & L/S: FDS8884 SO-8/ 30mOhm/ 4.5Vgs/ 84.08884.037
L/S: FDS8896 SO-8/ 7.3mOhm/ 4.5Vgs/ 84.08896.037
Ton = 200KOhm --> 330KHz

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: DCDC 1.05V

Size	Document Number	Rev
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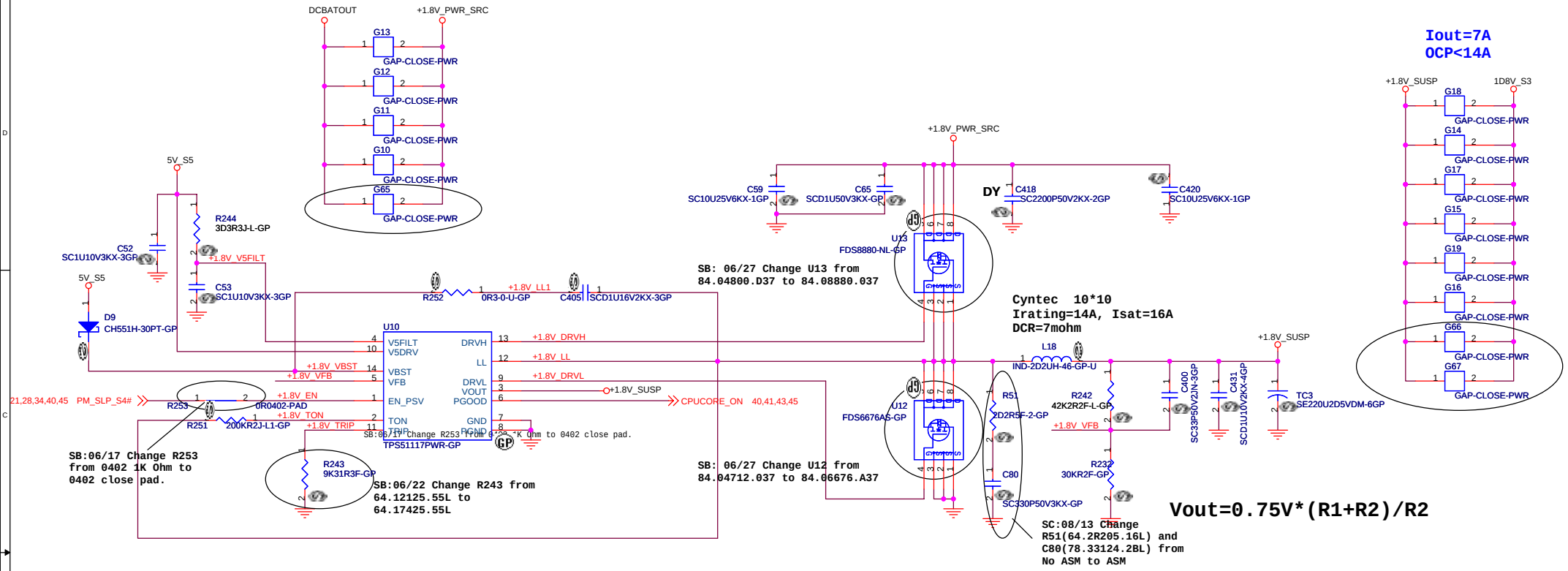

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH M MPL73-1R5 Delta 9Arms 18Apeak / 68.1R510.10I
O/P cap: 220U 4V 4TPE220MF 15mOhm 3.1Arms/ 77.22271.161
H/S & L/S: FDS8884 SO-8/ 30mOhm/ 4.5Vgs/ 84.08884.037
L/S: FDS8896 SO-8/ 7.3mOhm/ 4.5Vgs/ 84.08896.037
Ton = 200KOhm --> 330KHz

<Variant Name>

緯創資通 Wistron Corporation
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Title	DC/DC 1D8V	
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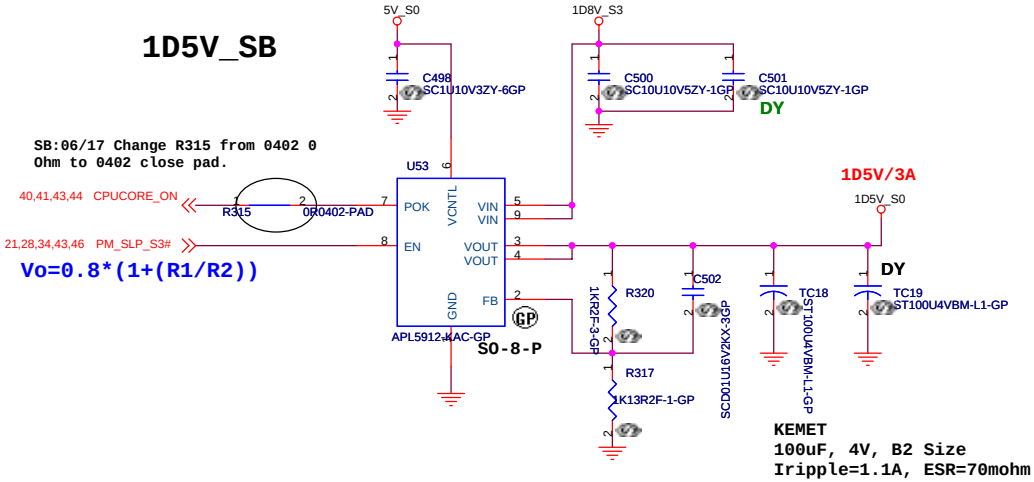
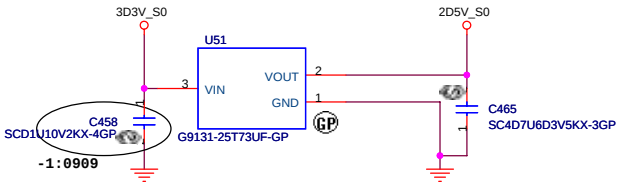
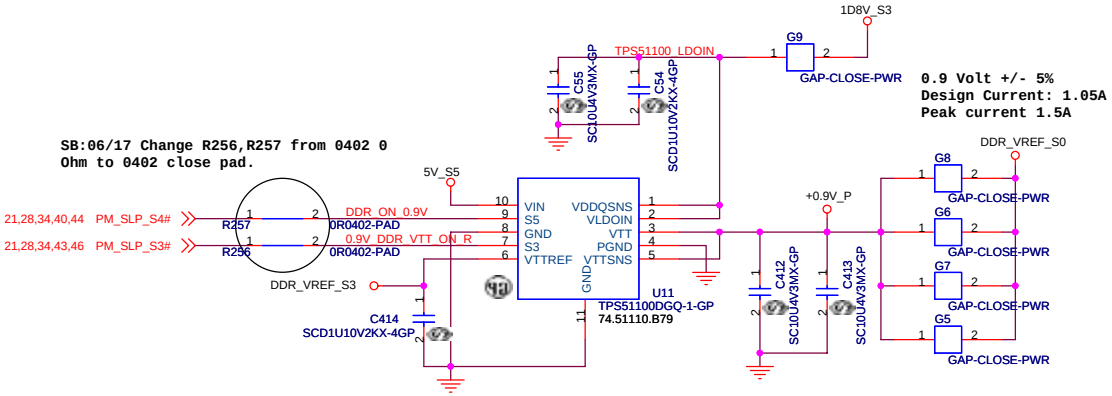
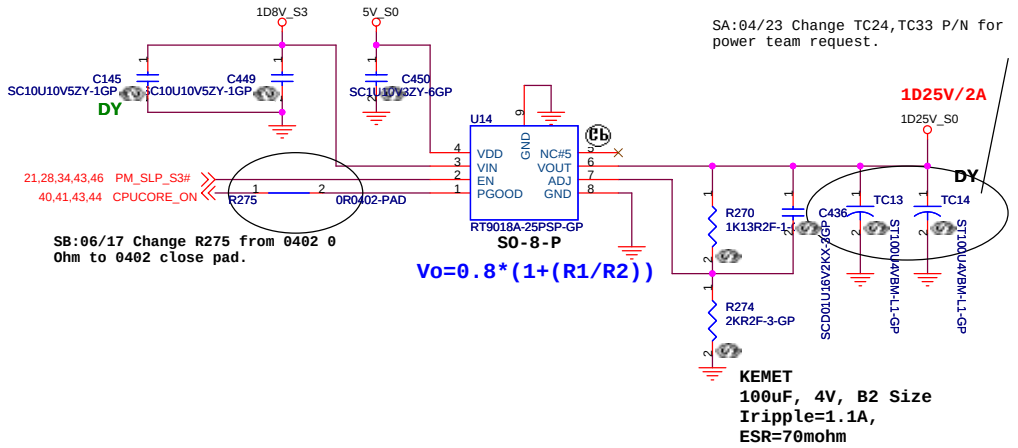
1D5V_SB





SSID = PWR.Plane.Regulator_0.9V





<Variant Name>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title	DC/DC 1D8V	
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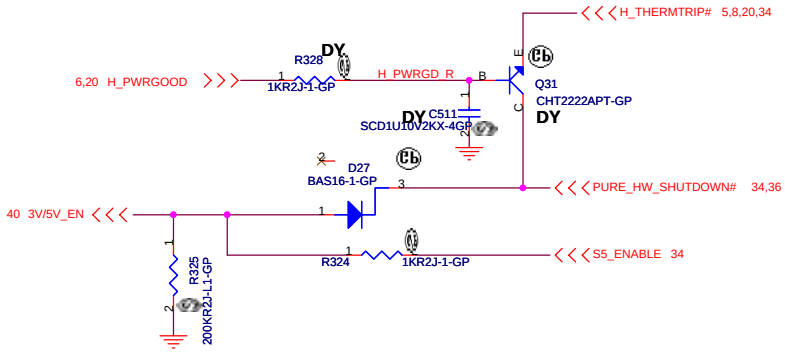
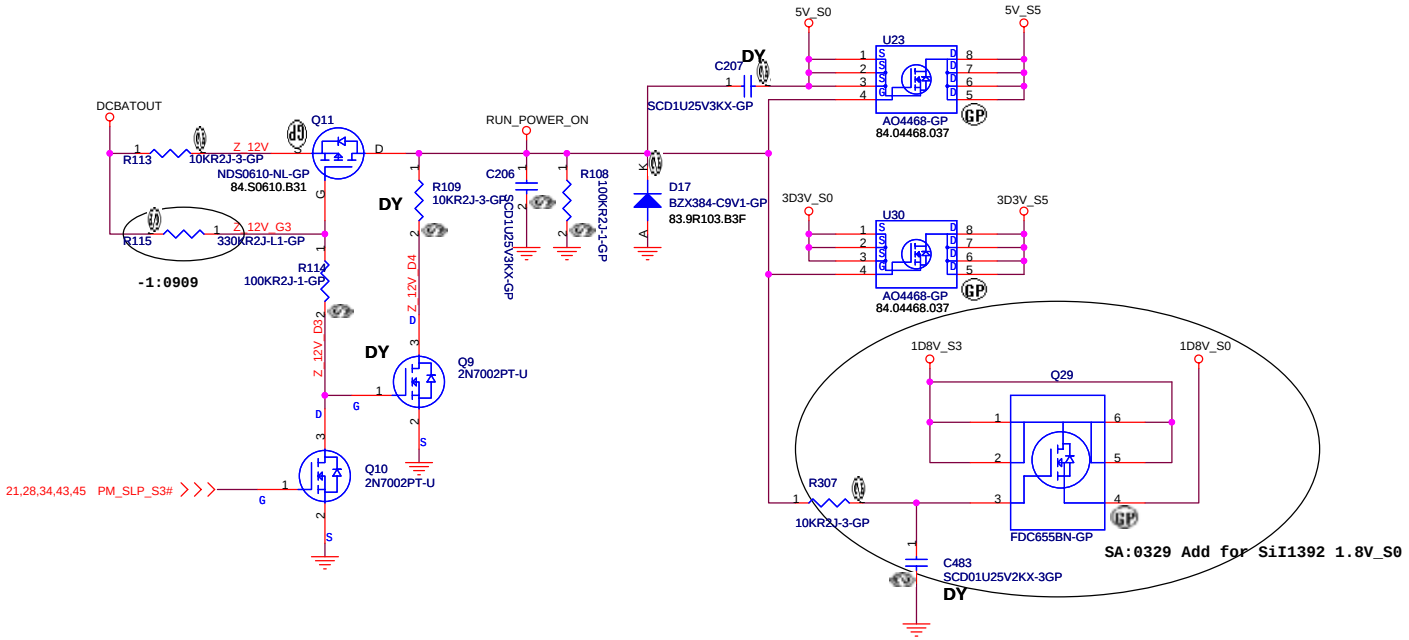


Run Power



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PWRPLANE&RESETLOGIC***

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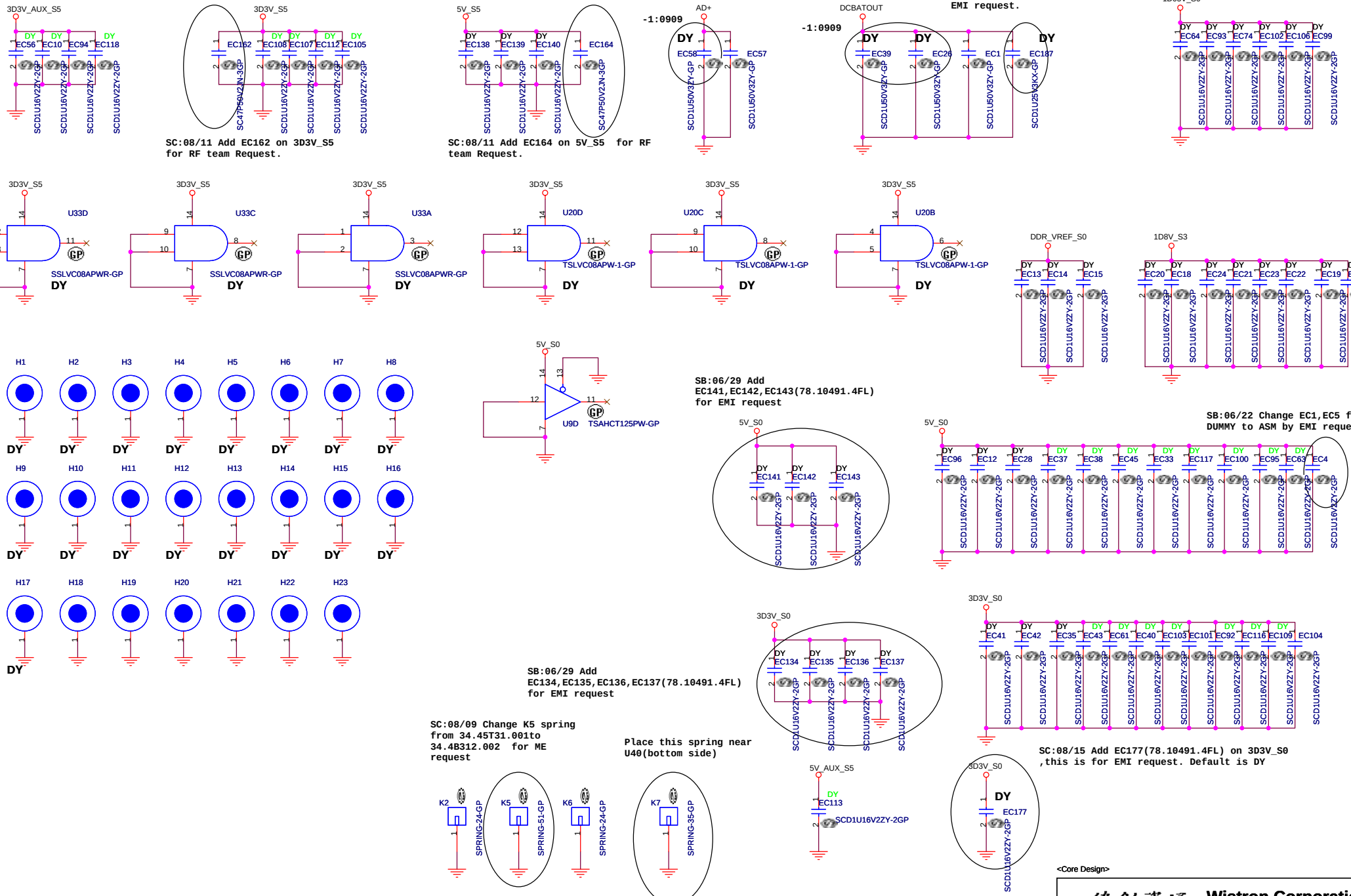
-1:0904 Add EC187(78.10422.2BL) for DCBATOUT decoupling , this is for EMI request.
SC:08/11 Add EC162 on 3D3V_S5 for RF team Request.
SC:08/11 Add EC164 on 5V_S5 for RF team Request.
SB:06/29 Add EC141,EC142,EC143(78.10491.4FL) for EMI request
SB:06/22 Change EC1,EC5 from DUMMY to ASM by EMI request.
SB:06/29 Add EC134,EC135,EC136,EC137(78.10491.4FL) for EMI request
SC:08/09 Change K5 spring from 34.45T31.001to 34.4B312.002 for ME request
Place this spring near U40(bottom side)
SC:08/11 Change K7 from 34.39S07.001 to 34.41P18.001.This change is for EMI request
SC:08/15 Add EC177(78.10491.4FL) on 3D3V_S0 ,this is for EMI request. Default is DY
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
MISC
Size A3
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DS2-Intel
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Date: Wednesday, September 12, 2007
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